SHARED DATA ACQUISITION SYSTEM FOR REAL-TIME POWER SYSTEMS APPLICATIONS

by

Yi-Fang Hsu

Presented to the Faculty of the Graduate School of

The University of Texas at Arlington in Partial Fulfillment

of the Requirements

for the Degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

THE UNIVERSITY OF TEXAS AT ARLINGTON

August 2005

ACKNOWLEDGEMENTS

Sincere appreciation is expressed to Doctors Bei Gou, Wei-Jen Lee, and Raymond R. Shoults, for serving as members of the author's graduate committee. The author would like to express appreciation and gratitude to his supervising professor, Dr. Bei Gou and Dr. Qing Zhao for their guidance and support Special appreciation for those friends I have known during my master studies here in UTA and ACC. The author's parents are the primary source of inspiration and support during his education. Finally, The author would like to thank everybody who has in some way helped him during the writing of this thesis.

April 15, 2005

ABSTRACT

SHARED DATA ACQUISITION SYSTEM FOR REAL-TIME

POWER SYSTEMS APPLICATIONS

Publication No. _____

Yi Fang Hsu, M.S.

The University of Texas at Arlington, 2005

Supervising Professor: Bei Gou

Digital signal processing chip (DSP's) can be used to perform data analysis computation and have very good performance in real-time system. Digital filters can be designed with consideration of both magnitude and phase responses for digital re-sampling in power system applications. The design consists of two parts: magnitude approximation and group delay compensation. It compromises between the amount of calculation needed to implement the filters and the performance of the filters, which makes the filters good candidates for both real-time and offline applications.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

Table Page

CHAPTER 1

INTRODUCTION

Electric power generation in the United States is changing from a regulated industry to a competitive industry[1]. Reliable power system control and monitoring solutions with low cost and high performance are highly demanded in deregulated power industry. The power industry restructuring is breaking the vertically integrated utility into competitive entities and introducing competition into electric power markets in order to improve economic efficiency [2]. Like other industries, cost-down is a major issue and strategy for every electricity seller, distributor and transmission service provider. However, the electric power industry has been an investment intensive industry and relatively stable. Today, the industry has been undergoing immense changes. At present, in a substation, a large amount of expensive and traditional control and monitor equipments are installed to provide power system security and operation reliability. With the progress made in the digital signal processing and telecommunication technologies [3], substation automation solutions with high performance can be designed with lower cost.

1.1 Conventional Data transmitting System

In traditional power system, Intelligent Electronic Devices (IED) can e electromechanical, solid-state, or both. Originally, all components were of the electromechanical type, and these are still in wide use. Current Transformers (CT) and the Potential Transformers (PT) are installed in the switch yard and convert high voltage and high current signals into low voltage and low current signals. These analog voltage and current signals are sent to the equipment room a few hundred meters away through cables to be digitized and processed by the IEDs [3][4]. There are several disvantages in conventional signal transmitting and processing approach. First, the analog signals are distorted and attenuated easily. Second, the transmitting system is expensive and complicated. Third, the data acquire system is independent everywhere. The whole system data analysis and communication are very difficult.

1.2 Digital Shared Data Acquisition System

Fortunately, a shared data acquisition system can be developed and directly placed in the switchyard. It digitizes analog voltage and current signals on multiple channels and sends the aggregated digital data to the equipment room through high speed data communication system, such as optical fiber or even air for wireless communications [4][6].

Thus, Radical cost down pressure from customers and market competition. The digital communication is an mature and hot technology. In addition, the electrical isolation between the high voltage switchyard and low voltage control equipment are naturally obtained if the carrier is optical fiber and wireless medium. Furthermore, this data acquisition system can be shared by several IEDs in the substations so that the IEDs can be built simply on general purpose microprocessor or DSP chip and the cost will be even lower.

Different power system applications may use different sample rate [7]. Applications, such as fault recorder, use higher sample rate; however the RTUs may use lower sample rate. In order to be shared by different IEDs, the shared data acquisition system must be able to provide data with multiple data rates. A simple approach to achieve this is to digitize the analog signal at a high sample rate in order to keep as more information on harmonics as possible. It then re-samples the data into sets of data with different sample rates. In IEEE report on COMTRADE [6], a digital re-sampling solution is proposed to convert the data captured by the data recorder for offline study or the IEDs testing. For both real-time and offline digital resampling, digital filters are required to prevent signal alias from happening [8].

The design of the digital filter for digital re-sampling is critical. Above all, the magnitude response needs to meet the specification in order to filter out unwanted signal components while keeping the interested components. Meanwhile, the phase response of the filter for the interested bandwidth needs to be linear so that the output signal wave shape is not distorted from the input signal. In [5], it reported that the

nonlinear phase response from the digital or analog filter has caused notable signal distortion in the PMU applications for WAMS. In addition, for real-time applications, the order of the filter needs to be kept as low as possible to minimize computation time or to decrease complexity in hardware implementation. A design of digital filters with both satisfying magnitude response and constant group delay property within interested bandwidth is presented in this paper.

CHAPTER 2

A PROPOSED DATA TRANSMISSION SOLUTION FOR SUBSTATION AUTOMATION

2.1 A Proposed Data Transmission Solution

Those IEDs can be installed in power system substations with logic control, data acquisition, event recording, fault location, remote sensing, and monitoring and checking components. Conventionally, the voltages and current signals from the secondary sides of the CTs and PTs are transmitted from the switch yard to the equipment room in analog through conducting cables as shown in Figure 2.1 . The conventional data transmitting system are costly and complicated to maintain. A lot of analog signals are transmitted with a large amount of long cables. Those analog signals are easily susceptible to noise and difficult to detect or fix errors.

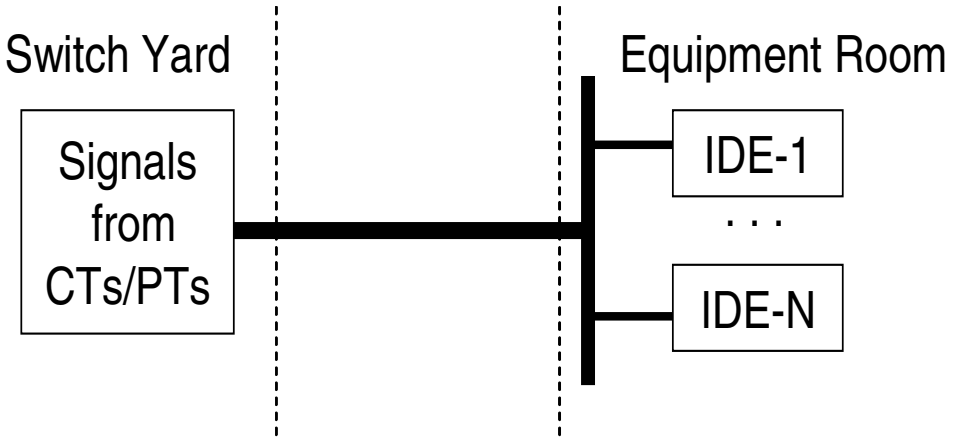

Figure 2.1 Conventional Analog Signal Transmission Solution

A digital data transmission solution as show in Figure 2.2 is proposed . Analog signals from CTs/PTs are digitized at a high speed. Aggregated digital data are sent to the equipment room through the local data communication network which can be high speed internet or high speed optical fiber channel [6]. Data received in the equipment room can be converted with different sample rate or any other format to process further computation. The digital data transmission solution brings many benefits.

a) The quality of the data is guaranteed because the error detection and correction can be applied.
b) Optical fibers or even air for wireless communications are the preferred medium to transmit the digital data.
c) Data transmission distance is much larger than a conventional diameter Equipment room can be set far away from switch yard, even in the area operation center.
d) This high speed data acquisition and the data format converter can provide a shared data acquisition for all the IEDs. And The IEDs can be developed simply through general purpose catalog devices, such as microprocessor, DSP chip or FPGA. The development and manufacturing cost of IEDs can be much cheaper.

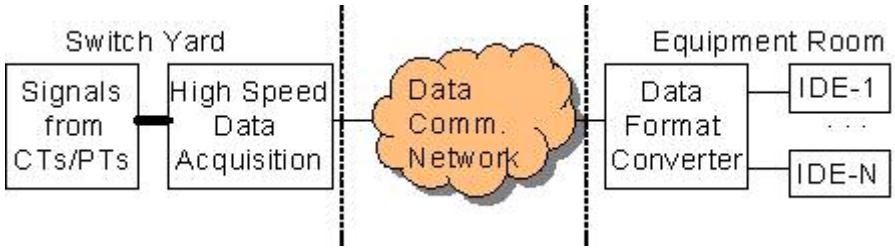

Figure 2.2 Proposed Digital Data Transmission Solution

2.2 Data Format Converter in the Proposed Digital Data Transmission Solution

The data with high sample rate sent from the switch yard are converted to data with the right format for the IEDs by the data format converter. For IEDs supporting digital inputs, the data format converter converts the data with high sample rate to data with the same data rate as these IEDs. For the IEDs only supporting analog signals, the data format converter convert data back to analog signal. So this data format converter as shown in Figure 2.3 uses a digital re-sampling system to generate different sets of data with standard sample rate as published in [5] and [7]. In addition, it also converts the digital data back to analog signal in order to be used by the IEDs which only support analog input signals.

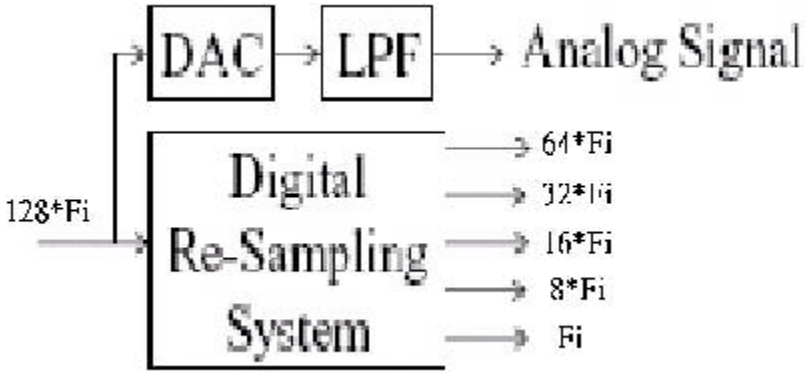

Figure 2.3 Data Format Converter

The sample rate of the high speed data acquisition in the switchyard is proposed to be 128 points per cycle of the fundamental frequency (60Hz in US and 50Hz in China). The data from this data acquisition system can have the signal components from DC to 64th harmonics, which are sufficient for power system steady state and transient state analysis. In addition, the power of 2, and Fast Fourie Transform (FFT) can be applied in the frequency spectrum (or harmonics) analysis [9].

CHAPTER 3

DIGITAL RE-SAMPLING AND DIGITAL FILTERING

3.1 Sampling and Digital Re-sampling

Discrete-time signals can arise in many ways, but they most commonly occur as representations of sampled continuous-time signal can be quite accurately represented by samples in some detail [10]. After Frequency domain analysis is one of the most popular analysis tools in digital signal processing [11]. However, an improperly designed data acquisition solution may cause the frequency-domain signal meaningless and even misleading. The Shannon Theorem or Nyquist Law require that the sampling rate is higher than twice the maximum frequency in the digitized signal.

$$Xc(j\Omega)=0 \text{ for } |\Omega| \geqq \Omega_N$$

$$X[n]=Xc(nT),n=0,\pm1, \pm2,\ldots\ldots, \text{if } \Omega s=(2\pi/T)>2\Omega_N \qquad (1)$$

Anti-alias filter (Low Pass filter) with cut-off frequency as Ω (also called anti-alias filter) is also needed in a data acquisition system as shown in Figure 3.1 Otherwise, it cannot be distinguished between the sampled values of a sine wave of The unexpected signal with frequency higher than 2 / s F appearing in the frequency spectrum is called alias.

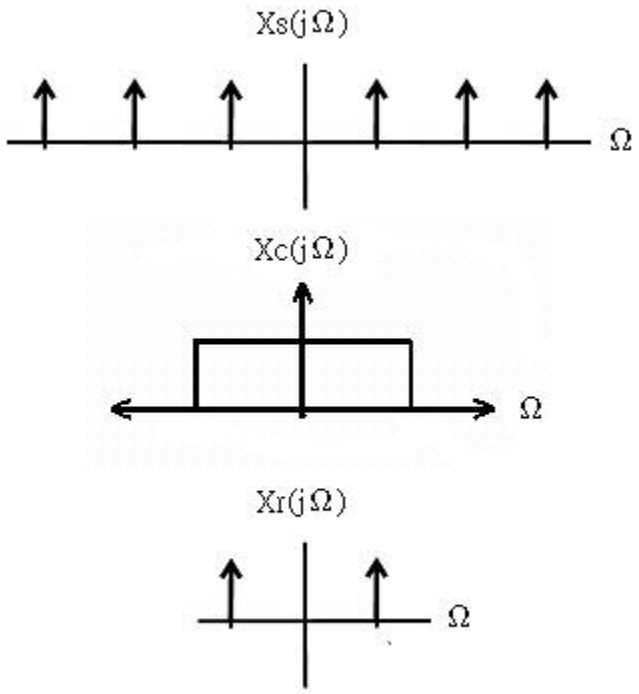

Figure 3.1 Recovery of a continuous-time signal with an lowpass filter

Changing sample rate of digital data is called digital re-sampling. There are two types of re-sampling: rate decreases (called decimation) and rate increases (called interpolation) [8]. Decimation is to reduce the sample rate by an integral factor, and interpolation is to increase the sample rate by an integral factor. In decimation, the sample rate decreases but the bandwidth of the input signal does not decrease. An anti-alias low pass filter is needed to remove the component with frequency higher than $2 / s F$. In interpolation, new samples need to be added into the data sequence and the new sample values need to be calculated. Zero-padding [8] method is often used for interpolation. In the zero-padding method, zeros are inserted into the original data sequence. Then the new data sequence is processed through a low-pass filter (called

interpolation filter). If the sample rate change factor is not integral, the sample rate change will need to be implemented with interpolation followed by decimation as shown in Figure 3.2.

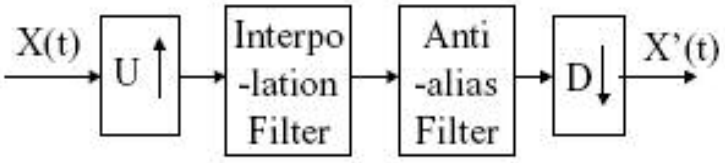

Figure 3.2 Digital Re-Sampling

3.2 Filtering

Filtering is the processing of a time-domain signal resulting in the reduction of some unwanted input spectral components [12]. The filters allow certain frequencies to pass while attenuating other frequencies as shown in Figure 3.3.

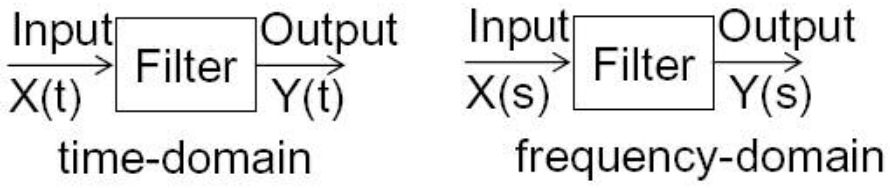

Figure 3.3 Filter

The transfer function of the filter in frequency domain is expressed as:

$$H(s)\Big|_{s=j\omega} = \frac{Y(s)}{X(s)}\Big|_{s=j\omega} = \left|H(j\omega)\right| e^{j\phi(\omega)} \qquad (1)$$

In frequency domain, the magnitude and the phase responses of the network function are the two main factors of designing the filter. The magnitude response is studied frequently in db through the gain function as in (2). The phase response is expressed by phase function or group delay function as in (3). The group delay function and the phase function have profound time-domain ramifications as they have a directly effect on the wave-shape of the output signals.

$$\alpha(\omega) = 20\log\left|H(j\omega)\right| \text{ db} \qquad (2)$$

$$T_d(\omega) = -\frac{d}{d\omega}\phi(\omega) \qquad (3)$$

3.3 Digital Filtering

Conventional linear digital filters typically come in two types: finite impulse response (FIR) filters and infinite impulse response (IIR) filters. The FIR digital filters use only current and past input samples to obtain a current output sample value as shown in (4). The transfer function in z-plane for the FIR filter is shown in (5).

$$y(n) = \sum_{k=0}^{N-1} h(k)x(n-k) \tag{4}$$

$$H(z) = \frac{Y(z)}{X(z)} = \sum_{k=0}^{N-1} h(k)z^{-k} \tag{5}$$

The IIR filters output sample value depends on previous input samples and previous filter output samples as shown in (6). The transfer function in z-plane for the IIR filter is shown in (7).

$$y(n) = \sum_{k=0}^{N} a(k)x(n-k) + \sum_{j=1}^{M} b(j)y(n-j) \tag{6}$$

$$H(z) = \frac{Y(z)}{X(z)} = \frac{\sum_{k=0}^{N} a(k)z^{-k}}{1 - \sum_{j=1}^{M} b(j)z^{-j}} \tag{7}$$

Where:

N is the order of the numerator of the filter;
M is the order of the denominator of the filter;
a(k) is the coefficients of the numerators of the filter;
b(k) is the coefficients of the denominators of the filter.

CHAPTER 4

DESIGN OF DIGITAL FILTERS FOR DATA FORMAT COMVERTER

4.1 Requirement of the Digital Filters

For the digital re-sampling system in this data format converter, the low pass filters as shown in Figure 4.1 are designed to attenuate the high frequency components before applying the decimation. In general, it is desirable to design a filter to have :

(1).Small passband ripple; (Apass)

(2). Large stopband attenuation; (Astop)

(3).Low transition–band ratio;

(4). Constant and small group delay;

(5). Lower order of the transfer function .

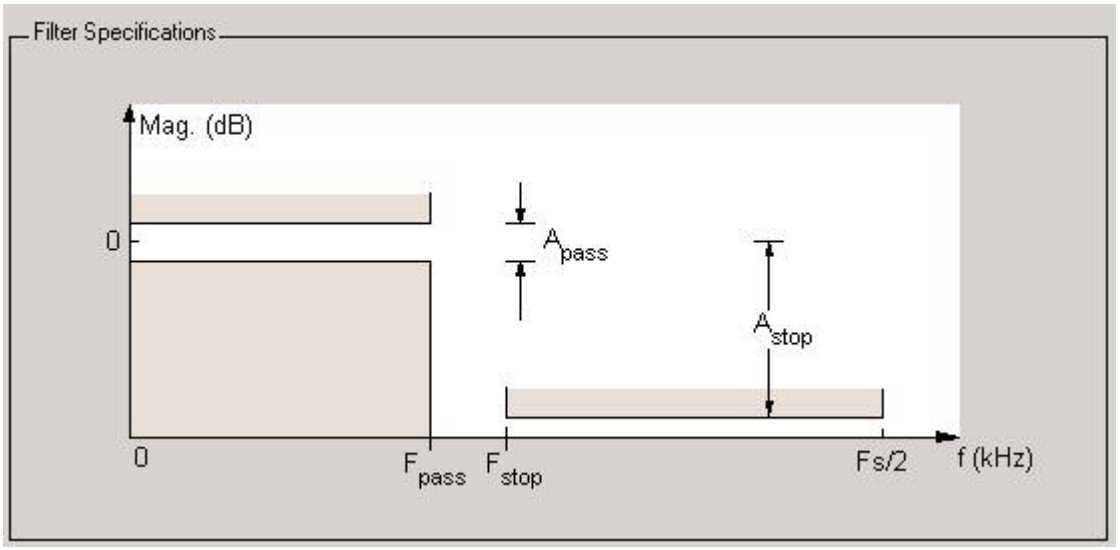

Figure 4.1 Low Pass Filter Specifications

In the data acquisition system for the substation automation, the Analog to Digital Converter (ADC) used is generally 14 bits or 16 bits. The ADC quantization error noise [11] is:

$$SNR=(n+1) * 6.02 + 1.76 \text{ db} \quad (8)$$

Where, N is number of bit in the ADC.

So, the spec for the stop attenuation is set at 104 db for these filters. The passband ripple is 0.3db, and the transition-band ratio is 1/0.9. The maximal deviation of group delay (in number of samples) within the interested bandwidth is 1. The transfer functions for the filters are designed here. The objectives of this design are to:

(1) minimize the order of the transfer function in order to reduce the amount of the calculation;

(2) minimize the number of samples in group delay so that there is shorter delay between the input and the output signals. The problem is formulated as a multi objective optimization problem [1] as Table 4.1:

Table 4.1 The objectives of this design

Minimize:	number of total orders
Minimize:	number of samples in group delay
passband ripple	$\leq$ 0.3 db
stopband attenuation	$\geq$ 104 db
transition-band ratio	$\leq$ 1/0.9
maximal deviation in group delay	$\leq$ 1 sample

4.2 Design Approach for the Digital Filters

The FIR filters with symmetric coefficients have linear phase response (or constant group delay) property [8]. However, the order of the filter might be very large and the number of the samples for the delay between the input and the output signals is half of the number of the order [8]. More calculations or hardware complexity are needed and the more delay are involved if these FIR filters are used in this data format converter.

Table 4.2 FIR & IIR Filter Order

Type	Euirripple FIR	Elliptic(IIR)	Cheby II* (IIR)
Wpass	0.45	0.45	0.45
Wstop	0.5	0.5	0.5
Mag Spec			
Apass (dB)	0.1	0.1	0.1
Astop (dB)	104	104	104
Min order to archive the magnitude requirement	162	12	24
Filter order	162	12	24
Compensator order	0	12	22
Total order	162	24	46
Avg Num. samples delay (after compensation) when group delay deviation is 10%	81	28.07	56.406
Max Samples Deviation	0	0.02956	1.6559
group deviation delay	0	0.0010531	0.029357

The IIR filters have much fewer orders than the FIR with the same filter spec. However, it can not guarantee the constant group delay. In addition, there is no design approach and tool to simultaneously optimize both magnitude and group delay requirement for the IIR filters. So, the design for the IIR filters involves two steps in this paper:

(1). Magnitude approximation;

(2). Group delay compensation.

At the magnitude approximation step, the filters are designed with minimal order and satisfy the requirements on the passband ripple, the stopband attenuation and the transition-band ratio.

Table 4.3 The result of Filter design in different approaches

Type	Elliptic	Butterworth	Cheby I	Cheby II
Wpass	0.45	0.45	X	X
Wstop	0.5	0.5	0.5	0.5
Apass (dB)	0.1	.5	0.1	X
Astop (dB)	100	15	X	80
Filter orders	14(min 12)	12	14	14
Min order	12	85	X	X
compensation range (0~0.4)**	0.001~0.551	0.001~0.551	0.001~0.651	0.001~0.651
After compensation				
1.Average delay (samples)	57.3757	56.1669	53.8193	48.1760
2.Deviation sample	0.1046	0.5790	8.9338	0.4201
3. Deviation rate(2./1.)	0.0018	0.0103	0.1660	0.0087
Order of compensator	30	30	30	30
compensation range (0~0.5)**	0.001~0.451	0.001~0.451	0.001~0.451	0.001~0.451
After compensation				
1.Average delay (samples)	65.9116	61.7871	83.9014	28.0712***
2.Deviation sample	0.3222	0.0300	34.3746	176.4244***
3. Deviation rate(2./1.)	0.0049	4.8579e-004	0.4097	6.2849***
Order of compensator	30	30	30	30
Total calculations	44	42	44	44

At the group delay compensation step, another all pass filter is designed to make the group delay constant within the interested bandwidth. Due to the tradeoff between the objective functions, there might not be one optimal solution for both objective functions. A value function [14] for this multi-objective optimization is defined as:

Minimize: (number of total order) + w * (number of samples in group delay)

Where, w is the weight for the group delay.

This optimization problem works on three types of filters: the equal-ripple FIR filter, the elliptic IIR filter and the Chebyshev II IIR filter. The type of filter and the number of order are the decision variables for this problem.

4.3 Design Result for the Digital Filters

This filter design aims at real-time applications. So "w = 10" is selected in the value function to put more weight on the objective for the group delay. The selection on the filters for the decimators with rates of 2, 4 and 8 considers both magnitude and phase response. And the phase response is not considered in the filter for the decimator with rate of 128 because the main purpose for this decimation is for the application of monitoring low frequency oscillation issue in power system. In the solution for this optimization problem, the filters for the decimator with rate of 2 and 4 are an elliptic IIR filter cascaded with an all-pass IIR filter. The total number of the orders and the total number of samples in the group delay for interested band are small and acceptable. However, the filter for the decimator with rate of 8 is an equal-ripple FIR filter. The order is 585 and the number of samples in group delay is 292.5, which is unacceptable for real-time application. So the architecture for this digital resampling in the data format converter is designed as in Figure 4.2.

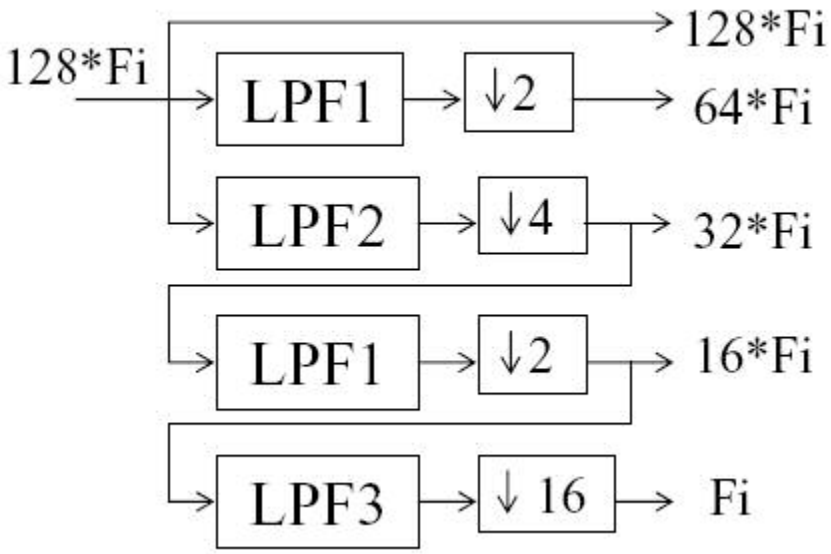

Figure 4.2 Digital Re-Sampling for Data Format Converter

The designed LPF1 consists of two filters: the elliptic IIR filter for the magnitude approximation and the all-pass IIR filter for the group delay compensation. The orders are 12 for the elliptic IIR filter and 6 for the all-pass IIR filter. The number of samples in the group delay within the interested bandwidth from 0 to 0.383 (normalized frequency) is about 19.4 with maximal variation of 0.90. The magnitude response and the group delay for the whole filter network are shown in Figure 4.3 and Figure 4.4. From the figures, it is notable that the magnitude response satisfies the filter spec and the group delay is constant in the interested bandwidth.

Table 4.4 the result of designing LPF1 in different approach

Type	Euirripple FIR	Elliptic	Cheby II*
Wpass	0.45	0.45	0.45
Wstop	0.5	0.5	0.5
Apass (dB)	0.1	0.1	0.1
Astop (dB)	104	104	104
Min order to archive the magnitude requirement	162	12	24
Filter order	162(no compensation needed)	12	24
Compensator order	0	12	22
Total order	162	24	46
Avg Num. samples delay (after compensation) when group delay deviation is 10%	81	28.07	56.406
Max Samples Deviation	0	0.02956	1.6559
group deviation delay	0	0.0010531	0.029357

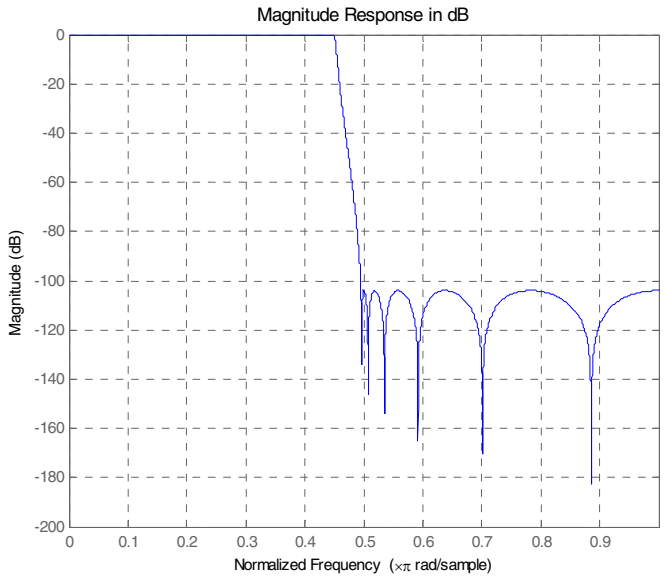

Figure 4.3 Low Pass Filter - LPF1 Magnitude Response

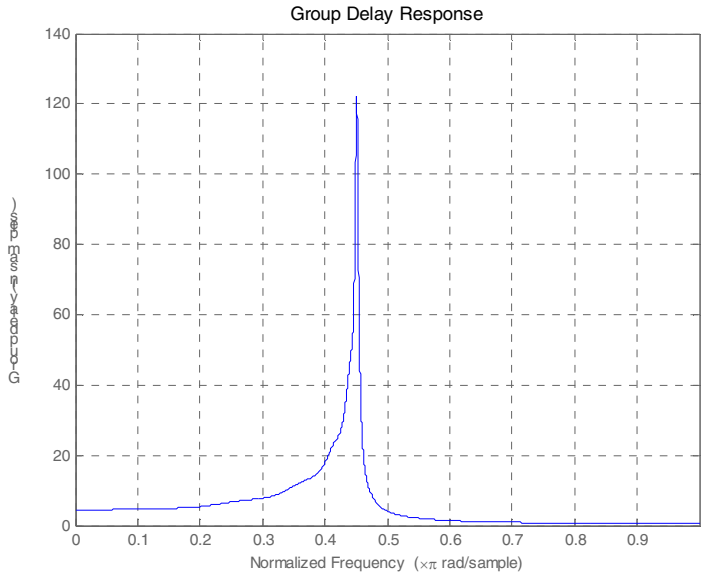

Figure 4.4 Low Pass Filter - LPF1 Group Delay Response

The LPF2 also consists of two filters: the elliptic IIR filter and the all-pass IIR filter. The orders are 13 for the elliptic IIR filter and 8 for the all-pass IIR filter. The number of samples in the group delay within the interested bandwidth from 0 to 0.195 (normalized frequency) is about 48.5 with maximal variation of 0.76. The magnitude response and the group delay are shown in Figure 4.5 and Figure 4.6 . From the figures, it is notable that the magnitude response satisfies the filter spec and the group delay is constant in the interested bandwidth.

Table 4.5 the result of designing LPF2 in different approach

Type	Euirripple FIR	Elliptic	Cheby II*
Wpass	0.22	0.22	0.22
Wstop	0.25	0.25	0.25
Apass (dB)	0.1	0.1	0.1
Astop (dB)	104	104	104
Min order to archive the magnitude requirement	271	12	26
Filter order	271	13	26
Compensator order	0	6	10
Total order	271	19	36
Avg Num. samples delay (after compensation) when group delay deviation is 10%	135.5 (no compensation needed)	35.273	56.607
Max Samples Deviation	0	0.19612	0.4454
group deviation delay	0	0.00556	0.007868

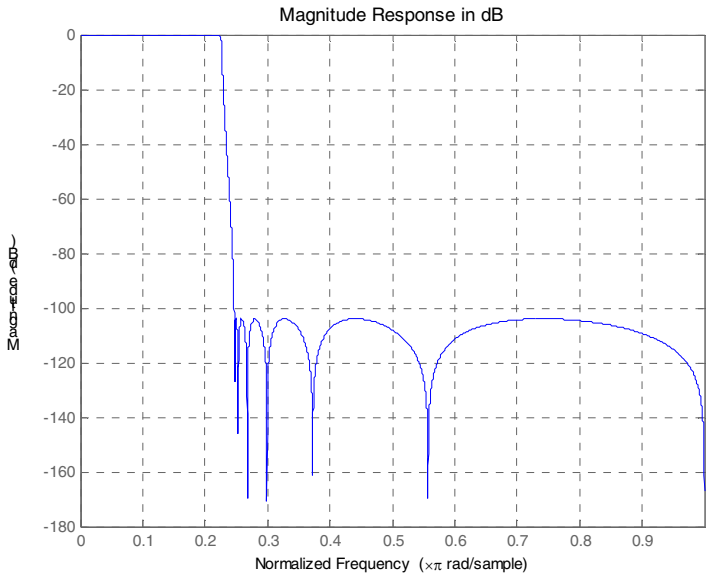

Figure 4.5 Low Pass Filter – LPF2 Magnitude Response

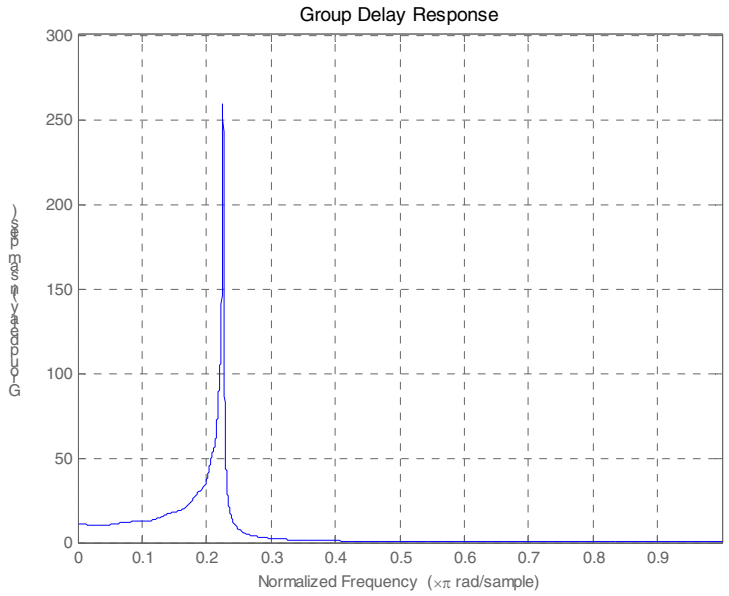

Figure 4.6 Low Pass Filter – LPF2 Group Delay Response

The transition-band ratio of the filter for the decimator with rate of 16 is re-defined as 1/0.8 because no stable elliptic IIR filter in direct form structure was able to be obtained. The designed LPF3 is an elliptic IIR filter with order of 11. The Magnitude response and group delay are shown in Figure 4.7 and Figure 4.8.

Table 4.6 the result of designing LPF3 in different approach

Type	Euirripple FIR	Elliptic	Cheby II*
Wpass	0.11	0.11	0.11
Wstop	0.125	0.125	0.125
Mag Spec			
Apass (dB)	0.1	0.1	0.1
Astop (dB)	104	104	104
Min order to archive the magnitude requirement	541	13	24
Filter order	541(no compensation needed)	25	26
Compensator order	0	14	6
Total order	541	39	32
Avg Num. samples delay (after compensation) when group delay deviation is 10%	270.5	23.295	30.4
Max Samples Deviation	0	1.6102	2.1948
group deviation delay	0	0.069123	0.072198

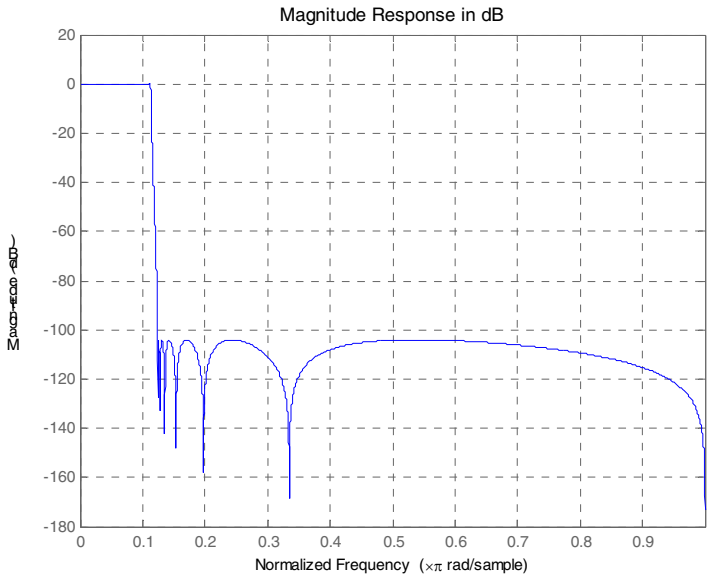

Figure 4.7 Low Pass Filter – LPF2 Magnitude Response

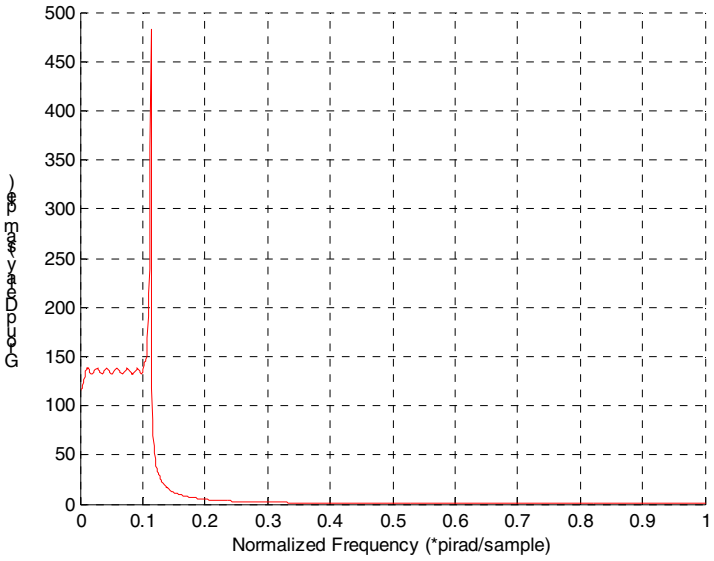

Figure 4.8 Low Pass Filter – LPF3 Group Delay Response

CHAPTER 5

IMPLEMENT THIS DATA FORMAT CONVERTER ONTO DSP CHIP

5.1 Introduction

Digital signal processing chips (DSP's) have caused a revolution in product design since 1980's. DSP's differ from ordinary microprocessors in that they are specifically designed to rapidly perform the sum of products operation required in many discrete-time signal processing algorithms. DSP can be streamlined to have a smaller size, use less power, and have a lower cost. Low cost DSP's have made it more economical to implement functions by digital signal processing techniques rather than by hard-wired analog circuits. In addition, programmable DSP's can implement both complicated linear and nonlinear algorithms and easily switch functions by jumping to different sections of program code [15].

Floating-point DSP's are easy in programming. However, integer DSP's are used most frequently because the calculation of integers are much better performance than the floating-point.

5.2 SOS Structure

Any transfer function H(z) has a second-order sections representation (9).

$$H(z) = \prod_{k=1}^{L} H_k(z) = \prod_{k=1}^{L} \frac{b_{0k} + b_{1k}z^{-1} + b_{2k}z^{-2}}{a_{0k} + a_{1k}z^{-1} + a_{2k}z^{-2}} \qquad \textbf{(9)}$$

where L is the number of second-order sections that describe the system. MATLAB represents the second-order section form of a discrete-time system as an L-by-6 array SOS. Each row of sos contains a single second-order section, where the row elements are the three numerator and three denominator coefficients that describe the second-order section.

$$sos = \begin{bmatrix} b_{01} & b_{11} & b_{21} & a_{01} & a_{11} & a_{21} \\ b_{02} & b_{12} & b_{22} & a_{02} & a_{12} & a_{22} \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ b_{0L} & b_{1L} & b_{2L} & a_{0L} & a_{1L} & a_{2L} \end{bmatrix} \qquad \textbf{(10)}$$

Through careful pairing of the pole and zero pairs, ordering of the sections in the cascade, and multiplicative scaling of the sections, it is possible to reduce quantization noise gain and avoid overflow in some fixed-point filter implementations. [16]

5.3 IIR filter hardware implement

The transfer function can be factored as

$$H(z)=CH_1(z)H_2(z)\ldots..H_r(z) \qquad (11)$$

Using new cascade transfer functions can represent the origin a transfer function as shown in Figure 5.1 For each section, the direct form II structure or its trans-pose version can be used.

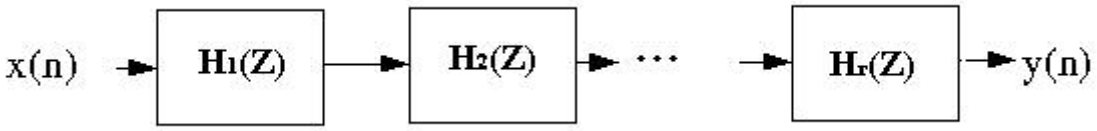

Figure 5.1 Cascade form IIR filter structure

In the cascade form as shown in Figure 5.2, the output of one section forms the input to the next: It does not matter in which order the sections are placed - the result will be the same.

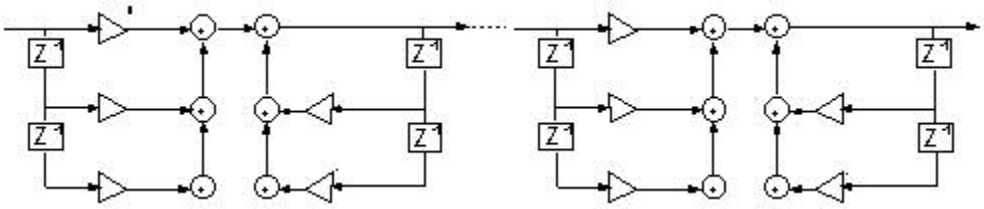

Figure 5.2 Cascade direct form IIR filter structure

The implement of IIR filter using the two equations (12) and (13) associated with each stage:

$$U(n)=X(n)-b1*U(n-1)-b2*U(n-2) \qquad (12)$$

$$Y(n)=A0*U(n)+A1U(n-1)+A2(n-2) \qquad (13)$$

The input signals as shown in Figure 5.3 is the combination of many sine signals. The output signals as shown in Figure 5.4 has some distortion in first 1.5 sec. With an intermediate output result stored in one of the registers, a premature truncation of the first 1.5 sec intermediate output is negligible. The LPF1, LPF2 , LPF3 frequency response are in Figure 5.4, Figure 5.5 Figure 5.6

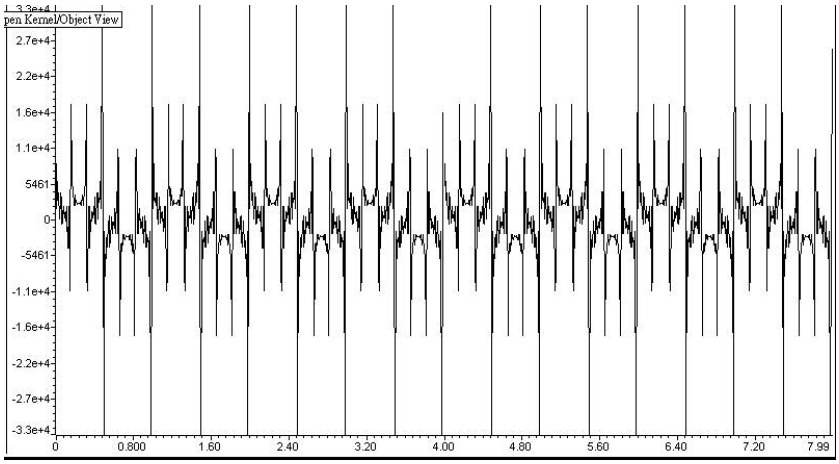

Figure 5.3 Input of DSP's

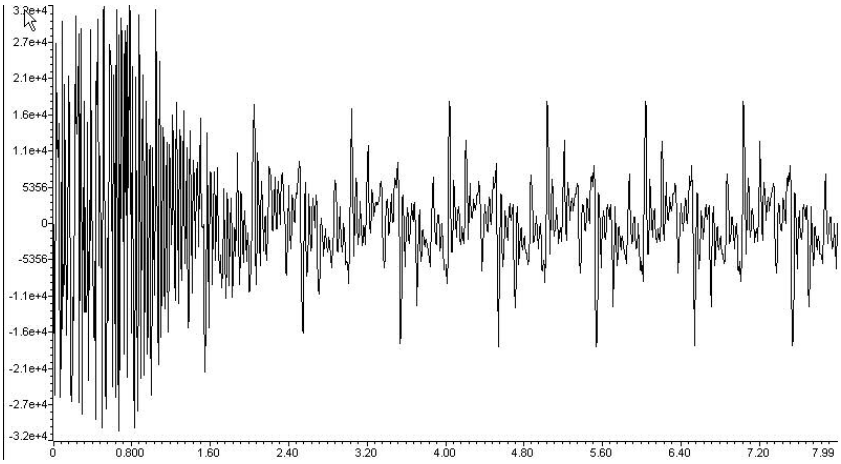

Figure 5.4 Output of DSP's

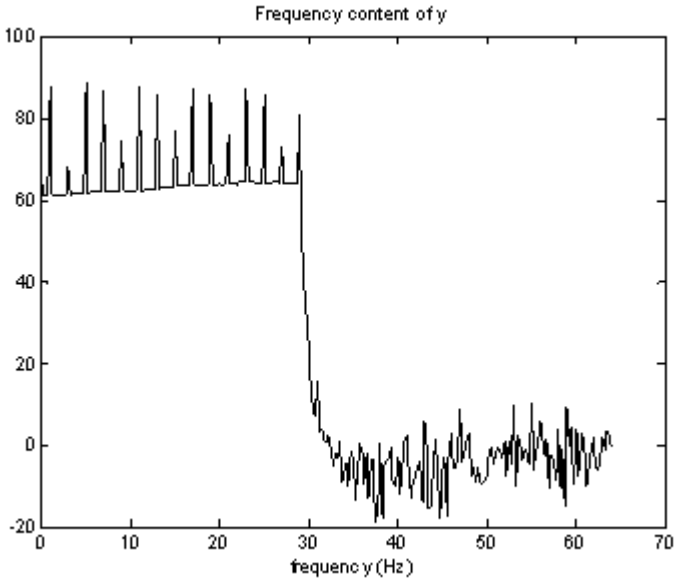

Figure 5.5 Low Pass Filter – LPF1 Total Response

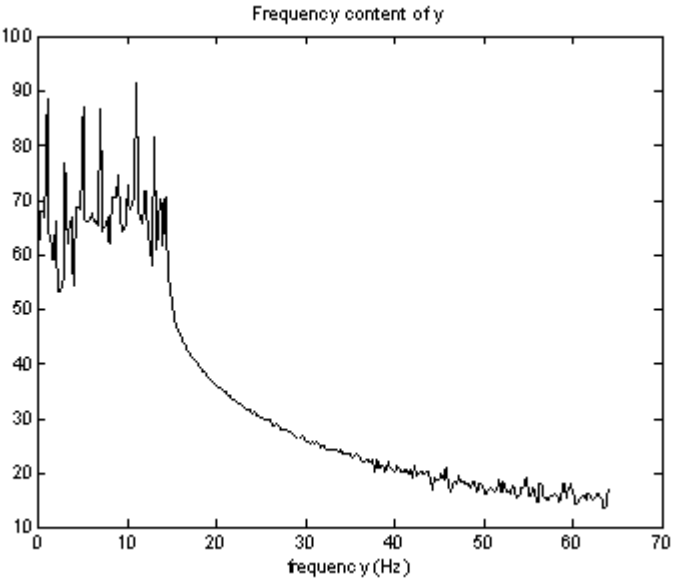

Figure 5.6 Low Pass Filter – LPF2 Total Response

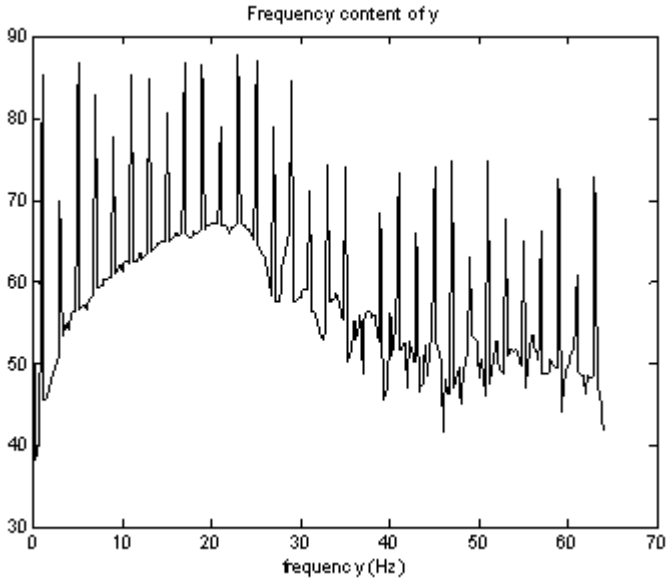

Figure 5.7 Low Pass Filter – LPF3 Magnitude Response

CHAPTER 6

CONCLUSION AND FUTUREWORK

A digital re-sampling solution is proposed for power system applications, especially for low cost substation automation development. Digital filters are designed with consideration of both magnitude and phase responses for this digital re-sampling solution. These digital filters have lower orders and fewer samples in group delay. They can be used for both real-time applications and offline studies. The simulation in the design demonstrates the good performance of these filters. Future work is: (1). to implement this data format converter onto both floating-point and fixed-point DSP chip (2). to add time stamp from a reference timing system (such as Global Positioning System) into the data with consideration of the affect of the group delay.

APPENDIX A

DESIGN FILTER PARAMETERS / RESULT

LPF1 Magnitude Filter Parameters

```
#define MWSPT_NSECO 6

const long NUMO[MWSPT_NSECO][3] = {
{43,80,43},
{32767,38752,32767},
{32767,18691,32767},
{32767,7206,32767},
{32767,1517,32767},
{32767,-790,32767},};

const long DENO[MWSPT_NSECO][2] = {
{-42121,15113},
{-33360,19403},
{-23142,24452},
{-15817,28191},
{-11688,30559},
{-9965,32112},};
```

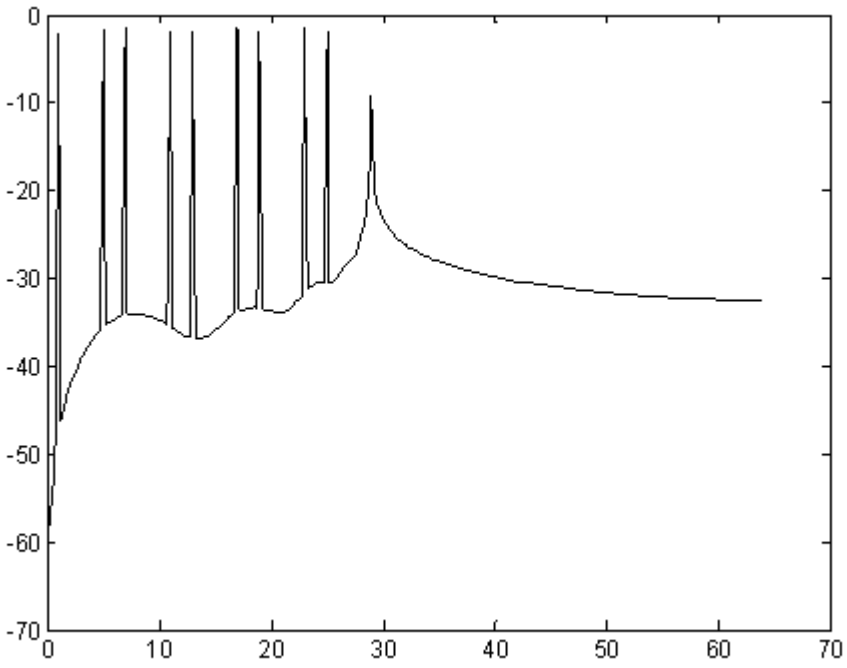

Figure A.1 LPF1 Magnitude Filter Magnitude Response

LPF1 Group 6 orders Compensator Filter Parameters

```
#define MWSPT_NSECG 3

const long NUMG[MWSPT_NSECG][3] = {
{7131,-18186,11953},
{32767,-50926,54672},
{32767,-71722,53837},};

const long DENG[MWSPT_NSECG][2] = {
{-49855,19550},
{-30522,19639},
{-43652,19943},};
```

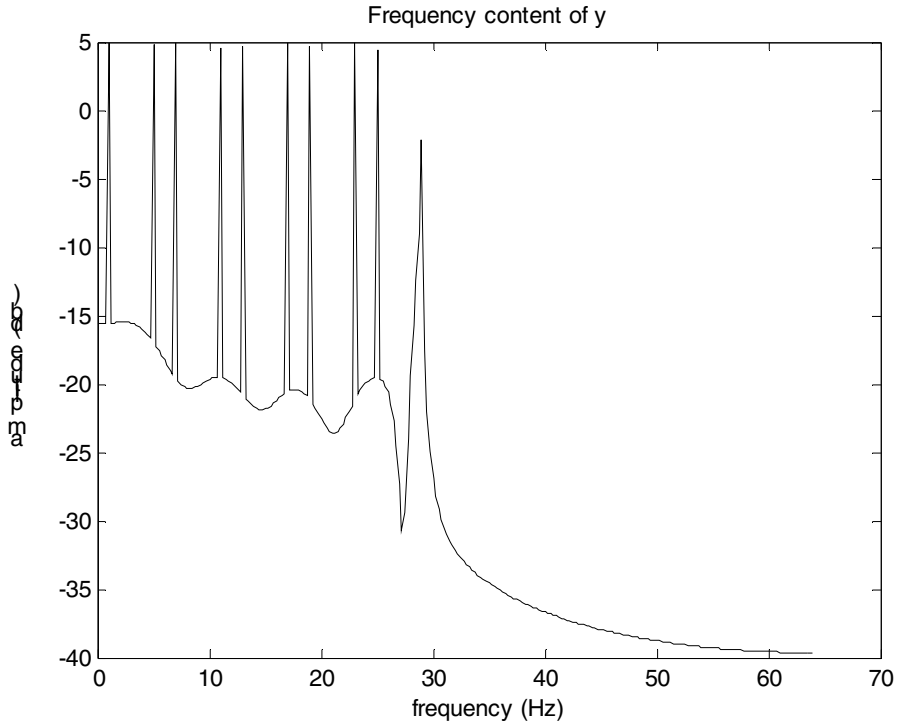

Figure A.2 LPF1 After Group 6 orders Compensator Filter Magnitude Response

LPF1 Group 8 orders Compensator Filter Parameters

```
#define MWSPT_NSECG 4

const long NUMG[MWSPT_NSECG][3] = {
{2001,-6469,5229},
{32767,-91040,69671},
{32767,-70732,58071},
{32767,-47176,54487},};

const long DENG[MWSPT_NSECG][2] = {
{-40535,12536},
{-42817,15411},
{-39911,18489},
{-28371,19705},};
```

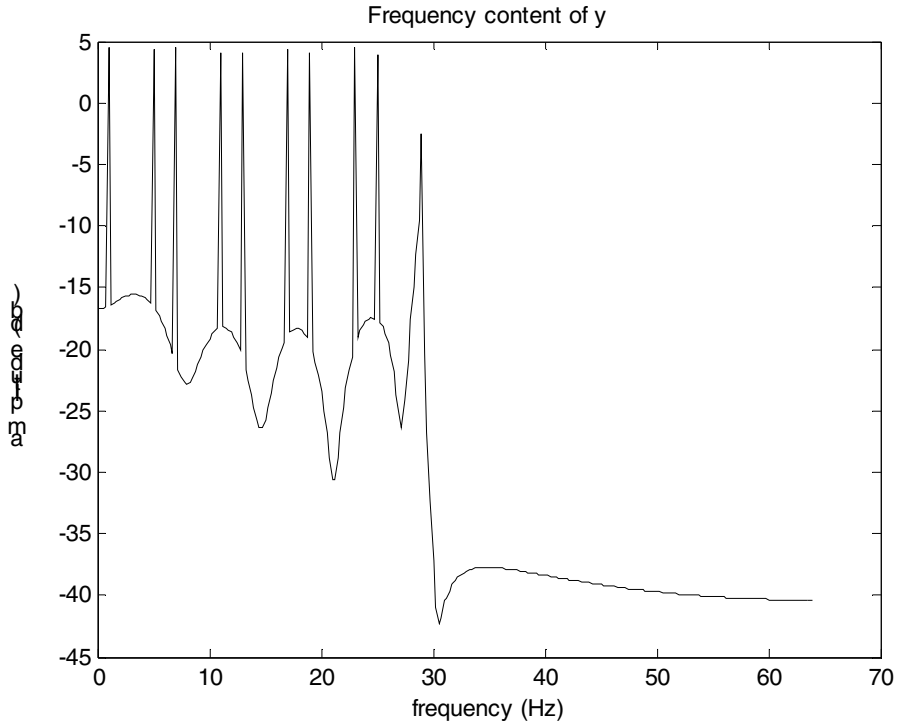

Figure A.3 LPF1 After Group 8 orders Compensator Filter Magnitude Response

LPF1 Group 10 orders Compensator Filter Parameters

```
#define MWSPT_NSECG 6

const long NUMG[MWSPT_NSECG][3] = {
{3510,-8616,6364},
{32767,-87030,58802},
{32767,-67437,57085},
{32767,-45636,52974},
{32767,-14250,33379},};

constlongDENG[MWSPT_NSECG][2]={
{-44364,18071}
{-48497,18259}
{-38709,18808}
{-28228,20268}
{-13989,32166},};
```

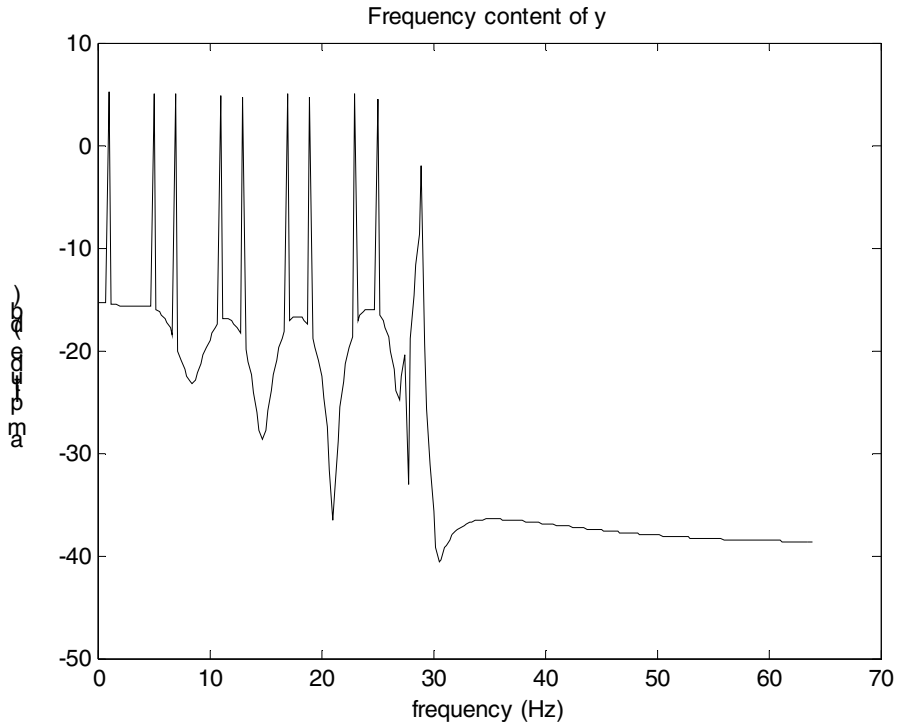

Figure A.4 LPF1 After Group 10 orders Compensator Filter Magnitude Response

LPF1 Group 12 orders Compensator Filter Parameters

```
#define MWSPT_NSECG 6

const long NUMG[MWSPT_NSECG][3] = {
{1600,-1122,2897}
{32767,-79964,54456}
{32767,-61444,54167}
{32767,-83365,53632}
{32767,-71455,53486}
{32767,-44326,50500},};

Const long DENG[MWSPT_NSECG][2]={
{-12698,18101}
{-48115,19716}
{-37169,19821}
{-50933,20019}
{-43775,20074}
{-28761,21261},};
```

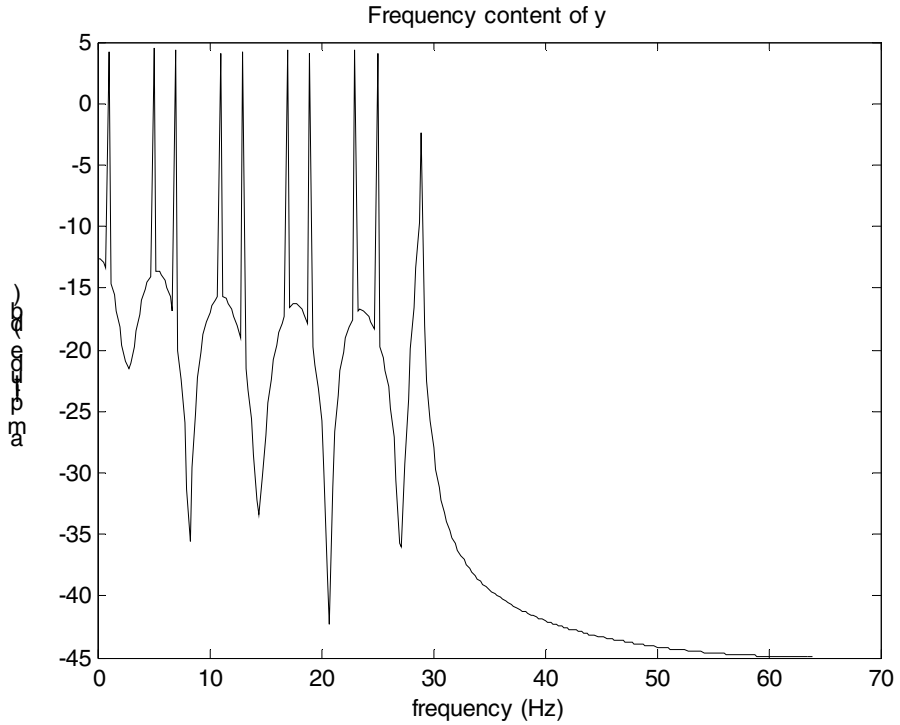

Figure A.5 LPF1 After Group 12 orders Compensator Filter Magnitude Response

LPF1 Group 14 orders Compensator Filter Parameters

```
#define MWSPT_NSECO 6

const long NUMO[MWSPT_NSECO][3] = {
{43,80,43},
{32767,38752,32767},
{32767,18691,32767},
{32767,7206,32767},
{32767,1517,32767},
{32767,-790,32767},};

Const long DENO[MWSPT_NSECO][2]={
{-42121,15113},
{-33360,19403},
{-23142,24452},
{-15817,28191},
{-11688,30559},
{-9965,32112},};
```

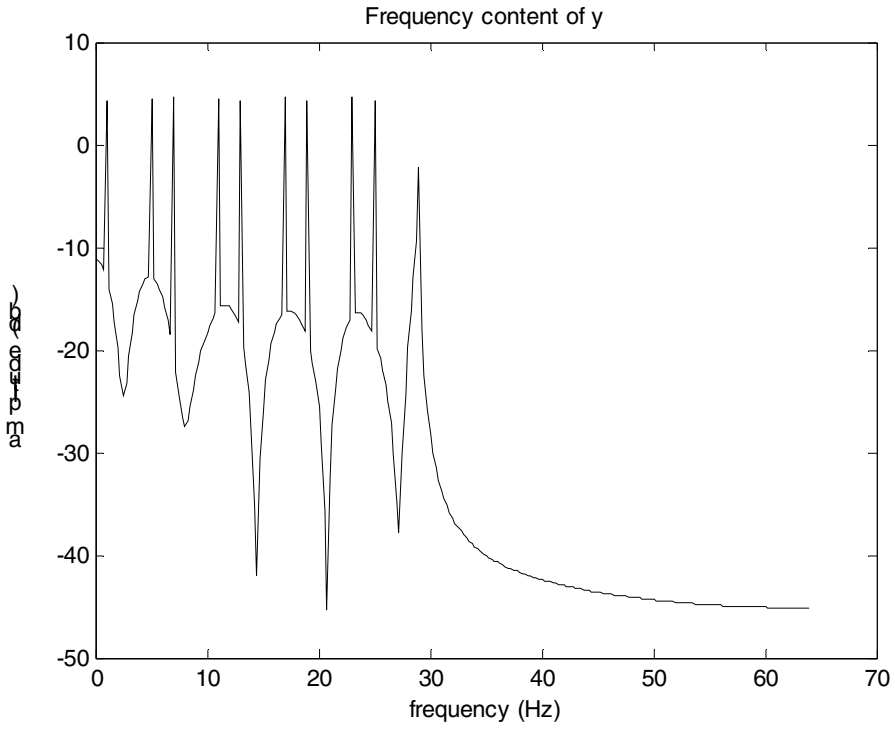

Figure A.6 LPF1 After Group 14 orders Compensator Filter Magnitude Response

LPF2 Magnitude Filter Parameters

```
#define MWSPT_NSECO 7

Const long NUMO[MWSPT_NSECO][3]={
{2,2,0},
{32767,11733,32767},
{32767,-25557,32767},
{32767,-38614,32767},
{32767,-43729,32767},
{32767,-45897,32767},
{32767,-46721,32767},};


Const long DENO[MWSPT_NSECO][2]={
{-27601,0},
{-54476,24273},
{-52845,26589},
{-51241,28913},
{-50140,30620},
{-49593,31723},
{-49540,32457},};
```

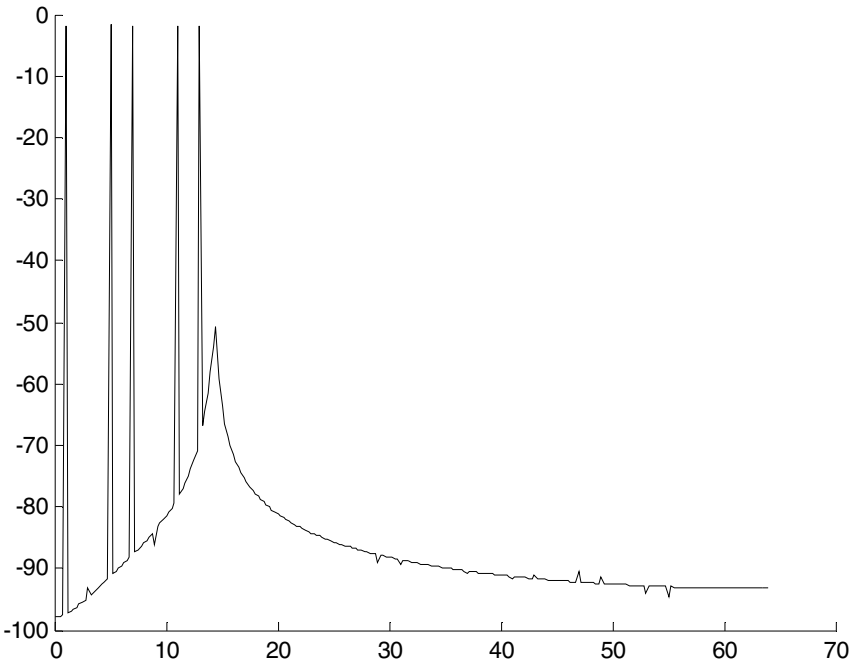

Figure A.7 LPF2 Magnitude Filter Magnitude Response

LPF2 Group 6 orders Compensator Filter Parameters

```
#define MWSPT_NSECG 3

const long NUMG[MWSPT_NSECG][3] = {
{16671,-33591,21160},
{32767,-70544,41135},
{32767,-72443,40420},};

const long DENG[MWSPT_NSECG][2] = {
{-52018,25816},
{-56194,26101},
{-58728,26563},};
```

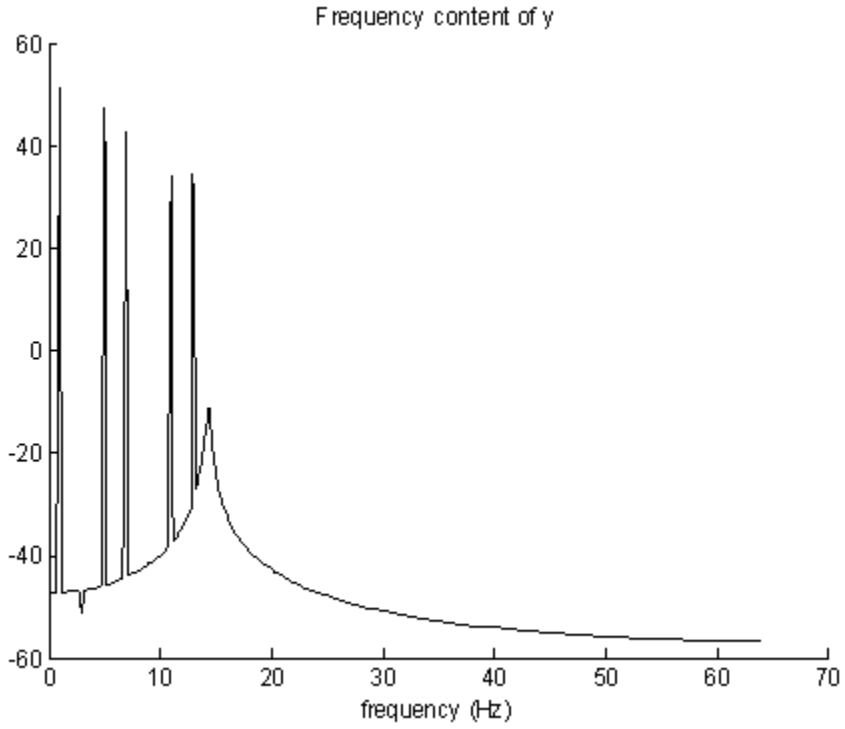

Figure A.8 LPF2 After Group 6 orders Compensator Filter Magnitude Response

LPF2 Group 8 orders Compensator Filter Parameters

```
#define MWSPT_NSECG 4

const long NUMG[MWSPT_NSECG][3] = {
{12740,-28225,16336}
{32767,-73750,41738}
{32767,-68824,41150}
{32767,-64028,41086},};

const long DENG[MWSPT_NSECG][2] = {
{-56613,25553}
{-57898,25724}
{-54804,26092}
{-51064,26133}
```

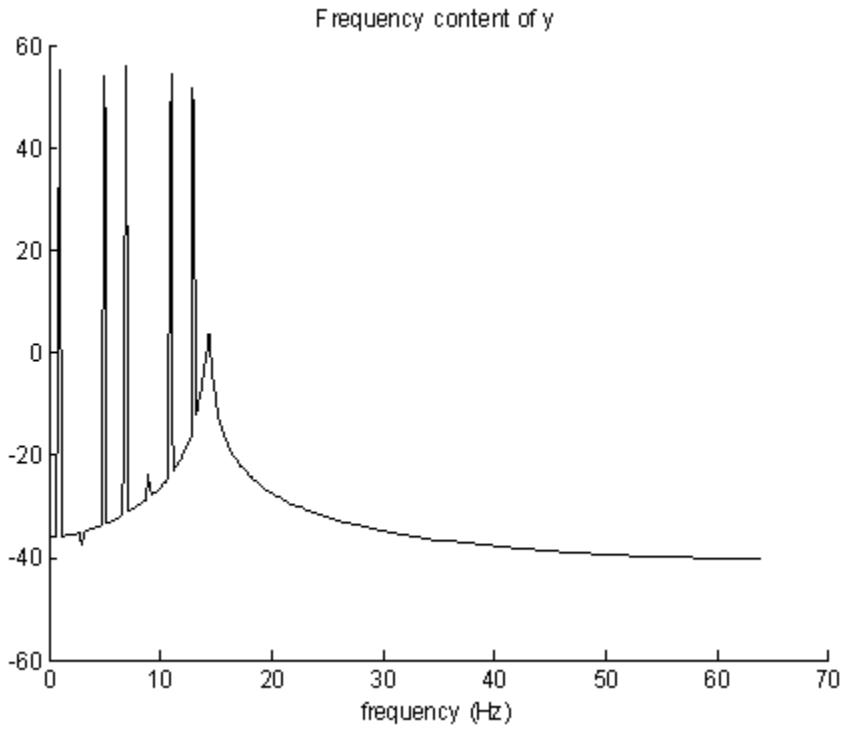

Figure A.9 LPF2 After Group 8 orders Compensator Filter Magnitude Response

LPF2 Group 10 orders Compensator Filter Parameters

```
#define MWSPT_NSECG 5

const long NUMG[MWSPT_NSECG][3] = {


{1878,-9687,12493},
{32767,-72867,42367},
{32767,-74043,42079},
{32767,-68895,41300},
{32767,-63928,41065},};

const long DENG[MWSPT_NSECG][2] = {
{-25409,4926},
{-56356,25342},
{-57657,25516},
{-54661,25997},
{-51010,26146},};
```

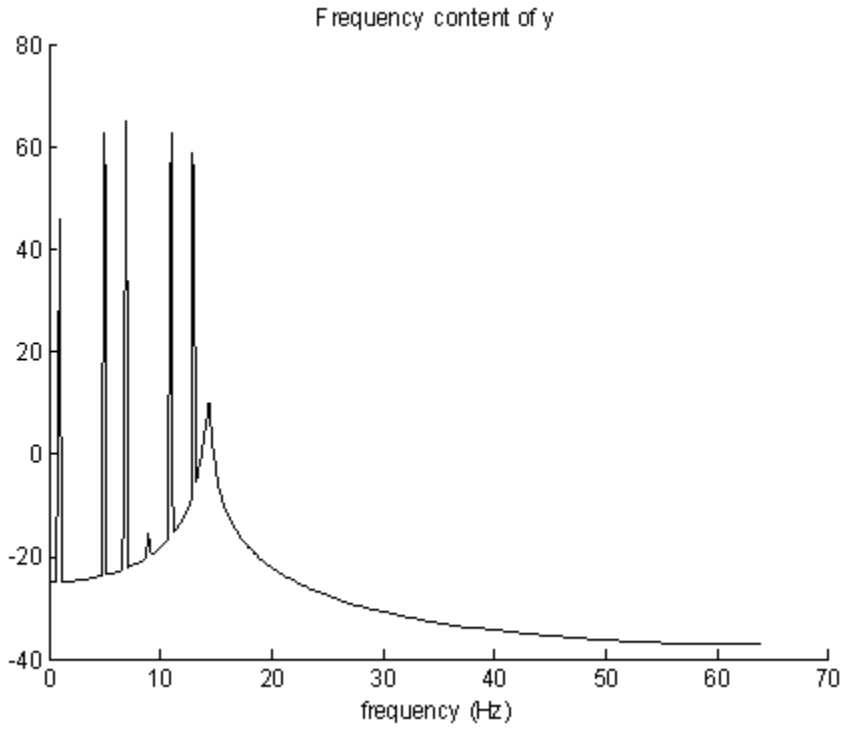

Figure A.10 LPF2 After Group 10 orders Compensator Filter Magnitude Response

LPF2 Group 12 orders Compensator Filter Parameters

```
#define MWSPT_NSECG 6

const long NUMG[MWSPT_NSECG][3] = {

{8555,-18508,10865}
{32767,-73406,41261},
{32767,-72455,41204},
{32767,-54031,41082},
{32767,-67675,40819},
{32767,-62837,39955},};

const long DENG[MWSPT_NSECG][2] = {

{-55813,25801},
{-58294,26021},
{-57618,26057},
{-43095,26135},
{-54326,26303},
{-51532,26872},};
```

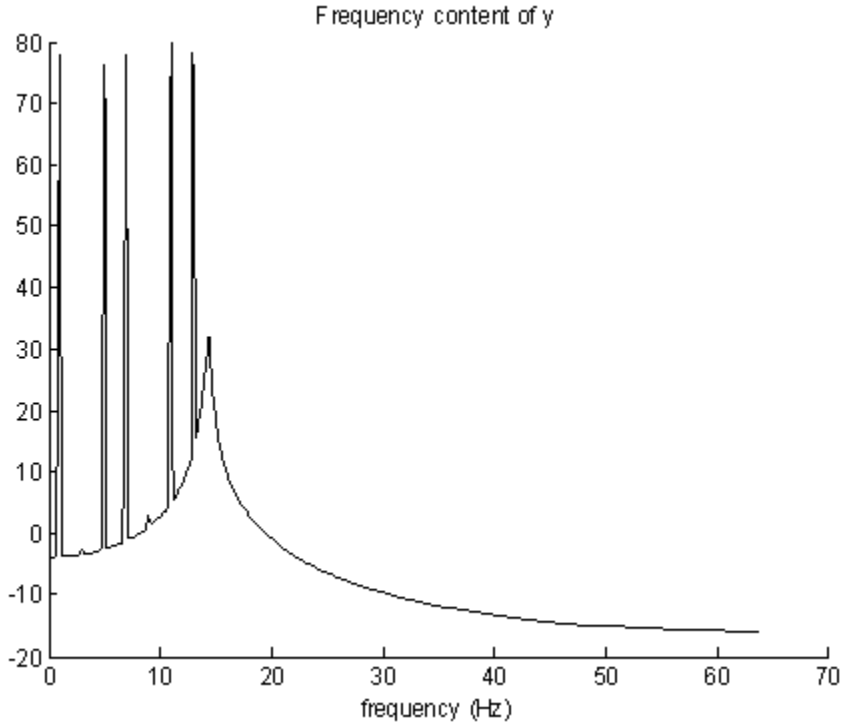

Figure A.11 LPF2 After Group 12 orders Compensator Filter Magnitude Response

LPF2 Group 14 orders Compensator Filter Parameters

```
#define MWSPT_NSECG 7

const long NUMG[MWSPT_NSECG][3] = {

{7958,-14239,9940},
{32767,-70731,40326},
{32767,-66377,40183},
{32767,-68591,40102},
{32767,-72344,40030},
{32767,-71697,40014},
{32767,-62183,39199},};

const long DENG[MWSPT_NSECG][2] = {

{-46939,26235},
{-57472,26625},
{-54126,26719},
{-56044,26773},
{-59219,26822},
{-58712,26833},
{-5198027390},};
```

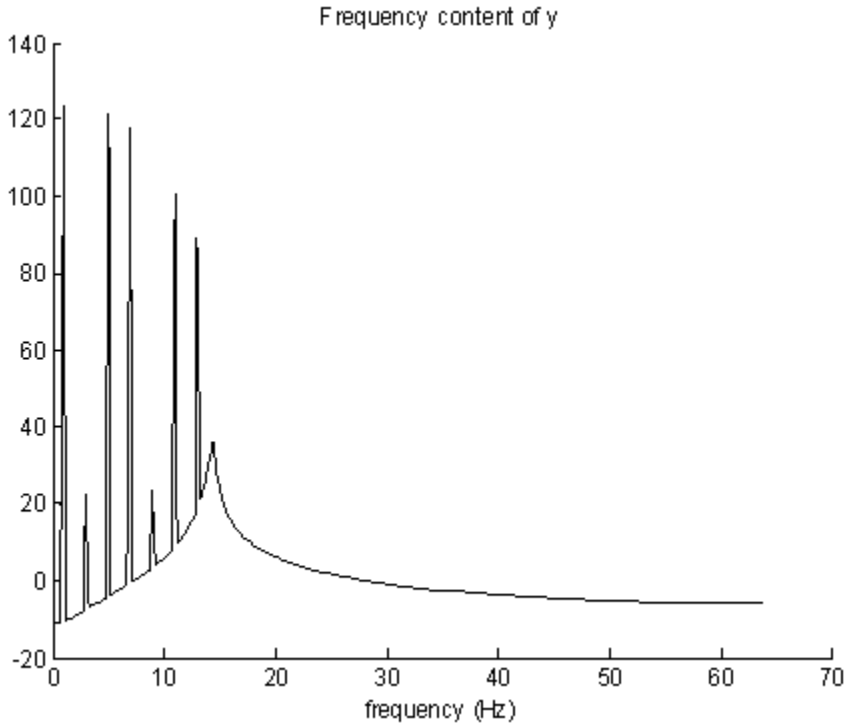

Figure A.12 LPF2 After Group 14 orders Compensator Filter Magnitude Response

LPF3 Magnitude Filter Parameters

```
#define MWSPT_NSECO 7

const long NUMO[MWSPT_NSECO][3] = {
{0,0,0},
{32767,-32533,32767},
{32767,-53313,32767},
{32767,-58049,32767},
{32767,-59679,32767},
{32767,-60337,32767},
{32767,-60582,32767},};

const long DENO[MWSPT_NSECO][2] = {
{-30160,0},
{-60402,28290},
{-60590,29492},
{-60782,30709},
{-60977,31634},
{-61095,32188},
{-61322,32612},};
```

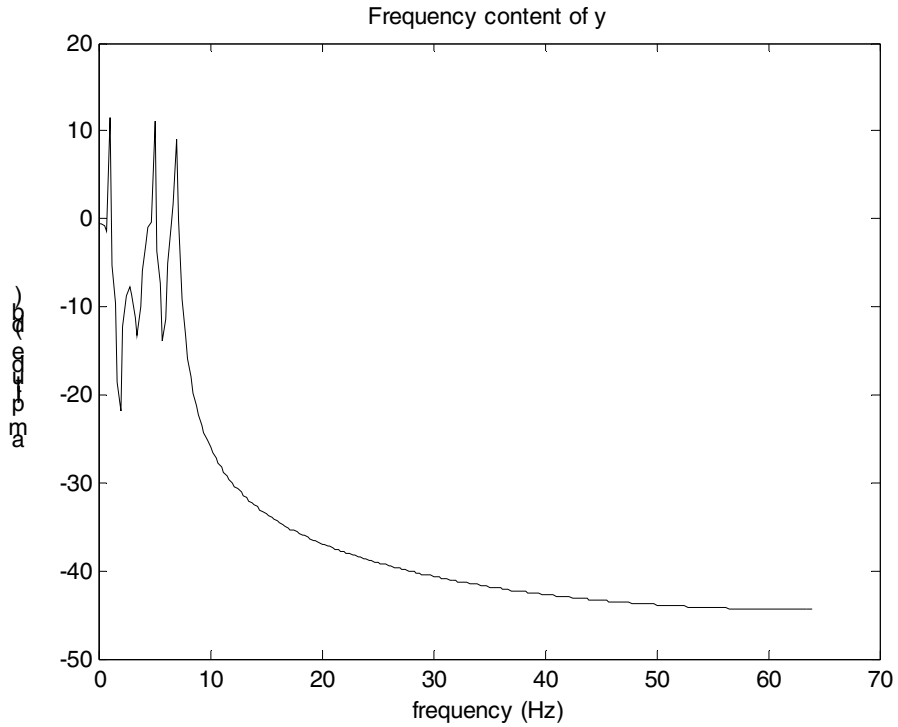

Figure A.13 LPF3 Magnitude Filter Magnitude Response

REFERENCES

[1] Energy Information Administration, The Changing Structure of the Electric Power Industry 2000: An Update, DOE/EIA-0562(00) Distribution Category UC-950, 2000

[2] Qing Zhao, Development of Multi-Objective Optimization & Ecommerce Software Architecture for Commodity Trading in Deregulated Power Market, Ph.D. Dissertation, Texas A&M University, 2000..

[3] John D. McDonald, Electronic Power Substations Engineering, CRC Press, 2003.

[4] IEEE Tutorial Course, Advancements in Microprocessor BasedProtection and Communication, IEEE Operations Center, 1997.

[5] IEEE-SA Standards Board, "IEEE Standard for Synchrophasors forPower Systems," IEEE Std 1344-1995, March 17, 2001.

[6] Tor Skeie, etc., "ETHERNET in Substation Automation," IEEE ControlSystems Magazine, pp43-51, June 2002.

[7] IEEE-SA Standards Board, "IEEE Standard Common Format for Transient Data Exchange (COMTRADE) for Power Systems," IEEE Std C37.111-1999, March 19, 1999.

[8] Ricahrd G. Lyons, Understanding Digital Signal Processing, Rrentice Hall PTR, 2001.

[9] Robert W. Ramirez, the FFT Fundamentals and Concepts, Rrentice Hall PTR, 1985.

[10] Alan V. Oppenheim and Ronald W. Schafer, Discrete-time Signal Processing second edition, 1999

[11] Rudy van de Plassche, Integrated Analog-To-Digital And Digital-To-Analog Converters, KAP, 1994.

[12] Kendall Su, Analog Filters, Kluwer Academic Publishers, second edition, 2002.

[13] Qing Zhao, Development of Multi-Objective Optimization & Ecommerce Software Architecture for Commodity Trading in Deregulated Power Market, Ph.D. Dissertation, Texas A&M University, 2000.

[14] Craig Marven, Gillian Ewers, A Simple Approach to Digital Signal Processing, Wiley Interscience, 1996.

[15] Steven A. Tretter, Communication System Design Using DSP Algorithms, Kluwer Academic/ plenum publishers.

[16] Signal Processing Toolbox User's Guide (December 1996)

[17] Rulph Chassaing, DSP Appliations Using C and the TMS320C6x DSK, Wiley Inter-science 2002

BIOGRAPHICAL INFORMATION

The author received the B.S. degree in Electronic Engineering from Chung Yuan Christian University in Taiwan in 1997. He served in Taiwan Army as a Sergeant in Command since 1997 until 2000. He was an communication specialist in Managing and designing the Army Helicopter Base communication system. After that, He returned to Chung Yuan Christian University as a Project leader and Computer network administrator. He Led multimedia research groups to construct e-commerce and ERP system for industry. In year 2003, he attended for Higher Education to continue his graduate studies at the University of Texas at Arlington. He is a Research Assistant of Energy Systems Research Center (ESRC), University of Texas at Arlington (UTA), Arlington, Texas. He is also a member of The Institute of Electrical and Electronics Engineers, Inc (IEEE).