DESIGN OF AN ENHANCED TRANSLINEAR VARIABLE RESISTANCE AND ITS APPLICATION IN A VGA

by

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Presented to the Faculty of the Graduate School of

The University of Texas at Arlington in Partial Fulfillment

of the Requirements

for the Degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

THE UNIVERSITY OF TEXAS AT ARLINGTON

August 2006

To my mother Malathi, father Jagannathan, my sister Ramya
and my brother Raghunathan who made me who I am.

ACKNOWLEDGEMENTS

I would like to thank Dr. Ronald Carter for giving me the opportunity to work in his group and trusting me with the projects and thesis. I am very grateful for his support throughout my graduate studies. Thank you Dr. Russell, for patiently spending so much time with me on this thesis and for constantly motivating me in the direction. I am also thankful to Dr. Davis for his suggestions during the meetings and his valuable comments on my thesis document.

I would like to extend my gratitude and love to my parents, sister and brother, who have been extremely supportive, motivating and inspiring.

A very special thanks to Sam, my best friend, for making me realize this thesis in the best possible way. Thank you so much Sam, I couldn't have done it without your support. To my roommates Sethu(for being such a lovely sis), Sirisha(for her tasty dishes) and Kranthi(for her exciting company, and for a lovely time during the winter break) and another very enthused person, Kalyan for being there whenever I needed them.

May 10, 2006

ABSTRACT

DESIGN OF AN ENHANCED TRANSLINEAR VARIABLE
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Publication No. _____

NITHYA JAGANNATHAN, M.S.

The University of Texas at Arlington, 2006

Supervising Professor: Ronald L. Carter

An improved current controlled floating resistor is designed based on translinear loops for application in a Variable Gain Amplifier (VGA). This work compares the use of two different devices and evaluates the difference based on the model parameters and circuit performance. The different architectures employed allow clearly demarcate the performance variations. The translinear variable resistor exhibits a dynamic range greater than 60 mV. The resistance value lies in the range of 3 KΩ to few Ohms. A Current Feedback Operational Amplifier (CFOA) is also designed to have an f_{-3dB} of 250 MHz. The CFOA together with the variable resistor in a difference amplifier configuration constitutes a VGA with a variable voltage gain in the range of 1 to 10. The circuit's intended applications involve frontend of communication systems, temperature sensors, filters etc. The circuit has been implemented using National's VIP10 process, which caters to the high speed bipolar technology. Measurement results obtained are a good

reflection of the various factors that affect the performance and show a good amount of compliance to that of the simulated results.

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CHAPTER 1

INTRODUCTION

Resistors are basic, inexpensive and passive[1] elements of numerous important circuits. They come in magnitudes ranging from tens of Ohms up to millions (mega) of Ohms. They are used to resist and regulate the current flow in a circuit. Broadly, resistors fall in two different classes:

1. Fixed resistors: The value of these resistors do not change.
2. Variable resistors: These resistors have varying resistance values.

The fixed and the variable resistors in turn are divided into two types: passive resistors and active resistors (transistors emulating the behavior of a resistor).

Variable resistors are built using different techniques. The very first set of variable resistors were either a block of carbon (or other equivalent resistive material) with a sliding contact or a box full of carbon granules with a threaded screw to compress the granules, in which more compression leads to lower resistance and vice versa. These devices are rarely used in modern equipment. The rotary variable resistor is the cheapest type of variable resistor. The pre-set resistor is a smaller version used in small electronic classroom type projects. A potentiometer achieves a variation in the value of resistance by converting a simple rotary or linear motion to a change in resistance. It is a simple electro-mechanical transducer. It was originally known as a rheostat (a variable wire wound resistor).

The concept of resistors being variable is useful in providing the user with some degree of flexibility in controlling the circuit in which they are used. There are many

[1]Passive devices are components that do not increase power

methods to vary the resistance of a device. Resistance of a device can be changed by varying the length of the device. However this method is not suitable for the IC world. Resistance can also be changed by increasing or decreasing the current, when the voltage across it is fixed. This scheme is used in this thesis for building variable resistors. When the current is a constant, the voltage can act as a resistance controlling element. Present industry demands within the passive components sector constitutes a wide range of values, higher-frequency performance characteristics, tighter tolerances, and a greater level of stability, all within small packages.

We have come a long way from SSI (Small Scale Integration, containing up to 100 electronic components) to ULSI (Ultra Large-Scale Integration, containing more than 1 million electronic components). Proceeding at such a rate of miniaturization to meet the ever increasing demands for squeezing more components into tighter space and still reach performance requirements, justifies the transition from passive elements to using active components to extract the same behavior. There exists certain tradeoffs in using active components to build variable resistors, but the demands on area garner priority in many applications today. For example, in applications like cell phones, the tinier resistor dies are more attractive because of the miniaturization form factors provided by them. On the other hand, over-voltage protection is mandatory. In certain applications such as medical, making larger-size resistor die prove more appealing.

The physical constraints on present IC designs do not allow the inclusion of standard resistors. However, due to their usefulness resistors have become indispensable. This forms the motivation for us to develop a feasible way to include resistor in the IC design and harness its benefits. In this direction, this thesis comes up with a design of an improved floating resistor based on the exponential behavior of the bipolar transistor effectively employed in translinear loops.

Two types of variable resistors can be found: (1) grounded resistors and (2) floating resistors. Floating resistors are generally preferred to grounded resistors since they can be easily embedded in integrated circuits. The magnitude of the floating resistor can be chosen by appropriately choosing the magnitude of the controlling current. The superiority of the floating resistor is by its linearity and dynamic range. A basic current controlled resistor schematic is modified to enhance its dynamic range and linearity for use in various stringent linearity requirement applications. The schematic implementation of the resistor is based on translinear mixed loops containing bipolar transistors. The combination of two similar translinear loops combined together in a cross coupled nature is intended to improve the dynamic range and linearity in the basic structure [2].

The control over the value of resistance opens up many potential applications to control. Variation of resistance in a circuit can potentially impact many of the system parameters. One of the parameters impacted is the gain of the circuit, which is of utmost interest in most applications. Modifying the resistance with current can be used in Variable Gain Amplifiers (VGA). This feature is extremely useful in devices used in wireless communication, industrial scanning, radar, ultrasound, speech-analysis applications that require a wide dynamic range of continuous voltage, temperature sensors, etc. The concept of variable gain amplification was first seen in the Gilbert Cell. A Gilbert Cell is a cross-coupled differential amplifier, where the gain is controlled by modulating the bias current. Since the gain control is highly linear, Gilbert cells are often referred to as four-quadrant multipliers and have numerous applications, Automatic Gain Control (AGC) circuits, being one of them. The VGA is used in the feedback loop of an AGC, whose output signal has a fixed magnitude for different input strengths. AGC loop is included in wireless systems as the received signal power of all communication systems has wide dynamic range. VGAs in the AGC help maximize the dynamic range of the overall system. Imaging circuits, hearing aids, disk drives, front ends of Analog to Digital

Converters (ADCs), temperature sensors, bandgap reference circuits, are other important areas of application of VGAs.

Three variations of the design of variable resistors are discussed, and they are then embedded in a difference amplifier architecture implemented around a Current Feedback Operational Amplifier (CFOA) to make a VGA. Their performance is evaluated. The chips are fabricated using National's VIP10[2] process, which is meant for high speed analog ICs that are growing rapidly due to the increasing demand for bandwidth. It is dielectrically-isolated, complementary bipolar IC process that utilizes deep trench technology on a bonded wafer for complete dielectrically isolated and optimal high speed amplifier performance. Trench technology with bonded wafers helps minimize parasitic capacitance for optimal power-to-bandwidth performance, lower distortion and decreased die size. Thus it offers the best features combining that of high speed, high bandwidth, low power consumption, low supply voltages, large output swing, high output current and low distortion.

This thesis achieves the following:

- It incorporates improved designs of variable floating resistors and to exemplify their potential, they are deployed with a CFOA to make a VGA.
- Layout and fabrication of the designs.
- Test, measurement and evaluation showing performance differences.

The rest of the thesis is organized as follows: We begin with explaining the building blocks of the VGA in Chapter 2, including the basic translinear element, the three variations in the design of the floating resistor, the design of CFOA, and the concept of the difference amplifier. In Chapter 3, the basic theory behind the VGA configuration is discussed. Chapter 4 contains three floating resistor designs with their schematic simu-

[2]VIP stands for Vertically Integrated PNP and VIP10 is the latest of National's VIP family of complementary bipolar processes.

lation results and their application in a VGA. Chapter 5 provides test results, tabulates the measurements and compares the performances. Chapter 6 concludes the work and provides recommendations for future work.

CHAPTER 2

COMPONENTS OF VGA

Bipolar transistors are governed by the Ebers-Moll equation [3]. The Ebers-Moll equation gives the relationship between the collector current I_c and the voltage drop from base to emitter V_{BE} according to Equation (2.1).

$$I_C = I_S \left[e^{V_{BE}/V_T} - 1 \right] \approx I_S e^{V_{BE}/V_T} \tag{2.1}$$

where, I_s is the reverse leakage current from the emitter to the base,

$V_T = \frac{kT}{q}$,

$q = 1.6\times10^{-19}$ C, is the elementary unit of charge,

$k = 1.38\times10^{-23}$ J/K, is the Boltzmann constant, and T is the absolute temperature in Kelvin.

With typical doping levels, the leakage current arising from the intrinsic behavior of the pure semiconductor is very small, and the second term, 1, becomes negligible, giving a simple exponential dependence of I_c on V_{BE}. Typically $V_{BE} = 600mV \gg V_T$, so the exponential term is much larger than 1, and $I_S \ll I_C$. Equation (2.1) suggests that a change in V_{BE}, ΔV_{BE}, needed to get a tenfold change in I_C is $V_T \ln(10)$ or about 60mV. Thus the collector current increases ten times for a 60mV increase in V_{BE}. A consequence of Ebers-Moll equation is that we see the intrinsic emitter resistance r_e. By definition,

$$\frac{1}{r_e} = \frac{i_E}{V_{BE}} \sim \frac{i_C}{V_{BE}} = \frac{dI_C}{dV_{BE}}$$

The derivative is simply $\frac{i_C}{V_T}$. So $r_e = \frac{V_T}{i_C}$. Section 2.2.1 contains more details on r_e.

2.1 Basic Translinear Element

The circuit adopting exponential I-V characteristic, $I_c = I_s e^{-V_{BE}/V_T}$ or linear dependence of transconductance on bias current, $g_m = I_c/V_T$, of the bipolar transistors are referred to as translinear circuits [4]. A basic translinear loop is shown in Figure 2.1.

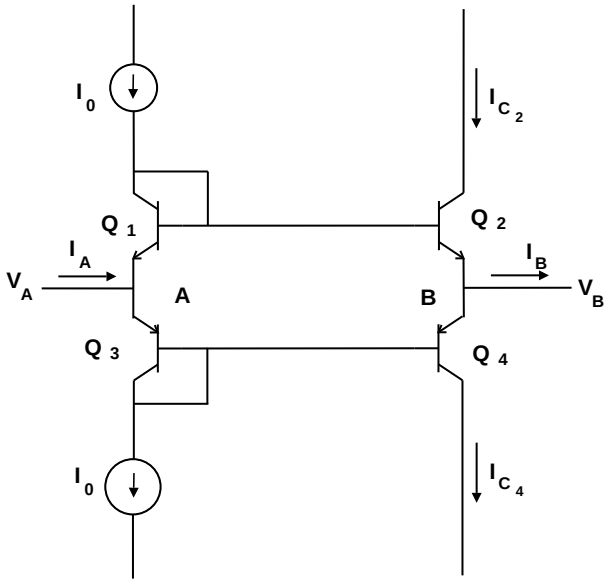

Figure 2.1. Basic translinear loop.

Bipolars conform very accurately to the exponential characteristics over many decades of bias current and so the core of a translinear circuit will normally provide its designed function over a wide dynamic range. Since the circuit behavior is determined by the interplay of transistors in a loop, no overall feedback and no compensation are required. Hence, the *translinear circuits are wideband*. For the purpose of analysis of the basic loop in Figure 2.1, it is assumed that the base currents are negligible.

$$\implies I_o = I_{c_1} = I_{c_3} \quad \text{and} \quad I_A = 0$$

$$I_{c_2} = I_{e_2} = I_{c_4} + I_B$$

$$= I_{e_4} + I_B$$

$$\implies I_{c_2} - I_{c_4} = I_B$$

$$V_A - V_{EB_1} - V_{BE_2} = V_B$$

$$V_A - V_B + V_{BE_1} = V_{BE_2}$$

$$\begin{aligned} I_{c_2} &= I_s \exp\left(\frac{V_{BE_2}}{V_T}\right) \\ &= I_s \exp\left(\frac{V_A - V_B + V_{BE_1}}{V_T}\right) \\ &= I_s \exp\left(\frac{V_{AB} + V_T \ln \frac{I_o}{I_s}}{V_T}\right) \\ &= I_s \exp\left(\frac{V_{AB}}{V_T} + \ln \frac{I_o}{I_s}\right) \\ &= I_s \exp\left(\frac{V_{AB}}{V_T}\right) \frac{I_o}{I_s} \\ I_{c_2} &= I_o \exp\left(\frac{V_{AB}}{V_T}\right) \end{aligned}$$

Similarly,

$$V_B + V_{BE_4} - V_{BE_3} = V_A$$

$$\begin{aligned} V_B - V_A - V_{BE_3} &= V_{EB_4} \\ &= V_B - V_A + V_{EB_3} \\ I_{c_4} &= I_s \exp\left(\frac{V_{EB_4}}{V_T}\right) \\ V_{EB_3} &= V_T \ln \frac{I_c}{I_s} = V_T \ln \frac{I_o}{I_s} \end{aligned}$$

$$\begin{aligned} I_{c_4} &= I_s \exp\left(\frac{V_B - V_A + V_{EB_3}}{V_T}\right) \\ &= I_s \exp\left(\frac{V_{BA} + V_T \ln \frac{I_o}{I_s}}{V_T}\right) \\ &= I_s \exp\left(\frac{V_{BA}}{V_T}\right) \frac{I_o}{I_s} \\ I_{c_4} &= I_o \exp\left(\frac{V_{BA}}{V_T}\right) \end{aligned}$$

Therefore,

$$I_{c_2} = I_o \exp\left(\frac{V_{AB}}{V_T}\right) \quad \text{and} \quad I_{c_4} = I_o \exp\left(\frac{-V_{AB}}{V_T}\right)$$

$$I_B = I_{c_2} - I_{c_4} = I_o \left[\exp\left(\frac{V_{AB}}{V_T}\right) - \exp\left(\frac{-V_{AB}}{V_T}\right)\right]$$

$$= 2I_o \sinh\left(\frac{V_{AB}}{V_T}\right)$$

$$I_{AB} = 2I_o \sinh\left(\frac{V_{AB}}{V_T}\right)$$

$$\text{Since} \quad V_{AB} \ll V_T, \quad I_{AB} \approx 2I_o \frac{V_{AB}}{V_T}$$

$$\text{i.e.,} \quad \lim V_{AB} \to 0, R_{AB} = \frac{V_{AB}}{I_{AB}} = \frac{V_T}{2I_o} = R_{AB,0}$$

$$\boxed{\mathbf{R_{AB,0}} = \frac{V_T}{2\mathbf{I_o}}} \tag{2.2}$$

The current controlled resistance behavior in Equation (2.2) captures the dependence of resistance on the bias current. This behavior is realized in Figure 2.2 by combining two basic translinear cells back-to-back [5].

Treating the two translinear loops independently, the first translinear loop yields I' and the second translinear loop yields I".

$$I' = 2I_o \sinh\left(\frac{V_{AX}}{V_T}\right)$$

$$I'' = 2I_o \sinh\left(\frac{V_{XB}}{V_T}\right)$$

where, X is the floating terminal in each case

This current is a hyperbolic sine function of the ratio of voltages. The hyperbolic sine function is defined as:

$$\sinh x \equiv \frac{1}{2}\left(e^x - e^{-x}\right)$$

This characteristic is shown in Figure 2.3. The circuit in Figure 2.2 reveals a similar characteristic between its current and voltage, i.e., the current does not saturate as the voltage increases.

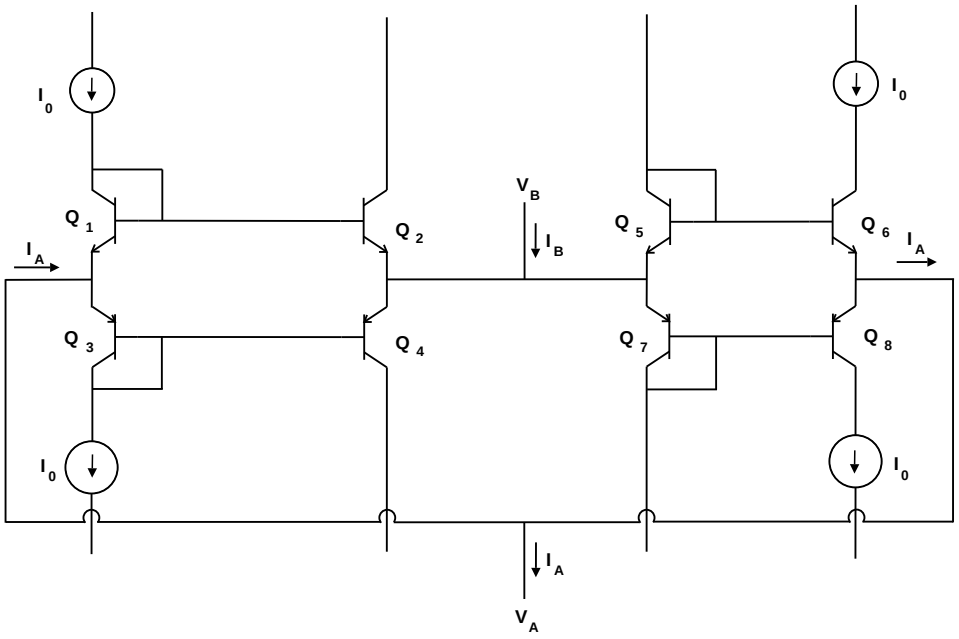

Figure 2.2. Floating resistor based on mixed translinear cells.

This particular circuit configuration was chosen since the nodes A and B impose a low voltage swing on the variable resistor, approximately 60mV, thus remaining well within the dynamic range of the resistor. This configuration also eliminates common mode problems. The design is modified to have buffers connected in place of the simple diode connection over the transistors Q_1, Q_3, Q_5, and Q_7. These buffers are added to prevent current saturation, which in turn leads to good dynamic range as evident from simulation result presented in Chapter 4.

2.2 Cross-coupled Translinear Cell - Expansion of Theoretical Approach

The design explained in the previous section can be extended to include another translinear loop. This loop consists of eight transistors listed below. The overall design also consists of the two basic loops discussed in Secion 2.1. The cross coupled loop enhances the dynamic range and prevents crossover distortion effects.

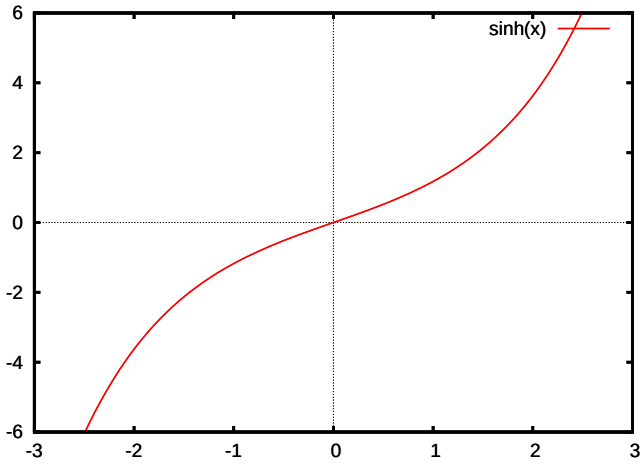

Figure 2.3. Characteristic plot of sinh.

This floating resistor exists between nodes X and Y as shown in Figure 2.4. The schematic is based on three translinear loops of transistors [6].

- Loop 1: Q_1, Q_3, Q_A, Q_C
- Loop 2: Q_5, Q_7, Q_B, Q_D
- Loop 3: Q_A, Q_C, Q_B, Q_D, Q_2, Q_6, Q_8, Q_4

The bias current for diode connected transistors Q_A through Q_D is supplied by I_o. Current mirrors in the schematic (not included in the schematic) allow the duplication of collector currents of Q_2, Q_4, Q_6 and Q_8. It is assumed that the current gain for all transistors, $\beta \gg 1$, which implies that the collector currents of Q_2 and Q_4 and collector currents of Q_8 and Q_6 are equal,

$$\text{i.e.,} \quad I_{c_2} = I_{c_4} \quad \text{and} \quad I_{c_8} = I_{c_6} \tag{2.3}$$

Applying Kirchhoff's law,:

$$I_{c_1} + I_A = I_o + I_{c_6} \tag{2.4}$$

$$I_{c_3} + I_A = I_o + I_{c_4} \tag{2.5}$$

$$I_o + I_{c_2} = I_{c_5} + I_B \tag{2.6}$$

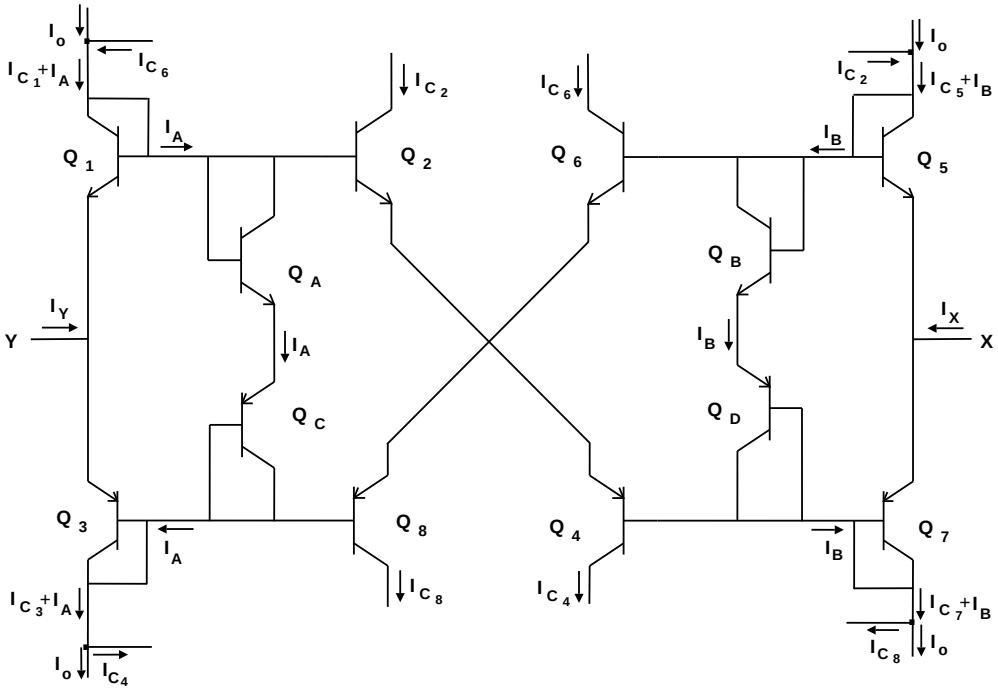

Figure 2.4. Basic schematic of current controlled floating resistor.

$$I_{c_7} + I_B = I_{c_8} + I_o \tag{2.7}$$

Combining 2.3 with 2.4, 2.5, 2.6 and 2.7,

$$\begin{aligned} & I_{c_1} + I_A = I_o + I_{c_6} = I_o + I_{c_8} = I_{c_7} + I_B \\ \implies & I_{c_1} + I_A = I_o + I_{c_6} = I_{c_7} + I_B \end{aligned} \tag{2.8}$$

$$\begin{aligned} & I_{c_3} + I_A = I_o + I_{c_4} = I_o + I_{c_2} = I_{c_5} + I_B \\ \implies & I_{c_3} + I_A = I_o + I_{c_4} = I_{c_5} + I_B \end{aligned} \tag{2.9}$$

Nodal equations at node X:

$$\begin{aligned} I_{c_5} + I_x &= I_{c_7} \\ I_{c_7} - I_{c_5} &= I_x \end{aligned} \tag{2.10}$$

Nodal equations at node Y:

$$\begin{aligned} I_{c_1} + I_y &= I_{c_3} \\ I_{c_1} - I_{c_3} &= -I_y \end{aligned} \tag{2.11}$$

$$I_{c_1} - I_{c_7} = I_B - I_A$$

$$I_{c_3} - I_{c_5} = I_B - I_A$$

$$\implies I_{c_1} - I_{c_7} = I_{c_3} - I_{c_5}$$

$$I_{c_1} - I_{c_3} = I_{c_7} - I_{c_5}$$

Therefore from 2.8, 2.9, 2.10 and 2.11 we get,

$$I_{c_7} - I_{c_5} = I_{c_1} - I_{c_3} = I_x = -I_y \tag{2.12}$$

Assuming all transistors are identical and operate at the same temperature, the three translinear loops yield the following results.

First Translinear loop (Q_1, Q_3, Q_A, Q_C)

This loop, illustrated in Figure 2.5, consists of transistors Q_1, Q_3, Q_A, Q_C.

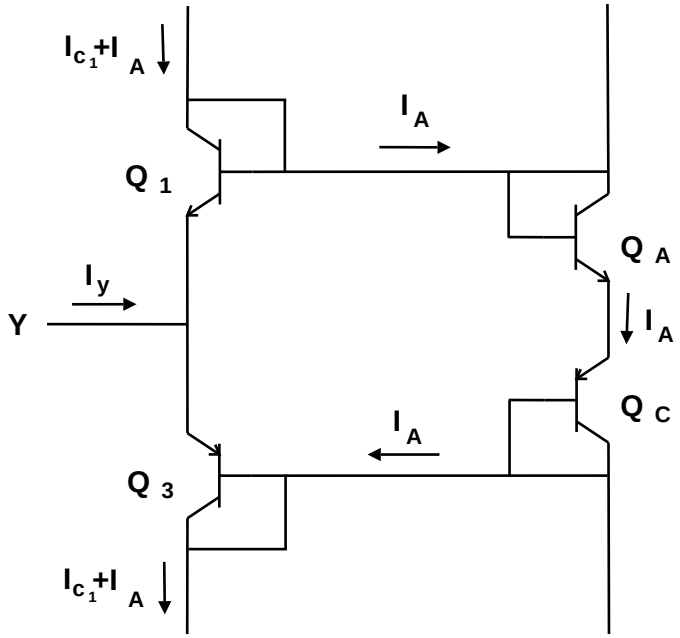

Figure 2.5. First translinear loop.

$$V_{BE_1} + V_{EB_3} = V_{BE_A} + V_{EB_C}$$

$$V_{BE} = V_T \ln\left(\frac{I_c}{I_s}\right)$$

Therefore,

$$V_T \ln\left(\frac{I_{c_1}}{I_{s_1}}\right) + V_T \ln\left(\frac{I_{c_3}}{I_{s_3}}\right) = V_T \ln\left(\frac{I_{c_A}}{I_{s_A}}\right) + V_T \ln\left(\frac{I_{c_C}}{I_{s_C}}\right)$$

$$I_{c_1} I_{c_3} = I_{c_A} I_{c_C}$$

$$= I_A I_A$$

$$I_{c_1} I_{c_3} = {I_A}^2 \tag{2.13}$$

Second translinear loop (Q_5, Q_7, Q_B, Q_D)

This loop is illustrated in Figure 2.6 and consists of transistors Q_5, Q_7, Q_B, Q_D.

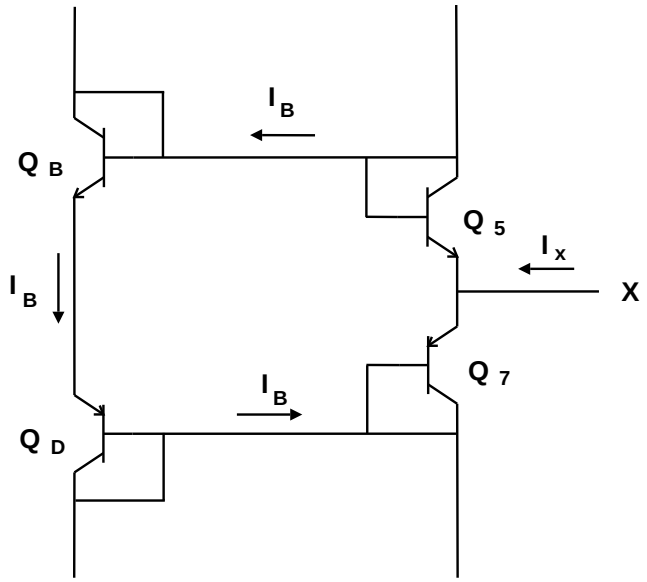

Figure 2.6. Second translinear loop.

$$V_{BE_B} + V_{EB_D} = V_{BE_5} + V_{EB_7}$$

$$I_{c_B} I_{c_D} = I_{c_5} I_{c_7}$$

$$I_B I_B = I_{c_5} I_{c_7}$$

$$I_{c_5} I_{c_7} = {I_B}^2 \tag{2.14}$$

Third translinear loop ($Q_A, Q_C, Q_B, Q_D, Q_2, Q_6, Q_8, Q_4$)

This loop is illustrated in Figure 2.7 and consists of transistors Q_A, Q_C, Q_B, Q_D, Q_2, Q_6, Q_8, Q_4.

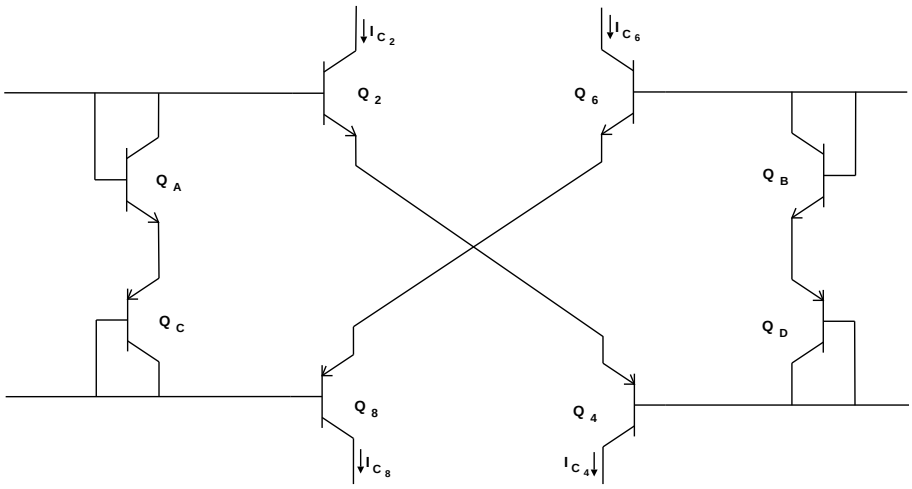

Figure 2.7. Third translinear loop.

$$V_{BE_2} + V_{EB_4} = V_{BE_B} + V_{EB_D}$$

$$I_{c_2} I_{c_4} = I_B I_B$$

$${I_{c_2}}^2 = {I_B}^2$$

$${I_{c_6}}^2 = {I_A}^2$$

$$I_{c_2} I_{c_6} = I_A I_B \tag{2.15}$$

The collector currents I_{c_1}, I_{c_6} and I_{c_7} can be expressed from Equations (2.14) through (2.15), as a function of I_y (with I_y=-I_x) and the diode current I_A and I_B. Replacing, I_{c_1},

I_{c_6} and I_{c_7} in Equations (2.8) and (2.9) with these expressions results in $I_A = I_B = I_o$. Then allowing I_x=0, all collector currents become identical and equal to I_o.

Now from Equation (2.14)

$$I_{c_1} I_{c_3} = {I_A}^2 = {I_o}^2$$

From Equation (2.11),

$$I_{c_1} - I_{c_3} = I_x = -I_y$$

$$I_{c_1} + I_y = I_{c_3}$$

$$I_{c_1} (I_{c_1} + I_y) = {I_o}^2$$

$${I_{c_1}}^2 + I_{c_1} I_y - {I_o}^2 = 0$$

$$I_{c_1} = \frac{-I_y \pm \sqrt{{I_y}^2 + 4{I_o}^2}}{2}$$

$$= -\frac{I_y}{2} \pm \frac{\sqrt{{I_y}^2 + 4{I_o}^2}}{2}$$

$$I_{c_1} = -\frac{I_y}{2} + \frac{\sqrt{{I_y}^2 + 4{I_o}^2}}{2}$$

$$I_{c_5} I_{c_7} = {I_B}^2$$

$$I_{c_7} - I_{c_5} = I_x = -I_y$$

$$I_{c_5} = I_{c_7} + I_y$$

$$(I_{c_7} + I_y) I_{c_7} = {I_B}^2$$

$${I_{c_7}}^2 + I_{c_7} I_y = {I_B}^2$$

$$I_{c_7} = -\frac{I_y}{2} + \frac{\sqrt{{I_y}^2 + 4{I_o}^2}}{2}$$

$$I_{c_1} = I_{c_7}$$

$$I_o + I_{c_6} = I_{c_7} + I_B$$

$$I_o + I_{c_6} = I_{c_7} + I_o$$

$$I_{c_6} = I_{c_7} \quad \text{and} \quad I_{c_6} = I_{c_8}$$

Therefore,

$$\begin{aligned} I_{c_1} = I_{c_7} = I_{c_6} = I_{c_8} \\ = -\frac{I_y}{2} \pm \frac{\sqrt{{I_y}^2 + 4{I_o}^2}}{2} \end{aligned} \tag{2.16}$$

$$I_{c_1} I_{c_3} = {I_o}^2$$

$$\implies I_{c_3} = \frac{{I_o}^2}{I_{c_1}}$$

$$I_{c_1} - I_{c_3} = -I_y$$

From Equation (2.11),

$$I_{c_1} = I_{c_3} - I_y$$

$$I_{c_3} = \frac{{I_o}^2}{(I_{c_3} - I_y)}$$

$$I_{c_3} (I_{c_3} - I_y) = {I_o}^2$$

$${I_{c_3}}^2 - I_{c_3} I_y - {I_o}^2 = 0$$

$$I_{c_3} = \frac{I_y}{2} + \frac{\sqrt{{I_y}^2 + 4{I_o}^2}}{2} \tag{2.17}$$

$$I_{c_5} I_{c_7} = {I_o}^2 = {I_B}^2$$

$$I_{c_7} - I_{c_5} = -I_y$$

where,

$$I_{c_7} = I_{c_5} - I_y$$

$$I_{c_5} (I_{c_5} - I_y) = {I_o}^2$$

$${I_{c_5}}^2 - I_{c_5} I_y - {I_o}^2 = 0$$

$$I_{c_5} = \frac{I_y}{2} + \frac{\sqrt{{I_y}^2 + 4{I_o}^2}}{2} \tag{2.18}$$

From Equations (2.17) and (2.18),

$$\implies I_{c_5} = I_{c_3} \tag{2.19}$$

$$I_o + I_{c_4} = I_{c_3} + I_o$$
$$\implies I_{c_3} = I_{c_4}$$

$$\begin{aligned} I_{c_2} = I_{c_4} = I_{c_3} = I_{c_5} \\ = \frac{I_y}{2} + \frac{\sqrt{{I_y}^2 + 4{I_o}^2}}{2} \end{aligned} \tag{2.20}$$

Equations (2.16) and (2.20) indicate that all collector currents are positive and hence it is class AB [7].

The voltage difference between nodes Y and X, V_{yx} is calculated as shown below.

$$\begin{aligned} V_y - V_x &= V_{EB_3} - V_{EB_8} - V_{BE_6} + V_{BE_5} \quad \text{(or)} \\ &= -V_{BE_1} + V_{BE_2} + V_{EB_4} - V_{EB_7} \\ V_{yx} &= V_T \ln\left(\frac{I_{c_3}}{I_{s_3}}\right) - V_T \ln\left(\frac{I_{c_8}}{I_{s_8}}\right) - V_T \ln\left(\frac{I_{c_6}}{I_{s_6}}\right) + V_T \ln\left(\frac{I_{c_5}}{I_{s_5}}\right) \\ &= V_T \ln\left(\frac{I_{c_3} I_{c_5}}{I_{c_8} I_{c_6}}\right) \\ &= V_T \ln\left(\frac{{I_{c_3}}^2}{{I_{c_6}}^2}\right) \qquad \text{(From Equation (2.19) and since } I_{c_6} = I_{c_8}\text{)} \\ &= V_T \ln\left(\frac{I_{c_3}}{I_{c_6}}\right)^2 \end{aligned}$$

Using Equations (2.16), (2.17) and $I_A = I_o = I_{c_6}$, we have,

$$I_{c_3} = I_o e^{(V_{yx}/4V_T)}$$

Similarly,

$$I_{c_1} = I_o e^{(-V_{yx}/4V_T)}$$

$$\begin{aligned} I_y &= I_{c_3} - I_{c_1} \\ &= 2I_o \left(\frac{e^{(V_{yx}/4V_T)} - e^{(-V_{yx}/4V_T)}}{2} \right) \end{aligned}$$

$$I_y = 2I_o \sinh \left(\frac{V_{xy}}{4V_T} \right) \tag{2.21}$$

Therefore under the assumption, $|V_{xy}| \ll V_T$ Equation (2.21),

$$I'_y = 2I_o \left(\frac{V_{xy}}{4V_T} \right)$$

$$\implies R_{xy,0} = \frac{2V_T}{I_o} \tag{2.22}$$

2.2.1 Linearization techniques and dynamic range Expansion

The floating resistor design presents the challenge of linearity and dynamic range extension. The circuit idea from [6] has been improvised upon to meet this challenge. Initially the design consisted of a particular type of bipolar transistor which resulted in the output current to be saturated at very low values. Probing into the model file of the device revealed that the emitter resistance, r_e, was large and this caused the current to saturate. The value of r_e is given by Equation (2.23) and illustrated in Figure 2.8.

$$r_e = \frac{V_T}{I_c} = \frac{25mV}{I_c} \tag{2.23}$$

Essentially one can treat this as any other resistance. Numerically, typical values reveal that r_e is safely ignored. For example, $I_C = 1mA$ gives $r_e = 25\Omega$, whereas an external resistance in the emiter, R_E might be typically $\sim 1k\Omega$. The exception is an emitter follower output, where the output voltage is divided between r_e and R_E. The

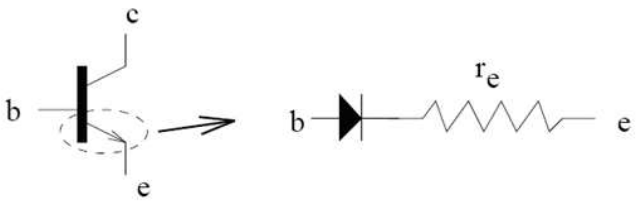

Figure 2.8. Emitter Resistance.

resistance, r_e, prevents the output resistance from getting too small. In some cases an external emitter resistor R_E is omitted. Thus, at a collector current of 1 mA, the effective emitter resistance is 25 Ω. This means that drawing 1 mA from the emitter would cause the emitter voltage to fall by 25 mV. A low resistance source (e.g., power supply, power amplifier) requires a large I_C. So, transistors for these applications are run at large quiescent currents. Hence this device was replaced by another type whose r_e was one-sixth of the previous one. This greatly enhanced the current levels at the output.

The emitter degeneration resistors were added to the current mirrors in the design so as to improve matching and linearity properties. Any mismatch manifests itself as a big problem during measurement using silicon. So care must be taken during the design stage to decrease any undesirable impacts of mismatch. The floating resistors can be applied to numerous applications. One of the major application of interest in this thesis is its use in a Variable Gain Amplifier. Other interesting applications include filters, current mirrors and temperature sensors. The PTAT (Proportional To Absolute Temperature) current source can be used to control the floating resistor value, thereby enabling temperature sensing.

2.3 Current Feedback Operational Amplifier

The Current Feedback Operational Amplfier (CFOA) is used in the VGA system. The CFOA is chosen because its bandwidth is dependent on due to the fact tthe closed

loop gain unlike the Voltage Feedback Amplifier (VFA), where the gain-bandwidth product is constant. The closed loop bandwidth of the CFOA is almost constant with the closed loop gain settings in the range of 1 to 10. Thus a CFOA is preferred for applications requiring variable closed loop gains with constant bandwidth, such as in automatic gain control applications. The CFOA also exhibits a much better differential gain and phase performance than typical the VFA [1].

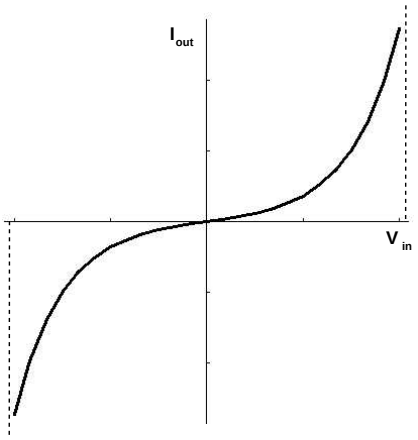

Figure 2.9. Output characteristic curve of CFOA.

Current feedback operational amplifiers are well known for their high slew rate. Slew Rate (SR) is very important because it is a major cause of high frequency distortion in high frequency amplifiers. Initially, the limitation in the amount of current available for slewing was due to the fixed bias current in the input stage of the differential amplifier. The slew rate can be increased by making the amount of bias current proportional to the input voltage. A very high slew rate is usually obtained using current as the feedback error signal. Typical SR values for CFOAs are 500 to 2500 $V/\mu s$, while that of VFAs are on the order of 100 $V/\mu s$.

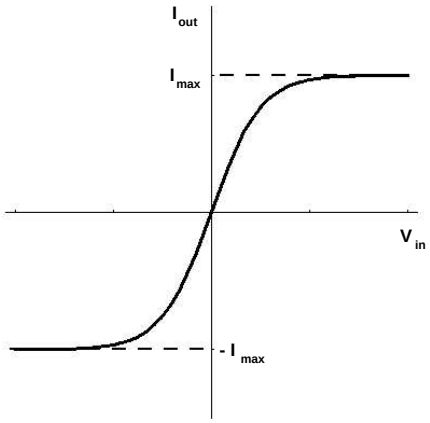

Figure 2.10. tanh characteristics.

The analysis of the CFOA shows that the frontend transconductance is a hyperbolic sine function. This non-saturating transconductance provides for the unlimited slew-rate capability. This implies low distortion for large amplitude, high frequency inputs. The transconductance of the Voltage Operational Amplfier (VOA) is slew-rate limited due to the maximum fixed current available and the total load impedance. Its output characteristic is governed by a hyperbolic tangent function, which is saturating by nature as shown in Figure 2.10.

The design of the CFOA uses a double buffer [8] as shown in Figure 2.11. This double buffer is based on complementary bipolar high-speed transistors. It is a cascade of two emitter follower structures. It provides near unity voltage gain and isolates the high impedance current summing node from the amplifier load. The amplifier provides for very high bandwidth at the expense of open-loop transimpedance. This loss is acceptable in high-speed applications in which these amplifiers are employed. The double buffer is a simple class AB output stage that operates as a four transistor emitter follower to

maintain the output voltage swing and output current to the load. The output voltage swing is,

$$V_o{}^+ \approx V_{CC} - [V_{BE} + V_{sat}] \approx V_{CC} - 1V$$

$$V_o{}^- \approx V_{EE} + [V_{BE} + V_{sat}] \approx V_{EE} + 1V$$

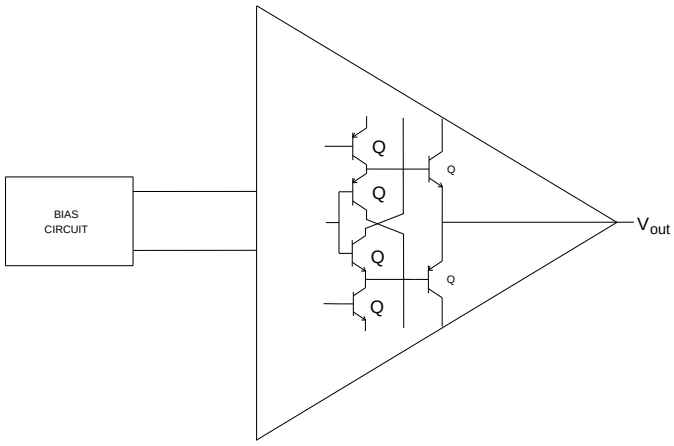

Figure 2.11. CFOA implementing double buffer output stage [1].

The architectural benefits of the CFOA include wide bandwidth and slew rate at low supply currents. The closed loop bandwidth is independent of the closed loop gain and the amplifier's stability is dependent of the feedback resistor value. The CFOA is characterized by its transimpedance gain. However, CFOAs exhibit higher noise gain (explained in Section 2.5) than VFAs. A common error in implementing a current feedback amplifier is to short the output to the inverting input in order to configure a unity gain buffer. This will cause the circuit to oscillate. The circuit requires the recommended feedback resistor in the feedback in place of the short to maintain stability. In this design, the slew rate is quite high, due to the large transient currents that flow in the input stage to handle rapid changes in voltage across the compensating capacitor. Also, the low impedance at the negative input makes sure that the stray input capacitance will

not substantially affect the amplifier's bandwidth. The impedance at the inverting input terminal sets the bandwidth and therefore the stability of the amplifier.

2.4 Difference Amplifier

The difference amplifier configuration shown in Figure 2.12 is chosen to implement the VGA since it combines the features of both non-inverting and inverting amplifiers. For correct circuit operation, it is important that the two resistor ratios be matched. The bridge condition is satisfied when $R_4/R_3 = R_2/R_1$. This circuit operates cleanly and accurately, but does have a limitation. It cannot be used to sum multiple signals at the inverting(-) input because that input is no longer at a virtual ground. As a result, additional input signals to this point will interact with each other and produce distorted results. If all the resistor values are equal, this amplifier will have a differential voltage gain of 1. The analysis of this circuit is essentially the same as that of an inverting amplifier, except that the noninverting input (+) of the op-amp is at a voltage equal to a fraction of V_2, rather than being connected directly to ground. As would stand to reason, V_2 functions as the noninverting input and V_1 functions as the inverting input of the final amplifier circuit. Therefore,

$$V_o = \frac{R_2}{R_1}(V_2 - V_1)$$

If a differential gain of anything other than 1 is desired then the resistors in both the upper and lower voltage dividers need to be adjusted. This would necessitate multiple resistor changes and a need to balance the two dividers for symmetrical operation. This is not always practical. Thus, introducing the current controlled floating resistor R_{float} in between the two nodes A and B in a way that affects the gain is preferred. This is shown in Figure 2.13 In this case only R_{float} has to be varied to achieve the desired differential gain.

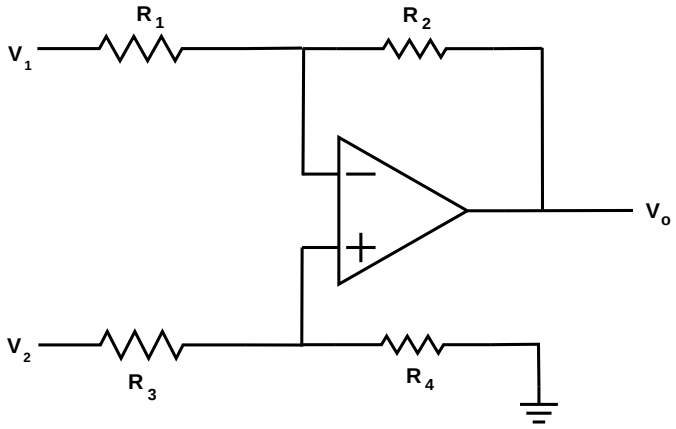

Figure 2.12. Difference Amplifier.

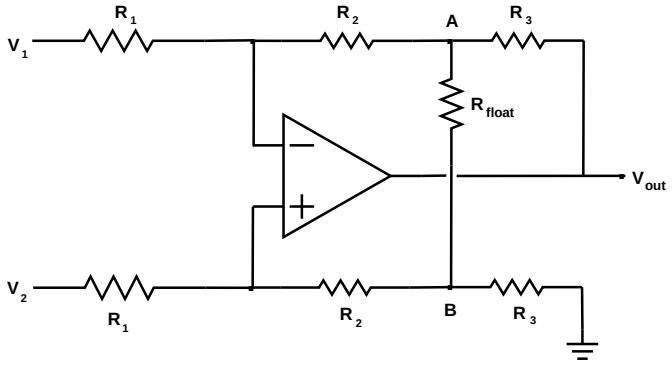

Figure 2.13. Difference amplifier including floating resistor R_{float}.

2.4.1 Relation between R_{float}, V_1 and V_2

$$\frac{V_1 - V_n}{R_1} + \frac{V_A - V_n}{R_2} = I_n \tag{2.24}$$

$$\frac{V_2 - V_p}{R_1} + \frac{V_B - V_p}{R_2} = I_p \tag{2.25}$$

$I_n = I_p = 0$, and the gain being large, $V_n = V_p$.

$$\frac{V_n - V_A}{R_2} + \frac{V_o - V_A}{R_3} = \frac{V_A - V_B}{R_{float}}$$

$$\frac{V_n - V_B}{R_2} + \frac{0 - V_B}{R_3} = \frac{V_B - V_A}{R_{float}}$$

$$2.24 - 2.25 \implies (V_1 - V_n)\,G_1 + (V_A - V_n)\,G_2 - (V_2 - V_n)\,G_1 - (V_B - V_n)\,G_2 = 0$$

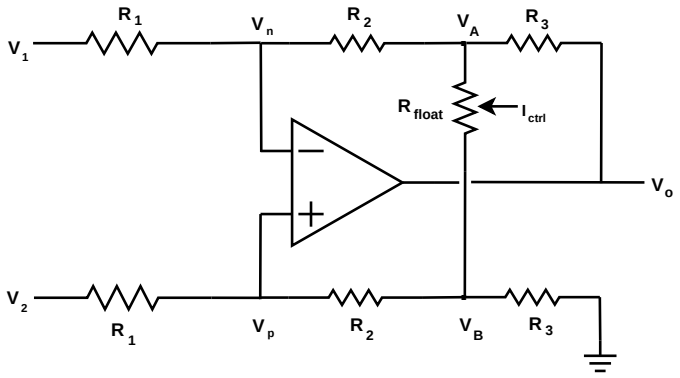

Figure 2.14. VGA configuration.

$$
\begin{aligned}
(V_1 - V_2)\, G_1 + (V_A - V_B)\, G_2 &= 0 \\
\frac{V_A - V_B}{R_2} &= \frac{V_2 - V_1}{R_1} \\
\frac{V_n - V_A}{R_2} + \frac{V_o - V_A}{R_3} - \frac{V_n - V_B}{R_2} - \frac{0 - V_B}{R_3} &= \frac{V_A - V_B}{R_{float}} - \frac{V_B - V_A}{R_{float}} \\
\frac{V_n - V_A - V_n + V_B}{R_2} + \frac{V_o - V_A + V_B}{R_3} &= \frac{V_A - V_B - V_B + V_A}{R_{float}} \\
\frac{V_B - V_A}{R_2} + \frac{V_o + (V_1 - V_2)\,\frac{R_2}{R_1}}{R_3} &= \frac{2\,(V_2 - V_1)\,R_2}{R_1 R_{float}} \\
(V_1 - V_2)\left[\frac{1}{R_1} + \frac{R_2}{R_1 R_3} + \frac{2R_2}{R_1 R_{float}}\right] &= -\frac{V_o}{R_3} \\
(V_2 - V_1)\left[\frac{R_3}{R_1} + \frac{R_2}{R_1} + 2\frac{R_2 R_3}{R_1 R_{float}}\right] &= V_o \\
\frac{V_o}{V_2 - V_1} = \frac{R_3}{R_1} + \frac{R_2}{R_1} + 2\frac{(R_2 R_3)}{R_1 R_{float}} &= \frac{1}{R_1}\left(R_3 + R_2 + 2\frac{R_2 R_3}{R_{float}}\right)
\end{aligned}
$$

As R_{float} increases, gain decreases. If $R_3 = R_2$ then,

$$
\begin{aligned}
\frac{V_o}{V_2 - V_1} &= \frac{1}{R_1}\left(2R_2 + 2\frac{{R_2}^2}{R_{float}}\right) \\
\frac{V_o}{V_2 - V_1} &= 2\frac{R_2}{R_1}\left(1 + \frac{R_2}{R_{float}}\right)
\end{aligned}
\tag{2.26}
$$

Thus from Equation (2.26), it is clear that gain can be varied using the single resistor R_{float}.

2.5 Noise Gain

Noise gain is the reciprocal of the attenuation from the output of an opamp (or any feedback loop) to the input. Noise gain from 1 to 2000 will suffice for most opamps. But amplifiers with a specified gain of 10 minimum have excessive phase shift at high frequencies. They will surely oscillate if the noise gain is not at least 10. The inverting input noise current tends to be higher in a CFOA. Hence, the drawback of this VGA configuration is noise gain. A powerful way to maintain stability in low-frequency applications involve increasing the circuit's closed-loop gain (i.e., noise gain) without changing signal gain, thus reducing the frequency at which the product of open-loop gain and feedback attenuation goes to unity.

CHAPTER 3

VARIABLE GAIN AMPLIFIER

Variable Gain Amplifiers (VGA) find numerous applications, some of which are hearing aids, disk drives, pre-amplifiers with Automatic Gain Control (AGC) for Asymmetric Digital Subscriber Line (ADSL), and front-ends of many communication systems to increase dynamic range of the receivers. In wireless communication systems, the amplitudes of the receiver and the transmitter signals vary by a large amount such that very wide gain control range VGAs are needed. For example, a CDMA receiver requires at least 80 dB of dynamic gain range.

3.1 AVGA vs. DVGA

A VGA controlled by digital signals, is composed of a series of switchable gain stages. A VGA controlled by analog signals typically adopt variable transconductance or resistance stages for the gain variation. The AVGA is preferred over the DVGA as the AVGA tends to require fewer gain control signals [9].

3.2 Exponential Function Generators in CMOS Technology

VGAs in wireless transceivers are usually embedded in an AGC to provide an output signal with constant amplitude. Therefore, to minimize the settling time of the AGCs, the gain of the VGA has to be an exponential transfer function of the control signal [10].

The classical wideband VGAs were based on the Gilbert gain cell [11] whose gain is accurately controlled by the ratio of bias currents. For the design presented, initially the

Table 3.1. Comparison of methods to extract exponential characteristics from MOSFET

Methods	Pros	Cons
Master Slave Control and Signal Summing Technique	dB linear gain characteristic	less than 20dB gain variation per one-stage VGA
Taylor Concept and Pseudo Exponential Generator	dB linear gain characteristic	Give less gain control range (12 to 15 dB with a gain error of less than +/- 0.5 dB respectively
Multiple Stage VGA	Satisfy wide gain variations of communication systems	High power consumption and a large chip size or high cost
VGA adopting BJT: translinear circuits	Wide exponential gain control	Not compatible with standard CMOS based circuits
BiCMOS VGA	Provide acceptable gain control	Not Cost effective
PMOS transistor with the body terminal as a control signal for varying the gain	Has wide gain control range and low power consumption	Has to have linearization technique to improve linearity

suitability of MOS device was analyzed. Since MOSFETs exhibit square law behavior in the saturation region and exponential characteristics in weak inversion (which can be adopted only for low frequency applications) there has been a drive to look into other ways of extracting the exponential characteristic from MOSFETs [12] [13]. Extracting the exponential characteristic from MOSFETs [14] [15] in the desired region of operation is useful in the sense; it enables enjoying the benefits of bipolar technology in the highly scalable MOS technology. This is usually realized by one of the methods shown in Table 3.1.

The parasitic bipolar transistors in a CMOS technology, shown in Figure 3.1 ,have two collectors available: the vertical to substrate, which always exists in the well and the lateral which may optionally be added by a diffusion surrounding the emitter. The well acts as a base.

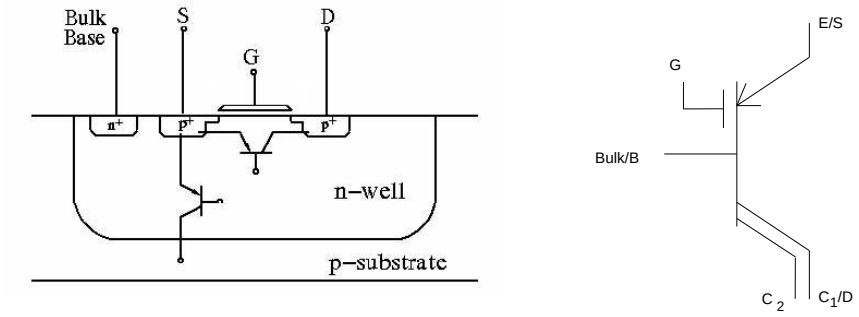

Figure 3.1. Structure of lateral and vertical bipolars in a CMOS well.

Table 3.2. Comparison of lateral and vertical parasitic bipolar transistors

Vertical BJT	Lateral BJT
Used in bandgap reference voltage circuit and emitter followers to drive small capacitor lines on SRAM chips.	Used in opamp's input stages with low offset voltages and in improved bandgap references.
Beta Vertical is two times greater than lateral	Laterals obey IV characteristics over large decades of current. Typical beta is 100 over 5 decades of current

The comparison of the lateral and vertical parasitic transistors is presented in Table 3.2

The disadvantages of the vertical BJT is that its collector is always tied to the substrate of the chip and so to one of the power supplies. Hence, its use is severely limited. The lateral BJT however offers free collector at the expense of unavoidable vertical collector, that is inherited form the bottom area of the wall. Standard way of suppressing the vertical collector in Bipolar IC technology is the buried layer. This is not supported by a standard CMOS.

Since National's technology being used is highly specialized for extremely high performance bipolar transistors, it was decided to continue the design of VGA with the

transistors supported by this technology so that it can be fabricated and its performance studied in more detail.

CHAPTER 4

SIMULATION RESULTS

The design phase consists of three different modules. Each module is designed using Perfect10c technology of National Semiconductor Inc. The DC and transient response are studied and the schematic simulation results for these designs are provided.

4.1 Simulation Results for Mixed Translinear Cell Based Floating Resistor

The first module is the design of an enhanced floating resistor described in Section 2.2.1 using buffers in place of diode connections. In this design all the transistors in the translinear loop are matched. The simulation result for a small range of ΔV, where the relationship of I to V is nearly linear, is plotted for a contant I_{ctrl} in Figure 4.1.

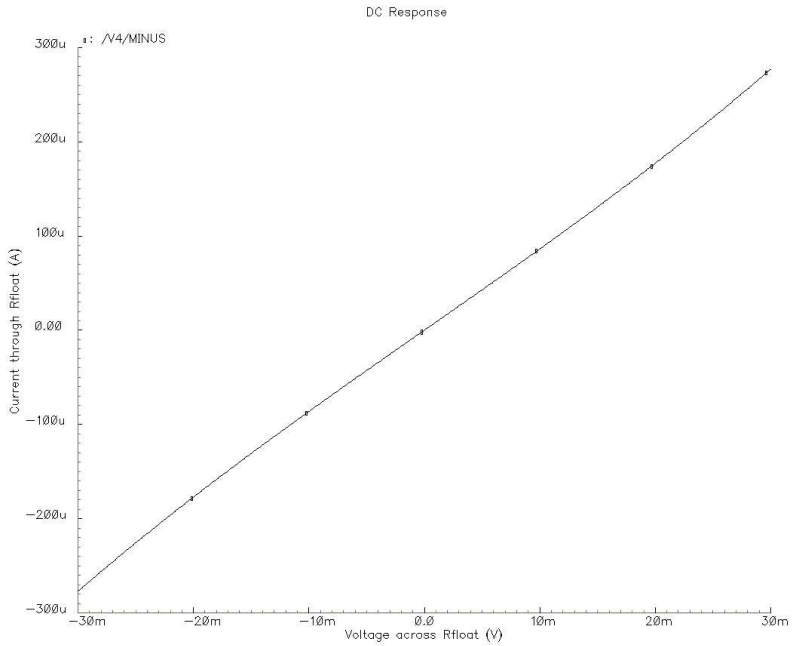

Figure 4.1. Design 1: Transconductance plot for a constant I_{ctrl}.

The plot in Figure 4.1 verifies that it is safe to assume an input dynamic range of 60 mV for applications employing it. For a higher voltage across the floating resistor the through current tends to saturate. This saturation occurs due to a current limiting factor in the emitter of the transistor in the translinear loop. The buffers in place of simple diode connections supply the extra current required and hence prevent early saturation. This result is presented in Figure 4.2 for varying values of the controlling current. The deviation from the linear behavior beyond the 60 mV range leads to prominent variations in the floating resistor value for a constant control current (illustrated in Chapter 5), which is undesirable. Hence it is recommended to operate the floating resistor only within this range to get the desired performance.

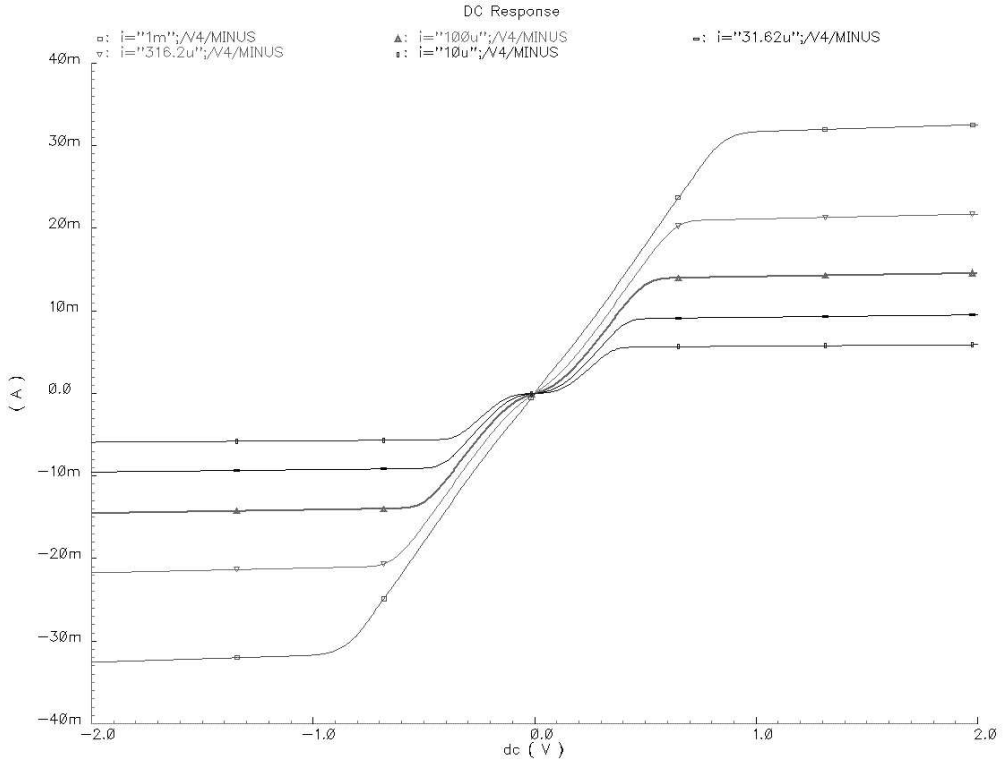

Figure 4.2. Design 1: Transconductance plot for varying I_{ctrl}(i).

The change in the value of the floating resistor as the control current changes is demonstrated in Figure 4.3. From the plot in Figure 4.3, it can be inferred that resistance in the range of 3 $K\Omega$ to a few Ohms is achievable when the control current varies from 100 nA to 1 mA. Such a wide range of the controlling parameter permits the choice of resistance accurately.

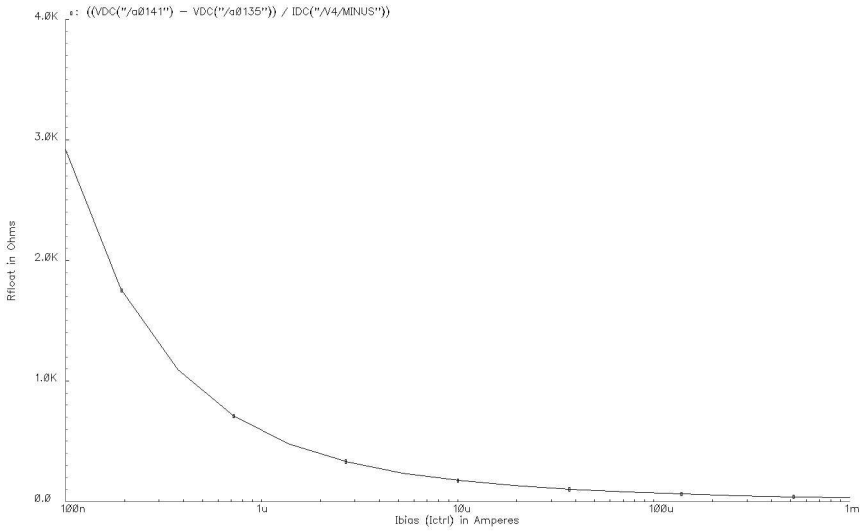

Figure 4.3. Design 1: R_{float} vs I_{ctrl}.

The schematic of this floating resistor was employed in a simple voltage divider configuration shown in Figure 4.4 and its simulation results are presented in Figure 4.5. The value of the floating resistor is treated as unknown for a constant control current and the transient analysis is run for a constant passive load resistor R_{load} of 330 Ω and shown in Figure 4.5. The value of this unknown is then precisely calculated by observing the peaks of the signals V_{in} and V_{out} in Figure 4.5 and applying it in the formula: $\left(\frac{V_{out}}{V_{in}} - 1\right) * R_{load}$. This analysis is based on the discussion in Chapter 5.

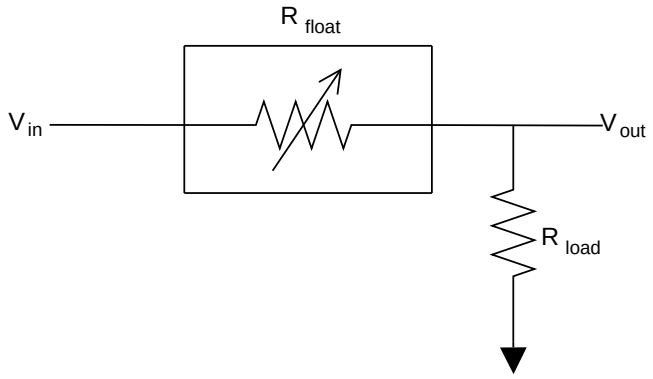

Figure 4.4. Testbench for transient analysis.

The Discrete Fourier Transform (DFT) of the input and output signals are given in Figures 4.6 and 4.7.

In the DFT analysis of the input signal shown in Figure 4.6, it is seen that there are other harmonics present even though the source is ideal. These harmonics are mainly due to the rounding effect of the mathematical model used in the DFT analysis. Thus, they can be treated as noise. Extending the number of samples to 128 or 1024 does not change the noise level. The DFT analysis of the output signal in Figure 4.7 shows a 3^{rd} harmonic component at -44.28 dB. This effect is greatly reduced in the next design which includes a cross coupled translinear loop.

4.2 Simulation Results for the Cross Coupled Loop Based Floating Resistor

The second design module is based on the analysis in Section 2.2.1 on cross coupled translinear loops. DC and transient analysis are performed by sweeping the control current from 10 μA to 1 mA. The transconductance plot is shown in Figure 4.8. This figure also shows a good linear response in a range greater than 60 mV and the inherent non-linearity and saturation of currents can be observed.

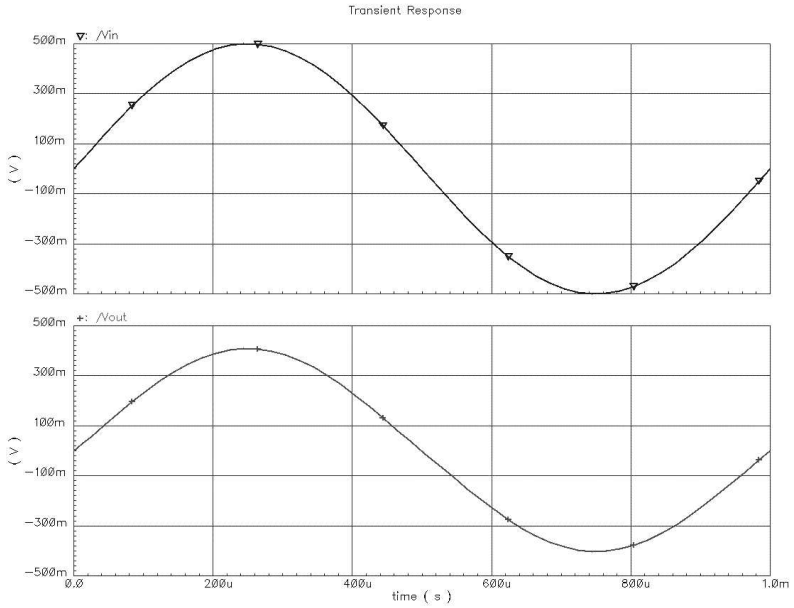

Figure 4.5. Design 1: Transient response.

The variation of resistance with respect to the variation in the value of the control current is simulated and presented in Figure 4.9. In contrast to Figure 4.3, the range of control current over which the same change in resistance occurs is reduced in Figure 4.9. This is overcome by the fact of achievable linear range which is greater than 60 mV for this case.

A similar transient response is taken for this design module also and it is used to calculate the value of the unknown floating resistor at a constant control current. This response is illustrated in Figure 4.10. The value of the floating resistor is calculated as described for the first module and it is verified against the simulation results in Figure 4.9.

The DFT analysis of the input and output signals are given in Figures 4.11 and 4.12. The output signal has a considerable decrease in its 3^{rd} harmonic content around -110 dB.

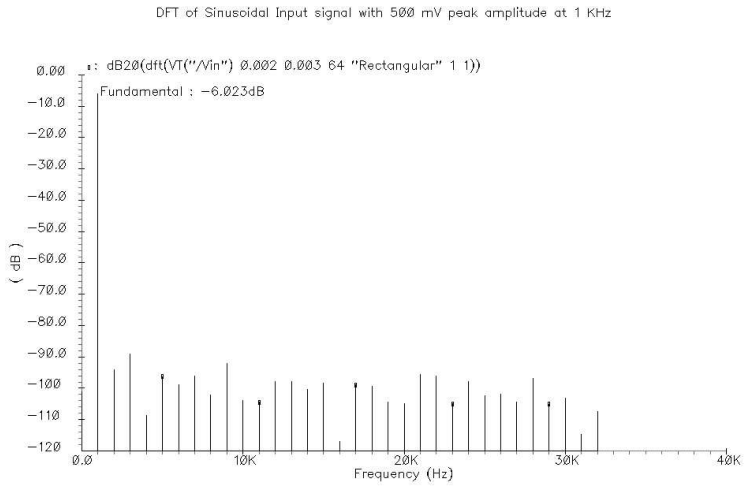

Figure 4.6. Design 1: DFT of input signal.

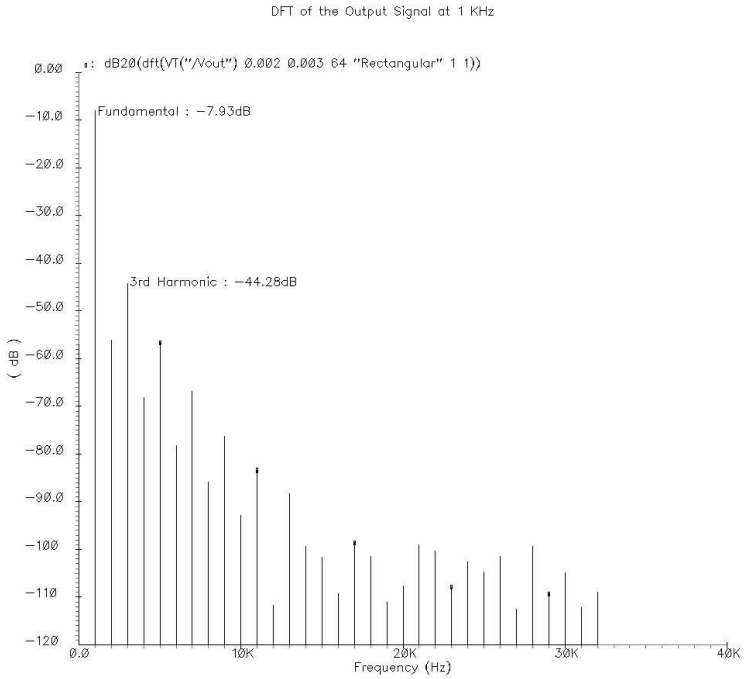

Figure 4.7. Design 1: DFT of output signal.

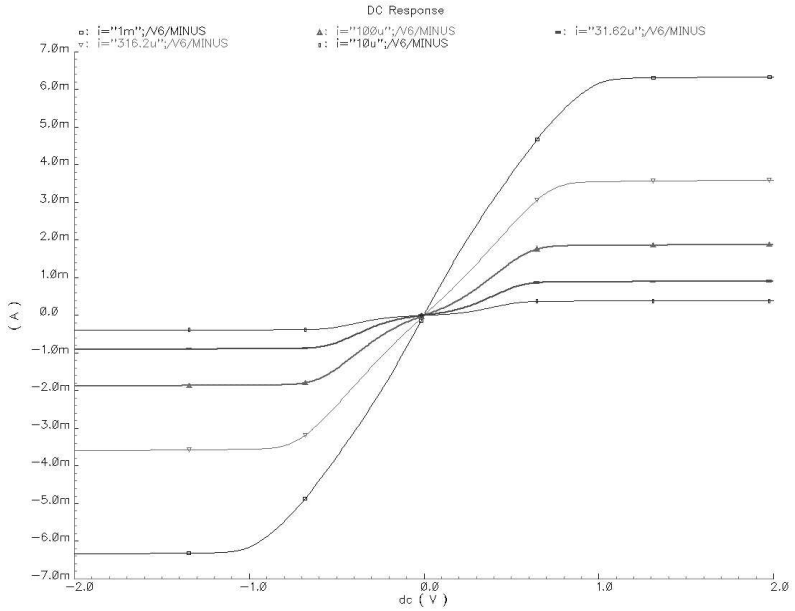

Figure 4.8. Design 2: Transconductance plot for varying $I_{ctrl}(i)$.

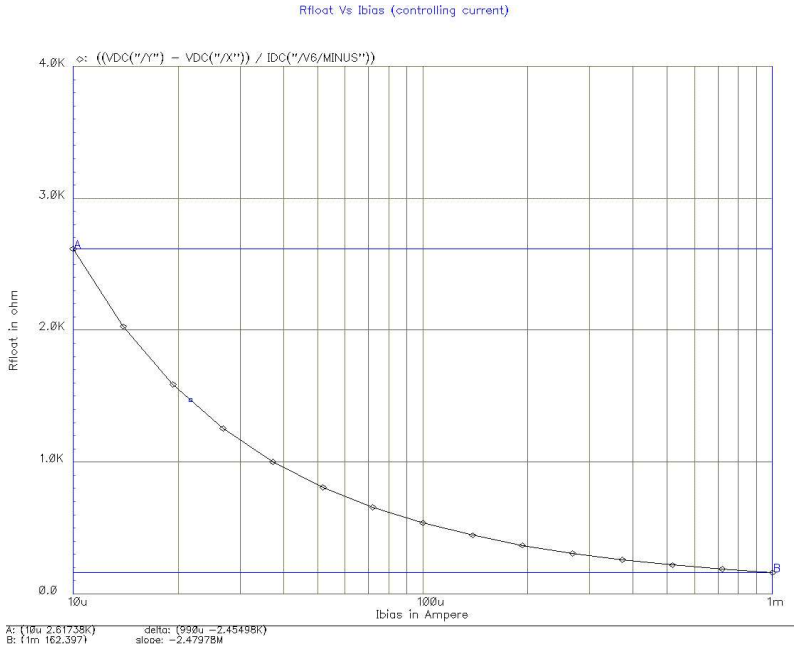

Figure 4.9. Design 2: R_{float} vs I_{ctrl}.

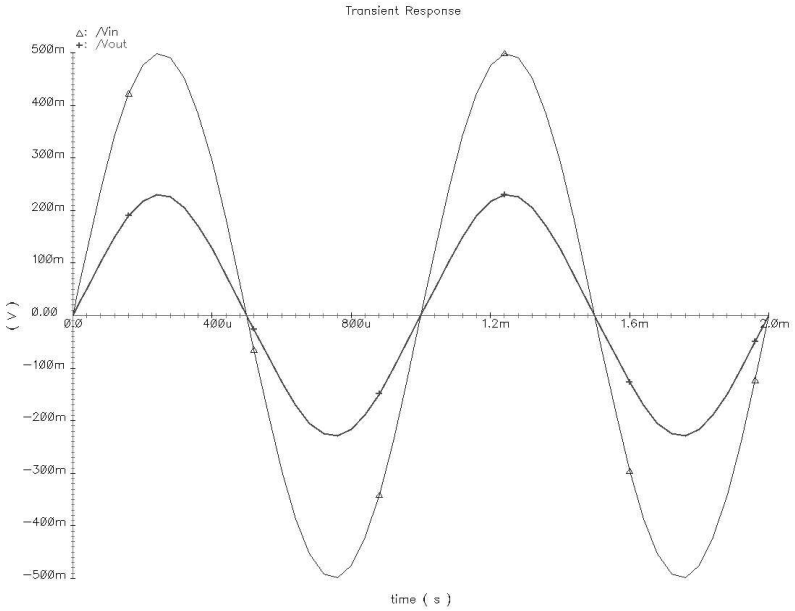

Figure 4.10. Design 2: Transient response.

4.3 Simulation Results for Third Design of Floating Resistor

The final module differs only slightly from the second module. A mismatch is introduced in the transistors that appear in the translinear loop and the non-linearity induced by this effect is studied. Figure 4.13 is the transconductance plot for this module. A clear observation of the distortion is made from its transient response shown in Figure 4.14.

The DFT analysis shown in Figure 4.15 and 4.16 shows an aparent 3rd harmonic distortion of -45.37 dB compared to the fundamental of -35.27 dB as expected. The crossover distortion is due to the bias current mismatch in the translinear loop due to the properties of the different devices used. This behavior is verified in Chapter 5, where measurement results are listed and the actual response is captured.

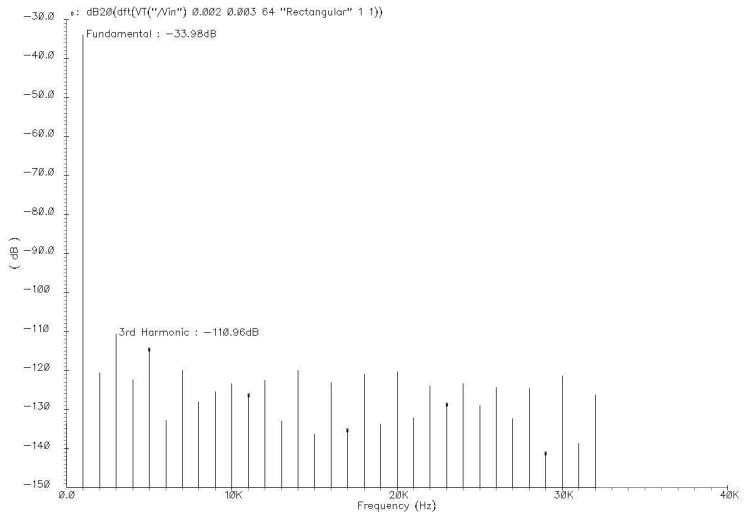

Figure 4.11. Design 2: DFT of input signal.

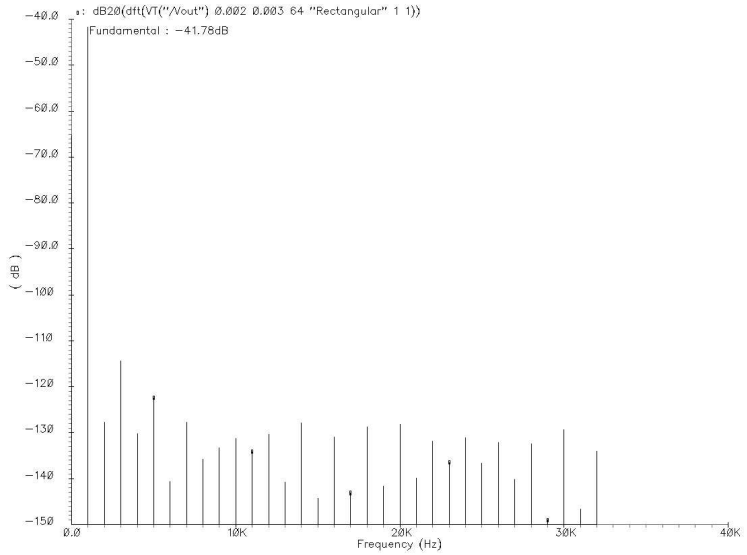

Figure 4.12. Design 2: DFT of output signal.

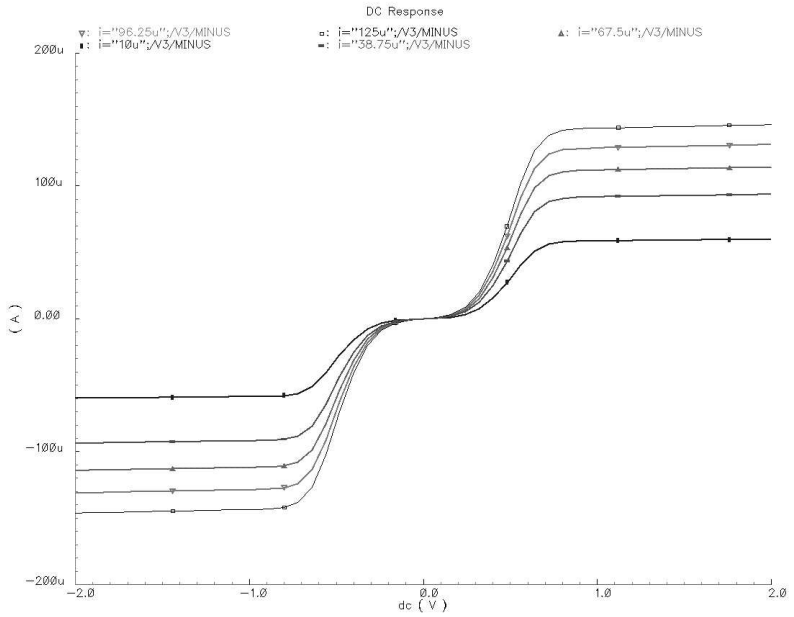

Figure 4.13. Design 2: Transconductance plot for varying $I_{ctrl}(i)$.

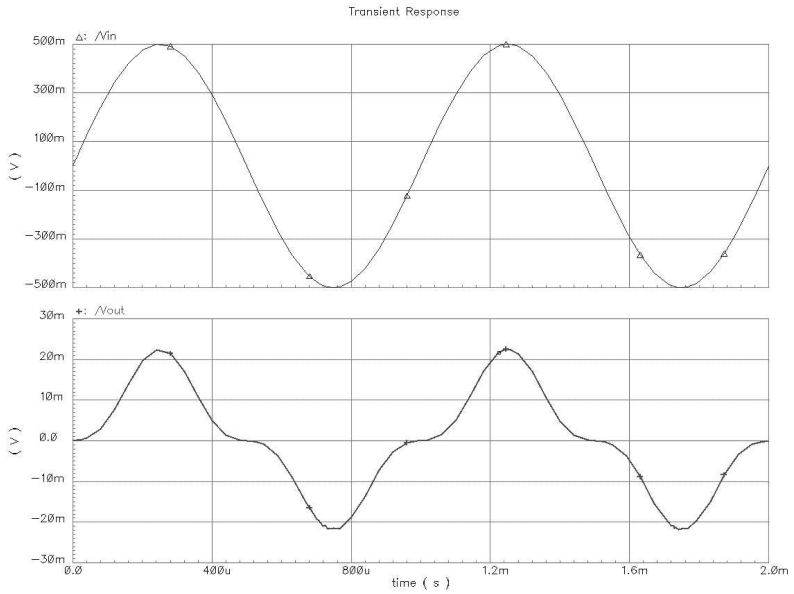

Figure 4.14. Design 3: Transient response showing crossover distortion.

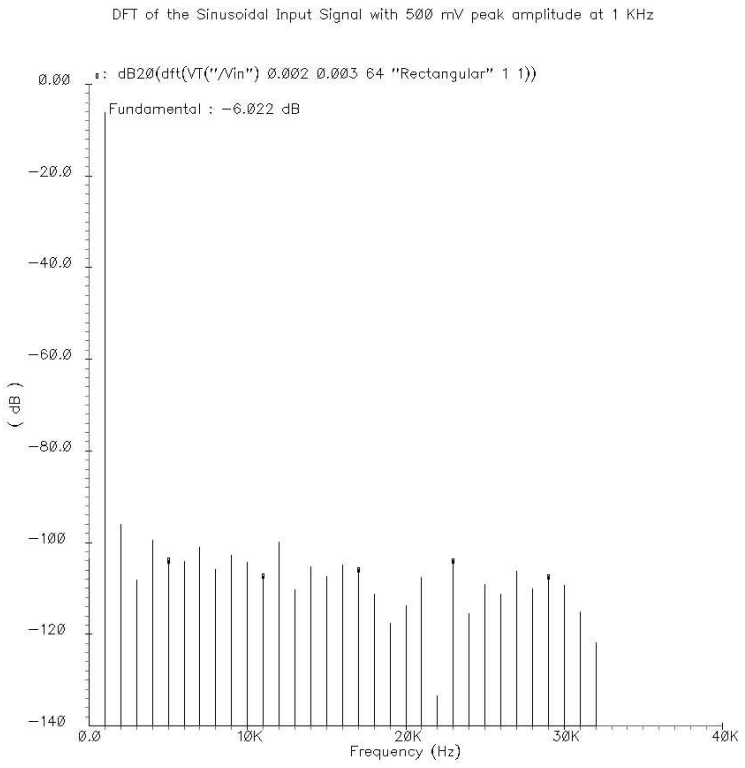

Figure 4.15. Design 3: DFT of input signal.

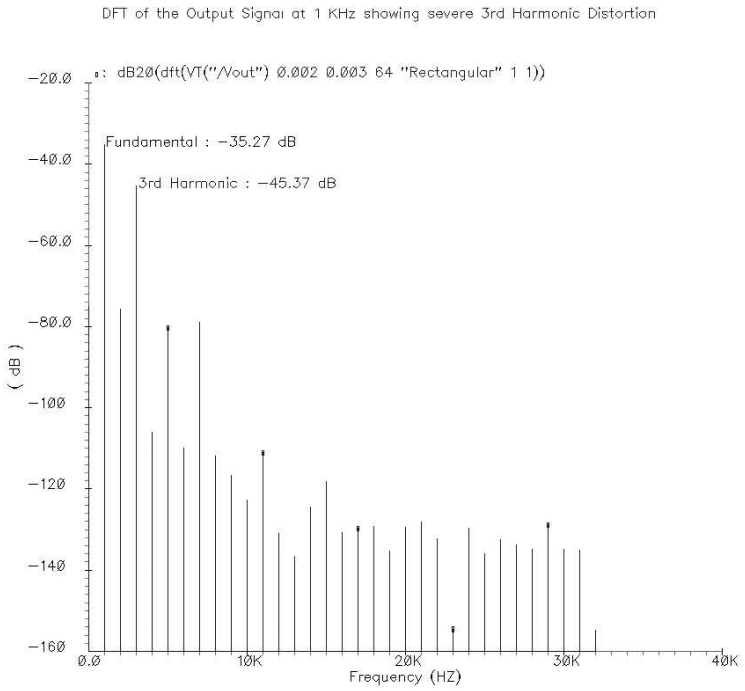

Figure 4.16. Design 3: DFT of output signal.

CHAPTER 5

TEST AND MEASUREMENT RESULTS

In this chapter, the conclusions derived in Chapter 4 are verified based on actual tests and measurements performed on the chips. The variation in the value of resistance due to the non-linearity exhibited by the designs in their schematic simulations are also evident while these are tested in the lab. The chips are plugged into the setup shown in Figure 4.4. The results are provided for all three modules for the floating resistor design. In addition, the results are alse provided for its application in a VGA configuration discussed in Section 2.4.

5.1 Testbench Analysis

A simple voltage divider configuration for is chosen the purpose of measurement. In this configuration, the floating resistor chip is connected with another passive resistor, R_{load}(330 Ω in this case). I_{ctrl} is provided by an external biasing mechanism. This involves the use of a passive resistor, R_{bias}, of appropriate value corresponding to the R_{float} value required. The calculated value of R_{float} is then verified against simulation results. R_{bias} is changed from 5 $M\Omega$ to 10.7 $K\Omega$ i.e., the bias current varies from 16.6 μA to 750 μA. As I_{ctrl} increases, it is noted that R_{float} decreases, as per simulated results. This behavior is well reflected in measurements. Due to the inherent non-linearity in the design of the floating resistor, the value of the resistance is expected to vary as the voltage across it varies beyond its linear range. Thus as the input voltage V_{in} in Figure 4.4 varies, the resistance is also found to vary slightly. The effective value of resistance will include the effect of internal emitter resistance of the transistors. The formulae used in

calculating the component values are derived from the bias circuit shown in Figure 5.1. These formulae are listed in Equations (5.1) through (5.3).

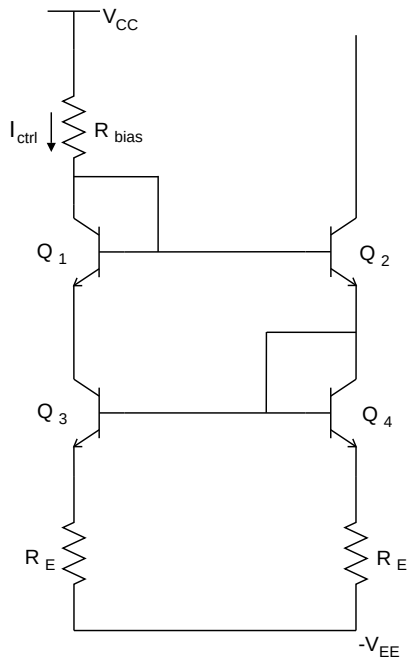

Figure 5.1. Bias Circuit.

$$R_{bias} = \frac{V_{CC} + V_{EE} - 2V_{BE}}{I_{ctrl}} - R_E \tag{5.1}$$

$$\text{when,} \quad R_E = 500\Omega, V_{CC} = |V_{EE}| = 5V, V_{BE} = 0.6V$$

$$R_{bias} = \frac{8.4}{I_{ctrl}} - 500 \tag{5.2}$$

$$R_{float} = \left(\frac{V_{in}}{V_{out}} - 1\right) R_{load} \tag{5.3}$$

5.2 Test Results

Using the testbench in Figure 4.4, the values of V_{out} for varying values of V_{in} are noted. These values are plugged in Equation (5.3) to calculateR_{float}. The results are

tabulated in Table 5.1. In this table the $\Delta V(=V_{in} - V_{out})$ values are calculated from the measured readings.

Table 5.1. Test results for floating resistor design 1

$I_{ctrl}(\mu$A(	$\Delta V_{min}(V)$	$\Delta V_{max}(V)$	$R_{float}(\Omega)(measured)$	$R_{float}(\Omega)(simulated)$
16.66	14m	111m	741.50	741.43
125	5.5m	100m	117.35	116.46
750	2m	40m	36.81	32.47

The data values shown in Table 5.1 represent the actual measurement readings for each case and are compared to the simulated R_{float} values. In most cases, the behavior of the data points is in compliance with the simulation results.

In Figure 5.2, the deviation of simulated and measured results for $R_{float}$from the theoretical approximation(Equation (2.22)) is due to a slightly greater change in V_{BE} of the transistors that leads to an excess change in the overall voltage across the floating resistor. This is also partially due to the internal emitter resistance, r_e, of the transistors in the design.

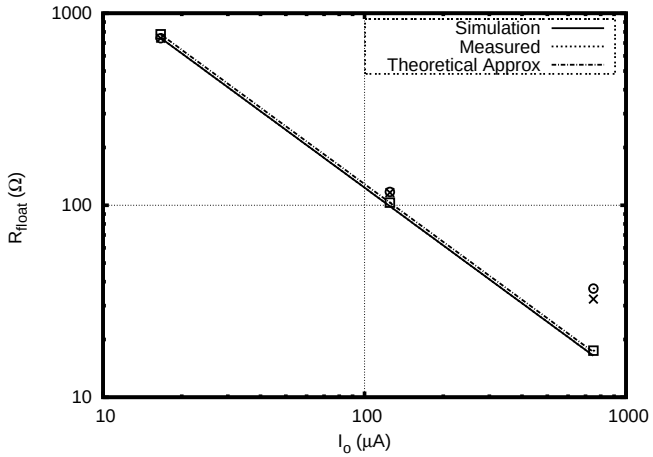

Figure 5.2. Design 1: R_{float} vs. I_o on logscale.

The first design of the floating is applied to the VGA configuration discussed in Chapter 2.4. The results are tabulated in Table 5.2. The variation of gain as R_{float} varies is shown in Figure 5.3.

Table 5.2. Variable gain amplification

V_{in}(V)	V_{out}(V)	$R_{float}(\Omega)$	Gain
0.353	0.619	500	1.75
0.353	0.657	400	1.86
0.335	1.14	220	3.4
0.338	1.14	180	3.37

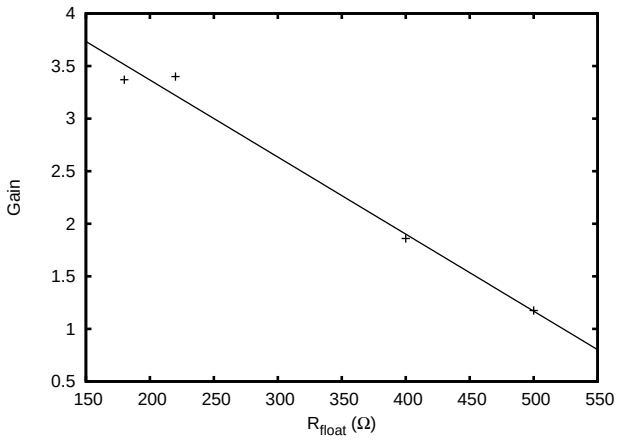

Figure 5.3. R_{float} vs Gain.

The test is repeated using the testbench shown in Figure 4.4 for the second module. The average of 10 sets of readings is calculated and tabulated in Tables 5.3. Analysis of the measured and simulated data with that of the theoretical linear approximation results are presented in Figure 5.4.

Table 5.3. Test results for floating resistor design 2

$I_{ctrl}\mu$A	$\Delta V_{min}(V)$	$\Delta V_{max}(V)$	$R_{float}(\Omega)(measured)$	$R_{float}(\Omega)(simulated)$
1125	12m	230m	493.23	480.76
148.67	11.4m	220m	413.60	416.08
750	6m	120m	137.31	133.72

As seen from this figure, the measured and the simulated results match each other closely. A 15% deviation of these results from the theoretical linear approximation is again due to variation in V_{BE} of the internal transistors in the design.

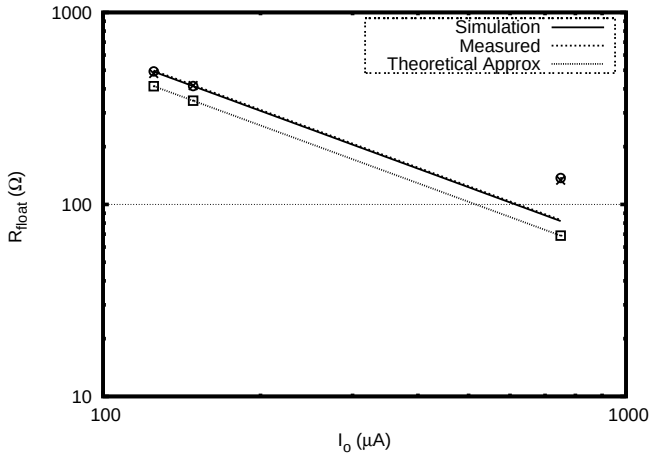

Figure 5.4. Design 2: R_{float} vs. I_o on logscale.

Figure 5.5 illustrates the behavior of the circuit for a sinusoidal input signal of 500 mV at 1 kHz. The third design consists of a deliberate mismatch in the transistors in the translinear loop. This exhibits itself as a crossover distortion in the transient response captured in Figure 5.6.

The distortion seen in Figure 5.6 is clearly due to the mismatch in the bias currents introduced by different types of transistors in the loop.

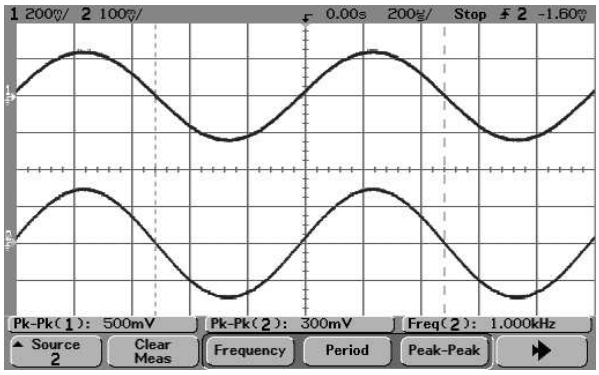

Figure 5.5. Oscilloscope output for testbench.

Thus it is seen that the first and second designs are well suited for applications involving at least 60 mV of dynamic range.

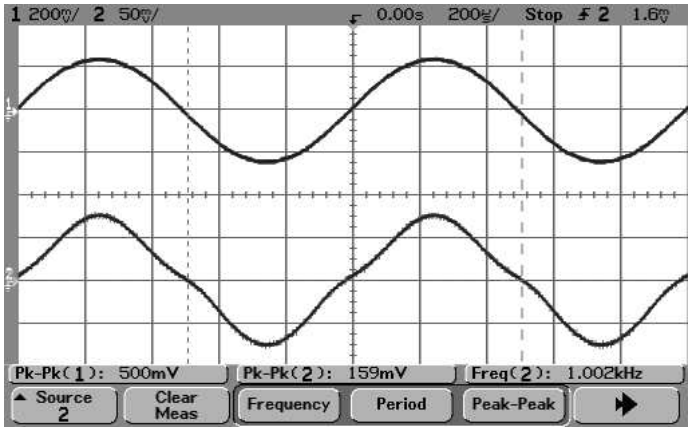

Figure 5.6. Illustration of crossover distortion for design 3.

CHAPTER 6

CONCLUSION AND FUTURE WORK

Two different realizations of floating resistor using National's VIP10 process is presented in this thesis. It is combined with a CFOA to make a VGA. This thesis achieves the goal of extension of linearity and dynamic range of floating resistors effectively. Enhancements to the original design in terms of the biasing circuit are made. The VGA system is based on the difference amplifier configuration. The improvement in the VGA design results from use of the floating resistor to vary the gain. Only this resistor needs to be changed to get a change in gain, which does not affect the other parameters. When the gain of the VGA is high, less voltage difference across the floating resistor is required and hence less distortion. The resistor is linear when the voltage difference across it is small. On the other hand for lower gains, the swing across this resistor becomes large and this leads to excess distortion. Thus the extension of linearity and dynamic range achieved proves beneficial. Another design of floating resistor having mismatches is studied and the distortion effects analyzed. Each of the architecture was carefully taken through the whole design cycle. Analysis and measurement results are in good compliance with each other.

Further research involves the study of noise gain of the circuit. The VGA is developed with a CFOA core that is prone to larger noise gain than a VFA. Voltage Offset problems can also be addressed and covered as a part of further course of action.

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BIOGRAPHICAL STATEMENT

Nithya Jagannathan was born in Trichy, India, in 1982. She received her B.E.(Hons) degree in Electronics and Instrumentation from Birla Institute of Technology and Science, India, in 2004 , and her M.S. in Electrical Engineering from The University of Texas at Arlington in 2006. In 2003, she was with in STMicroelectronics, India as a research intern and worked on the design of analog subsystems using Cadence. Her current research interest includes design of analog and mixed signal circuits.