1/f NOISE IN HAFNIUM BASED HIGH-k GATE DIELECTRIC MOSFETS AND A REVIEW OF MODELING

by

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ABSTRACT

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For next generation MOSFETs, the constant field scaling rule dictates a reduction in the gate oxide thickness among other parameters. Consequently, gate leakage current becomes a serious issue with very thin SiO_2 that is conventionally used as gate dielectric since it is the native oxide for Si substrate. This has driven an industry wide search for suitable alternate 'high-k' gate dielectric that has a high value of relative permittivity compared to SiO_2 thereby presenting a physically thicker barrier for tunneling carriers while providing a high gate capacitance. Consequently, it is essential to study the properties of these novel materials and the interfaces that they form with the substrate, gate or other dielectrics in a multi-level stack.

The main focus of this work is the 1/f noise that is specifically used as a characterization tool to evaluate the performance of high-k MOSFETs. Nevertheless, DC and split C-V characterization are done as well to obtain device performance parameters that are used in the noise analysis.

At first, the room temperature 1/f noise characteristics are presented for n- and p-channel poly-Si gated MOSFETs with three different gate dielectrics- HfO_2, Al_2O_3 (top layer)/HfO_2 (bottom layer), $HfAlO_x$. The devices had either 1 nm or 4 nm SiO_2 interfacial layer, thus presenting an opportunity to understand the effects of interfacial layer thickness on noise and carrier mobility. In the initial study, the analysis of noise is done based on the Unified Flicker Noise Model. Next, a comparative study of 1/f noise behavior is presented for TaSiN (NMOS) and TiN (PMOS) gated MOSFETs with HfO_2 gate dielectric and their poly-Si gated counterparts. Additionally, in TaSiN MOSFETs, the effect of the different deposition methods employed for interfacial layer formation on the overall device performance is studied.

Finally, the 'Multi-Stack Unified Noise' model (MSUN) is proposed to better model/characterize the 1/f noise in multi-layered high-k MOSFETs. This model takes the non-uniform trap density profile and other physical properties of the constituent gate dielectrics into account. The MSUN model is shown to be in excellent agreement with the experimental data obtained on TaSiN/HfO_2/SiO_2 MOSFETs in the 78-350 K range. Additionally, the MSUN model is expressed in terms of surface potential based parameters for inclusion in to the circuit simulators.

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C_B	Si bulk capacitance at maximum depletion (Fcm^{-2})
C_{CET}	capacitance equivalent oxide capacitance of MOSFET (Fcm^{-2})
C_D	depletion capacitance (Fcm^{-2})
C_{EOT}	equivalent oxide capacitance of MOSFET (Fcm^{-2})
C_g	total gate capacitance of MOSFET (Fcm^{-2})
C_{gb}	gate to bulk capacitance of MOSFET (Fcm^{-2})
C_{gc}	gate to channel capacitance of MOSFET (Fcm^{-2})
C_{it}	interface trap charge (Fcm^{-2})
C_{ox}	gate oxide capacitance of MOSFET (Fcm^{-2})
$C_{overlap}$	overlap capacitance (Fcm^{-2})
D_{it}	interface trap density from sub-threshold measurements ($eV^{-1}cm^{-2}$)
E	energy level (eV)
EOT	equivalent oxide thickness (nm)
E_c	conduction band edge (eV)
E_{fn}	quasi Fermi level (eV)
E_g	energy Gap (eV)
E_i	intrinsic Fermi level (eV)

E_v	valence band edge (eV)
E_x	field along the channel (Vcm^{-1})
f	frequency (Hz)
f_t	trap occupancy function
g_d	Conductance ($A\ V^{-1}$)
g_m	transconductance ($A\ V^{-1}$)
h	Planck's constant (eV-s)
I_d	drain current (A)
k	dielectric constant
k	Boltzmann's constant ($eV\ K^{-1}$)
L	MOSFET channel length (μm)
ΔL	length of pinch-off/velocity saturation region (μm)
m^*	electron effective mass (kg)
m_{HK}^*	carrier effective mass in the high-k dielectric (kg)
m_{IL}^*	carrier effective mass in the interfacial layer (kg)
N	inversion layer charge density (cm^{-2})
N_0	source end charge density (cm^{-2})
N_f	fixed charge density (cm^{-2})

N_I	substrate doping concentration (cm^{-3})
N_L	drain end charge density (cm^{-2})
N_m	charge density corresponding to surface potential mid-point (cm^{-2})
$N(x)$	inversion layer charge density at distance x from the source (cm^{-2})
N_t	oxide trap density (cm^{-3} eV^{-1})
N_{ot}	occupied traps per unit area (cm^{-2})
N_{tHK0}	trap density at the intrinsic Fermi level, at the high-k dielectric - interfacial layer interface (cm^{-3} eV^{-1})
$N_{tHK}(E, x, y, z)$	trap density distribution over space and energy in the high-k layer (cm^{-3} eV^{-1})
$N_{tHK}(E_{fn}, z)$	trap density distribution in the high-k layer at the quasi Fermi level (cm^{-3} eV^{-1})
N_{tIL0}	trap density at the intrinsic Fermi level and at the interfacial layer – Si interface (cm^{-3} eV^{-1})
$N_{tIL}(E, x, y, z)$	trap density distribution over space and energy in the interfacial layer (cm^{-3} eV^{-1})
$N_{tIL}(E_{fn}, z)$	trap density distribution in the interfacial layer at the quasi Fermi level (cm^{-3} eV^{-1})
ΔN	inversion charge in the $W\Delta x$ area
ΔN_{ot}	number of occupied traps in the gate oxide ($W\Delta x$ area)

q	electronic charge (C)
Q_{bulk}	bulk charge (Ccm^{-2})
Q_D	depletion charge (Ccm^{-2})
Q_G	gate charge (Ccm^{-2})
Q_{inv}	inversion layer charge (Ccm^{-2})
Q_{it}	interface trap charge (Ccm^{-2})
Q_{sc}	semiconductor charge (Ccm^{-2})
Q_t	oxide trap charge (Ccm^{-2})
R	coupling coefficient between fluctuations in the channel charge and in the gate oxide trapped charge
S	subthreshold slope (V^{-1})
$S_{Id}(f)$	total drain current noise power spectral density ($A^2\ Hz^{-1}$)
$S_{\Delta Id}(x,f)$	power spectral density of the local current fluctuations ($A^2\ Hz^{-1}$)
$S_{\Delta Nt}(x, f)$	power spectral density of the mean square fluctuations in the trapped charge carriers over the area $W\Delta x$ (Hz^{-1})
S_{V_d}	voltage noise power spectral density ($V^2\ Hz^{-1}$)
S_{Vfb}	flat band voltage noise power spectral density ($V^2\ Hz^{-1}$)
S_{V_g}	input referred noise ($V^2\ Hz^{-1}$)
T	temperature (K)

t_{CET}	capacitance equivalent thickness (nm)
T_{EOT}	equivalent oxide thickness (cm)
T_{HK}	high-*k* dielectric thickness (cm)
T_{IL}	thickness of interfacial layer (cm)
T_{ox}	thickness of gate oxide (cm)
T_{SiO_2}	thickness of SiO_2 (cm)
V	channel quasi-Fermi potential (V)
V_d	drain to source voltage (V)
V_{dsat}	drain to source voltage at pinch-off/velocity saturation point (V)
V_{FB}^{0}	gate-substrate work function difference (V)
V_g	gate to source voltage (V)
V_{gHK}	band bending in the high-k layer (V)
V_{gIL}	band bending in the interfacial layer (V)
V_{ox}	potential across gate oxide (V)
V_t	threshold voltage (V)
$V(x)$	horizontal channel potential in the channel at a distance x from the source (V)
W	MOSFET channel width of (μm)
x	distance in the channel from source towards drain(cm)

y	distance in the width dimension (cm)
z	distance into the gate dielectric stack (cm)
Δx	infinitesimal length in the gate dielectric (cm)
Δy	infinitesimal width in the gate dielectric (cm)
Δz	infinitesimal thickness in the gate dielectric (cm)
α	surface potential based screened coulomb scattering coefficient (V s)
α_H	Hooge's Coefficient
α_{sc}	screened coulomb scattering coefficient (V s)
γ	carrier tunneling coefficient in the gate dielectric (cm^{-1})
γ_{HK}	carrier tunneling coefficient in the high-k gate dielectric (cm^{-1})
γ_{IL}	carrier tunneling coefficient in the interfacial layer (cm^{-1})
ε_0	permittivity of free space (Fcm^{-1})
ε_{HK}	dielectric constant of high-k material (Fcm^{-1})
ε_{IL}	dielectric constant of interfacial layer (Fcm^{-1})
ε_{Si}	permittivity of silicon (Fcm^{-1})
ε_{SiO_2}	permittivity of silicon oxide (Fcm^{-1})

η_{HK}	fitting parameter that determines the high-k dielectric trap density distribution as a function of z (cm^{-1})
η_{IL}	fitting parameter that determines the interfacial layer trap density distribution as a function of z (cm^{-1})
λ_{HK}	fitting parameter that defines the effect of dielectric band-bending on the trap density that the tunneling electron encounters in the high-k dielectric layer (eV^{-1})
λ_{IL}	fitting parameter that defines the effect of dielectric band-bending on the trap density that the tunneling electron encounters in the interfacial layer (eV^{-1})
μ	surface potential based effective carrier mobility (cm^2/Vs)
μ_{c0}	mobility fitting parameter (cm/Vs)
μ_{eff}	effective carrier mobility (cm^2/Vs)
μ_{imp}	mobility due to impurity scattering ($cm^2V^{-1}s^{-1}$)
μ_{latt}	mobility due to lattice scattering ($cm^2V^{-1}s^{-1}$)
μ_{others}	mobility due to other scattering phenomena (cm^2/Vs)
μ_{ox}	mobility due to oxide charge scattering (cm^2/Vs)
ξ_{HK}	fitting parameter for energy dependence of high-k traps (eV^{-1})
ξ_{IL}	fitting parameter for energy dependence of interfacial layer traps (eV^{-1})

$\tau(E, x, y, z)$	trapping time constant in the gate dielectric (s)
τ	trapping time constant (s)
τ_0	trapping time constant at the Si/SiO_2 interface (s)
Φ	barrier height (eV)
ϕ_F	bulk potential (V)
Φ_{HK}	high-k barrier height for tunneling carriers (eV)
Φ_{IL}	interfacial layer barrier height for tunneling carriers (eV)
σ	frequency exponent as in $1/f^{\sigma}$
ω	angular frequency (radians/s)
ψ_m	surface potential mid-point (V)
ψ_s	surface potential (V)
ψ_{sat}	surface potential at pinch-off/velocity saturation point (V)
ψ_{ss}	source side surface potential (V)
ψ_{sd}	drain side surface potential (V)

CHAPTER 1

INTRODUCTION

1.1 High Dielectric Constant Materials as Gate Dielectrics

The current scaling trend in CMOS devices is the motivation for research in high dielectric constant films. Applications demanding low power consumption, low off-state leakage, and faster response require the devices to shrink. As the device dimensions scale down, the conventional SiO_2 gate dielectric is no longer viable below the 1.5 nm thickness due to prohibitively high gate leakage currents (>1 A/cm^2) caused by quantum mechanical tunneling of electrons/holes [1,2,3]. This results in the loss of inversion layer charge and an increase in standby power consumption. In theory, high dielectric constant or high-k materials offer an attractive solution in that they provide low leakage currents owing to a thicker physical layer for the same electrical thickness as their SiO_2 counterparts. For example, the MOSFETs in Figure 1.1 provide the same gate capacitance ($\varepsilon_0 k/T_{ox}$) of ~2.3 μFcm^{-2} so that their electrical thicknesses are equal. However, the device with 7 nm HfO_2 results in much lower gate leakage currents due to its larger physical thickness compared to 1.5 nm SiO_2. Thus, high-k materials are advantageous in this context as they can be much thicker physically to block the tunneling current and yet have a thinner electrical thickness. While this seems to solve the quantum-tunneling problem, primary issues regarding the properties of high-k

materials and incorporation of these novel dielectrics into the standard CMOS process flow need to be dealt with.

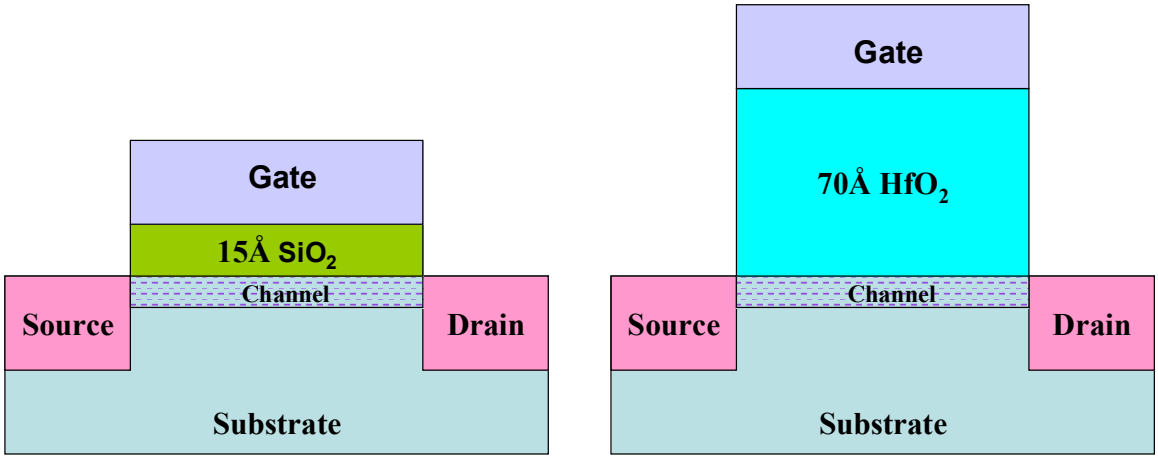

Figure 1.1 MOSFET gate stacks with 7 nm HfO_2 (k~18) and 1.5 nm SiO_2 (k~3.9) yield the same gate capacitance. However, device with HfO_2 exhibits lower gate leakage currents.

There are several materials that can be used as high-k dielectrics as shown in Table 1.1, which can be can be broadly classified as-

- Metal oxides
- Silicates (metal oxides doped with silicon)
- Aluminates (metal oxides doped with aluminum)

In the following, the fundamental issues with high-k materials and the various factors affecting the choice of these dielectrics for incorporation in to the standard CMOS processes are briefly discussed.

Table 1.1 A few potential high-k dielectrics for CMOS applications with approximate dielectric constant and band gap values [4].

Material	Dielectric constant, k	Band gap, E_g (eV)
HfO_2	19	5.8
ZrO_2	25	7.8
Al_2O_3	9	8.7
Si_3N_4	7	5.1
TiO_2	80	3.5
Ta_2O_5	26	4.5
La_2O_3	30	4.3
Y_2O_3	15	5.6
HfSiON	8	-
$HfAlO_x$	-	6.5

Formation of Interfacial Layer:

The most fundamental advantage of SiO_2 is the quality of its interface with Si bulk. Most of the high-k materials considered so far have unstable interfaces with Si and an unintentional interfacial layer is formed at the Si surface due to oxygen diffusion through high-k or reactions at the Si/high-k interface. Although it is possible to control the interfacial formation by means of careful interface engineering, the presence of this interfacial layer limits the maximum achievable gate capacitance. This can be explained

by considering the resulting structure with the interfacial layer as shown in Figure 1.2. From MOSFET theory, the total applied gate voltage is distributed across the gate

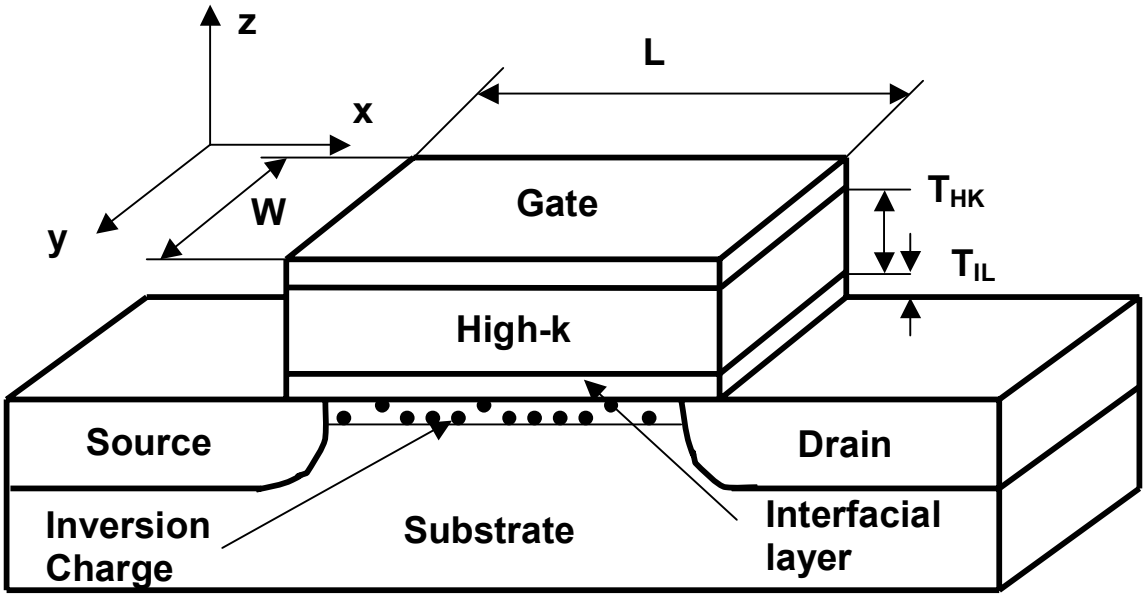

Figure 1.2 Cross section of MOSFET with high-k and interfacial layers.

dielectric and the substrate. If the gate dielectric has multiple layers, they form a series combination so that the total voltage across the stack is divided among the layers. Hence, the overall gate dielectric capacitance is given by

$$1/C_{eq} = 1/C_{HK} + 1/C_{IL}$$

Clearly, the interfacial layer with a lower capacitance dominates the overall capacitance thereby compromising the maximum capacitance that can be obtained with the high-k alone. To understand how this reduction in capacitance limits the overall equivalent oxide thickness, consider the equivalent oxide thickness of high-k dielectric without any interfacial layer, which is given by-

$$T_{EOT} = 3.9 \times \left(\frac{T_{HK}}{\varepsilon_{HK}} \right)$$

Here, T_{EOT} represents the equivalent physical thickness of SiO_2 that would provide the same gate capacitance as the dielectric under consideration and without any regards to leakage or reliability issues. Assuming SiO_2 interfacial layer for simplicity, the equivalent oxide thickness of the resulting stack is given as

$$T_{EOT} = T_{SiO_2} + 3.9 \times \left(\frac{T_{HK}}{\varepsilon_{HK}} \right)$$

Therefore, the thickness of the interfacial layer sets the lower limit to the gate dielectric scaling.

It should be noted that conventional SiO_2 gate dielectrics had an interface state density of about 1×10^{10} cm^{-2}. High-k materials investigated by charge pumping measurements showed higher interface trap density values [5,6]. Consequently, there is degradation in mobility in addition to substantial fixed charges and flatband/ threshold voltage shifts [7,8,9,10,11,12,13]. It has been shown in this work that the overall electrical behavior and reliability of high-k dielectric MOSFETs would strongly depend on the material properties of the interfacial layer that exists between the high-k and the substrate.

*Trade-off between permittivity (*k*) and band gap (E_g)*:

High permittivity dielectrics can provide high gate capacitance for good channel control in conjunction with larger physical thickness, thereby avoiding the unintentional conduction paths from the channel to the gate. However, the band gap of the dielectric

plays an equally important role in warding off the leakage currents. The band gap of SiO_2 is ~9 eV with 3.5 eV and 4.4 eV as conduction and valence band offsets with Si. This means that the electrons in the NMOS inversion layer have to cross a barrier of 3.5 eV to tunnel through the oxide. Similarly, the holes need to overcome a barrier of 4.4 eV to contribute to the gate tunneling currents. In both Fowler-Nordheim and direct tunneling mechanisms, tunneling current density has an exponential dependence on the barrier height [14,15]. Thus, the potential high-k dielectric is required to present an appropriate barrier height to the channel carriers to prevent carrier tunneling and in turn check the gate leakage. Among the several high-k materials investigated for gate dielectric application, the dielectric constant generally exhibited an inverse relationship to the band gap [4]. Therefore, a compromise has to be made between the permittivity and band gap values so that a high enough k value can be chosen to obtain the desired performance while having a large tunneling barrier. Figure 1.3 gives a plot of dielectric constant vs. band gap for a few potential high-k dielectric materials [16].

It can be noted that HfO_2 and ZrO_2 have reasonably high values for both k and E_g. Al_2O_3 has a low value of k but a higher band gap ensuring low leakage currents. Other materials with high values of k have low barrier heights making them unsuitable for low power applications. Additionally, fringing or field induced barrier lowering (FIBL) is seen as an anomalous degradation in turn-on/off characteristics in sub-micron devices, especially involving dielectrics with very high permittivity values. FIBL shows similar effects as the drain induced barrier lowering (DIBL) but has a slightly different mechanism. While in DIBL, the electric fields from the drain junction terminate directly

on the channel and/or source regions causing a reduction in the drain/source barrier. For FIBL, the drain is coupled to the channel via through the gate dielectric in turn causing lowered threshold voltage, increased off-state leakage and a deteriorated sub-threshold

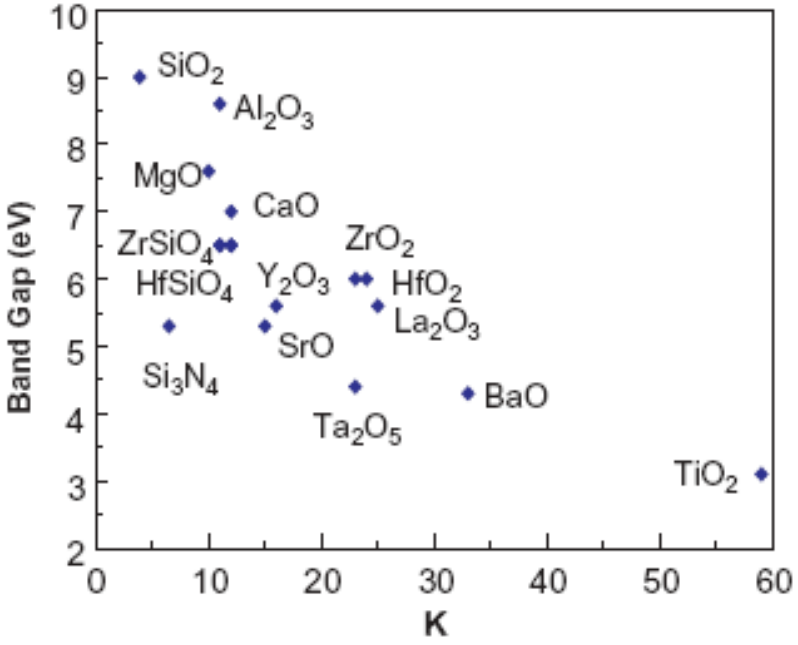

Figure 1.3 Plot of dielectric constant vs. band gap for few potential high-k dielectric materials. Reprinted from [16] with permission from Elsevier.

swing. FIBL effect is not as conspicuous in SiO_2 MOSFETs as in high-k devices owing to the physical thickness and permittivity values. FIBL is gate length and permittivity dependent worsening for short channel devices and higher permittivity dielectrics. The choice of dielectrics with low dielectric constant values compared to Al_2O_3 is limited due to other factors like stable interfaces, ability to withstand high CMOS process temperatures etc.

Crystallization temperature/Film microstructure:

In the past, amorphous SiO_2 films were preferred over single crystal or polycrystalline films. The grain boundaries in polycrystalline films are dominant in causing high leakage currents besides yielding non-uniformities in the permittivity values owing to the localized variations in grain size and orientation. Oxygen and dopant atoms diffuse much faster in polycrystalline structures and triple points generate defects or voids. Amorphous films on the other hand, exhibit better insulation properties, less severe oxygen and dopant diffusion resulting in lower defect density. Hence, the high-k films need to have high crystallization temperatures to endure the high temperature processing steps involved. Al_2O_3 fares well compared to other high-k materials in this regard [4].

Compatibility with the gate electrode:

Gate compatibility is another integration issue for high-k dielectric materials. In the past, poly-silicon gates were the preferred choice, as their integration schemes were well established and they offered precise control of threshold voltages for both n-MOS and p-MOS structures by simply varying the doping concentrations of the poly-Si. However, it has been shown recently, that Fermi level pinning occurs at HfO_2/poly-Si gate interface due to the interface states originating from the reactions between HfO_2 and poly-Si [17,18]. This sets a lower limit on the threshold voltage and necessitates the use of alternative gates. Besides, additional problems posed by poly-Si gate such as depletion effects in strong inversion, large sheet resistance and high activation temperatures can be avoided using metal gates [19,20,21,22], which might otherwise

result in dopant penetration into the high-k causing significant fixed charges, traps, flatband and threshold voltage shifts. Table 1.2 lists a few potential metal gates that can be used in CMOS processes. Some of the main criteria concerning the metal gate selection are -

- Single mid-gap metal gate or dual metal gates
- Thermal, chemical and mechanical stability with gate dielectric/surrounding materials
- Low sheet resistance
- Compatibility with process integration

Table1.2 A few CMOS metal gates with approximate work functions [23,24,25,26,27].

Gate Material	Work Function (eV)
Ti	4.0
TiN	4.8-5.3
Ru	5.1
Ta	4.2
$TaSi_2$	4.7- 4.8
TaSiN	4.4
Mo	5.0
RuO_2	5.1

Metal work function is an important parameter in selecting the gate material because of the fact that threshold voltage of MOS device depends on it. If a single metal gate is

needed for both PMOS and NMOS, a midgap metal with its Fermi level at the mid gap of the silicon substrate can be used. Although this simplifies the processing steps, the major disadvantage with this approach is that the threshold voltages for both NMOS and PMOS would be the range of 0.5 V, which is high for next generation devices. Alternatively, the dual metal gate approach can be made where in two different metals with work functions near the conduction and valence band of Si could be chosen as electrodes for n and p type MOSFETs. The integration process is complicated as extra masking and depositions steps would be necessary. Recently, stable alloys with varying compositions of Ru and Ta have been indicated to provide a range of work functions to be used as dual CMOS gates [28]. In this work, the evaluation of low frequency noise and mobility are presented for MOSFETs with TiN (pMOS) and TaSiN (nMOS) as metal gates.

Deposition Techniques:

The choice of deposition technique is yet another key factor in determining the properties and final quality of the dielectric film. A few deposition techniques that could be employed for high-k dielectrics are listed below-

- Physical Vapor deposition (PVD)
- Metal Organic Chemical Vapor Deposition (MOCVD)
- Molecular Beam Epitaxy (MBE)
- Atomic Layer Deposition (ALD)
- Jet Vapor Deposition (JVD)

MOSFETs with HfO_2 gate dielectric made by MOCVD and ALD techniques have been evaluated for device performance parameters in this work.

Recent studies addressing the various integration issues and band gap considerations put HfO_2 at the forefront, followed by Hf-based dielectrics [9,29,30,31,32]. However, problems persist concerning the interfaces formed by these novel gate dielectrics with the substrate and the gate, mobility degradation, fixed charges, threshold shifts etc. Although, metal gates like TiN, TaN, TaSiN, Mo, Ru are suggested replacements for poly-Si gate towards a better high-k/gate interface, mobility degradation exists due to the traps in the high-k and the interface it forms with the substrate. In any case, an in-depth characterization study of charge trapping in these alternative gate dielectric materials and the interface they form with the substrate or interfacial layer is a subject of interest. Few widely used characterization tools are-

1. Quasi-static C-V technique
2. Conductance technique
3. Charge pumping measurements
4. Charge injection scheme
5. Low frequency noise method (1/f noise)

Quasi-static C-V measurements are routinely performed to obtain plethora of information regarding the MOS device parameters. Although it is easy to employ this method for interface trap characterization, it presents a limitation concerning the area of devices as it is difficult to obtain reliable/usable data in sub-micron MOSFETs due to parasitic capacitances. While charge pumping and charge injection techniques are used

for short channel devices, the analysis is limited to mid-gap range and the methods are destructive. Flicker or 1/f noise, is the predominant source of noise in the low frequency region, typically 1-100 kHz for a MOSFET. Low frequency noise (1/f noise) method can offer dielectric trap characteristics over a wide range of energies around the band edges for MOSFETs with dimensions in the sub-micron range, and is non-destructive in nature [33]. Further, the study of 1/f noise is significant for several reasons. It is an important design constraint for RF/microwave and analog applications, as it can get up-converted to phase noise thus causing a degradation in circuit/system performance [34,35,36,37]. In this work, the 1/f noise characterization is done to evaluate the performance of novel high-k materials as MOSFET gate dielectrics.

The next section gives a general categorization of different types of noise in MOSFETs to help identify 1/f noise that is the subject of interest, along with the underlying physical mechanisms that cause this particular noise.

1.2 Noise Classification in MOSFETs

Noise intrinsic to a device or circuit is a consequence of minute current or voltage fluctuations that are fundamentally associated with the discrete nature of electron charge transfer or motion of the charge carriers. Several mechanisms exist that generate noise in semiconductors leading to a unique spectral power distribution in the frequency domain. This section gives a brief overview of the types of noise encountered in MOSFETs.

Thermal Noise:

This type of noise is intrinsic to all resistors and is found in MOSFETs due to the resistive nature of the channel. It is also known as Johnson-Nyquist or thermal agitation noise and is caused by the random thermal motion of charge carriers. Its magnitude depends on the temperature but is independent of frequency or the current through the resistor as long as the thermal equilibrium is maintained. In general, the power spectral density of such a noise is given based on Nyquist theorem as [38]:

$$S_V(f) = 4kTR \tag{1.1}$$

where, k is the Boltzman constant, T is the equilibrium temperature, and R represents the linear resistor.

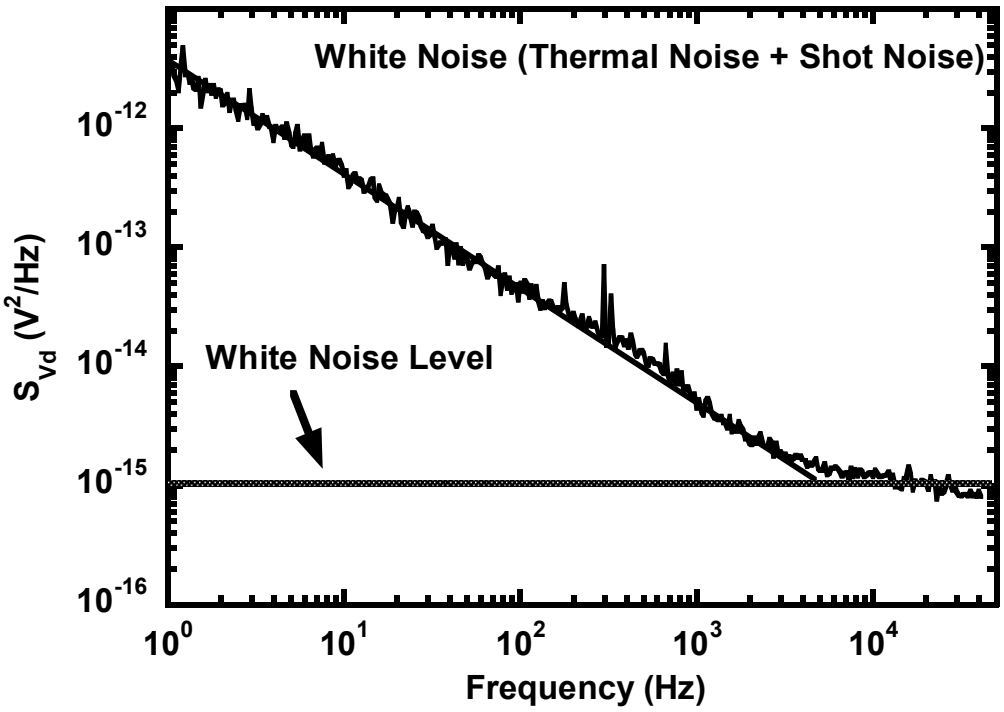

Figure 1.4 Typical MOSFET white noise at high frequencies. The device here is a $TaSiN/HfO_2/SiO_2$ MOSFET biased at V_g = 1.13 V and V_d = 0.05 V and at T = 100 K.

In case of a MOSFET, the resistance of the channel is not a constant and depends on the operating point i.e., gate and drain voltages.

In most circuit simulators the thermal noise model for a MOSFET in the saturation region is given as [39]

$$S_I(f) = 4kT(\frac{2}{3} g_m) \tag{1.2}$$

where, g_m is the device transconductance at a particular operating point. This noise is a major contributor to total noise at high frequencies in a MOSFET. Figure 1.4 depicts white noise in a MOSFET that constitutes thermal noise as well as shot noise that is described next.

Shot Noise:

In semiconductor devices, shot noise is a bias dependent component that is present whenever there is a DC flow due to random movement of charge carriers across a potential barrier. This is in view of the fact that the average current appearing as DC is actually a summation of discrete random independent pulses of electron charge flow. The time-domain mean squared deviation from the mean DC value is known as shot noise. The expression for shot noise power spectral density takes the following form [38,40]:

$$S_I(f) = 2qI \tag{1.3}$$

Due to the flat nature of its frequency spectrum, shot noise qualifies as another source of white noise and is indistinguishable from the thermal noise (Figure 1.4) as far as the spectral form is concerned. In a MOSFET, shot noise is generally associated with

substrate to channel leakage currents that cause drain current fluctuations. In addition, the high gate leakage currents in ultra-thin MOSFETs can be a source of shot noise [41,42,43].

Generation-Recombination Noise:

As the name suggests, this noise is associated with the fluctuations in the generation and recombination of carriers by localized centers that can be seen as fluctuations in the current passing through the semiconductor. In a MOSFET, the localized defect states may exist in the semiconductor bulk or the gate dielectric that cause trapping/detrapping of inversion layer carriers and exhibiting a predominant characteristic trapping time constant, τ. The general expression for G-R noise is given as [38],

$$S(f) = 4\overline{\Delta N^2}\,\frac{\tau}{1+(2\pi f\tau)^2} \tag{1.4}$$

where, $\overline{\Delta N^2}$ represents the variance of the charge carriers, f is the frequency and τ is the characteristic time constant of the defect band. The power spectral density plot of pure G-R noise is that of a Lorentzian spectrum, which is constant at low frequencies and drops down as f^{-2} above the corner frequency defined by the characteristic time constant as $f_c = 1/2\pi\tau$. Figure 1.5 depicts an example of G-R noise component in a MOSFET noise spectrum.

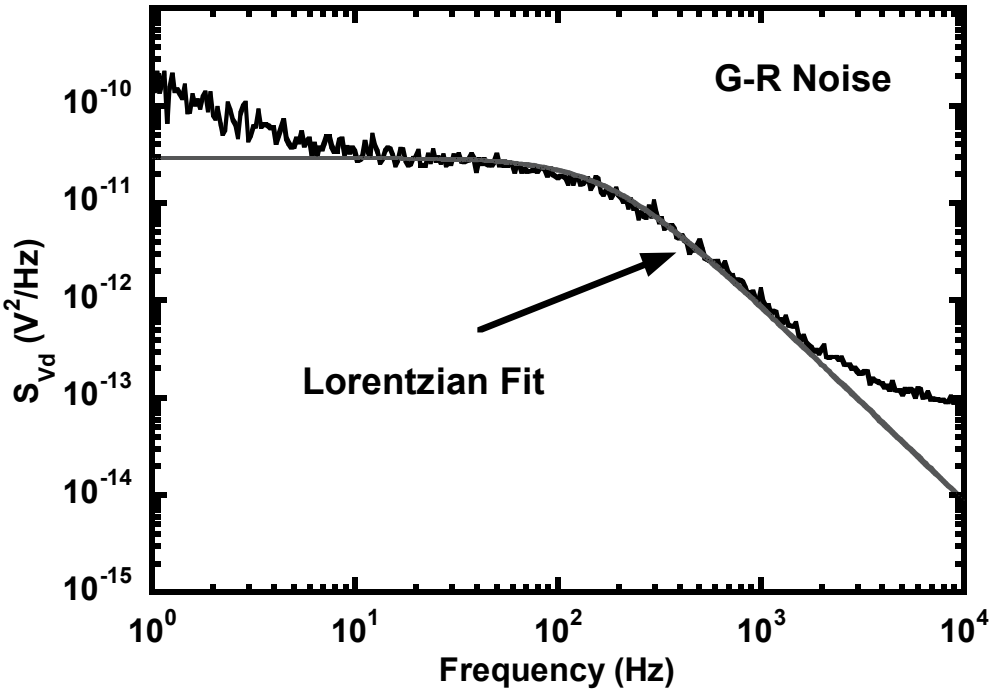

Figure 1.5 G-R noise in TaSiN/HfO_2/SiO_2 MOSFET biased at V_g = 0.5 V and V_d = 0.05 V and at T = 125 K. The Lorentzian approximation is provided for reference.

RTS Noise:

RTS stands for Random Telegraph Signal. This kind of noise is observed in small area devices appearing in time domain as discrete random voltage or current pulses. In frequency domain, RTS is characterized by a Lorentzian spectrum given by [44,45]:

$$S_{I_d}(f) = \frac{4(\Delta I_d)^2}{(\bar{\tau}_0 + \bar{\tau}_1)[(1/\bar{\tau}_0 + 1/\bar{\tau}_1)^2 + (2\pi f)^2]} \tag{1.5}$$

where, $\bar{\tau}_0$ and $\bar{\tau}_1$ have a Poisson distribution and they represent the mean capture and emission times. Alternatively, they can be considered as the average time durations in low and high states. However, unlike G-R noise, the amplitude spectrum of a well

defined RTS does not have a Gaussian distribution. In MOSFETs, RTS noise can be found in high quality small area SiO_2/Si systems where the oxide can have a single defect state causing trapping/de-trapping of a single channel carrier resulting in a Lorentzian spectrum as shown in Figure 1.6. When the number of traps is higher, the resulting Lorentzians can correspond to a unique or distributed time constants. Consequently, when summed up, the resulting spectrum can be one of G-R noise or can yield a 1/f like spectrum as discussed in the next section.

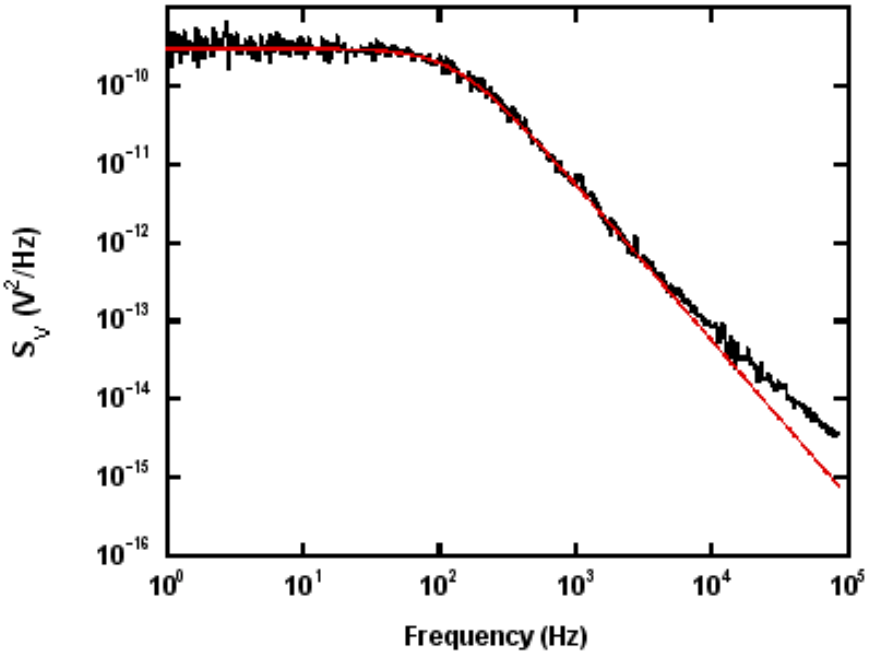

Figure 1.6 Voltage noise power spectrum of small area SiO_2 MOSFET biased at V_g = 1.3 V and V_d = 0.05 V along with a Lorentzian fitting [46].

Flicker Noise:

This is a major source of noise at low frequencies and is found in almost all electronic materials and semiconductor devices like metal films, Ionic Solutions, MOSFETs, BJTs, JFETs, MESFETs and junction diodes [38,47, 48,49, 50]. It is also known as 1/f noise since the noise power spectral density is inversely proportional to frequency that can be typically expressed as [38]:

$$\frac{S_I(f)}{I^2} = \frac{C}{f^\sigma} \tag{1.6}$$

where, I is the current flowing through the device, C is a constant typical of the device

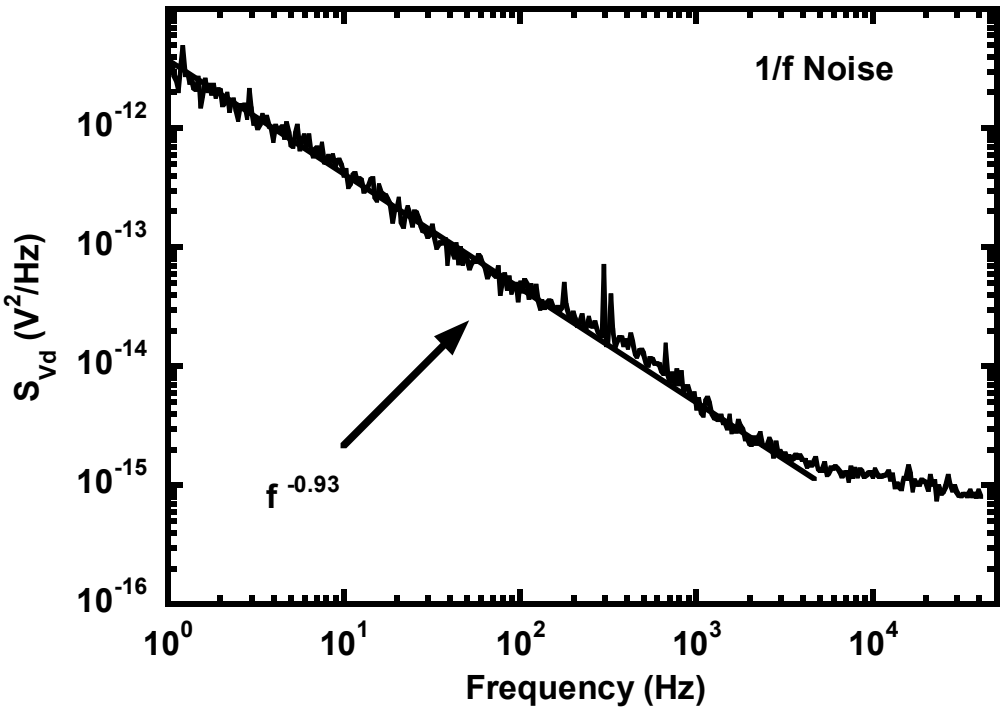

Figure 1.7 1/f noise in TaSiN/HfO_2/SiO_2 MOSFET biased at V_g = 1.13 V and V_d = 0.05 V and at T = 100 K.

and σ ranges from 0.7 to 1.4, in general. A typical spectrum of 1/f noise is plotted in Figure 1.7 for a MOSFET.

Although this noise is a universal phenomenon in active devices, several mechanisms cause 1/f noise. Bulk mobility fluctuations and inversion carrier number fluctuations are the two popular approaches to explain the occurrence of flicker noise in MOSFETs. According to the Hooge's model, low frequency noise is a bulk phenomenon resulting from the fluctuations in the mobility of channel carriers.

It was shown that flicker noise and RTS share a common origin in that the summation of several RTS with distributed characteristic time constants can result in 1/f noise [45,51,52]. According to McWhorter's theory [53], flicker noise is a surface phenomenon caused by the fluctuations in the number of charge carriers in the inversion layer due to capture and emission by traps in the gate insulator. Although experimental data exists to support both the models, the universality of either model is often debatable. However, the Unified Flicker Noise model that is based on Mc Whorter's theory is widely used in circuit simulators today [54].

The aforementioned models are discussed in detail following the general noise theory in Chapter 2. Additionally, the measurement procedure for obtaining 1/f noise, I-V and split C-V data is explained.

In Chapter 3, the data, analysis and discussion of 1/f noise in n,p-channel poly-Si gated MOSFETs with three different gate dielectrics- HfO_2, Al_2O_3/HfO_2, $HfAlO_x$ are presented. The devices had either 1 nm or 4 nm SiO_2 interfacial layer thus giving us an opportunity to understand the effects of interfacial layer thickness.

Chapter 4 deals with 1/f noise in TaSiN and TiN gated MOSFETs with HfO_2 gate dielectric. A comparative study of 1/f noise behavior is presented for metal and poly-Si gated devices. In addition, the effect of the deposition method on interfacial layer quality and thus the overall device performance is studied.

In Chapter 5, 1/f noise modeling is revisited in view of the multi-layered gate stack in high-k MOSFETs. The 'Multi-Stack Unified Noise' model (MSUN) is derived to better model/characterize the 1/f noise in high-k MOSFETs by taking the non-uniform trap density profile and other physical properties of the constituent gate dielectrics in to account. Experimental data is presented for $TaSiN/HfO_2/SiO_2$ gate stack in the 78-350 K range to validate the MSUN model. Finally, the MSUN model is expressed in terms of surface potential based parameters for inclusion in to the circuit simulators.

Chapter 6 provides a summary of conclusions of this dissertation work.

CHAPTER 2

1/f NOISE IN MOSFETs

2.1 Introduction

The random voltage or current fluctuations at the device terminals can arise from noise sources that are intrinsic to the device or by extraneous means like equipment and environmental interferences. The MOSFET intrinsic noise, specifically 1/f noise, is the main object of this work. In this chapter, a relationship between the microscopic noise sources in the channel and the current fluctuations that they cause at the MOSFET terminals is deduced at first. Subsequently, a general noise power spectral density expression is derived that can be used to calculate thermal, 1/f or gate induced noise [55,56,57,58]. Later, the Hooge's mobility fluctuations and Unified Flicker Noise models are introduced. The final model expressions for these are arrived at by using the noise power spectral density expression mentioned before. Finally, details are provided about the measurement set-up and the experimental procedure used to perform low frequency noise, split C-V and DC characterization.

2.2 General MOSFET Noise Theory

Noise that is intrinsic to a semiconductor device is associated with the locally occurring random fluctuations of carrier density or velocity that cause voltage or current fluctuations at the device terminals. In a MOSFET, there can be several local noise

sources in the channel that contribute to the variations in the drain current. In the following, the derivation of the general expression for the current noise power spectral density at the MOSFET output terminals from all the microscopic noise sources in the channel, is presented [55,56,59].

The drain current expression for a MOSFET can be given as,

$$I_d = g(x)\frac{dV}{dx} \tag{2.1}$$

where, $g(x) = -W\mu_{eff}(qN(x))$, W is the width (cm), μ_{eff} is the carrier mobility (cm^2/Vs), q is the electronic charge (C), $N(x)$ is the channel carrier density per unit area at point x along the length (cm^{-2}) and V is the channel quasi-Fermi potential (V).

Considering that a current noise source $h(x,t)$ that is present at a position x along the channel would cause a flow of noise current $\Delta I_d(t)$ in the external leads, the total terminal current would be $I_d + \Delta I_d(t)$. Then the quasi-Fermi potential is $V + \Delta V(t)$, where $\Delta V(t)$ is the fluctuating potential along the channel. Noting that both the conductance $g(x)$ and V are functions of x, $g(x)$ can be represented as a function of V, so that $g(x)=g(V)$. The terminal drain current that includes the noise current can now be written as,

$$I_d + \Delta I_d(t) = g(V + \Delta V(t))\frac{d(V + \Delta V(t))}{dx} + h(x,t) \tag{2.2}$$

For small fluctuations, the right hand side of (2.2) can be expanded using Taylor series and by neglecting the second order terms we have,

$$I_d + \Delta I_d(t) \approx g(V)\frac{dV}{dx} + g(V)\frac{d\Delta V(t)}{dx} + \frac{dg}{dV}\frac{dV}{dx}\Delta V(t) + h(x,t)$$
$$= g(V)\frac{dV}{dx} + \frac{d}{dx}(g(V)\Delta V(t)) + h(x,t) \quad (2.3)$$

In (2.3), $g(V)\frac{dV}{dx} = I_d$ so that,

$$\Delta I_d(t) = \frac{d}{dx}(g(V)\Delta V(t)) + h(x,t) \quad (2.4)$$

Integrating (2.4) with respect to x and applying the short circuit boundary condition that $\Delta V(t) = 0$ at x=0 and x=L,

$$\Delta I_d(t) = \frac{1}{L}\int_0^L h(x,t)dx \quad (2.5)$$

Equation (2.5) gives the relation between the current noise sources in the channel and the current fluctuation at the device terminals. The next step would be to find the autocorrelation function of the drain terminal noise current which is given as,

$$\overline{\Delta I_d(t)\Delta I_d(t+s)} = \overline{\frac{1}{L}\int_0^L h(x,t)dx \frac{1}{L}\int_0^L h(x',t+s)dx'} = \frac{1}{L^2}\int_0^L\int_0^L \overline{h(x,t)h(x',t+s)}dxdx' \quad (2.6)$$

From Wiener-Khintchine theorem [60, 61], the drain current noise power spectral density can be obtained as the Fourier transform of the autocorrelation function in (2.6) and is written as,

$$S_{I_d}(f) = \frac{1}{L^2}\int_0^L\int_0^L S_h(x,x',f)dxdx' \quad (2.7)$$

where, $S_h(x,x',f)$ is the cross power spectral density between noise at points x and x' in the channel. Here, the noise sources are assumed to be spatially uncorrelated so

that, $S_h(x,x',f)$ is a Dirac impulse located at the point $(x'-x)$ and can be represented as,

$$S_h(x,x',f) = F(x',f)\delta(x'-x) \tag{2.8}$$

Using (2.8) in (2.7) gives,

$$S_{I_d}(f) = \frac{1}{L^2}\int_0^L F(x,f)dx \tag{2.9}$$

Evaluating (2.9) in an elemental section between x and $x+\Delta x$, the power spectral density of the local current fluctuations can be obtained as,

$$S_{\Delta I_d}(x,f) = \frac{1}{\Delta x^2}\int_0^{\Delta x} F(x,f)dx = \frac{F(x,f)}{\Delta x} \tag{2.10}$$

Therefore,

$$F(x,f) = S_{\Delta I_d}(x,f)\Delta x \tag{2.11}$$

Finally, the total drain current noise spectral density is given by,

$$S_{I_d}(f) = \frac{1}{L^2}\int_0^L S_{\Delta I_d}(x,f)\Delta x dx \tag{2.12}$$

Eq. (2.12) would be used in deriving the 1/f noise expressions in the next section.

2.3 1/f Noise Models

1/f noise in MOSFETs has been studied for over a few decades now. The exact physical origin responsible for this kind of noise is not completely understood and is still open to debate. In the following, description is provided for the two widely popular models that are used to explain the 1/f noise in MOSFETS namely- Hooge's Bulk Mobility Fluctuation Model and the Unified Flicker Noise Model.

Hooge's Model:

According to Hooge's theory, low frequency noise is a bulk phenomenon originating from the fluctuations in the carrier mobility due to lattice scattering in the semiconductor bulk [62, 63]. The empirical formula takes the following form [48]:

$$\frac{S_{I_d}}{I_d^{\,2}} = \frac{\alpha_H}{fWLN} \tag{2.13}$$

Here, S_{Id} is the power spectral density, I_d is the drain current, α_H is Hooge's parameter that is a dimensionless universal constant (~$2\text{x}10^{-3}$), N is the inversion carrier density per unit area, f is the frequency, L and W are the MOSFET channel length and width, respectively.

In the case of a MOSFET, the final expression for current noise power spectral density is derived as follows. Considering an infinitesimal channel length Δx with $\Delta N = NW\Delta x$ carriers, the spectral density for the local current fluctuations is given using (2.13) as [57],

$$S_{\Delta I_d}(x,f) = \frac{\alpha_H}{fW\Delta xN} I_d^{\,2} \tag{2.14}$$

The total current noise spectral density is then obtained by integrating $S_{\Delta I_d}(x,f)$ along the channel according to (2.12) and can written as,

$$S_{I_d}(f) = \frac{\alpha_H I_d}{fL^2} \int_0^L \left(\frac{I_d}{W\Delta xN} \right) \Delta x dx \tag{2.15}$$

Using $I_d = -W\mu_{eff}(qN(x))\dfrac{dV}{dx}$,

$$S_{I_d}(f) = \left(\frac{\alpha_H q \mu_{eff} I_d}{f L^2} \right) \int_0^L dV \tag{2.16}$$

Considering V_d as the drain to source voltage, the Hooge's model expression for the total current noise spectral density is given by,

$$S_{I_d}(f) = \frac{\alpha_H q \mu_{eff} I_d V_d}{f L^2} \tag{2.17}$$

It should be noted that although α_H was a constant in the original Hooge's formula, it was later observed by many researchers that α_H was lower than $2\text{x}10^{-3}$ and had a weak gate bias dependence. This prompted a modification to the original model allowing α_H to assume lower values when other scattering mechanisms are present according to [64],

$$\alpha_H = 2 \times 10^{-3} \left(\frac{\mu_{eff}}{\mu_{latt}} \right)^2 \tag{2.18}$$

where, the total mobility is given by Matthiessen's rule as,

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_{latt}} + \frac{1}{\mu_{imp}} \tag{2.19}$$

In (2.19) μ_{latt} and μ_{imp} represent the mobility due to lattice scattering and impurity scattering, respectively.

Unified Flicker Noise Model:

According to the "Unified Flicker Noise Model" [54], the traps in the gate oxide cause trapping and de-trapping of charge carriers establishing communication with the channel as shown in Figure 2.1. The two-fold effect that arises is the fluctuations in the channel carrier number and the fluctuations in the mobility due to the Coulombic

interactions between the charged trap sites and the channel carriers. These fluctuations in the carrier number along with the correlated mobility fluctuations cause 1/f noise.

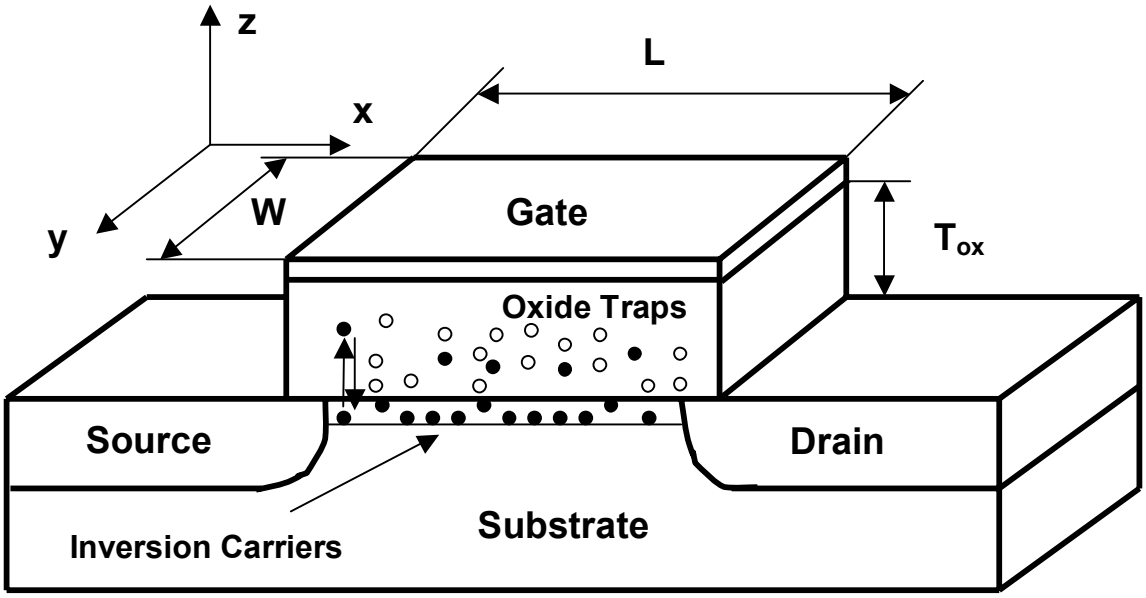

Figure 2.1 Cross section of a MOSFET showing trapping/de-trapping of inversion layer carriers by traps in the gate oxide.

To derive the model expression, we begin with the drain current in a MOSFET that is given as,

$$I_d = W\mu_{eff}(qN)E_x \tag{2.20}$$

where W is the width (cm), μ_{eff} is the carrier mobility (cm^2/Vs), q is the electronic charge (C), N is the channel carrier density per unit area (cm^{-2}) and E_x is the field along the channel (V/cm). The coordinates considered here are as follows: x is along the channel from source to drain; y is along the width of the device; z is into the gate oxide.

Considering an infinitesimal channel length Δx, the fractional change in the local drain current can be written as [54],

$$\frac{\delta I_d}{I_d} = -\left(\frac{1}{\Delta N}\frac{\delta \Delta N}{\delta \Delta N_{ot}} \pm \frac{1}{\mu_{eff}}\frac{\delta \mu_{eff}}{\delta \Delta N_{ot}}\right)\delta \Delta N_{ot} \tag{2.21}$$

where, $\Delta N = NW\Delta x$ is the inversion charge in the area, $W\Delta x$, $\Delta N_{ot} = N_{ot}W\Delta x$ is the number of occupied traps in the corresponding area in the gate oxide ($W\Delta x$), $R = \left|\frac{\delta \Delta N}{\delta \Delta N_{ot}}\right|$ is the coupling coefficient between the fluctuations in the channel charge and charge trapped in the gate oxide. This value can be approximated to unity in the strong inversion region. However, the expression in the weak inversion can be found by considering the fact that a fluctuation in the trapped charge (Q_t) induces fluctuations in the gate (Q_G), depletion (Q_D), inversion (Q_{inv}) and interface trap (Q_{it}) charges [65]. By virtue of charge conservation,

$$\delta Q_G + \delta Q_{it} + \delta Q_D + \delta Q_{inv} + \delta Q_t = 0 \tag{2.22}$$

Therefore,

$$\frac{\delta \Delta N}{\delta \Delta N_{ot}} = \frac{\delta Q_{inv}}{\delta Q_t} = -\left(\frac{\delta Q_{inv}}{\delta Q_G + \delta Q_{it} + \delta Q_D + \delta Q_{inv}}\right) \tag{2.23}$$

Considering $\delta\psi_s$ as the fluctuations in the surface potential and with C_{ox}, C_{it}, C_D, and C_{inv} as the oxide, interface trap, depletion and inversion layer capacitances per unit area, respectively,

$\delta Q_G = -C_{ox}\delta\psi_s$, $\delta Q_{it} = -C_{it}\delta\psi_s$, $\delta Q_D = -C_D\delta\psi_s$, $\delta Q_{inv} = -C_{inv}\delta\psi_s$

Using $C_{inv} = -(q/kT)Q_{inv}$,

$$R = \left| \frac{(q/kT)Q_{inv}}{C_{ox} + C_{it} + C_D - (q/kT)Q_{inv}} \right| = \frac{N}{N + N^*} \tag{2.24}$$

where, $N^* = (kT/q^2)(C_{ox} + C_{it} + C_D)$. It should be noted here that R approaches unity in the inversion region and assumes lower values for weak inversion region.

The sign in front of the mobility term in (2.21) is chosen as positive for traps that are charged when filled by a carrier resulting in repulsive type of Coulomb interaction with the channel carriers and it is negative for traps that become neutral after capturing a carrier.

Now, from Matthiessen's rule, the effective mobility can be written as,

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_{others}} + \frac{1}{\mu_{ox}} = \frac{1}{\mu_{others}} + \alpha_{sc} N_{ot} \tag{2.25}$$

where, μ_{ox} is the mobility due to oxide charge scattering, μ_{others} is the mobility due to other scattering phenomena and α_{sc} is the Coulomb scattering coefficient (Vs) that is a function of inversion carrier density due to screening.

Differentiating (2.10) with respect to N_{ot} gives,

$$\frac{\delta\mu_{eff}}{\delta N_{ot}} = \alpha_{sc}\mu_{eff}^{\ 2} \quad \text{or} \quad \frac{\delta\mu_{eff}}{\delta\Delta N_{ot}} = \frac{\alpha_{sc}\mu_{eff}^{\ 2}}{W\Delta x} \tag{2.26}$$

Substituting (2.26) in (2.21) we have,

$$\frac{\delta I_d}{I_d} = -\left(\frac{1}{N} \pm \alpha_{sc}\mu_{eff}\right)\frac{\delta\Delta N_{ot}}{W\Delta x} \tag{2.27}$$

Then the expression for power spectral density of local current fluctuations becomes,

$$S_{\Delta I_d}(x,f) = \left[\frac{I_d}{W\Delta x}\left(\frac{1}{N} \pm \alpha_{sc}\mu_{eff}\right)\right]^2 S_{\Delta N_t}(x,f) \tag{2.28}$$

Here, $S_{\Delta N_t}(x,f)$ is the power spectral density of the mean square fluctuations in the trapped charge carriers over the area $W\Delta x$ and is given as,

$$S_{\Delta N_t}(x,f) = \int_{E_v}^{E_c}\int_0^W\int_0^{T_{ox}} 4N_t(E,x,y,z)\Delta x f_t(1-f_t)\frac{\tau(E,x,y,z)}{1+\omega^2\tau^2(E,x,y,z)}\,dE\,dy\,dz \tag{2.29}$$

where, $\tau(E,x,y,z)$ is the trapping time constant in the gate dielectric (s), $\omega = 2\pi f$ is angular frequency (rad/s), E denotes the trap energy level (eV), $f_t = \left[1/\left(1+\exp[(E-E_{fn})/kT]\right)\right]$ is the trap occupancy function, E_{fn} is the quasi-Fermi level (eV), $N_t(E,x,y,z)$ is the distribution of traps in the gate oxide ($cm^{-3}eV^{-1}$), E_c is the conduction band edge (eV), E_v is the valence band edge (eV) and T_{ox} is the oxide thickness (cm). The term $f_t(1-f_t)$ acts as a delta function around the quasi-Fermi level so that the major contribution to noise is made by the traps in a small energy interval around this level. Assuming uniform trap density distribution in the gate dielectric, $N_t(E,x,y,z)$ in (2.29) can now be replaced by $N_t(E_{Fn})$.

Now, $$(1-f_t) = \left[\frac{\exp[(E-E_{fn})/kT]}{\left[1+\exp[(E-E_{fn})/kT]\right]}\right] \quad \text{and}$$

$$\frac{df_t}{dE} = \left[\frac{-\exp[(E-E_{fn})/kT]}{\left[1+\exp[(E-E_{fn})/kT]\right]^2}\right]\times\frac{1}{kT}$$

$$= -\left[\frac{1}{\left[1+\exp[(E-E_{fn})/kT]\right]}\right]\times\left[\frac{\exp[(E-E_{fn})/kT]}{\left[1+\exp[(E-E_{fn})/kT]\right]}\right]\times\frac{1}{kT}$$

i.e. $$\frac{df_t}{dE} = -\frac{1}{kT} f_t(1-f_t) \tag{2.30}$$

Since the traps below a few *kT* from the quasi-Fermi level are always full and those above a few *kT* from the quasi-Fermi level are always empty, the upper and lower limits of the energy integral can be approximated as $E_c = \infty$ and $E_v = -\infty$. Consequently, the energy integral in (2.29) can be solved by substituting $f_t(1-f_t) = -kTdf_t/dE$ and changing the upper limit to *0* and the lower limit to *1*.

Equal energy tunneling phenomenon is assumed here and accordingly, the characteristic time constant for the channel carriers tunneling into the traps located in the gate oxide is given from WKB (Wentzel-Kramer-Brillouin) approximation as [66],

$$\tau = \tau_0 \exp(\gamma z) \tag{2.31}$$

so that, $$d\tau = \tau_0 \gamma \exp(\gamma z) dz \quad \text{or} \quad \frac{d\tau}{\gamma\tau} = dz \tag{2.32}$$

Here, $\tau_0 = 10^{-10} s$ and is the trap time constant at the oxide/substrate interface, $\gamma = \frac{4\pi}{h}\sqrt{2m^*\Phi}$ is the electron tunneling coefficient in the interfacial layer (cm^{-1}) with a typical value of $10^8\ cm^{-1}$ for Si/SiO_2 system, m^* is the effective mass of an electron in the gate oxide (Kg), and Φ is the barrier height for tunneling carriers (eV).

Substitution of (2.30) and (2.32) in (2.29) gives,

$$S_{\Delta N_t}(x,f) = \frac{N_t(E_{f_n})WkT\Delta x}{\gamma f} \tag{2.33}$$

The final expression for drain noise power spectral density is obtained using (2.28) and (2.33) in (2.12) as,

$$S_{I_d}(f) = \frac{kTI_d^{\,2}}{\gamma f W L^2} \int_0^L \left(\frac{R}{N(x)} \pm \alpha_{sc}\mu_{eff}\right)^2 N_t(E_{Fn})dx \tag{2.34}$$

where, *N(x)* is the channel carrier density per unit area at a point *x* in the channel (cm^{-2}) and $N_t(E_{Fn})$ remains in the integral due to the variation of quasi-Fermi level along the channel. For small drain voltages the channel quasi-Fermi level can be assumed to be constant which would mean a uniform carrier distribution along the channel and taking *R*=1in the strong inversion region, (2.34) can be simplified as,

$$S_{I_d}(f) = \frac{kTI_d^{\,2}}{\gamma f W L} \left(\frac{1}{N} \pm \alpha_{sc}\mu_{eff}\right)^2 N_t \tag{2.35}$$

In the initial part of this work, the above expression was used to model the noise. Albeit, with a modification for the Coulomb scattering parameter as will be described later.

2.4 Experimental Procedure

The MOSFETs used in this work were provided by Freescale Semiconductor Inc. Firstly, the layout on the wafers was inspected with the help of a powerful microscope and the wafers were diced to obtain individual dies. Each die, containing the isolated MOSFETs, was mounted on a 0.4×0.4 inch 64 lead package and the devices of interest were located. A 1 mil (25 μm) aluminum wire was used to make bonds from the package leads on to the bond pads of the device under study (DUT) using 7400A West Bond ultrasonic bonder. The package leads, onto which the bonds would be made, were shorted prior to bonding. This was to ensure the safety of devices from possible voltage

spikes or electro-static discharge (ESD). The short on the leads remained at all times when measurements were not being made and a grounded wrist strap was always used while handling the devices. In the following subsections, the measurement set-up and experimental procedure are presented for conducting DC, low frequency noise and split C-V measurements on MOSFETs.

Low frequency Noise Measurements:

The standard noise measurement set-up included a low-noise DC biasing circuitry, an EG&G PAR113 pre-amplifier (that is battery powered for low noise) and a HP 3562A dynamic signal analyzer. Here, several rechargeable Ni-Cd batteries were connected together in series to form two individual sets that provided the necessary gate-source and drain-source biases through the resistive voltage divider networks as shown in Figure 2.2. To be able to vary the device terminal voltages, ten-turn wire wound variable resistors (maximum 100 kΩ) were employed. The minute fluctuations in the drain-source voltage were amplified to the measurable range using low noise EG&G PAR113 pre-amplifier operating in the 0.03 Hz-300 kHz range with voltage gain set to 1000. The output of the pre-amplifier is fed to HP 3562A dynamic signal analyzer that performs the fast Fourier transform on the time domain signal (V_d) to yield the voltage noise power spectral density (S_{Vd}) in the 1-100 kHz range after correcting for pre-amplifier gain. In order to obtain a stable spectrum, the number of averages was set at 30 and a 90% sampling window overlap was used for optimal real time processing. A computer interface was provided to control the dynamic signal analyzer and automate the noise data collection.

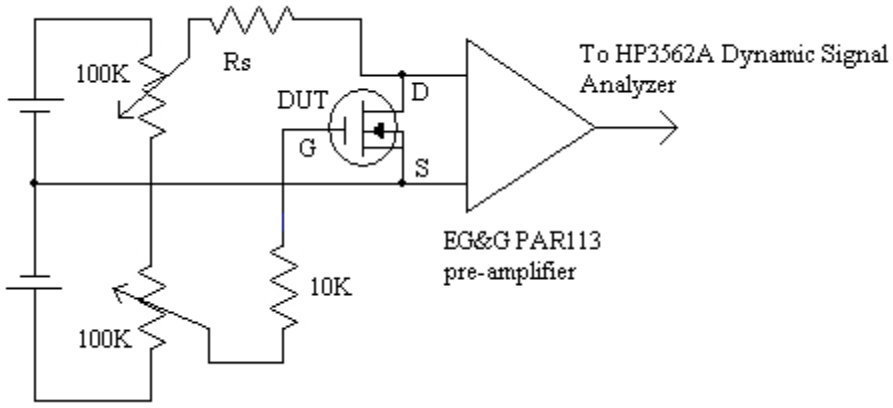

Figure 2.2 Typical bias arrangement for an n-MOSFET. The series resistance (R_s) in the drain circuit is chosen to be 10 times the channel resistance. This ensures a constant voltage source providing the drain bias so that only device noise gets amplified.

As such, the low frequency noise exhibited by the metal film resistors used here is significantly low when compared to MOSFET noise. Additionally, by appropriate choice of series resistance values (R_s), the sum total of 'R_s' and the resistance of the potentiometer is ensured to be at least 10 times higher than the MOSFET channel resistance. This arrangement makes a low noise voltage supply across the drain and source terminals further minimizing any noise contribution from the biasing circuitry so that the amplified noise at the output terminals of the low noise pre-amplifier comes mainly from the DUT. In addition, the DUT is placed in a 6 ft. x 6 ft. shielded room with an attenuation capability of 100 dB to electric fields, 30 dB to magnetic fields at 60 Hz and plane waves from 14 Hz to 10 GHz. Furthermore, connections were made by BNC cables whose guards were tied together to the earth ground of the shielded room along with the source terminal (that acts as signal ground) thus preventing the occurrence of ground loops. It should be noted that the source and substrate terminals

were shorted for all noise measurements. After avoiding the stray noise sources by taking the precautions mentioned above, the background noise comprising mainly of pre-amplifier inherent noise is measured. The MOSFET is biased at the desired gate overdrive and the noise data is collected for zero drain bias (V_d = 0 V). The back ground noise thus obtained is subtracted from subsequent noise data measured at the set gate overdrive for different drain voltages. This yields the actual device noise. The back ground noise measurement is repeated for all gate overdrives considered.

In order to ensure the safety of the DUT during its handling, the procedure followed is explained next. At first, all the connections were made as described above and the potentiometer knobs on the bias box were set to zero drain and gate biases. The package containing the DUT, with its leads shorted, was then mounted on the cryostat and the short was removed. The bias was then adjusted to the desired values and the noise data is collected. When the noise measurements were done, the bias settings were again set to zero and the short on the leads is put on before dismounting the packaged DUT.

In the passing, it should be mentioned that wafer level measurements were performed on a few device samples at room temperature using an enclosed low noise 8600 series MicroManipulator probe station with proper grounding. The measurement procedure was essentially the same as above. After making the connections and setting the bias values to zero, the probe contact was made on the bond pads at the end to continue with measurements and upon concluding the measurements a reverse order was followed.

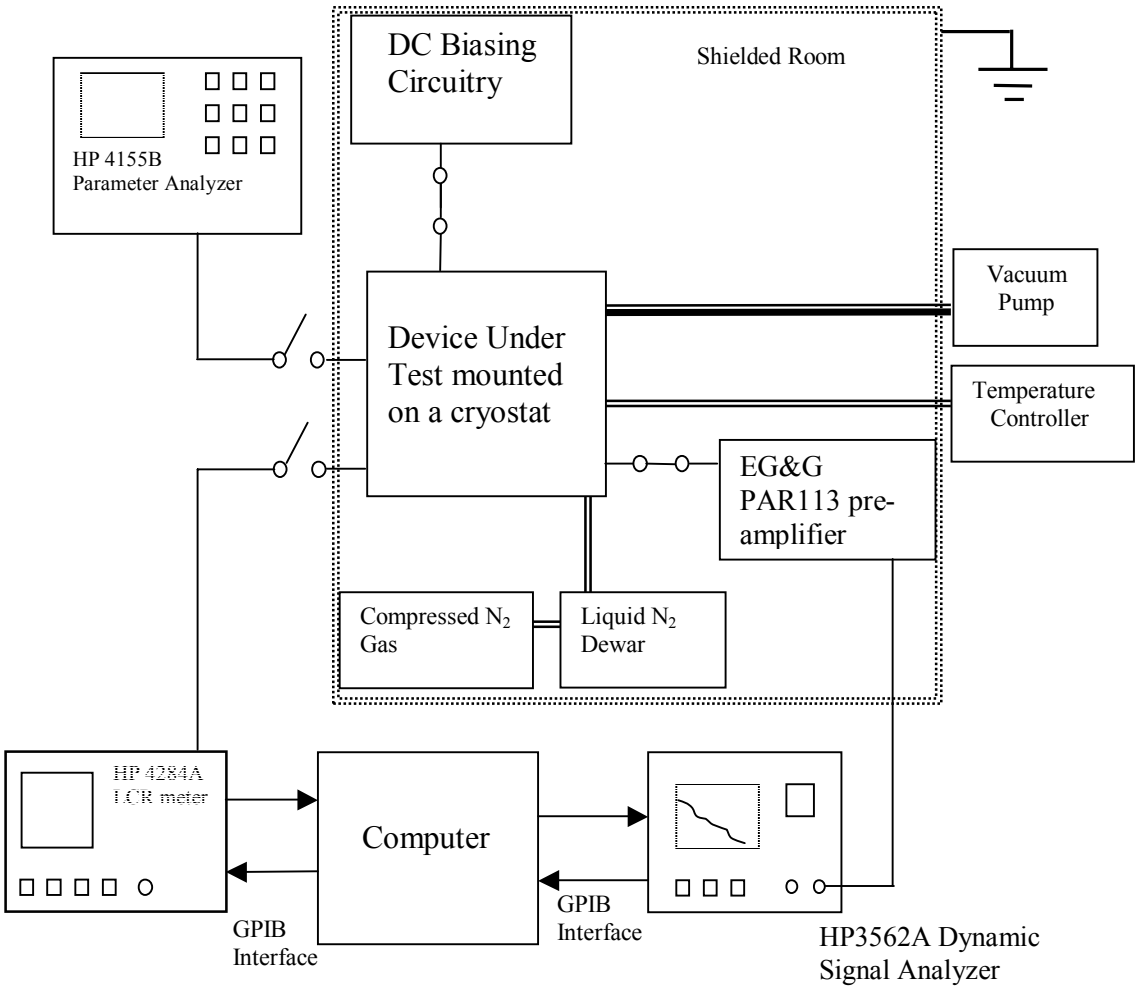

Figure 2.3 An overview of variable temperature measurement system. The DUT is placed in the shielded room enclosure to minimize interference from stray noise sources.

Figures 2.3 and 2.4 depict the setup to perform variable temperature measurements. The packaged device would be mounted on the cold finger of a continuous-flow cryostat (Cryo RC102) that is evacuated to ~80 mTorr by a vacuum pump. This facilitated good temperature control and ensured that no condensation

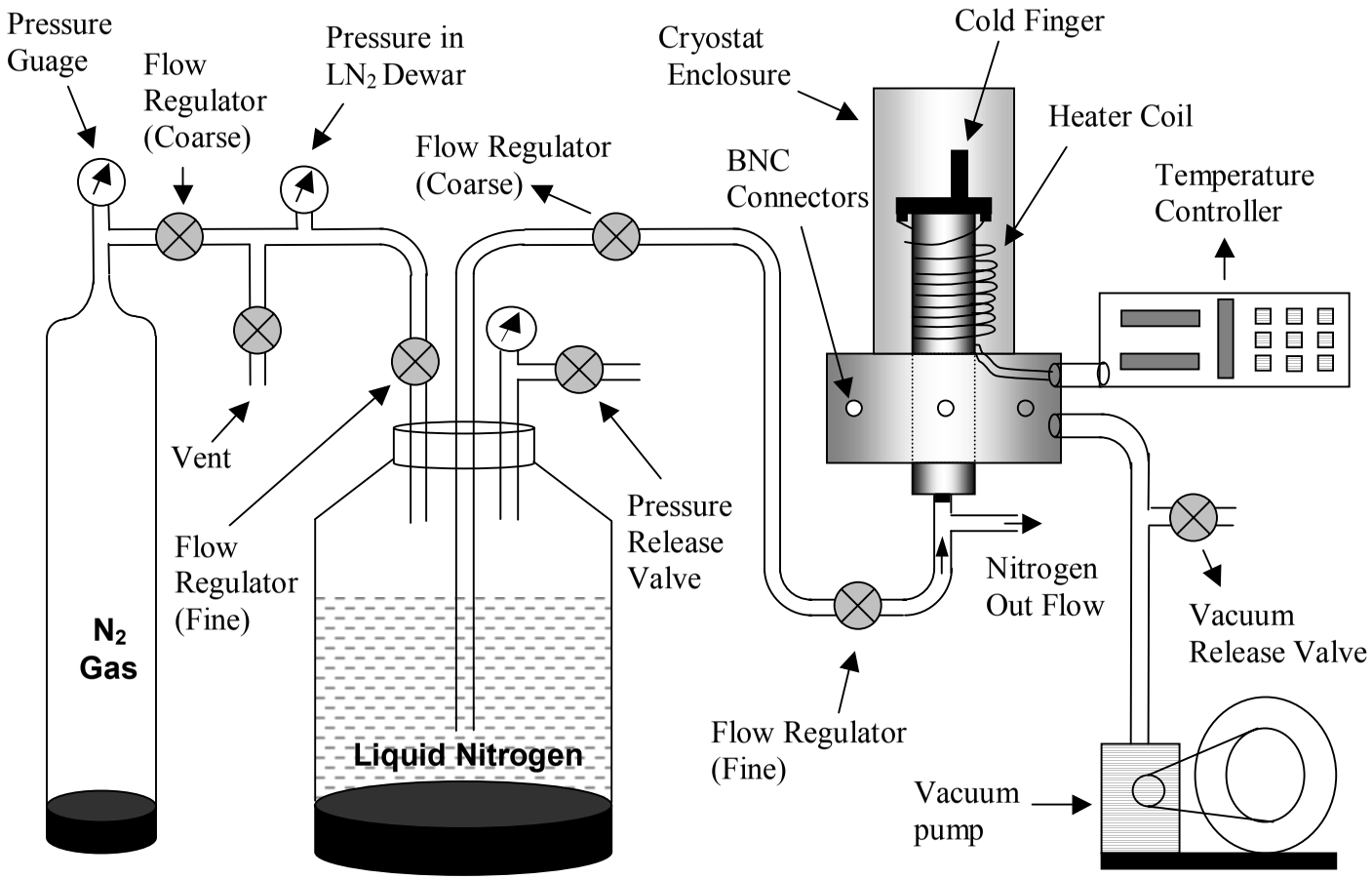

Figure 2.4 Schematic of the variable temperature measurement set-up.

occurred on the die. The device temperature was lowered by regulated liquid nitrogen flow from a dewar. A steady flow of liquid nitrogen was ensured by maintaining a constant pressure in the dewar using compressed nitrogen gas. This cooling system in tandem with Lake Shore 330 auto tuning temperature controller enabled stabilization of the temperature at a particular set point. In this work, measurements were performed in the 78-350 K range on metal gated MOSFETs with a step size of 25 K in 100-350 K.

DC Measurements:

Various MOSFET device performance parameters were required for noise analysis. Thus, DC characterization was always done prior to the noise measurements. Additionally, the DC measurements were repeated after the noise measurements to check for any change in the device characteristics. A typical set of DC curves are shown in Figure 2.5 that were obtained using HP-4155B semiconductor parameter analyzer on TaSiN/2.7 nm HfO_2/1 nm SiO_2 10 μm/0.18 μm n-channel MOSFET. From the I_d-V_d and I_d-V_g curves, parameters like ac conductance ($g_d = \partial I_d / \partial V_d$), transconductance ($g_m = \partial I_d / \partial V_g$), subthreshold slope ($S = \partial \log(I_d) / \partial V_g$) were derived. The threshold voltage (V_t) was obtained as the intercept of the tangent to the $\sqrt{I_d}$ vs. V_g curve at the point of maximum slope $(d\sqrt{I_d}/dV_g)$. The maximum gate leakage was ~10^{-2} Acm^{-2} at the highest recommended operating gate voltage for the high-k MOSFETs used in this work and any value higher than this would imply a damaged

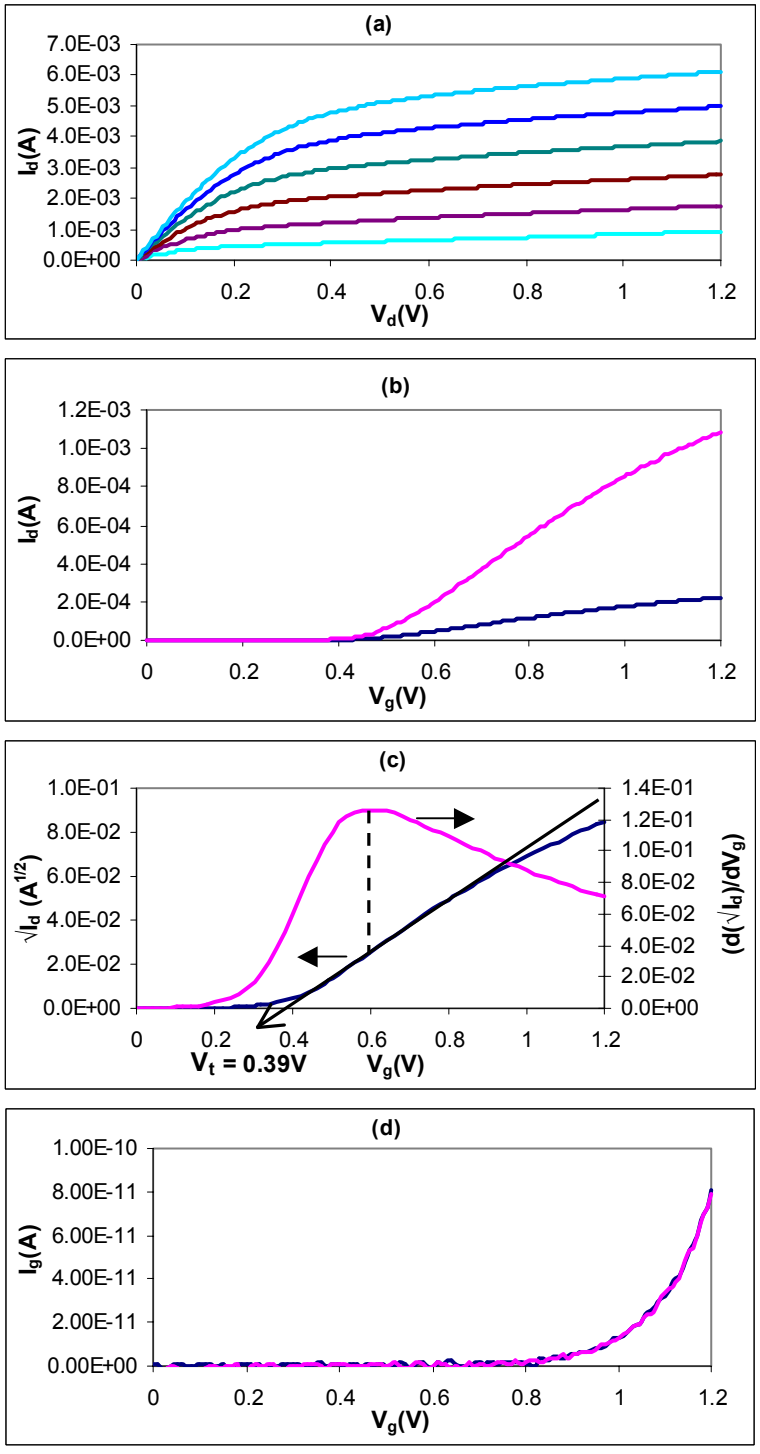

Figure 2.5 (a) I_d-V_d curve for V_g varying from 0.6 to 1.1 V in 0.1 V steps. (b) I_d-V_g curve for V_d =10 mV and 50 mV. (c) Plot for threshold voltage extraction. (d) Gate leakage current vs. V_g for V_d =10 mV and 50 mV.

device. Thus, the gate leakage served as a figure of merit for the DUTs. It should be noted that the source and substrate were shorted for all DC measurements.

In the initial part of the work on poly-Si gated MOSFETs, the carrier mobility in the linear region of operation was extracted from the transconductance characteristic using, $\mu_{eff} = \frac{g_m L_{eff}}{W C_{ox} V_d}$. In addition, the inversion charge was calculated as, $Q_{inv} = C_{ox}(V_g - V_t)$. However, for the latter part these two parameters were directly measured using split C-V technique as described in the next section.

Split C-V measurements:

The inversion layer charge density and mobility values at different gate biases are needed for the noise analysis. This section provides the theory and experimental procedure, that was originally suggested by Koomen [67], to perform conventional split C-V measurements and accurately determine the MOSFET inversion layer charge density and channel carrier mobility from the gate to channel capacitance.

From MOSFET theory, the applied gate voltage is the sum of surface potential (ψ_s) and potential across the oxide (V_{ox}) i.e.,

$$V_g = \psi_s + V_{ox} \qquad \text{or} \qquad V_g = \psi_s + \frac{Q_{sc}}{C_{ox}}$$

where the inversion layer charge and charges in the bulk constitute the semiconductor charge (Q_{sc}),

$$Q_{sc} = Q_{inv} + Q_{bulk} \tag{2.36}$$

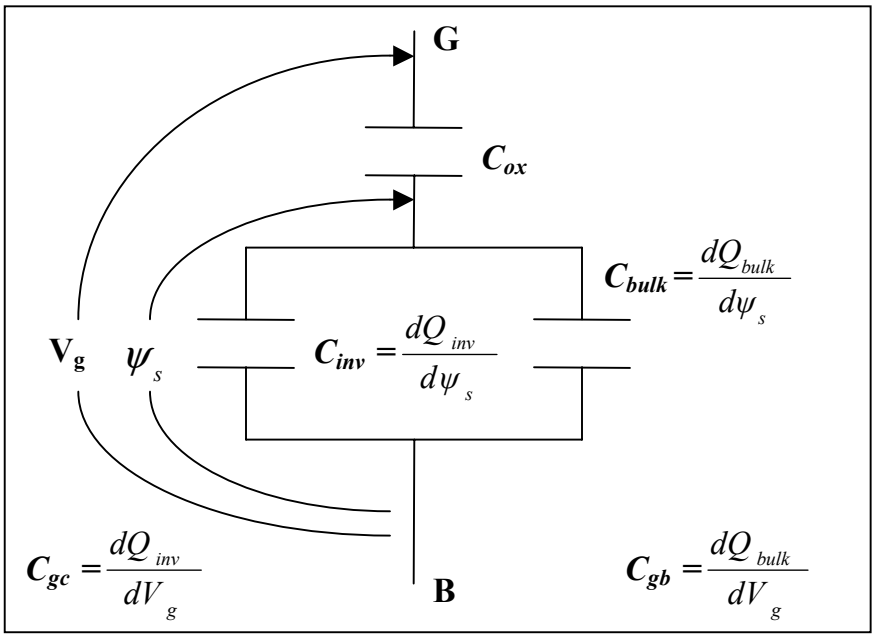

Figure 2.6 MOSFET capacitances. C_{inv}, C_{bulk} are given as the derivative of inversion and bulk charges, respectively, with respect to surface potential while C_{gc}, C_{gb} are obtained from the derivative of the inversion and bulk charges with respect to the applied gate potential [67].

Figure 2.6 depicts the MOS structure in terms of the capacitors along with the notation used.

Differentiating the surface potential with respect to the applied gate voltage (V_g),

$$\frac{d\psi_s}{dV_g} = (1 - \frac{dQ_{sc}}{d\psi_s}\frac{d\psi_s}{dV_g}\frac{1}{C_{ox}}) \qquad \text{or} \qquad \frac{d\psi_s}{dV_g}(1 + \frac{dQ_{sc}}{d\psi_s}\frac{1}{C_{ox}}) = 1$$

$$\frac{d\psi_s}{dV_g} = \frac{C_{ox}}{C_{ox} + \frac{dQ_{sc}}{d\psi_s}} \qquad \text{or} \qquad \frac{d\psi_s}{dV_g} = \frac{C_{ox}}{C_{ox} + \frac{d(Q_{inv} + Q_{bulk})}{d\psi_s}}$$

$$\frac{d\psi_s}{dV_g} = \frac{C_{ox}}{C_{ox} + \frac{dQ_{inv}}{d\psi_s} + \frac{dQ_{bulk}}{d\psi_s}} \tag{2.37}$$

Gate to channel capacitance (C_{gc}) is given by,

$$C_{gc} = \frac{dQ_{inv}}{dV_g} = \frac{dQ_{inv}}{d\psi_s}\frac{d\psi_s}{dV_g} = \frac{\frac{dQ_{inv}}{d\psi_s}C_{ox}}{C_{ox} + \frac{dQ_{inv}}{d\psi_s} + \frac{dQ_{bulk}}{d\psi_s}} \tag{2.38}$$

and gate to bulk capacitance will be,

$$C_{gb} = \frac{dQ_{bulk}}{dV_g} = \frac{dQ_{bulk}}{d\psi_s}\frac{d\psi_s}{dV_g} = \frac{\frac{dQ_{bulk}}{d\psi_s}C_{ox}}{C_{ox} + \frac{dQ_{inv}}{d\psi_s} + \frac{dQ_{bulk}}{d\psi_s}} \tag{2.39}$$

From (2.38) and (2.39),

$$C_{gc} = \frac{C_{inv}C_{ox}}{C_{ox} + C_{inv} + C_{bulk}} \quad ; \quad C_{gb} = \frac{C_{bulk}C_{ox}}{C_{ox} + C_{inv} + C_{bulk}}$$

so that, $C_g = C_{gc} + C_{gb}$

Furthermore,

$$Q_{inv} = \int_{-\infty}^{V_g} C_{gc}(V_g)\, dV_g \quad \text{and} \quad Q_{bulk} = \int_{-V_g}^{\infty} C_{gb}(V_g)\, dV_g$$

Thus the effective mobility can be obtained as,

$$\mu_{eff} = \frac{g_d}{(W/L)\, Q_{inv}} \tag{2.40}$$

The g_d characteristic in (2.40) is to be obtained at a very low drain bias, typically10-20 mV.

In this work, the split C-V measurements were done on 10 µm x 10 µm MOSFETs using HP4284A LCR meter. After performing the necessary compensations for the stray capacitances introduced by the measurement system, the connections for C_{gc} measurement were made as shown in Figure 2.7. The gate was connected to the High end of the LCR meter while the drain and source terminals were shorted to the Low end of HP4284A. The substrate was connected to the guard terminal. This arrangement ensured the accurate counting of inversion charge, as the bulk charge was bypassed to the system ground (guard terminal).

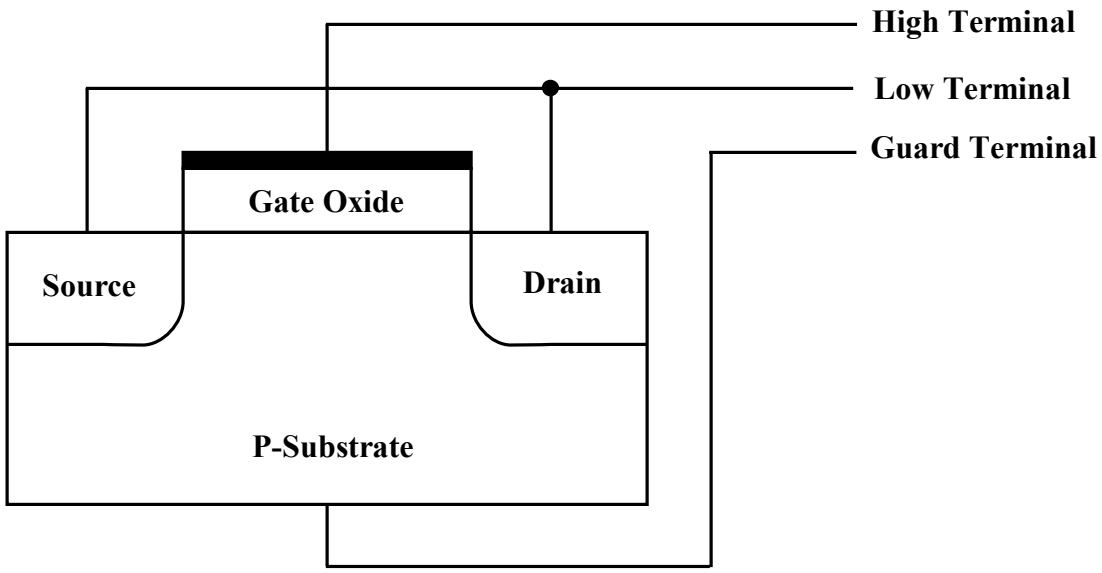

Figure 2.7 Set-up for gate to channel capacitance measurement (C_{gc}). The High terminal of the LCR meter was connected to the gate while source and drain were shorted to the Low end of HP4284A. The substrate response to the applied bias was bypassed (from the internal ammeter) to the guard/ground terminal [67].

For measuring C_{gc}, the DC bias on the gate was varied from -1.5 V to 1.5 V (in steps of 10 mV) with an impinged AC voltage of 10 mV (RMS) at 1 MHz. Using 1MHz frequency ensured that interface traps do not follow the AC signal and thus there

is no capacitance contribution from them. The measurement was automated using Lab-VIEW. A typical gate to channel capacitance curve for an n-type MOSFET is shown in Figure 2.8. The non-zero constant values in the accumulation region are due to the overlap capacitances that might be resulting from the contact pads and/or gate to source/drain overlap regions and was corrected by subtracting the C_{gc} curve for the entire bias range by $C_{overlap}$. The inversion charge was extracted from the corrected curve as, $Q_{inv} = \int_0^{V_g} C_{gc}\, dV_g$.

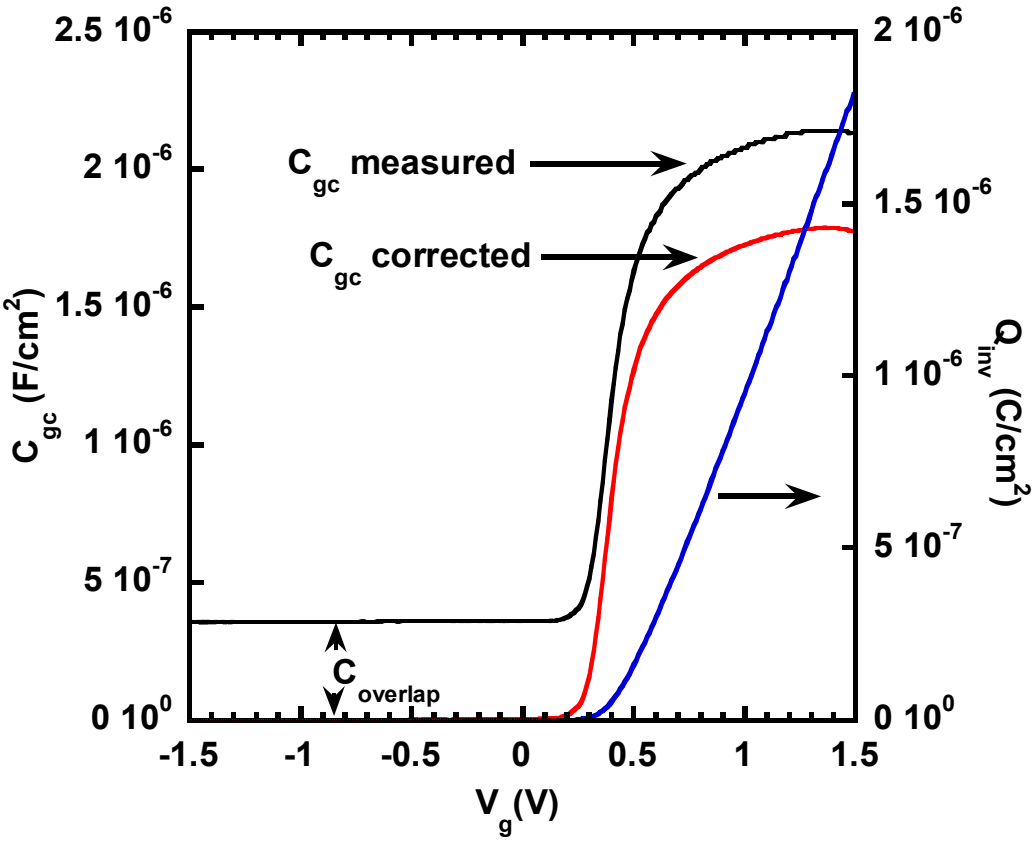

Figure 2.8 Gate to channel capacitance of TaSiN/HfO_2/SiO_2 MOSFET (n-channel) from conventional split C-V measurement that is corrected for overlap capacitance and inversion layer charge.

Finally, the effective mobility was extracted using I_d-V_g characteristic at V_d = 10 mV in $\mu_{eff} = I_d L/WQ_{inv}V_d$. Assuming that mobility is not affected by the drain voltage in the linear region, the inversion layer charge at V_d = 50 mV was calculated from I_d-V_g characteristic at V_d = 50 mV and the mobility as obtained above. In addition, the capacitance equivalent thickness (t_{CET}) was calculated using the C_{gc} value at a gate voltage of 1.5 V as $t_{CET} = (\varepsilon_0 * 3.9)/C_{gc}(V_g = 1.5V)$.

Since high-k gate dielectrics were used here, the gate leakage was at least an order of magnitude lower than the drain current even at the highest gate overdrive. If significant gate leakage currents are observed, appropriate corrections can be made as suggested in [68,69]. Further, the intent here was to obtain the inversion layer charge and carrier mobility for use in noise analysis. Thus, the description here is limited to C_{gc} measurement only. The reader is directed to Appendix A for additional information.

2.5 Summary

The general expression for noise power spectral density at the MOSFET terminals was derived. The two widely popular MOSFET 1/f noise models- Hooge's Bulk Mobility Fluctuation Model and the Unified Flicker Noise Model, were introduced. Subsequently, the final model expressions were arrived at by using the general noise expression and based on the underlying physical mechanisms assumed by the models. Finally, a detailed explanation was provided for the measurement set-up and experimental procedure to perform 1/f noise, DC and conventional split C-V measurements.

CHAPTER 3

1/f NOISE IN POLY-Si/HIGH-k MOSFETs

3.1 Introduction

In this chapter, a general discussion is presented on room temperature low frequency noise characteristics of n and p-channel MOSFETs with three different high-k gate dielectrics- HfO_2, $HfAlO_x$ and HfO_2 capped by Al_2O_3. Additionally, the effect of the thickness of the SiO_2 interfacial layer on device characteristics is studied. Finally, comments are made on the effect of high-k dielectrics on various MOSFET performance parameters.

3.2 MOSFET Device Information and Experiments

Poly-Si gated MOSFETs with three high-k dielectric compositions- Al_2O_3 (top layer)/HfO_2 (bottom layer), HfO_2, and $HfAlO_x$, were considered in this study. The aforementioned high-k layers were on top of either 1 nm (in Single-Gate-Oxide/SGO devices) or 4 nm (in Double-Gate-Oxide/DGO devices) SiO_2 interfacial layer. The physical thickness of the Al_2O_3/HfO_2 gate stack made by atomic layer deposition (ALD) was 3 nm/3 nm, which yielded an equivalent thickness (EOT) of 3.3 nm for SGO devices and 6.3 nm for DGO devices. The HfO_2 gate dielectric was grown by metal-oxide chemical vapor deposition (MOCVD) to 5.5 nm, resulting in an EOT of 2.3 nm and 5.3 nm, respectively, for SGO and DGO devices. The EOT values for SGO and DGO MOSFETs with ALD-deposited $HfAlO_x$ were 2.85 nm and 5.85 nm, respectively.

The physical thickness value of $HfAlO_x$ is not available. While the gate width was 10 μm for all the devices, gate (mask) lengths for SGO devices was 0.135 μm, 0.165 μm, and 0.18 μm and that for DGO MOSFETs was 0.3 μm and 0.36 μm. A 0.07 μm length correction was done in calculations for etch-caused gate trimming. The channel doping concentrations for NMOS and PMOS were $7x10^{16}$ cm^{-3} and $3x10^{16}$ cm^{-3}, respectively. The following abbreviations will be used in further discussions- NSGO and PSGO for n and p type single gate oxide devices with 1 nm SiO_2 interfacial layer, NDGO and PDGO for n and p type double gate oxide devices with 4 nm SiO_2 interfacial layer.

As discussed in Chapter 2, DC characterization was performed initially to obtain various device performance parameters. Subsequently, the 1/f noise measurements were done using the set-up mentioned earlier. It should be noted that the source and substrate are shorted at all times in DC and noise measurements. Noise measurements were performed for variable band bending conditions by driving the gate from sub-threshold to strong inversion region at a constant V_d (±40 mV / ± 50 mV and ±0.4 V). In addition, band bending conditions were kept constant with respect to the gate overdrive (V_g-V_t) of 0.1 V for different values of V_d in the linear region. The background noise was always subtracted from the measured noise to obtain the net device noise. The final step was to obtain the DC data to check for any alteration in device characteristics after the noise measurements.

A typical voltage noise spectral density plot is shown in Figure 3.1. The n-type SGO device with $HfAlO_x$ was biased at a constant gate overdrive of 0.1 V in the linear regime. The solid lines depict the straight-line fit to the data for 1-100 Hz range.

The voltage power spectral density can be converted into current power spectral density using,

$$S_{I_d} = S_{V_d} \cdot (g_d)^2 \tag{3.1}$$

For the conversion above, S_{Vd} value at 1Hz was obtained from the fitted line. In addition, the slope of the straight line fit to the curve gives the frequency exponent σ (as in $1/f^{\sigma}$) which conformed to the range of 0.9-1.2 for all poly-Si gated MOSFETs in this study and did not follow any particular trend with respect to the applied bias. In general, $0.7 < \sigma < 1.4$ is noted as flicker noise. The 1 Hz value of S_{Id} as obtained from (3.1) will be considered for further analysis.

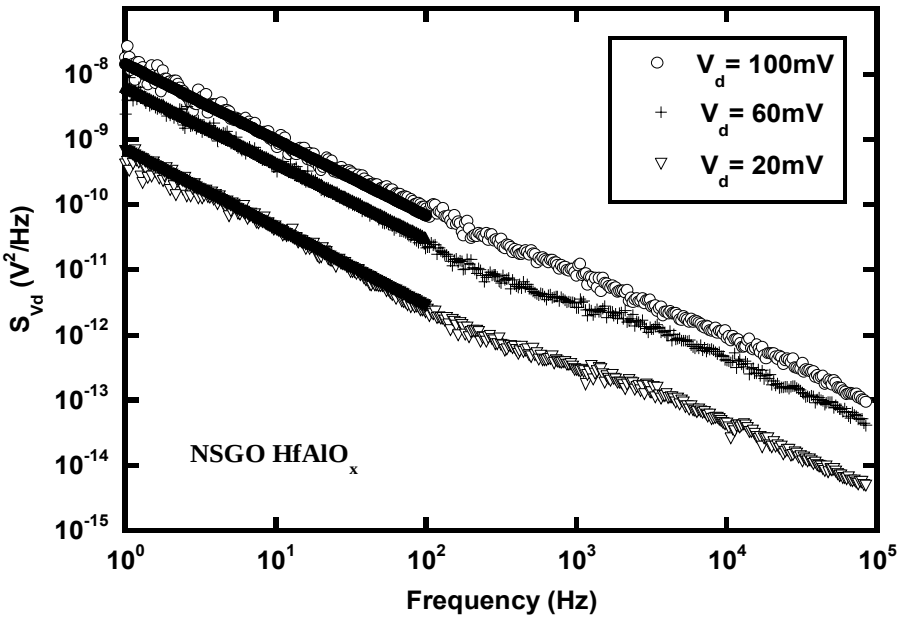

Figure 3.1 Drain voltage noise power spectral density S_{Vd} ($V^2\,Hz^{-1}$) vs. frequency in log-log scale for an NSGO with $HfAlO_x$ (W/L = 10.02 μm/0.165 μm). The gate overdrive was 0.1 V with V_d = 20/60/100 mV. The device exhibited $1/f^{\sigma}$ noise with $1 < \sigma < 1.2$. Here, σ was obtained as the slope of the straight line fit in the 1-100 Hz region as depicted by the solid line.

3.3 Physical Mechanism for Noise

The underlying noise causing mechanism will be established here. An explanation was provided in Chapter 2 about the two most widely accepted 1/f noise models - Hooge's Model [62,63] and Unified Flicker Noise Model [54]. The general empirical Hooge's formula is given by:

$$\frac{S_{I_d}}{I_d^{\,2}} = \frac{\alpha_H}{fWLN} \tag{3.2}$$

where, S_{Id} is the power spectral density, I_d is the drain current, α_H is the Hooge's coefficient, f is the frequency, N is the inversion carrier density per unit area, L and W are the MOSFET channel length and width, respectively.

Unlike Hooge's model that is empirical in nature, the Unified Model gives better insight about the physical mechanism and is given as [54],

$$S_{I_d} = \frac{kTI_d^{\,2}}{\gamma fWL}\left(\frac{1}{N} \pm \alpha_{sc}\mu_{eff}\right)^2 N_t \tag{3.3}$$

where, N_t is the trap density in $cm^{-3}eV^{-1}$, μ_{eff} is effective mobility ($cm^2V^{-1}s^{-1}$), α_{sc} is the screened scattering coefficient (Vs), N is the channel carrier density per unit area (cm^{-2}), γ is the tunneling coefficient (cm^{-1}), f is the frequency (Hz), T is the absolute temperature (K), k is the Boltzmann constant (eVK^{-1}), L and W are the MOSFET channel length and width, respectively.

In order to confirm the validity of the above models, a general rule of thumb was proposed by [70], where the power spectral density equation was rewritten for both models as:

Hooge's model $\rightarrow$

$$\frac{S_{I_d}}{I_d^2} = \frac{q\alpha_H < \mu_{eff} > V_d}{fL^2 I_d} \tag{3.4}$$

Unified model $\rightarrow$

$$\frac{S_{I_d}}{I_d^2} = (1 + \alpha_{sc}\mu_{eff} C_{ox} I_d / g_m)^2 (\frac{g_m}{I_d})^2 S_{Vfb} \tag{3.5}$$

$$\text{with, } S_{Vfb} = \frac{q^2 kT\gamma N_t}{WLC_{ox}^2 f^\alpha} \tag{3.6}$$

Here, g_m is the transconductance, S_{Vfb} is the flatband voltage power spectral density, C_{ox} is the oxide capacitance, and the rest of the terms are as mentioned earlier. From (3.4) and (3.5), it could be said that the number fluctuations mechanism is dominant if $S_{I_d} / I_d^2 \propto (g_m / I_d)^2$ while $S_{I_d} / I_d^2 \propto 1/I_d$ holds well if bulk-mobility fluctuations (Hooge's Model) were to be the main cause.

Figure 3.2 gives a plot of S_{Id}/I_d^2 vs. I_d and $(g_m/I_d)^2$ vs. I_d on primary and secondary axes, respectively, for NMOS devices with Al_2O_3/HfO_2 dielectric stack. It could be readily seen that S_{Id}/I_d^2 follows the same trend as $(g_m/I_d)^2$,implying number fluctuations to be the principal cause of noise. If S_{Id}/I_d^2 were to follow as $1/I_d$, bulk mobility fluctuations would have been the primary cause, which is clearly not the case here. Additionally, according to the bulk-mobility fluctuation model α_H needs to be a constant (~$2\text{x}10^{-3}$) for a given process [71]. When (3.2) was applied to our measured data, α_H was found to vary with gate voltage. Table 3.1 shows the average α_H values extracted at individual bias points in the voltage range considered. For most of the devices, α_H was found to be higher than $2\text{x}10^{-3}$. The refinement suggested in [64],

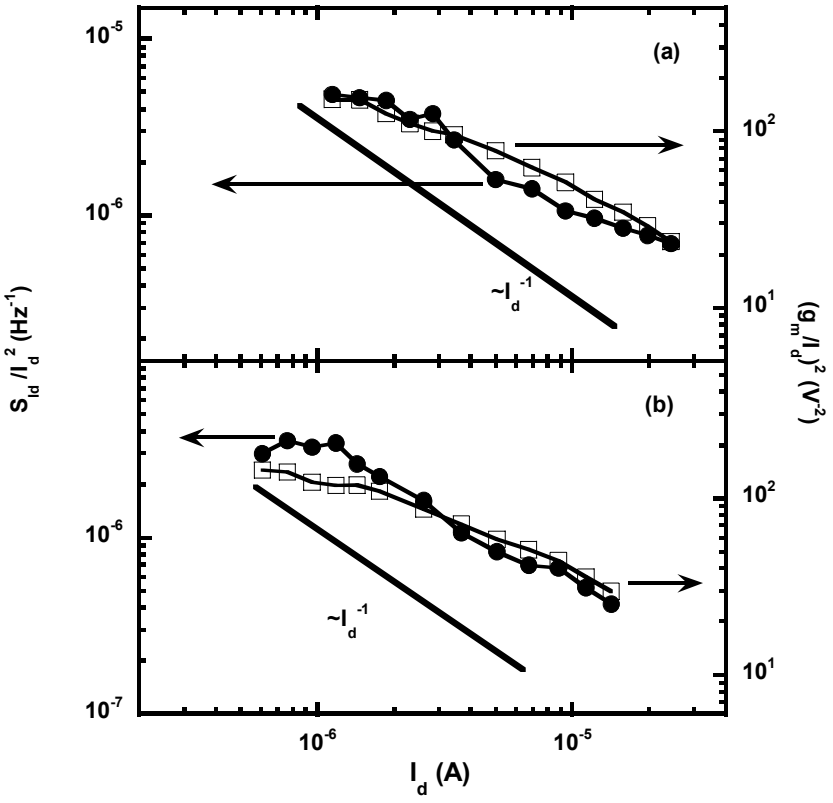

Figure 3.2 The trends for S_{Id}/I_d^2 and $(g_m/I_d)^2$ plotted against drain current in the log-log scale are the same. Thus, Unified Model can better explain the observed noise. The solid reference line is drawn to check for the $1/I_d$ dependence predicted by Hooge's Model. Here (a) Al_2O_3/HfO_2 NSGO and (b) Al_2O_3/HfO_2 PSGO.

based on the dominant scattering mechanisms, only yielded lower values than $2x10^{-3}$. However, it was implied as well that higher α_H values can be obtained in case of irradiation or stress damaged crystals [64]. Since that is not the case here, bulk mobility fluctuations were not pursued as a possible cause for the observed noise. Therefore, the trapping/de-trapping of channel carriers is established to be the noise causing mechanism and accordingly, the Unified Noise Model is used for further analysis.

Table3.1 Summary of devices and extracted parameters. *Reference device data for NMOS [72] and PMOS [73].

Gate Material	Device Parameters	NSGO (NMOS)	PSGO (PMOS)	NDGO (NMOS)	PDGO (PMOS)
HfO_2/Al_2O_3	W (μm)	10.02	10.02	10.02	10.02
	L (μm)	0.18	0.165	0.36, 0.3	0.36
	EOT (nm)	3.3	3.3	6.3	6.3
	C_{EOT} (Fcm^{-2})	1.05×10^{-6}	1.05×10^{-6}	5.48×10^{-7}	5.48×10^{-7}
	V_t (V)	0.59	-0.80, -0.81	0.98, 1.02	-0.86
	μ_{eff} (cm^2/ Vs)	44	24	72	45
	α_H	1.00×10^{-2}	6.56×10^{-3}	2.38×10^{-4}	3.03×10^{-4}
	μ_{c0} ($cm\ V^{-1}\ s^{-1}$)	2.8×10^{7}	3.3×10^{7}	2.9×10^{7}	3.1×10^{7}
	N_t ($cm^{-3}\ eV^{-1}$)	1.05×10^{19}	8.08×10^{18}	8.94×10^{17}	1.80×10^{17}
	N_f (cm^{-2})	-3.69×10^{12}	5.45×10^{12}	-2.99×10^{12}	2.61×10^{12}
HfO_2	W (μm)	10.02	10.02	10.02	10.02
	L (μm)	0.18, 0.165	0.165, 0.135	0.3	0.36
	EOT (nm)	2.3	2.3	5.3	5.3
	C_{EOT} (Fcm^{-2})	1.50×10^{-6}	1.50×10^{-6}	6.51×10^{-7}	6.51×10^{-7}
	V_t (V)	0.28, 0.28	-1.12, -1.02	0.27	-1.12
	μ_{eff} (cm^2/ Vs)	131	33	326	
	α_H	1.55×10^{-3}	6.89×10^{-3}	9.89×10^{-4}	

Table 3.2 - *CONTINUED.*

	μ_{c0} (cm V^{-1} s^{-1})	1.5×10^{8}	5.0×10^{7}	3.0×10^{8}	
	N_t (cm^{-3} eV^{-1})	1.41x10^{18}	9.95x10^{18}	6.10x10^{17}	
	N_f (cm^{-2})	-2.74×10^{12}	1.03E×10^{13}	-7.06×10^{11}	
$HfAlO_x$	W (μm)	10.02	10.02	10.02	10.02
	L (μm)	0.18, 0.18	0.18, 0.165	0.36	0.36, 0.3
	EOT (nm)	2.85	2.85	5.85	5.85
	C_{EOT}(Fcm^{-2})	1.21×10^{-6}	1.21×10^{-6}	5.90×10^{-7}	5.90×10^{-7}
	V_t(V)	0.75, 0.74	-0.43, -0.52	0.96	-0.75, -0.77
	μ_{eff} (cm^2/ Vs)	39	25	86	50
	α_H	3.21×10^{-3}	4.03×10^{-3}	2.80×10^{-3}	2.86×10^{-4}
	μ_{c0} (cm V^{-1} s^{-1})	2.5×10^{7}	9.0×10^{7}	3.8×10^{7}	3.5×10^{7}
	N_t (cm^{-3} eV^{-1})	3.58x10^{18}	1.25x10^{19}	9.94x10^{17}	1.93x10^{17}
	N_f (cm^{-2})	-5.60×10^{12}	4.22×10^{12}	-3.07×10^{12}	2.54×10^{12}
SiO_2^*	W (μm)	5	5		
	L (μm)	0.23	0.32		
	EOT (nm)	4	4		
	C_{EOT}(Fcm^{-2})	8.63×10^{-7}	8.63×10^{-7}		
	V_t(V)	0.45	-0.61		
	μ_{eff} (cm^2/ Vs)	257	95		
	N_t (cm^{-3} eV^{-1})	2.5×10^{16}	4.13×10^{16}		

3.4 Discussion on Noise in High-k MOSFETs

After identifying correlated carrier number and mobility fluctuations as the physical mechanism responsible for noise, normalization of current noise power spectral density was done to assure valid comparison of inherent noise in devices with different physical dimensions and resulting currents. To achieve this, the current noise power spectral density was at first divided by I_d^2 to obtain the noise spectral density in Hz^{-1}. According to number fluctuations theory, the noise power is inversely proportional to MOSFET channel area and the square of gate oxide capacitance [65,74]. Hence, for MOSFETs with same widths, S_{I_d} / I_d^2 was multiplied by L and $C_{EOT}{}^2$ to obtain the device inherent noise. Figure 3.3 shows the relative comparison of normalized current noise spectral density vs. gate overdrive, at a constant drain voltage of ±40 mV or ±50 mV, for devices with the same interfacial layer thickness and different dielectric materials. Plotting against gate overdrive instead of gate voltage ensured that same surface potential conditions were considered for the devices with different threshold voltages. In the case of NMOS devices, HfO_2 MOSFETs exhibited the lowest noise overall when compared to devices with other dielectrics. No such generalization can be made in PMOS devices as the noise levels are close to each other in the strong inversion region. However, $HfAlO_x$ devices showed the lowest noise in the sub-threshold region. Considering the limited data reported here for the sub-threshold region, it is interesting to note that the normalized noise decreased for high-k MOSFETs biased below the threshold voltage instead of holding steady at a constant value. Further

investigation needs to be conducted in the subthreshold region. It must be mentioned in the passing that the parameter extraction and data analysis was limited to the strong inversion region of operation at low drain voltages. Normalized S_{Id} vs. V_d is plotted in Figure 3.4 for MOSFETs biased at a constant gate overdrive of 0.1 V with drain voltage varying from 20 mV to 0.1 V. As can be observed, the normalized noise in the linear operation region did not show any change with drain bias implying an Ohmic noise source coming from the channel. It should be noted that for the gate bias values employed here, there is negligible noise contribution from the drain and source series resistance [70].

In Fig. 3.5 a comparison of normalized current noise spectral density is made for MOSFETs with the same high-k material. Within each type of gate stack, DGO devices exhibited lower noise magnitude than the SGO devices. This is a significant result due to the fact that the channel carriers tunneling to about 3 nm into the gate dielectric cause noise in the low frequency region. In DGO devices, the SiO_2 interfacial layer thickness is 4 nm. This would mean that the observed noise is mainly coming from the interfacial layer and not the high-k material. For SGO MOSFETs, the tunneling carriers reach the traps in the high-k dielectric and the fact that the noise level is higher in SGO devices points to a higher level of defect states in the high-k layer. This was confirmed from the trap density extracted using the Unified model and will be discussed later.

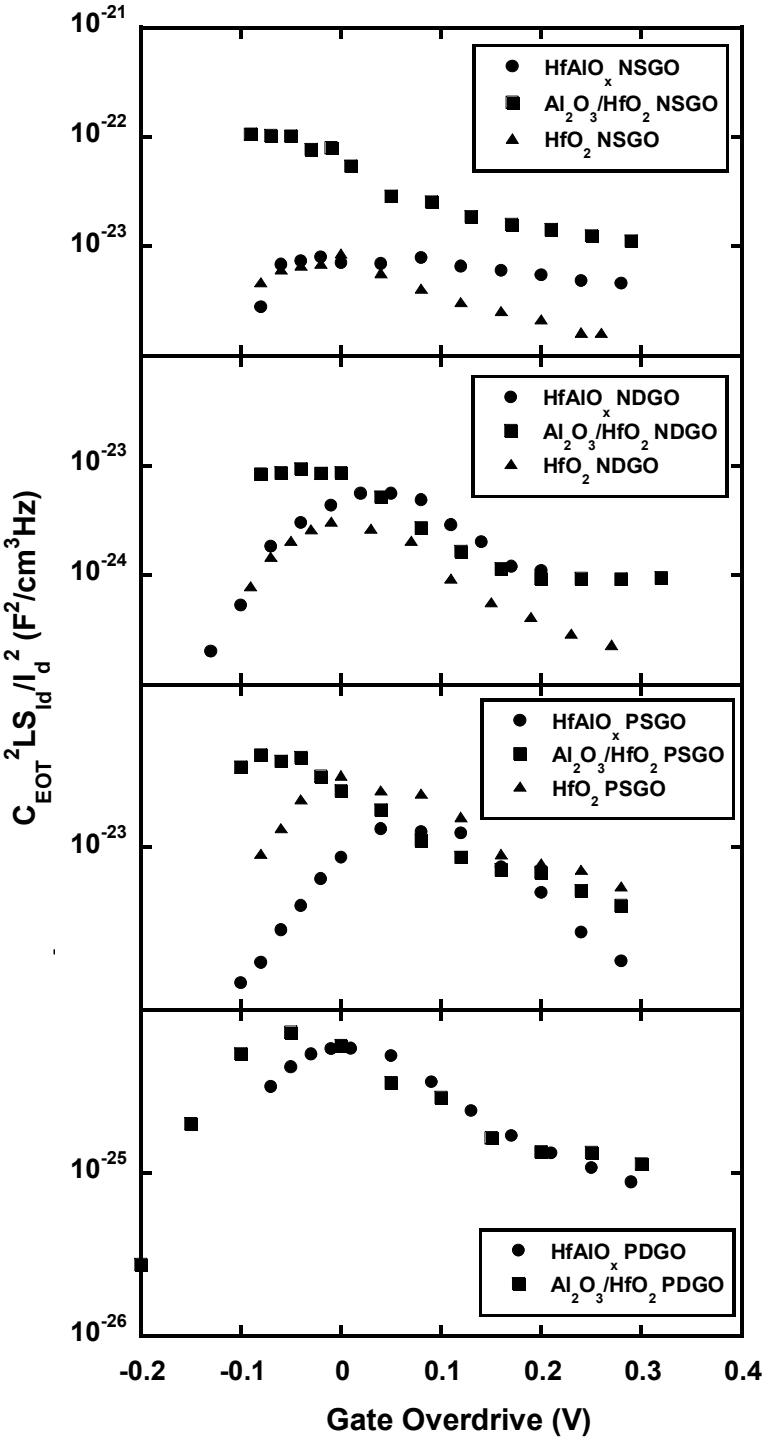

Figure 3.3 Comparison of normalized noise spectral density among different gate stack devices with the same interfacial oxide thickness. ▼ HfO_2, ● $HfAlO_x$, ■ Al_2O_3/ HfO_2. V_d = ±40/±50 mV.

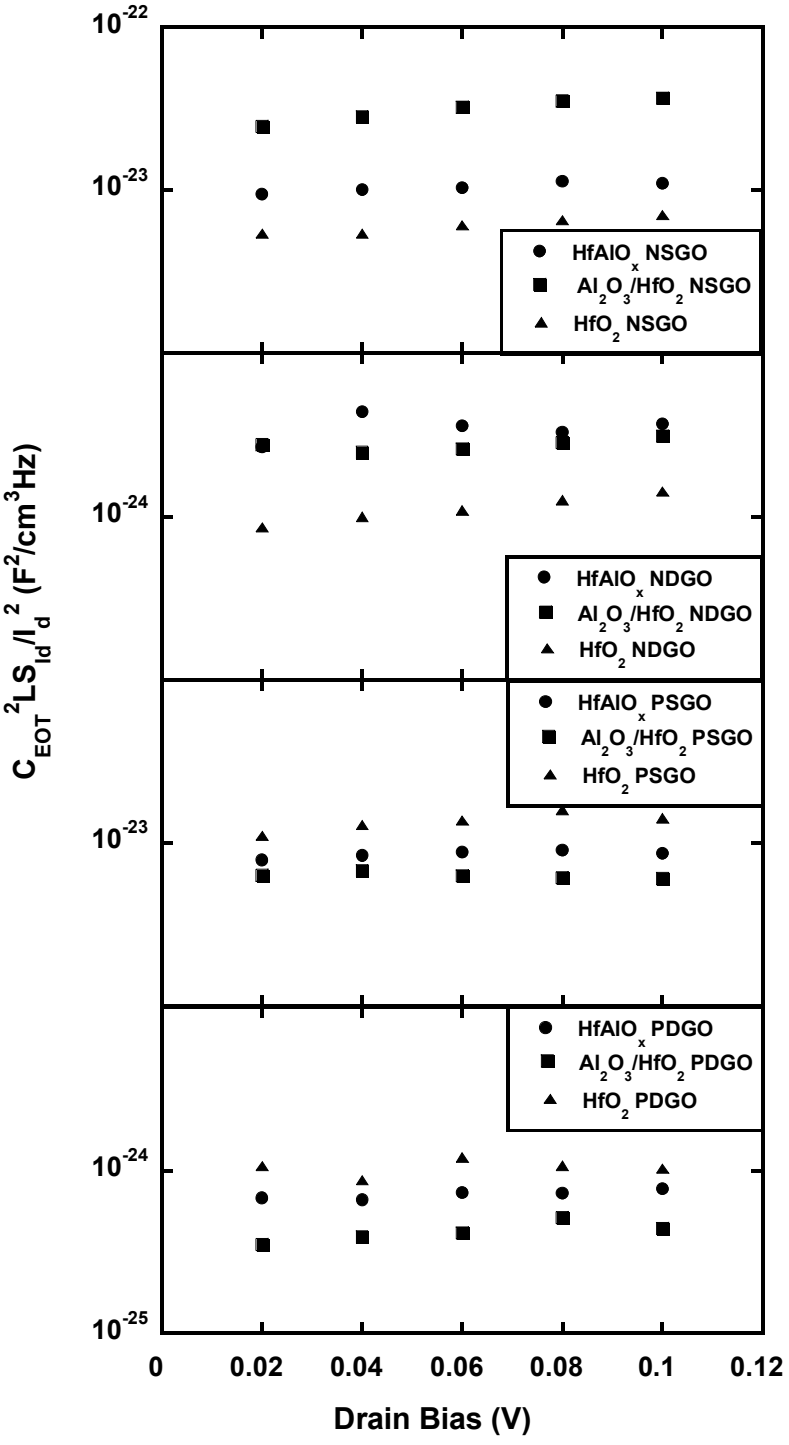

Figure 3.4. Comparison of normalized S_{Id} plotted as a function V_d. Symbols ▼,● and ■ represent HfO_2, $HfAlO_x$ and Al_2O_3/HfO_2, respectively. A gate overdrive of 0.1 V was used.

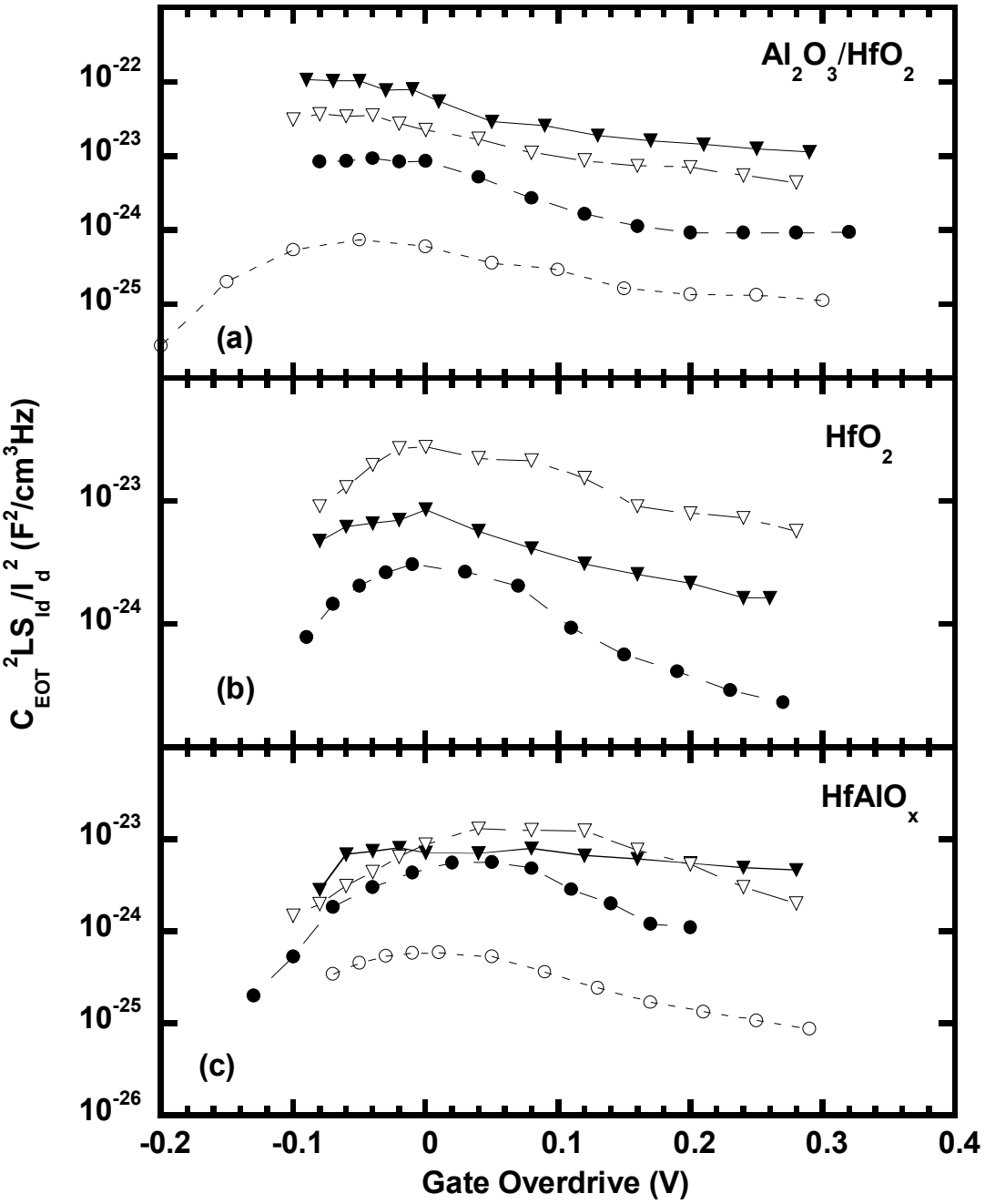

Figure 3.5 Comparison of normalized noise spectral density for SGO and DGO MOSFETs with Al_2O_3/ HfO_2, HfO_2, and $HfAlO_x$. Symbols ▼,∇, ●, and ○ represent NSGO, PSGO, NDGO and PDGO, respectively. Lines are guide to the eye.

In general, the n-type MOSFETs with Al_2O_3/HfO_2 dielectric stack showed higher noise level compared to their p-type counterparts. In HfO_2 devices however, PSGO noise was higher than that of NSGO. For $HfAlO_x$ devices there was no clear trend. The NSGO and PSGO had similar noise magnitude while NDGO noise was higher than PDGO noise. Additionally, the NDGO noise was close to that of NSGO for $HfAlO_x$ MOSFETs.

For strong inversion region and small drain voltages, the Unified noise model can be given by,

$$S_{I_d}(f) = \frac{kTI_d^{\ 2}}{\gamma fWL}\left(\frac{1}{N} \pm \alpha_{sc}\mu_{eff}\right)^2 N_t \tag{3.7}$$

where, the terms have been previously defined. The Coulomb scattering coefficient (α_{sc}) in the above expression must essentially be calculated from the physical properties of the MOSFET such as substrate doping concentration, gate-oxide thickness, gate bias and physical constants [15,75]. However, it is a fitting parameter in the original Unified model with a logarithmic dependence on the inversion layer charge and taking the form: $\alpha_{sc} = \alpha_0 + \alpha_1 \ln(N)$ where, α_0 and α_1 are empirical constants. Later observations by Koga et al. [76,77] implied a dependence of the form, $\alpha_{sc} = \frac{1}{\mu_{c0}\sqrt{N}}$ that was found to hold well for n-type MOSFETs [78]. Additionally, a positive sign was adopted for the mobility term assuming the presence of repulsive trap centers and was found to hold well for both NMOS and PMOS devices, irrespective of the dielectric. Therefore we have,

$$S_{I_d} = \frac{kTI_d^{\ 2}}{\gamma f WL}\left(\frac{1}{N} + \frac{\mu_{eff}}{\mu_{c0}\sqrt{N}}\right)^2 N_t \tag{3.8}$$

Here, N_t and μ_{c0} are the fitting parameters. The tunneling coefficient was re-calculated for high-k gate stacks using the WKB (Wentzel-Kramer-Brillouin) approximation as [66]:

$$\gamma = \frac{4\pi}{h}\sqrt{2m^*\Phi} \tag{3.9}$$

where m^* is the electron effective mass in the dielectric, h is the Planck's constant and Φ is the barrier height. The barrier height values were 1.13 eV for HfO_2 [32] and 2.8 eV for Al_2O_3 [79]. The effective mass values for electrons in HfO_2 and Al_2O_3 were taken as $0.18m_0$ and $0.28m_0$, respectively [80]. The tunneling coefficients thus obtained were 0.476×10^8 cm^{-1} for HfO_2 and $0.908x10^8$ cm^{-1} for Al_2O_3. It should be noted that Al_2O_3 is a capping layer for HfO_2 so that the tunneling coefficient for this particular gate stack would still be 0.476×10^8 cm^{-1}. Due to its mixed composition, a value of 0.692×10^8 cm^{-1} was deemed reasonable for $HfAlO_x$. In the case of DGO MOSFETs, the tunneling coefficient value of SiO_2 ($1x10^8$ cm^{-1}) holds well since the noise contribution in the frequency range of interest comes only from this layer as indicated earlier. On a related note, in [32,79,80], the barrier height and carrier effective mass were extracted from data on gate tunneling current. The tunneling current data used here, were obtained on MOSFETs with HfO_2 or Al_2O_3 and ~ 6-10 nm thick interfacial layers. Since the interfacial layer was present in these devices, the absolute barrier height/carrier effective mass values that are specific to high-k dielectrics could be marginally different.

Figure 3.6 shows current noise power spectral density as a function of gate overdrive. The solid lines were obtained by choosing appropriate values for the two fitting parameters N_t and μ_{c0} in (3.8) and Table 3.1 lists these noise parameters for different gate dielectric MOSFETs. The overall effective trap density in SGO devices was found to be at least an order of magnitude higher than DGO devices. This was expected since the channel carriers tunnel back and forth from the traps lying within ~3 nm of the gate dielectric to cause 1/f noise. This would imply that the noise contribution in DGO devices is from the traps in the thick SiO_2 layer that is relatively defect-free. And in SGO devices, the observed noise is mainly from the higher number of traps lying in the high-k layer. Additionally, the Coulomb scattering arising from these traps in SGO devices would cause severe degradation in carrier mobility. This is confirmed by the lower effective mobility values (averaged in the strong inversion region) listed in Table 3.1 for SGO MOSFETs when compared to DGO devices. Thus, Coulomb scattering is a dominant mechanism for mobility degradation in high-k MOSFETs. It should be noted that the effective mobility in this part of the work was calculated from the transconductance relationship as $\mu_{eff} = g_m L / W C_{EOT} V_d$.

In general, μ_{c0} was found to be ~$3x10^7$ cm/Vs for HfO_2/Al_2O_3 and $HfAlO_x$ devices (except PSGO with $9x10^7$) and $5x10^7$-$3x10^8$ cm/Vs for HfO_2 MOSFETs. For conventional SiO_2 MOSFETs, a value of ~$6x10^8$ cm/Vs was reported [78]. The fact that μ_{c0} was found to be lower in high-k MOSFETs implies that the degradation in carrier mobility due to screened Coulomb scattering would be prominent in these devices when compared to conventional SiO_2 MOSFETs, which is consistent with low mobility

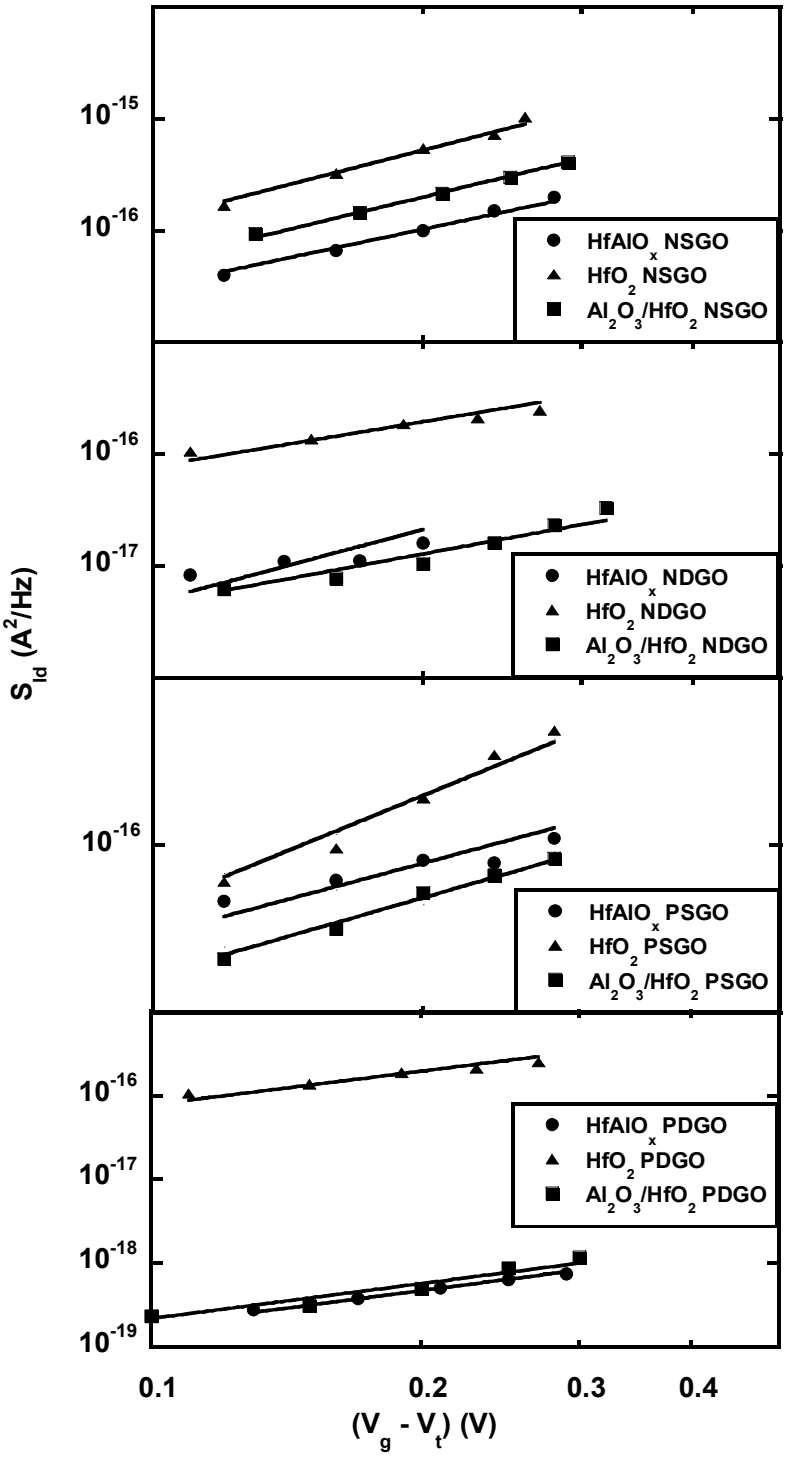

Figure 3.6 Good fit to the data was obtained (solid lines) by using appropriate μ_{c0} and N_t values in the Unified Noise Model expressions.

values observed in high-k devices. In addition, the DGO trap density is marginally higher than conventional SiO_2 defect density as quoted in Table 3.1. This would imply a lower mobility for DGO devices. Further, the low effective mobility found in DGO devices compared to conventional SiO_2 MOSFETs might be partly explained by the soft optical phonon scattering mechanism that has been reported to degrade mobility in high-k MOSFETs [7,81].

3.5 Interface of High-k with Poly-Si Gate

In addition to the higher trap densities in high-k MOSFETs, the observed threshold voltages in both SGO and DGO devices indicated larger threshold shifts when compared to their SiO_2 counterparts. Assuming that this shift is caused by the formation of fixed charges at the interface, the fixed charge density was calculated from the expression for threshold voltage given as,

$$V_t = V_{FB}^0 - \frac{qN_f}{C_{EOT}} \pm 2|\phi_F| \pm \frac{\sqrt{4q\varepsilon_{Si}N_I|\phi_F|}}{C_{EOT}} \tag{3.10}$$

where V_t is the threshold voltage (V), V_{FB}^0 is the difference in work functions of gate material and the Si substrate (V), N_f is the fixed charge density in cm^{-2}, C_{EOT} is the oxide capacitance (Fcm^{-2}), ϕ_F is the bulk potential (V), N_I is the substrate doping concentration (cm^{-3}), and ε_{Si} is the permittivity of Si (Fcm^{-1}). The substrate type, n or p, determines the positive or negative sign in front of the last two terms on right hand side of (3.9).

From Table 3.1, NMOS devices with n-type poly-Si gate showed negative fixed charges (positive threshold shift) while PMOS devices with p-type poly-Si showed positive fixed charges (negative shift). This cannot be attributed to the dopant diffusion during the poly-Si gate formation, as opposite signs for fixed charges would be observed if that were to be the case. Furthermore, in NMOS and PMOS alike, both SGO and DGO devices yielded the same sign despite the difference in interfacial layer thickness. Thus, the threshold shift is not a consequence of fixed charge density at the interface.

It was recently reported [82] that irrespective of the substrate type, MOSFETs with HfO_2 gate dielectric and n-type poly-Si gate showed a positive flat band voltage shift (corresponding to negative fixed charges) and those with p-type poly-Si showed a negative shift in flat band voltage (corresponding to positive fixed charges), owing to the interface states between HfO_2 and the poly-Si gate. Thus, in the current case, it can be concluded that acceptor or donor type states are formed at the interface with HfO_2, Al_2O_3, $HfAlO_x$ and the poly-Si gate that resulted in the threshold shift. More recently, the threshold shift was attributed to Fermi-level pinning occurring at poly-Si/ high-k interface due to Si-Hf interfacial bonds and/or oxygen vacancies in the case of HfO_2 and Si-O-Al bonds in Al_2O_3 [17,18].

$N_f \approx \pm 2 - 5x10^{12}$ cm^{-2} for all devices, except for HfO_2 PMOS, which had $N_f \approx 10^{13}$ cm^{-2}. Although the level of charge observed in this work seems to be consistent with other results on high-k films [83,84,85,86,87,88,89], it must be noted

that (3.10) was only used to indicate the presence of interface states at the poly-Si/ high-k interface and as such is a crude method for calculating the fixed charges. On a side note, it can be seen that the threshold voltage is about the same for HfO_2 SGO and DGO MOSFETs, despite the different oxide capacitances. This might be attributed to the reverse short channel effects (RSCE) owing to the size of SGO (0.165 μm) and DGO (0.36 μm) devices.

3.6 Summary

The 1/f noise characteristics of poly-Si gated n and p-type MOSFETs with HfO_2, HfO_2/Al_2O_3, $HfAlO_x$ gate stacks were studied. The correlated carrier number-mobility fluctuations mechanism was identified as the underlying cause of noise. The normalized noise and extracted overall effective dielectric trap density using Unified model were found to be higher in high-k devices compared to conventional SiO_2 MOSFETs. The Coulomb scattering mechanism was found to be more pronounced in these devices resulting in severe mobility degradation of channel carriers. Better overall performance was exhibited by HfO_2 devices in NMOS while there was no marked winner in PMOS. Finally, the interface states at the poly-Si gate and high-k interface were suggested to be the cause for higher threshold voltages observed.

CHAPTER 4

1/f NOISE IN METAL GATED MOSFETs WITH HfO_2 AS GATE DIELECTRIC

4.1 Introduction

The interface states at the poly-Si/high-k interface were previously shown to adversely affect the threshold voltage. Additionally, there are inherent problems with poly-Si gate electrode such as dopant diffusion during gate formation, high processing temperatures required for dopant activation, and gate depletion effects. This evokes interest in metal gate electrodes as they minimize/eliminate such problems. Specifically, dual metal gates are being considered so as to obtain suitable threshold voltages for CMOS applications. Recently, promising results were reported as regards to the integration of TaSiN and TiN gates on HfO_2 into CMOS and their influence on device characteristics [20,90,91,92,93,94,95,96]. This chapter deals with the low frequency noise characteristics of MOSFETs with HfO_2 (made by atomic layer deposition, ALD) gate dielectric and dual metal gates - TiN for PMOS, and TaSiN for NMOS. Further, the effects of processing method employed for interfacial layer formation on the various MOSFET performance parameters are studied. For this, n-type MOSFETs were considered that had these interfacial layers - thermal SiO_2 by Stress Relieved Pre-Oxide

(SRPO) pretreatment or chemical SiO_2 resulting from standard RCA (Radio Corporation of America) clean process.

4.2 TaSiN Metal Gate for N-Type MOSFETs

The n-type MOSFETs used here had TaSiN metal as gate electrode (work function ~ 4.4 eV). Devices from three process splits were considered for this work. Splits 1 and 2 had 2.7 nm thick HfO_2 (k~17) as the high-k layer on top of 0.6 nm and 1 nm thermal SiO_2, respectively. The thermal SiO_2, that is the interfacial layer here, was formed by a novel Stress Relieved Pre-Oxide treatment method (SRPO) wherein a 7 nm thick thermal SiO_2 is initially grown at a high temperature (greater than glass flow temperature) for stress relief and is etched back to desired final thickness (0.6 nm or 1 nm) [97]. Split 3 had a 1 nm thick chemical SiO_2 interfacial layer resulting from a standard RCA surface pre-clean process. The reference poly-Si gated device (as described in Chapter 3) had 5.5 nm of HfO_2 deposited by metal organic chemical vapor deposition (MOCVD) with a ~1 nm chemical SiO_2 interfacial layer. All SiO_2 thicknesses are targeted values. The devices considered for noise measurements were 10 μm wide with mask lengths of 0.15 μm, 0.165 μm and/or 0.18 μm. Due to etch-caused trimming of the gate, a length correction of 0.07 μm was made wherever applicable. It should be noted that in this part of the work, on-wafer measurements were made in an enclosed low noise 8600 series MicroManipulator probe station.

Following the procedure detailed in Chapter 2, conventional split C-V measurements were performed on 10 μm x 10 μm devices to obtain the inversion layer

charge directly from the gate to channel capacitance (C_{gc}) as $Q_{inv} = \int_0^{V_g} C_{gc}\, dV_g$. The effective mobility was extracted using I_d-V_g characteristic at V_d = 10 mV in $\mu_{eff} = I_d L / W Q_{inv} V_d$. The capacitance equivalent thickness (t_{CET}) was calculated using the C_{gc} value at a gate voltage of 1.5 V as $t_{CET} = \varepsilon_{SiO_2} / C_{gc}(V_g = 1.5V)$. Neglecting the quantum mechanical effects, this would be the same as equivalent oxide thickness in the case of metal gate MOSFETs.

A comparison of electron effective mobility vs. inversion layer charge density is depicted in Figure 4.1 for MOSFETs from the three lot splits. In general, devices from

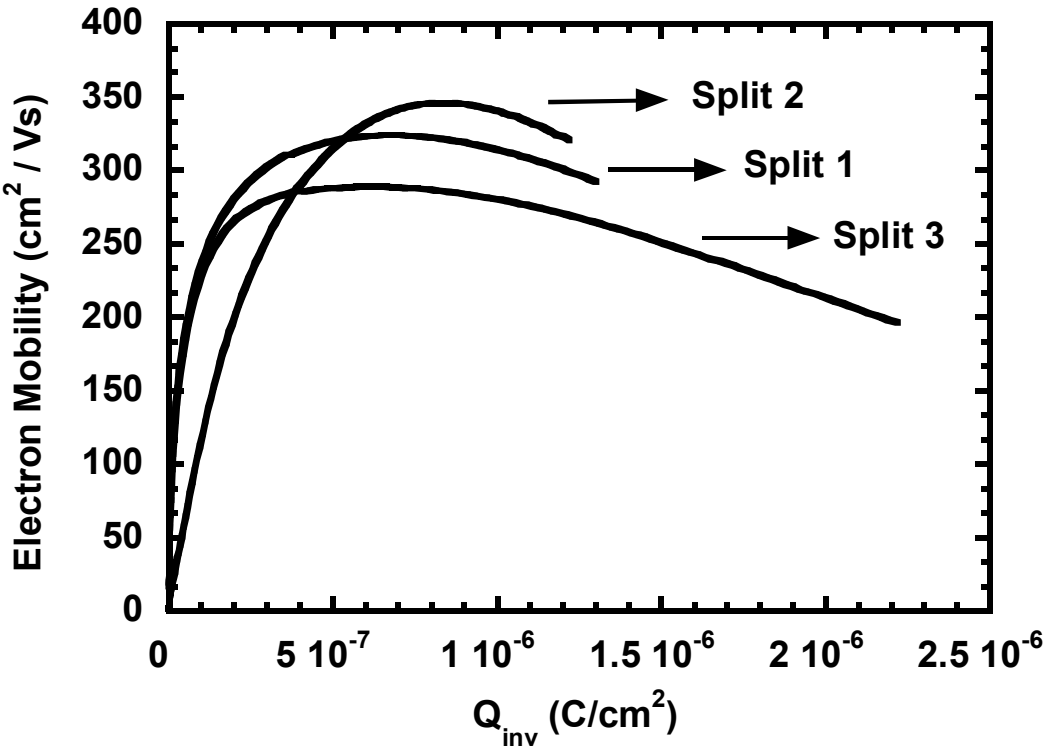

Figure 4.1 Effective electron mobility as a function of inversion layer charge. Generally, SRPO devices exhibited higher mobility compared to RCA devices.

splits 1 and 2 (SRPO devices) exhibited at least 10% higher values compared to the split 3 devices (RCA devices). This could be due to an improved substrate / SiO_2 interface, dielectric quality or some other unidentified mechanism.

Now, the interface trap density can be extracted using the sub-threshold slope as, $D_{it} = \frac{1}{q}\left[(q/2.3SkT)C_{EOT} - C_B\right]$, where $S = \left[\left(\delta(\log(I_d))/\delta V_g\right)\right]$ is the sub-threshold slope, C_B is the Si bulk capacitance at maximum depletion. The D_{it} values for devices from the three process splits were within the range of 7.3-7.8x10^{11} $eV^{-1}cm^{-2}$. Consequently, interface trap density alone cannot account for the difference in electron mobility. It will be shown later that the observed difference in the carrier mobility in RCA and SRPO devices can be partially explained by the level of screening due to the trapped oxide charge that changes the Coulomb scattering effect.

Additionally, the room temperature electron mobility reported here is higher than most found in the literature for poly-Si or metal/HfO_2 counterparts [7,93,94,98,99]. In fact, the peak carrier mobility in SRPO devices is comparable to that of SiO_2 control devices in the aforementioned references. Nonetheless, mobility values given in [100] seem to be the highest reported for HfO_2 nMOSFETs.

The voltage noise power spectral density was measured with the devices biased at V_d = 50 mV and varying the gate overdrive from 0.1 to 0.8 V insteps of 0.1 V. The 1 Hz value of current noise spectral density was used for noise analysis. As previously described, this was deduced from the straight line fit to the drain voltage noise power

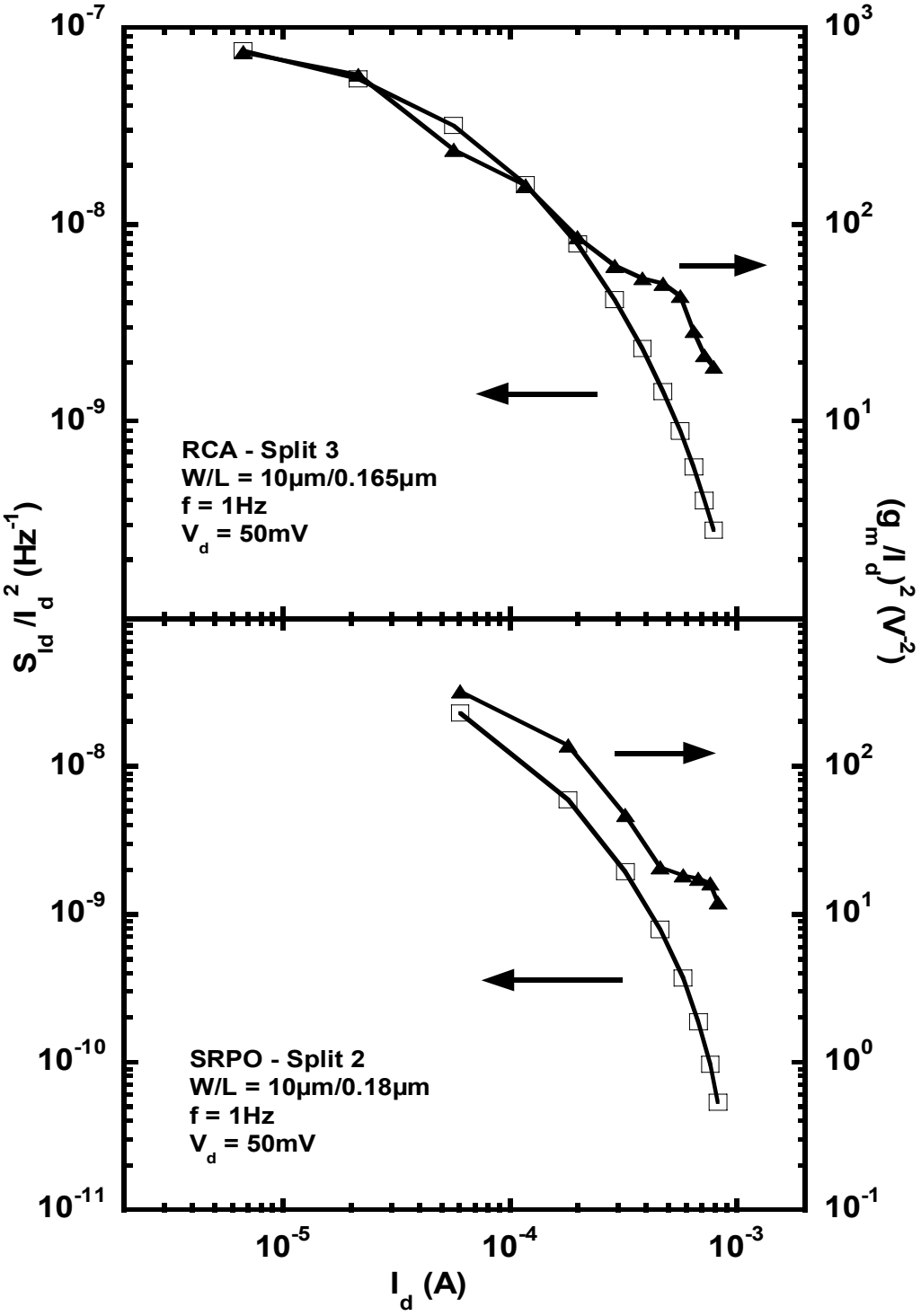

Figure 4.2 S_{Id} and $(g_m/I_d)^2$ follow the same trend implying that number fluctuations is the main noise causing mechanism.

spectral density in the 1-100 Hz range and by using, $S_{I_d} = S_{V_d}.(g_d)^2$.

From Figure 4.2, it can be seen that S_{Id}/I_d^2 and $(g_m/I_d)^2$ follow the same trend in both RCA and SRPO devices, which by general rule [101] indicates that correlated number and mobility fluctuations is the physical mechanism responsible for noise in these meta-gated high-k MOSFETs. Accordingly, the Unified Model is used for further analysis that is given as ,

$$S_{I_d} = \frac{kTI_d^2}{\gamma fWL}\left(\frac{1}{N} + \frac{\mu_{eff}}{\mu_{c0}\sqrt{N}}\right)^2 N_t \qquad (4.1)$$

where, the terms were defined earlier.

Figures 4.3 and 4.4 illustrate a comparison of the inherent noise of RCA, SRPO and poly-Si reference devices after normalization with respect to drain current, equivalent oxide capacitance and channel length (as explained in Chapter 3). Clearly, the noise levels in TaSiN gate devices with either interfacial layer are lower than the poly-Si reference device that is indicative of an improved dielectric quality. Table 4.1 lists the oxide trap density (N_t) and μ_{c0} values extracted using (4.1) and Figure 4.5 depicts typical model fittings to the experimental data. The lower effective trap density obtained for the metal-gated MOSFETs when compared to that of the reference device confirms the improvement in the quality of the dielectric stack. This could be due to many reasons: a better dielectric quality using ALD compared to MOCVD in the deposition of HfO_2, lower thermal budgets required for TaSiN deposition, elimination of dopant diffusion as a source of defect generator and better blocking properties of

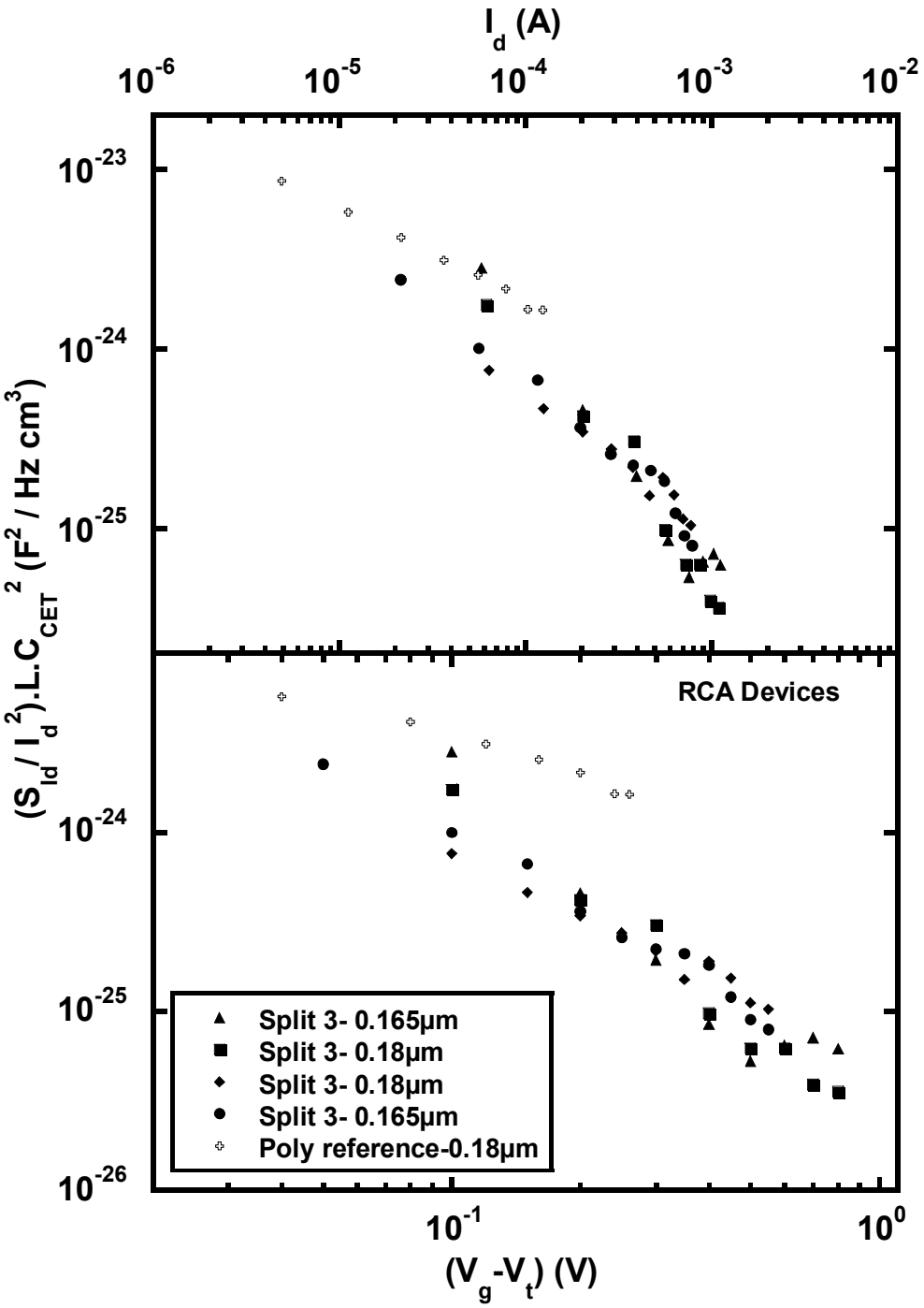

Figure 4.3 Normalized noise spectra for RCA devices as a function of gate overdrive and drain current, in comparison to poly-Si reference device.

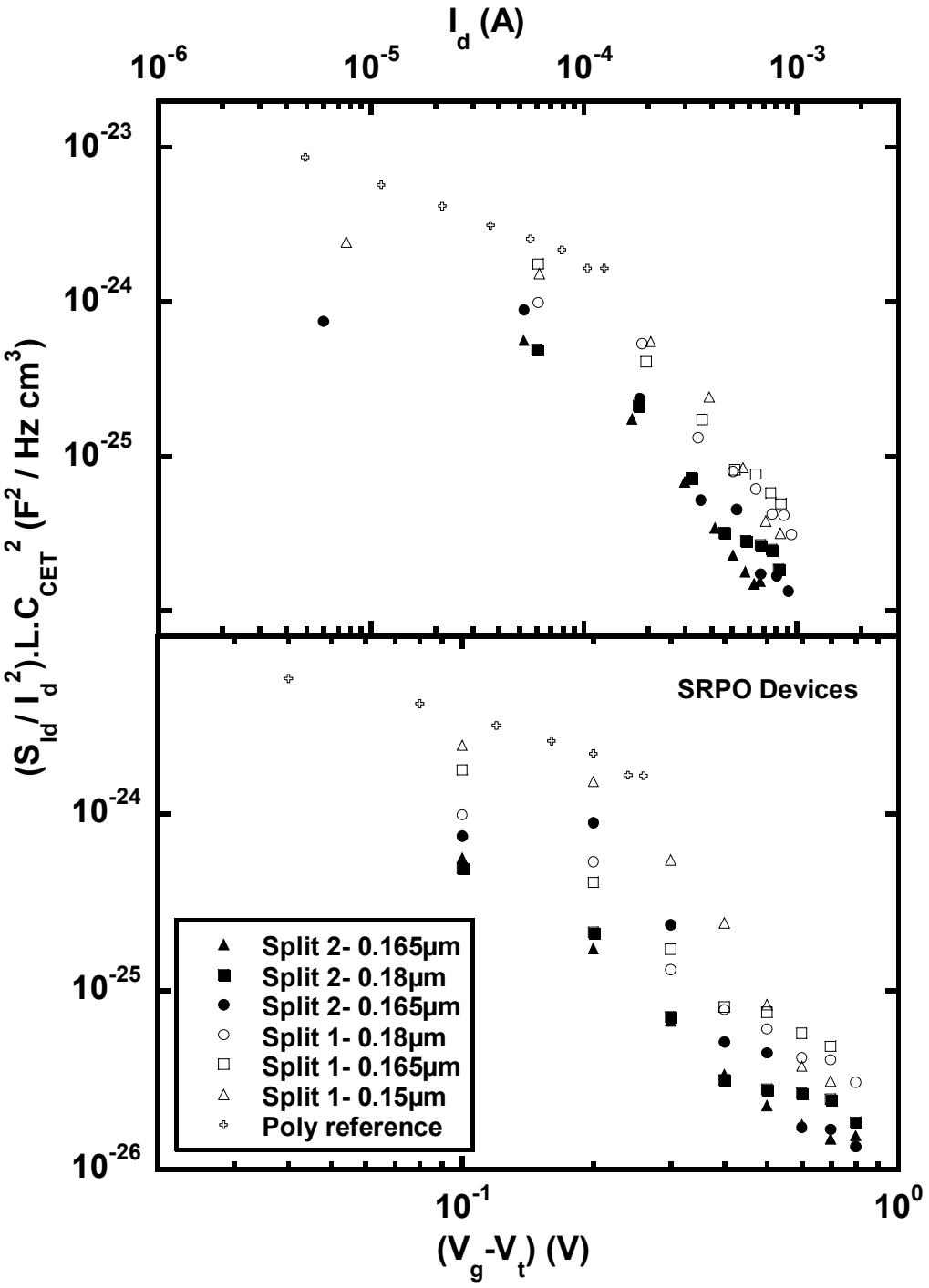

Figure 4.4 Normalized noise power spectral density of SRPO devices for V_d = 50 mV. For all drain currents, the devices with thinner interfacial oxide layer showed slightly higher magnitude. Reference poly-Si device showed highest overall.

Table 4.1 Summary of the gate stacks considered along with the extracted effective trap density and μ_{c0} values. * Poly-Silicon gated device from Chapter 3.

Split no.	High-k	Interfacial layer	L (μm)	N_t ($cm^{-3}eV^{-1}$)	μ_{c0} (cm/Vs)
01	2.7 nm HfO_2 (ALD)	0.6 nm SRPO SiO_2	0.18	2.1×10^{17}	7.0×10^{8}
			0.18	1.6×10^{17}	7.0×10^{8}
			0.15	2.4×10^{17}	9.0×10^{8}
02	2.7 nm HfO_2 (ALD)	1 nm SRPO SiO_2	0.18	1.9×10^{17}	1.0×10^{9}
			0.165	2.2×10^{17}	2.0×10^{9}
			0.165	2.1×10^{17}	1.5×10^{9}
03	2.7 nm HfO_2 (ALD)	1 nm RCA SiO_2	0.18	1.6×10^{17}	4.0×10^{8}
			0.165	3.0×10^{17}	6.0×10^{8}
			0.165	1.9×10^{17}	4.5×10^{8}
			0.18	1.9×10^{17}	4.5×10^{8}
Ref.*	5.5 nm HfO_2 (MOCVD)	1 nm RCA SiO_2	0.18	1.4×10^{18}	1.5×10^{8}

TaSiN gate against oxygen diffusion. Although the poly-Si reference device had MOCVD HfO_2, the role of TaSiN gate in reducing the defect density can be further established by making a comparison with poly-Si/ALD HfO_2 devices. The 1Hz input referred noise values (not shown here) for the devices in this study, as obtained from $S_{V_g} = S_{I_d} / (g_m)^2$, were within the same order as the 10 Hz values reported on poly-Si gated MOSFETs [102,103]. Accounting for the inverse frequency (1/f) dependence of

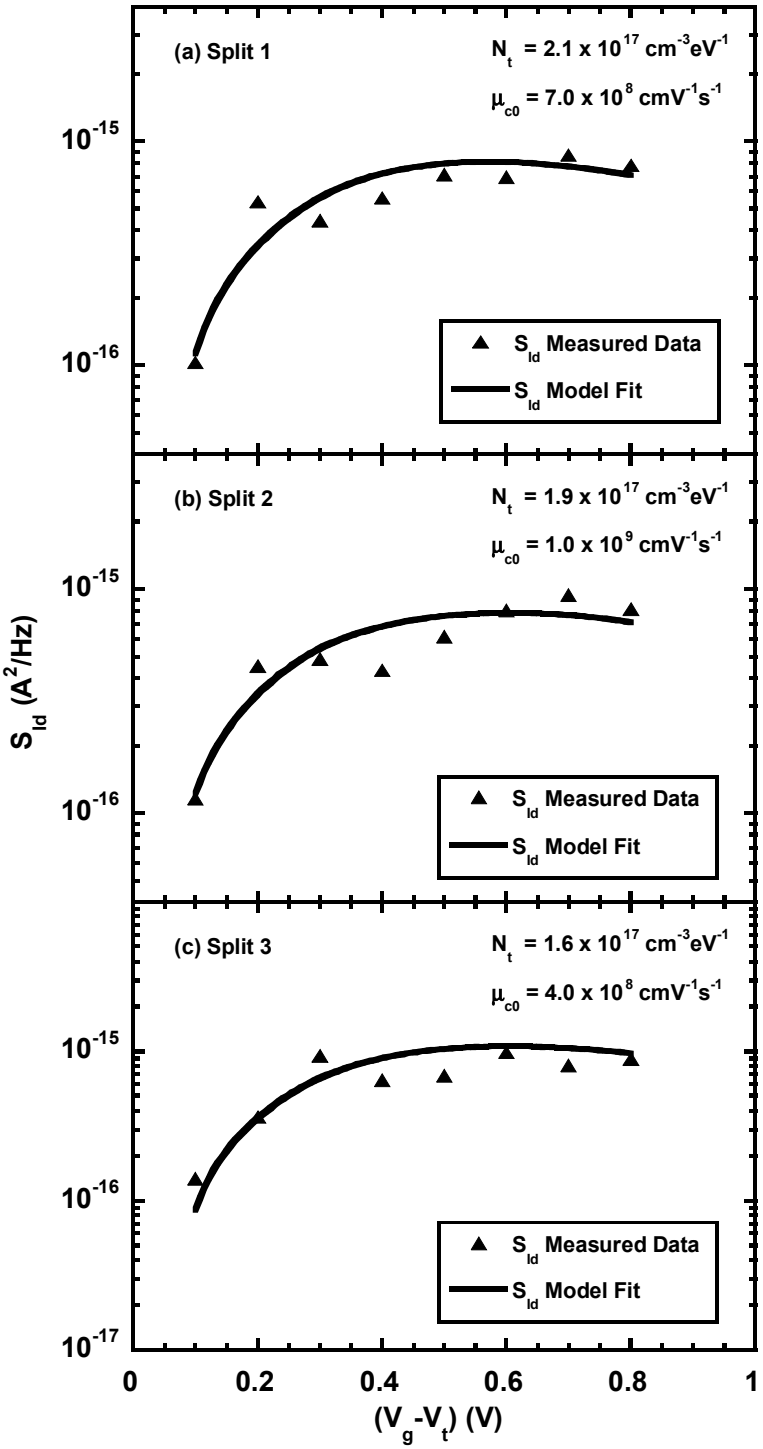

Figure 4.5 Typical model fitting, using N_t and μ_{c0} as the fitting parameters, to the noise data on 0.18μm length devices from (a) Split1 (b) Split 2 and (c) Split 3.

noise, the metal gate devices in fact exhibit an order of magnitude lower noise level, comparatively. This in turn indicates an order of magnitude lower trap density values in MOSFETs considered here. In light of these observations, it can be concluded that gate electrode deposition affects the dielectric quality and therefore noise. More evidence can be found in [104,105] where the metal gate deposition method was shown to affect the trap density in the underlying SiO_2.

In Table 4.1, the extracted dielectric trap density values are similar for metal–gated devices from the three splits. Additionally, SRPO devices had higher μ_{c0} values than RCA devices suggesting lower levels of Coulomb scattering in the former. This is further made evident in Figure 4.6, where the extracted Coulomb scattering coefficient ($\alpha_{sc} = 1/\mu_{c0}\sqrt{N}$) is comparatively lower in SRPO devices. The number fluctuation ($1/N$) and correlated mobility fluctuation components that contribute to the overall noise are plotted in Figure 4.7 for devices with both SRPO and RCA interfacial layers. While the level of contribution from the number fluctuations term is similar in all splits, a noticeable difference in the magnitudes of mobility fluctuations term can be observed. In effect, this indicates that the presence of SRPO SiO_2 offers better screening to the channel carriers from the charged trap sites in the dielectric bulk thereby improving the carrier mobility. The reason for this, however, remains unknown at this time. In addition, the trend observed for the Coulomb scattering coefficient values in Figure 4.6 is in agreement with the observed mobility trend in Figure 4.1. Thus, the difference in effective mobility values can be attributed partly to the Coulomb scattering phenomenon.

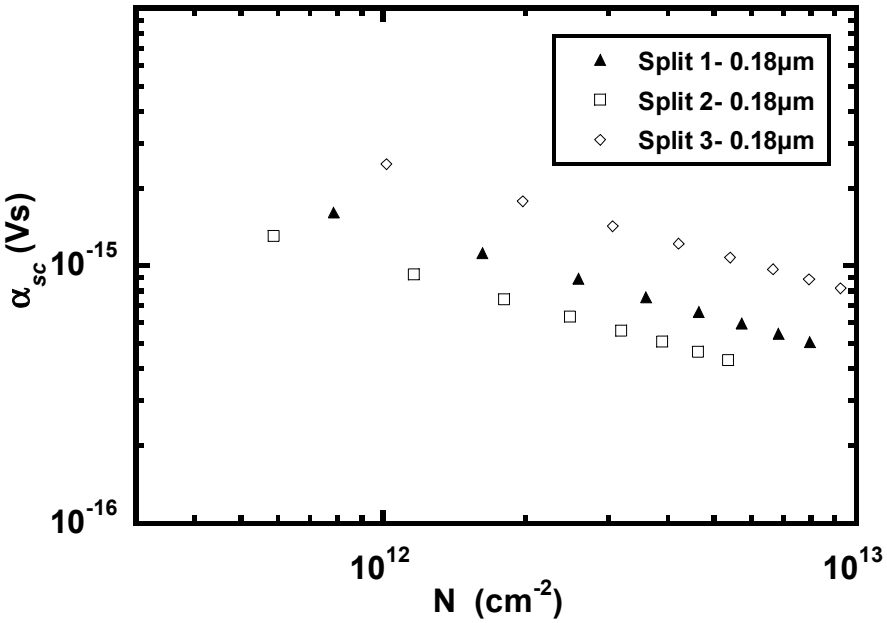

Figure 4.6 Comparison of the extracted Coulomb scattering coefficient (α_{sc}).

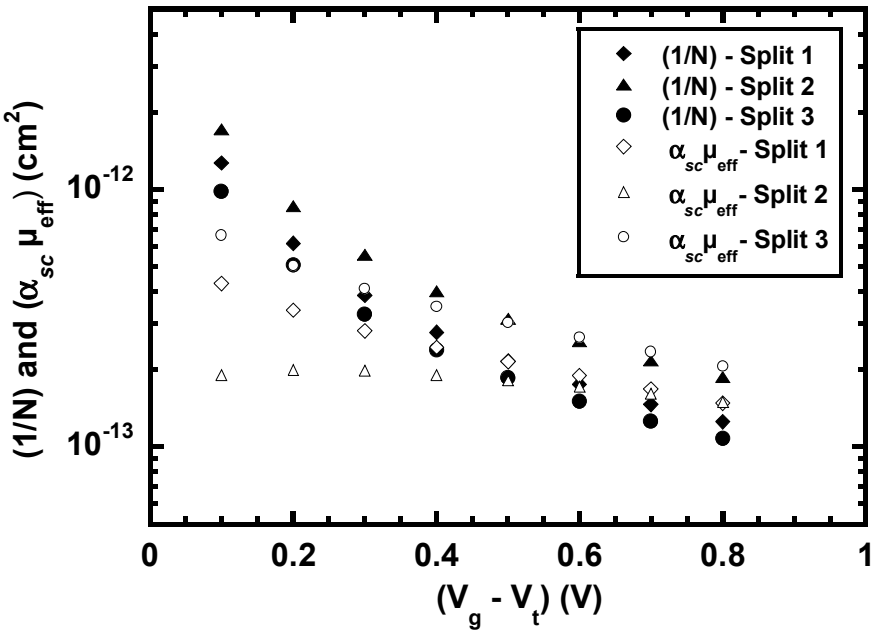

Figure 4.7 The number fluctuations (1/N) and the mobility fluctuations (α_{sc} μ_{eff}) components of noise.

Figure 4.8 shows a compilation of the extracted oxide trap densities in high-k MOSFETs plotted against the interfacial layer thickness [106]. The inset shows the same with respect to the equivalent oxide thickness. Clearly, the trap density values reported for TaSiN/HfO_2 MOSFETs in this study are at the lower end for devices with comparable interfacial layer thickness and EOTs. It should be noted that capacitance equivalent thickness was used in calculations here. The actual EOTs might be 0.2-0.4 nm smaller if quantum mechanical effects were to be considered. Nevertheless, the high-k dielectric trap density, even in metal gated MOSFETs, is still higher than conventional SiO_2.

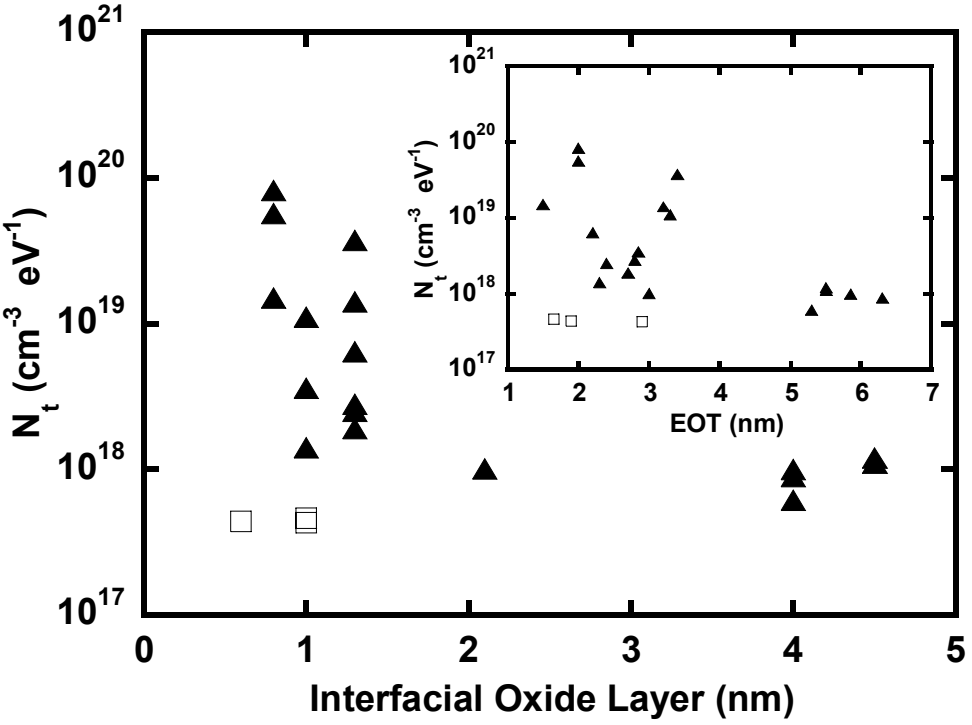

Figure 4.8 The comparison for the extracted overall effective trap density values of metal gate devices under discussion (○) to those reported in literature for comparable high-k stacks (▲) compiled by [106].

4.3 TiN Metal Gate for P-Type MOSFETs

The p-type MOSFETs had TiN metal (work function ~ 4.65 eV) as the gate electrode on top of 2.3 nm HfO_2 (ALD) with 1 nm RCA SiO_2 as the interfacial layer. The information about the reference poly-Si gated MOSFET with HfO_2/RCA SiO_2 can be found in Chapter 3. Following the procedure given in Chapter 2, wafer level DC and noise measurements were performed on 10 μm wide MOSFETs with mask lengths of 0.135 μm, 0.165 μm and 0.18 μm. The hole carrier mobility and inversion layer charge were obtained from the transconductance characteristic as explained in Chapter 2. For noise data, the MOSFETs were biased at V_d = -50 mV while varying the gate overdrive from -0.1 to -0.4 V insteps of -0.05 V.

As in the case of n-type MOSFETs earlier, the validity of number fluctuations theory was established at first and the normalization of noise was done accordingly. Figure 4.9 shows a comparison of the normalized noise of TiN gated MOSFETs and reference poly-Si gate MOSFETs. It can be seen that the noise magnitude is lower for metal gate MOSFETs compared to poly-Si reference devices implying a lower high-k defect density in the former and is confirmed by the N_t values listed in Table 4.2. Thus, it can be generalized that the metal gates are a better choice, than poly-Si gates, for ensuring the quality of underlying high-k dielectric. In addition, the peak hole mobility in the bias range considered was higher in case of TiN MOSFETs comparatively. This is due to the lower dielectric trap density in metal gate MOSFETs compared to reference devices.

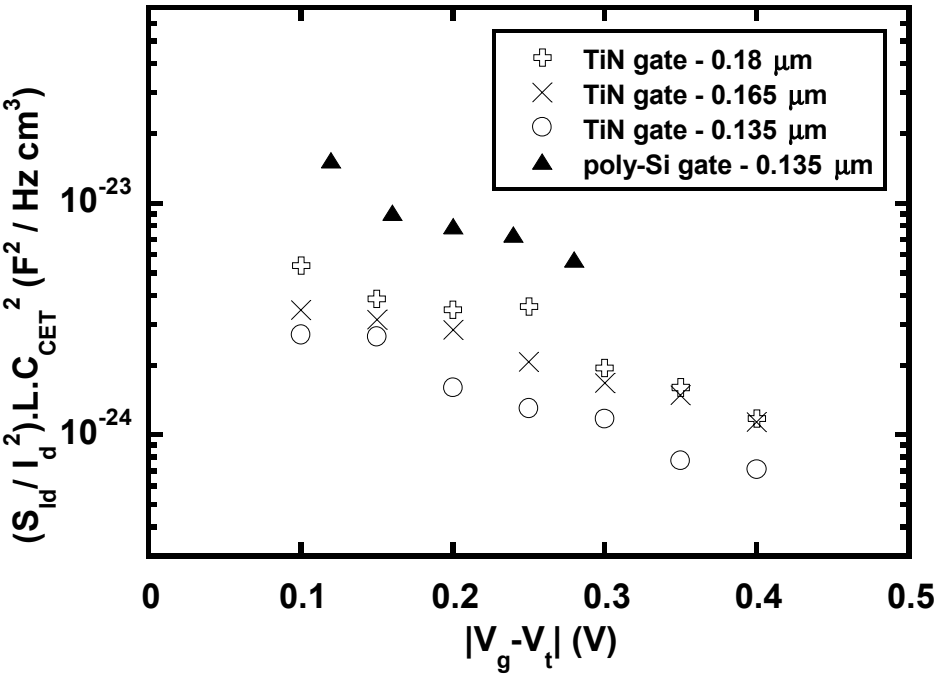

Figure 4.9 Normalized noise level is higher for reference poly-Si MOSFETs compared to TiN gate MOSFETs indicating a better high-k in the latter.

Table 4.2 The extracted noise parameters. * Poly-Silicon gated device from Chapter 3.

Gate	**High-k**	**Interfacial layer**	***L* (μm)**	**N_t ($cm^{-3}eV^{-1}$)**	**μ_{c0} (cm/Vs)**	**μ_{eff} (cm^2/Vs)**
TiN	2.3 nm HfO_2 (ALD)	1 nm RCA SiO_2	0.18	1.6×10^{18}	5.0×10^{7}	72
			0.165	9.0×10^{17}	4.5×10^{7}	82
			0.135	9.5×10^{17}	4.5×10^{7}	58
Poly-Si (p-type)*	5.5 nm HfO_2 (MOCVD)	1 nm RCA SiO_2	0.135	1.0×10^{19}	5.0×10^{7}	33

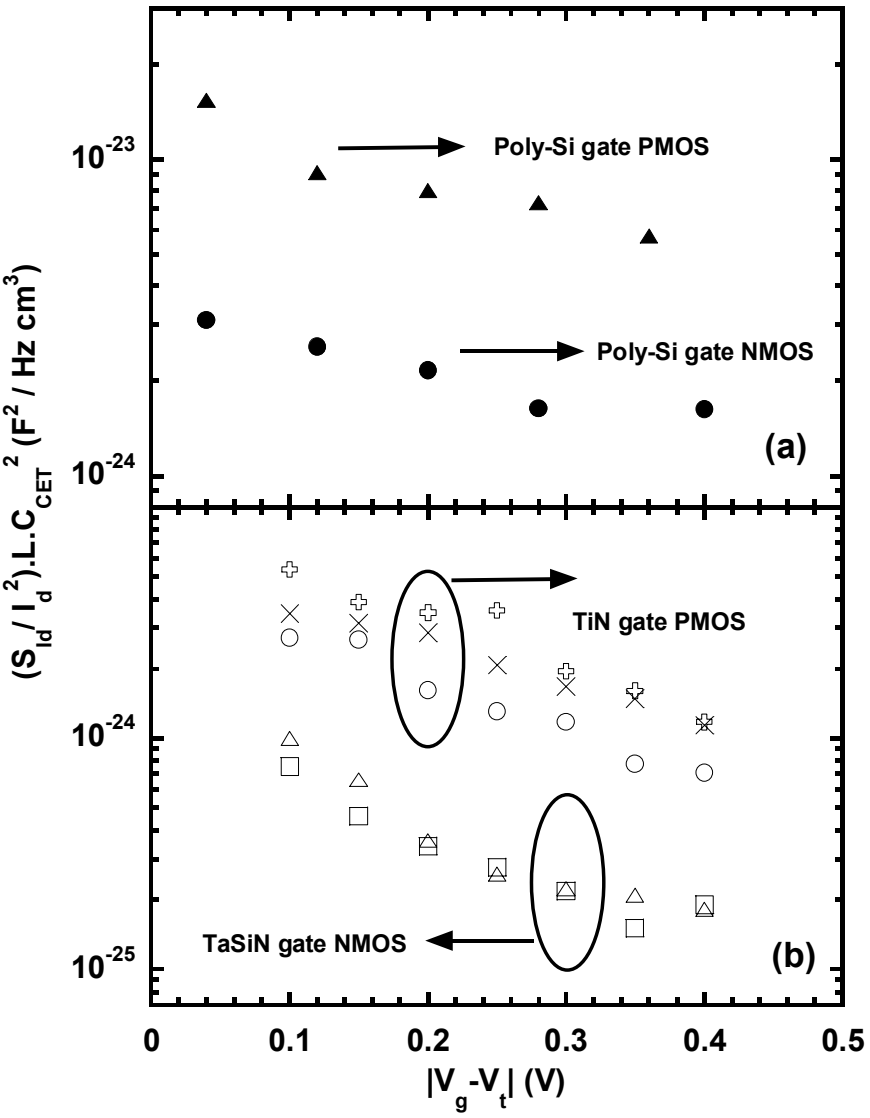

Figure 4.10 Inherent device noise comparison among n- & p-type MOSFETs with HfO_2 gate dielectric and (a) poly-Si gate (b) metal gates.

A comparison of normalized noise in n and p-type MOSFETs, with HfO_2 as the high-k gate dielectric, is given for both poly-Si and metal gate devices. Irrespective of the gate electrode material, the p-type high-k MOSFETs exhibited higher noise magnitude compared to n-type devices. From Tables 4.1 and 4.2, the trap density values

were found to be higher in p-type MOSFETs comparatively. Therefore, the HfO_2 trap density is lower in the upper mid-gap region than that in the lower mid-gap region of the silicon band gap. On the contrary, a reverse trend for trap distribution was reported in [5,107] and this discrepancy might be attributed to differences in process-related parameters.

4.5 Summary

A comparative study has been provided for low frequency noise characteristics of MOSFETs with TaSiN/HfO_2/SRPO SiO_2, TaSiN/HfO_2/RCA SiO_2, TiN/HfO_2/RCA SiO_2 and poly-Si/HfO_2/RCA SiO_2 gate stacks. The metal-gated devices exhibited lower noise magnitude and higher mobility values than poly-Si gated devices. This implies a less defective gate dielectric stack. The dielectric trap density extracted for TaSiN gate high-k MOSFETs here, was the lowest reported value thus far for any high-k gate stack. The lower Coulomb scattering coefficient obtained from noise data for SRPO devices compared to RCA devices implied higher effective mobility for the former and was confirmed by split C-V measurements. Regardless of the gate material, p-type MOSFETs exhibited higher noise than n-type counterparts indicating a higher trap density at the lower Si band gap region compared to the upper mid-gap region.

CHAPTER 5

NOISE MODELING REVISITED

5.1 Introduction

Thus far, the analysis of 1/f noise and parameter extraction was done using the Unified noise model. This model was based on correlated carrier number-mobility fluctuations theory that attributes noise to the trapping/de-trapping of channel carriers (via equal energy tunneling process) by traps located in the gate dielectric. Now, the model was originally proposed for single gate dielectric MOSFETs and under the assumption that the dielectric trap density is uniform both spatially and with respect to energy.

In the case of high-k MOSFETs, the interfacial layer is formed either inadvertently or intentionally resulting in a multi-layered dielectric stack. Consequently, several new aspects come in to play that modify the 1/f noise characteristics. To clarify, the tunneling coefficient for channel carriers is a function of the material properties of the dielectrics such as barrier height and carrier effective mass. While the barrier heights presented to the tunneling channel carriers by the constituent dielectric layers would be different, the effective mass of the carriers is specific to the type of dielectric material. In addition, it has been shown in Chapter 3 that the high-k trap density is higher than that of the underlying interfacial layer so that the uniform trap density

assumption would not be valid anymore. Further, the individual thicknesses of the high-k and interfacial layers can be parameters that define the noise characteristics.

The Multi-Stack Unified Noise model (MSUN), which is based on correlated carrier number and mobility fluctuations theory, is hereby proposed to characterize 1/f noise. This model takes in to account the various material properties of the dielectrics constituting the gate stack and is scalable with respect to MOSFET dimensions, bias, temperature and high-/interfacial layer thicknesses. Additionally, the non-uniformity in the dielectric trap density profile is incorporated in the formulation as explained in the next section. The model will be shown to be in good agreement with the experimental data. In the following, HK and IL will be used as a short form for high-k dielectric and interfacial layers, respectively.

5.2 Multi-Stack Unified Noise (MSUN) Model Derivation

The MSUN model is based on the correlated carrier number and mobility fluctuations theory. Pursuing a similar approach as the Unified Model in Chapter 2, the expression for power spectral density of local current fluctuations in an infinitesimal channel length Δx can be written as,

$$S_{\Delta I_d}(x,f) = \left[\frac{I_d}{W\Delta x}\left(\frac{1}{N} \pm \alpha_{sc}\mu_{eff}\right)\right]^2 S_{\Delta N_t}(x,f) \tag{5.1}$$

where, the terms have their usual meaning. Figure 5.1 depicts the MOSFET structure with high-k/interfacial layer stack. The co-ordinate system considered is provided for reference. The power spectral density of the mean square fluctuations in the trapped

charge carriers over the area $W\Delta x$ can be written as the summation of Lorentzian spectra due to traps in the interfacial and high-k layers as [106],

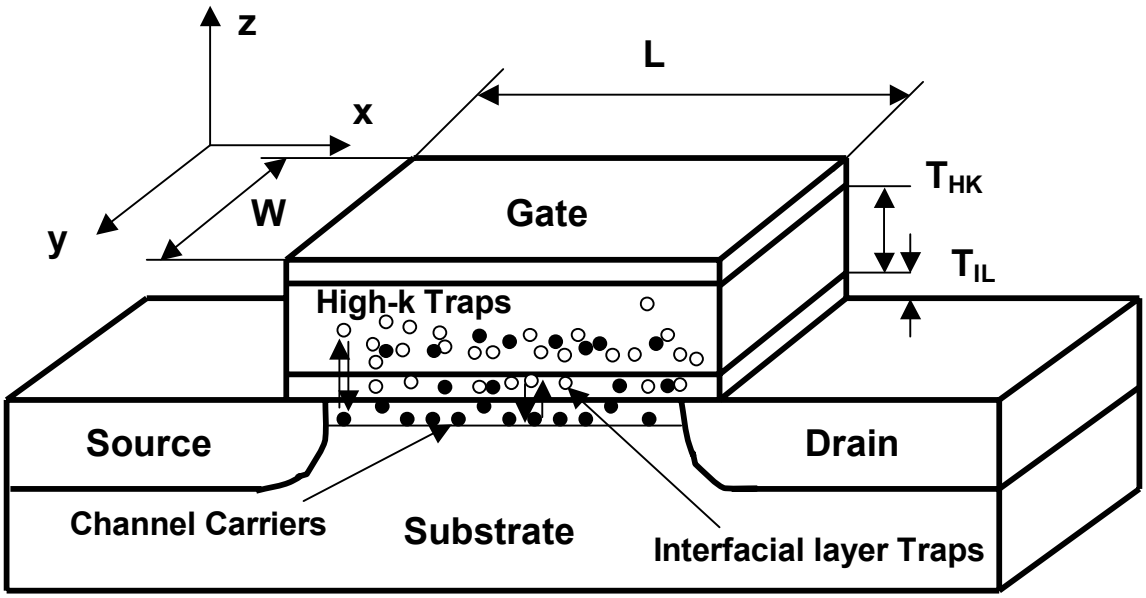

Figure 5.1 Typical structure of MOSFET with high-k/interfacial layer gate stack.

$$S_{\Delta N_t}(x,f)=\int_{E_v}^{E_c}\int_{0}^{W}\int_{0}^{T_{IL}}4N_{tIL}(E,x,y,z)\Delta x f_t(1-f_t)\frac{\tau(E,x,y,z)}{1+\omega^2\tau^2(E,x,y,z)}dzdydE + \int_{E_v}^{E_c}\int_{0}^{W}\int_{T_{IL}}^{T_{HK}+T_{IL}}4N_{tHK}(E,x,y,z)\Delta x f_t(1-f_t)\frac{\tau(E,x,y,z)}{1+\omega^2\tau^2(E,x,y,z)}dzdydE \tag{5.2}$$

where, $\tau(E,x,y,z)$ is the trapping time constant in the gate dielectric (s), T_{IL} is the interfacial layer thickness (cm), T_{HK} is high-k dielectric layer thickness (cm), $\omega=2\pi f$ is angular frequency (rad/s), E_c is the conduction band edge (eV), E_v is the valence band edge (eV), E denotes the trap energy level (eV), E_{fn} is the quasi-Fermi level (eV), $f_t=\left\lfloor 1/\left(1+\exp[(E-E_{fn})/kT]\right)\right\rfloor$ is the trap occupancy function, $N_{tIL}(E,x,y,z)$ is the trap

density in the interfacial layer ($cm^{-3}eV^{-1}$), $N_{tHK}(E,x,y,z)$ is the trap density in the high-k dielectric layer ($cm^{-3}eV^{-1}$).

Under the assumption of a uniform trap distribution along the length and width of the channel, and since $f_t(1-f_t)$ acts as a delta function around quasi-Fermi level (as shown in Chapter 2), it can be deduced that $\int_{E_v}^{E_c} N_t(E,x,y,z) f_t(1-f_t) dE = kTN_t(E_{fn},z)$. In addition, the trapping time constant would now be a function of only the distance into the gate dielectric. Thus, (5.2) can be modified as,

$$S_{\Delta N_t}(x,f) = 4kTW\Delta x \left[\left(\int_0^{T_{IL}} N_{tIL}(E_{fn},z) \frac{\tau(z)}{1+\omega^2\tau^2(z)} dz \right) + \left(\int_{T_{IL}}^{T_{HK}+T_{IL}} N_{tHK}(E_{fn},z) \frac{\tau(z)}{1+\omega^2\tau^2(z)} dz \right) \right] \quad (5.3)$$

It has been reported that the interface trap density takes a U-shaped profile across the Si energy gap in conventional SiO_2 MOSFETs [108]. Based on this observation, the energy dependence of HK/IL trap density will be formulated as explained next.

Figure 5.2 depicts a typical band diagram for the high-k MOSFET. Here, N_{tIL0} is the mid-gap (i.e. intrinsic Fermi level) trap density at the Si/IL interface ($cm^{-3}eV^{-1}$), N_{tHK0} is the mid-gap trap density at the IL/HK interface ($cm^{-3}eV^{-1}$), E_i is the intrinsic Fermi level at the Si/SiO_2 interface (eV). With the mid-gap trap densities as the reference point, the non-uniform trap density is represented by an exponentially

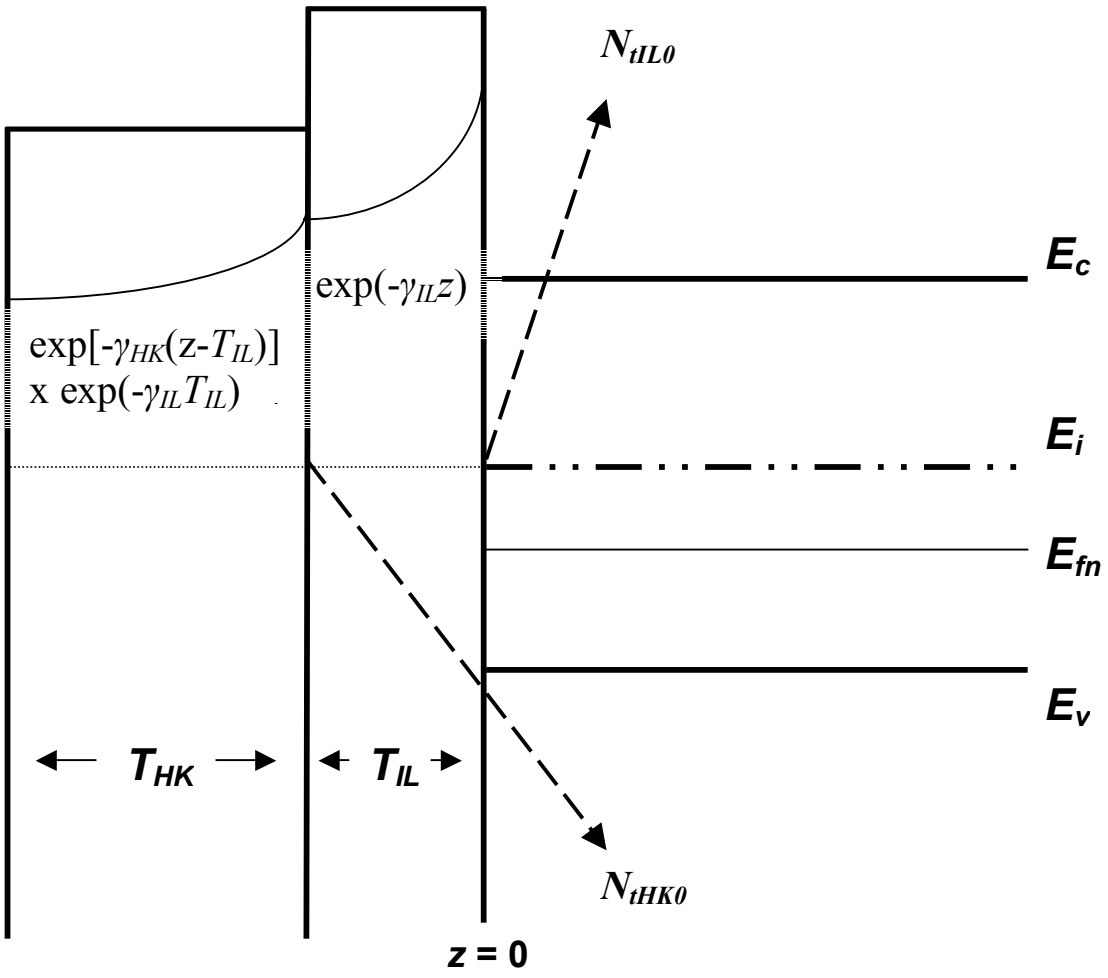

Figure 5.2 General band structure for high-k MOSFETs.

varying function with respect to Si band gap energy and the distance into the gate dielectric with the functional form as shown in Figures 5.3 and 5.4. Here, N_{t0} represents the trap density at the Si/SiO_2 interface and the intrinsic Fermi level. The parameter ξ (with positive/negative sign) defines the exponential rate at which the trap density changes (increases/decreases) in the small energy interval that the quasi-Fermi level sweeps. That is, the dielectric trap density in the energy interval of interest is an

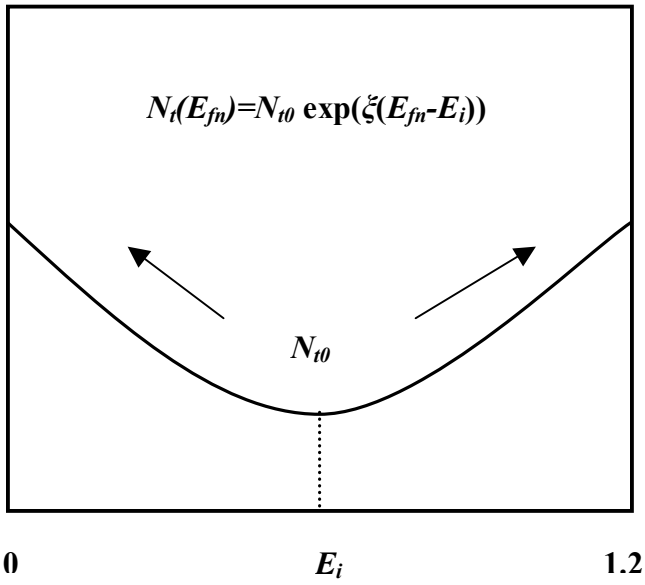

Figure 5.3 Dielectric trap density variation with respect to energy for a positive value of ξ (Illustration only. Not a real profile).

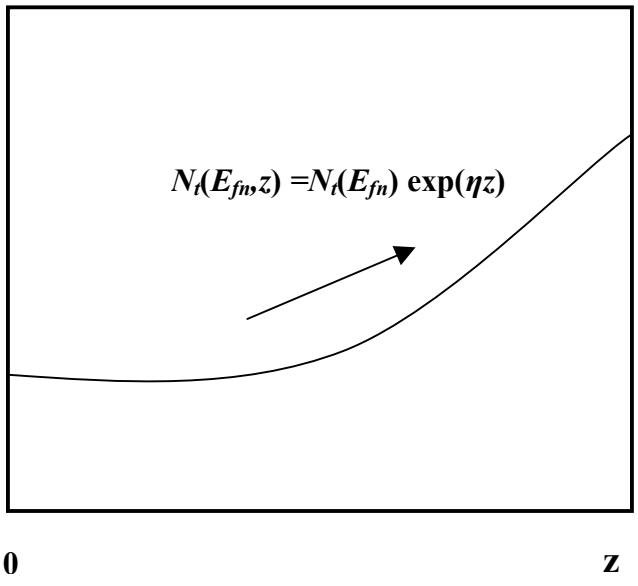

Figure 5.4 Trap density profile into the gate dielectric for a positive value of η (Illustration only. Not an actual profile).

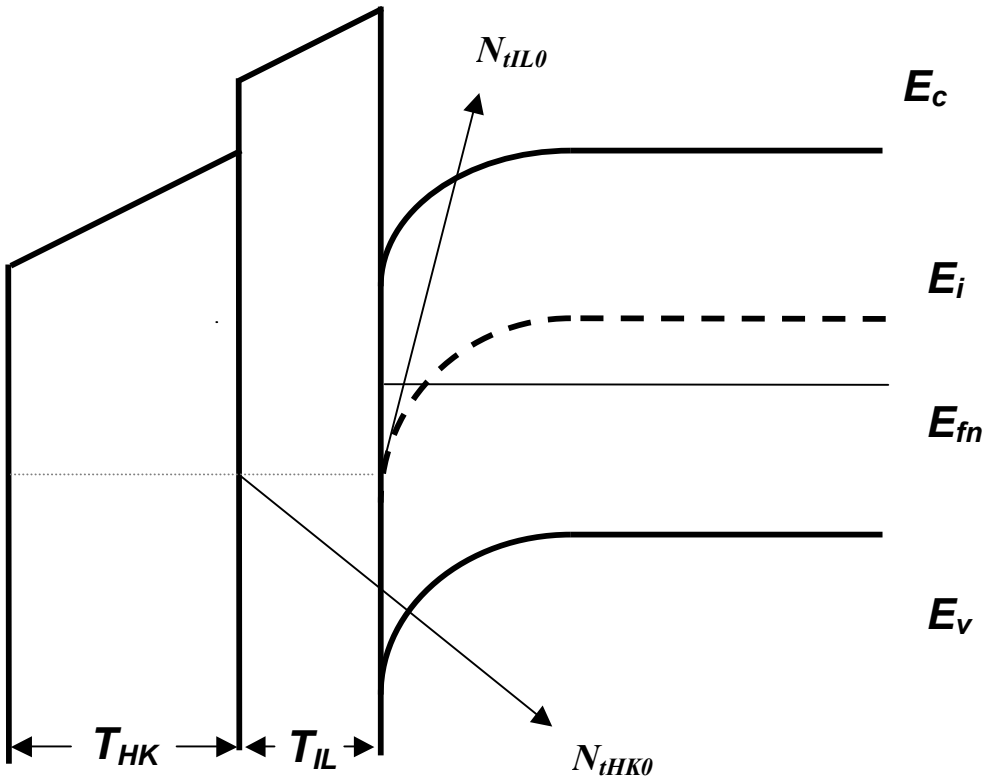

Figure 5.5 The band bending caused by the applied bias modifies the trap profile at any location in the dielectric stack.

extrapolation of the trap density at the intrinsic Fermi level (or Si-substrate mid-gap energy level). For a particular energy level, the distribution of traps looking into the gate dielectric is given by an exponentially varying function with parameter η representing the rate at which the trap density increase/decreases with respect to the distance from the substrate. Further, when a gate bias is applied, the energy bands of the gate dielectrics bend i.e., they are pulled down as shown in Figure 5.5. This causes an alteration in the trap density encountered by the channel carriers that are tunneling into the dielectric traps at constant energy. This effect is incorporated in the trap profile by a

band bending term represented by the parameter λ. Thus, the quasi-Fermi level trap density at any position in the high-k/interfacial layer stack can now be written as,

$$N_{tIL}(E_{fn},z)=N_{tIL0}\exp[\xi_{IL}(E_{fn}-E_i)+(q\lambda_{IL}V_{gIL}/T_{IL})z+\eta_{IL}z] \quad \text{for } 0<z<T_{IL} \tag{5.4}$$

$$N_{tHK}(E_{fn},z)=N_{tHK0}\exp[\xi_{HK}(E_{fn}-E_i)+(q\lambda_{HK}V_{gHK}/T_{HK})(z-T_{IL})+\eta_{HK}(z-T_{IL})]$$

$$\text{for } T_{IL}<z<T_{HK}+T_{IL} \tag{5.5}$$

with, ξ_{IL} and ξ_{HK} as the model fitting parameters that define the energy dependence of IL and HK traps (eV^{-1}), η_{IL} and η_{HK} being the respective fitting parameters for the distribution of traps in the IL and HK (cm^{-1}), λ_{IL} and λ_{HK} representing the band bending parameters for IL and HK (eV^{-1}). Additionally, $V_{gIL}=(V_g-V(x))[T_{IL}\varepsilon_{HK}/(T_{IL}\varepsilon_{HK}+T_{HK}\varepsilon_{IL})]$, $V_{gHK}=(V_g-V(x))[T_{HK}\varepsilon_{IL}/(T_{IL}\varepsilon_{HK}+T_{HK}\varepsilon_{IL})]$ (V), V_g is the applied gate potential (V), $V(x)=(V_d/L)x$ is the channel potential due to lateral field at a distance x from the source (V), V_d is the drain to source bias, $\varepsilon_{IL}/\varepsilon_{HK}$ are dielectric constants of IL/HK (Fcm^{-1}), respectively. On a related note, the exponential dependence for the trap density is assumed here for mathematical convenience and other forms can be readily incorporated as desired.

The tunneling probability into the gate dielectric for the channel carriers is considered as an exponentially decaying function with attenuation rates that are specific to the dielectric material as indicated in Figure 5.2. Here, the reflections at the gate/high-k interface are neglected so that the ratio of the magnitudes of forward

traveling wave to that of the reflected wave at the HK/IL interface can be approximated as $exp(2\gamma_{IL}T_{IL})$. For a typical high-k gate stack with ~1nm IL thickness the ratio would be ~ $exp(20)$ >> 1. Thus, the reflections from the HK/IL interface could be neglected to arrive at the tunneling probabilities as illustrated.

Using WKB (Wentzel-Kramer-Brillouin) approximation, the trapping time constant (using $\tau(z)=\tau$ for convenience) for interfacial layer ($0<z<T_{IL}$) is written as,

$$\tau = \tau_0 \exp(\gamma_{IL} z) \tag{5.6}$$

so that, $$d\tau = \tau_0 \gamma_{IL} \exp(\gamma_{IL} z) dz \quad \text{or} \quad \frac{d\tau}{\gamma_{IL}\tau} = dz \tag{5.7}$$

where, $\tau_0 = 10^{-10} s$ [109], $\gamma_{IL} = \frac{4\pi}{h}\sqrt{2m_{IL}^{*}\Phi_{IL}}$ [54,66] is the carrier tunneling coefficient in the IL (cm^{-1}), m_{IL}^{*} is the effective mass of the carrier in the IL (Kg), and Φ_{IL} is the interfacial layer barrier height encountered by the channel carriers (eV).

Correspondingly, the characteristic time constant for traps in the HK ($T_{IL}<z<T_{HK}+T_{IL}$) is expressed as,

$$\tau = \tau_0 \exp(\gamma_{IL} T_{IL} - \gamma_{HK} T_{IL}) \exp(\gamma_{HK} z) \tag{5.8}$$

$$d\tau = \tau_0 \exp(\gamma_{IL} T_{IL} - \gamma_{HK} T_{IL}) \exp(\gamma_{HK} z) dz \quad \text{and} \quad \frac{d\tau}{\gamma_{HK}\tau} = dz \tag{5.9}$$

where, $\gamma_{HK} = \frac{4\pi}{h}\sqrt{2m_{HK}^{*}\Phi_{HK}}$ is the carrier tunneling coefficient in HK (cm^{-1}), m_{HK}^{*} is the carrier effective mass in HK (kg), and Φ_{HK} is the HK band offset from silicon (eV).

A change of variable from z to τ in (5.3) is needed. Hence, (5.6) is modified as follows,

$$z = \ln\left(\frac{\tau}{\tau_0}\right)^{\left(1/\gamma_{IL}\right)}$$

$$z\left[(q\lambda_{IL}V_{gIL}/T_{IL})+\eta_{IL}\right] = \left[(q\lambda_{IL}V_{gIL}/T_{IL})+\eta_{IL}\right]\ln\left(\frac{\tau}{\tau_0}\right)^{\left(1/\gamma_{IL}\right)}$$

$$z\left[(q\lambda_{IL}V_{gIL}/T_{IL})+\eta_{IL}\right] = \ln\left(\frac{\tau}{\tau_0}\right)^{\left[(q\lambda_{IL}V_{gIL}/T_{IL})+\eta_{IL}\right]\left(1/\gamma_{IL}\right)}.$$

Defining $\beta_{IL} = [(q\lambda_{IL}V_{gIL}/T_{IL})+\eta_{IL}]$,

$$\beta_{IL} z = \ln\left(\frac{\tau}{\tau_0}\right)^{\left(1/\gamma_{IL}\right)\beta_{IL}}$$

$$\exp\left(\beta_{IL} z\right) = \left(\frac{\tau}{\tau_0}\right)^{\left(\beta_{IL}/\gamma_{IL}\right)} \tag{5.10}$$

Similarly, considering (5.8) and by using $\beta_{HK} = [(q\lambda_{HK}V_{gHK}/T_{HK})+\eta_{HK}]$, we have,

$$\exp\left[\beta_{HK}\left(z - T_{IL}\right)\right] = \exp\left(-\beta_{HK}T_{IL}\right)\left(\frac{\tau}{\tau_0 \exp[(\gamma_{IL}T_{IL} - \gamma_{HK}T_{IL})]}\right)^{\left(\beta_{HK}/\gamma_{HK}\right)} \tag{5.11}$$

After substituting (5.4), (5.5), (5.7), (5.9), (5.10) and (5.11) in (5.3) and setting the appropriate limits for the integral we get,

$$S_{\Delta N_t}(x,f) =$$

$$4kTW\Delta x\left[\begin{array}{l}\dfrac{N_{tIL0}\exp[\xi_{IL}(E_{fn}-E_i)]}{\gamma_{IL}}\displaystyle\int_{\tau_0}^{\tau_0\exp(\gamma_{IL}T_{IL})}\frac{1}{1+\omega^2\tau^2}\left(\frac{\tau}{\tau_0}\right)^{(\beta_{IL}/\gamma_{IL})}d\tau \\ +\dfrac{N_{tHK0}\exp[\xi_{HK}(E_{fn}-E_i)]}{\gamma_{HK}}\displaystyle\int_{\tau_0\exp(\gamma_{IL}T_{IL})}^{\tau_0\exp(\gamma_{HK}T_{HK}+\gamma_{IL}T_{IL})}\frac{1}{1+\omega^2\tau^2}\left(\frac{\tau}{\tau_0\exp(\gamma_{IL}T_{IL})}\right)^{(\beta_{HK}/\gamma_{HK})}d\tau\end{array}\right]$$

Using $\omega\tau = u$ in the above expression,

$$S_{\Delta N_t}(x,f)=\frac{4kTW\Delta x}{\omega}\left[\begin{array}{l}\dfrac{N_{tIL0}\exp[\xi_{IL}(E_{fn}-E_i)]}{\gamma_{IL}(\omega\tau_0)^{(\beta_{IL}/\gamma_{IL})}}\displaystyle\int_{\omega\tau_0}^{\omega\tau_0\exp(\gamma_{IL}T_{IL})}\frac{u^{(\beta_{IL}/\gamma_{IL})}}{1+u^2}du \\ +\dfrac{N_{tHK0}\exp[\xi_{HK}(E_{fn}-E_i)]}{\gamma_{HK}[\omega\tau_0\exp(\gamma_{IL}T_{IL})]^{(\beta_{HK}/\gamma_{HK})}}\displaystyle\int_{\omega\tau_0\exp(\gamma_{IL}T_{IL})}^{\omega\tau_0\exp(\gamma_{HK}T_{HK}+\gamma_{IL}T_{IL})}\frac{u^{(\beta_{HK}/\gamma_{HK})}}{1+u^2}du\end{array}\right] \tag{5.12}$$

Including the variation of channel carrier density due to the lateral field in the channel direction, (5.1) can be written as,

$$S_{\Delta I_d}(x,f)=\left[\frac{I_d}{W\Delta x}\left(\frac{1}{N(x)}\pm\alpha_{sc}\mu_{eff}\right)\right]^2 S_{\Delta N_t}(x,f) \tag{5.13}$$

The total drain current noise power spectral density can thus be obtained from (5.12) and (5.13) as,

$$S_{I_d}(f)=\frac{1}{L^2}\int_0^L S_{\Delta I_d}(x,f)\Delta x dx \tag{5.14}$$

With these substitutions, the MSUN model is derived to characterize the noise power spectral density in MOSFETs with high-k/interfacial layer gate stack.

5.3 Experimental Verification of MSUN Model

In the following, the MSUN model is experimentally verified by data on TaSiN/27Å HfO_2/ 10Å (SRPO or RCA) SiO_2 MOSFETs in the 78-350K range and relevant analysis is provided. 1/f noise, I-V, and split C-V measurements were performed employing the procedure outlined in Chapter 2. Further details regarding the MOSFETs used here can be found in Chapter 4.

The MSUN model is based upon the correlated number and mobility fluctuations theory and Figure 5.6 shows a plot that validates this assumption. S_{Id}/ I_d^2 and $(g_m/I_d)^2$ plotted against I_d are found to follow the same trend implying the carrier number fluctuations to be the dominant noise causing mechanism. In the foregoing chapters and generally [110, 111], this validation was done for high-k MOSFETs operated at room temperature. It is shown here that the number fluctuations mechanism holds well for temperatures down to 78K.

The procedure for MSUN model parameter extraction will be outlined next. At first, the frequency exponent (σ as in $1/f^{\sigma}$) is obtained as the negative slope of noise curve in the 1-100 Hz region (log-log plot), for various gate bias conditions in the temperature range considered. It can be seen in (5.12) that the frequency dependence of noise power spectral density primarily comes from $(\omega)^{-(1+\beta_{IL}/\gamma_{IL})}$ and $(\omega)^{-(1+\beta_{HK}/\gamma_{HK})}$ terms, where $\beta_{HK} = [(q\lambda_{HK}V_{gHK}/T_{HK}) + \eta_{HK}]$ and $\beta_{IL} = [(q\lambda_{IL}V_{gIL}/T_{IL}) + \eta_{IL}]$. In view of the fact that, for ~1 nm interfacial layer, the main contribution to the total noise in the considered frequency range comes from the high-k layer [110], only the high-k term can

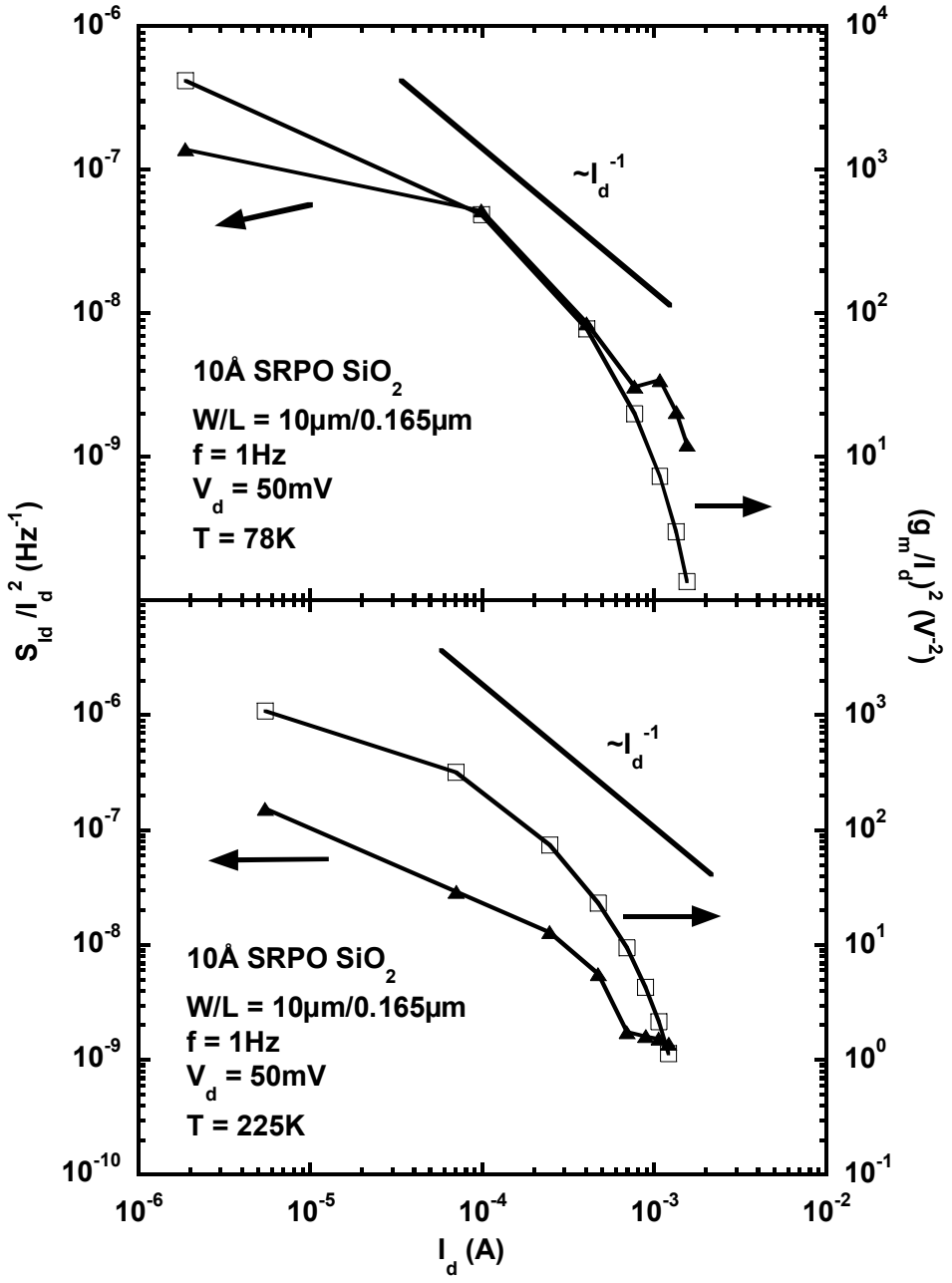

Figure 5.6 Plot to confirm the validity of correlated carrier number-mobility fluctuations as the physical mechanism for noise at low temperatures.

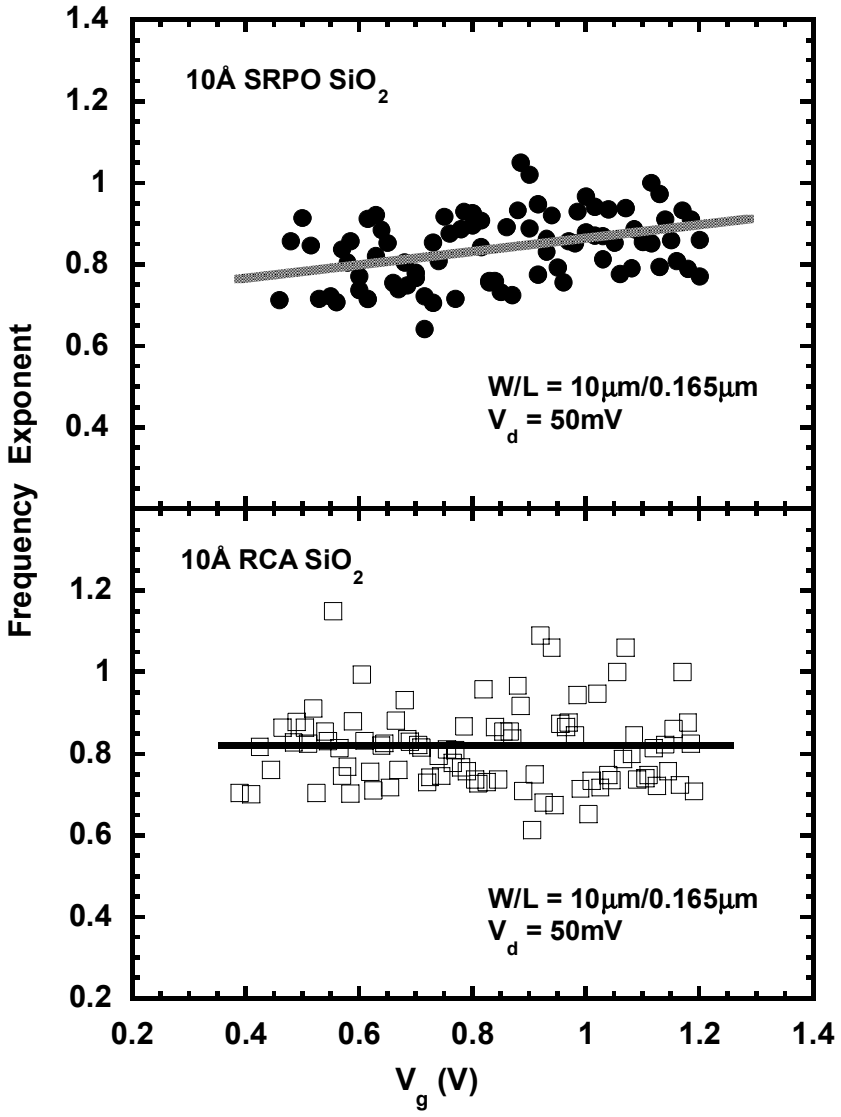

Figure 5.7 The frequency exponent σ of noise in the 1-100 Hz region is plotted for applied gate bias. A straight line fit is made to the data from which parameters η_{HK}, λ_{HK} are extracted.

be considered for further calculations. Thus, the parameters λ_{HK} and η_{HK} can be extracted as the slope and intercept, respectively, from σ in Figure 5.7.

The parameter values extracted are λ_{HK} = 4.68 eV^{-1} and η_{HK} = -1.27x10^7 cm^{-1} for SRPO devices, and λ_{HK} = 0.045 eV^{-1}, η_{HK} = -0.85x10^7 cm^{-1} for RCA devices. The negative sign for η_{HK} implies a decreasing trend for trap density farther into the high-k dielectric from the HK/IL interface and this decline in the number of traps is comparatively higher for SRPO devices than RCA devices. In addition, the positive sign for λ_{HK} implies that the tunneling carriers find an increased trap density in the HK due to band-bending caused by the applied gate bias. This would mean a higher trap concentration towards the band edges that results in an increased noise level as the gate voltage is increased. For all devices, a positive value of ξ_{HK} = 0.1 eV^{-1} was used that is consistent with the above observation. Now, when the gate bias is applied, the position of quasi-Fermi level changes and the energy band in the gate dielectric is pulled down (considering inversion in NMOS). Therefore, the applied bias has a two fold effect on the effective trap density as seen by the channel carriers tunneling into the gate dielectric at equal energy. Firstly, the non-uniform trap distribution with respect to energy and the altered trap density profile at any location in the gate dielectric stemming from this energy dependence of the trap density. Consequently, $\xi_{HK} = \lambda_{HK}$ and $\xi_{IL} = \lambda_{IL}$ in an ideal case. However, independent values for λ_{HK} and λ_{IL} would be used since the validity of the assumed ξ_{HK} and ξ_{IL} values is limited to a very narrow energy interval [108]. In the passing, it should be mentioned that the parameter sets

(λ_{HK}, η_{HK}) and (λ_{IL}, η_{IL}) can be extracted from σ that is obtained in the corresponding frequency regions where the individual dielectric layers have a major noise contribution.

The MSUN model can now be fit to the noise data by using λ_{HK} and η_{HK} as obtained above, and appropriately choosing the parameters N_{tHK0}, ξ_{HK}, and μ_{c0} that are substituted in (5.12), (5.13) and (5.14). Other parameters such as inversion layer charge, mobility were obtained from C-V and I-V measurements. Figure 5.8 shows the current noise power spectra in the 1-100 Hz region for SRPO and RCA devices biased at (V_g-V_t) = 0.7 V and V_d = 50 mV. Further, Figure 5.9 depicts the 1 Hz current noise power spectral density values from the experiments and MSUN model plotted against the gate overdrive. In general, an excellent agreement is obtained between the model fittings and the experimental data for all devices and at all temperatures. It should be noted that, for all MOSFETs belonging to a particular process split, a single trap distribution parameter set (η_{HK}, λ_{HK}, ξ_{HK}) was used for fitting to the noise spectra at all temperatures and bias conditions. The parameters N_{tHK0} and μ_{c0} were allowed to vary freely with respect to temperature. It can be observed in Figure 5.10 that, within the experimental error, the values are fairly constant.

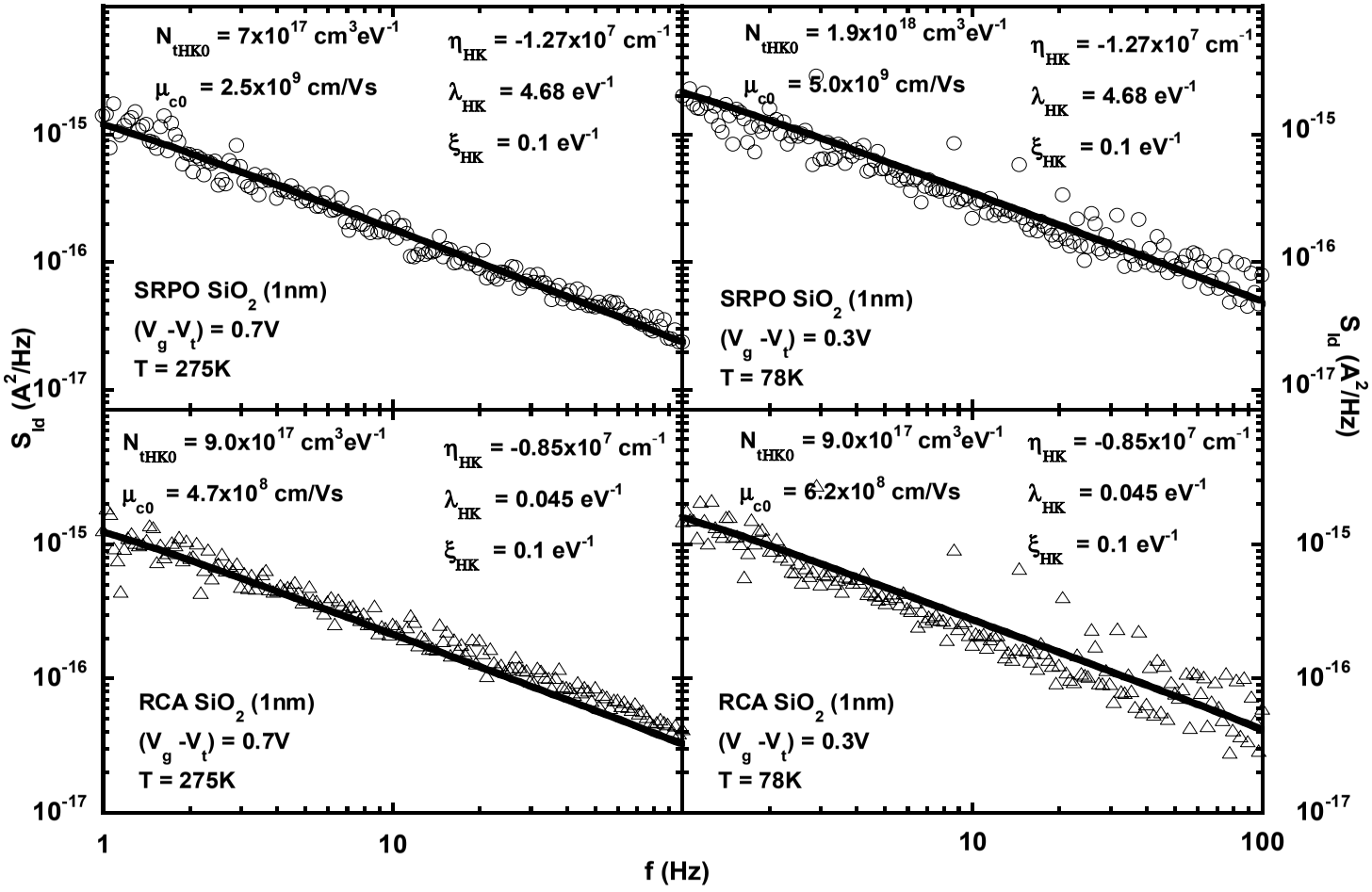

Figure 5.8 The solid line depicts the MSUN model fitting to the experimental noise data. Good agreement is observed at all temperatures and for all devices.

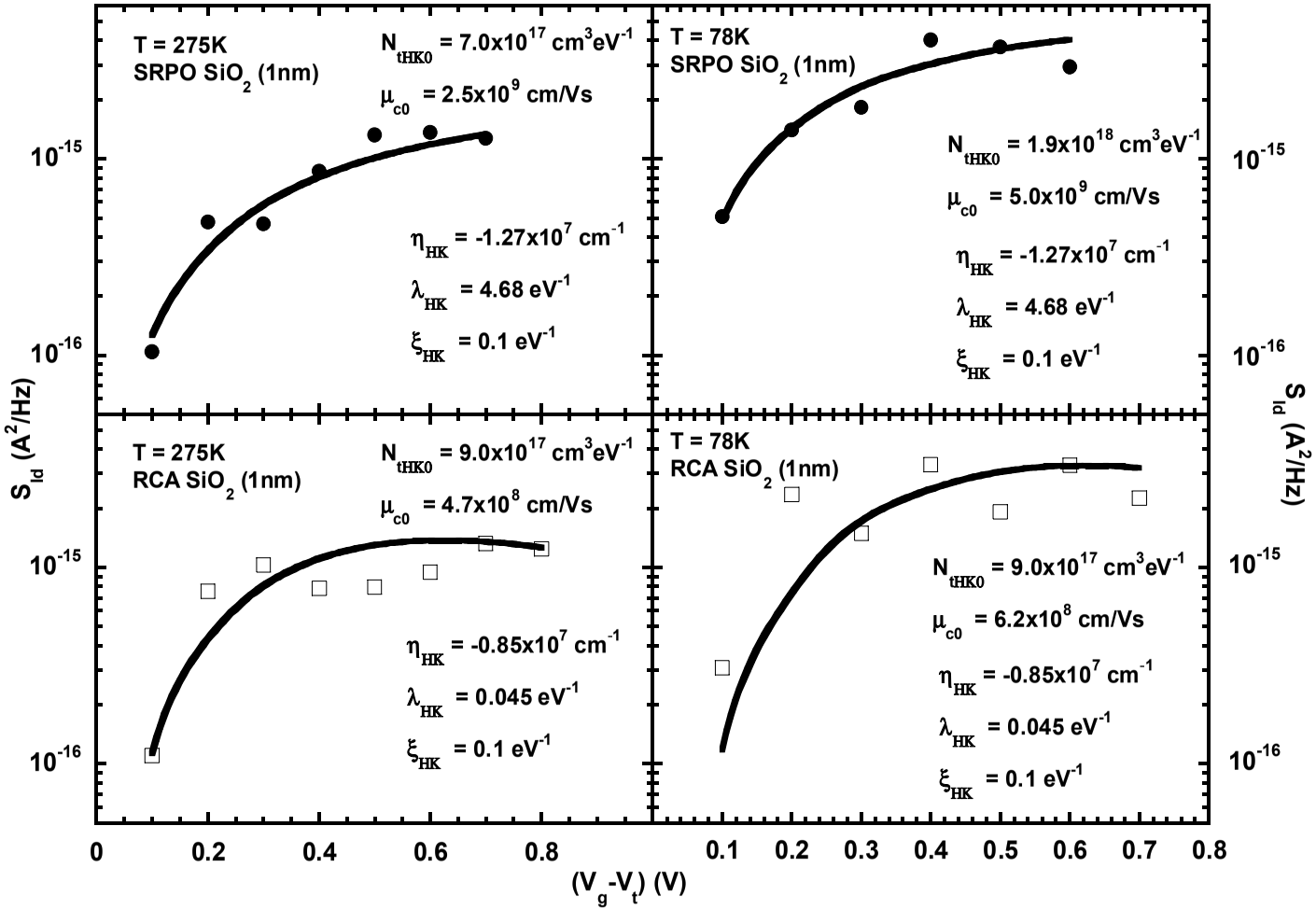

Figure 5.9 The MSUN model fitting is in excellent agreement with the actual noise data at all bias points. Here, the 1 Hz value of the current noise power spectral density is plotted for different gate bias values.

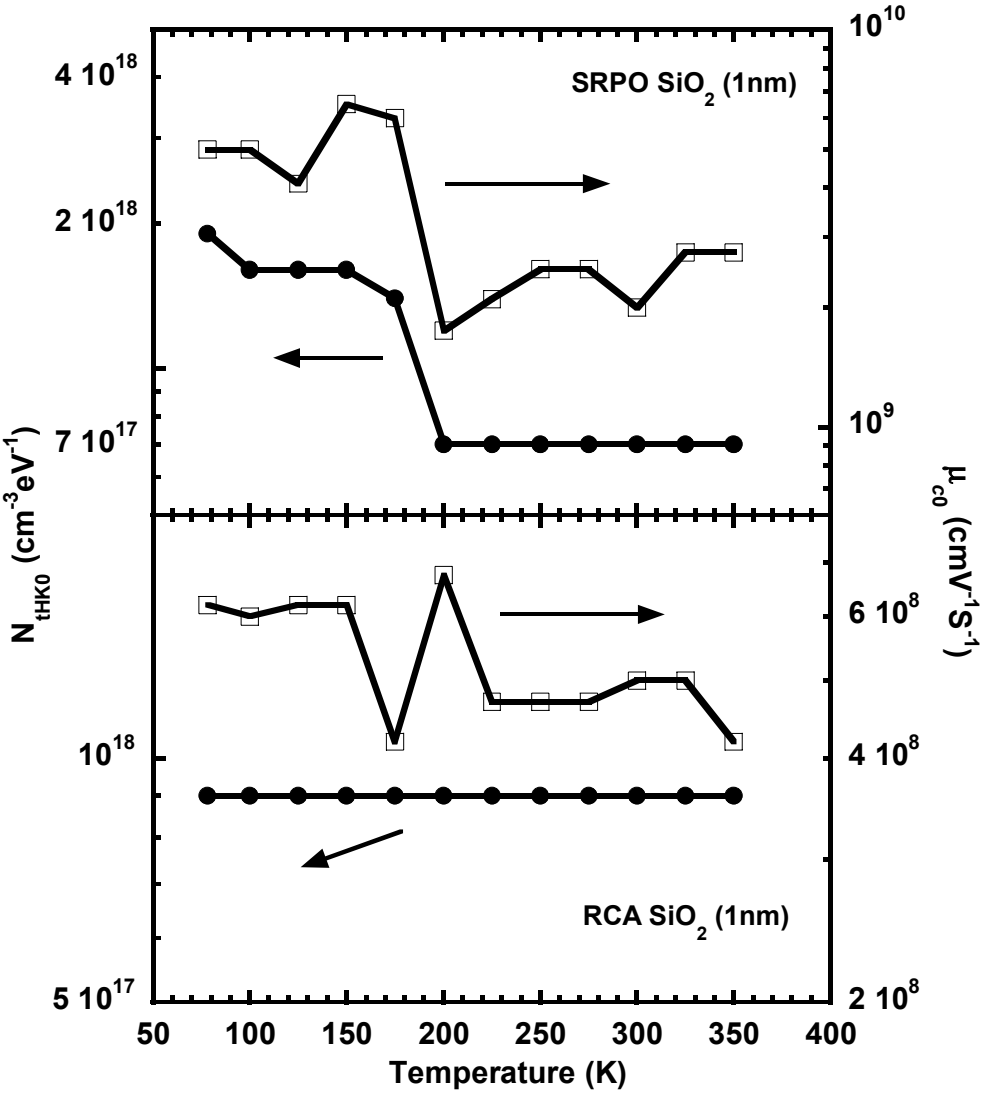

Figure 5.10 The mid-gap trap density at HfO_2/SiO_2 (SRPO or RCA) interface along with the fitting parameter μ_{c0} extracted from the noise data by using the MSUN model.

For MOSFETs from the two splits considered, the effective trap density was extracted at each temperature set-point, using the original Unified Flicker Noise Model expression. As depicted in Figure 5.11, there was over an order magnitude variation in the trap density within the temperature range considered. In comprehending this

decreasing trend with respect to temperature, one might point to the fact that the quasi-Fermi level would be located closer to the mid-gap for the same gate overdrive at low temperatures, thereby deducing that the trap density is decreasing towards the mid-gap and away from the band edges. However, the energy interval swept by the quasi-Fermi

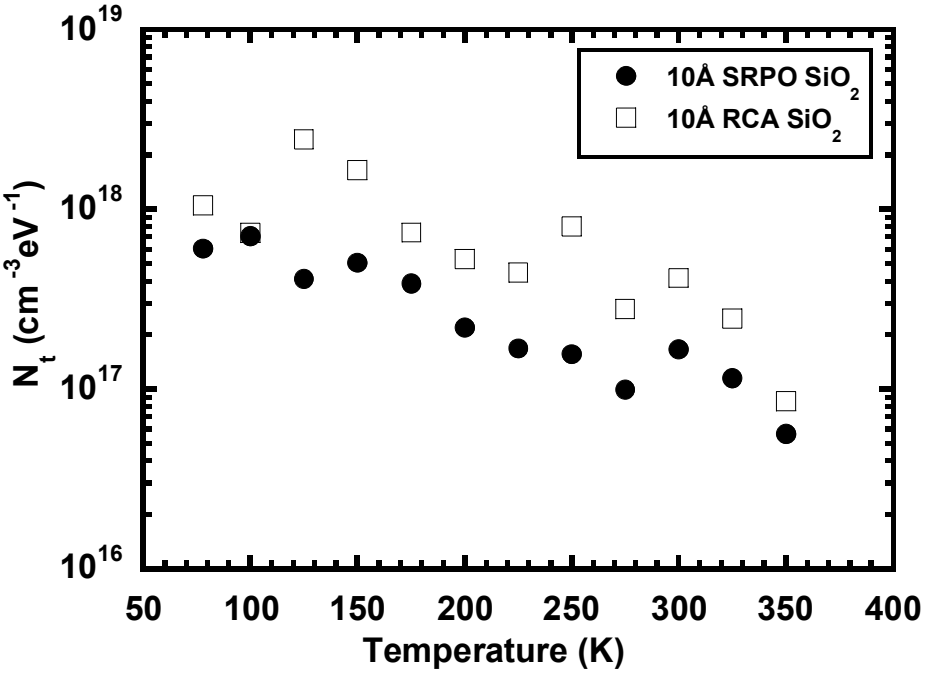

Figure 5.11 The effective trap density values calculated at each temperature set-point using the Unified Flicker Noise Model.

level for the temperature and the bias range considered in this work was 0.05 eV as shown in Figure 5.12, which is too small to witness over an order of magnitude variation in the trap density. Hence, the observed trend is unrealistic. Moreover, the Unified Model assumes a uniform trap density with respect to space and energy at the core of the derivation that is inconsistent with the extracted values above. In contrast, the MSUN model accounts for the trap density variation with respect to

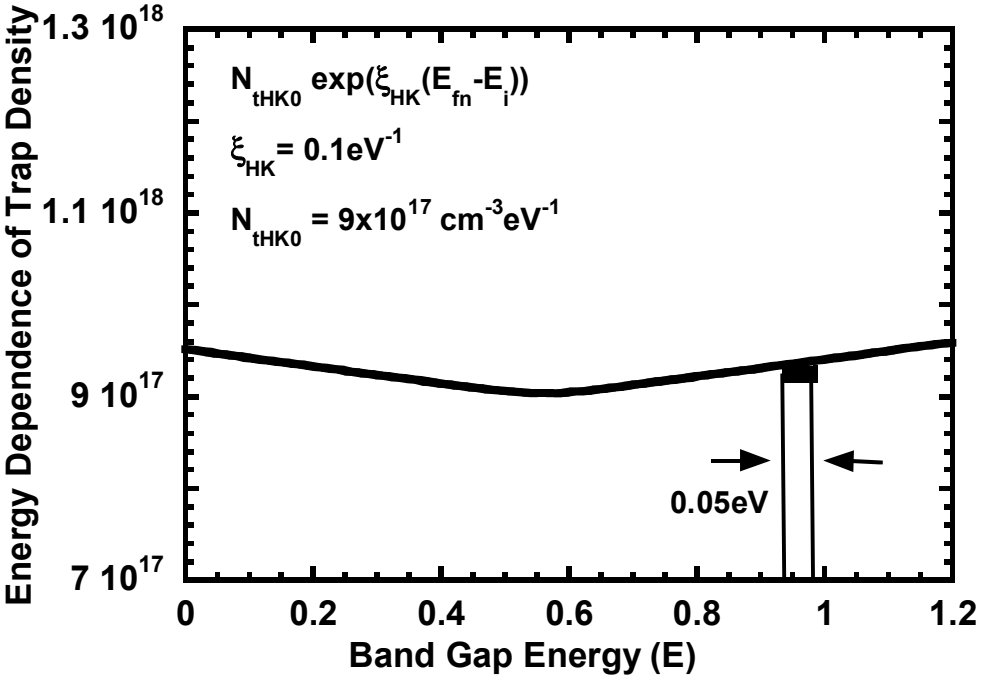

Figure 5.12 The energy interval swept by the quasi-Fermi level for the temperature and bias range considered.

energy and distance, thereby avoiding the aforementioned anomaly with temperature scaling.

It should be noted, that the fitting parameter set necessary to obtain the complete 1/f noise spectrum is given by ($N_{tHK0}, \xi_{HK}, \lambda_{HK}, \eta_{HK}, N_{tIL0}, \xi_{IL}, \lambda_{IL}, \eta_{IL}, \mu_{c0}$). In practice, the MOSFETs would have an interfacial layer thickness that is about 0.6-1nm. Since the low frequency region is of interest (where the noise contribution is mainly from the high-k dielectric), the parameters $N_{tIL0}, \xi_{IL}, \lambda_{IL}, \eta_{IL}$ would be redundant and only 5 parameters would be needed. Further, for relatively smaller sweeps made by the quasi-Fermi level, using $\xi_{HK} = \lambda_{HK}$ would reduce the total noise parameters to 4.

Error Analysis:

The measurements, from which the various parameters were extracted above, can be repeated with reasonable accuracy. From measurements done on the same MOSFET at different times, the DC parameters such as drain current, conductance, transconductance, threshold voltage can be obtained with an error margin that is well within 5%. Similarly, the inversion layer charge density and effective carrier mobility can be extracted from gate to channel capacitance with less than 5% relative error. Additionally, it is estimated that the values assumed by the dielectric trap density (N_t, N_{tHK0}) and μ_{c0} would span less than half an order of magnitude. Finally, the error in extracting the trap parameters ($\xi_{HK}, \lambda_{HK}, \eta_{HK}$) is expected to be less than 10%.

5.4 MSUN Model for Circuit Simulators

The surface potential based version of the MSUN model will be presented that encompasses all regions of MOSFET operation and would be suitable for circuit simulators. The preliminary MSUN model expressions were deduced earlier for linear-strong inversion region of operation and summarized as,

$$S_{I_d}(f) = \frac{1}{L^2}\int_0^L S_{\Delta I_d}(x,f)\Delta x dx \tag{5.15}$$

$$S_{\Delta I_d}(x,f) = \left[\frac{I_d}{W\Delta x}\left(\frac{R}{N(x)} \pm \alpha_{sc}\mu_{eff}\right)\right]^2 S_{\Delta N_t}(x,f) \tag{5.16}$$

$$S_{\Delta N_t}(x,f)=\frac{4kTW\Delta x}{\omega}\left[\frac{N_{tIL0}\exp[\xi_{IL}(E_{fn}-E_i)]}{\gamma_{IL}\left(\omega\tau_0\right)^{(\beta_{IL}/\gamma_{IL})}}\int_{\omega\tau_0}^{\omega\tau_0\exp(\gamma_{IL}T_{IL})}\frac{u^{(\beta_{IL}/\gamma_{IL})}}{1+u^2}du+\left(\frac{N_{tHK0}\exp[\xi_{HK}(E_{fn}-E_i)]}{\gamma_{HK}\left[\omega\tau_0\exp(\gamma_{IL}T_{IL})\right]^{(\beta_{HK}/\gamma_{HK})}}\int_{\omega\tau_0\exp(\gamma_{IL}T_{IL})}^{\omega\tau_0\exp(\gamma_{HK}T_{HK}+\gamma_{IL}T_{IL})}\frac{u^{(\beta_{HK}/\gamma_{HK})}}{1+u^2}du\right)\right] \tag{5.17}$$

where, R in (5.16) was considered unity in the strong inversion region. In the next section, the total noise power spectral density as given above will be represented as the sum of individual power spectral densities originating from the constituent dielectrics. Later the noise expressions are re-formulated in terms of surface potential related variables. Finally, the MSUN model is presented in a form that is suitable for circuit simulators. For convenience, $N(x) = N$ will be used from here on.

Refined Form of S_{Id}:

The total power spectral density $S_{I_d}(f)$ is expressed in a suitable manner before incorporating the surface potential related variables. At first, substitution of (5.16) and (5.17) in (5.15) gives:

$$S_{I_d}(f)=\frac{2kTI_d^{\,2}}{\pi L^2Wf}\int_0^L([R/N]\pm\alpha_{sc}\mu_{eff})^2\left[\frac{N_{tIL0}\exp[\xi_{IL}(E_{fn}-E_i)]}{\gamma_{IL}\left(\omega\tau_0\right)^{(\beta_{IL}/\gamma_{IL})}}\int_{\omega\tau_0}^{\omega\tau_0\exp(\gamma_{IL}T_{IL})}\frac{u^{(\beta_{IL}/\gamma_{IL})}}{1+u^2}du+\frac{N_{tHK0}\exp[\xi_{HK}(E_{fn}-E_i)]}{\gamma_{HK}\left[\omega\tau_0\exp(\gamma_{IL}T_{IL})\right]^{(\beta_{HK}/\gamma_{HK})}}\int_{\omega\tau_0\exp(\gamma_{IL}T_{IL})}^{\omega\tau_0\exp(\gamma_{HK}T_{HK}+\gamma_{IL}T_{IL})}\frac{u^{(\beta_{HK}/\gamma_{HK})}}{1+u^2}du\right]dx \tag{5.18}$$

The total noise power spectral density in (5.18) can be written as the sum of noise power spectral densities due to high-k and interfacial layers:

$$S_{I_d}(f) = S_{I_d 1}(f) + S_{I_d 2}(f) \tag{5.19}$$

where,

$$S_{I_d 1}(f) = \frac{2kTI_d^{\,2}}{\pi L^2 Wf} \int_0^L ([R/N] \pm \alpha_{sc}\mu_{eff})^2 \left[\frac{N_{tHK0} \exp[\xi_{HK}(E_{fn} - E_i)]}{\gamma_{HK}\left[\omega\tau_0 \exp(\gamma_{IL} T_{IL})\right]^{(\beta_{HK}/\gamma_{HK})}} \int_{\omega\tau_0 \exp(\gamma_{IL}T_{IL})}^{\omega\tau_0 \exp(\gamma_{HK}T_{HK}+\gamma_{IL}T_{IL})} \frac{u^{(\beta_{HK}/\gamma_{HK})}}{1+u^2} du \right] dx \tag{5.20}$$

$$S_{I_d 2}(f) = \frac{2kTI_d^{\,2}}{\pi L^2 Wf} \int_0^L ([R/N] \pm \alpha_{sc}\mu_{eff})^2 \left[\frac{N_{tIL0} \exp[\xi_{IL}(E_{fn} - E_i)]}{\gamma_{IL}\left(\omega\tau_0\right)^{(\beta_{IL}/\gamma_{IL})}} \int_{\omega\tau_0}^{\omega\tau_0 \exp(\gamma_{IL}T_{IL})} \frac{u^{(\beta_{IL}/\gamma_{IL})}}{1+u^2} du \right] dx \tag{5.21}$$

In (5.20) and (5.21), β_{HK} and β_{IL} are functions of channel potential (given by $(V_d/L)x$) due to the terms V_{gHK} and V_{gIL} as defined earlier. Now, neglecting the channel potential dependence on the position along the channel, the double integral with respect to *dx* can be simplified as shown below.

Defining,

$$Y_1 = \left[\frac{1}{\gamma_{HK}\left[\omega\tau_0 \exp(\gamma_{IL} T_{IL})\right]^{(\beta_{HK}/\gamma_{HK})}} \int_{\omega\tau_0 \exp(\gamma_{IL}T_{IL})}^{\omega\tau_0 \exp(\gamma_{HK}T_{HK}+\gamma_{IL}T_{IL})} \frac{u^{(\beta_{HK}/\gamma_{HK})}}{1+u^2} du \right] \tag{5.22}$$

$$Y_2 = \left[\frac{1}{\gamma_{IL}\left(\omega\tau_0\right)^{(\beta_{IL}/\gamma_{IL})}} \int_{\omega\tau_0}^{\omega\tau_0 \exp(\gamma_{IL}T_{IL})} \frac{u^{(\beta_{IL}/\gamma_{IL})}}{1+u^2} du \right] \tag{5.23}$$

the noise spectra can be given as,

$$S_{I_d 1}(f) = \frac{2kTI_d^{\,2} Y_1}{\pi L^2 Wf} \int_0^L (1 \pm \alpha_{sc}\mu_{eff} \frac{N}{R})^2 [R/N]^2 \left[N_{tHK0} \exp[\xi_{HK}(E_{fn} - E_i)]\right] dx \tag{5.24}$$

$$S_{I_d 2}(f) = \frac{2kTI_d{}^2 Y_2}{\pi L^2 W f} \int_0^L (1 \pm \alpha_{sc}\mu_{eff}\frac{N}{R})^2 [R/N]^2 \left[N_{tIL0} \exp[\xi_{IL}(E_{fn} - E_i)]\right] dx \qquad (5.25)$$

Surface Potential Version of MSUN model:

In this section, the MSUN model expressions are transformed to include surface potential related variables. Starting with the basic drain current equation for a MOSFET,

$$I_d = -W\mu_{eff} Q_{inv} \frac{dV}{dx} \qquad (5.26)$$

or

$$dx = \frac{-W\mu_{eff} Q_{inv}}{I_d} dV \qquad (5.27)$$

The differential voltage along the channel can be written as,

$$dV = \frac{dV}{d\psi_s}\frac{d\psi_s}{dN} dN = \frac{dV}{d\psi_s}\frac{q}{C_{inv}} dN \qquad (5.28)$$

From [112],

$$\frac{dV}{d\psi_s} \approx \frac{N + N^*}{N} \qquad (5.29)$$

where, $N^* = \frac{kT}{q^2}\left(C_g + C_b\right) \approx -\frac{\phi_t}{q} C_{inv}$ [112]. Hence,

$$dV = \frac{N + N^*}{N}\frac{q}{C_{inv}} dN = \frac{\phi_t}{N^*}\left(\frac{N + N^*}{N}\right) dN \qquad (5.30)$$

and,

$$dx = \frac{-W\mu_{eff} q}{I_d}\frac{\phi_t}{N^*}\left(N + N^*\right) dN \qquad (5.31)$$

The exponential terms in (5.24) and (5.25) represent the trap density variation with respect to energy and appear inside the integral due to the variation of quasi-Fermi

level (or energy and surface potential) along the channel. Now, $(E_{fn} - E_i) = q(\psi_s - \phi_F)$ where, $\phi_F = \phi_t \ln(\frac{N_I}{n_i})$, $\phi_t = kT/q$, N_I is the substrate doping and ψ_s is the surface potential that varies along the channel. For ease in computation, ψ_s that is implicit in the exponential terms is replaced by the surface potential mid-point value given by $\psi_m = \frac{\psi_{ss} + \psi_{sd}}{2}$ [113]. Here, ψ_{ss} and ψ_{sd} are source and drain side surface potentials. Accordingly, the exponential terms can be taken out of the integrals in (5.24) and (5.25). It should be noted that this surface potential mid-point approximation still preserves the energy dependence of dielectric trap density since ψ_m still depends on the applied gate bias. Additionally, an adjustment has to be made for proper description of noise in the weak inversion region by including-

$$R = \frac{\partial \Delta N}{\partial \Delta N_{ot}} = -\frac{N}{N + N^*} \tag{5.32}$$

Noise for Gradual Channel Approximation (Linear Region): -

The charge density at the source and drain ends is incorporated in Surface-Potential (SP) model [113] following the symmetric linearization about the mid-point surface potential charge so that,

$$N_L = N_m - \frac{\Delta N}{2} \qquad \text{and} \qquad N_0 = N_m + \frac{\Delta N}{2} \tag{5.33}$$

provide the respective drain side and source side charges with N_m being the charge corresponding to ψ_m. ΔN is the charge difference between the source and drain regions.

Substituting (5.31), (5.32) and (5.33) along with the above mentioned mid-point surface potential approximation, (5.24) and (5.25) become,

$$S_{I_d1}(f)=\frac{2q^2\phi_t^{\,2}I_dY_1\mu_{eff}N_{tHK0}\left[\exp[\xi'_{HK}(\psi_m-\phi_F)]\right]}{\pi L^2 fN^*}\int_{N_m-\frac{\Delta N}{2}}^{N_m+\frac{\Delta N}{2}}(1\pm\alpha_{sc}\mu_{eff}\frac{N}{R})^2.\frac{1}{N+N^*}dN \quad (5.34)$$

$$S_{I_d2}(f)=\frac{2q^2\phi_t^{\,2}I_dY_2\mu N_{tIL0}\left[\exp[\xi'_{il}(\psi_m-\phi_F)]\right]}{\pi L^2 fN^*}\int_{N_m-\frac{\Delta N}{2}}^{N_m+\frac{\Delta N}{2}}(1\pm\alpha_{sc}\mu_{eff}\frac{N}{R})^2.\frac{1}{N+N^*}dN \quad (5.35)$$

where, $\xi'_{HK}=q\xi_{HK}$, $\xi'_{IL}=q\xi_{IL}$; μ_{eff} is replaced by μ and α_{sc} is replaced by α for consistency with SP model [112].

From [54,112,114], the following approximation is made-

$$(1\pm\alpha\mu\frac{N}{R})^2=A+BN+CN^2 \quad (5.36)$$

so that,

$$\frac{A+BN+CN^2}{N+N^*}=\frac{A}{N+N^*}+B(1-\frac{N^*}{N+N^*})+C(N-N^*+\frac{N^{*2}}{N+N^*}) \quad (5.37)$$

Further, transforming mobility in terms of SP parameters [112],

$$\frac{\beta}{G_{vsat}}=\frac{W}{L}\mu_0C_{ox}\frac{1}{G_{vsat}}=\frac{W}{L}C_{ox}\mu \quad (5.38)$$

Using (5.37) and (5.38), we have,

$$S_{I_d1}(f)=\frac{2q^2\phi_t^{\,2}I_dY_1\beta N_{tHK0}\left[\exp[\xi'_{HK}(\psi_m-\phi_F)]\right]}{\pi C_{ox}WLfN^*G_{vsat}}$$
$$\left[\left(A-N^*B+N^{*2}C\right)\cdot\ln\left(\frac{N_m^{\,*}+\frac{\Delta N}{2}}{N_m^{\,*}-\frac{\Delta N}{2}}\right)+\Delta N\left(B+C\left(N_m^{\,*}-2N^*\right)\right)\right] \quad (5.39)$$

$$S_{I_d 2}(f) = \frac{2q^2\phi_t^{\,2} I_d Y_2 \beta N_{tIL0}\left[\exp[\xi'_{IL}(\psi_m - \phi_F)]\right]}{\pi C_{ox} WLf N^* G_{vsat}} \left[\left(A - N^* B + N^{*2} C\right)\cdot \ln\left(\frac{N_m^{\,*} + \frac{\Delta N}{2}}{N_m^{\,*} - \frac{\Delta N}{2}}\right) + \Delta N\left(B + C\left(N_m^{\,*} - 2N^*\right)\right)\right] \quad (5.40)$$

where, $N_m^{\,*} = N_m + N^*$, $A=1$ and $C=B^2/4$.

The expressions (5.39) and (5.40) represent the low frequency noise originating from the high-k and interfacial layers for MOSFETs operating in weak, moderate or strong inversion regions and are valid until channel pinch-off occurs at high drain voltages.

Noise for Pinched-off /Saturation region -

For high drain voltages ($V_d > V_{dsat}$), the graduate channel approximation falls apart and the channel current saturates and causes channel length modulation (shortening) additionally. Representing the distance of the pinch-off point (or velocity saturation point for short channel devices) from the drain as ΔL, the inverted channel length from the source to the pinch-off point will be (L- ΔL). Thus, the integrals in (5.24) and (5.25) need to be evaluated independently for the channel region and the ΔL part as shown below.

$$S_{I_d 1}(f) = \frac{2kTI_d^{\,2} Y_1}{\pi L^2 W f}\left[\int_0^{L-\Delta L} (1 \pm \alpha\mu \frac{N}{R})^2 [R/N]^2 \left[N_{tHK0} \exp[\xi_{HK}(E_{fn} - E_i)]\right] dx + \int_{L-\Delta L}^{L} (1 \pm \alpha\mu \frac{N}{R})^2 [R/N]^2 \left[N_{tHK0} \exp[\xi_{HK}(E_{fn} - E_i)]\right] dx\right] \quad (5.41)$$

$$S_{I_d 2}(f) = \frac{2kTI_d{}^2 Y_2}{\pi L^2 Wf}\left[\begin{array}{l}\int_0^{L-\Delta L}(1 \pm \alpha\mu\frac{N}{R})^2[R/N]^2\left[N_{tIL0}\exp[\xi_{IL}(E_{fn}-E_i)]\right]dx \\ +\int_{L-\Delta L}^{L}(1 \pm \alpha\mu\frac{N}{R})^2[R/N]^2\left[N_{tIL0}\exp[\xi_{IL}(E_{fn}-E_i)]\right]dx\end{array}\right] \quad (5.42)$$

The noise expressions for the inverted channel region will be exactly identical to (5.39) and (5.40). However, in the calculation of ψ_m, ψ_{sd} is now replaced by the surface potential at the pinch-off (or velocity saturation) point (ψ_{sat}). The quasi-Fermi level in the pinch-off (or velocity saturation) region is assumed to be uniform at a value equal to that of the pinch-off point so that the carrier density would be given by ($N_m - \Delta N/2$). Thus, the noise expression for this region can be given as,

$$S_{I_d 1\Delta L}(f) = \frac{2kTI_d{}^2 Y_1 N_{tHK0}\left[\exp[\xi'_{HK}(\psi_{sat}-\phi_F)]\right]}{\pi L^2 Wf}\Delta L\left[\frac{A+B\left(N_m-\frac{\Delta N}{2}\right)+C\left(N_m-\frac{\Delta N}{2}\right)^2}{\left(N_m{}^*-\frac{\Delta N}{2}\right)^2}\right] \quad (5.43)$$

$$S_{I_d 2\Delta L}(f) = \frac{2kTI_d{}^2 Y_2 N_{tIL0}\left[\exp[\xi'_{IL}(\psi_{sat}-\phi_F)]\right]}{\pi L^2 Wf}\Delta L\left[\frac{A+B\left(N_m-\frac{\Delta N}{2}\right)+C\left(N_m-\frac{\Delta N}{2}\right)^2}{\left(N_m{}^*-\frac{\Delta N}{2}\right)^2}\right] \quad (5.44)$$

Using $G_{\Delta L} = \left(1-\frac{\Delta L}{L}\right)$, the noise power spectral density expression including both the channel and pinch-off (or velocity saturation) region will be,

$$S_{I_d 1}(f) =$$

$$\frac{2q^2\phi_t{}^2 I_d Y_1 \beta N_{tHK0}\left[\exp[\xi'_{HK}(\psi_m - \phi_F)]\right]}{\pi C_{ox} WLfN^* G_{vsat}}\left[\left(A - N^*B + N^{*2}C\right)\cdot \ln\left(\frac{N_m{}^* + \frac{\Delta N}{2}}{N_m{}^* - \frac{\Delta N}{2}}\right) + \Delta N\left(B + C\left(N_m{}^* - 2N^*\right)\right)\right]$$

$$+\frac{2kTI_d{}^2 Y_1 N_{tHK0}\left[\exp[\xi'_{HK}(\psi_{sat} - \phi_F)]\right]}{\pi LWf}\left(1 - G_{\Delta L}\right)\left[\frac{A + B\left(N_m - \frac{\Delta N}{2}\right) + C\left(N_m - \frac{\Delta N}{2}\right)^2}{\left(N_m{}^* - \frac{\Delta N}{2}\right)^2}\right]$$

(5.45)

$$S_{I_d 2}(f) =$$

$$\frac{2q^2\phi_t{}^2 I_d Y_2 \beta N_{tIL0}\left[\exp[\xi'_{IL}(\psi_m - \phi_F)]\right]}{\pi C_{ox} WLfN^* G_{vsat}}\left[\left(A - N^*B + N^{*2}C\right)\cdot \ln\left(\frac{N_m{}^* + \frac{\Delta N}{2}}{N_m{}^* - \frac{\Delta N}{2}}\right) + \Delta N\left(B + C\left(N_m{}^* - 2N^*\right)\right)\right]$$

$$+\frac{2kTI_d{}^2 Y_2 N_{tIL0}\left[\exp[\xi'_{IL}(\psi_{sat} - \phi_F)]\right]}{\pi LWf}\left(1 - G_{\Delta L}\right)\left[\frac{A + B\left(N_m - \frac{\Delta N}{2}\right) + C\left(N_m - \frac{\Delta N}{2}\right)^2}{\left(N_m{}^* - \frac{\Delta N}{2}\right)^2}\right]$$

(5.46)

Finally, the total noise power spectral density for all regions of multi-gate dielectric stack MOSFET operation is given by the sum of (5.45) and (5.46) i.e.,

$$S_{I_d}(f) = S_{I_d 1}(f) + S_{I_d 2}(f) \tag{5.47}$$

Here, the parameters required to effectively express the noise power spectral density are: $A=1$ and $C=B^2/4$, $\xi'_{HK} = q\xi_{HK}$ and $\xi'_{IL} = q\xi_{IL}$, λ_{HK} and λ_{IL}, η_{HK} and η_{IL}, N_{tHK0} and N_{tIL0}.

In practice, MOSFETs have an interfacial dielectric layer that is about 0.6-1 nm thick, which makes the noise due to high-k layer dominant (few orders of magnitude

higher than the interfacial layer part) at low frequencies. Thus, choice of N_{tIL0}, ξ_{IL}, λ_{IL}, η_{IL} would not make a difference and can be omitted, there by limiting the total number of parameters to 5 as shown:

(1) $A=1$ and $C=B^2/4$ (2) $\xi'_{HK} = q\xi_{HK}$ (3) λ_{HK} (4) η_{HK} (5) N_{tHK0}

5.5 Summary

The Multi-Stack Unified Noise model that is based on correlated carrier number and mobility fluctuations theory was derived to characterize the 1/f noise in the high-k/interfacial layer MOSFETs. The model is scalable with respect to the high-k/interfacial layer thickness, temperature, and applied bias. In addition, it takes various material properties into account such as energy barrier height differences between the constituent gate dielectric layers, and dielectric trap density distribution with respect to Si band gap energy and location in the dielectric. It is shown to be in excellent agreement with the experimental data. Furthermore, the model was re-written in terms of surface potential based variables to be incorporated in the circuit simulators.

CHAPTER 6

SUMMARY AND CONCLUSIONS

In summary, 1/f noise in hafnium based high-k gate dielectric MOSFETs was studied. Both n and p-type MOSFETs, with poly-Si or dual metal gates, were considered. In poly-Si gate MOSFETs, the high-k dielectrics were 5.5nm HfO_2 (by MOCVD), 3 nm Al_2O_3 (ALD)/ 3 nm HfO_2 (ALD) or $HfAlO_x$ (ALD). These were deposited on top of either 1 nm or 4 nm SiO_2 interfacial layer (RCA process). TaSiN metal gate (n-channel MOSFETs) was used in conjunction with 2.7 nm ALD HfO_2 that was deposited on top of either 1 nm thermal SiO_2 by SRPO method or SiO_2 (1 nm)from RCA pre-clean process. In addition, TiN metal gate/ 2.7 nm ALD HfO_2/ 1 nm RCA SiO_2 gate stack was considered for p-type MOSFETs.

The validity of the two possible 1/f noise causing mechanisms, bulk mobility fluctuations due to lattice scattering or carrier number fluctuations due to trapping/de-trapping of channel carriers, was established at first by examining the noise data in the 78-350K range. It was concluded that the traps in the high-k gate stack caused the trapping/de-trapping of channel carriers via equal energy tunneling process thereby causing fluctuations in both channel carrier number and carrier mobility in a correlated manner. Consequently, based on the number fluctuations theory, the normalization of noise was done to make a valid comparison of inherent noise in MOSFETs with

different dimensions. In addition, the noise parameter extraction was done in the initial part of the work using the Unified Flicker Noise Model.

From room temperature noise characteristics of poly-Si gate MOSFETs, it was found that the normalized noise and the extracted dielectric trap density (using Unified Model) were higher in high-k devices compared to that for conventional SiO_2 MOSFETs. In addition, the noise magnitude was lower in MOSFETs with 4 nm thick SiO_2 when compared to devices with 1 nm SiO_2 interfacial layer. It was thereby concluded that the high-k gate dielectrics are more defective. Furthermore, the Coulomb scattering mechanism was found to be more pronounced in these high-k devices that resulted in severe degradation of carrier mobility. Better overall performance was exhibited by HfO_2 devices in n-channel MOSFETs while no clear conclusion could be drawn in p-channel MOSFETs. Additionally, from the threshold voltage characteristic, the presence of interface states at the poly-Si gate and high-k interface was indicated.

In general, the MOSFETs with TaSiN, TiN metal gate/HfO_2 gate stack exhibited lower noise magnitude and higher mobility values than their poly-Si gated counterparts. The lower gate dielectric defect density in the former was attributed to the processing conditions existing during the gate electrode formation. In TaSiN MOSFETs, the Coulomb scattering coefficient as obtained from the noise data was found to be lower in SRPO devices compared to RCA devices. This would imply a higher effective mobility for the former, which was confirmed by the mobility characteristics obtained from the split C-V measurements. Thus, evidence is presented that the MOSFET performance depends on the process employed in the deposition of the interfacial layer. In general, p-

type MOSFETs with HfO_2 gate dielectric were found to exhibit higher noise compared to n-type counterparts. This indicates that the trap density in HfO_2 is higher in the lower mid-gap region of Si than the upper mid-gap region.

Later, the 'Multi-Stack Unified Noise' model (MSUN) that is based on correlated carrier number and mobility fluctuations theory was proposed to better model/characterize the 1/f noise in multi-layered high-k MOSFETs. This model considers the distribution of the trap density profile with respect to Si band gap energy and location in the gate dielectric layers along with other material properties of the constituent gate dielectrics. Additionally, the model is scalable with respect to the high-k/interfacial layer thickness, temperature, and applied bias. The MSUN model is shown to be in excellent agreement with the experimental data obtained on TaSiN/HfO_2/(SRPO or RCA)SiO_2 MOSFETs in the 78-350 K range. Finally, the MSUN model was expressed in terms of surface potential based variables in order to be incorporated in the circuit simulators.

APPENDIX A

SET-UP FOR GATE TO BULK AND TOTAL GATE CAPACITANCE MEASUREMENTS

A.1 Gate to Bulk Capacitance Measurement

Figure A-1 depicts the configuration to measure the gate to bulk capacitance. The gate and the substrate are connected to the Low and High ends of the LCR meter (HP 4284A), respectively. The drain and source terminals are shorted to the guard terminal so as to bypass the inversion layer charge. The parasitic capacitance, due to the coupling between gate contact pad and substrate via field oxide [115], is obtained as the bias independent non-zero capacitance in the inversion region and is subtracted from the C_{gb} curve for the entire bias range. From the resulting C_{gb} vs. V_g curve, the bulk charge density can be extracted using, $Q_{bulk} = \int_{-V_g}^{\infty} C_{gb}(V_g)\, dV_g$.

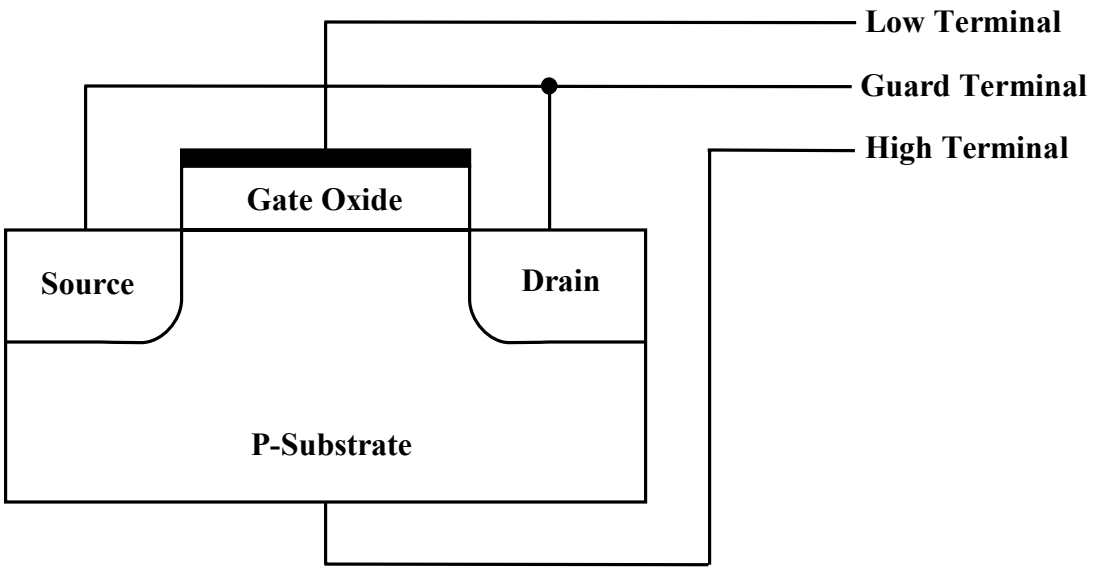

Figure A-1 Set-up for gate to bulk capacitance measurement (C_{gb}). The Low end of the LCR meter must be connected to the gate terminal. The High end is connected to the substrate while drain and source terminals were shorted to the ground so that only bulk charge was counted [67].

The vector ammeter is at the Low end of the LCR meter and is sensitive to noise and the substrate might be electrically coupled to the wafer chuck. Thus, for configurations involving the substrate terminal, it is always recommended to connect the High terminal of the LCR meter to the substrate. This would minimize the chuck-related noise in the measurement.

A.2 Total Gate Capacitance Measurement

Figure A-2 shows the connection diagram for the total gate capacitance measurement. The gate is connected to the Low end of the LCR meter while the drain, source and substrate terminals are shorted to the High end of HP4284A. The noise interference from chuck to the capacitance measurement is minimized here.

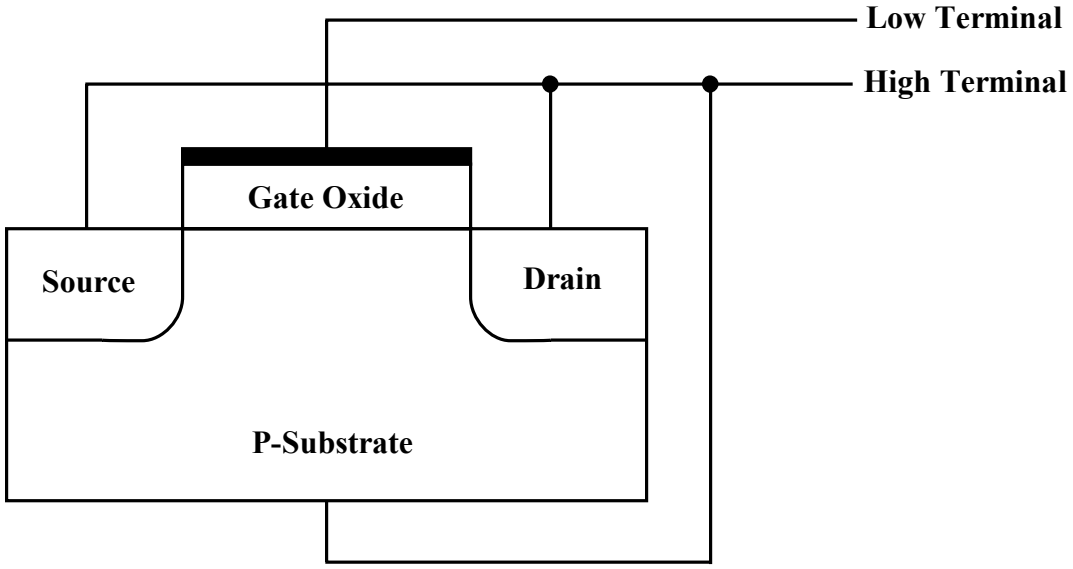

Figure A-2 Set-up for total gate capacitance measurement (C_g). The gate must be connected to the Low terminal in this configuration to minimize chuck-related noise in the measurement [116].

The sum total of parasitic capacitances as obtained from C_{gc} and C_{gb} measurements needs to be subtracted from total gate capacitance curve in the considered bias range to arrive at the actual MOSFET gate capacitance. It can be verified that $C_g = C_{gb} + C_{gc}$.

It should be noted that the configurations shown here are for n-type devices with a p-substrate. The High and Low terminal connections may have to be reversed while performing measurements on p-type devices.

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