OPTIMIZED CLASS-E RF POWER AMPLIFIER DESIGN IN BULK CMOS

by

TAO WANG

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ABSTRACT

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The rapid growth of telecommunication markets calls for the integration of complicated wireless applications into one single chip. However, even with the great advance in semiconductor technology, building good monolithic RF power amplifiers with CMOS processes remains challenging due to the inherent parasitic losses of CMOS. A lot of researches have been done on investigating various factors on the performance of the Class-E amplifiers, but few of them presented systematic analyses for the design in CMOS. The existing design methods are either too complicated or less accurate for RF CMOS applications.

The aim of this thesis is to provide an optimized yet explicit design method for the Class-E amplifiers using the CMOS technology. After a careful analysis of the

characteristics of deep-submicron CMOS, low quality inductors and non-ideal transistors appear to be the biggest constraints in monolithic Class-E power amplifier design. Taking the finite DC feed inductor into consideration, a simple but accurate numerical design method is proposed in this thesis by applying polynomial interpolation to a group of managed theoretical data. This method could produce optimized load networks for the cases with a finite DC feed inductance. Combining this method with a practical design strategy for non-ideal transistors of finite conductance and parasitic capacitances, a two-staged Class-E power amplifier is implemented in 0.18μm CMOS technology. The simulation results show that this power amplifier can deliver at least a 23dBm power to a 50Ohm load with 73.5% PAE at 2.4GHz. The good agreement between simulation results and the predicted values validates this design method and its applications in CMOS. This method could be applied to general design cases.

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CHAPTER 1

INTRODUCTION

1.1 Motivation

The trend in wireless communications nowadays demands a wireless standard that is capable of supporting a variety of services including voice, video and other multimedia, which in turn calls for low cost handheld electronics of high integration, high power efficiency yet with great performance. With the advance of Complementary Metal-Oxide Semiconductor (CMOS) technology, especially with the down-scaling of the CMOS technology, complicated high-speed digital modules can be integrated into one small chip, leading to high integration and low power consumption in the digital section. On the other hand, the radio frequency section of a wireless terminal continues to dominate the power consumption. And building monolithic Radio Frequency (RF) transceivers remains very challenging even with the aid of state-of-art CMOS technologies. Therefore, to design and implement monolithic high efficient transceivers in low-cost CMOS are the key to improving the performance of battery-operated handheld electronics.

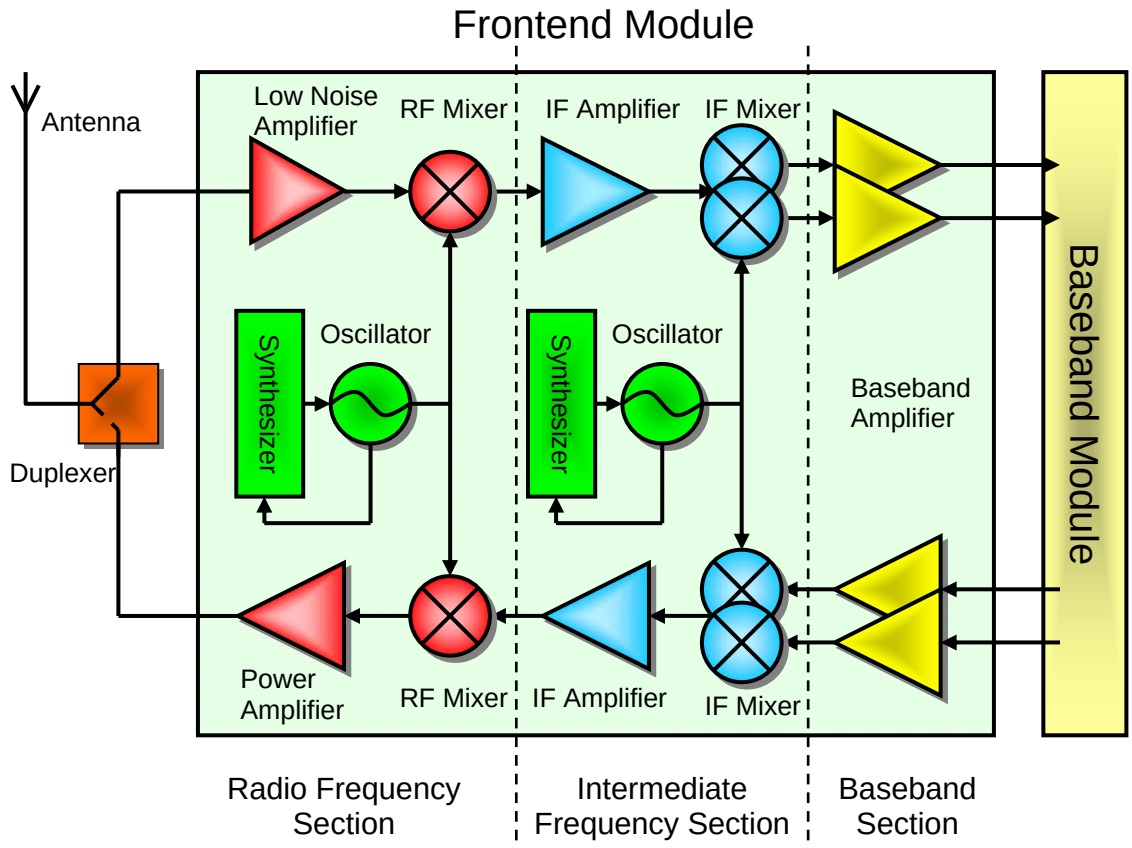

Figure 1.1 Block diagram of a typical RF transceiver

Figure 1.1 shows a typical architecture of RF frontend, which typically consists of a Radio Frequency section, an Intermediate Frequency section, and a Baseband section. In the transceiver, the power amplifier makes the major contribution to the power consumption of the transceiver. In the past decade, many researchers endeavored to improve power efficiencies for power amplifiers using different architectures and various semiconductor technologies. Among the high efficient power amplifiers, Class-E is an attractive option due to its high efficiency but low complexity. A great variety of theoretical and optimized design methods for Class-E amplifiers have been

introduced. But few comprehensive analyses have been presented for practical design in state-of-art bulk CMOS technologies. Due to the inherent limits of bulk CMOS, traditional analytical results are no longer hold. Conventional design methods either produce significant discrepancies in circuit parameters or become too complicated to apply. Therefore it is necessary to generate a better and simpler design method. The aim of this thesis is to develop a practical design method for Class-E power amplifier in bulk CMOS.

1.2 Thesis Organization

Chapter 2 first provides an overview of power amplifiers, and then introduces some basic concepts about power amplifiers including classifications of amplifiers, characteristics, and evaluation standards. Chapter 3 briefly introduces some important features of state-of-art CMOS processes. In Chapter 4, several important design considerations in Class-E amplifier design are discussed, and then a practical design method is presented. Based on this method, in Chapter 5, a prototype design in CMOS is explained in detail, followed by simulation results and discussions. Finally, conclusions of this work, as well as some suggestions for future study, are provided in Chapter 6.

CHAPTER 2

FUNDAMENTALS OF POWER AMPLIFIERS

2.1 Introduction

A typical single-stage power amplifier illustrated in Figure 2.1 consists of at least four parts: a power supply network, input and output matching networks, input and output bias networks and an active device. A power supply network provides desired voltage supply and/or current source. The input and output matching networks convert the source and load to certain impedances so that the amplifier can achieve better overall performance at desired frequencies. Input and output matching networks typically consist of only passive components. An active device ideally acts as a current/voltage controlled current/voltage source, or just some sort of switch. The input and output bias networks determine the operating point of the active device and output signal level, respectively. The same active device can work at different modes if its operating point is intentionally set to different values. The source and load are the previous and next stages, respectively, in a transceiver, typically of $50\,\Omega$ impedance.

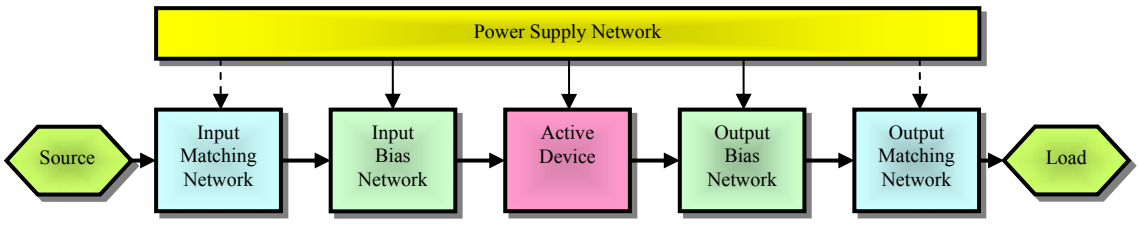

Figure 2.1 Block diagram of generalized single-stage power amplifier

Power delivered to the load, efficiency, gain, linearity and bandwidth are the most important indexes considered in power amplifier design, which are briefly introduced in the following sections.

2.2 Key Concepts in Power Amplifier Design

2.2.1. Power Calculation

Power is one essential figure for evaluating the capability of power amplifiers. Two power concepts are widely used in PA design. One is the DC power consumption, which is defined as:

$$P_{DC} = V_{DC} I_{DC} \tag{2.1}$$

The other is AC power, which is the average power of signals varying over a certain period. For a sinusoidal signal, AC power is defined as the product of the root mean square values of voltage and current. The RF power delivered to the load R is defined as:

$$P_O = \frac{1}{2}\mathrm{Re}\left\{V_O I_O^*\right\} = \frac{1}{2}\left|I_O^2\right|\mathrm{Re}\left\{Z_L\right\} = \frac{1}{2}\frac{\left|V_O^2\right|}{\mathrm{Re}\left\{Z_L\right\}} \tag{2.2}$$

In a RF system, the power obtained from a certain source is expressed as:

$$P_{AVA} = \frac{\left|V_G^2\right|}{8\,\mathrm{Re}\left\{Z_G\right\}} \tag{2.3}$$

2.2.2. Power Gain

There are many definitions of gain in RF circuit design, such as power gain, available gain, exchangeable gain, insertion gain and transducer power gain. The most commonly used gain definition in power amplifier design is the power gain, which is

defined in [1] as the ratio of power dissipated in the load, Z_L, to the power delivered to the input of the amplifier. The power gain is mathematically expressed as:

$$G_P = \frac{P_O}{P_{IN}} \tag{2.4}$$

Another useful gain definition is the transducer power gain, which is the ratio of the power delivered to the load to the available power from the source:

$$G_T = \frac{P_O}{P_{AVA}} \tag{2.5}$$

2.2.3. Efficiency

Efficiency is used to measure the quality of an amplifier in converting input supply energy to output usable energy. Higher efficiency means less power loss in the amplifier. Efficiency is a very important merit for evaluating the overall performance of power amplifiers, especially for switching power amplifiers, the power gain of which may not be meaningful. There are several kinds of efficiencies in use: drain/collector efficiency and power added efficiency are the most commonly used; sometimes overall efficiency and long-term mean efficiency should be applied if some other costs like that of the cooling systems are comparable to the price of the system and need to be taken into consideration [2].

The drain/collector efficiency is defined as:

$$\eta = \frac{P_O}{P_{DC}} \tag{2.6}$$

This efficiency definition does not provide information about the input. An amplifier of low power gain could exhibit high efficiency. The power added efficiency,

on the other hand, takes the input driving power into account and thus can better evaluate the performance of some high-efficiency power amplifiers. The power added efficiency is defined as:

$$PAE = \frac{P_O - P_{IN}}{P_{DC}} = \eta\left(1 - \frac{1}{G_P}\right) \tag{2.7}$$

2.2.4. Linearity

Linearity is defined as the property of a system in which the outputs are scales of the inputs without introducing new elements. It is another very crucial specification for power amplifiers in practice. For example, wireless communication standards supporting high-speed data rate services usually employ PSK and QAM modulations for higher spectrum efficiency, and hence demand for good linearity in power amplifiers. In practice, acceptable linearity could be achieved via using linear amplifiers or employing some linearity enhancement techniques to switching amplifiers. The typical linearity enhancement techniques include applying high profile technologies or adding some compensation circuits. As a result, the system complexity and the cost increase dramatically. Therefore, for economic reasons, linearity and efficiency have to be traded off in practical power amplifier designs.

Nonlinearity is usually caused by the undesired features of the active device in an amplifier. Nonlinear effects in active devices can be classified into two categories: strongly and weakly nonlinear effects [3]. Strongly nonlinear effects are introduced by the limiting behavior of the transistor such as cut-off, pinch-off, saturation and some other secondary effects. They can be predicted using device models based on I-V

curve-fitted equations. The other category, weakly nonlinear effects, can be examined by analyzing the output of the amplifier using sinusoidal signals as input. Several useful concepts for assessing weakly nonlinear effects are explained in the following sections.

In general, the nonlinear system response is described by a Taylor series:

$$y(t) = a_1 x(t) + a_2 x^2(t) + a_3 x^3(t) + \cdots \tag{2.8}$$

Substitute $x(t) = A\cos\omega t$ into the above expression, then the corresponding output can be given in the following third order approximation:

$$\begin{aligned} y(t) \quad &= a_1 A\cos\omega t + a_2 A^2 \cos^2 \omega t + a_3 A^3 \cos^3 \omega t \\ &= \frac{a_2 A^2}{2} + (a_1 A + \frac{3a_3 A^3}{4})\cos\omega t + \frac{a_2 A^2}{2}\cos 2\omega t + \frac{a_3 A^3}{4}\cos 3\omega t \end{aligned} \tag{2.9}$$

The equation above shows that the output comprises of three terms: DC, first-order and higher orders of the input frequency, the latter two of which are usually called "fundamental" term and "harmonics" term, respectively. It is observed that only the odd order (the third-order in this case) harmonic terms will appear in the interested frequency band, whereas the even order terms like the second-order harmonic could be removed by applying proper filters at the output.

Although the power series is useful for characterizing the behavior of nonlinear harmonics, it is only valid in a small operation zone around the DC operating point; the amplitudes and biasing levels of input and output signals pose limitations on this analytic method, especially in the case of large output signal. Moreover, this method is incapable of investigating phase distortions. Volterra series, a kind of complicated

power series with phase variables or memory effects, could be applied to explore the phase distortion effects if desired.

The 1-dB compression point is a widely-exploited merit of linearity. The 1-dB compression point of an amplifier refers to the output power level at which the transfer characteristic of the amplifier deviates from that of an ideal, linear, characteristic by 1 dB [3]. The 1-dB compression point describes the variation of the small-signal gain. The amplifier of the larger 1-dB compression point has a wider dynamic response range.

The concepts described above are based on monotone input signal. However, transceivers may use two or more working frequencies at the same time. In such case, one frequency element may have strong interference on another carrier, which is also known as cross-modulation. To investigate this effect, the typical method is the two-tone test, which applies the similar idea by feeding two carrier frequency signals of equal amplitude to reveal both amplitude and phase distortions in the amplifier. Substitute $x(t) = A_1 \cos \omega_1 t + A_2 \cos \omega_2 t$ into third-order approximation form of the system response, then the corresponding estimated output is

$$\begin{aligned} y(t) \quad &= a_1(A_1 \cos \omega_1 t + A_2 \cos \omega_2 t) \\ &+ a_2(A_1 \cos \omega_1 t + A_2 \cos \omega_2 t)^2 \\ &+ a_3(A_1 \cos \omega_1 t + A_2 \cos \omega_2 t)^3 \end{aligned} \tag{2.10}$$

Since the third order harmonics can be easily filtered out, here I only list the fundamental terms and intermodulation products:

$$\omega_1, \omega_2 \quad : \quad (a_1 A_1 + \frac{3}{4} a_3 A_1^3 + \frac{3}{2} a_3 A_1 A_2^2)\cos\omega_1 t + (a_1 A_2 + \frac{3}{4} a_3 A_2^3 + \frac{3}{2} a_3 A_2 A_1^2)\cos\omega_2 t$$

$$\omega_1 \pm \omega_2 : \quad a_2 A_1 A_2 \cos(\omega_1 + \omega_2)t + a_2 A_1 A_2 \cos(\omega_1 - \omega_2)t$$

$$2\omega_1 \pm \omega_2 : \quad \frac{3a_3 A_1^2 A_2}{4}\cos(2\omega_1 + \omega_2)t + \frac{3a_3 A_1^2 A_2}{4}\cos(2\omega_1 + \omega_2)t$$

$$2\omega_2 \pm \omega_1 : \quad \frac{3a_3 A_2^2 A_1}{4}\cos(2\omega_2 + \omega_1)t + \frac{3a_3 A_2^2 A_1}{4}\cos(2\omega_2 + \omega_1)t$$

The distortion products at $2\omega_2 - \omega_1$ and $2\omega_1 - \omega_2$ exist in the frequency band of interest and are hardly filtered out. The results of the two-tone test can be illustrated by third intercept point IP_3, which is defined as the interception of linear gain and third harmonic products.

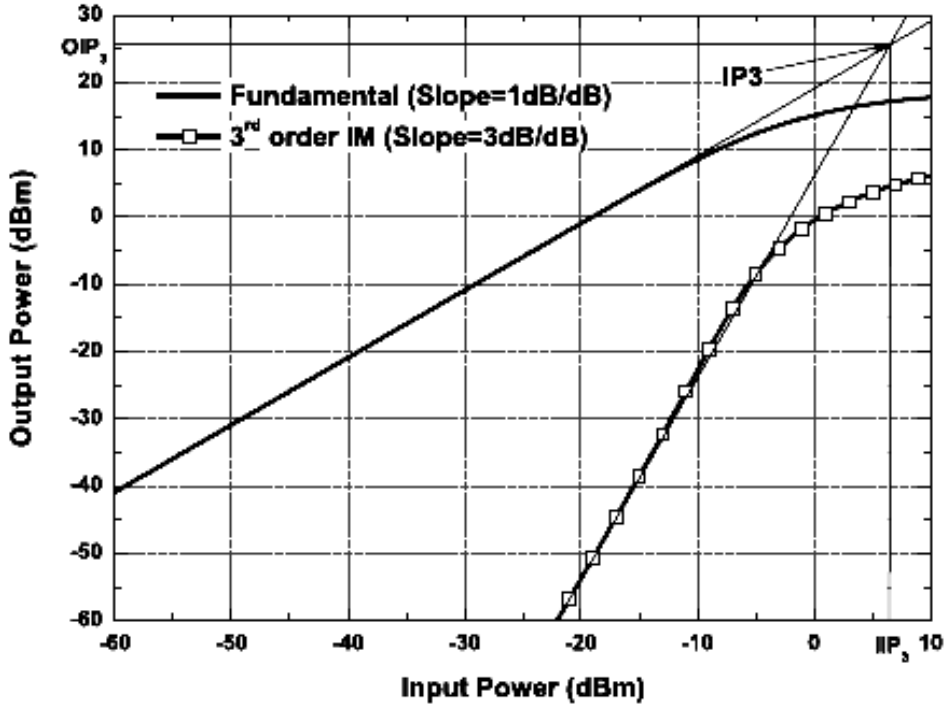

Figure 2.2 Illustration of third order interception point [4]

As for small-signal amplifiers, third-order nonlinearity is usually sufficient to describe these compression or saturation effects. But in power amplifiers, the fifth,

seventh, or even the ninth-degree terms become significant and may have to be considered in power amplifier design.

2.2.5. Bandwidth

Power amplifiers should be able to provide relatively constant performance in their desired bands. The bandwidth can be narrowband, wideband or ultra wideband. Amplifiers with wider operational bandwidths usually have lower gains. Narrowband power amplifiers are most widely used in recent wireless communication applications. Nevertheless, since supporting high speed data rate multimedia services has become a trend nowadays, power amplifiers of wideband and ultra wideband attract more and more attention.

2.3 An Overview of Classical Power Amplifiers

The basic specifications for power amplifier include output power level, device stress, gain, efficiency, linearity, bandwidth, form-factor and cost. Some of these design goals are in conflict with one another: gain vs. bandwidth, device stress vs. output power, linearity vs. efficiency, and high-profiled technologies vs. cost are the most common conflicts considered in power amplifier design. Designers have to make tradeoffs among these various specifications to obtain the optimized performance for different applications. To meet different demands, a variety of power amplifiers were invented to maximize certain features. These power amplifiers have either different circuit configurations or different working conditions. Power amplifiers are classified into several classes for practical reasons, although the boundaries between different classes are not very clear sometimes.

The most common classes are Classes A, AB, B, C, D, E, F, G, S, and H. Each class of power amplifiers offers some advantages over another. For example, Class-A has better linearity but poorer efficiency than other classes. Hybrid amplifiers, such as Classes AB, CE, DE, E/F amplifiers, usually enjoy the benefits of more than two basic classes. Based on the most important tradeoff in power amplifier design, efficiency and linearity, power amplifiers can be further divided into two groups: linear amplifiers and nonlinear (constant envelope) amplifiers. Classes A, AB, and B amplifiers belong to linear amplifiers, while Classes C, D, E, F, G, S, and H amplifiers are nonlinear since they make no attempt to preserve the wave shapes of input signal at the output.

Based on the working style of the active devices, power amplifiers can also be categorized into two groups, transconductance and switching-mode, which are shown in Figure 2.3. Transconductance amplifiers include the linear amplifiers and Class-C because they share the similar topology and employ the active device as a voltage controlled current source. On the other hand, Classes D, E, F, G, H and S belong to switching-mode amplifiers due to the fact that the active device could be ideally viewed as switches.

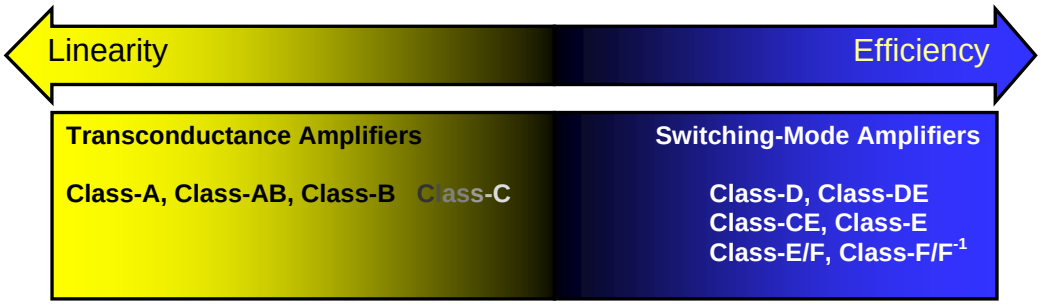

Figure 2.3 Transconductance and switching-mode amplifiers [5]

The difference between transconductance and switching-mode amplifiers can be explained by the loadline theory, which is depicted in Figure 2.4. Switching-mode amplifiers ideally won't conduct high voltage and high current at the same time. Therefore, the loadlines are along the contours on which either current or voltage is kept at minimum. This can also explain why switching-amplifiers can have high efficiency. On the other hand, transconductance amplifiers make use of the linear region of the active device to obtain an output proportional to the input. Class-A has the maximum linear loadline, but it consumes a great amount of power as well. Classes-AB, -B, and –C amplifiers sacrifice some linearity for better efficiency.

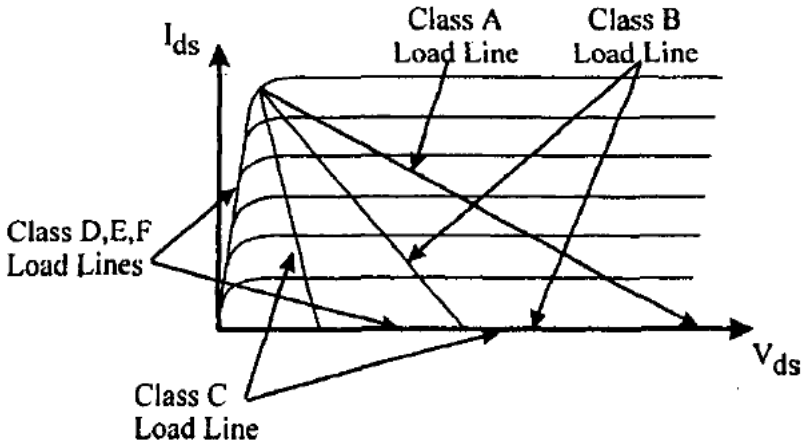

Figure 2.4 Load lines for typical power amplifiers

2.3.1. Transconductance Amplifiers

One of the typical features of transconductance amplifiers is that the active device is treated as a voltage controlled current source. Since transconductance power amplifiers typically have lower efficiencies than the switching-mode counterparts, they

are not good candidates for high efficiency power amplifiers. So they will only be briefly discussed for comparison later on.

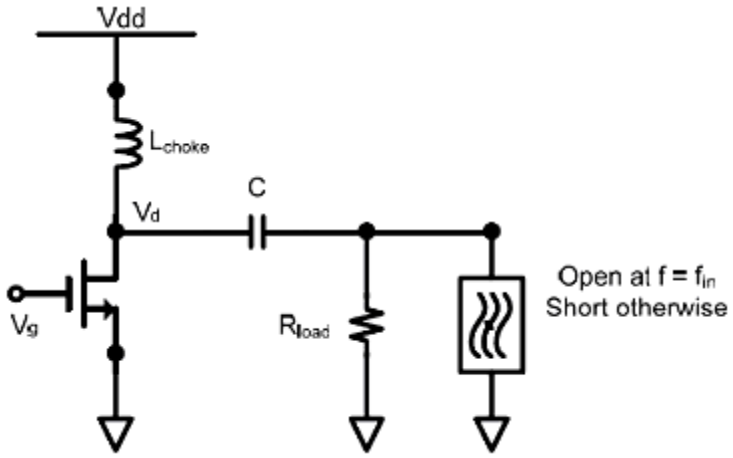

Figure 2.5 Circuit diagram of transconductance amplifier

A typical single-ended transconductance power amplifier has a circuit configuration illustrated in Figure 2.5. The fundamental difference among the transconductance amplifiers is the bias point. In a Class-A amplifier, the operating point and input signal level are set such that the output current flows without distortion at all times. Class-A amplifiers operate within the linear portion of the characteristic of its active device and thus suffer minimal distortion. As for Class-B amplifiers, they are usually implemented in push-pull topology, which consists of two single-ended amplifiers working in antiphase of the input signal. A single-ended Class-B amplifier conducts for one half of the input cycle. The output from each device is a half sinusoidal waveform of the same peak amplitude, and when the two combine, the output will be a full sinusoidal waveform. The characteristics of Class-AB amplifiers are very similar to those of Class-B, except that the biasing point of Class-AB is

intentionally set above zero voltage so that the crossover distortion can be compensated. Class-C amplifiers share similar circuit topologies as Class-A amplifiers, but they generate severe distortion in the output. The operating point of a Class-C amplifier is set at the point where the output signal is zero for more than one-half of an input sinusoidal signal cycle.

The fundamental difference among these classes can also be investigated from the perspective of conduction angle. As the biasing point is lowered, the conduction angle shrinks from 2π in Class-A case, to π in Class-B case, and eventually to less than π in Class-C case. The lower biasing point the active transistor has, the smaller the quiescent current is. Therefore, when compared to Class-A amplifiers, the DC power consumed in Class-C amplifiers are significantly less. This is the basic concept of sacrificing linearity for better efficiency. The relationship between efficiency and conduction angle is shown in Figure 2.6. Fourier analysis in Figure 2.7 provides an in-depth indication about this relationship through the ratio of the power of fundamental harmonic to the power of the DC component. As the conduction angle shrinks, DC power decreases too, but the energy of high-ordered harmonics become significant, resulting in more distortion. Class-A, which has the best linearity, only has a fundamental component in the output, whereas in Class-C, on the contrary, the harmonic components have the power strengths comparable with the fundamental one. Although Class-B has the same magnitude of the fundamental harmonic as the one in Class-A, it has lower linearity due to even harmonics of large energy. The performance of Class-AB ranks between Class-A and Class-B. It has better linearity than Class-B in

that it has higher power of fundamental harmonic and relatively lower power of higher order harmonics.

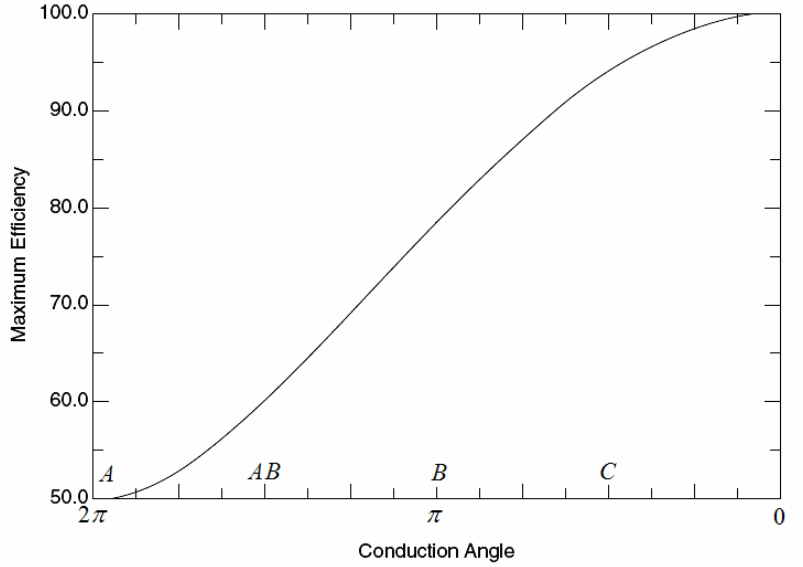

Figure 2.6 Power efficiency for transconductance amplifiers

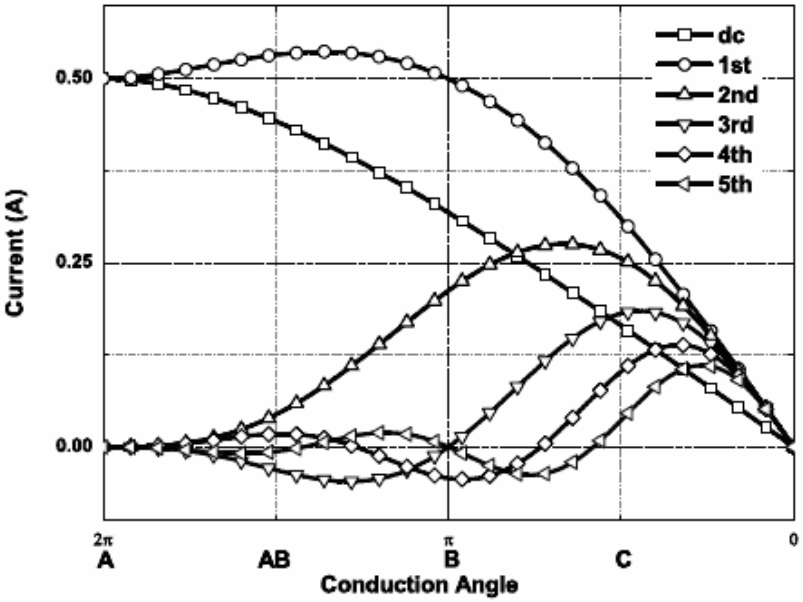

Figure 2.7 Fourier analysis for transconductance amplifiers

The basic features of transconductance amplifiers are summarized in the following table. Detailed explanation can be found in references [1], [3] and [4].

Table 2.1 Summary of transconductance amplifiers

Class	Biasing Point	Output Quiescent Current	Conduction Angle ψ	Maximum Efficiency η	Linearity	Voltage Stress
A	$\frac{V_{i,\max}}{2}$	$\frac{I_{o,\max}}{2}$	2π	50%	Best	2 V_{DC}
AB	$[0, \frac{V_{i,\max}}{2}]$	$[0, \frac{I_{o,\max}}{2}]$	$[0, \pi]$	$[50\%, \frac{\pi}{4}]$	Better	2 V_{DC}
B	0	0	π	$\frac{\pi}{4}$	Fair	2 V_{DC}
C	<0	0	$< \pi$	$\frac{2\psi - \sin 2\psi}{4(\sin\psi - \psi\cos\psi)}$	Bad	2 V_{DC}

* The variable ψ represents one half of the conduction angle, ranging from 0 to π

2.3.2. Switching-Mode Amplifiers

Switching-mode amplifiers have a relatively larger number of sub-categories. No common circuit topology is available for the switching-mode amplifiers, but various switching-mode amplifiers share one basic concept: no power will be lost if current and voltage aren't present in the device simultaneously. One type of switching-mode amplifiers differs from another in the way of control and switch mechanism. Some of the switching amplifiers, like Class-D and Class-S, cut down current or voltage in the switch device abruptly, while Class-E, belonging to soft switching amplifiers, doesn't switch on until the voltage and current vanish. Some switching-mode amplifiers like Classes G and H amplifiers achieve high efficiency by controlling supply rails directly.

Since a rectangular waveform could be viewed as the combination of infinite numbers of harmonics, Class-F makes use of the sum of some harmonics to generate pulses similar to those produced by real switches.

Among the switching amplifiers, Class-E, Class-F and their variants are the most viable solutions for RF amplifiers.

2.3.2.1 Class-F Amplifiers

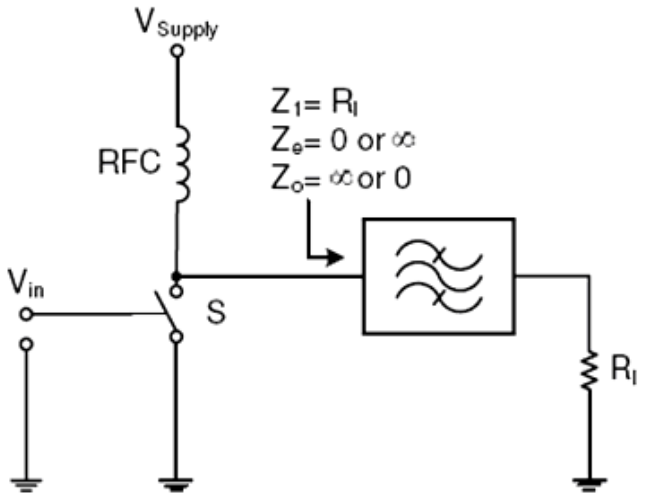

Figure 2.8 An ideal Class-F amplifier

A Class-F amplifier has a load network which is resonant at one or more harmonic frequencies in addition to the fundamental frequency. The sum of harmonics can approximate a squarewave with consequent improvements in both efficiency and output power [3]. In a class-F amplifier, the transistor acts as a current source, and the resulting drain current waveform is a half-sinewave as in a single-ended Class-B configuration. Some specified order harmonics are allowed to appear at the switch, which in turn produce the flattening voltage waveform. Class F could be viewed as a direct improvement of Class B transconductance amplifier. It also has the same peak

drain voltage of $2V_{DC}$ as Class B. It should be noted that Class-F could achieve 100% power efficiency only when infinite harmonics are accumulated, which is not possible in practice. Class-F amplifiers, when compared to Class E power amplifiers, rely heavily on high quality resonators such as expensive bond wires, which significantly limit its potential to apply in CMOS.

2.3.2.2 Class-E Amplifiers

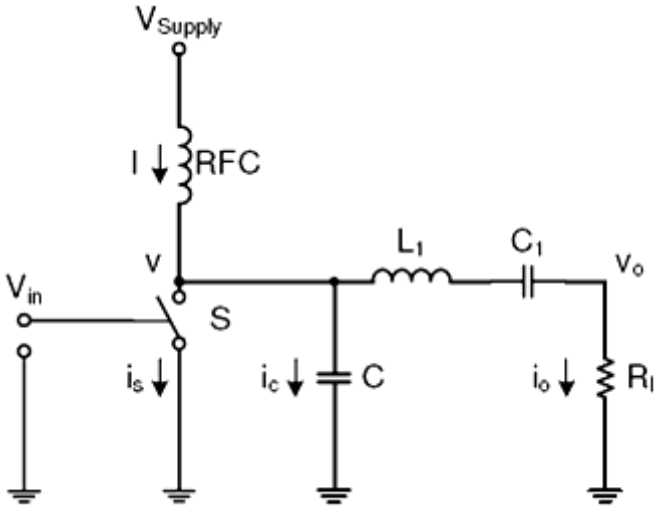

Figure 2.9 An ideal Class-E amplifier

Class-E high efficient switching power amplifier, which is shown in Figure 2.9, was first introduced by Sokals in 1972. Operating the transistor as an on/off switch, Class-E shapes the drain voltage and current waveforms by the load network to avoid simultaneous high voltage and high current in the transistor. The optimum working conditions require the switch voltage and the charges in the shunt capacitor are reduced to zero at the instant of turn-on. By doing so, the power consumption in transistor is minimized.

Class E power amplifiers are inherently nonlinear due to the asymmetrical driving arrangement. Moreover, non-ideal active devices result in more harmonic components and noise in the output. Substantial design efforts are needed to compensate for the nonlinearity or eliminate large noise if Class-E is to be used in wireless applications.

Class E exhibits higher peak drain voltage than other classes. The theoretical peak drain voltage is $3.56V_{DC}$. In reality, drain voltage this high will likely lead to breakdown of the transistor. Importantly, such device stress should be incorporated into the design considerations. An ideal Class E power amplifier has 100% drain efficiency, but this number will be reduced by many practical factors including finite circuit Q, breakdown voltage limitation, nonideal parasitics in transistor, and nonideal RF choker. But generally speaking, Class E amplifiers have many great benefits. Class-E has a simple circuitry and potential 100% efficiency, a *priori* designability, and high tolerance to circuit-parameter variations.

2.4 Summary

The purpose of power amplifiers is to deliver amplified power to the load according to the input signal. For wireless communication systems, the most crucial criterion for PA is that a desired power is delivered with high efficiency and good linearity. Designers must make complicated tradeoffs to meet the desired specifications.

Scientists have invented and employed a great variety of power amplifiers in practical applications. The power amplifiers can be roughly divided into two categories: transconductance and switching-mode amplifiers. There are a number of classes under

these two categories. Every class has its own advantages and disadvantages, whereas some newly introduced hybrid amplifiers combine the strengths of two or more classes. Generally speaking, the transconductance amplifiers have better linearity, while switching-mode amplifiers offer higher efficiency. In switched mode power amplifiers, the input signal has little relationship with the output signal; its major function is to drive the switch and control the fundamental frequency. In some sense, switching-mode amplifiers are more like power converters. To evaluate the performance of switching-mode power amplifiers, power added efficiency, instead of power gain, is the most important criterion.

In the era that CMOS technologies prevail, switching-mode power amplifiers are promising because MOSFET transistors can act as good switches. Among the switching-mode amplifiers, Classes E and F gain more attention in power amplifier designs. Since Class-E amplifiers can better tolerate real circuit variations [2], they are better candidates for low voltage, high efficiency and narrowband power amplifier design. However, to practically design a class E power amplifier in real semiconductor technologies remains very challenging. I will largely focus on the design of fully integrated Class-E power amplifiers in the rest of the thesis.

CHAPTER 3

RF BULK CMOS TECHNOLOGY

3.1 Introduction

In this thesis, 0.18μm silicon bulk CMOS technology is chosen for PA implementation because of its low cost and high integration. However, bulk CMOS inherently has many parasitics caused by finite conductance, leakage in the bulk, high-k insulator between metals, geometry dimensions, layout style and manufacturing processes. These parasicits, which are partially shown in Figure 3.1, lead to significant losses at high frequencies.

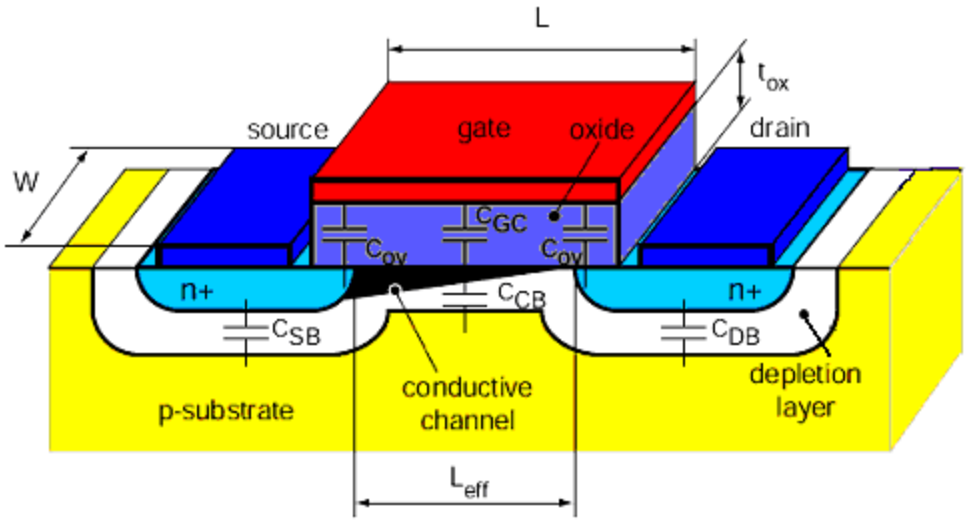

Figure 3.1 Cross-section of NMOS with parasitic capacitances [4]

To reduce these undesired effects and improve the performance of high-speed applications, novel materials, scaled-down feature sizes and different layout styles have been widely employed in recently emerging CMOS technologies. Although there are

some side effects of scaling CMOS, recent progresses make the RF CMOS a good solution for massive volume high performance wireless chip designs. The detailed discussion about RF CMOS can be found in references [6], and [7].

3.2 General Impacts of Scaled-Down CMOS

Table 3.1 The effects of scaling on MOSFET device parameters

Parameter	Symbol	Costant Field Scaling	Constant Voltage Scaling	Constant Voltage Scaling with Velocity Saturation
Gate Length	L	$1/\alpha$	$1/\alpha$	$1/\alpha$
Gate Width	W	$1/\alpha$	$1/\alpha$	$1/\alpha$
Field	E	1	α	α
Voltage	V	$1/\alpha$	1	1
Current	I	$1/\alpha$	α	1
Power	P	$1/\alpha^2$	α	1
Power Delay	$P\Delta t$	$1/\alpha^3$	$1/\alpha$	$1/\alpha$
Substrate Doping	N_a	α^2	α^2	α^2
Oxide Thickness	t_{ox}	$1/\alpha$	$1/\alpha$	$1/\alpha$
Gate Capacitance	C_G	$1/\alpha$	$1/\alpha$	$1/\alpha$
Oxide Capacitance	C_{OX}	α	α	α
Transient Time	t_r	$1/\alpha^2$	$1/\alpha^2$	$1/\alpha$
Cut off Frequency	f_T	α	α^2	α

Continuously scaled-down feature size is the well-known indication of progress in semiconductor industry. CMOS technology has benefited greatly from the continuous scaling, such as higher integration, lower power consumption, shorter signal delay, higher operational frequency. Common effects of scaling on MOSFET device parameters are listed in Table 3.1, where α is the scaling factor.

3.2.1 Limitations of Scaled-down MOSFET

3.2.1.1 Lower Breakdown Voltage

Scaling-down also has some negative effects on devices built in deep sub-micron CMOS technologies. One such effect is the degradation of breakdown voltage. The thickness of the gate oxide shrinks as the CMOS process is scaled down, which leads to lower breakdown voltage. For instance, in 0.18μm CMOS technology, the thickness of oxide is $4.1nm$. As a result, the breakdown voltage is approximately $4.2V$. The breakdown voltage limits the drain voltage swing which in turn determines the maximum power to be delivered. The problem is worsening in Class-E power amplifier due to its high voltage stress. In practice, the issue of breakdown voltage can be alleviated by applying new circuit topologies like cascode.

3.2.1.2 Short Channel Effects

Short channel effects are more appreciable for deep sub-micron CMOS technologies. Lower threshold voltage, mobility degradation, and velocity saturation should be accounted for precise performance analyses. As the channel length shrinks, the depletion regions at the drain and source become more appreciable, leading to less

charge needed to create the inversion. This phenomenon is more significant when the depletion region around the drain is expanded due to the high drain voltage. Therefore, the threshold voltage is effectively reduced.

The electric field is inversely proportional to the channel length. Drift velocity rolls off and eventually saturates in strong electric field because of carriers scattering. As channel length becomes shorter, the lateral field increases and transistors become velocity saturated if the supply voltage is held constant [8]. As the transverse electric field caused by the gate voltage increase, more electron collisions occur near the surface of the silicon, leading to mobility degradation. Therefore, higher overdrive voltage at the gate does not lead to higher drain current.

For Class-E amplifiers, high drain voltage and high drain current do not overlap. So fortunately, these short channel effects become insignificant in Class-E amplifiers. Moreover, if Class-E amplifiers are driven by moderate voltage signals, these effects can be neglected.

3.2.1.3 Large Parasitic Capacitance

Another serious problem for the scaled-down CMOS is the large parasitic capacitance, especially the increased oxide capacitance due to shrinking oxide thickness. Since active devices of large geometry are usually used in power amplifier designs, the input and output parasitic capacitance, including overlap, channel and junction capacitance, become significant, resulting in undesired circuit performance, i.e. low overall efficiency, off-optimum operation, and shifted center frequency. Therefore, large parasitic capacitance should be considered in power amplifier designs.

3.2.2 Limitations of On-Chip Passive Devices

As the cutoff frequency is improved, the transistor in advanced CMOS technology can function satisfactorily in 5 - 10GHz RF applications. However, for monolithic applications, a good active device alone does not necessarily lead to a good design. Passive components, including capacitor, inductor, resistor, and their variants, play equally critical roles in monolithic RF design. Due to the large aforementioned parasitic losses, passive components in bulk CMOS usually have lower qualities compared to their lumped counterparts. For instance, the quality of MIM (Metal-Insulator-Metal) capacitor in CMOS normally can reach 50 or above, whereas an on-chip planar inductor only has a typical quality factor of 5-10, no larger than 20 even in advanced RF CMOS [6]. Obviously, low quality inductors become the bottleneck of performance of RF applications. Since a planar inductor plays a critical role in on-chip RF circuit and takes up a large dead size, designers must pay a great deal of attention to optimizing the design of a planar inductor.

3.3 Features of 0.18μm 1P6M CMOS Process

0.18μm 1P6M CMOS process offers one polysilicon and six metal layers while has a small feature size of 0.18μm. It provides the aforementioned benefits of scaled-down CMOS. Moreover, a thick top metal layer is available for implementing on-chip inductors of high quality factors. Figure 3.2 illustrates the cross section of 0.18μm 1P6M process.

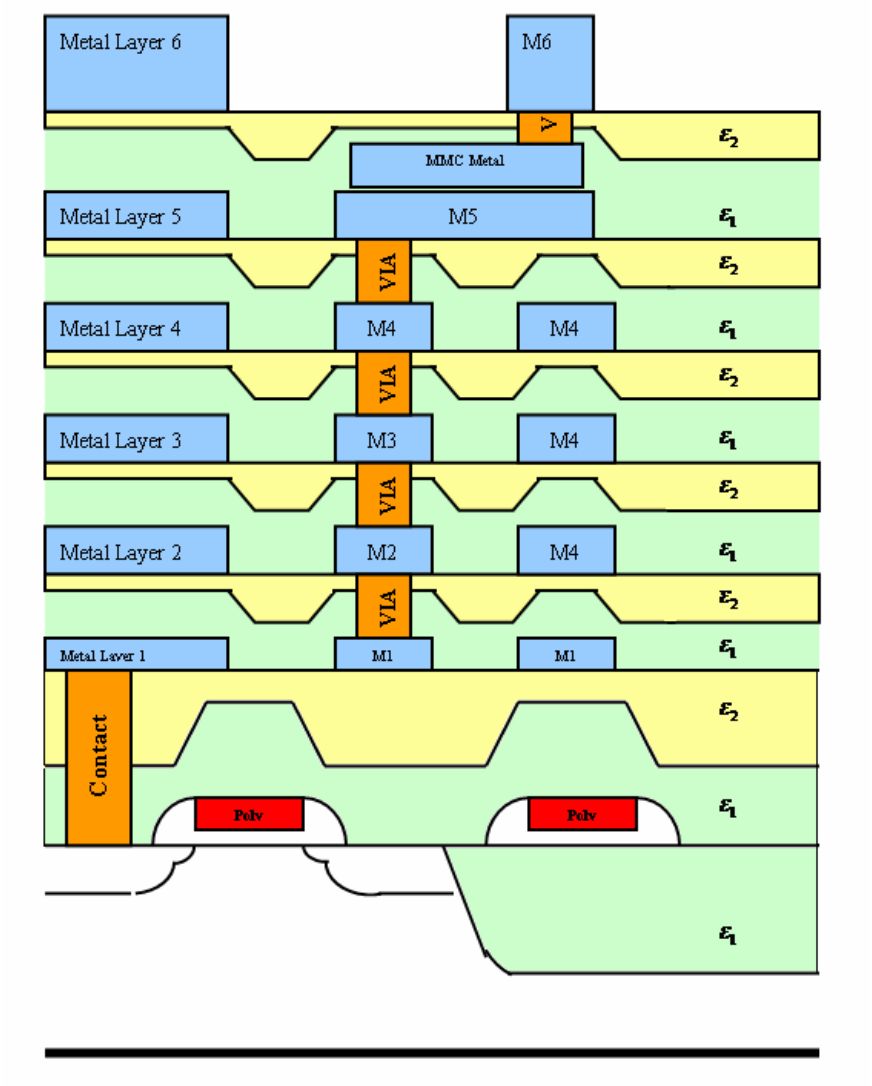

Figure 3.2 Cross section of 0.18μm 1P6M CMOS process

The detailed process parameters can be obtained from the foundry companies.

CHAPTER 4

CLASS-E POWER AMPLIFIER DESIGN METHODOLOGY

4.1 Ideal Class-E PA Design Method

A typical equivalent circuit of an ideal single-ended Class-E power amplifier depicted in Figure 4.1 contains an ideal voltage-controlled switch, a shunt capacitor at the output, a RF choke and a series-tuned R-L-C circuit as the load. The RF choke allows constant DC current to flow through when the switch is on, while blocks ac signals as an open circuit when the switch is off. The shunt capacitor is charged and discharged during the on-off cycle. The series-tuned tank allows the fundamental sinusoid appears at the output.

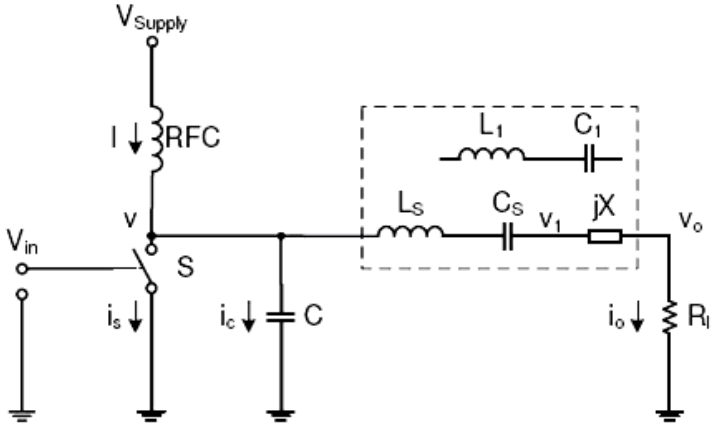

Figure 4.1 Equivalent circuit of Class-E amplifier

If no charge is stored in the capacitor and no current flows through it at the turn-on instant, the optimum Class-E is obtained. Raab suggested that the current and

voltage waveforms in an optimum class E power amplifier should meet the following conditions [9]:

a) The rise of the voltage across the transistor at turn-off should be delayed until the transistor fully turns off.
b) The voltage across the switch should be reduced to zero at the moment the transistor turns on.
c) The slope of the voltage across the switch should be zero at turn-on.

These conditions ensure that no large energy is dissipated even during the switching transition. For this reason, optimum Class-E amplifiers are also called zero-current or zero-voltage switching amplifiers. If the voltage signal vanishes earlier than the optimum time, it is called suboptimal operation. Both conditions, illustrated in Figure 4.2, can result in 100% efficiency; but only under the optimum working condition can deliver maximum energy $1/2CV^2$ with 100% efficiency to the load.

This optimum condition can be achieved through adjusting the phase difference between the switch voltage and current. This condition is uniquely determined by the appropriate load network and shunt capacitor. Unlike Classes B and C in which the load network only provides conjugate matched impedance to the load, the load network in Class-E is also used to adjust the phase difference between the switch current and voltage such that no high voltage and high current occur simultaneously across the switch, which is shown in Figure 4.3. Thus, the network design equations come from the solution of a set of simultaneous equations for the steady-state periodic response in time domain under optimum working conditions [10].

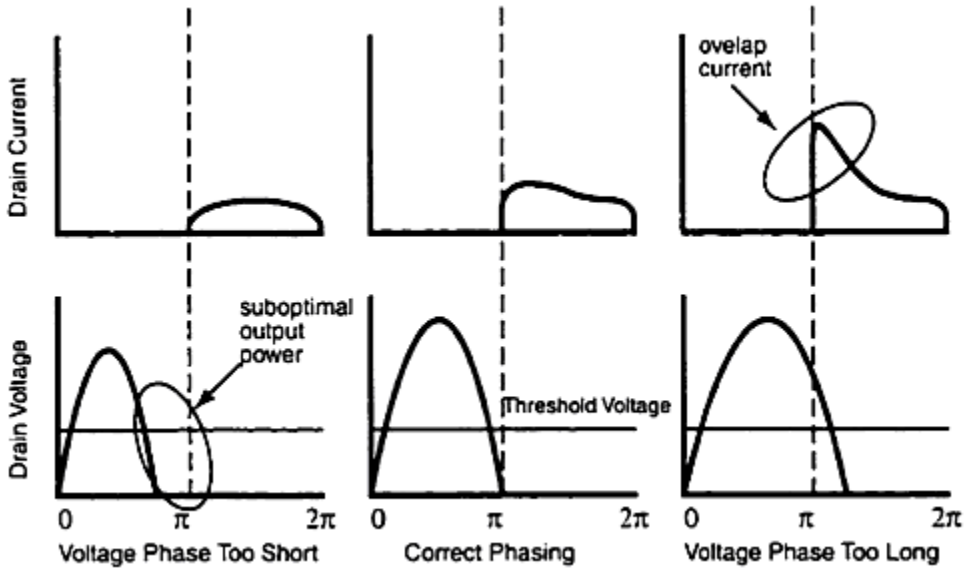

Figure 4.2 Drain voltage and current waveforms in Class-E. Waveforms from left to right are suboptimal, optimum, and off-nominal conditions, respectively. The efficiency can be 100% in suboptimal situation.

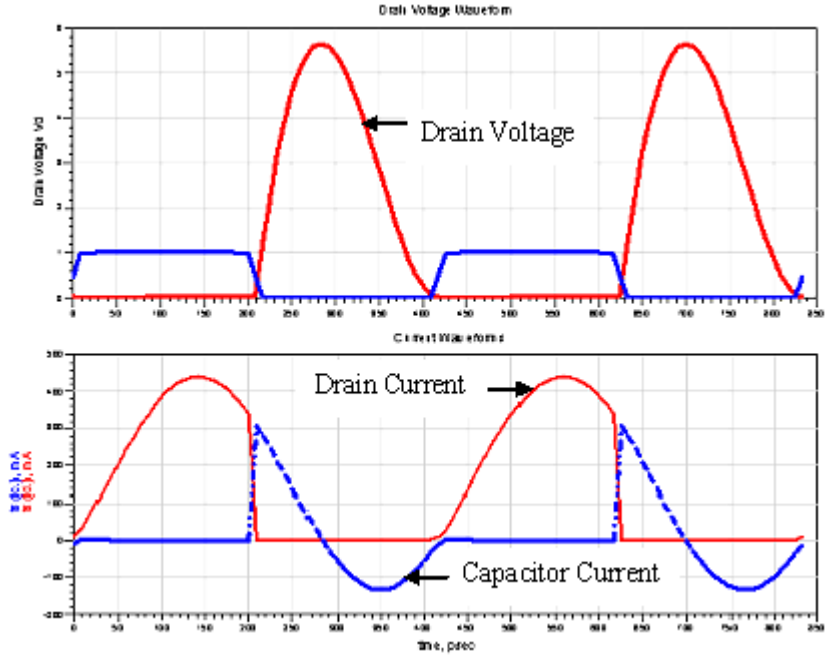

Figure 4.3 Optimum Class-E waveforms

Raab introduced an analytical method based on Fourier analysis to determine the circuit parameters for the optimum Class-E tuned power amplifiers [9]. For simplicity, the typical Class-E circuit under investigation switches at 50% duty cycle. The output sinusoid $v_o(t)$ can be expressed as

$$v_o(t) = V_o \sin(\omega t + \varphi) \tag{4.1}$$

, where φ is the output shift angle to the switching-on instant in radius. The load angle ψ is determined by the excess reactance and the load resistance, which is given by

$$\tan\psi = \frac{X}{R} \tag{4.2}$$

It should be noted that the excess reactance *jX* is finite only at the fundamental frequency and it is assumed to be infinite at harmonic frequencies. Five assumptions are made in this conventional method:

1) The RF choke is ideal so that only DC current I_{dc} flows through it.
2) The series-tuned circuit has high quality factor so that the load voltage is sinusoidal at the harmonic output frequency, i.e., $v_o(t) = V_o \sin(\omega t + \varphi)$.
3) The active device acts as an ideal switch: infinite conductance, zero turn-on resistance, and infinite turn-off resistance. This ideal switch also allows positive and negative voltages and currents.
4) The shunt capacitance including device output capacitance and external capacitance is independent of device voltage.

5) All passive circuit elements are ideal. This means no parasitic power loss. Thus, 100 percent drain efficiency is theoretically obtainable if optimum condition is established.

Numerous literatures have presented some mathematical analyses of the class E amplifier, most of which are tedious. The most widely used design equations for optimum circuit parameters are provided by Raab in [9], which are listed as follows:

$$\tan\varphi = -\frac{2}{\pi} \tag{4.3}$$

$$R_{dc} = \frac{V_{DC}}{I_{dc}} = \frac{1+\pi^2/4}{2} R = 1.7337R \tag{4.4}$$

$$B = \omega C = \frac{2}{\pi(1+\pi^2/4)R} = \frac{0.1836}{R} \tag{4.5}$$

$$X = R\tan\psi = \frac{\pi}{8}\left(\frac{\pi^2}{2} - 2\right)R = 1.1525R \tag{4.6}$$

$$V_o = \frac{2}{\sqrt{1+\pi^2/4}} V_{DC} = 1.074V_{DC} \tag{4.7}$$

$$P_o = \frac{V_o^2}{2R} = \frac{2}{1+\pi^2/4}\frac{V_{DC}^2}{R} = 0.5768\frac{V_{DC}^2}{R} \tag{4.8}$$

$$L_S = L - L_X = \frac{QR - X}{\omega} = \frac{8V_{DC}^2}{\omega P_o(4+\pi^2)}\left(Q - \frac{\pi(\pi^2-4)}{16}\right) \tag{4.9}$$

$$C_S = \frac{1}{\omega^2 L_S} \tag{4.10}$$

$$V_{SM} = -2\pi\varphi V_{DC} = 3.56V_{DC} \tag{4.11}$$

$$I_{SM} = \frac{4\left(\sqrt{\pi^2+4}+2\right)V_{DC}}{\left(\pi^2+4\right)R} = 2.84 I_{dc} \tag{4.12}$$

$$\eta = \frac{P_o}{P_{DC}} = \frac{\frac{2}{1+\pi^2/4}\frac{V_{DC}^2}{R}}{\frac{V_{DC}^2}{R_{dc}}} = \frac{2}{1+\pi^2/4}\frac{R_{dc}}{R} = 1 \tag{4.13}$$

More general analysis for ideal class E operations including multipliers can be found in [11] and [12]. These explicit design equations based on exhaustive Fourier analysis are proven to be accurate for those cases in which aforementioned assumptions can hold. However, these assumptions do not reflect the realities in RF CMOS applications, where only low quality passive components and non-ideal active devices are available. As a consequence, the closed-form analytical design equations based on ideal assumptions probably produce discrepant parameters for non-ideal cases. Moreover, variations and parasitics in circuit components result in power losses. Hence, a nominal 100 percent efficiency is hardly achieved in practice. Possible variations or non-ideal impacts exist in:

- parasitic capacitance of the transistor
- on-resistance of the transistor
- finite DC feed inductor
- finite loaded quality factor of series tuned circuit

These impacts are more severe in CMOS applications due to the inherent limitations mentioned in the last chapter.

A lot of published papers provide several optimized design methods from certain aspects. One or more ideal assumptions are replaced by more realistic models to develop optimized design methods. Inevitably, the complexity of analysis is expanded if no new constraints are introduced. Therefore, explicit analytical design equations are not available because of the convergence problems. Actually, numerical solutions are used instead.

Few previous works systematically discussed optimized design methods for CMOS. Obviously, it is very difficult and unnecessary to take all non-ideal impacts of CMOS into account to derive approximated initial design parameters. In this thesis, only those impacts could affect the working conditions are considered in developing optimized design equations for Class-E power amplifier in CMOS.

4.2 Practical Design Equations for CMOS Cases

The discrepancies between predicted parameters and real component values lead to power losses and thus lower efficiency. Efficiency degradation is mainly caused by the power losses in the passive components and the active device, which can be classified into two categories: switching power loss and parasitic power loss. Switching power loss is caused by the simultaneous occurrence of high drain current and high drain voltage, which relates to non-optimum working conditions caused by variations in circuit elements. Parasitic power loss mainly comes from the parasitic resistors like switching-on resistance. In practice, off-optimum power loss easily outweighs parasitic loss, especially in CMOS applications. Therefore, a good load network design is very critical.

The practical design equations presented here are optimized for the impacts of finite DC feed inductor and parasitic capacitance of the transistor. To reduce the complexity, the design procedure is divided into two steps for load network and active device.

4.2.1 Design of Load Network with Finite DC Feed Inductor

Using finite DC feed inductance instead of an RF-choke in a Class-E PA has significant benefits, including [13]:

1) a reduction in overall size and cost
2) a higher load resistance, leading to a more efficient output matching network
3) a possible reduction in the supply voltage required
4) larger switch parallel capacitor C for the same supply voltage, output power and load
5) easy employment in an envelope elimination and restoration (EER) system.

Figure 4.4 illustrates the drain voltage startup times of Class-E amplifiers with infinite and finite DC feed inductors. Obviously, the infinite DC feed inductor will take much longer time to establish the steady state, which is unexpected in practice.

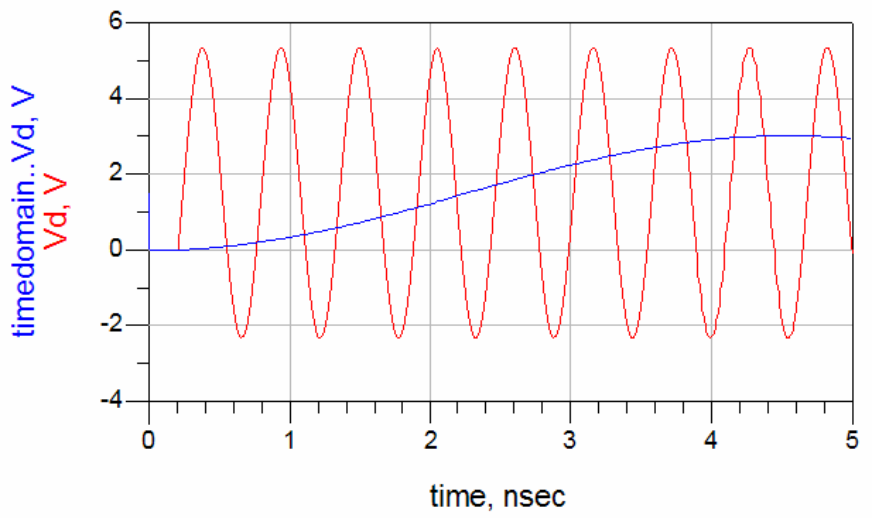

Figure 4.4 Transient analyses for cases with infinite and finite DC feed inductors

The analytical analysis of Class-E power amplifier with finite DC feed inductor can be found in [14]. For simplicity, several assumptions are adopted in this analysis:

1) The switch is ideal. The 'on' and 'off' resistances of the transistor are zero and infinity, respectively.
2) The shunt capacitor is independent of the voltage across it.
3) The series tuned resonator has large quality factor, i.e., Q > 10.
4) All circuit elements are ideal.
5) The input signal has 50% duty cycle.

The switching-off and on periods are defined as:

$$\begin{cases} 0 \le t \le \dfrac{\pi}{\omega} & OFF, \quad R_{OFF} = \infty \\ \dfrac{\pi}{\omega} < t \le \dfrac{2\pi}{\omega} & ON, \quad R_{ON} = 0 \end{cases} \tag{4.14}$$

Output voltage and current are:

$$i_o(t) = I_o \sin(\omega t + \phi) \qquad v_o(t) = I_o R \sin(\omega t + \phi) \tag{4.15}$$

The voltage v_1 at the fictious point is

$$v_1(t) = V_1 \sin(\omega t + \phi_1), \tag{4.16}$$

where

$$V_1 = I_o R \sqrt{1 + \frac{X^2}{R^2}}$$

$$\phi_1 = \phi + \tan^{-1} \frac{X}{R}$$

At the drain, apply KCL and the result is given as

$$i_L(t) = i_C(t) + I_O \sin(\omega t + \phi) + i_{SW}(t), \tag{4.17}$$

where $i_L(t)$ and $i_C(t)$ are constrained by the physical characteristics of inductor and capacitor, respectively, such as

$$V_{DD} - v_d(t) = L_1 \frac{di_L(t)}{dt} \tag{4.18}$$

$$i_C(t) = C_1 \frac{dv_d(t)}{dt} \tag{4.19}$$

When the switch turns on, $v_d(t)$ is kept zero. Hence $i_C(t) = 0$ during the ON state. And the relation between the supply voltage and the current flowing through the inductor is

$$V_{DD} = L_1 \frac{di_{Lon}(t)}{dt} \quad \text{for } \frac{\pi}{\omega} \le t \le \frac{2\pi}{\omega}$$

Thus, the on-state inductor current is given by

$$i_{Lon}(t) = \frac{V_{DD}}{L_1}\left(t - \frac{\pi}{\omega}\right) + C\,, \tag{4.20}$$

where C is a constant.

When the transistor is off, the capacitor current is given by

$$i_C(t) = C_1 \frac{dv_d(t)}{dt}$$

A second-order differential equation is therefore obtained as

$$L_1 C_1 i''_{Loff}(t) + i_{Loff}(t) = I_o \sin(\omega t + \phi) \tag{4.21}$$

The expression of $i_{Loff}(t)$ is

$$i_{Loff}(t) = A\cos\omega_0 t + B\sin\omega_0 t + \frac{I_o}{1-\beta^2}\sin(\omega t + \phi)\,, \tag{4.22}$$

where

$$\omega_0 = \frac{1}{\sqrt{L_1 C_1}}$$

$$\beta = \frac{\omega}{\omega_0}$$

$$0 \le t \le \frac{\pi}{\omega}$$

To evaluate the constants A, B, and C, certain boundary conditions should be applied.

Boundary condition 1:

$$\begin{cases} i_{Lon}\left(\dfrac{2\pi}{\omega}\right) = i_{Loff}\left(0\right) \\ i_{Lon}\left(\dfrac{\pi}{\omega}\right) = i_{Loff}\left(\dfrac{\pi}{\omega}\right) \end{cases} \tag{4.23}$$

Boundary condition 2:

$v_d(t)$ must also be continuous based on the characteristics of capacitance. As $v_{don}(t) = 0$, another boundary condition is $v_{doff}(0) = 0$.

From $v_{doff}(0) = 0$, it has

$$L_1 \frac{d_{iLoff}(t)}{dt}\Big|_{t=0} = V_{DD} \quad \text{or} \qquad i'_{Loff}(0) = \frac{V_{DD}}{L_1} \tag{4.24}$$

Therefore, it follows

$$\frac{di_{Loff}(t)}{dt} = -A\omega_0 \sin\omega_0 t + B\omega_0 \cos\omega_0 t + \frac{I_o\omega}{1-\beta^2}\cos(\omega t + \phi), \tag{4.25}$$

and

$$\frac{V_{DD}}{L_1} = B\omega_0 + \frac{I_o\omega}{1-\beta^2}\cos\phi \tag{4.26}$$

$$B = \frac{V_{DD}}{L_1\omega_0} - \frac{I_o\beta}{1-\beta^2}\cos\phi \tag{4.27}$$

From $i_{Lon}\left(\dfrac{2\pi}{\omega}\right) = i_{Loff}\left(0\right)$, it has

$$A + \frac{I_o}{1-\beta^2}\sin\phi = \frac{V_{DD}}{L_1}\frac{\pi}{\omega} + C \tag{4.28}$$

On the other hand, $i_{Loff}\left(\dfrac{\pi}{\omega}\right) = i_{Lon}\left(\dfrac{\pi}{\omega}\right)$. Hence, it has

$$C = A\cos\frac{\pi}{\beta} + B\sin\frac{\pi}{\beta} - \frac{I_o}{1-\beta^2}\sin\phi \tag{4.29}$$

$$\begin{aligned} A &= \frac{1}{1-\cos\frac{\pi}{\beta}}\left[B\sin\frac{\pi}{\beta} - \frac{2I_o}{1-\beta^2}\sin\phi + \frac{V_{DD}}{L_1}\frac{\pi}{\omega}\right] \\ &= \frac{1}{1-\cos\frac{\pi}{\beta}}\left[\left(\frac{V_{DD}}{L_1\omega_0} - \frac{I_o\beta}{1-\beta^2}\cos\phi\right)\sin\frac{\pi}{\beta} - \frac{2I_o}{1-\beta^2}\sin\phi + \frac{V_{DD}}{L_1}\frac{\pi}{\omega}\right] \end{aligned} \tag{4.30}$$

$$C = \frac{1}{1-\cos\frac{\pi}{\beta}}\left[\begin{array}{l}\left(\frac{V_{DD}}{L_1\omega_0} - \frac{I_o\beta}{1-\beta^2}\cos\phi\right)\sin\frac{\pi}{\beta} \\ -\left(1+\cos\frac{\pi}{\beta}\right)\frac{I_o}{1-\beta^2}\sin\phi + \cos\frac{\pi}{\beta}\cdot\frac{V_{DD}}{L_1}\frac{\pi}{\omega}\end{array}\right] \tag{4.31}$$

Now consider the optimum conditions

$$\begin{cases} v_d(t)\big|_{t=\pi/\omega} = 0 \\ \dfrac{dv_d(t)}{dt}\big|_{t=\pi/\omega} = 0 \end{cases} \tag{4.32}$$

From the zero derivate voltage condition $\frac{dv_d(t)}{dt} = 0$, it has

$$i_{Loff}\left(\frac{\pi}{\omega}\right) = 0 + I_o\sin(\pi+\phi) = -I_o\sin\phi = A\cos\frac{\pi}{\beta} + B\sin\frac{\pi}{\beta} - \frac{I_o}{1-\beta^2}\sin\phi$$

$$i_{Loff}\left(\frac{\pi}{\omega}\right) = i_{Lon}\left(\frac{\pi}{\omega}\right)$$

$$i_{Lon}\left(\frac{\pi}{\omega}\right) = \frac{V_{DD}}{L_1}\cdot 0 + C$$

$$C = -I_o\sin\phi$$

Step further by applying the period condition $i_{Loff}(0) = i_{Lon}\left(\frac{2\pi}{\omega}\right)$, and it follows

$$A = \frac{V_{DD}}{L_1}\frac{\pi}{\omega} + \frac{I_o\left(\beta^2 - 2\right)}{1-\beta^2}\sin\phi \tag{4.33}$$

From the condition $v_d(t)\big|_{t=\pi/\omega} = 0$, it has

$$\begin{aligned} &\frac{di_{Loff}(t)}{dt}\Big|_{t=\pi/\omega} = \frac{V_{DD}}{L_1} \Rightarrow \\ &-A\sin\frac{\pi}{\beta} + B\cos\frac{\pi}{\beta} - \frac{I_o\beta}{1-\beta^2}\cos\phi = \frac{V_{DD}}{L_1\omega_0} \end{aligned} \tag{4.34}$$

Substitute A, B, C into the above two equations, and rewrite them as

$$\frac{I_o\beta\cot\left(\frac{\pi}{2\beta}\right)}{1-\beta^2}\left[\beta\sin\phi + \cot\left(\frac{\pi}{2\beta}\right)\cos\phi\right] = \frac{V_{DD}}{L_1\omega_0}, \tag{4.35}$$

and

$$\frac{I_o}{1-\beta^2}\begin{bmatrix}\beta\sin\frac{\pi}{\beta}\cos\phi + \beta^2\sin\phi \\ +\left(2-\beta^2\right)\sin\phi\cos\frac{\pi}{\beta}\end{bmatrix} = \frac{V_{DD}}{L_1}\left(\frac{1}{\omega_0}\sin\frac{\pi}{\beta} + \frac{\pi}{\omega}\cos\frac{\pi}{\beta}\right) \tag{4.36}$$

Solve these two equations for ϕ and I_o, leading to

$$\cot\phi = \frac{(1-\beta^2)\left(1-\cos\frac{\pi}{\beta}\right)^2 - \frac{\beta\pi}{2}\sin\frac{\pi}{\beta}\left(1+\cos\frac{\pi}{\beta}\right)}{\beta\sin\frac{\pi}{\beta}\left(1-\cos\frac{\pi}{\beta} + \frac{\pi}{2\beta}\sin\frac{\pi}{\beta}\right)}, \tag{4.37}$$

and

$$I_o = \frac{V_{DD}(1-\beta^2)\left(1-\cos\frac{\pi}{\beta}+\frac{\pi}{2\beta}\sin\frac{\pi}{\beta}\right)}{L_1\omega_0 \sin\phi \sin\frac{\pi}{\beta}} \tag{4.38}$$

Output power and circuit parameters for the optimum Class-E now can be determined by this known output signal. However, the resulting analytical design equations are too complicated to be used in practice. Many researchers like Milosevic et al have developed some relatively simpler numerical design equations.

In [15], the authors used $Q_{dc} = X_{dc} / R_{dc}$ as an independent variable and numerically evaluated other circuit parameters in functions of Q_{dc}. Based on the theoretical discrete data, they then employed Lagrange interpolation method to build two sets of continuous design equations for non-ideal cases with finite DC-feed inductance of low and high quality factors, respectively. And the simulation result of an example with low quality factor inductance demonstrated that the design equations had really good accuracy. However, the design equations produce large discrepancy in the cases of large quality factor inductance. Moreover, the complicated design equations are confusing and error-prone.

The reason that the author adopted two sets equations probably is that the coefficients scatter over a large range, i.e., from 1 to infinity, which are listed in Table 4.1. In such a broad range, typical curve fitting methods cannot work well or produce acceptable results across the board, but much higher order polynomial equations are needed.

Table 4.1 Analytical values for interpolation used in [15]

X_{dc}/R_{dc}	$P_{out}R/V_{dc}^2$	BR	X/R
∞(RFC)	0.5768	0.1836	1.152
1000	0.5774	0.1839	1.151
500	0.5781	0.1843	1.150
200	0.5801	0.1852	1.147
100	0.5834	0.1867	1.141
50	0.5901	0.1899	1.130
20	0.6106	0.1999	1.096
15	0.6227	0.2056	1.077
10	0.647	0.2175	1.039
5	0.7263	0.2573	0.9251
3	0.8461	0.3201	0.7726
2	1.013	0.4142	0.5809
1	1.363	0.6839	0.0007

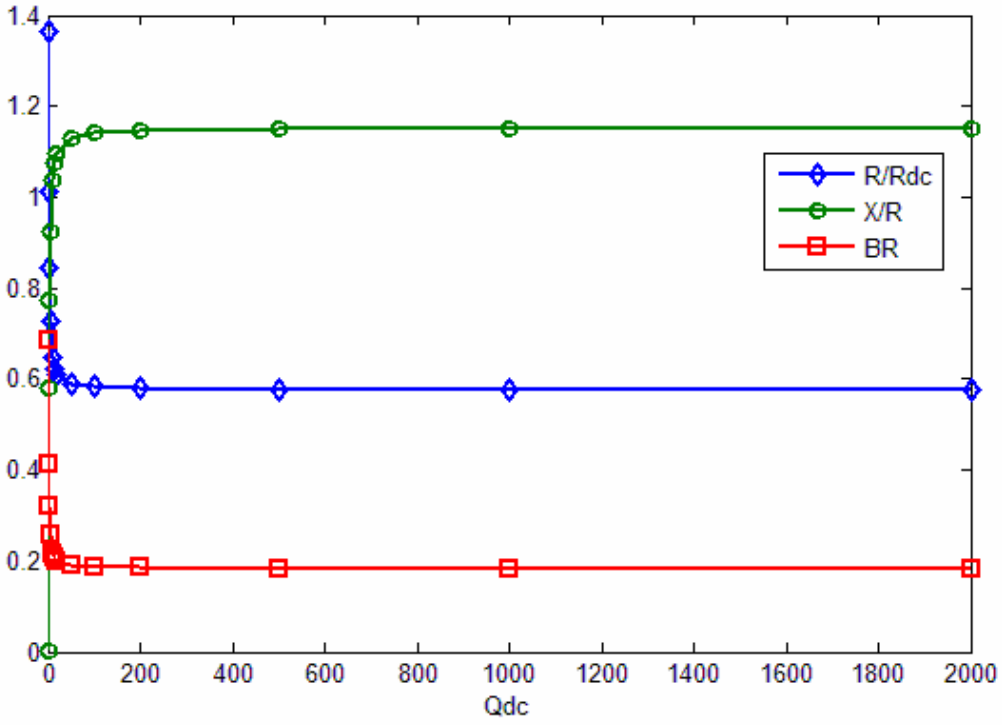

Figure 4.5 Steep curves for interpolation in [15]

If the data listed in Table 4.1 are transformed to a set of new data such that large difference is smoothed and the range is shortened, a more "linear" relationship among the data can be established, leading to single set of equations but having more precise interpolation values. First, we can replace X_{dc}/R_{dc} with $\ln\left(X_{dc}/R_{dc}\right)$, safely assuming that a RFC has reactance larger than $e^{10} \approx 22026$. Additionally, the products of XB and X/R_{dc} instead of BR and X/R are used for curve fitting, which are listed in Table 4.2.

Table 4.2 New data used for polynomial interpolation

$\ln(X_{dc}/R_{dc})$	$\frac{R/R_{dc}}{(R/R_{dc})_0}$	$\frac{X/R_{dc}}{(X/R_{dc})_0}$	$\frac{XB}{(XB)_0}$
10.000	1.0000	1.0000	1.0000
6.9078	1.0010	1.0002	1.0008
6.2146	1.0023	1.0005	1.0021
5.2983	1.0057	1.0014	1.0043
4.6052	1.0114	1.0018	1.0072
3.9120	1.0231	1.0035	1.0146
2.9957	1.0586	1.0071	1.0359
2.7081	1.0796	1.0093	1.0469
2.3026	1.1217	1.0117	1.0684
1.6094	1.2592	1.0112	1.1254
1.0986	1.4669	0.9838	1.1693
0.6931	1.7562	0.8856	1.1376
0.0000	2.3630	0.0014	0.0023

In this way, the error in R would not affect the accuracy of X and R. And these new data shows less variation, which is great for interpolation. The normalized data used here are to preserve the expressions like the ideal value plus some modifications. In this way, the complicated terms can be dropped off for calculation by hand.

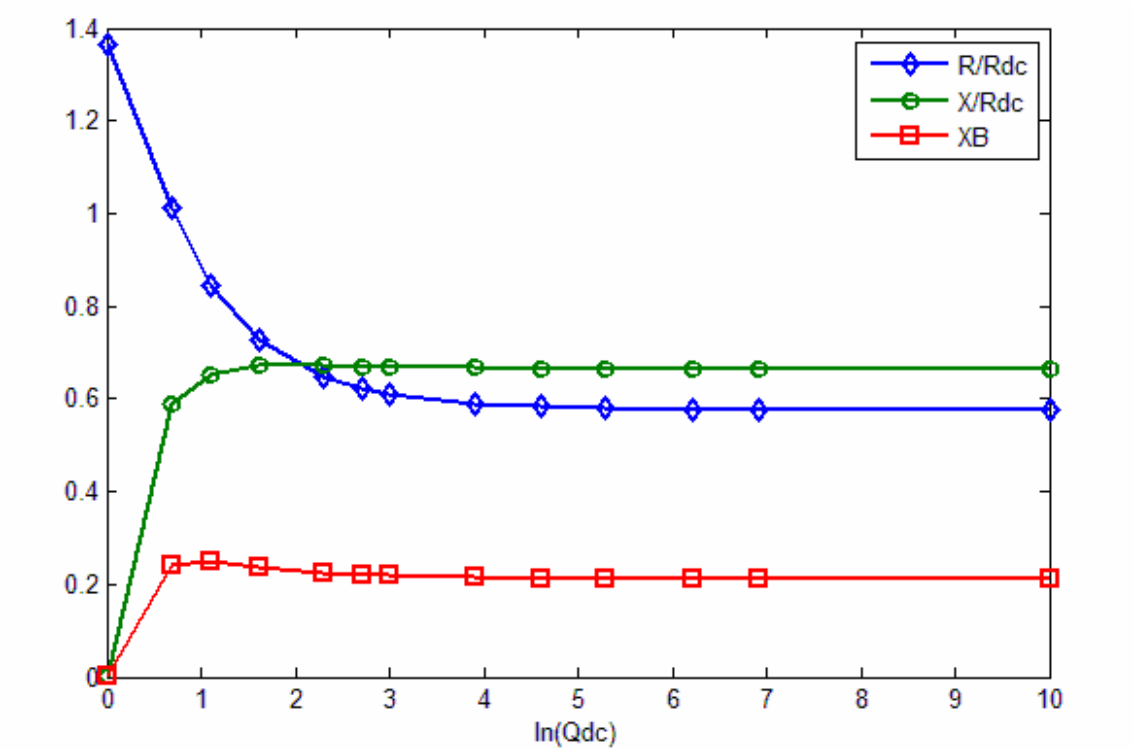

Figure 4.6 Smooth transformed curves for curve fitting

With the aid of curve-fitting tools provided by MATLAB, the resulting design equations can be found as:

$$X_{dc} = \omega L_{dc} \qquad R_{dc} = V_{DD}^2 / P_o \tag{4.39}$$

$$Q_{dc} = \frac{X_{dc}}{R_{dc}} \qquad m = \ln(Q_{dc}) \tag{4.40}$$

$$X = R_{dc} \cdot 0.664574 \cdot \left(1 - \frac{0.05156m^2 - 0.5168m + 0.5808}{m^4 - 1.902m^3 + 4.444m^2 - 0.2203m + 0.5816}\right) \quad (4.41)$$

$$R = R_{dc} \cdot 0.5897 \cdot \left(1 - \frac{0.416m - 1.611}{m^2 + 0.2034m + 1.234}\right) \quad (4.42)$$

$$XB = 0.2115 \cdot \left(1 - \frac{0.1628m^2 - 1.43m + 0.6794}{m^4 - 2.687m^3 + 6.435m^2 - 2.032m + 0.6809}\right) \quad (4.43)$$

$$B = XB / X \quad (4.44)$$

The simulation results listed in Table 4.3 show that predicated circuit parameters generated by this method perfectly agree with the ideal values. The method proposed by Milosevic et al produces significant errors when Q_{dc} is larger than 5, which is shown in Table 4.3 and Figure 4.8.

Table 4.3 Tests for different design equations

Method	Results Vdc=1.6V, Po=0.25W, f=2.4GHz, Ron=0.1Ohm Rdc=10.24Ohm	
Raab's [9]	Ldc=∞, PAE=98.9% PDC=0.248, Po=0.245	
Test Cases	Ldc=2nH, Qdc=2.95	Ldc=3.73nH, Qdc=5.49
Milosevic's [15]	PAE=97.4% PDC=0.251,Po=0.244	PAE=97.3% PDC=0.309,Po=0.301
This Method	PAE=98.9% PDC=0.248, Po=0.245	PAE=99.6% PDC=0.249, Po=0.248

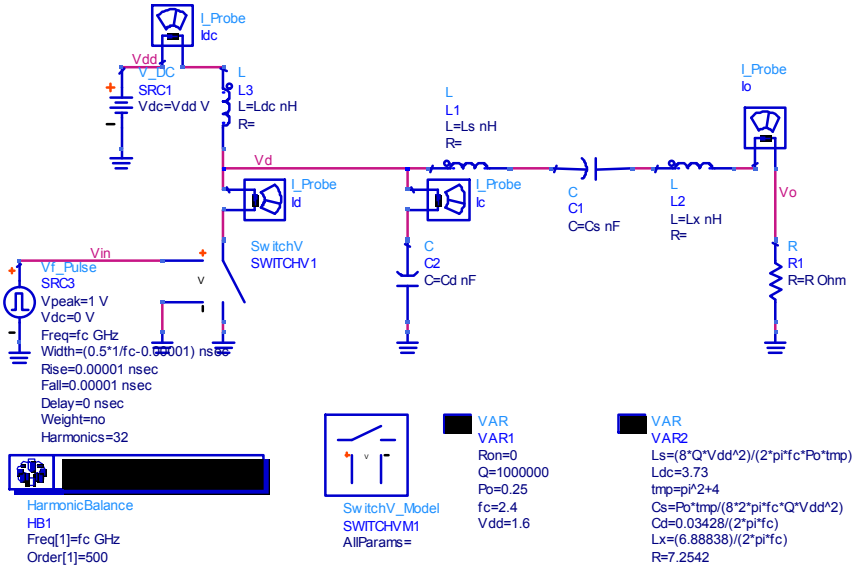

Figure 4.7 Protocol circuit in ADS

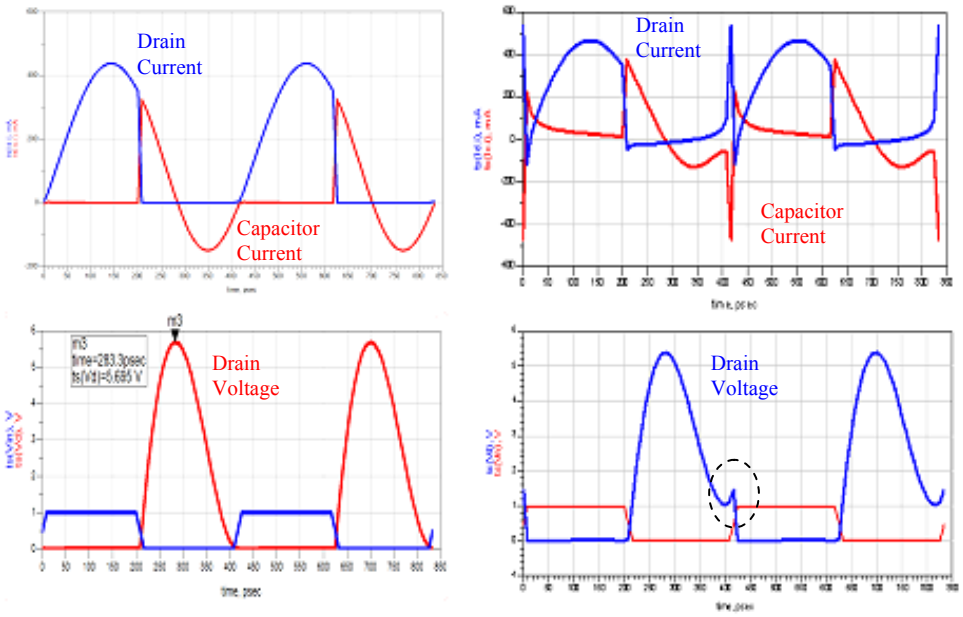

Figure 4.8 Comparison of simulation results using circuit parameters produced by proposed method (left) and Milosevic et al's (right). The amplifier designed with Milosevic et al's equations apparently cannot reach optimum working condition.

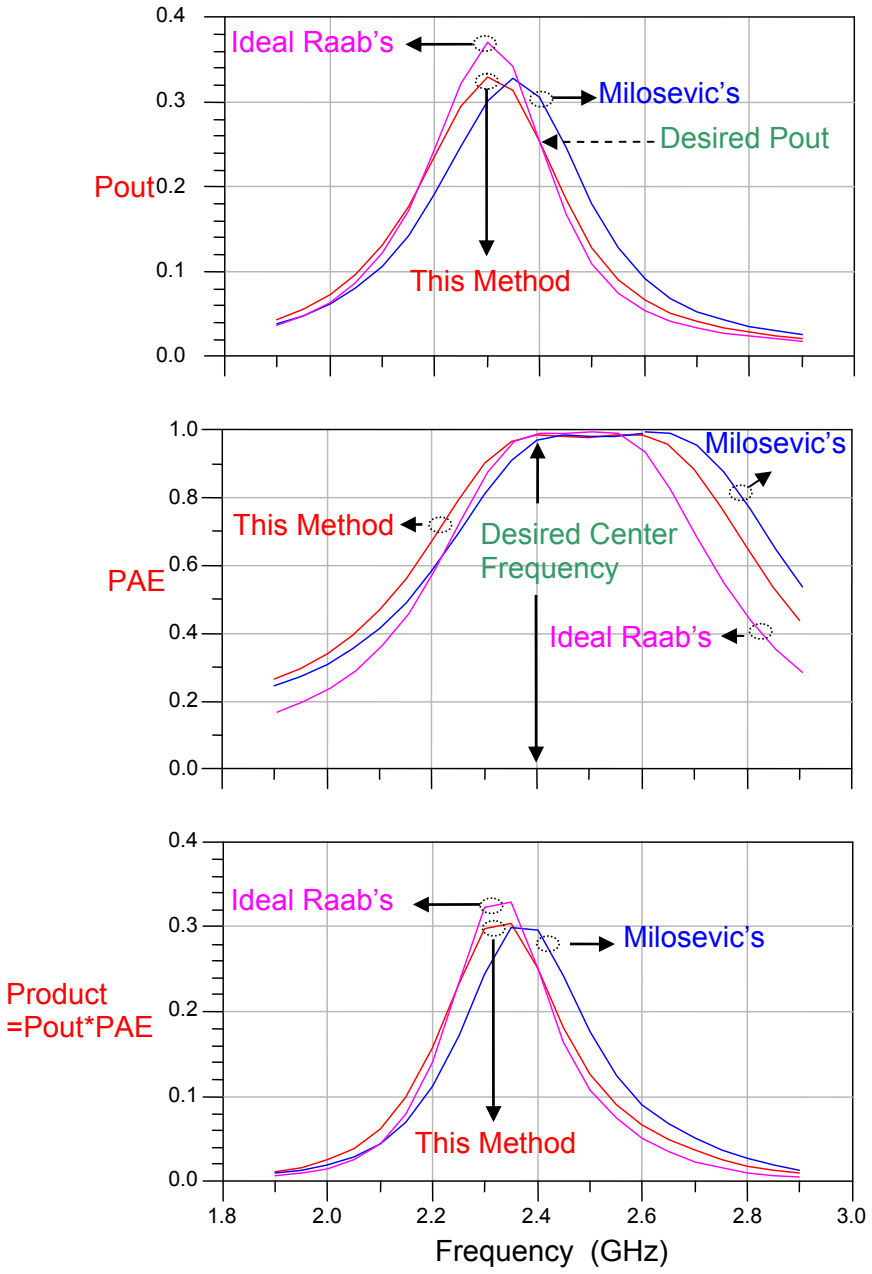

Figure 4.9 Comparisons of different design methods with finite Q load networks

The comparisons shown in Figure 4.8 and 4.9 indicate that this proposed method does exhibit similar performance as the ideal one, while reduces the need for

excess power capability. This method also produces the optimized load network such that zero-voltage and zero-voltage-slope conditions are satisfied at the turn-on instant.

The term "product" is defined as the output power times the power added efficiency. Since that the peak performance shifts from the desired center frequency and the peaks of output power and PAE occur at different frequencies, the geometric mean of these two power performance is more meaningful when finite inductance is employed. The relatively constant product relates to the operation frequency range in which the output power and the power added efficiency vary within acceptable ranges. The difference between the Milosevic's and this design method is minor except that the phase shifts from the center frequency are different. The difference can be reduced by changing the excess inductance. This feature could be useful in the wideband applications.

The employment of inductors of finite quality factors leads to parasitic power losses. The power losses due to parasitic resistance in the DC feed inductor and the inductor of the series-tuned network are given by [13]:

$$P_{loss,Ldc} = \frac{0.5768 r_{dc}}{R} P_o \approx \frac{2.5}{Q_{Ldc}} P_o , \tag{4.45}$$

and

$$P_{loss,Lx} = \frac{r_x}{R} P_o = \frac{\omega L_x}{Q_{Lx} R} P_o = \frac{1.7879}{Q_{Lx}} P_o \tag{4.46}$$

4.2.2 Design of Active Device with Parasitic Effects

The device stresses posed on the transistor can be considered in two scenarios. One scenario is that high switch voltage occurs when the switch is off, leading to possible oxide breakdown. The other case is that high current is required during the switch-on cycle. However, finite conductance g_m generates unexpected performance. Although larger device can produce higher current under the same external bias, the resultant high device capacitance may cause deviation in circuit working conditions, leading to off-optimum working conditions. Therefore complicated tradeoffs are needed in practice.

4.2.2.1 Limitations of Breakdown Voltage

Higher voltage swing leads to higher output power. But the voltage swing cannot be increased unlimitedly. The bottleneck of switch voltage is posed by the low oxide breakdown voltage, which is 4.2V for 0.18μm CMOS. One practical design consideration for the supply voltage of typical one-transistor Class-E power amplifier is given by

$$V_{DD,\max} = \frac{BV}{3.56} = 1.18V \tag{4.47}$$

However, low supply voltage requires high quality output matching network, which is hard to implement in CMOS. Another solution for low breakdown voltage is to use the cascode circuit architecture shown in Figure 4.10. Cascode circuits can effectively reduce the device stress at the cost of larger chip area. The device stress is then posed on the common gate transistor, which is illustrated in Figure 4.11.

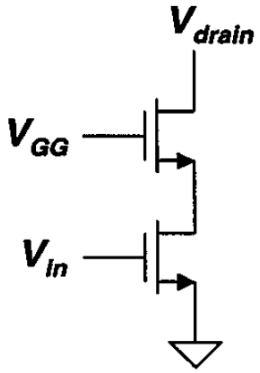

Figure 4.10 Cascode configuration

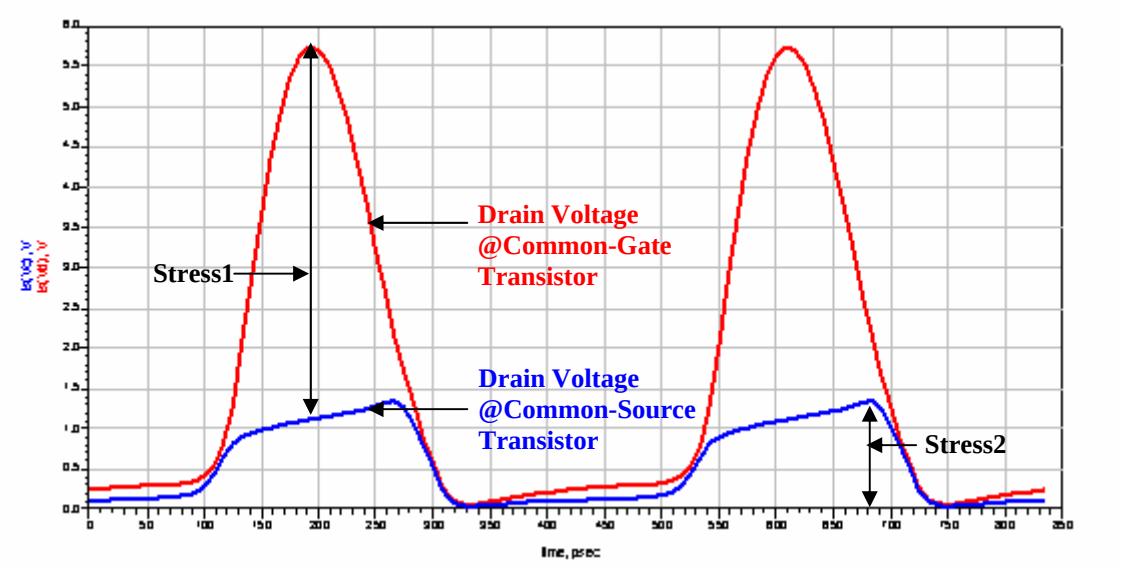

Figure 4.11 Drain voltage waveforms of the common gate
and the common source transistors

The maximum voltage stresses on the oxide for cascode and conventional single-ended structures are

$$V_{stress,M2} = V_{SM} - V_{GG}$$

$$V_{stress,M1} = V_{M2,MAX} - V_{IN,MIN} = V_{GG} - V_{th} - V_{IN,MIN}$$

and

$$V_{stress,M1} = V_{SM} - V_{IN,MIN},$$

respectively. Normally, V_{bias} is set to a voltage level around V_{DC}. Then the maximum stresses in cascode and single-transistor structures are $2.56V_{DC}$ and $3.56V_{DC}$, respectively. Therefore, the maximum supply voltage of cascode topology is

$$V_{DD,\max} = \frac{BV}{2.56} = 1.64V \tag{4.48}$$

If there is a need to exceed this limit, the bias voltage for the cascode transistor should increase to avoid possible oxide breakdown risks.

4.2.2.2 Constraints of Finite Conductance

The constraints of transistor dimension mostly lie in finite conductance and large parasitic capacitance. To avoid large power loss, the drain voltage in Class-E should be ideally kept zero during the switch-on cycle. However, in practice, the conductance is finite. Thus switch voltage is above zero when the transistor is on, which is illustrated in Figure 4.12.

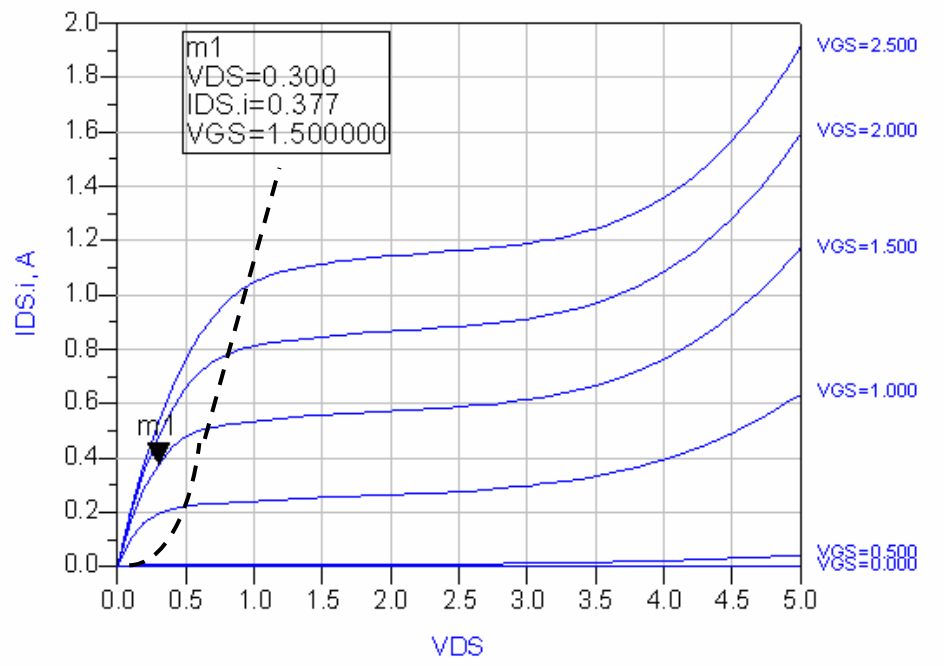

Figure 4.12 DC I-V curves of MOSFET in 0.18μm CMOS

To minimize the power loss due to finite conductance, it is essential to obtain the maximum switch current while keep the switch voltage as small as possible. In practice, the drain voltage during the turn-on cycle is much less than the knee voltage. Therefore, the transistor works within the triode region. The drain current and drain voltage have the relationship such as:

$$i_{ds} = \frac{\mu C_{ox} W}{L}\left(V_{GS} - V_{th} - \frac{v_{ds}}{2}\right)v_{ds} \tag{4.49}$$

To keep the transistor working within the triode region, the drain voltage v_{ds} is set below the knee voltage, i.e., around $0.25Vth$. Drain voltage that is too low leads to large device size or high gate-source voltage, which may cause degradation in overall

efficiency. Since the device works in the triode region, a resistance formed by the conduct channel therefore can be determined as

$$R_{on} \equiv \frac{v_{ds}}{i_{ds}} = \frac{L}{\mu C_{ox} W \left(V_{GS} - V_{th} - \frac{v_{ds}}{2} \right)} \tag{4.50}$$

Raab and Sokal provided an expression for the power loss due to this parasitic resistance in ideal cases [16]:

$$P_{loss,Ron} \approx 1.365 \frac{R_{on}}{R} P_o \tag{4.51}$$

Therefore, reducing the switching-on resistance can improve the efficiency. Two ways are usually adopted to obtain smaller R_{on}: larger device size or higher gate-source voltage. Unfortunately, both methods have side effects. Higher gate-source voltage is hard to reach unless a powerful driver stage is used. Larger device size leads to large parasitic capacitance. Either of two solutions causes some degradation in overall performance of the power amplifier.

4.2.2.3 Impacts of Parasitic Gate Capacitance

Another big concern in Class-E design is the input and output shunt capacitance. When the transistor turns on, the large input capacitance requires long charge time and large input current, which in turn lays strict requirements on the driver stage. The input capacitance C_G in the triode region is composed of channel and overlap capacitances, which can be expressed as

$$C_G = C_{GSO} + C_{GDO} + C_{GC} \tag{4.52}$$

And the gate capacitance needs to be charged to V_{GS} and discharged to about zero. Suppose the input signal is a square wave, this process consumes a DC power of

$$P_{drive} = fC_G V_{GS}^2 \tag{4.53}$$

4.2.2.4 Impacts of Parasitic Drain Capacitance

The output drain capacitance C_D plays a critical role in Class-E amplifier. Two major impacts are usually considered: nonlinear parasitic capacitance and excess drain capacitance. First, nonlinear parasitic capacitance causes higher drain voltage than in ideal case [17]. The nonlinear parasitic capacitance mostly comes from the junction capacitance, which can be expressed as:

$$C' = C_{j0}\left(1+\frac{v_S}{V_{bi}}\right)^{-(n/(n+1))}, \tag{4.54}$$

where $n/(n+1) = MJ$ is a grading coefficient. The maximum drain voltage in an ideal amplifier with nonlinear parasitic capacitance is [17]:

$$v_{SM} = V_{bi}\left\{\left[\frac{3.562V_{DD}}{(n+1)V_{bi}(C_{j0}/C)}+1\right]^{n+1}-1\right\} \tag{4.55}$$

Second, the output drain capacitance determines the maximum operation frequency of the circuit. Smaller capacitance will have higher operation frequency. For an ideal Class-E power amplifier with 50% duty cycle input, the maximum operation frequency is given by [18]:

$$f_{\max}(C,R) = \frac{1}{\pi^3 RC} \tag{4.56}$$

Furthermore, the output drain capacitance C_D directly affects the working condition of Class-E amplifier. As mentioned earlier, the optimum working conditions imply that no charge is left in the shunt capacitor at the instant of turn-on, otherwise power loss will happen. An excess shunt capacitance will take longer to be charged and discharged if the rest conditions remain the same, leading to switching loss. In an ideal case with 50% duty cycle switching, the power loss in the shunt capacitor is calculated by

$$P_{loss,switching} = \frac{1}{2} fC_1 V_{dsw}^2 , \tag{4.57}$$

where V_{dsw} is the drain voltage at the instant the switch closes. V_{dsw} can be determined by the total charge Q deposited in the shunt capacitor:

$$Q = \int_0^{\frac{1}{2f}} [I_{dc} - I_o \sin(\omega t + \phi)] dt \tag{4.58}$$

It follows that

$$Q = \frac{I_{dc}}{2f} - \frac{I_o \cos\phi}{\pi f} \tag{4.59}$$

Recall that $V_{dsw} = Q / C_1$, leading to

$$P_{loss,switching} = \frac{1}{2fC_1} \left(\frac{I_{dc}}{2} - \frac{I_o \cos\phi}{\pi} \right)^2 \tag{4.60}$$

4.2.2.5 Investigation of Manipulating Non-Optimum Waveforms at Turn-on

Under optimum working conditions, the switching power loss should be zero. It can be derived that $\cos\phi$ equals $\pi / \sqrt{4+\pi^2}$ in ideal cases, which is identical to the previous result. As for non-optimum cases, the impact of excess capacitance is

complicated because I_{dc}, I_o and $\cos\phi$ are affected at the same time, leading to both PAE and output power degradation. Since the optimum condition is uniquely determined by the load network, any unexpected variation in the load network will result in non-optimum phenomena. If a component shifts from the expected value, the impacts can be compensated by adjusting the rest elements. This method is demonstrated with an example of excess shunt capacitance.

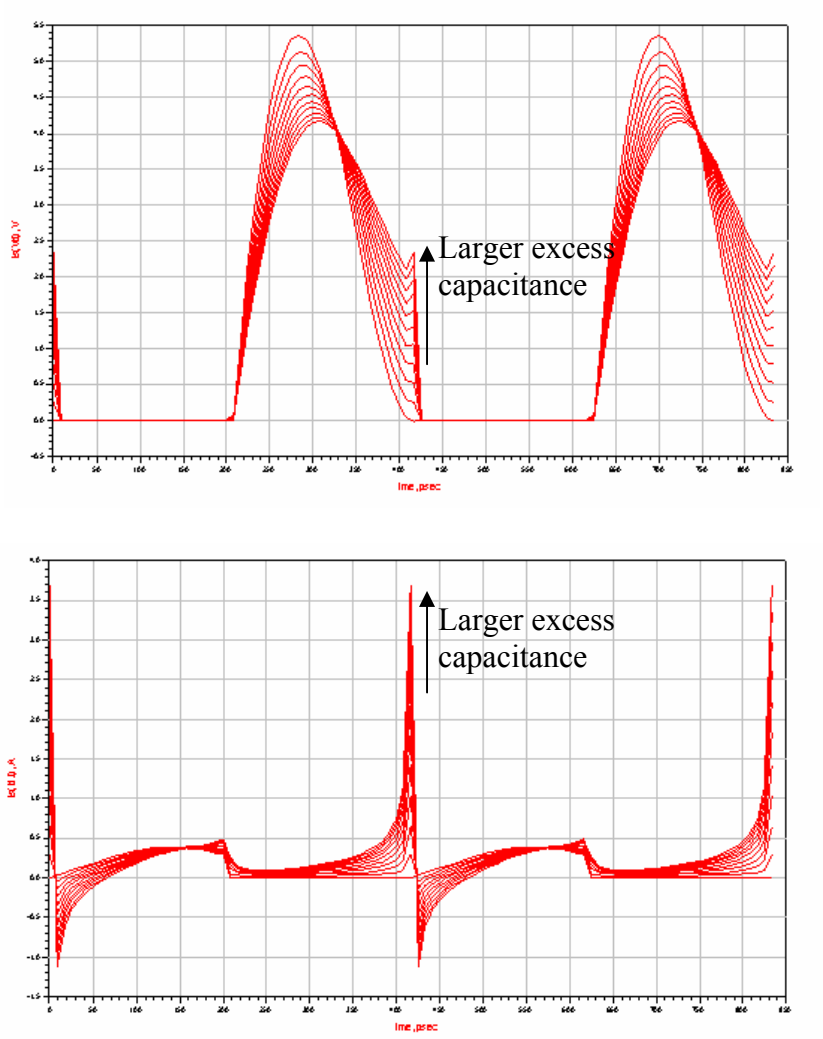

Figure 4.13 Impacts of excess drain capacitance on drain waveforms

The impacts of excess shunt capacitance on the optimum working conditions are illustrated in Figure 4.13. It is clearly shown that the larger excess capacitance, the higher drain voltage at the instant of turn-on, resulting in more dissipated charges.

Because the high current occurs as a pulse, the power loss is not so significant if the excess capacitance is less than 50% of the predicted. However, the output power level degrades apparently. Figure 4.14 shows that the output power degrades faster than PAE. From the figure, we know that when 100% excess capacitance exists, the output power shrinks to 81% although the PAE remains 90.9%. Obviously, other approaches must be adopted to remedy the degradation of the output power.

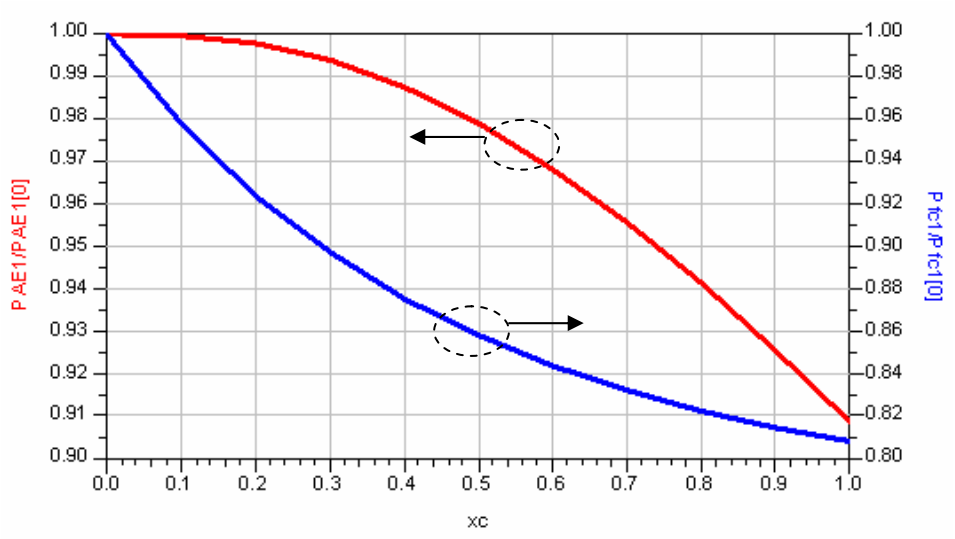

Figure 4.14 Normalized PAE and output power degradations due to excess capacitance

From Figure 4.13, we know that the drain voltage at the instant of switching-on is proportional to the shunt capacitance, or the time constant RC. To reduce this harmful drain voltage, one can reduce the time constant by decreasing the value of R.

The results of this method are illustrated in Figure 4.15. This method can improve the PAE but the output power level remains the same. To obtain desired output power level, one further step is to increase the supply voltage a little bit since P_o is proportional to V_{DD}^2 / R. The results is shown in Figure 4.15 and 4.16.

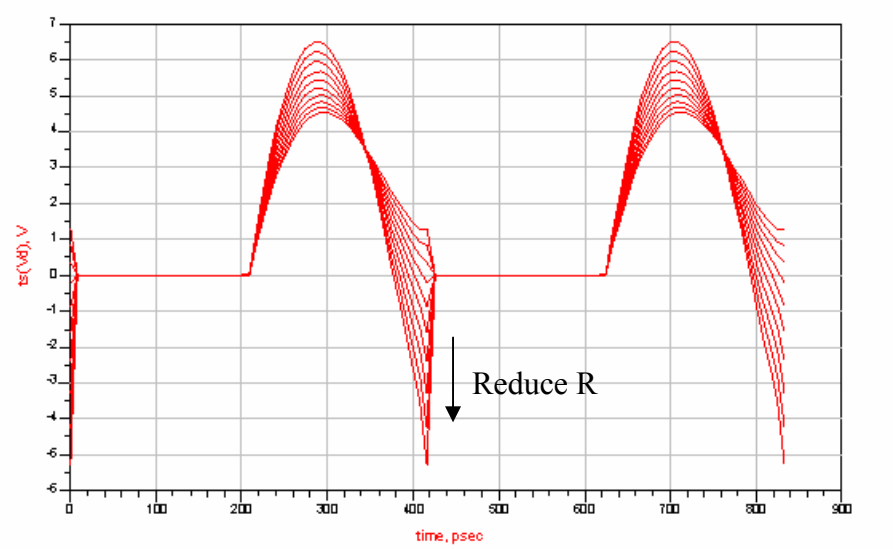

Figure 4.15 Reduce the drain voltage at the turn-on by decreasing the time constant

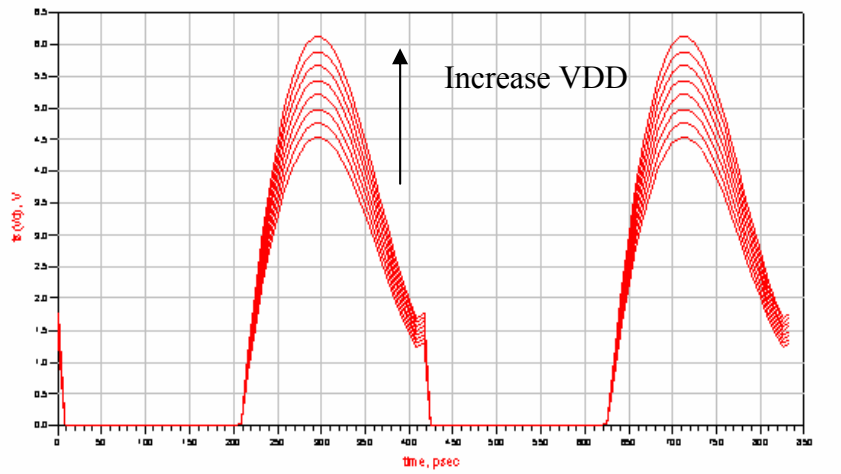

Figure 4.16 Change of the supply voltage to reach the desired output power

From Figure 4.16, one can expect that the power efficiency would roughly remain constant because the drain voltages at the turn-on are nearly unchanged, while the output power will be enhanced as the supply voltage increases. The results in Figure 4.17 verify these points.

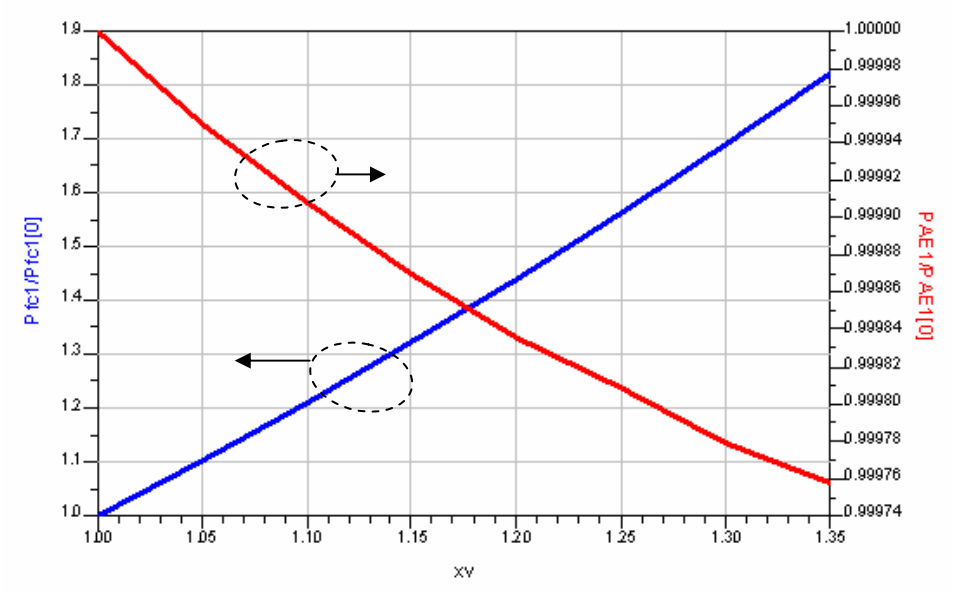

Figure 4.17 Impacts of increased supply voltage

From the previous analysis, it is shown that excess drain capacitance leads to significant degradations in PAE and output power. To reduce such impacts and restore optimum working conditions, designers can increase the supply voltage and reduce the load at the same time. For example, if there is 50% excess capacitance, resulting in 14% degradation in the output power, the supply voltage should be increased by $\sqrt{1/(1-14\%)} = 1.08$, which is shown in previous figures. And the load resistance needs to be reduced to $1/1.5 = 66.7\%$ of the original value. Through the comparison of circuit

performance before and after this solution is applied, which is depicted in Figure 4.18, we can see the validity of this practical solution.

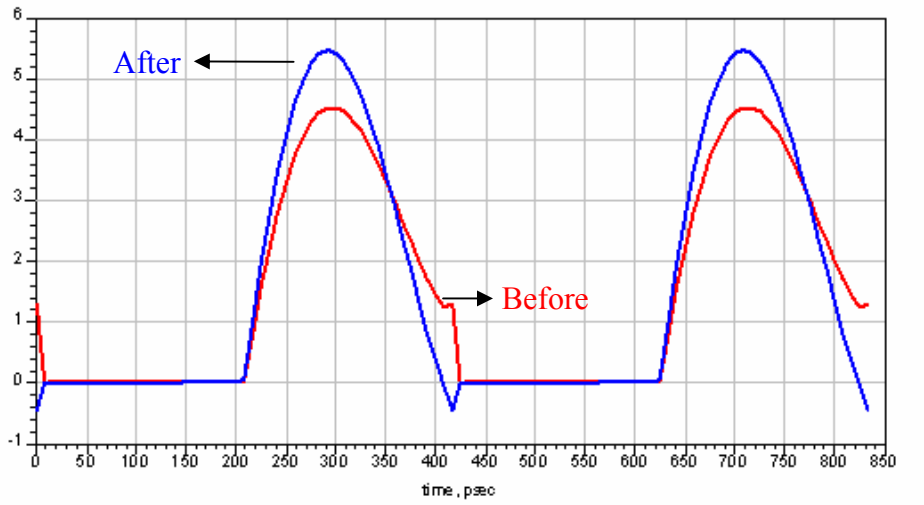

Figure 4.18 Comparison of the drain voltages before and after compensation solution. The normalized output power increases from 0.86 to 0.995 after compensation.

These manipulation methods discussed here can be extended to handle general non-optimum waveforms which don't meet the ZVS criterion.

CHAPTER 5

PA IMPLEMENTATION AND SIMULATIONS

In this chapter, the detailed design and simulations of a Class-E RF power amplifier in 0.18μm CMOS technology are presented. This design is discussed in four parts: on-chip inductor, amplifier stage, pre-amplifier stage, and matching networks. Then the whole circuit will be tested by simulation.

5.1 Design Specifications

Table 5.1 Power amplifier specifications for 2.4GHz WLAN

Parameters	Specification
Applicable Input power (Typical)	From -10dBm to 6dBm (0dBm)
Output power	23dBm
Maximum gain	33dB
Power Added Efficiency	50%
Center frequency	2.4GHz

The RF PA supposedly is capable of delivering 23dBm power to a typical 50Ω load with high efficiency at 2.4GHz, and offers the maximum power gain of 33dB for the typical RF input.

5.2 Design of On-Chip Spiral Inductor

5.2.1 Models for On-Chip Spiral Inductor

Inductor is crucial in monolithic RF design. Good inductors will significantly relief the constraints on other design parameters. However, high quality inductors are difficult to be implemented in bulk CMOS due to parasitic losses. Therefore, in Mixed-single/RF CMOS processes, the option of a thicker top metal layer is available for implementing on-chip inductors with higher quality factors than in normal logical processes.

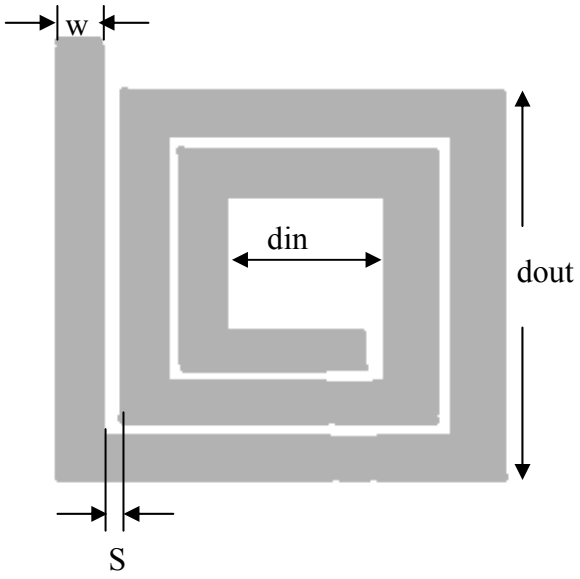

Figure 5.1 Illustration of a 2.5-turn square spiral inductor

Process- and design-controlled parameters are needed to model on-chip inductors. Process-controlled parameters include oxide thickness, metal thickness, pitches, permeability, substrate depth and resistivity. Design-controlled parameters include metal width, number of turns, centre spacing, metal line spacing. The most common types of planar inductors include square, hexagonal, octagonal, and circular

spiral inductors. Due to less DC current and eddy current losses, circular spiral inductors have the best quality factors among all, while square ones are the simplest to manufacture. For simplicity purpose, only square spiral inductors are used in this work. A typical π -structure inductor model shown in Figure 5.2 is widely employed to simulate the performance of the on-chip design. In this model, L_S is the inductance of the planar; R_S, C_P, and C_{ox} are parasitics; R_{Sub} and C_{Sub} stand for the substrate loss.

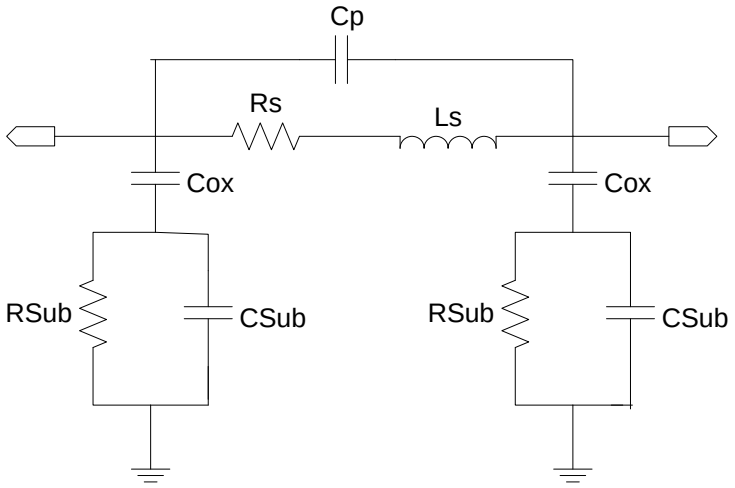

Figure 5.2 A regular symmetrical model for spiral inductor

The model parameters for an n-turn square planar inductor can be estimated by using the following formula [19]:

$$L_S \approx \frac{9.375\mu_0 n^2 d_{avg}^2}{11d_{out} - 7d_{avg}} \qquad R_S \approx \frac{l}{w\sigma\delta(1-e^{-t/\delta})}$$

$$C_{ox} = \frac{1}{2} wl \frac{\varepsilon_{ox}}{t_{ox}} \qquad C_P = nw^2 \frac{\varepsilon_{ox}}{t_{ox}}$$

$$C_{Sub} \approx \frac{wlC_{sub0}}{2} \qquad R_{Sub} \approx \frac{2}{wlG_{sub0}},$$

where

μ_0 : vacuum permeability of $4\pi \times 10^{-7} H/m$.

σ : conductivity of the metal, For Aluminum, $\sigma = 3.538 \times 10^7 S/m$.

δ : skin depth given by $\delta = \sqrt{\frac{2}{\omega \mu_0 \sigma}}$, for Aluminum material at 2.4GHz, the skin depth is 1.81μm. The top metal layer of 0.18μm CMOS has a thickness of 2μm, which is good enough for this design.

G_{sub0} / C_{sub0} is a process-dependent parameter.

Two important indexes for inductors are quality factor and self-resonant frequency. The definition of quality factor Q of an inductor is a measure of the energy storage capability.

$$Q = 2\pi \frac{\left|\text{Net energy stored in one ac cycle}\right|}{\text{Energy dissipated in one ac cycle}} = \frac{\text{Im}(Z)}{\text{Re}(Z)}$$

$$L = \frac{\text{Im}(Z)}{\omega}$$

5.2.2 Simulations for On-Chip Spiral Inductor

ASITIC, one small computer software for inductor design and simulation, is used here to calculate all the parameters of the inductor model. Applying the 0.18μm CMOS process parameters in ASITIC, one can find out a 4.5-turn square spiral inductor has a series inductance of 3.807nH at 2.4GHz. This tool also gives a corresponding six-component asymmetrical model. To verify this result, electrical-magnetic momentum simulation for the actual layout is carried out in ADS. The comparison of these two

methods, which is illustrated in Figure 5.3 through 5.8, shows good agreement between these tools. Therefore, we can use ASITIC to generate alternative models for the on-chip inductors.

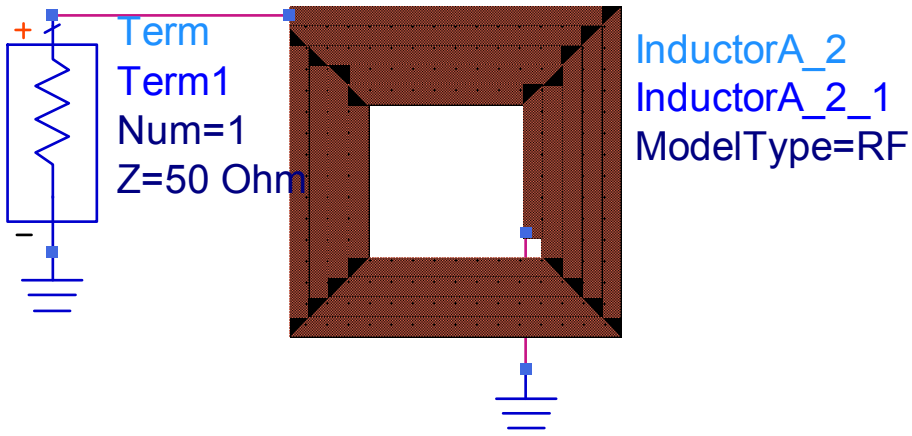

Figure 5.3 Momentum simulation circuit for the actual inductor layout

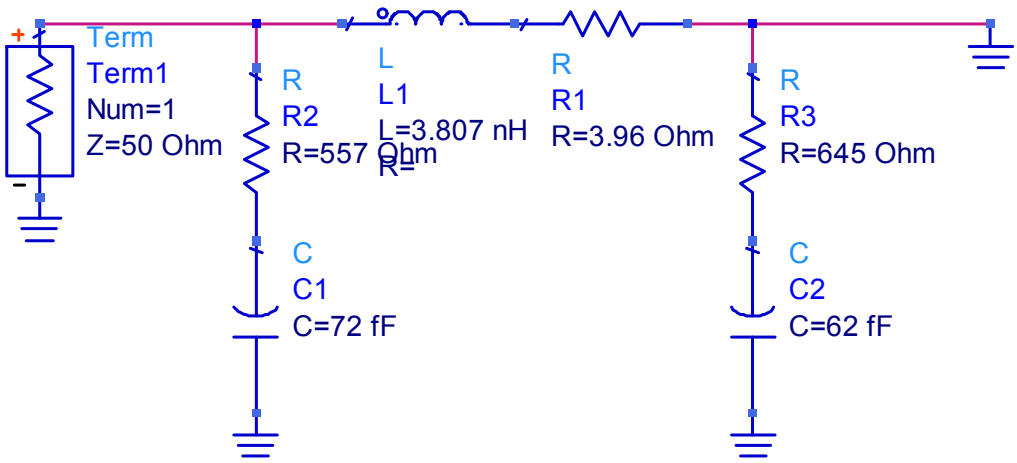

Figure 5.4 Simulation for the lumped-component spiral inductor model

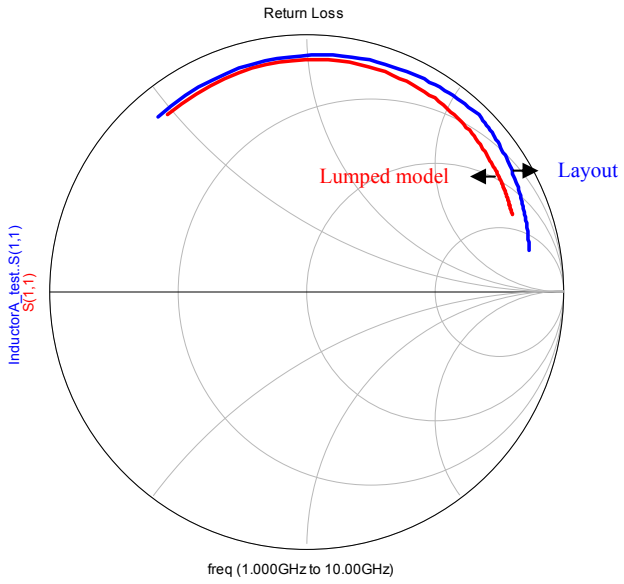

Figure 5.5 Good agreements of S-parameter simulations for the actual layout and the lumped component model

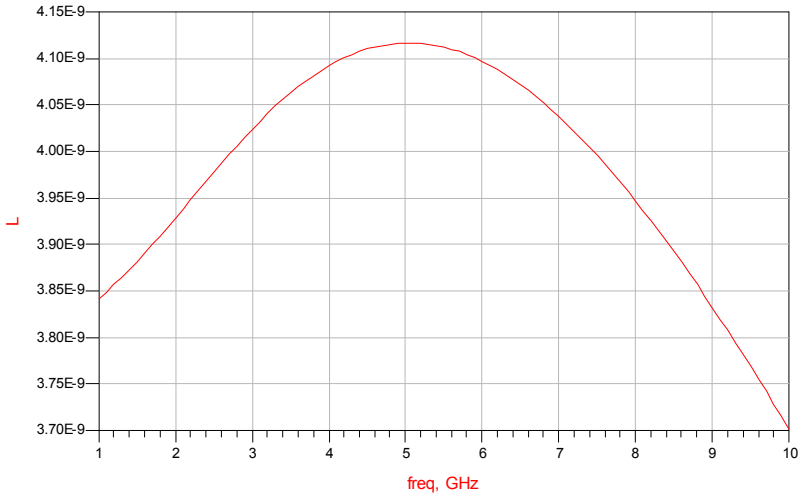

Figure 5.6 The inductor has 3.95nH at 2.4GHz

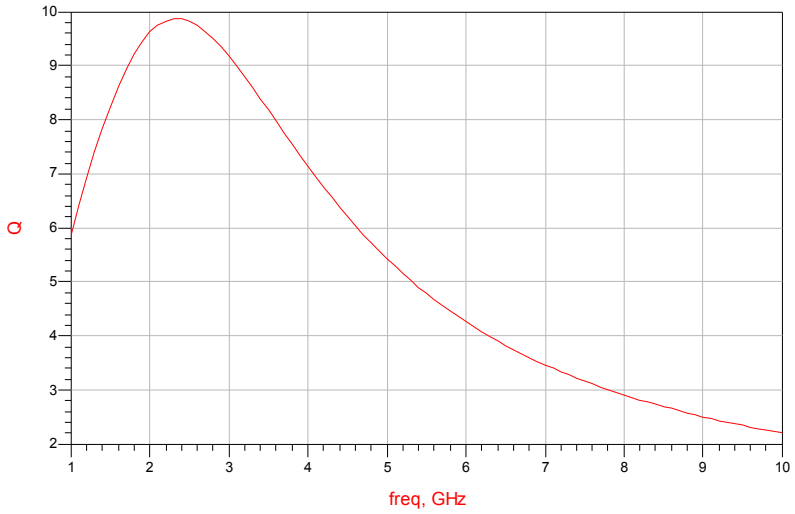

Figure 5.7 The quality factor of the inductor varies with frequency.

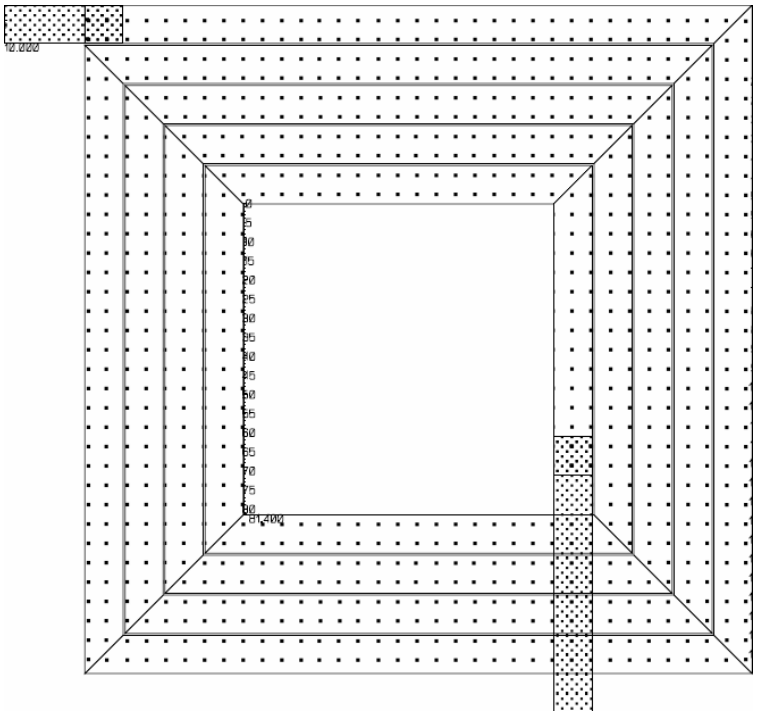

Figure 5.8 Layout of the square spiral inductor of 3.65nH at 2.4GHz

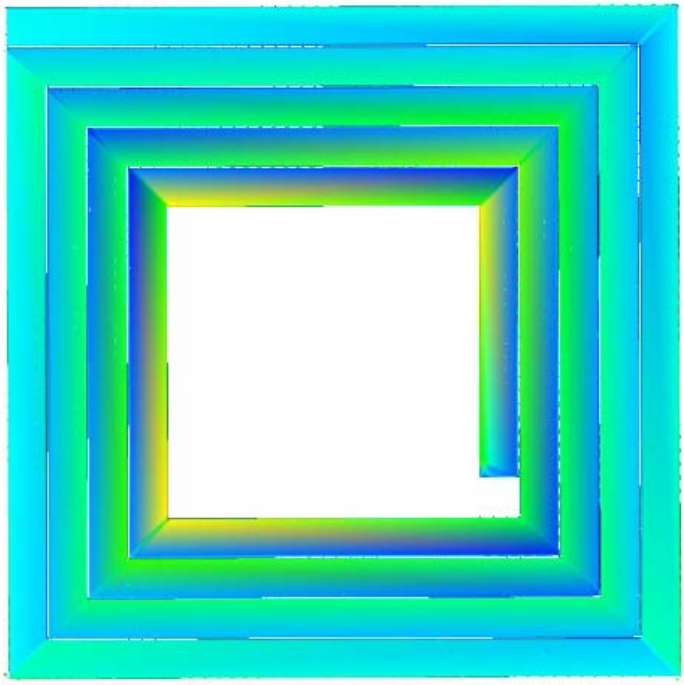

Figure 5.9 Current density distribution in this square spiral inductor at 2.4GHz. Asymmetrical circuit models are preferred due to the non-uniform current density.

5.3 Output Stage Design and Simulations

5.3.1 Protocol Amplifier Design and Verification

Initially assuming that the supply voltage is 1.5V and the finite DC feed inductor is 3.807nH, the initial values for the circuit components in the load network can be determined by applying the proposed design equations.

$$X_{dc} = 2\pi f \times L_{dc} = 57.408\Omega$$

$$R_{dc} = \frac{V_{DD}^2}{P_o} = 11.25\Omega$$

Therefore the design variable m is

$$m = \ln(X_{dc} / R_{dc}) = 1.63$$

The calculated results are listed in Table 5.2.

Table 5.2 Initial circuit parameters used in the power stage

Name	Value
Operation frequency f	2.4GHz
Required output power P_o	200mW
Supply voltage V_{DD}	1.5V
Finite DC feed inductor L_{dc}	3.807nH
Optional load resistance R	8.1Ohm
Excess reactance X	7.561Ohm
Shunt susceptance B	0.03142 S

The protocol circuit and its simulation result are illustrated in Figure 5.10 and 5.11, respectively.

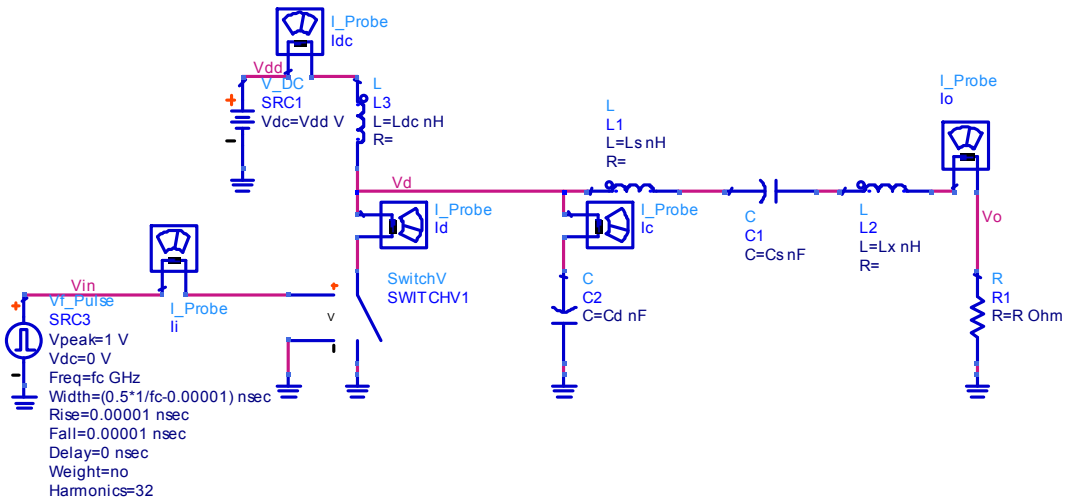

Figure 5.10 Protocol circuit for verifying the load network design

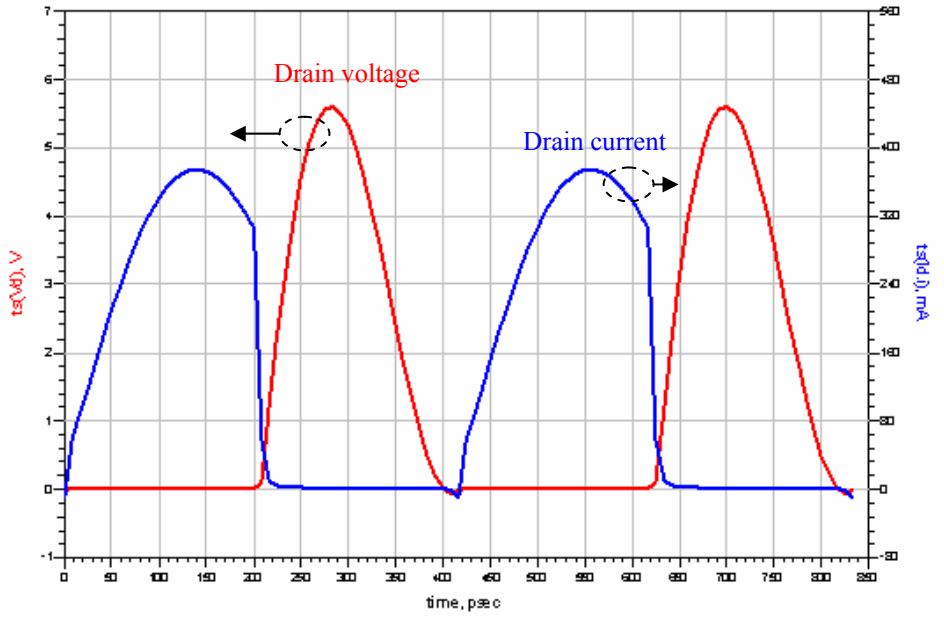

Figure 5.11 Nominal drain current and voltage waveforms

The protocol circuit is capable of delivering 201mW power to the load with 99.8% efficiency. The maximum drain voltage is 5.4V. And the maximum switch current is 376mA. These results provide a guideline for the design of the transistor.

5.3.2 Practical Output Stage Design

In this section, the ideal switch is replaced by real transistors. Since the drain voltage has exceeded the oxide breakdown voltage, the cascode topology is adopted in this active device design. The bias voltage V_{GG} for the common gate transistor is determined by

$$V_{GG} > 3.6V_{DD} - BV = 1.2V$$

A good practice is to make V_{GG} equal to V_{DD}.

From the design specification, the peak switch current can be calculated as

$$I_{SM} = 2.84 I_{dc} = 2.84 \frac{P_o}{V_{DD}} = 378mA,$$

which is close to the simulation result in the protocol circuit. Based on this requirement of the drain current, the initial value for the device size can be calculated by:

$$W \geq \frac{4 I_{SM} L}{\mu_n C_{ox} \left(V_{GS} - \frac{9}{8} V_{th} \right) V_{th}},$$

where

$\mu_n C_{ox}$ is $351.2 \mu A / V^2$ for the 0.18μm CMOS

V_{th} is the threshold voltage of 0.5V

V_{GS} is the input voltage at the common source transistor. Typically it is equal to V_{DD} for square wave inputs.

As a result, the transistor should have the minimum device width of $1650 \mu m$ to conduct the desired switch current. In practice, transistors of such large width are typically implemented in an interdigital style. If a finger has a width of $30 \mu m$, at least 55 fingers are needed.

With the device width known, we can evaluate the impacts of the parasitic capacitances C_G and C_D. Since the effect of the gate-to-drain capacitance is eliminated by the cascode topology, the gate capacitance C_G in the resistive mode is

$$C_G = C_{ox} W L_{eff} + 2 C_{ox} x_d W = C_{ox} W L \approx 2.52 pF$$

The large gate capacitance requires the previous stage to provide a large amount of driving power. The power can be estimated as

$$P_{drive} = fC_G V_{GS}^2 = 13.4mW ,$$

which is significant compared to the desired output power. This impact can be alleviated by tuning out the gate capacitance or employing some positive feedback circuits to boost the input signal.

For the cascode topology, the common gate transistor works within the saturation region. The drain capacitance C_D is then composed of the gate-to-drain overlap capacitance, the junction capacitance and the sidewall capacitance.

$$\begin{aligned} C_D &= C_{GDO} + C_{DB} \\ &\approx WC_{gd0} + WL_d \frac{C_J}{\left(1 + v_d / V_{bi}\right)^{MJ}} + \left(W + 2L_d\right) \frac{C_{JSW}}{\left(1 + v_d / V_{bsw}\right)^{MJSW}} \end{aligned}$$

The transistor characteristics for 0.18μm CMOS are $L_d = 5\lambda$, $C_J = 0.98\, fF / \mu m^2$, C_{JSW} = $0.22\, fF / \mu m$, the junction grading coefficient $MJ = 0.36$, the sidewall grading coefficient $MJSW = 0.10$, and $\psi_0 = 0.75V$. Thus the drain capacitance C_D can be about 1.4pF, which is less than the required shunt capacitance for the optimum Class-E. Hence an external output capacitance is needed.

If the device width is 1650μm, the switching-on resistance is calculated by

$$R_{on} = \frac{v_{ds}}{i_d} \cong \frac{L}{\mu C_{ox} W (V_{GS} - V_{th} - \frac{v_{ds}}{2})} = 0.33\Omega$$

Therefore the drain efficiency will be lower than the unity due to the thermal power loss.

$$\eta = \frac{1}{1+1.365\frac{R_{on}}{R}} = 0.946$$

When the drive power is considered, the maximum PAE can be estimated as

$$PAE \approx \frac{P_o - P_{in}}{P_o + P_{loss,Ron} + P_{drive} + P_{loss,passive} + P_{loss,switching}}$$

$$\approx \frac{1}{1+1.365\frac{R_{on}}{R}+\frac{1}{G_P}}$$

$$PAE\max = 0.86$$

The design of the output stage is shown in Figure 5.12. The drain voltage waveforms are illustrated in Figure 5.13.

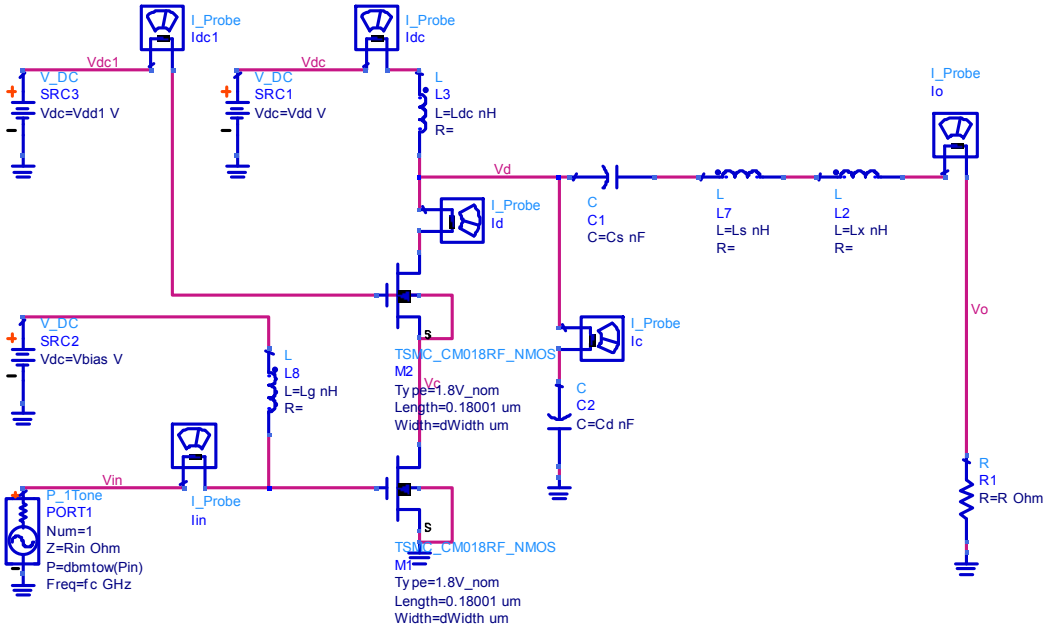

Figure 5.12 Practical cascode output stage

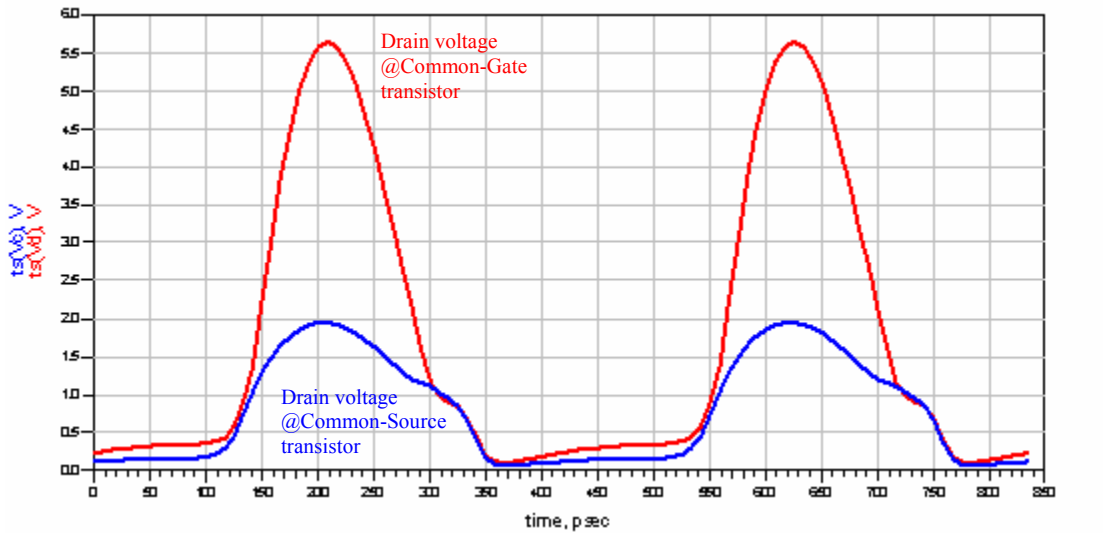

Figure 5.13 Drain voltage waveforms for practical cascode output stage

For a given technology, enhancing the size of the transistor is the typical way to reduce the switching-on resistor. However, large transistors have significant parasitic capacitance, which may cause non-optimum problems. Therefore, the upper-limit of the transistor size is posed by the required optimum shunt capacitance. Figure 5.14 shows that this limit can be extended by increasing the supply voltage. In this case, the maximum device width is 2500μm.

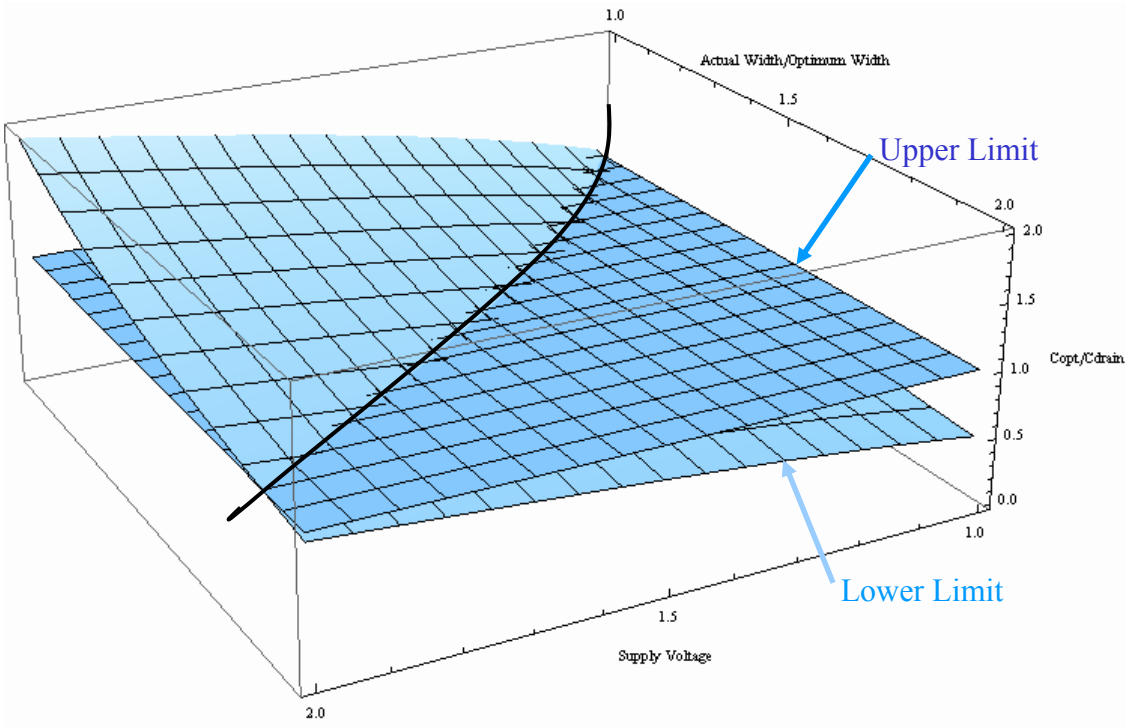

Figure 5.14 Upper and lower limits of device width

The optimized device width can be determined by comparing the circuit performance with different device configurations, which is illustrated in Figure 5.15. The device width is chosen such that the requirement of the output power is met while high efficiency is achieved at the same time. From Figure 5.15, the optimized device width is found to be 2100μm.

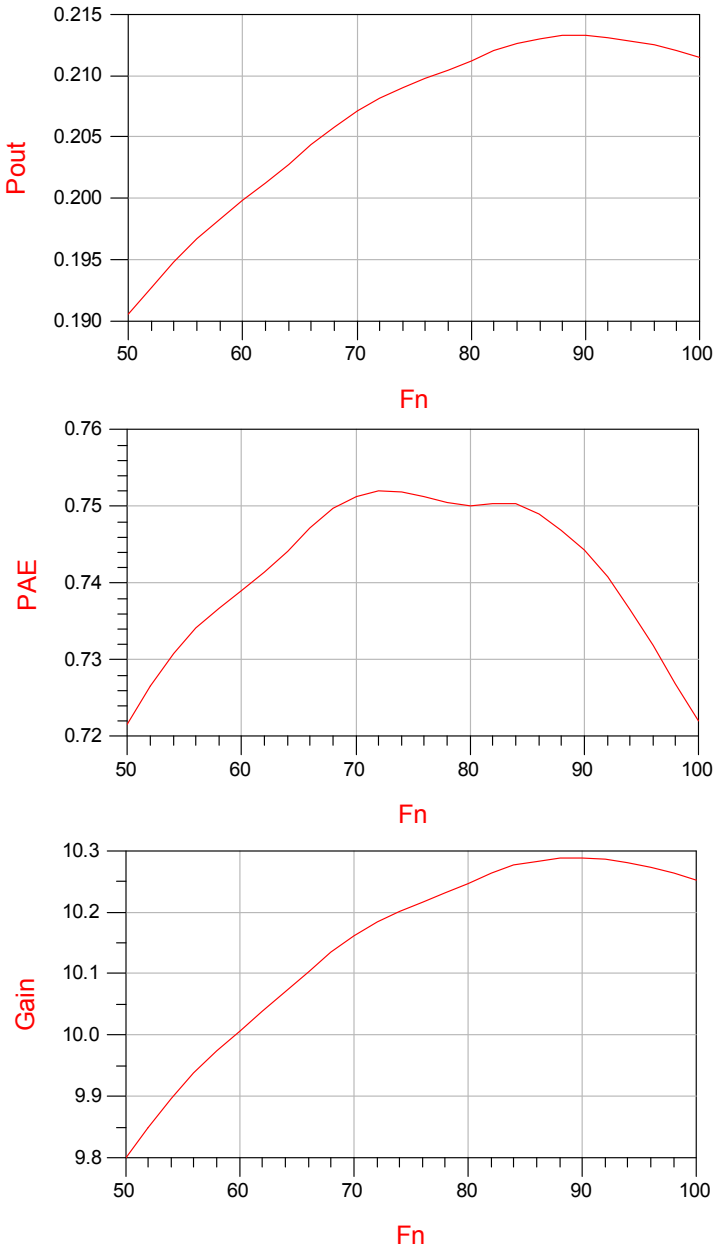

Figure 5.15 Impacts of device width. To obtain the optimized performance, the device width is increased to 2100μm.

With the known active device and the load network, the simulation of the output stage can be carried out. The simulation results indicate that this power stage provides 82.5% PAE when the G_p is 15dB. If the input is too small, it will result in an incorrect output, which is illustrated in Figure 5.16. Therefore, a preamplifier is needed to provide enough gain for the small inputs.

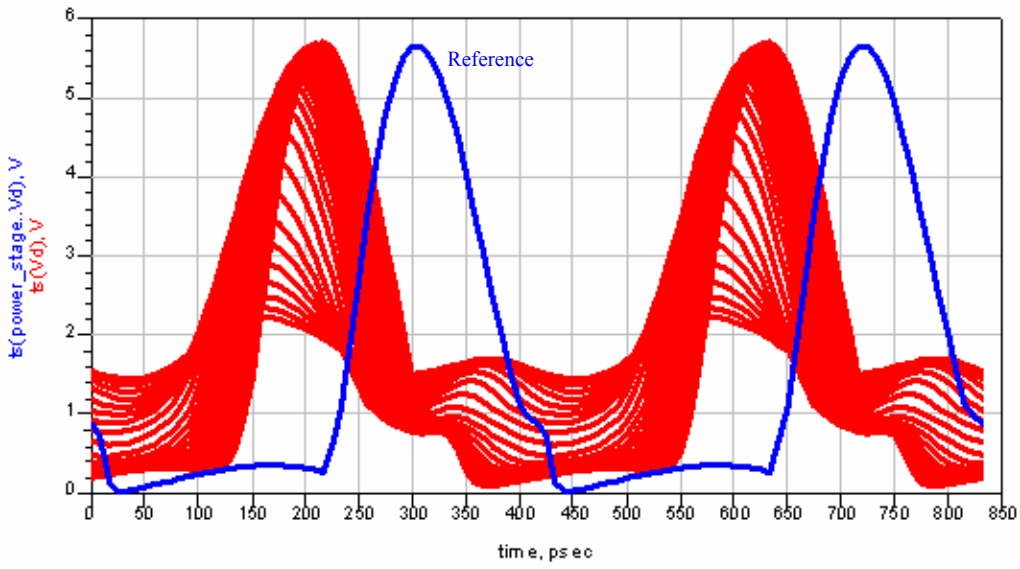

Figure 5.16 Drain voltage shrinks due to reduced input power

5.4 Preamplifier Stage Design and Simulations

The purpose of the drive stage is to provide sufficient gain for the small inputs and to shape the voltage waveform for the final stage. For an input of -10dBm power, the drive stage should provide 23dB gain so that the final stage can be driven by an input of 13dBm power. Hence, the preamplifier stage should have high gain. Besides the power, the drive stage needs to produce input signal of suitable waveforms for the output stage. The ideal input for the Class-E circuit has a trapezoid waveform [10].

However, it is hard to generate square-wave signals at GHz frequencies. One practical solution is to approximate the square wave by summing a finite number of harmonics, which can be implemented in Class-F amplifiers. Therefore, the preamplifier stage is composed by a Class-F amplifier.

In this design, a simplified Class-F/F^{-1} amplifier is implemented. This amplifier only makes use of the fundamental and the third-order harmonics to approximate the square wave. Theoretically, this amplifier can achieve 87.5% drain efficiency. The idea of a Class-F^{-1} amplifier is illustrated in Figure 5.17.

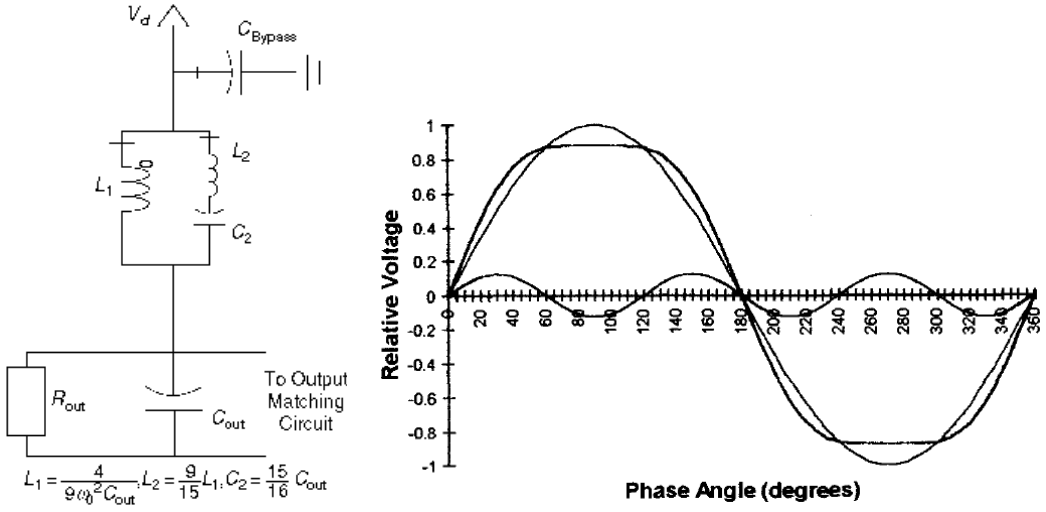

Figure 5.17 Third-harmonic peaking circuit design
and approximated square waveform [20]

The design is shown in Figure 5.18. The tank connecting the power supply and the drain is tuned to the third harmonic. The input capacitance of the output stage and the corresponding tuning inductance form the peaking circuit for the fundamental frequency.

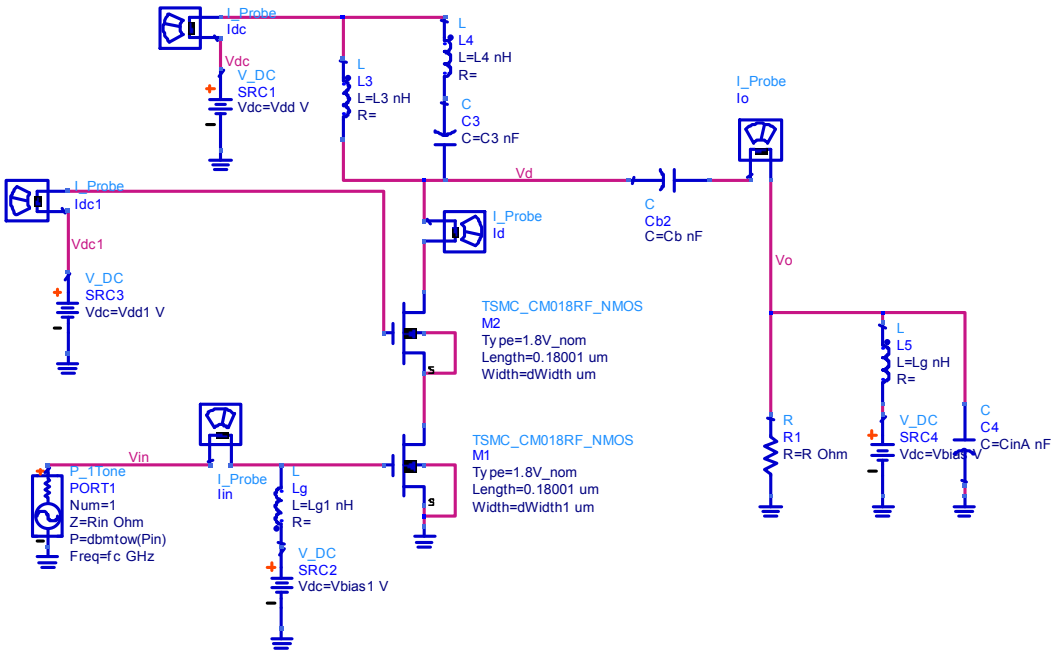

Figure 5.18 Simplified Class-F drive stage

The amplifier structure in the drive stage is similar to the one in the final stage, except the bias voltage and the device size. The common-source transistor in the drive stage is biased such that it can work as Class-AB. The cascode structure used here is for larger output impedance, thus leading to higher gain. It is noteworthy that two transistors work within the saturation region.

The output waveforms of the drive stage in Figure 5.19 demonstrate the effects of shaping the drain voltage and current waveforms. The relatively flat top curve is produced by using the third harmonic peaking circuit.

The simulation result in Figure 5.20 shows that the drive stage can provide 20dB gain for typical RF inputs. When the 0dBm power is fed into the driver stage, 15.12dBm power is delivered to the load with 62.5% power added efficiency.

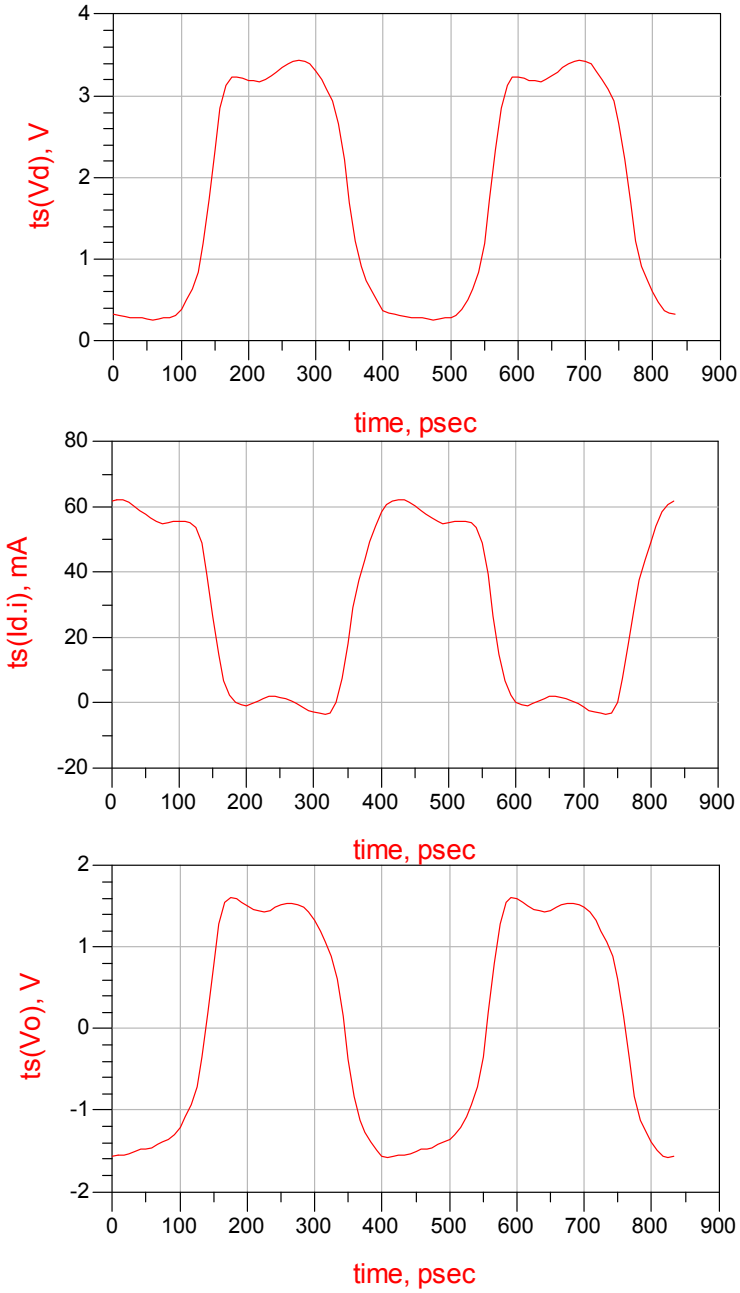

Figure 5.19 Drain voltage, drain current and output waveforms of the drive stage

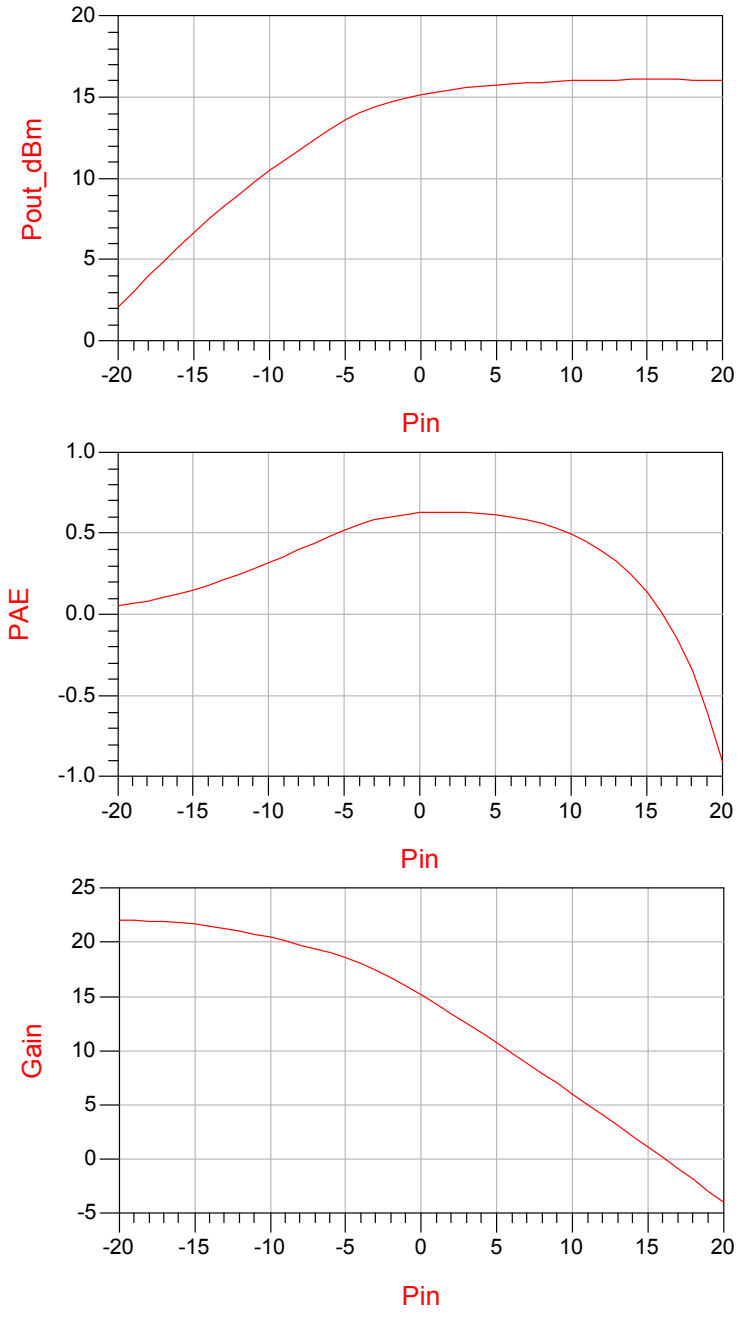

Figure 5.20 Power performance of the drive stage

5.5 Impedance Matching Network Design

The impedance matching network is an essential content of RF circuit design. The purpose of the impedance matching network is to reduce the reflection power loss and deliver as much as possible power from the source to the load. Typically, input and output impedances of a module need to be transformed to a common resistance, i.e., 50 Ohms. Since input and output impedances are related, it is difficult to determine input and output matching networks of the circuit simultaneously. Fortunately, the output impedance is known in this case. Thus, in practice, we can design the output matching network first, and then solve the input matching network with the aid of computer.

The output matching network is shown in Figure 5.21. In Figure 5.22, it shows that the return and insertion losses of this output matching network are -66dB and 0dB, respectively.

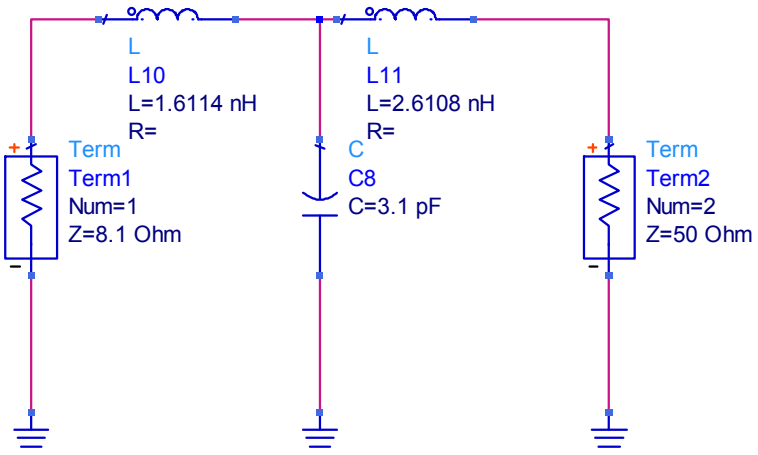

Figure 5.21 Narrowband output impedance matching network

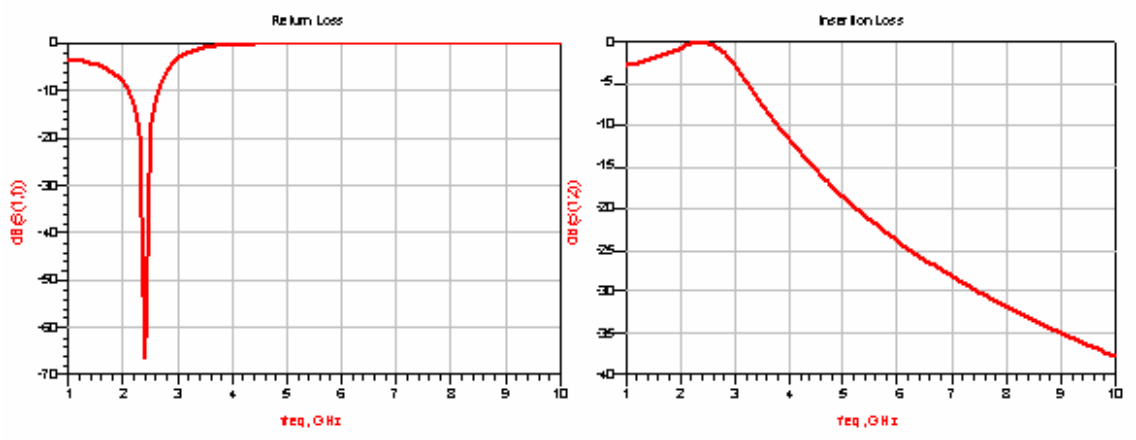

Figure 5.22 Return and insertion losses of this narrowband output matching network

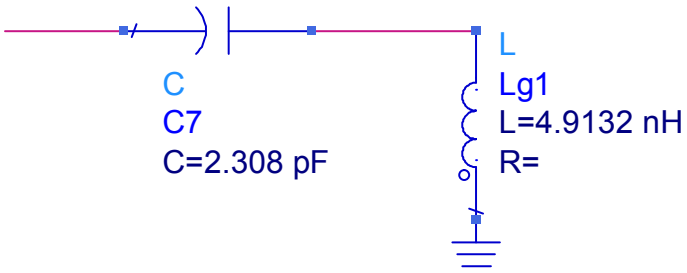

Figure 5.23 The input impedance matching network

5.6 Full Circuit Simulations

The full schematic of the two-staged Class-E power amplifier is given in Figure 5.24. Input and output matching networks are developed for 2.4GHz fixed carrier frequency. The input power is set to the typical value, 0dBm.

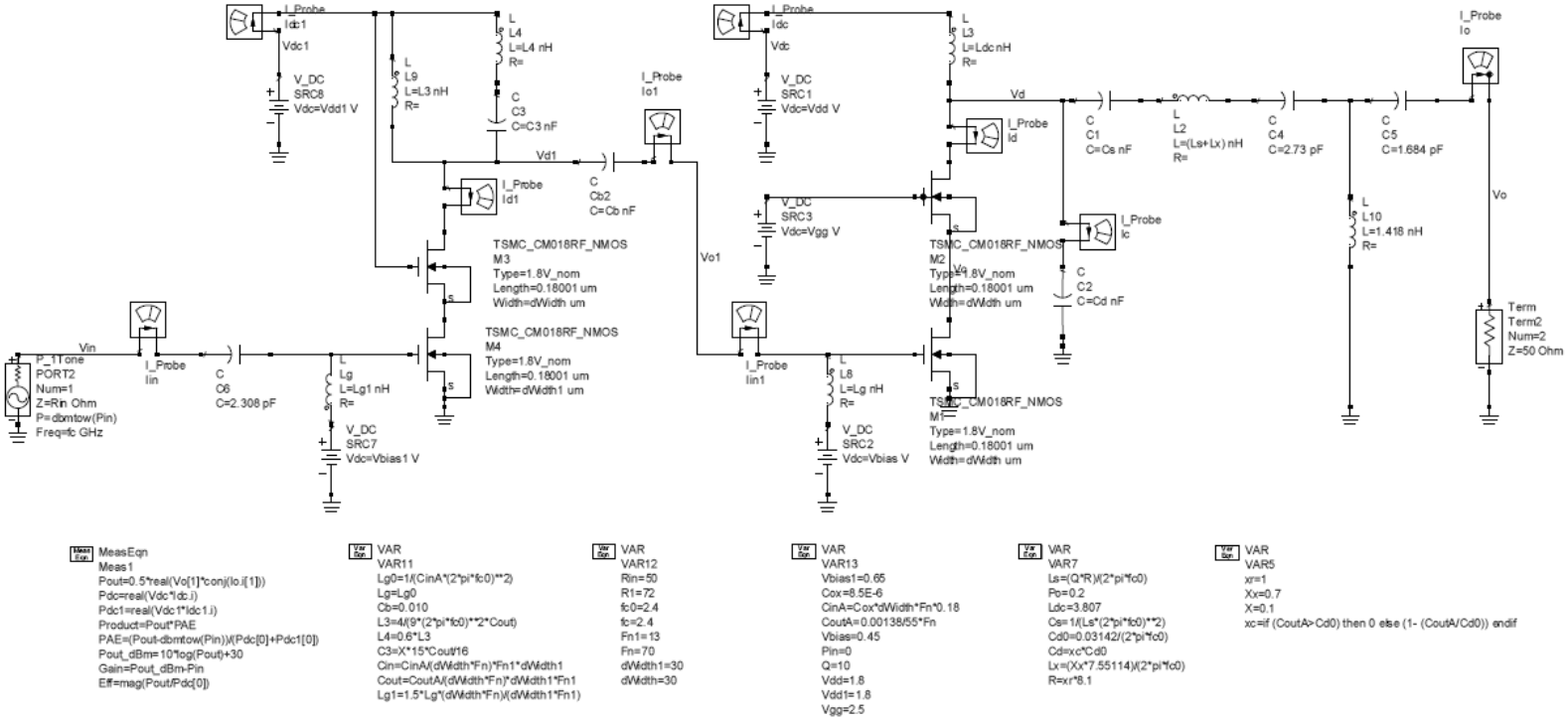

Figure 5.24 Schematic of narrowband two-staged power amplifier

Table 5.3 Circuit component values

Circuit Components	Value
Terminal Impedance R_S, R_L	50Ω
Source Impedance Matching C7, Lg1	C7=2.308pF Lg1=4.9132nH
Third Harmonics Tuned Circuit C3, L3, L4	C3=235.3fF L3=7.7868nH, L4=4.672nH
Interstage Matching Lg	Lg=1.745nH
Finite DC feed inductor Ldc	3.087nH
Shunt capacitance C2	541.7fF
Series Tuned circuit Cs, Ls	Cs=818.7fF Ls=5.3715nH
Excess Conductance Lx	Lx=0.5 nH
Output Matching Network C4,C5, L10	C4=2.73pF, C5=1.884pF L10=1.458nH
Transistors in Drive Stage	M1=M2=390/0.18 M3=M4=2100/0.18
Supply Voltage	Vdd=1.8V
Bias Voltages	Vbias=0.45V Vbias1=0.65V Vgg=2.5V

5.6.1 Basic Evaluations

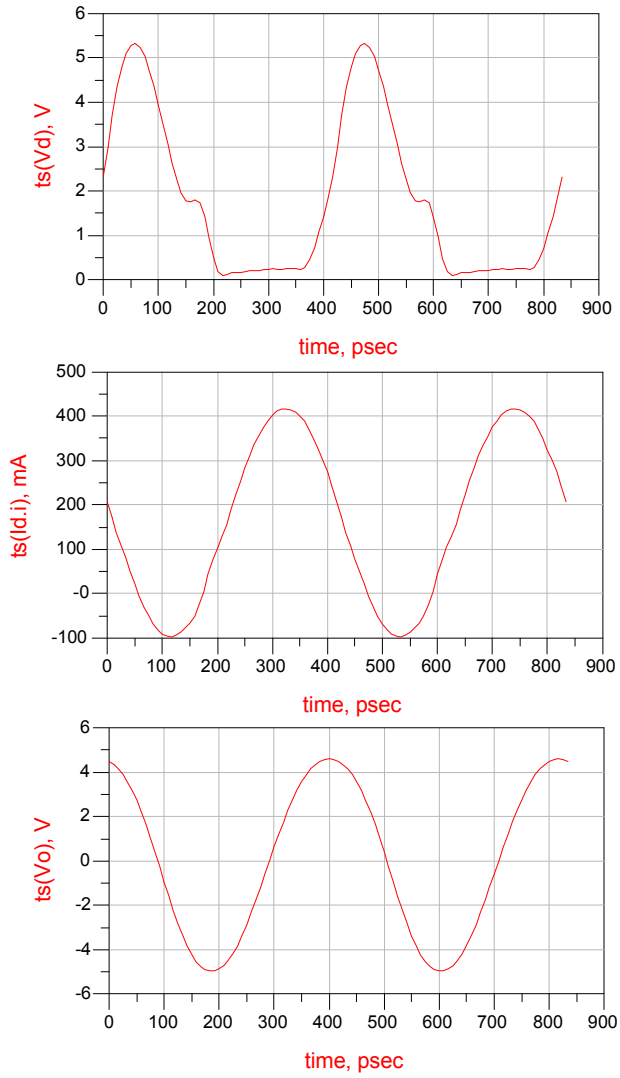

Figure 5.25 Drain voltage, drain current and output waveforms

When the input power is 0dBm, 23.7dBm output power is delivered to the load with the 73.6% power added efficiency. Clearly, this circuit provides 23.7 dB power gains in this case.

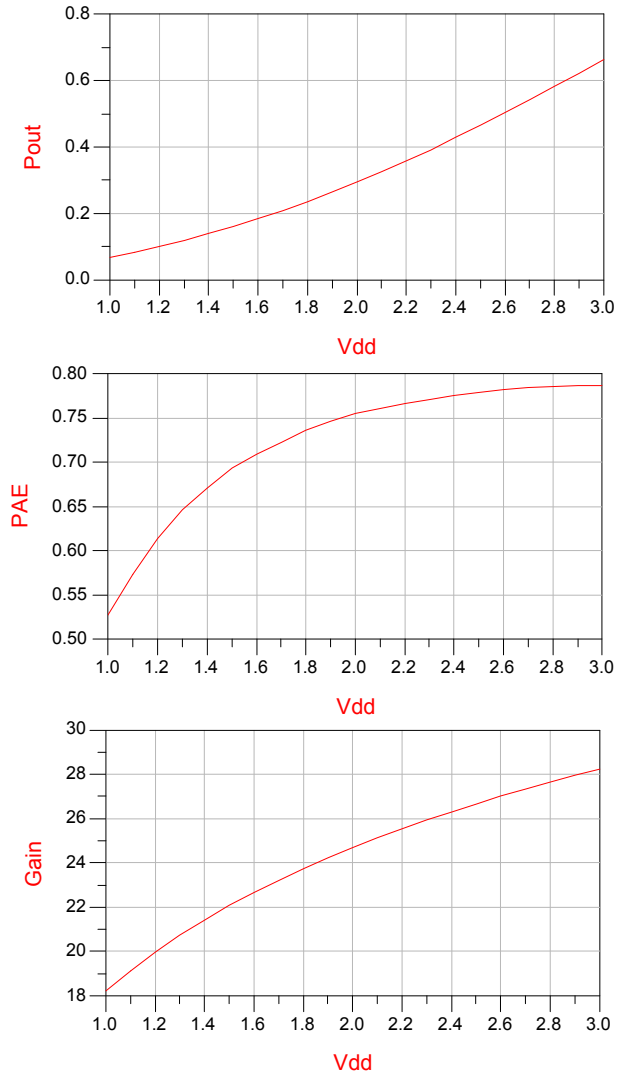

Figure 5.26 Power performance vs. the supply voltage Vdd

Figure 5.26 demonstrates that the output power and the power gain change roughly linearly with the supply voltage, whereas the PAE nearly remains constant when high supply voltage is used. In practice, additional modulation can be applied to

the supply lead of the Class-E power amplifier to obtain amplified AM-modulated signals.

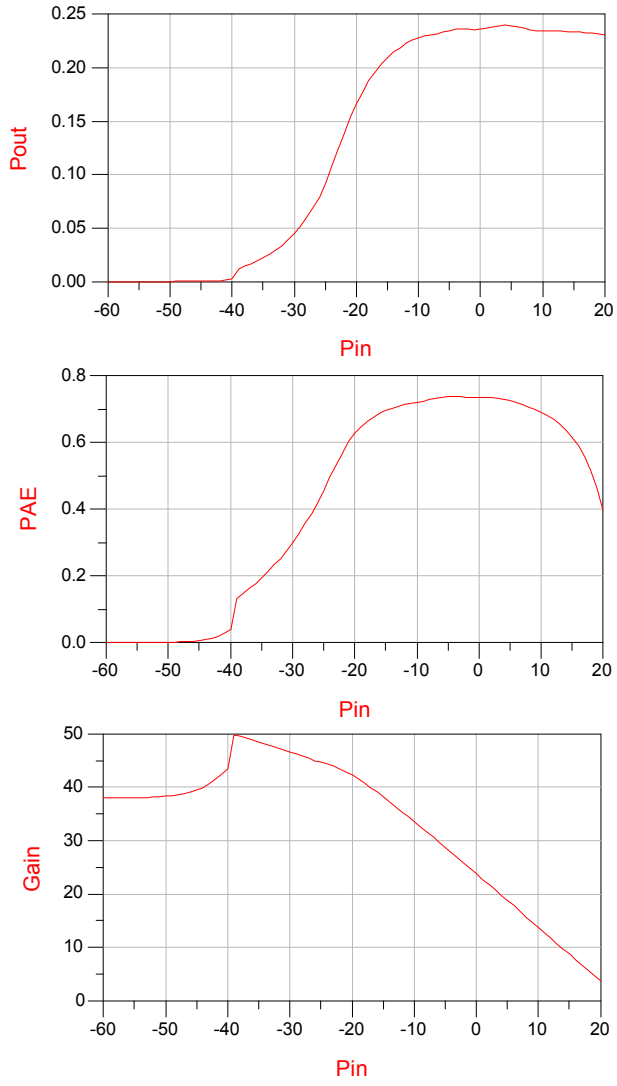

Figure 5.27 Pout, PAE and power gain vs. input power

As shown in Figure 5.27, when the input power is in the range from -10dBm to 6dBm, the power amplifier works stably and delivers nearly constant power to the load,

which is 23.7dBm. Thus, this amplifier thus can function very well for typical RF input signals of power level ranging from -10dBm to 6dBm.

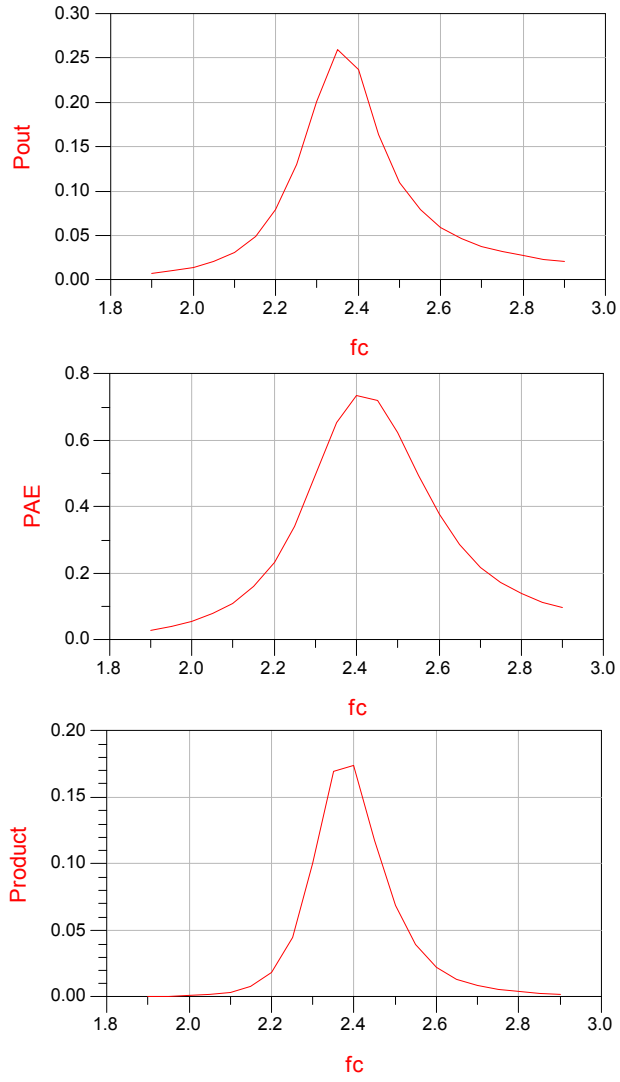

Figure 5.28 Pout, PAE and capability vs. working frequency

Figure 5.28 illustrates the frequency selectivity of this RF PA. Since only narrowband networks are used here, power performance degrades dramatically when

operating frequency is shifted from the desired central frequency. This limits the usage of the Class-E in multi-channel applications.

5.6.2 Expand Bandwidth

If impedance matching networks are replaced with Butterworth impedance transformer, one can expand the working band without losing too much energy. A practical Butterworth impedance transformer may look similar to the one in Figure 5.29.

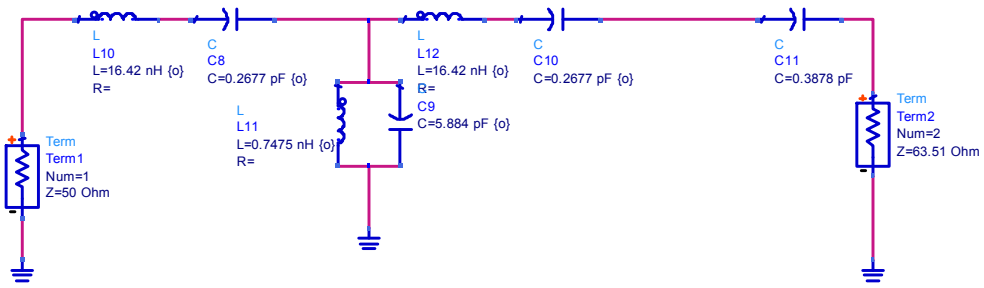

Figure 5.29 A Butterworth impedance transformer

The circuit component values can be determined by using the Optimizer in ADS. S-parameter simulation results show that the Butterworth network has wider operating bandwidth than the simple ones used before.

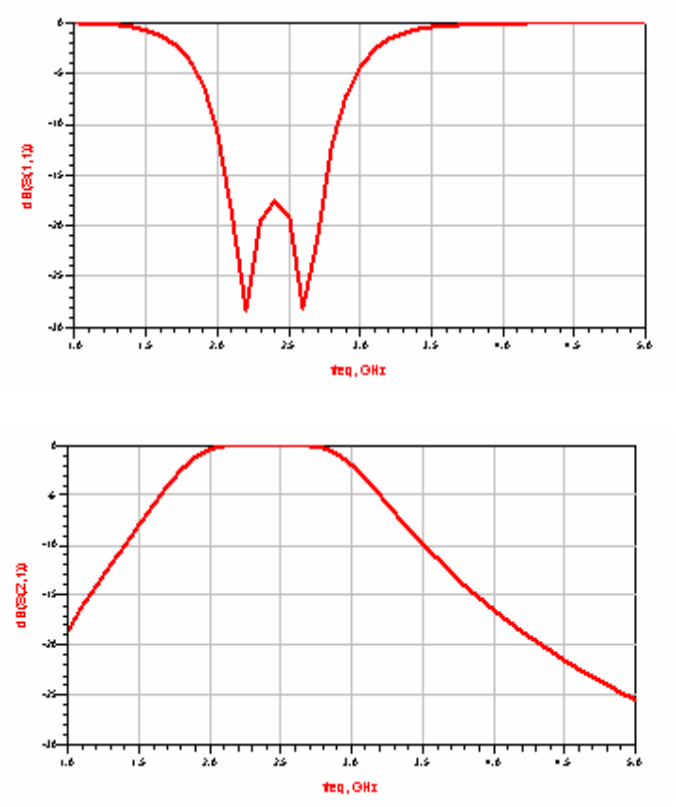

Figure 5.30 Return and insertion losses of a Butterworth network

A modified two-stage Class-E for wideband applications is shown in Figure 5.31. The output matching network is built with Butterworth transformers. The comparisons of this circuit and the previous one are illustrated in Figure 5.32-5.37.

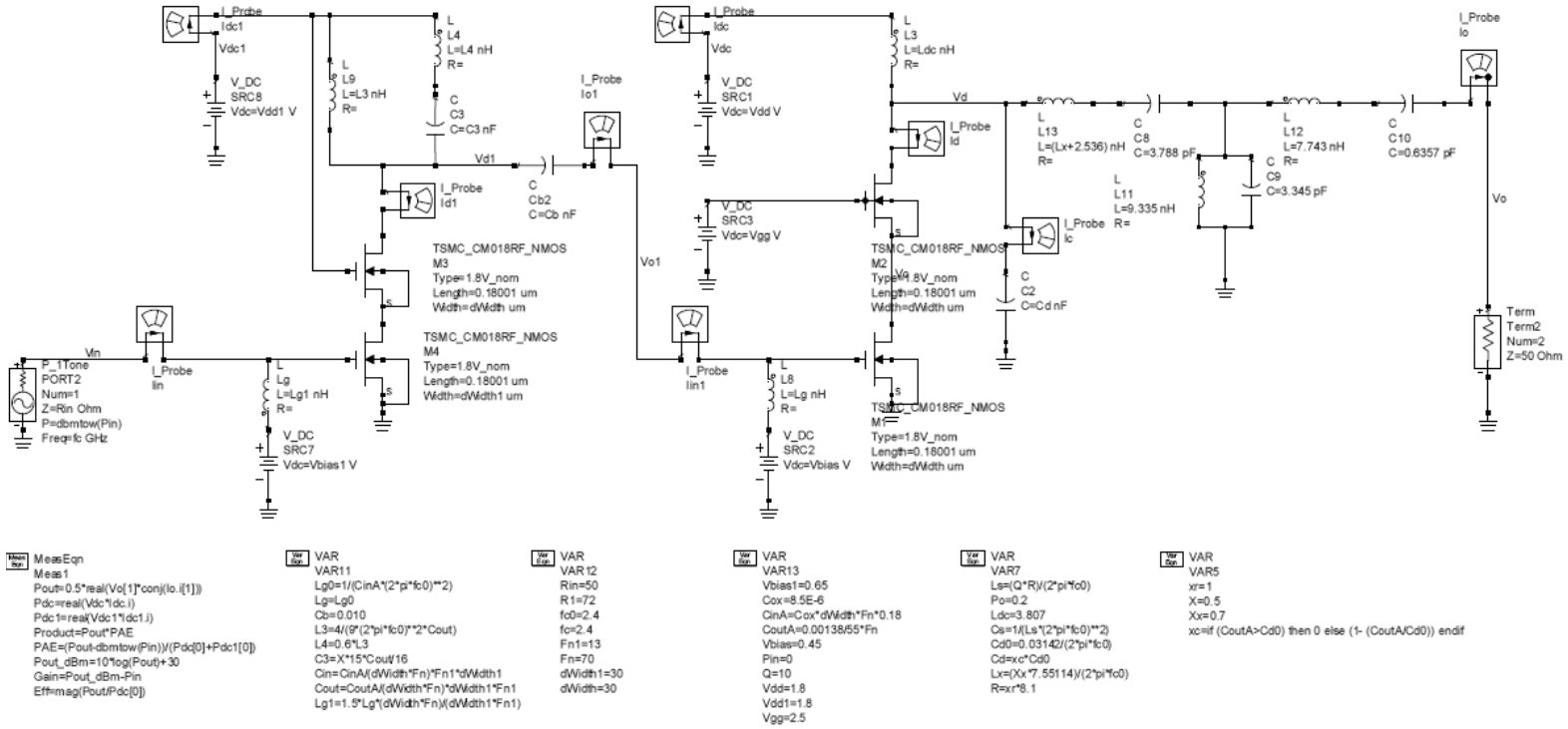

Figure 5.31 Schematic of two-staged wideband power amplifier

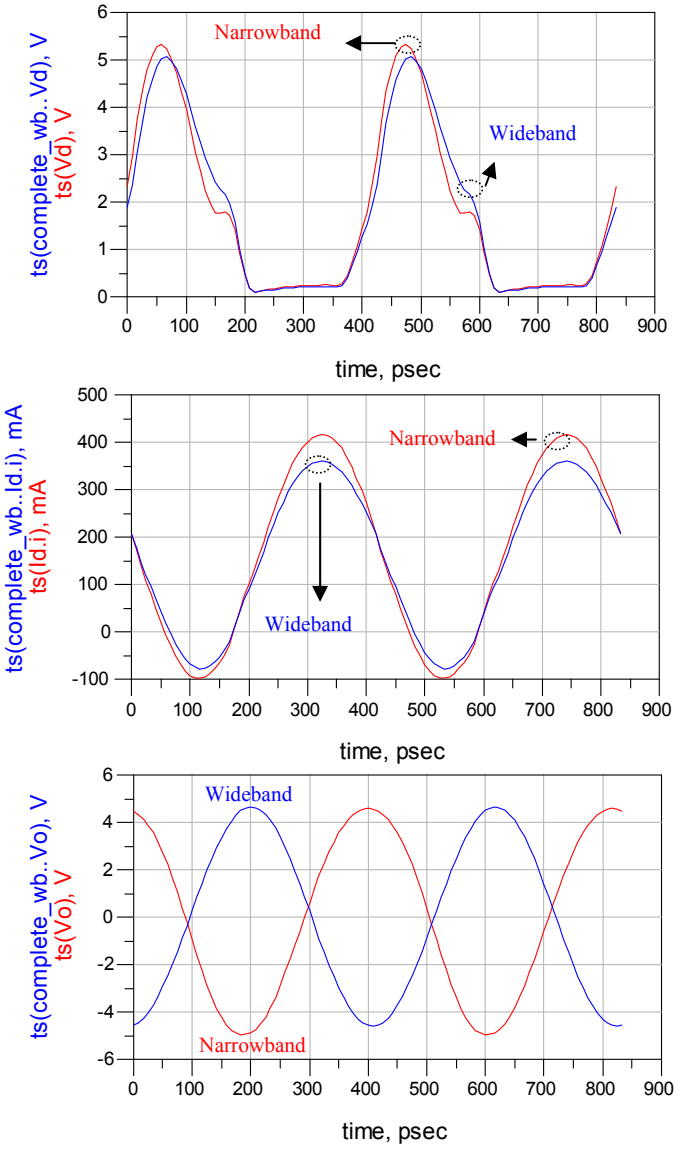

Figure 5.32 Comparison of the output waveforms

Figure 5.32 shows that drain voltage and current waveforms are almost identical except small differences in the magnitudes. The outputs have almost opposite phases.

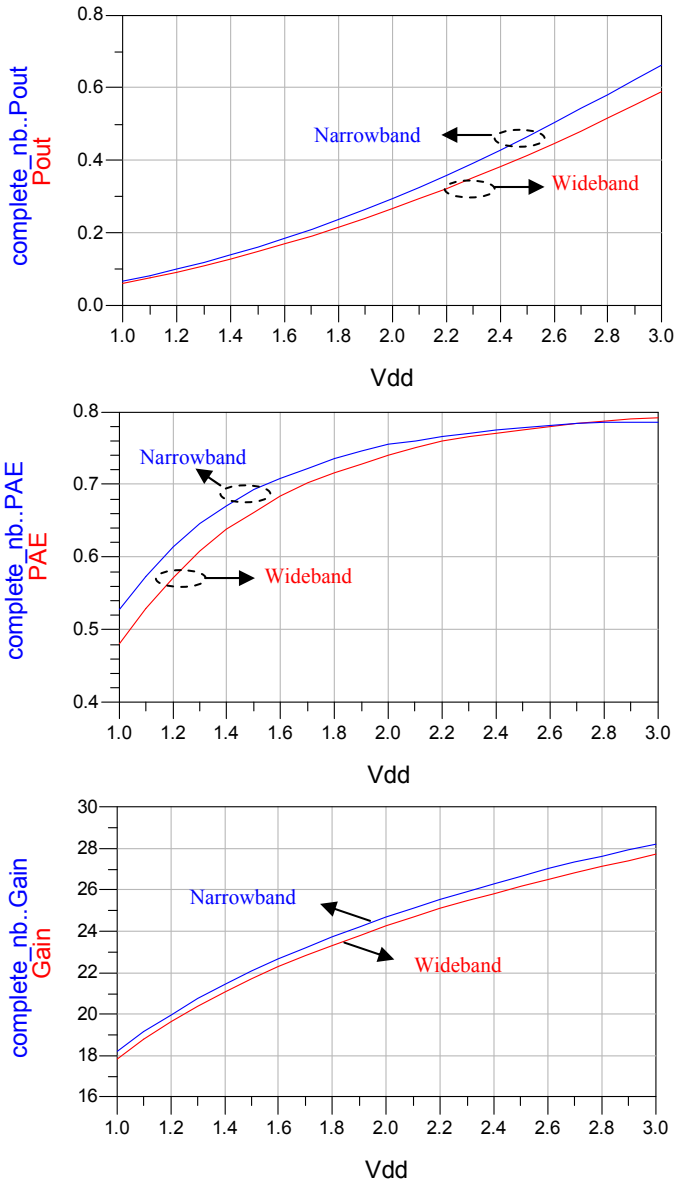

Figure 5.33 Power performance vs. Vdd

This figure shows that the circuits in narrowband and wideband cases have similar behaviors when the supply voltage varies.

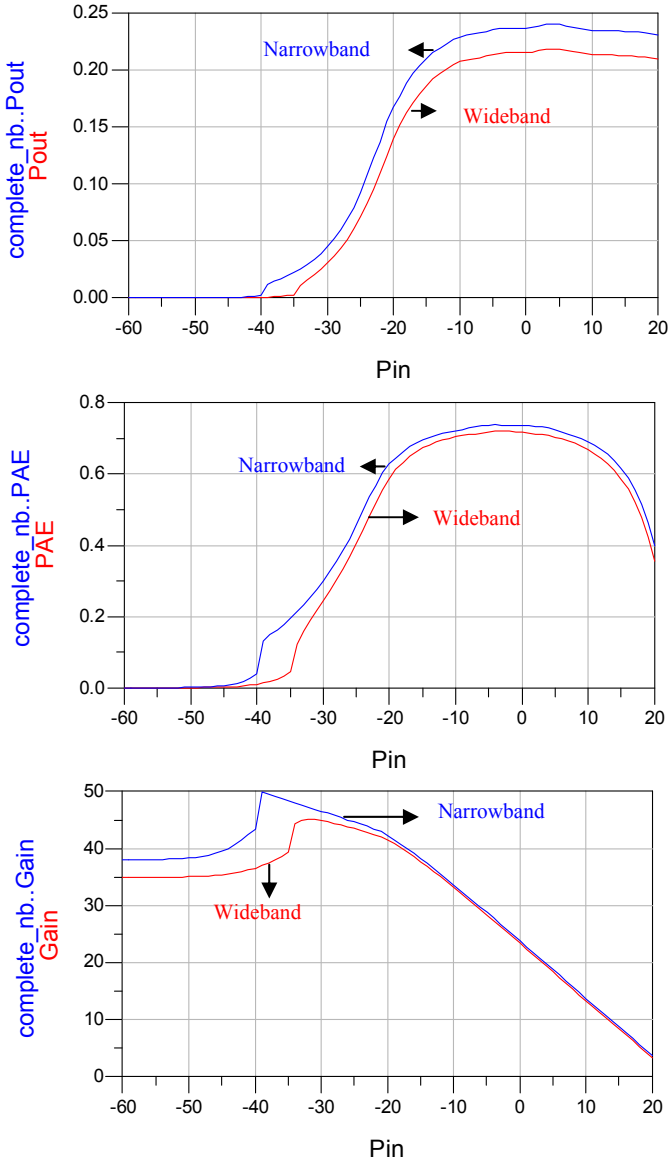

Figure 5.34 Power performance vs. input power

Figure 5.34 demonstrates that the circuit of the wideband case has small degradations in power performance with varying input power.

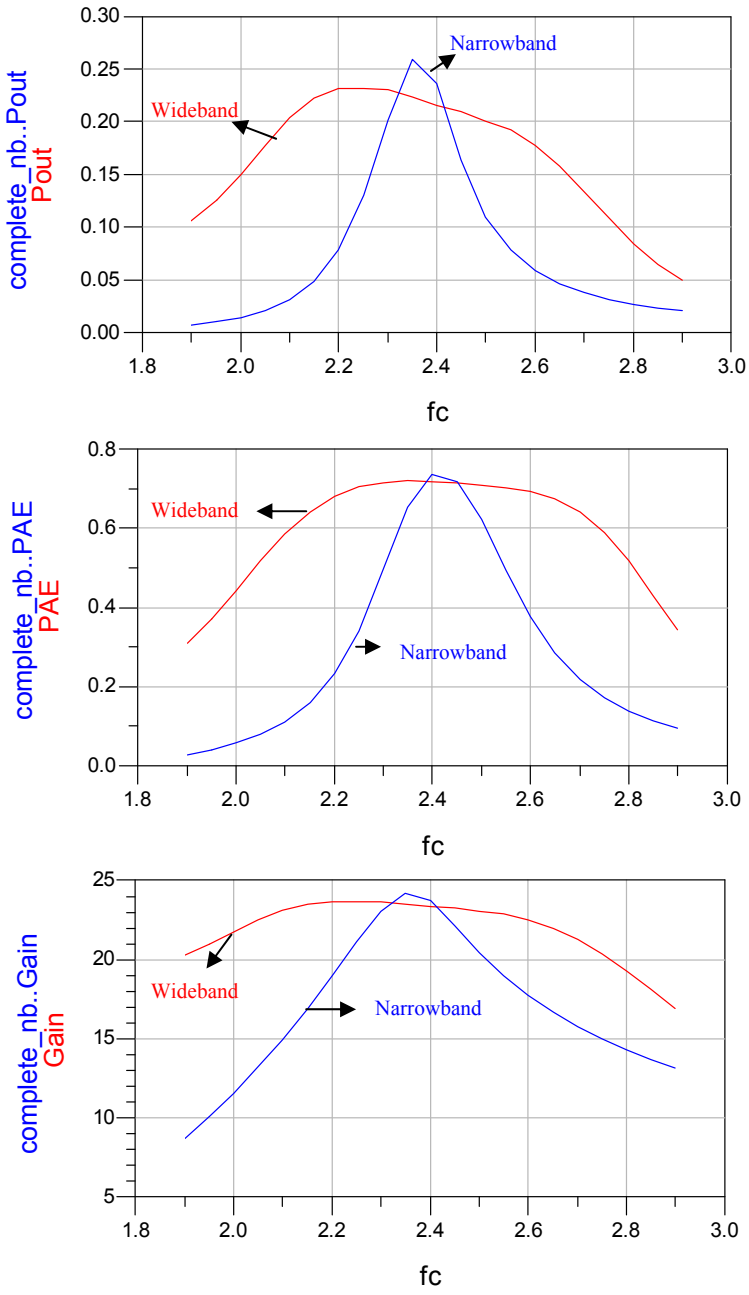

Figure 5.35 Power performance vs. frequency

From the comparison in Figure 5.35, we can see that the operating bandwidth has been expanded because of the employment of matching networks supporting wider

bandwidth. It is noteworthy that the possible maximum output power is reduced more significantly compared to the other two figures of merit. Other than that, the wideband implementation has similar dynamic characteristics. The power ability is also increased in the wideband case, which is shown in Figure 5.36. But this monolithic wideband circuit will consume much larger chip size since more passive devices are used.

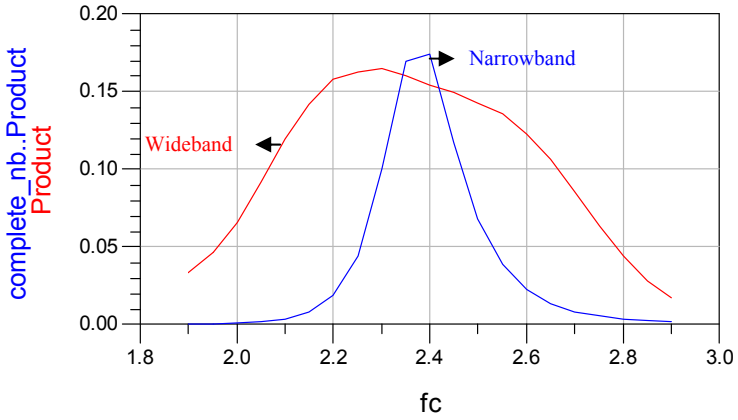

Figure 5.36 Power abilities for the narrow- and wide-band cases

5.6.3 Impacts of Variant Active Devices

Variants in the devices can cause the circuit performance to shift from the prediction. For semiconductor devices, variants are caused by errors in geometry and doping values. The typical results are the changes in the thickness of the oxide layer and the value of the carrier mobility.

The effects of employing typical, fast and slow NMOS transistors are illustrated in Figure 5.37. It shows that the case in the fast corner has the highest output power and

narrowest working bandwidth. But the performance doesn't change too much from case to case.

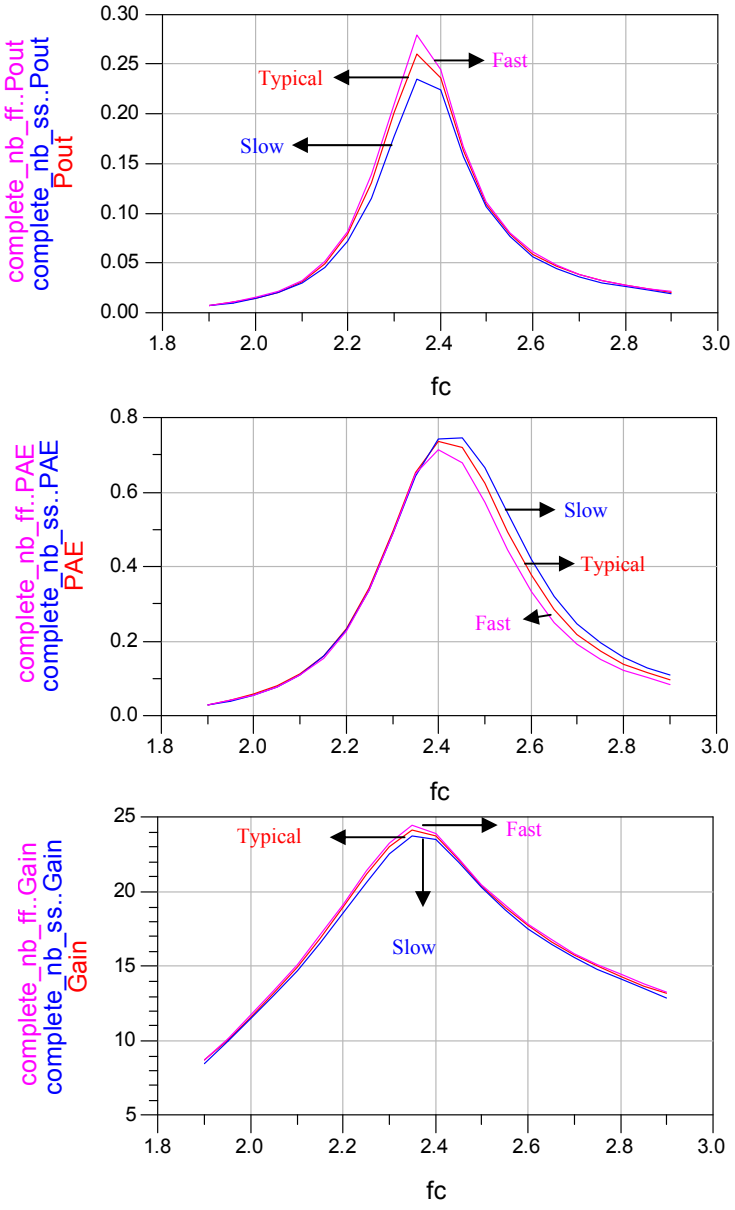

Figure 5.37 Power performance vs. frequency in cases with variants in the transistors

5.6.4 Linearity of Class-E Power Amplifier

Class-E amplifiers belong to the switching-mode amplifiers. Therefore, Class-E amplifiers have strong nonlinearity. The typical 1-dB compression point and two-tone tests are not applicable for the Class-E amplifiers. The nonlinearity is illustrated in Figure 5.38. In the applicable input power ranges, -16dBm to 20dBm in this case; the gain is almost inversely proportional to the input power.

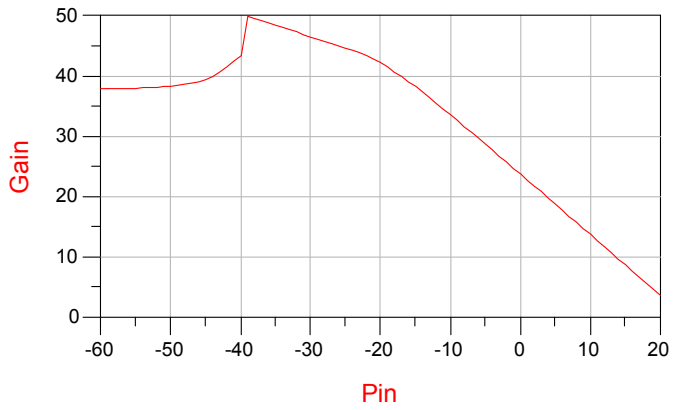

Figure 5.38 Nonlinearity of this Class-E power amplifier

5.6.5 Comparison of Different Design Methods

As discussed before, the design method used here is optimized for the applications with a finite DC feed inductance. Figure 5.39 illustrates the power performance of the narrowband implementations designed by three methods. It shows that the ideal method provided by Raab will generate significant discrepancies from the desired values when finite inductance is used. The proposed method has the same behavior with the one provided by Milosevic et al but provides simpler design equations.

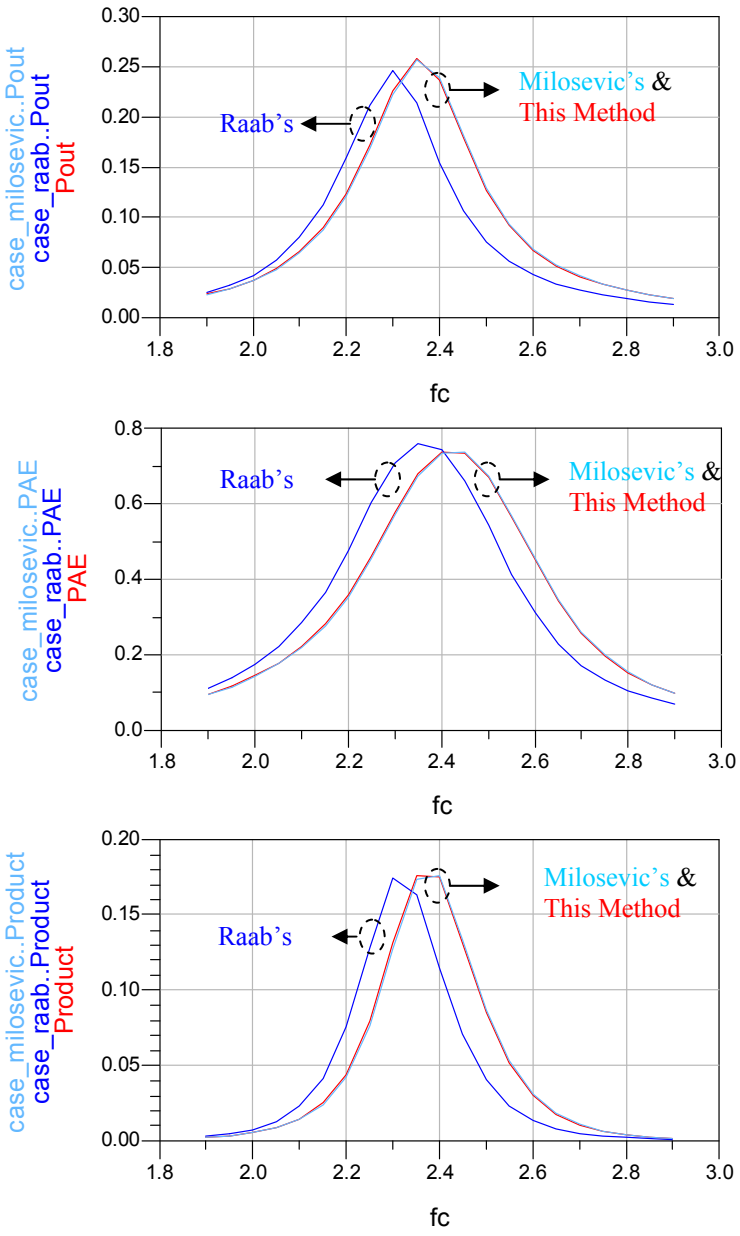

Figure 5.39 Comparison of three design methods

CHAPTER 6

CONCLUSION

6.1 Summary

Class-E, one of switching-mode amplifiers, consists of a load network and a voltage-controlled transistor as a switch. It can achieve high efficiencies if the load network successfully prevents simultaneous high voltage and high current in the transistor. Class-E has a simpler topology and a good tolerance to the variations in the circuit components, which makes it a good candidate for RF power amplifier designs.

The aim of this work is to develop an optimized yet explicit Class-E power amplifier design method with bulk CMOS technology. Due to the inherent parasitic losses of the sub-micron bulk CMOS, low quality inductor and non-ideal transistor are considered the main causes for inaccuracy of the theoretical predictions, which may result in large power losses. The conventional design method cannot provide accurate initial circuit parameters for the designs in CMOS. Here I develop a set of explicit numerical design equations for the load network. Besides the load network, the constraints of the transistor have also been discussed during the designing process. The parasitic resistance and capacitances are calculated to estimate other design parameters.

This design technique is validated through a practical design of a Class-E power amplifier in 0.18μm CMOS for 2.4GHz WLAN applications. The practical design issues including the inductor modeling, the protocol load network verification,

the transistor geometry tradeoff, the drive stage design, and the matching network realization have been explained in detail. The simulation results indicate that the two-staged amplifier of maximum 43dB power gain can deliver at least 23dBm output power with 73.6% PAE at 2.4GHz if the input power is 0dBm. This result demonstrates that the proposed design technique can produce optimized Class-E circuit parameters for the applications in bulk CMOS. It also suggests that deep-submicron bulk CMOS technology is suitable for implementing low-power monolithic Class-E power amplifiers.

Table 6.1 Performance summary of the proposed power amplifier

Parameters	Specification	Implementation
Applicable Input power (Typical)	From -10dBm to 6 dBm (0dBm)	From -16dBm to 20dBm (0dBm)
Output power	23dBm	>23dBm
Maximum gain	33dB	>39dB
Power Added Efficiency	50%	73.6% (Drive stage: 62.5%, Output stage: 82.5%)
Center frequency	2.4GHz	2.4GHz
Supply voltage	3.3V	1.8V/2.5V

6.2 Future Work

An accurate estimation is a good start for the future work. Although Class-E has excellent power efficiency, it exhibits strong nonlinearity. In practice, additional compensation circuits are needed to provide acceptable linearity which is required by most wireless standards. The future work includes:

1) Layout
2) Linearity compensation techniques
3) Circuit implementation with distributed transmission line
4) Active inductors/varactors
5) Power control circuitry
6) Wideband applications

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BIOGRAPHICAL INFORMATION

Tao Wang received his bachelor degree in Information Engineering from Beijing University of Posts and Telecommunications, China, in 1999. After five years as an embedded hardware engineer in 3G Mobile Communication R&D Center, China Academy of Telecommunication Technology, he began his graduate study in the School of Electrical Engineering at the University of Texas at Arlington in the spring of 2005, and then joined the Integrated Circuit Design and Reliability Lab (ICDAR) in the fall of 2006. His current research interests include high-speed circuit reliability and signal integrity analysis, mixed-signal and radio frequency integrated circuit design for wireless communications.