CMOS VCO & LNA IMPLEMENTED BY AIR-SUSPENDED ON-CHIP RF MEMS INDUCTORS

by

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ABSTRACT

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In this thesis, a CMOS 2.4 GHz Low noise amplifier (LNA) and Voltage-controlled oscillator (VCO) was designed and simulated. These circuits were designed to operate in the 2.4GHz Industrial Scientific Medicine (ISM) band and to achieve Bluetooth and Wifi standard specifications. High-Q RF MEMS air-suspended circular spiral inductors are used in both circuits. High-Q inductors give the circuit better performance parameters including higher gain, lower noise figure and narrower bandwidth. The integration of these RF MEMS inductors onto RF circuit chips was carried out using the UV-LIGA technique and an additive pattern transfer technique such as electroplating. The LNA maintains a gain of 10dB and noise figure of 0.8dB at 2.4 GHz. With an input reflection coefficient of -10.8dB and output reflection

coefficient of -12.93dB, the LNA matches successfully with 50Ω load at 2.4 GHz. The VCO maintains an average output swing of 1.95V in a frequency range of 2.94GHz to 2.2GHz achieving a 740GHz of tuning range.

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CHAPTER 1

INTRODUCTION

With increase in demand for wireless communication applications, the wireless circuit design technologies and techniques have made remarkable progress in recent years. Technology scaling has brought both advantages and disadvantages in design of RF transceivers for portable wireless devices. Introduction of wireless communication standards has been a driving force in continual research and development. The two most widespread short-range communication standards are Bluetooth and IEEE802.11b.

Bluetooth has been introduced to connect any home or office appliances such as personal computers, printers with data rate at 1 Mbps. It is aimed to operate in even the smallest battery-powered devices, the Bluetooth specification calls for a small form factor, low power consumption and low cost. The range and speed of the technology is kept low to ensure maximum battery life and minimum incremental cost for devices incorporating the technology. Bluetooth creates a Wireless Personal Area Network (WPAN) consisting of all the Bluetooth-enabled electronic devices immediately surrounding a user, wherever that user may be located.

IEEE 802.11b (popularly known as Wifi) proliferated due to explosive growth of internet users, providing high data rate wireless communications up to 11 Mbps. IEEE 802.11 a/b uses the unlicensed spectrum for transmission and thus it must use spread spectrum techniques. This process increases the communication channel's interference immunity or the processing gain, decreases interference between multiple

users and increases the ability to re-use the spectrum. 802.11b uses the 2.400 GHz to 2.483 GHz spectrum. 802.11 is the wireless extension of 802.3 and supports all the underlying protocols that Ethernet uses.

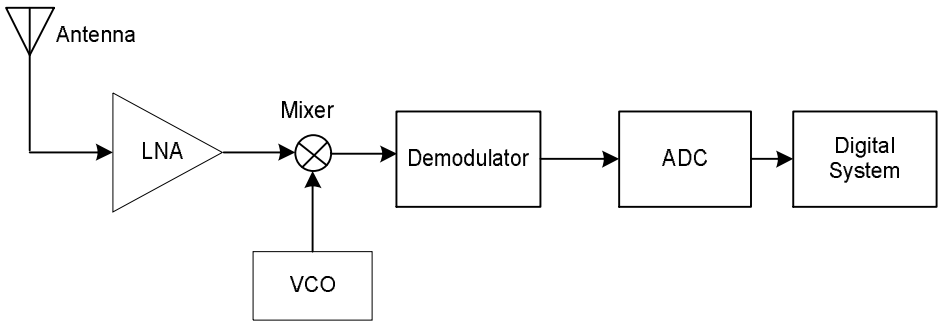


Figure1.1 Block diagram of generic analog RF receiver.

Both Bluetooth and IEEE 802.11 operate at RF frequency 2.4 GHz. A simple RF receiver architecture is shown in Figure1.1. The signal received at the antenna, is amplified by a Low-noise amplifier (LNA), the spectrum is translated to a lower frequency by a Mixer to facilitate subsequent demodulation. The lower frequency is decided by the Voltage-controlled oscillator (VCO). The demodulated signal is then converted to a digital signal by an Analog to Digital converter (ADC) which is then processed by the digital system.

The VCOs and LNAs are critical components in RF systems. The cost effective CMOS VCOs and LNAs are very attractive to be used for recent wireless communication systems in CMOS technology.

For VCOs, an inductor – capacitor resonator (LC tank) determines the center frequency of oscillation. Designing this LC tank is the most critical factor for the whole performance of VCOs. Performance of these energy storage components directly relate

to the quality of outputs such as phase noise and noise factor. Then, the high phase noise cause poor signal detection at receiver part. In order to minimize the phase noise, using high-Q inductors and capacitors is very encouraged for VCO studying.

For LNAs, at high frequency, CMOS technology has a problem of signal loss through conducting silicon substrate. The signal loss through drain or source to substrate parasitics degrades the noise factor and gain. Also impedance matching is an important issue for maximum power transfer. Use of inductors in LNA topologies is common and effective for input impedance matching. The noise contributed by the parasitics of the inductors degrades the noise factor and gain. In order to minimize noise factor and maximize gain high-Q inductors are required.

The inductors obtained from standard silicon processes cannot provide high-Q factors sufficient for high-performance VCOs and LNAs. The reasons for low-Q factors come from thin metal layers (ohmic loss) and high substrate coupling (eddy-current loss) in standard silicon processes. High resistive loss of these layers plays an important role in determining the Qs in lower frequency regions below a peak-Q frequency.

Integration of MEMS and radio-frequency (RF) microelectronics, called RF-MEMS, has been rapidly gaining a great interest as an enabling technology to realize high-performance on-chip RF-MEMS passives by replacing off-chip passives in communication systems. In order to reduce such resistive loss, low-resistivity material is used and the metal layers are much thicker than the skin depth in RF-MEMS inductors. And because the substrate loss is caused by the electromagnetic coupling of passive devices residing right on top of the conductive silicon substrate, air-suspended

inductors from the substrate realized by RF MEMS technique can significantly reduce such substrate coupling loss and obtain a high-Q inductor.

In chapter 2, there is a brief description of Bluetooth and Wifi standards. This is followed by analysis of common LNA and VCO topologies. In chapter 3, detailed design procedure of LNA and VCO is discussed, with respective simulation results, layout and chip photos. Tables comparing the results of LNAs and VCOs designed with air-suspended RF MEMS inductors and monolithic planar inductors are shown. Chapter 4 concludes the thesis work.

CHAPTER 2

BACKGROUND

In recent years mobile digital devices such as personal digital assistants, mobile phones, digital cameras, and laptops have entered the consumer market with high demand. These devices require powerful short-range communication methods for data exchange between each other and connections with printers or local area network (LAN) access. The communication methods can be based on cable connections, radio links, or infrared links. Each has its individual strengths and weaknesses. Each technology found its way into various products.

2.1 Wireless Narrowband systems

Infrared transmission based on the Infrared Data Association (IrDA) standard enables fast connection establishment due to its point-and-shoot characteristic. With the high baud rates of up to 16Mb/s, it is well suited to applications that require high performance as hoc point-to-point connections. Examples include downloading of pictures from digital camera to laptop or paying for meal in a company's cafeteria with your mobile phone via IrDA port. IrDA standards have been widely implemented in laptops, computers and PDAs. Recently, due to high cost, the technology was difficult to implement.

Radio-based short-range wireless (SRW) communication is an alternative class of technologies designed primarily for indoor use over very short distances. It provides fast (10-100Mb/s) and low cost, cable-free connections to the internet. SRW communication has transmission powers of several microwatts up to milliwatts yielding a communication range between 10 and 100 meter. SRW provides connectivity to portable devices such as laptops, PDAs, cell phones and others. Short-range communications standards fall into two broad but overlapping categories: personal area networks (PAN) and local area networks (LAN).

Wireless PAN Technologies emphasize low cost and low power consumption, at the expense of range and peak speed. In a typical wireless PAN application, a short wireless link less than 10 meters, replaces a computer serial cable or USB cable. Standards, such as Bluetooth and Home-RF, have been created to regulate short-range wireless communications. Bluetooth has been implemented in most of the mobile devices used today. Bluetooth transmits data through solid nonmetal objects and supports a nominal link range of 10cm-10m at a moderate baud rate up to 720kb/s (raw data rate is 1Mb/s) [1]. An optional high power mode in the current specifications allows for ranges up to 100m. Bluetooth is a point to multipoint communication system. It supports connections of two devices as well as ad hoc networking between several devices. To prevent unauthorized access, Bluetooth requires authentication and encryption mechanisms, which hampers speed of establishing a connection. It is good for applications where mobility is a key requirement.

Wireless LAN technologies emphasize a higher peak speed and longer range at the expense of cost and power consumption. Typically, wireless LANs provides links from portable laptops to a wired LAN access point. To date, 802.11b has gained acceptance rapidly as a wireless LAN standard. Its nominal open-space range is 100m and peak over-the-air speed is 11Mb/s. Users get maximum available speeds of about 5.5Mb/s. Other communication standards offer even higher data rates, like 802.11a and 802.11g.

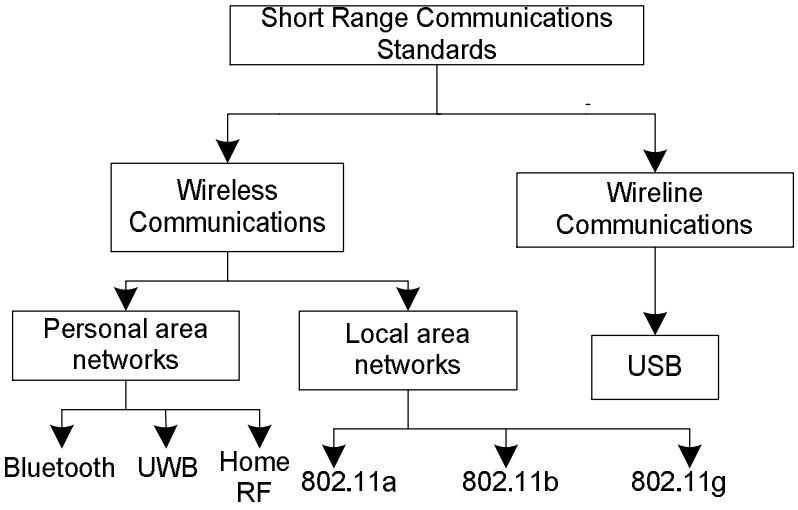


Figure 2.1 Short-range communication standards

2.1.1 Bluetooth

Bluetooth technology was developed to serve as a short-range wireless voice and data link between electronic devices such as PCs, notebook computers, handhelds and PDAs, mobile phones and digital cameras. It is aimed to operate in even the smallest battery-powered devices, the Bluetooth specification calls for a small form factor, low power consumption and low cost. The range and speed of the technology is

kept low to ensure maximum battery life and minimum incremental cost for devices incorporating the technology. Bluetooth is creates a Wireless Personal Area Network (WPAN) consisting of all the Bluetooth-enabled electronic devices immediately surrounding a user, wherever that user may be located. This project is supported by a special interest group formed by several companies that lead technological development.

Specifications of Bluetooth give its limitations and possibilities. Bluetooth operates in the 2.4GHz frequency range which is free for use to everyone globally. This frequency provides an effective data rate of 720 Kbit/s. There are multiple categories of transmission strengths which decide the use and the energy efficiency of these devices. Bluetooth achieves its functionality through its modulation and packet scheme. This is also known as Gaussian Frequency Shift Keying (GFSK).

Bluetooth hops to one of 79 different channels (US and Europe) with a repetitive process that keeps errors to a minimum. This packet hopping technique leads to interference with 802.11b technology. The channel hopping feature of Bluetooth is the main cause of its low power consumption, error correction and the distinct topology that it can support. Bluetooth divides the data to be sent into packets. Each packet is sent within a 625us slot. A frame is includes a transmit slot and a receive slot, providing full duplex communication between a master and a slave in one time frame. To avoid noise and other interferences, Bluetooth hops to one of 79 different channels each time frame. The channel that it hops to is determined by a Master ID and the previous channel number. This algorithm repeats. If there is severe noise between 2.408GHz and

2.410GHz, it is avoided the most of the time. There is little to no time contention between masters within reach of each other which might result in the masters picking up the same channels simultaneously. Due to the channel hopping mechanism, interference is kept to a minimum despite the highly dense network.

Bluetooth was originally conceived by Ericsson in 1994, during a study to examine alternatives to cables that linked mobile phone accessories. Ericsson has a strong history in short range wireless, being a key pioneer of the European DECT cordless telecommunications standard, which is largely based on their earlier proprietary DCT900 technology. In February 1998, the Bluetooth SIG (Special Interest Group) was founded by a small core of major companies - IBM, Intel, Nokia, Toshiba and Ericsson - to work together to develop the technology and to subsequently promote its widespread commercial acceptance [1].

2.1.1.1 Bluetooth Modulation format

The modulation format is Gaussian Frequency Shift Keying (GFSK) with a bandwidth*bit-time product (BT) of 0.5. The modulation index is between 0.28 and 0.35. For the 1Mbps data rate in Bluetooth, frequency deviation is from 140 to 175kHz. The data signal is passed through a Gaussian filter. The Gaussian filtered signal is modulates with the carrier signal with frequency shift keying. The BT specification of 0.5 in the Bluetooth standard is chosen by keeping the trade-off between minimizing the inter-symbol interference while maximizing the bandwidth.

2.1.1.2 Frequency Band

Bluetooth operates in the 2.4GHz Industrial Scientific Medicine (ISM) band. The range of this frequency band is 2400MHz – 2483.5MHz. With Time Division Duplex (TDD), transmitter and receiver share the same frequency band. To regulate the use of the same spectrum simultaneously by several devices, the device needs to spread the power of its transmissions across the ISM band. Two methods used for spreading out the power are: direct sequence spread spectrum (DSSS) and frequency-hopping spread spectrum (FHSS). DSSS smears a transmission across a wide range of frequencies at low power. FHSS spectrum uses a small bandwidth but changes (or hops) frequency after each packet.

Bluetooth uses frequency-hopping spread spectrum. The spectrum is split into 79 channels of 1MHz each. Transmitters change frequencies 1,600 times every second. To prevent two linked pairs to collide on the same channel, one pair hops off to a new frequency and re-transmits any lost data. This technique also minimizes the risk that portable phones or baby monitors will disrupt Bluetooth services, since the effect of any interferer on a particular frequency will last only a tiny fraction of a second. Bluetooth uses the master's device ID to algorithmically determine the frequency hopping pattern. This algorithm generates a unique pattern that is quite random and exhibits an extremely long repeat cycle.

Table 2.1 Overall system specifications for Bluetooth and WLAN

Characteristics	Bluetooth		IEEE802.11b	
Frequency Bands	2.4 ~ 2.4835GHz		2.4 ~ 2.4835GHz	
Bandwidth	1MHz		22MHz	
Channel Spacing	1MHz		5MHz	
NO. of Channels	79*		13**	
Modulation Scheme	GFSK		DBPSK (1Mbps) DQPSK (2 & 5.5Mbps) QPSK (11 Mbps)	
Multiple Access	FHSS		DSSS CCK	
Duplexing	TDD		TDD	
Minimum Sensitivity	-70dBm		$\geq$ -76dBm	
Maximum Sensitivity	-20dBm		-10dBm	
QoS	BER 10^{-4}		FER = 8 * 10^{-2} ($\approx$ BER 10^{-3})	
Input Noise	-114dBm		-100.6dBm	
Input SNR	44dB		24.6dB	
Required SNR	23dB		-2dB (1Mbps, PG *** of 10.4dB) 1.6dB (2Mbps,PG*** of 7.4dB) 11dB (5.5Mbps) 14dB (11Mbps)	
Overall System NF *(NF_{system})*	21dB		26.6dB (1Mbps) 23dB (2Mbps) 13.6dB (5.5Mbps) 10.6dB (11Mbps)	
Overall System IIP3 system	-17.5dBm		-30.5dBm (1Mbps) -29dBm (2Mbps) -24dBm (5.5Mbps) -22.5dBm (11Mbps)	
Phase noise of local oscillator	Offset	Phase Noise	Offset	Phase Noise
	1MHz	-80dBc/Hz		
	2MHz	-110dBc/Hz	22MHz	-93dBc/Hz
	3MHz	-120dBc/Hz	44MHz	-123dBc/Hz

* fc = 2402 + k MHz, k = 0,1,2…..78

** fc = 2412 + k * 5MHz, k = 0,1,2,…..12

*** Processing Gain

2.1.2 IEEE 802.11b

The IEEE 802.11b is popularly known as Wifi (for Wireless Fidelity). It emerged in 1999 and is the most popular wireless networking standard. Operating in the 2.4GHz radio band, 802.11b is the current mainstay of the 802.11 family of wireless networking standards established by the IEEE (Institute of Electrical and Electronics Engineers). 802.11 define the PHY (physical) and MAC (media access control) layers of the protocol. The other layers are identical to the 802.3 (Ethernet) protocol.

802.11a/b uses the unlicensed spectrum for transmission and thus it must use spread spectrum techniques. This process increases the communication channel's interference immunity or the processing gain, decreases interference between multiple users and increases the ability to re-use the spectrum. 802.11b uses the 2.400 GHz to 2.483 GHz spectrum. 802.11 is the wireless extension of 802.3 and supports all the underlying protocols that Ethernet uses. An Access Point (AP) is the center of the Basic Service Set (BSS) which may overlap partially, completely or doesn't overlap with each other without the problem of interfering with functionality. Mobile users can roam from AP to AP and these APs are connected together using the same ID which forms an Extended Service Set (ESS). Each AP has its own MAC and IP addresses and they are fault tolerant when setup with multiple failure points. Addition of capacity to the network is done by adding APs to a new Ethernet port which uses the same ID. 802.11b follows the DSSS (Direct Sequence Spread Spectrum) method to disperse the data frame signal over a relatively wide (30 MHz) portion of the 2.4 GHz band. This results in greater immunity to radio frequency interference as compared to narrowband

signaling. Due to the relatively wide DSSS signal, 802.11b AP must be set to specific channels to avoid channel overlap which may cause a reduction in performance. To spread the signal, the transmitter combines the Physical Layer Convergence Procedure (PLCP) protocol data unit with a spreading sequence through the use of a binary adder. PLCP is a frame modification technique used by 802.11b. For higher data rates (5Mbps, 11Mbps) 802.11b uses Complementary code keying (CCK) to provide spreading sequences. Detailed 802.11b standard specifications can be found in [2]. A summary of Wifi RF specifications is listed in Table 2.1.

Wifi networks operate in two modes: ad hoc networks and infrastructure networks. Ad hoc network is a temporary self-contained group of stations with no connection to a larger LAN or the Internet. It includes two or more wireless stations with no access point or connection to the rest of the world. Ad hoc networks are also called peer-to-peer networks and Independent Basic Service Sets (IBSS). Infrastructure networks have one or more access points, almost always connected to a wired network. Each wireless station exchanges messages and data with the access point, which relays them to other nodes on the wireless network or the wired LAN. Any network that requires a wired connection through an access point to a printer, a file server or an Internet gateway is an infrastructure network

2.1.2.1 IEEE 802.11b modulation format

802.11b is an extension of the 802.11 standard that uses two data rates, 1 and 2Mbits/s, use DBPSK and DQPSK modulation formats, respectively. In both data rates, an 11-bit Barker sequence (+1, –1, +1, +1, –1, +1, +1, +1, –1, –1, –1) is used to spread

the signal at 11MHz chipping rate. In addition to these two rates, 802.11b provides 5.5 and 11Mbit/s data rates. 8-chip complementary code keying (CCK) is employed as the modulation scheme at 11MHz chipping rate which is the same as the chipping rate in 802.11 standard, thus providing the same occupied channel bandwidth.

2.1.2.2 Frequency band

Wifi operates in the same frequency range 2.4-2.4385GHz as Bluetooth. With Time Division Duplex (TDD), transmitter and receiver share the same frequency band. To regulate the use of the same spectrum simultaneously by several devices, the device needs to spread the power of its transmissions across the ISM band. Two methods used for spreading out the power are: direct sequence spread spectrum (DSSS) and frequency-hopping spread spectrum (FHSS). DSSS smears a transmission across a wide range of frequencies at low power. Wifi uses DSSS method.

2.3 LNA topologies and analysis

There are several architectures for building a LNA. Figure 2.2 shows five popular architectures and all are capable of providing 50Ω input matching.

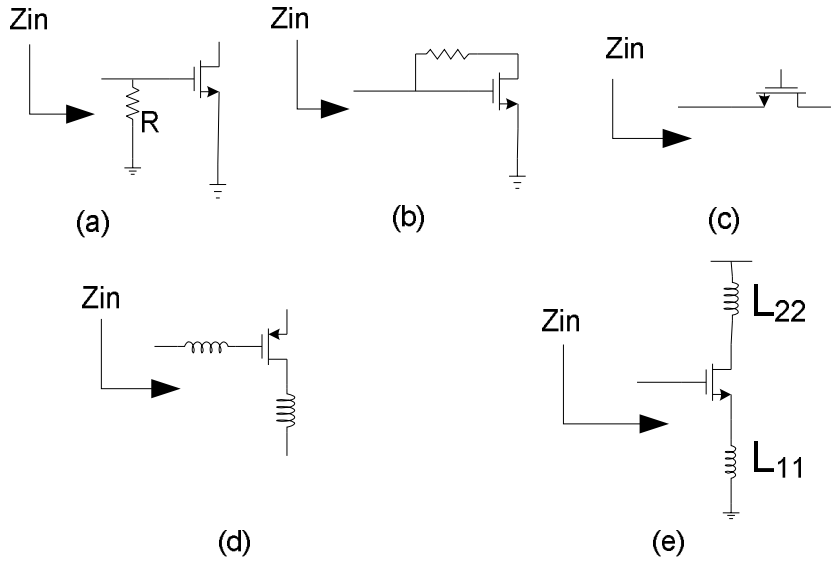


Figure 2.2 LNA architectures (a) Resistive termination (b) Shunt-series feedback (c) Common gate (d) Inductive degeneration (e) Transformer feedback

2.3.1 Resistive Termination

Input matching is achieved by adding a resistor R as shown in Figure 2.2(a); the resistor provides the source impedance. This architecture produces more noise with matched input.

$$NF = \frac{4KTR_s(1/2gZ_1) + 4KTR_{in}(1/2gZ_1)^2 + 4KT\gamma g_{d0}Z_1^2}{4KTR_s(1/2g_mZ_1)^2} = 2 + \frac{2\gamma g_{d0}}{R_s g_m^2} \qquad (2.40)$$

The lower limitation of the above equation is 3 dB. Practical situations make the lower limit of NF much greater. A termination-less amplifier with a 6-dB noise figure would likely possess an 11.5-dB noise figure with the addition of the termination resistor [3]. This is because the resistor produces its own noise and attenuates the input signal. The Friis equation proves that if an amplification stage attenuates the signal instead of amplifying it, the NF after that stage is amplified. The combined noise contribution makes this topology unattractive [4].

2.3.2 Shunt-Series Feedback

This architecture employs the shunt-series resistor, as shown in Figure 2.2(b) to provide load matching. However, it suffers from high power consumption with the same noise figure as other architectures [3]. This is due to its broadband design, which is unnecessary in narrowband applications [5, 6].

2.3.3 Common Gate

In common gate amplifiers, shown in Figure 2.2(c), the input impedance is $1/g_m$, which is made equal to the source resistor, R=50Ω. With a proper choice of bias current, the input impedance is made equal to the source impedance. The capacitors are assumed negligible, the load, Z_L, is noiseless, and r_0 is much larger than Z_L. From MOSFET small-signal model Figure 2.3, the noise factor is given by the following equation [7].

$$NF = \frac{\overline{v_{ns}^2}(\frac{g_m Z_l}{2})^2 / Z_l + \frac{\overline{i_d^2}}{4} Z_l}{\overline{v_{ns}^2}(\frac{g_m Z_l}{2})^2 / Z_l} = \frac{\overline{v_{ns}^2} g_m^2 + i_d^2}{\overline{v_{ns}^2} g_m^2} = 1 + \frac{4KT\gamma g_{d0}}{4KTR_s g_m^2} = 1 + \frac{\gamma g_{d0}}{g_m} = 1 + \frac{\gamma}{\alpha} \qquad (2.41)$$

Long-channel devices have the in-equality $\frac{2}{3} < \gamma < 1$. For short-channel devices, γ is much larger, 2/3 in the saturation region [8]. Letting γ_{L-C} = 2/3 and α = 1, we find the lower limit of $NF_{L\text{-}C}$ for CMOS: 1+2/3=5/3=2.2 dB.

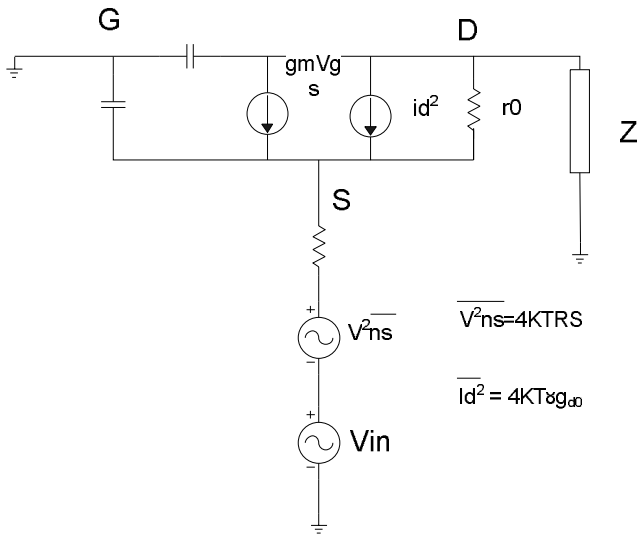


Figure 2.3 Small-signal model of a common gate LNA

The common-gate architecture is easier to match, has greater linearity and provides great reverse isolation for homodyne architecture, which is especially useful in a homodyne system where RF signals are directly shifted to baseband. However, this architecture suffers from an inherently high noise figure. For applications requiring a sub-2-dB NF LNA, this architecture is not a good choice.

2.3.4 Inductive Degeneration

This is the most popular architecture used in LNA designs. It can provide a sub-2-dB NF. The reason it can achieve that low NF is that the noise contributed by the transistor is on the output. The topology is shown in Figure 2.2d. L_g and the parasitic capacitor C_{gs} form a simple L-section matching network to provide the 50 ohm input impedance. Figure 2.4 shows a typical LNA circuit with channel noise. The cascode topology minimizes the Miller effect. Thus, C_{gd} is negligible [3].

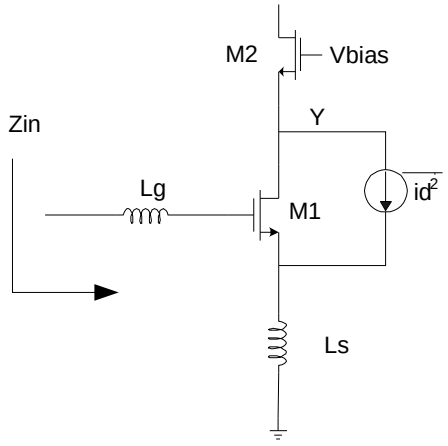


Figure 2.4 Common source cascode LNA

Noise from the second transistor (M2) is minor and is ignored. M2 serves to alleviate the Miller effect of C_{gd} (X and Y). Figure 2.5 is the small-signal model of the device in Figure 2.4, the input impedance is given by equation 2.42.

$$Z_{in} = sL_g + g_m \frac{L_s}{C_{gs}} \_ sL_s + \frac{1}{sC_{gs}} = j\omega(L_g + L_s - \frac{1}{\omega C_{gs}} + \omega_T L_s \qquad (2.42)$$

At the resonance frequency, $\omega = 1/\sqrt{(L_g + L_s)C_{gs}}$, the input impedance is expressed as

$$Z_{in} \approx \omega_T L_s \ at\ \omega = 1/\sqrt{(L_g + L_s)C_{gs}} \qquad (2.43)$$

The 50 ohm input impedance can be achieved by choosing the right value L_s. This inductor can use a bond-wire, which has high Q. L_g can be made with a low-Q on-chip spiral inductor or a high-Q off-chip inductor.

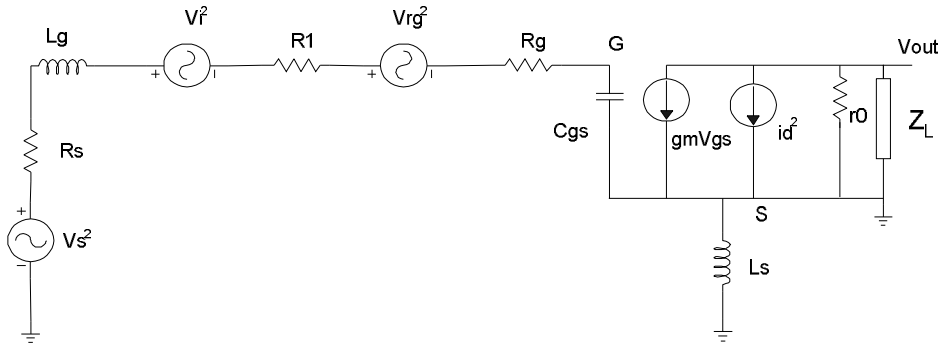


Figure 2.5 Small signal equivalent model of Inductive degeneration LNA

Assuming $r_0 >> Z_{L,}$ L_S is small and its Q is high, so that the series resistor from L_S is neglected. Only thermal noise from channel is considered. The gain from input to output is

$$Gain = A = \frac{g_m Z_l}{sC_{gs}(R_s + sL_g + R_l + R_g) + 1 + s^2 L_s C_{gs} + sL_s g_m} \tag{2.44}$$

At resonance frequency—that is, $\omega = 1/\sqrt{(L_g + L_s)C_{gs}}$, the equation 2.44

$$|Gain| = \frac{g_m Z_l}{\omega_0 C_{gs}(R_s + R_l + R_g + \frac{L_s g_m}{C_{gs}})} = \frac{\omega_T Z_l}{\omega_0 (R_s + R_l + R_g + \omega_T L_s)} \approx \frac{\omega_T}{2\omega_0 R_s} Z_l \tag{2.45}$$

where R_l and R_g are small compared to R_s. [3]

The output noise comes from $\overline{i_d^2}$ and is described as

$$\overline{i_{out}^2} = \frac{\overline{i_d^2}(R_s + R_l + R_g)^2}{(R_s + R_l + R_g + \omega_T L_s)^2} \approx \frac{\overline{i_d^2}}{(1 + \frac{\omega_T L_s}{R_s})^2} \approx \frac{1}{4}\overline{i_d^2} \tag{2.46}$$

and the total NF is

$$NF = \frac{Total\ output\ noise}{Total\ output\ noise\ due\ to\ the\ source} = \frac{\overline{v_s^2}A^2 + \overline{v_l^2}A^2 + \overline{v_g^2}A^2 + \overline{i_{out}^2}Z_l^2}{\overline{v_s^2}A^2}$$
$$= 1 + \frac{R_l + R_g}{R_s} + \frac{KT\gamma g_{d0}}{4KTR_s(\frac{\omega_T}{2\omega_0 R_s})^2} = 1 + \frac{R_l + R_g}{R_s} + \gamma g_{d0} R_s (\frac{\omega_T}{\omega_0})^2 \quad (2.47)$$

with small R_l and R_g , the last term dominates. According to equation 2.47 by decreasing g_{d0} without modifying ω_T, simultaneous improvement of noise figure and reduction of the power dissipation is possible. This can be achieved by scaling down the width of the device while keeping ω_T constant (which only depends on the biasing voltage) and leaving the channel length unchanged.

The analysis above does not consider the gate noise and the noise due to the parasitic resistance of L_g. Choosing a high-Q inductor lowers R_l, and thus lowers the NF, but also reduces the power loss. On the other hand, Q should not be selected too high, which will de-tune the circuits and make them sensitive to the impedance of band filter or antenna.

The minimal NF shown to be[3]:

$$NF_{\min} = 1 + 1.33\left(\frac{\omega}{\omega_T}\right) fixed\ G_m\ (total\ transconduc\tan ce)\ optimization \quad (2.48)$$

$$NF_{\min} = 1 + 1.62\left(\frac{\omega}{\omega_T}\right) fixed\ P_D\ (total\ power\ consumption)\ optimization \quad (2.49)$$

A rule-of-thumb guidance to choose the optimal LNA MOSFET transistor width in the power-constrained condition has been given[9].

$$W_{op,P} = \frac{3}{2}\frac{1}{\omega L C_{OX} R_s Q_{sP}} \approx \frac{1}{3\omega L C_{OX} R_s}.\ L\ is\ gate\ length \quad (2.50)$$

where $Q_{sP} = 1/(\omega C_{gs} R_s)$ is defined as the input's Q. ($Q_{sP} \approx 4.5$)

The second transistor in the cascode load adds some noise, the over NF is computed to be

$$NF_{tot} = 1 + \frac{R_l + R_g}{R_s} + \gamma_1 g_{d01} R_s \left(\frac{\omega_0}{\omega_{T1}} \right)^2 \left(1 + \frac{4 g_{d02}}{g_{d01}} \right) \tag{2.51}$$

The disadvantage of inductive degeneration is its narrowband architecture is not suitable for broadband applications.

2.3.5 Transformer Feedback

This configuration is shown in Figure 2.7e and is similar to inductive degeneration. In ultra-low-voltage designs, where inductive degeneration's transistor stack is not workable, the transformer feedback architecture is more feasible. In this architecture, negative feedback from the transformer neutralizes the Miller effect from C_{gd} by providing some output signal to flow back and cancel the input going into the output through C_{gd} improving linearity. This architecture provides a way to design an LNA with a power supply under one volt, but also increases the linearity [10].

The input impedance matching analysis is similar to inductive degeneration. However, here an on-chip transformer replaces the inductor L_s. Having only one active component lowers NF, but it requires an on-chip transformer, which typically occupies a larger area. Additionally, poor Q and an inaccurate approximation limit this architecture's usefulness.

2.4 VCO Topologies

The Voltage Control Oscillator (VCO) is a key building block for Phase locked loops, which determines the overall phase noise (jitter) performance and the loop bandwidth trade-off. Low phase noise and large tuning range are the two main design objectives for a VCO.

2.4.1 Oscillator Classification

Two primary classifications for the oscillator are based on the output waveform being either sinusoidal or non-sinusoidal. Sinusoidal output oscillators employ a positive feedback loop consisting of an amplifier and a frequency-selective resonator, such as cavity, crystal or LC tank. The amplitude of the output sine wave is limited using a nonlinear mechanism implemented either with a separate circuit or using the nonlinearities of the amplifying device itself [11]. Non-sinusoidal oscillators require only one type of energy storage element, and rely on the threshold switching characteristics of the circuit rather than on a frequency-selective element to define an oscillatory waveform.

For a monolithic implementation in several Giga Hertz range, there are two main types that are used: a ring oscillator using several delay stages, and a LC oscillator, using an inductor and varactor. Ring-oscillator-based VCOs generally exhibit higher jitter than LC resonators, due to lack of high Q circuits to attenuate the thermal and flicker noise of the transistors. LC-based oscillator have better jitter performance that improves with increasing resonator Q. LC oscillator have high Q factor by the nature of its design: a good quality inductor and a minimal number of active

components. LC oscillators have a Q factor that is typically four times the Q factor of a relaxation oscillator. [12]

2.4.2 Oscillator models

2.4.2.1 Feedback Model of oscillators

Oscillators are nonlinear in nature, though are usually viewed as a linear time-invariant feedback system as shown in Figure 2.6. In the *s*-domain, the transfer function of this negative feedback system is given by

$$\frac{V_{out}}{V_{in}}(s) = \frac{A(s)}{1 + A(s)F(s)} \tag{2.52}$$

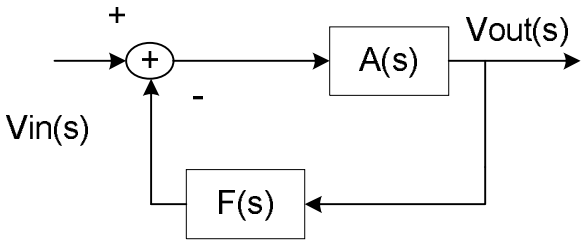


Figure 2.6 Block diagram of negative feedback systems

If the loop gain $A(s)F(s)$ is equal to –1 at a specific frequency ω_0, the closed-loop gain approaches infinity. Under this condition, the feedback becomes positive and the system trends to be unstable. Separating the magnitude and the phase of $A(s)F(s)$, the well-known "Barkhausen criteria" are obtained for the oscillation start-up

$$\left|A(j\omega_0)F(j\omega_0)\right| \geq 1 \tag{2.53}$$

$$\angle A(j\omega_0)F(j\omega_0) = 180° \tag{2.54}$$

To guarantee the effective “regeneration” of the input signal, the magnitude of the loop gain has to be greater than unity (usually choose 2~3 in practical oscillators). The “input signal” here may be generated by any noise or fluctuation in oscillators.

2.4.2.2 Negative Resistance model of oscillators

It is convenient to apply the feedback model to some types of oscillators such as ring oscillators. However, for resonator-based oscillators, an alternative view providing more insight into the oscillation phenomenon employs the concept of “negative resistance”. The resonator can be equivalent to a parallel *RLC* tank circuit, whose R_p (parallel resistance) captures the energy loss inevitable in any practical system. If the tank is stimulated by a current impulse, the tank responds with a decaying oscillatory behavior due to R_p. If a resistor equal to $-R_p$ is placed in parallel with R_p , as shown in Figure 2.7, since $R_p // (-R_p) = \infty$, the tank oscillates at ω_0 indefinitely.

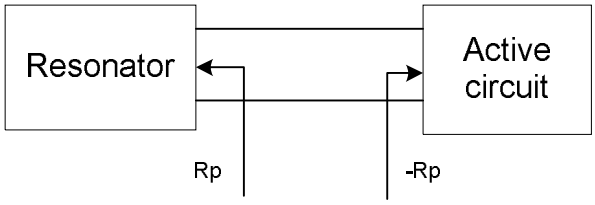


Figure 2.7 a simple negative gm oscillator block diagram

Thus, if a one-port circuit exhibiting a negative resistance is placed in parallel with a tank, the combination may oscillate. This topology is called as negative resistance model.

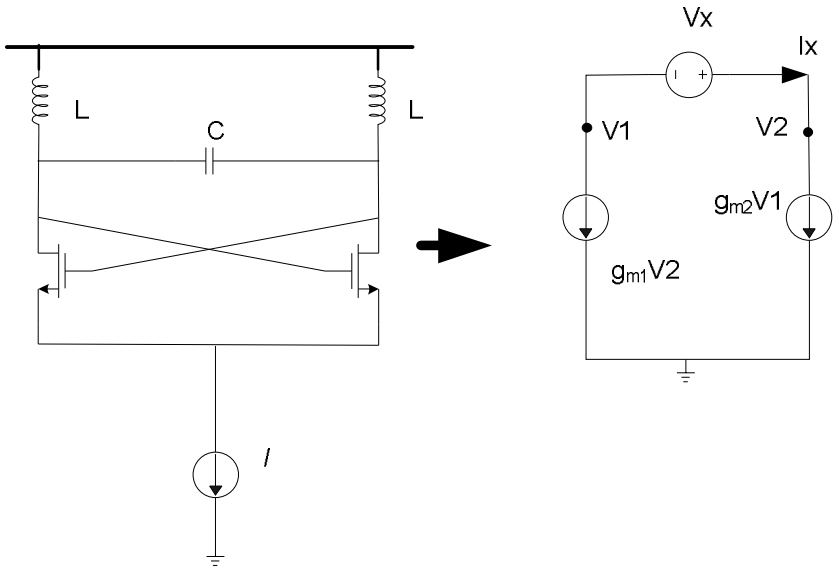


Figure 2.8 Negative resistance provided by cross coupled transistors in LC oscillators

Active circuit can provide the negative resistance required in the negative resistance model. In the *LC* oscillator, the cross-couple transistors can be modeled as the small signal equivalent circuit depicted in Figure 2.8, where the 2nd order effects are neglected. If a voltage source is applied to the input, the following voltage and current equations can be derived

$$V_x = V_2 - V_1 \tag{2.55}$$

$$I_x = g_{m2} \cdot V_1 = -g_{m1} \cdot V_2 \tag{2.56}$$

Therefore, V_x is given by

$$V_x = V_2 - V_1 = -I_x \left(\frac{1}{g_{m1}} + \frac{1}{g_{m2}} \right) \tag{2.57}$$

If two transistors are identical, then the negative resistance is

$$\frac{V_x}{I_x} = \frac{-2}{g_m} \tag{2.58}$$

This negative resistance will compensate the energy loss in the tank if $R_p \leq 2/g_m$ and the oscillation can sustain in the *LC* oscillator.

2.4.3 Ring Oscillator

Ring oscillators have been popular in all-digital phase-locked loops due to their simplicity and ease of integration with other digital circuits. As technology scaling continues to drive faster, higher performance, digital circuits, ring oscillators also benefit and begin to become a viable choice for frequencies needed for Wireless and high-speed data Communication.

Ring oscillators are superior to the LC-based oscillators in several respect. Since ring oscillators consist of only transistors and no bulky inductors, the area required by ring oscillator is significantly smaller. Controlling the frequency can be achieved by varying the current used to charge and discharge the load capacitance. This method can allow a tuning range if 2:1, which is easily enough to compensate for variations due to processing, temperature and age. When a differential inverter is used, an even number of delay stages can be used in the ring. By using an even number, the ring inherently provides quadrature outputs by tapping the signals at different points, as illustrated in Figure 2.9. [13]

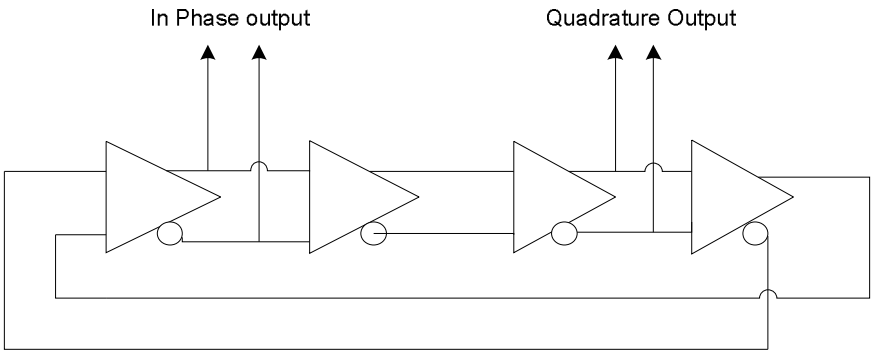


Figure 2.9 Differential 4-stage ring oscillator with quadrature output

While ring oscillators provide the numerous benefits, they have limited use in multi-gigabit data communication due to poor phase noise. The SONET stringent jitter requirement culls for a very low oscillator phase noise. It can be shown that ring oscillators have an equivalent Q of 1-1.5

Using Leeson's Equation, the phase noise of the ring oscillator is about 6-10dB worse than that of a comparable LC tuned oscillator.[14]

2.4.4 LC based Oscillator

A typical LC based oscillator is made up of three distinct blocks as shown in Figure 2.17. The amplifier supplies energy to maintain oscillation in the circuit during the intervals between pulses of excitation energy. The LC tank circuit alternately stores energy in the inductor and the capacitor. A portion of the output of the LC network is fed back to the input of the amplifier through the regenerative-feedback network which helps to sustain oscillation by overcoming the effect of damping caused by the LC tanks internal and load resistance. A greater than unity gain needed to sustain oscillation is

achieved. The operating or center frequency of the oscillator is fixed by the resonant frequency of the LC tank circuit, which is defined by the equation:

$$f_{res} = \frac{1}{2\pi\sqrt{LC}} \tag{2.59}$$

The two types of controlled oscillators include: voltage controlled oscillators (VCO) with a voltage control signal, and current controlled oscillators (ICO) with a current control signal. The VCO is more often used in IC design.

2.4.5 LC Oscillator Topologies

There are several different topologies for LC oscillators. Classical LC oscillator designs were based on simple single-ended configurations. The four classical LC oscillator configurations are: Armstrong oscillator, Hartley oscillator, Colpitts oscillator and Clapp oscillator. They are distinguished by their method of coupling the feedback signal from the LC tank. The more recently introduced differential-pair oscillator has also been gaining popularity and usage. Newer LC oscillator circuit designs currently being introduced are often based on the basic configurations of the classical single-ended LC oscillators. Both Armstrong and Hartley oscillators are inductively coupled. The Armstrong oscillator Figure 2.10(a) uses a transformer to sample its feedback signal from the inductor of the resonant circuit. In the Hartley oscillator Figure 2.10(b), the feedback signal is directly tapped from the inductor. This eliminates the need for another coil.

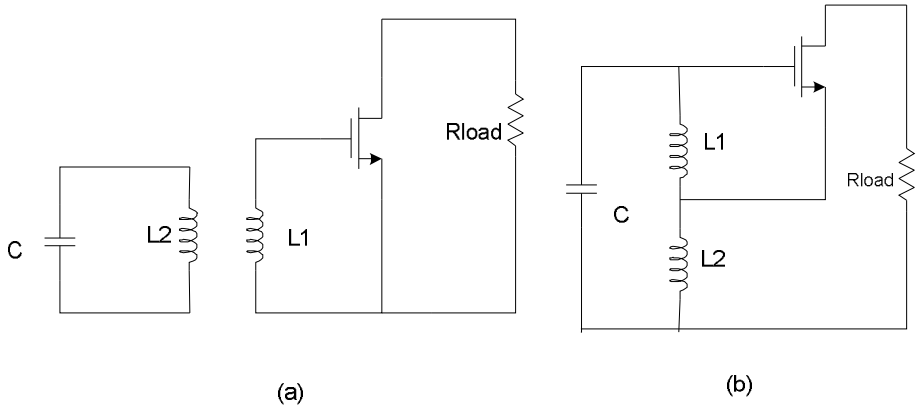


Figure 2.10 (a) A simple Armstrong oscillator (b) A simple Hartley oscillator

The Colpitts and Clapp oscillators are capacitively coupled. The Colpitts oscillator (Figure 2.11(a)) taps its feedback signal from between two capacitors in series within the LC tank. The Hartley oscillator taps the inductor, while the Colpitts oscillator taps the capacitor. The Clapp oscillator (Figure 2.11(b)) is a variation of the Colpitts oscillator, in that the inductors in the LC tank are replaced with an inductor in series with a capacitor. This allows frequency to be tuned via L1 and C3. For a given inductor value, the Clapp configuration has a higher loaded Q than that of the Colpitts oscillator. [15]

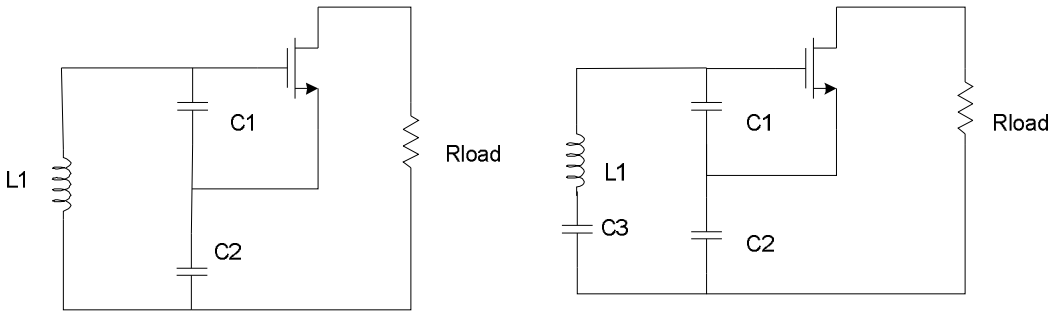


Figure 2.11 (a) A simple Colpitts oscillator (b) A simple Clapp oscillator.

In applications such as Clock date recovery circuits, a tunable with differential or quadrature output is often required. The differential-pair oscillator provides such complementary outputs, while additionally maximizing the rejection of common mode disturbances. The oscillator contains two LC tank circuits with different resonant frequencies. Loop feedback is applied to each tuned circuit in a classical Colpitts configuration.

All LC VCOs described in bipolar technology can also be realized in Standard CMOS technology. Modern differential LC VCO in CMOS technology is much simpler and utilizes only two cross-coupled transistors (FETs) to produce a negative resistance to sustain oscillation. Such topology is called a "negative-gm oscillator" and can be implemented in either NMOS only or PMOS only or combination of both that is complementary, as shown in Figure 2.12[16-18] and Figure 2.13.

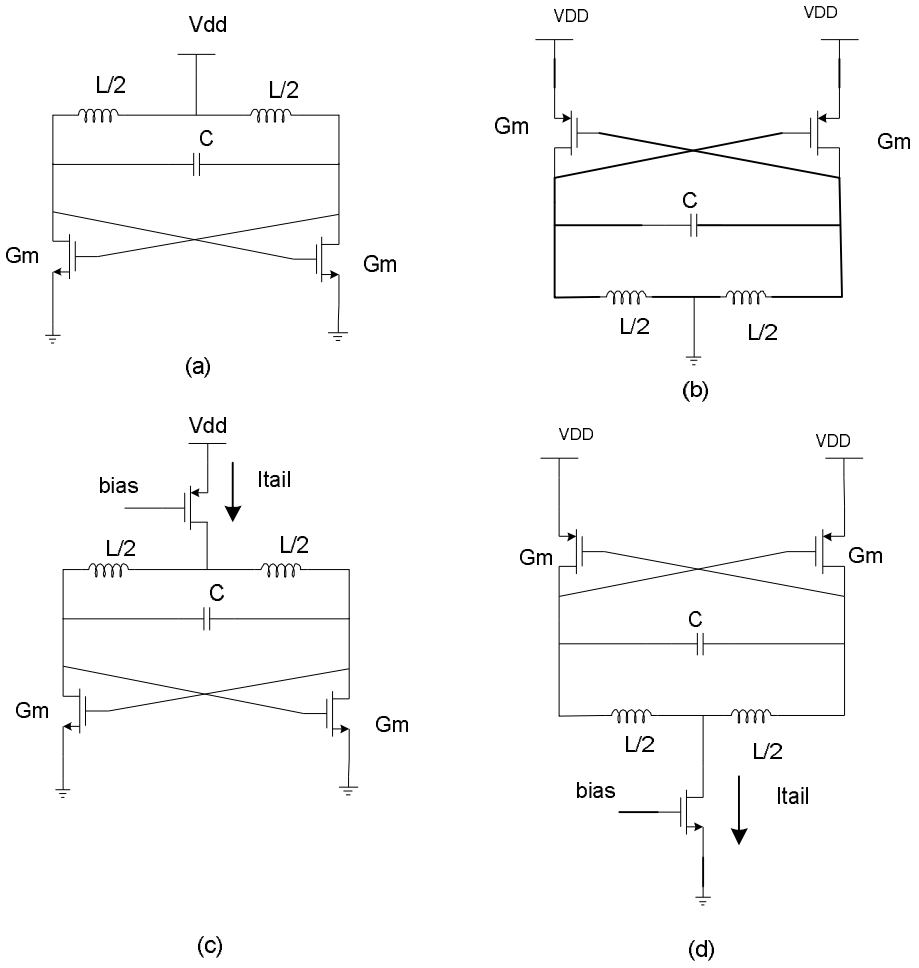


Figure 2.12 LC VCO -Gm Oscillator architectures in (a), (b) are NMOS implementations and (c), (d) PMOS implementations.

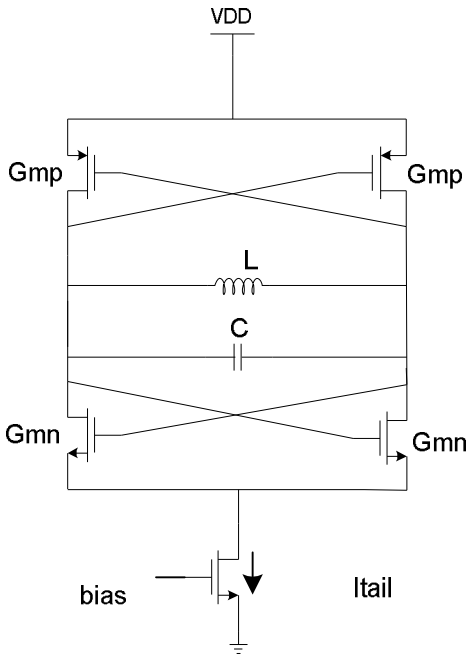


Figure 2.13 LC VCO -Gm oscillator in complementary implementation

2.4.6 Phase noise fundamentals

2.4.6.1 Definition of phase noise

For an ideal oscillator, the output can be expressed as $V_{out}(t) = V_0 \cos[\omega_0 t + \Phi_0]$, where amplitude V_0, the frequency ω_0, and the phase reference Φ_0 are constants. In the frequency domain, the one-side spectrum of such an oscillation signal is an impulse at ω_0. It has power around harmonics of ω_0 if the oscillation waveform is not sinusoidal. More important, due to the existence of the noise generated by active and passive elements, the spectrum of a practical oscillator has sidebands close to and its harmonics, resulting in the fluctuation in oscillation frequency. These sidebands are generally referred as phase noise sidebands.

The phase noise describes the fluctuation of the oscillation frequency. Many ways of quantifying a signal's frequency instabilities have been put forward [19], but it

is usually characterized in terms of the single sideband noise spectral density. It has units of decibels below the carrier per hertz (dBc/Hz) and it is defined as

$$L\{\Delta\omega\} = 10 \cdot \log\left[\frac{P_{sideband}(\omega_0 + \Delta\omega, 1Hz)}{P_{carrier}}\right] \tag{2.60}$$

where $P_{sideband}(\omega_0+\Delta\omega, 1\text{Hz})$ represents the single side-band power at a frequency offset of $\Delta\omega$ from the carrier with a measurement bandwidth of 1Hz as shown in Figure 2.14. Note that the above definition includes the effect of both amplitude and phase fluctuations.

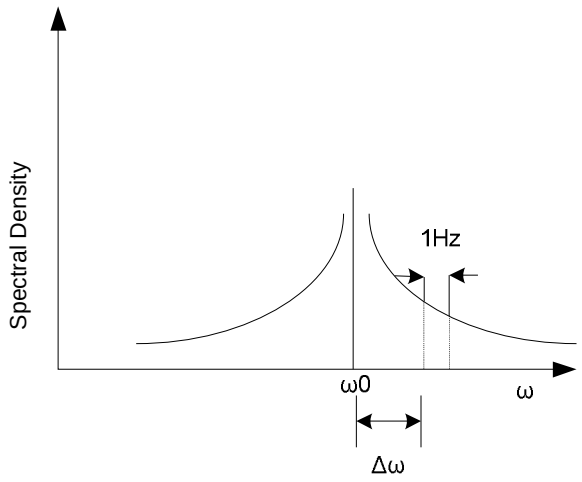


Figure 2.14 Definition of phase noise

2.4.6.2 Effects of phase noise

The destructive effect of phase noise can be best seen in the front-end of a super-heterodyne radio receiver. Figure 2.15 illustrates a typical front-end block diagram, in which the receiver consists of a LNA, a band-pass filter and a down-conversion mixer and the transmitter comprises an up-conversion mixer, a band-pass filter and a power amplifier. The LO that provides the carrier signal for both mixers is

embedded in a frequency synthesizer. If the LO is noisy, both the down-converted signal is corrupted.

Note that a large interferer in an adjacent channel may accompany the wanted signal. When two signals are mixed with the LO output exhibiting finite phase noise, the down-converted band consists of two overlapping spectra, with the want signal suffering from significant noise due to tail of the interferer. This effect is called “reciprocal mixing”.

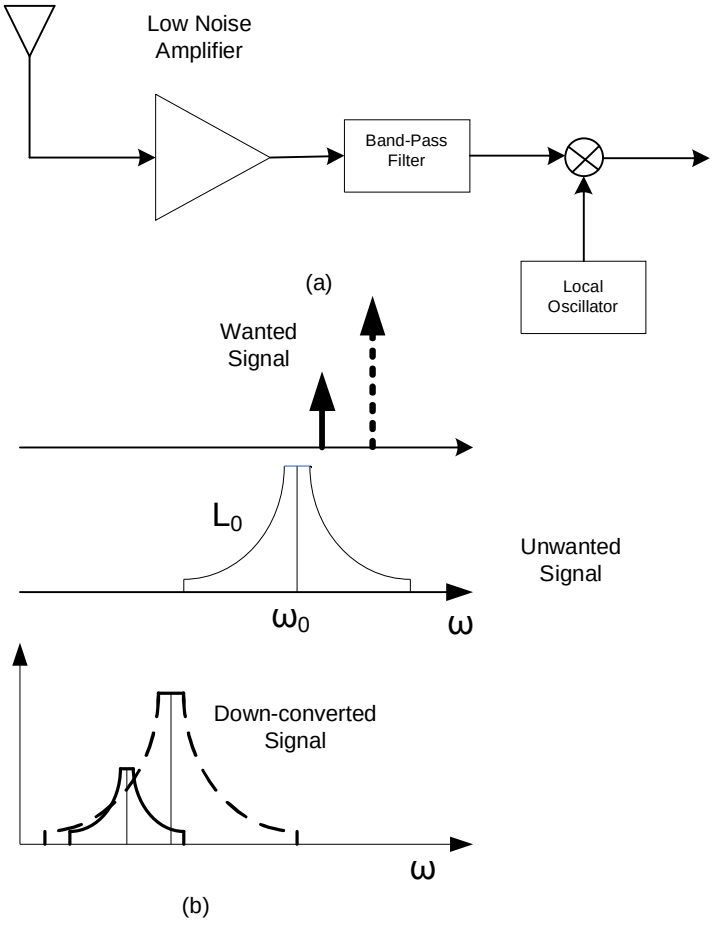


Figure 2.15 (a) Block diagram of wireless receiver (b) Effect of phase noise on receive path

Note the channel spacing in modern wireless communication systems can be as small as a few tens of kilohertz while the carrier frequency may be several hundreds megahertz or even several gigahertz. Therefore, the output spectrum of the LO must be extremely sharp. For example, in a GSM system, the phase noise power per unit bandwidth must be about 118dB below the carrier power (-138dBc/Hz) at an offset of 200 KHz. Such stringent requirements impose a great challenge in low-noise oscillator design.

CHAPTER 3

IMPLEMENTATION

3.1 RF MEMS Inductors

Fully integrated CMOS RF circuits such as low noise amplifiers (LNAs) and voltage-controlled oscillators (VCOs) on standard CMOS silicon substrates (substrate resistivity of about 10 Q-cm) show poor RF performances in noise figure, phase noise, and power consumption, because the monolithic on-chip spiral inductors used along with LNA and VCO suffer from a low quality factor due to the metal ohmic loss and conductive substrate loss [20]. Hence off-chip discrete inductors and bond-wire inductors [21] have been used in the RF applications to provide high quality factor so as to improve the overall RF system performances. But off-chip inductors usually occupy large areas of the RF systems, and bond-wire inductors have a limitation in process repeatability.

Radio-frequency (RF) micro-electromechanical systems (MEMS) technology has been emerging as an alternative to provide major advantages on the existing RF architectures in wireless communication applications such as reduced weight, size, cost, noise, and power consumption over the conventional counterparts [22]. Many research works for RF MEMS on-chip inductors have been carried out to improve Q-factor and self-resonant frequency (SRF) using the partial removal of the Si substrate underneath the planar spiral inductors[23], self-assembly of the out-of-plane inductors[24],

solenoid-based inductors [25], and air- suspended spiral inductors [26]. Especially, air-suspended spiral inductors showed a high Q-factor of up to 70 at 6 GHz and a self-resonant frequency more than 20 GHz.

The RF performance parameters such as noise, gain, and power consumption in typical RF circuits and systems depend on the circuit topology used, the minimum noise figure of the active device, and the quality factor of inductors [27]. The phase noise is inversely proportional to the square of the quality factor of an LC tank used in VCO. Hence high-Q RF MEMS on-chip inductors and capacitors can be used for reduced noise and power consumption, and increased gain in LNA, and for lower phase noise and power consumption in VCO in general wireless transceiver.

3.1.1 Fabrication

The integration of RF MEMS air-suspended circular spiral inductors onto RF circuit chips was carried out using the UV-LIGA technique and an additive pattern transfer technique such as electroplating. Prior to the integration process, the small chip is attached to a carrier substrate to prevent handling problem in subsequent processing. The chip is placed at the center of 3-inch oxidized silicon wafer. [28]

The overall process sequence for the post-IC integration of RF MEMS inductors onto RF circuit chips are shown in Figure 3.1.

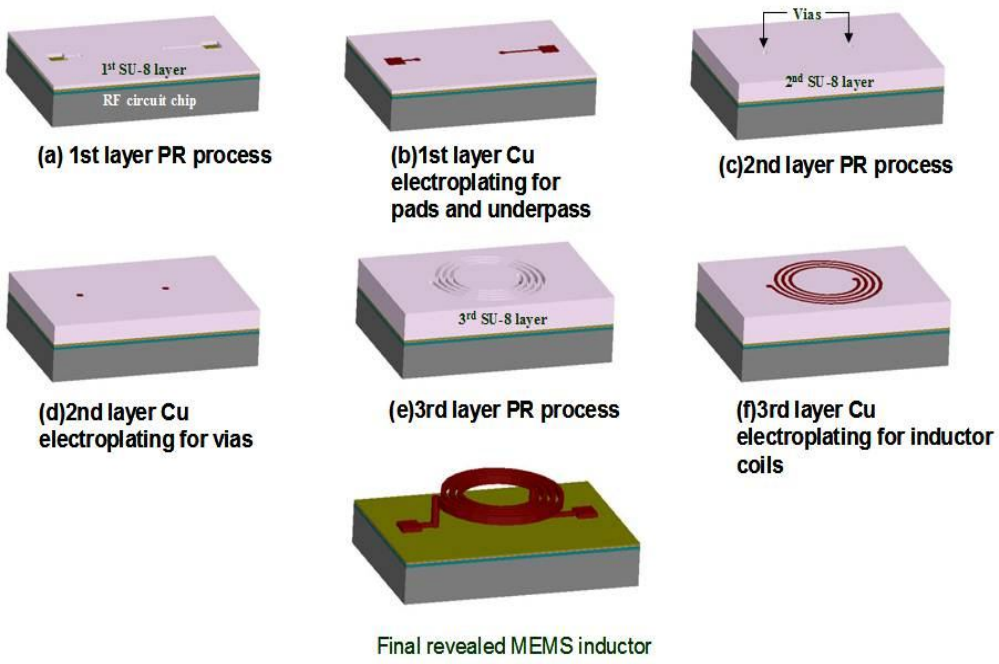


Figure 3.1 Process sequence for post-IC integration of RF MEMS inductors

For the 1st layer process for the pads and underpass, a 10μm thick SU-8 layer is coated on the sample, and followed by the two-step baking and UV-light exposure. The sample then undergoes a de-scum process to be cleaned (Figure 3.1a). The electroplating process is carried out by immersing the sample in Cu electroplating solution to obtain the first metal layer (Figure 3.1(b)).

In the 2nd layer process, a 40 μm thick SU-8 layer is coated for vias between the bottom metal layer and the top metal spiral coils. After the two-step baking and UV-light exposure is applied, the dried sample is cleaned by a de-scum process (Figure 3.1c). Electroplating was carried out by the same condition as the 1st layer metal plating process to obtain 40 μm thick via structures (Figure 3.1d).

For the final layer of the metallic spiral coils, a 20 μm thick SU-8 layer is added. The same process of two-step baking, UV-light exposure gives the 3rd layer

(Figure 3.1e). After final electroplating, a 15 ~ 20 μm thick spiral coil is obtained (Figure 3.1f).

To reveal the air-suspended MEMS spiral inductors, all the SU-8 mold structures are removed using RIE plasma etching. Figure 3.2 shows the scanning electron microscopy (SEM) microphotograph of the micro-machined air-suspended circular spiral inductors on the RF circuit chip. All inductors suspended approximately 50μm from the chip surface to minimize the capacitive parasitic coupling to the substrate. Electroplated copper in spiral coils has the thickness of 20μm so that Q-factor can be maximized due to the low resistivity of copper. [28]

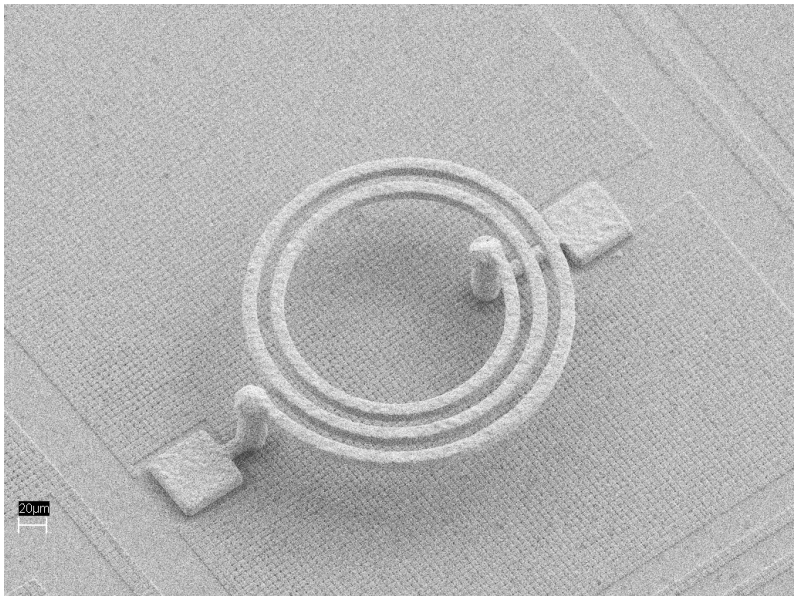


Figure 3.2 SEM microphotograph of micro-machined air-suspended circular spiral inductor

3.1.2 Modeling of Spiral inductor

An on-chip spiral inductor can be modeled by the traditional lumped equivalent model shown in Figure 3.3.

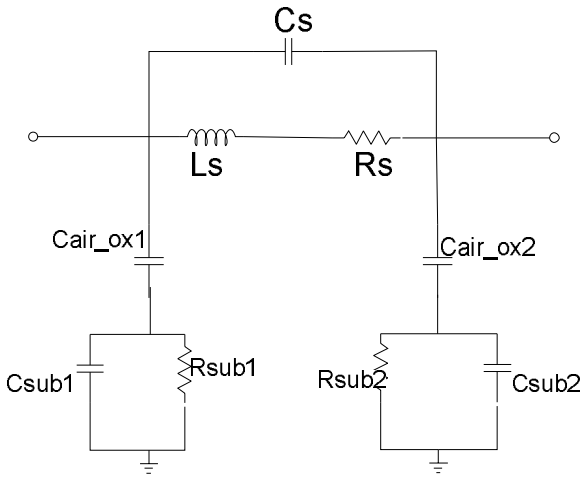


Figure 3.3 Lumped equivalent model of an on-chip inductor

L_s is a series inductance, R_s is a series resistance, and C_s is a inter-turn fringing capacitance and metal overlap coupling capacitance between the spiral and underpass metal layers, C_{sub} and R_{sub} are parasitic capacitance and resistance to the substrate. When the inductor is suspended in air, air-gap capacitance between the spiral inductor and the substrate and the oxide capacitance, C_{air_ox} is included.

3.1.2.1 Inductance

The approximate self-inductance can theoretically computed using the formula

$$L = 4\pi a\left(\ln\frac{8a}{R} - 1.75\right) \tag{3.1}$$

where a is the mean radius of the coil, and R is the geometric mean distance of the rectangular cross section of the coil. The units of a and R are cm, and L is in nH.

3.1.2.2 Resistance

The spiral conductor will have a finite resistivity and a finite cross-section giving the inductor a series resistance R_s to the modeled inductance L_s. At higher

frequencies, the current density across the cross section becomes non-uniform because skin effect and proximity effect due to eddy current appear in the conductor, which result in significant increase in the series resistance R_s. The series resistance can be estimated using the following formula:

$$R = \sqrt{\left(\frac{\rho l}{wt}\right)^2 + \left(k\frac{\rho l}{2\delta(w+t)}\right)^2} \tag{3.2}$$

where ρ is the resistivity, l is the total length of the spiral metal lines, w is the width, t is the thickness, δ is the skin depth, and k is the correction factor (k=1.2).

3.1.2.3 Series Capacitance

The series capacitance C_s represents the parasitic capacitive coupling between input and output of the inductor. It is the sum of inter-turn fringing capacitances between spiral turns and the metal overlap capacitances between the spiral and the underpass metal lines. The value of C_s is usually very small and negligible in the air-suspended spiral inductor.

3.1.3.4 Substrate parasitics

Substrate parasitics include the air gap and oxide capacitance for air suspended spiral inductors $C_{air\text{-}ox}$, substrate capacitance C_{sub}, and substrate resistance R_{sub}. These parasitics play a major role in the reduction in the quality factor and the self-resonant frequency. The magnetic field of the spiral inductor penetrates into the substrate and induces the electric field in the substrate, which produces circular current loop in the substrate imitating the current loop in the spiral inductor [29]. Such substrate current opposes the original current flow in the spiral inductor, decreasing the original magnetic

flux magnitude of the spiral inductor. This has significant effects on the inductance and the quality factor of the spiral inductor. RF CMOS processes use low resistivity Si substrates, the substrate loss due to this substrate current effect is inevitable at high frequencies and should be avoided as much as possible.

3.1.3 Inductor parameter extraction

For parameter extraction of the spiral inductor, a measurement setup for high frequency characterization is employed which is combination of vector network analyzer, S-parameter test set and a frequency sweeper. The S-parameters measurements are made, and the Arcioni et al‘s method [30] with matrix inversion and multiplication is used for de-embedding the probe pad and ground plane parasitics. This method involves conversion of S-parameters matrix to ABCD-parameter matrix using following equation

$$A = \frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{2S_{21}} \tag{3.3}$$

$$B = 50\frac{(1+S_{11})(1+S_{22})-S_{12}S_{21}}{2S_{21}} \tag{3.4}$$

$$C = \frac{1}{50}\frac{(1-S_{11})(1-S_{22})-S_{12}S_{21}}{2S_{21}} \tag{3.5}$$

$$D = \frac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{2S_{21}} \tag{3.6}$$

The ABCD-parameter matrix is de-embedded and converted to Y parameters, Y_π for inductor modeling using following equations

$$Y_{\pi 11} = \frac{D}{B} \tag{3.7}$$

$$Y_{\pi 12} = \frac{-(AD - BC)}{B} \tag{3.8}$$

$$Y_{\pi 21} = \frac{-1}{B} \tag{3.9}$$

$$Y_{\pi 22} = \frac{A}{B} \tag{3.10}$$

The information in the de-embedded matrix Y_π allows characterization of the admittance of Y_s , Y_{SUBin}, Y_{SUBout} of the network shown in Figure 3.4.

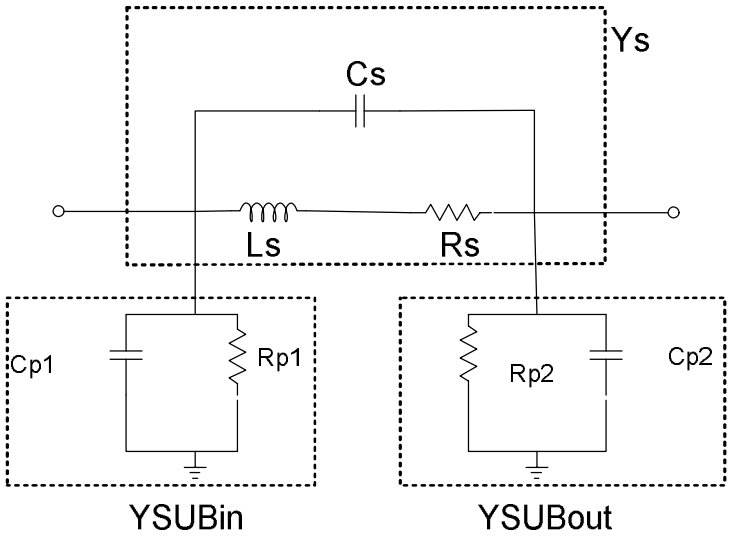


Figure 3.4 Pi-network inductor model

$$Y_S = -Y_{\pi 12} = \frac{1}{Z_s} \tag{3.11}$$

$$Y_{SUBin} = Y_{\pi 11} + Y_{\pi 12} = \frac{1}{Z_{p1}} \tag{3.12}$$

$$Y_{SUBout} = Y_{\pi 22} + Y_{\pi 21} = \frac{1}{Z_{p2}} \tag{3.13}$$

C_s is independent of frequency and is very small; it can be extracted using the values for low frequency $L_{low\text{-}freq}$ and resonant frequency of the inductor ω_0:

$$C_S = \frac{1}{\omega_0{}^2 L_{low-freq}} \tag{3.14}$$

L_s and R_s are extracted from imaginary and real parts of the series impedance Z_s and the measured frequencies.

$$L_S = \frac{\mathrm{Im}(Z_S)}{\omega} = \frac{\mathrm{Im}(-1/Y_{\pi 12})}{\omega} \tag{3.15}$$

$$R_S = \mathrm{Re}(Z_S) = \mathrm{Re}(-1/Y_{\pi 12}) \tag{3.16}$$

The substrate parasitics C_p and R_p is extracted from the imaginary and real part of Z_{P1} and Z_{P2}.

$$C_{P1} = \frac{\mathrm{Im}[\frac{1}{Z_{P1}}]}{\omega} = \frac{\mathrm{Im}(Y_{\pi 11} + Y_{\pi 12})}{\omega} \tag{3.17}$$

$$R_{P2} = \frac{1}{\mathrm{Re}[\frac{1}{Z_{P1}}]} = \frac{1}{\mathrm{Re}(Y_{\pi 11} + Y_{\pi 12})} \tag{3.18}$$

$$C_{P2} = \frac{\mathrm{Im}[\frac{1}{Z_{P2}}]}{\omega} = \frac{\mathrm{Im}(Y_{\pi 22} + Y_{\pi 21})}{\omega} \tag{3.19}$$

$$R_{P2} = \frac{1}{\mathrm{Re}[\frac{1}{Z_{P2}}]} = \frac{1}{\mathrm{Re}(Y_{\pi 22} + Y_{\pi 21})} \tag{3.20}$$

HFSS simulations is employed verify and compare with measurement results. The chips are fabricated in TSMC 0.35 μm, it uses a low resistivity 250 μm thick substrate (0.008 – 0.02 Ω-cm), and an 8 μm thick epitaxial layer (8 -12 Ω-cm).

Passivation layers are assumed to be 2 μm thick silicon dioxide layers and 4 μm thick silicon nitride layers. These substrate properties are important for accurate simulations of the RF MEMS inductors on MOSIS substrates to obtain the required inductance values used in LNA and VCO.

Using the Arcioni method for parameter extraction from S-parameters, the measurement results and HFSS simulation results come within 10-20% range of each other. The lumped physical model with extracted parameter values is shown in figure.

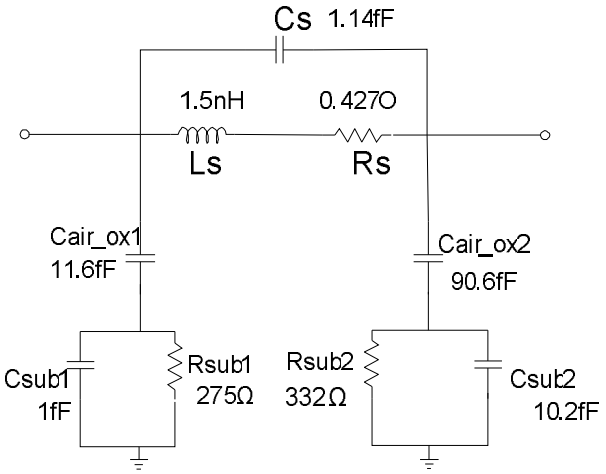


Figure 3.6 MEMS inductor model with extracted parameters

3.1.4 Comparison: RF MEMS inductor vs. Monolithic on-chip Inductor

In this work, both RF MEMS inductor and monolithic on-chip inductor are used to design the LNA and VCO for comparison. The planar monolithic inductors are layout and simulated using ADS Momentum for S-parameter simulation. The Q factor and inductance value L are extracted from the S-parameters and plotted versus frequency. Figure 3.7 shows the planar monolithic inductor layout of a 3.5 turn 4.5nH with width of 2 μm and a spacing of 0.5 μm. It is seen in Figure 3.8 that the RF MEMS inductor

achieves a more constant inductance value of 4.5nH over a large frequency range compared to monolithic planar inductors. Also the Q-factor of the RF MEMS inductor is 80 compared to 10 of monolithic planar inductor.

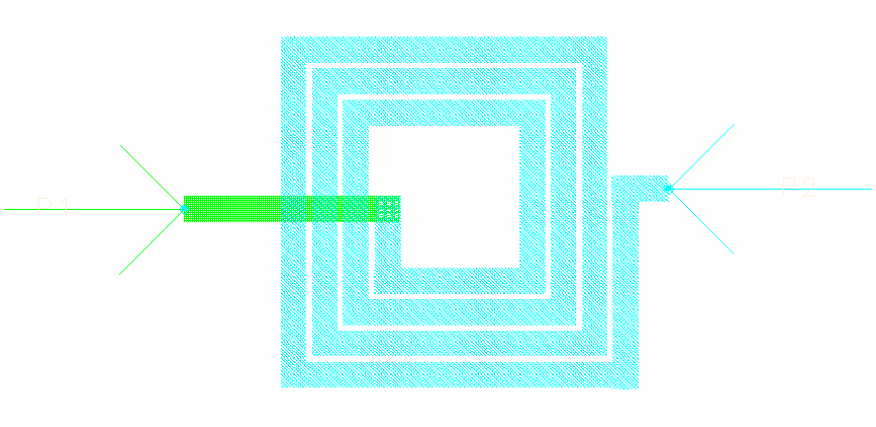
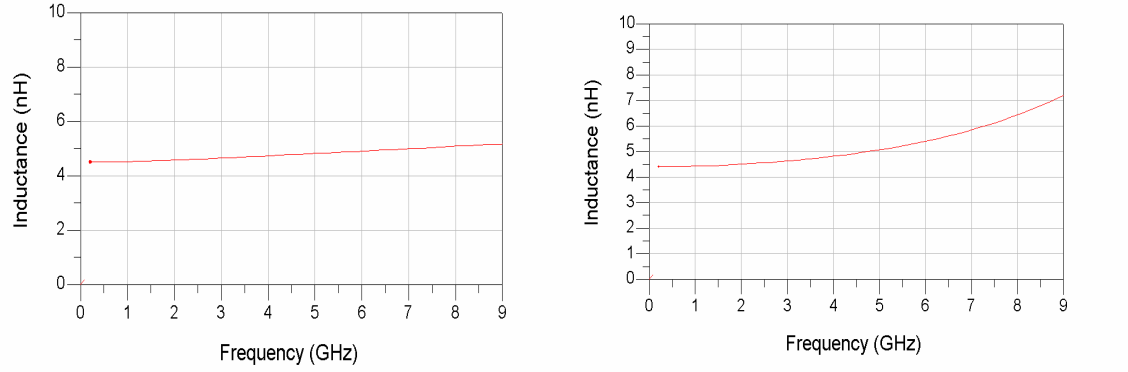
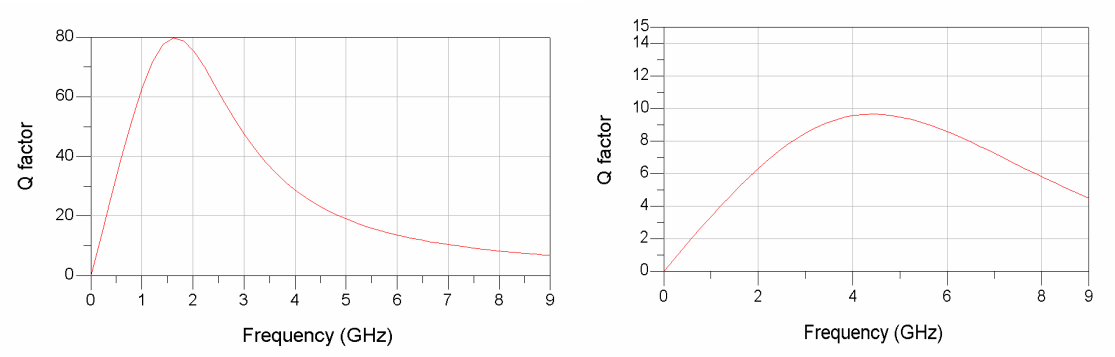


Figure 3.7 Monolithic planar inductor layout in ADS



(a) (b)

Figure 3.8 Inductance (a) RF MEMS inductor (b) Monolithic on-chip Inductor.



(a) (b)

Figure 3.9 Q factor of (a) RF MEMS inductor (b) Monolithic on-chip Inductor

3.2 Low Noise Amplifier Design

In this work, a single-transistor inductive-degeneration topology is chosen for the Low-noise amplifier (Figure 3.10). This topology is chosen as it is capable for providing noise figure below 3dB. Inductors at the gate and source, L_g and L_s along with the parasitic capacitor C_{gs} form a simple L-section matching network to provide 50Ω input impedance. The cascode structure is not implemented in-order to obtain high gain. The C_{gd} effect on the input impedance is minimized by choosing proper values for L_g and L_s. In the output loop, the drain inductor L_d gives maximum impedance, and hence maximum gain at the oscillation frequency. The oscillation frequency depends on the value of L_d and capacitance seen at the drain of the transistor.

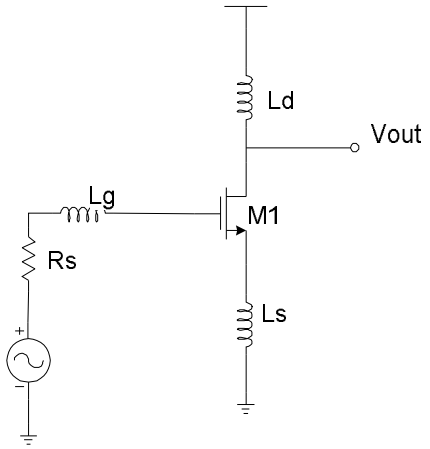


Figure 3.10 Low noise amplifier topology

Target specifications are chosen within the range of specifications specified by Bluetooth and Wifi standards.

Table 3.1 Target Specifications [1]

Parameter	Target value
Frequency	2.4 GHz
Inductor values limits	<10nH
Current consumption	<7mA
Gain	>10dB
Noise figure	<3dB

3.2.1 Design Procedure

In this work, the low noise amplifier and voltage controlled oscillator is designed in TSMC 0.35 µm technology. The process technology parameters from the TSMC 0.35 µm for NMOS and PMOS are shown in Table 3.2.

Table 3.2 TSMC 0.35µm process technology parameters

Parameter	Value	**Parameter**	Value
Min. L	0.35 (0.4) ㎛	**Tox**	75 angstroms
Min. W	0.35 (0.4) ㎛	**Cox**	46.02E-6 F/m
Vdd	3.3 V	**Lamda**	0.2
Mo	0.0487 ㎠/V/s	**Vtho**	0.57 V

From [9], the optimum transistor width $W_{opt\ P}$ for minimum noise figure within the power constraint of the process is estimated by:

$$W_{opt\ P} = \frac{1}{3\omega L C_{OX} R_S} \tag{3.21}$$

Where L is channel length, C_{ox} is gate oxide capacitance and R_s is source resistance. With R_s = 50Ω, L =0.4μm and C_{ox} = 4.49fF/ μm^2 (for TSMC 0.35μm technology), $W_{opt\ P}$ is calculated as 281μm. With device width $W_{opt\ P}$, the noise figure obtained within the power constraint is given by equation 3.22.

$$F_{\min P} \approx 1 + 2.4\frac{\gamma}{\alpha}[\frac{\omega}{\omega_T}] \tag{3.22}$$

The value for ω_T is approximately about 2.3GHz for a self-biased transistor of 281 μm in TSMC 0.35μm technology. The factor α is commonly assumed to be 0.85 [9] and γ is assumed as 2. Substituting these values in equation 3.22, noise figure for this amplifier is approximately 3.2 dB. To decrease noise figure even further, ω_T needs to be increased. This is done by increasing current through transistor which is requires higher transistor width. As the transistor width is increased to 400μm, the ω_T increases to 3.6 GHz and noise figure decreases to 2.5dB which satisfies the target noise figure.

The next step is to obtain input matching between the LNA and the source. The source resistance R_s is 50Ω.The input impedance of an inductively degenerated common-source amplifier is computed from Figure3.11.

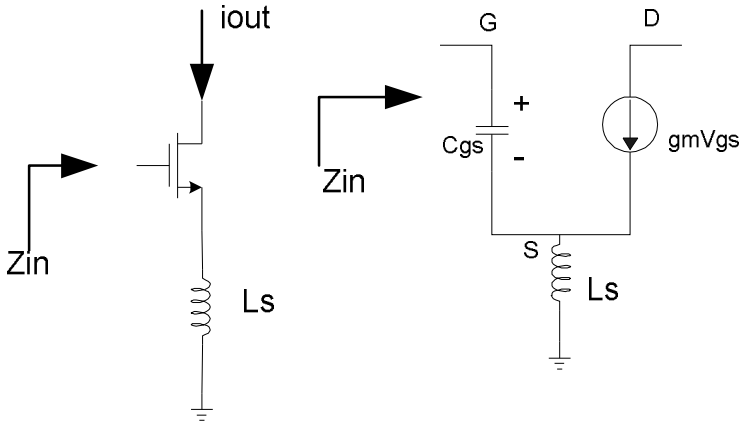


Figure 3.11 Input impedance of low noise amplifier and its small signal equivalent circuit

$$Z_{in} = sL + \frac{1}{sC_{gs}} + \frac{g_m}{C_{gs}}L \approx sL + \frac{1}{sC_{gs}} + \omega_T L \tag{3.23}$$

For input matching of the common-source amplifier, the real part of Z_{in} must be equated to 50Ω. The value for ω_T is approximately about 3.6GHz for a self-biased transistor of 400μm in TSMC 0.35μm technology. The value of L_s is computed as:

$$\mathrm{Re}(Z_{in}) = \omega_T L_S \Rightarrow 50 = (2\times\pi\times 3.6G)L_S \Rightarrow L_S = 1.9nH \tag{3.24}$$

With the calculated the transistor width and source inductor value, the input loop of the common-source amplifier needs to be tuned to the target operating frequency. The input loop is a series LC tank. The LNA should have purely real input impedance at the tuning frequency. It follows that the imaginary part of Z_{in} must be equal to 0 at f=2.4GHz.

$$\mathrm{Im}(Z_{in}) \Rightarrow sL + \frac{1}{sC_{gs}} = 0 \Rightarrow f = \frac{1}{2\pi\sqrt{LC_{gs}}} \tag{3.25}$$

Here, $C=C_{gs}$ of the transistor which is approximately 0.4pF for a 400μm. The required L is found to be:

$$L = \frac{1}{4\pi^2 (0.4p)(2.4G)^2} \Rightarrow L = 10nH \qquad (3.26)$$

To make the total inductance of the input loop of the amplifier equal to 10nH, an additional inductance L_g of (L-L_s) 8.1nH is added at the gate of the transistor.

At the output, the drain inductor L_d is gives high gain at the center frequency and simultaneously provides an additional level of band pass filtering. The inductance value is chosen such that the output loop of the LNA tunes to operating frequency of 2.4GHz with the drain capacitance of the transistor. L_d is calculated to be 4.5nH for an estimated drain capacitance of 1pF.

3.2.2 Simulation Results

The designed low noise amplifier is simulated in Agilent's Advance Design System (ADS). TSMC 0.35 μm CMOS process models are used for simulation. For the RF-MEMS inductors the extracted model provided by University of Texas at Dallas Micro/Nano devices and systems (Minds) group. The planar monolithic inductors were designed in ADS Layout and extracted as a component to be used in the ADS schematic simulator.

Table 3.3 Component values used in design of LNA

Component	Value	Component	Value
L_g	8.9nH	**M1**	400μm
L_s	1.5nH	**Vdd**	3.3 V
L_d	4.53nH		

3.2.2.1 LNA with RF MEMS inductor

Figure 3.12 shows the S parameter simulation result of the LNA with RF MEMS inductors. At 2.4 GHz, S21 is measured to be 10.03 dB, S11 is -10.8 dB and S22 is -12.93dB. The results prove that the input and output impedances are matched.

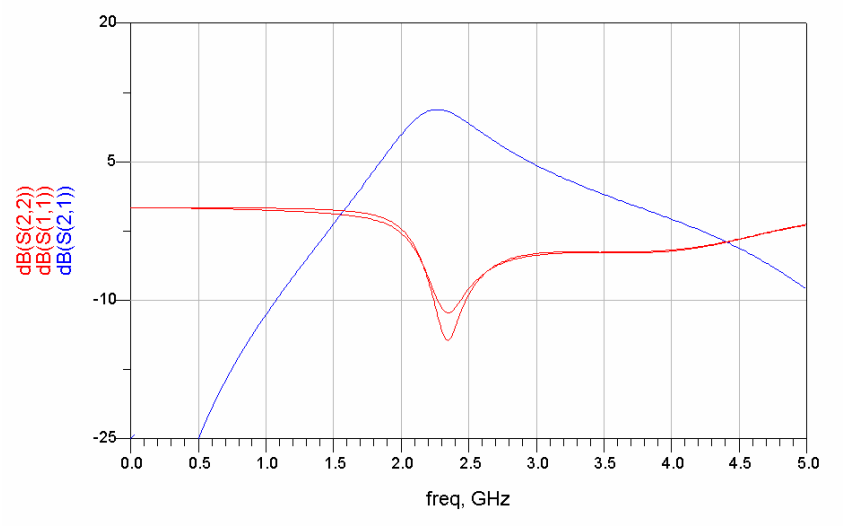


Figure 3.12 S parameter simulation result of LNA with RF MEMS inductor.

Figure 3.13 shows the noise figure of the LNA with RF MEMS inductor. The noise figure at 2.4GHz is 0.8dB. The low noise figure is estimated to be much lower than the expected 2.5dB. This is due to pessimistic assumption of constants α and γ in equation 3.22.

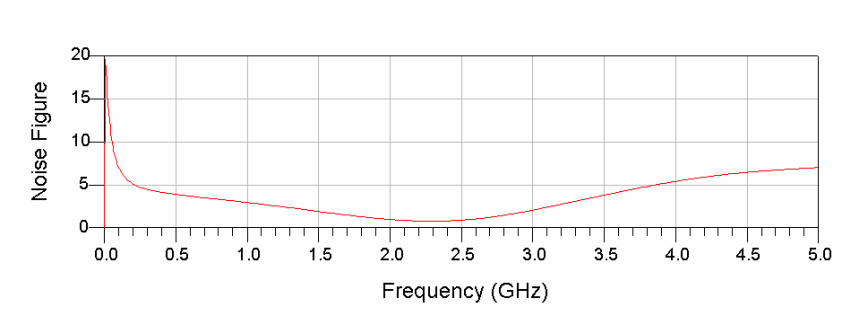


Figure 3.13 Noise Figure of LNA with RF MEMS inductor.

The variation of stability factor with frequency is shown in figure 3.14. The stability factor at 2.4 GHz is 1.143 showing the LNA is stable at the operating frequency.

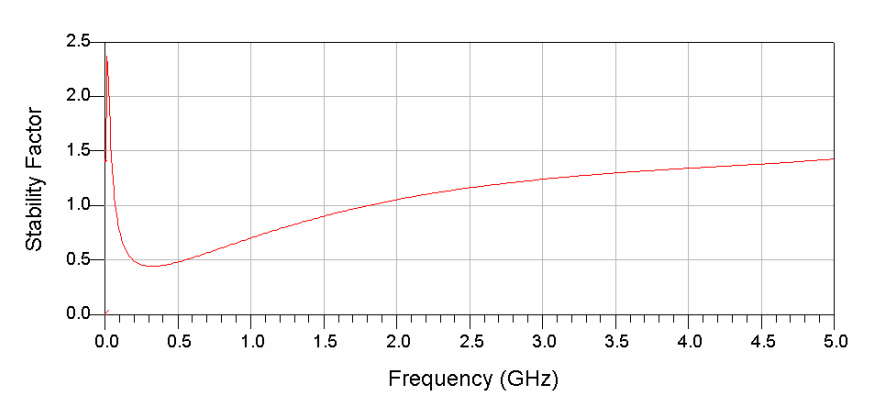


Figure 3.14 Stability factor of LNA with RF MEMS inductor

The 1-dB compression point using a 1-tone input test and inter-modulation components at the output using a 2-tone input test is shown in Figure 3.15 and Figure 3.16 respectively. The 1-dB compression point is 5.4 dBm and third order intercept point is 19.16 dBm.

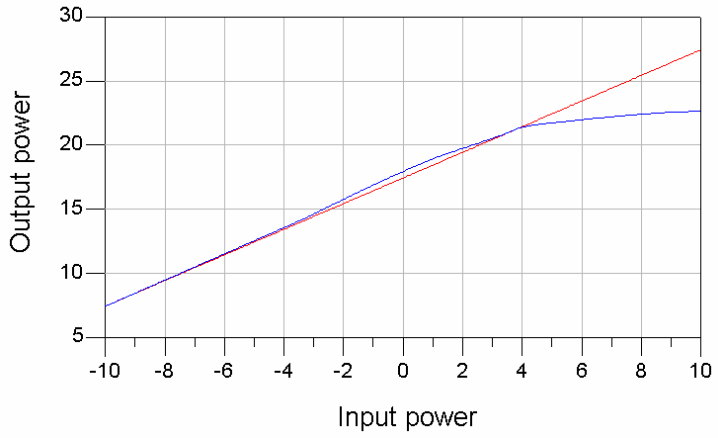


Figure 3.15 Output power versus Input power at 2.4 GHz

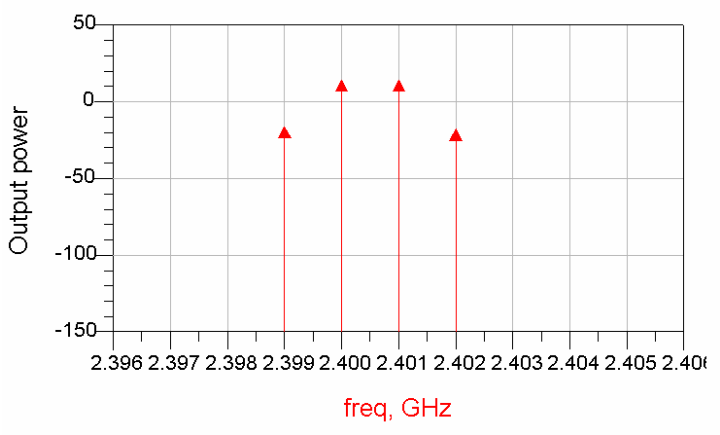


Figure 3.16 Third order inter-modulation components at the output

3.2.2.2 LNA with Planar monolithic inductor

The S parameter simulation result of the LNA with planar monolithic inductors is shown in Figure 3.17. The power gain S21 is 6.342 dB, S11 is -19dB and S22 is -10.1dB. This shows that LNA with spiral inductor is well matched, but it has about 3.6dB less gain than that of the LNA with RF MEMS inductor.

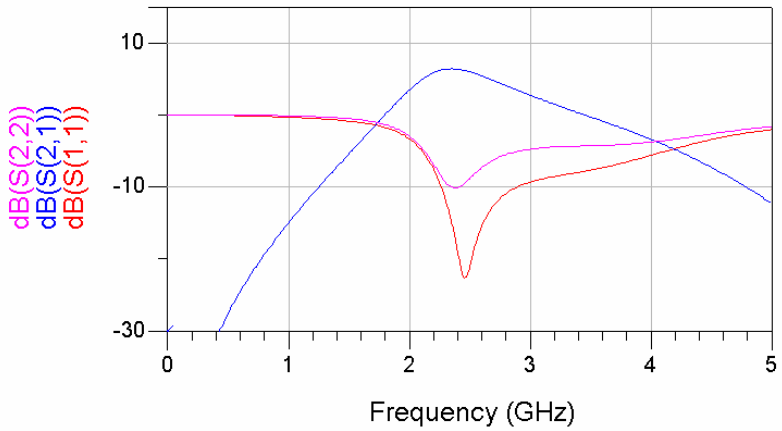


Figure 3.17 S parameter simulation result of LNA with planar monolithic inductor

The noise figure of LNA with planar monolithic inductor at 2.4GHz is equal to 2.9dB. This is high as compared to LNA with MEMS inductors, due to the low Q of

planar inductors, the parasitic resistances are larger. This large parasitic resistance produces more noise current increasing noise figure.

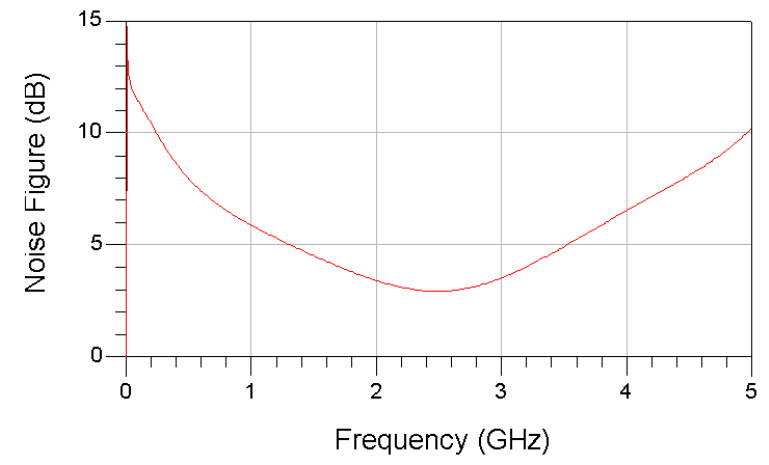


Figure 3.18 Noise Figure of LNA with planar monolithic inductor.

The stability factor of the LNA with planar monolithic inductor at 2.4 GHz is 1.792.

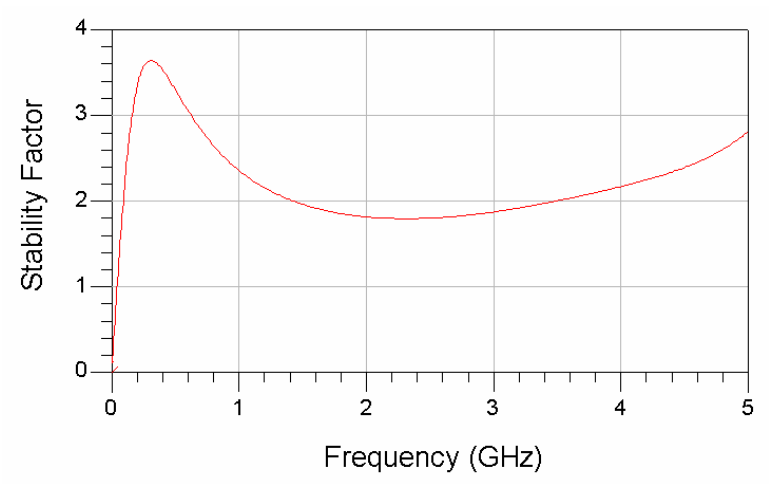


Figure 3.19 Stability Factor of LNA with planar monolithic inductor.

The 1-dB compression point using a 1-tone input test and inter-modulation components at the output using a 2-tone input test is shown in Figure 3.20 and Figure

3.21 respectively. The 1-dB compression point is 6.4 dBm and third order intercept point is 14.87 dBm.

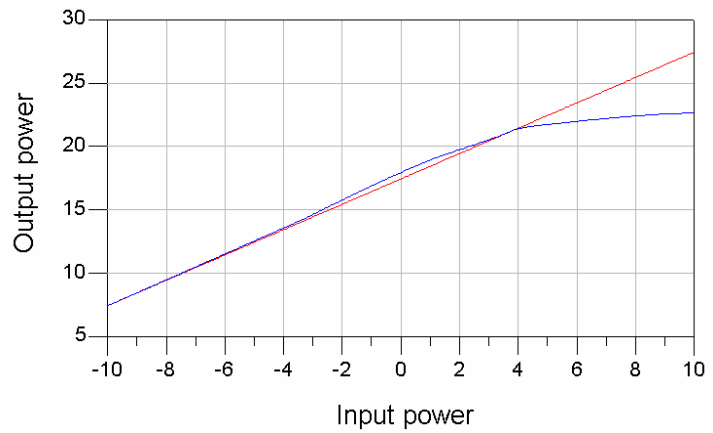


Figure 3.20 Output power versus Input power at 2.4 GHz

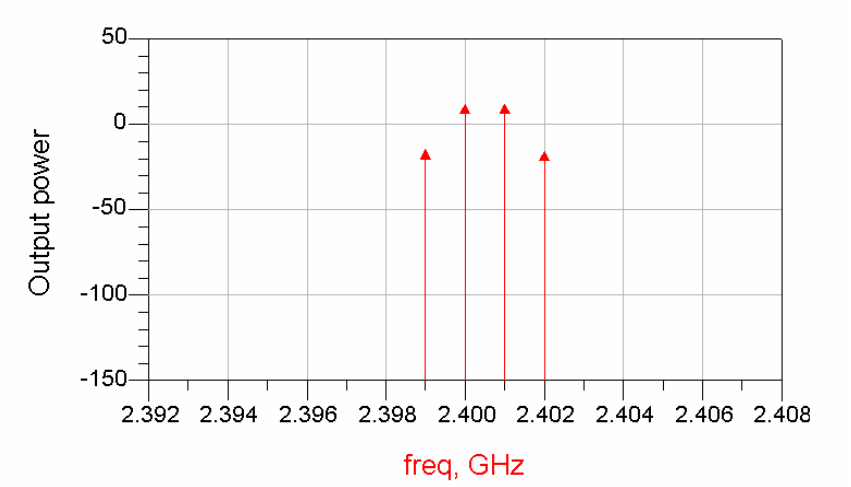


Figure 3.21 Third order inter-modulation components at the output

Table 3.4 LNA performance

LNA	w/RF MEMS	w/Planar Monolithic
S21	10	6.34dB
S11	-10.8dB	-19dB
S22	-12.93dB	-10.1dB
Noise Figure	0.8dB	2.92dB
Stability Factor	1.143	1.7

Table 3.4 shows a comparison of performance of LNA with RF MEMS and planar monolithic inductors. Table 3.5 shows comparison of LNA in this work with recent 2.4GHz LNAs.

Table 3.5 Performance comparison with recent 2.4 GHz LNAs

Ref. No.	S11(dB)	S21(dB)	NF(dB)	CMOS (Tech)	Power
[31]	-20	15	6.5	0.18µm	14.6mW
[32]	-7.1	13.8	2.8	0.18µm	6.5mW
[33]	-25	6	4.8	0.35µm	n/a
[34]	-30.8	13.29	2.87	0.25µm	11mW
[35]	-5.8	23	3	0.18µm	36mW
[36]	7	14.7	2.88	0.25µm	28.5mW
This work	-10.8	10	0.8	0.35µm	21mW

3.2.3 Layout & Chip Photo

The layout of the LNA was done using Cadence. Figure 3.22 shows the layout of the LNA. The three empty squares with open pads were provided for post-integration of the RF MEMS inductors.

A scanning electron microscopy(SEM) microphotograph of the LNA with the post-IC integrated RF MEMS inductors is shown in Figure 3.23.

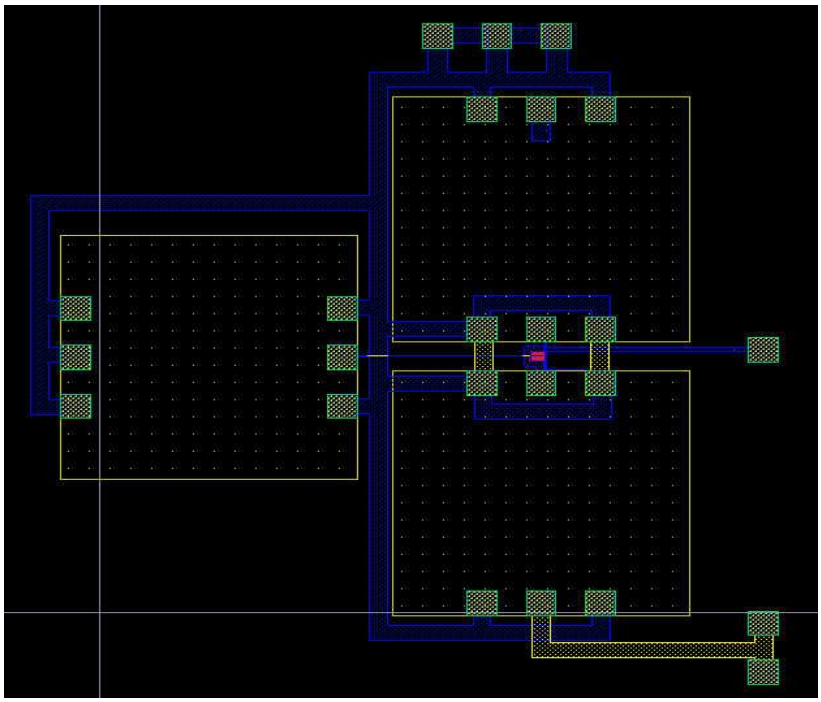


Figure 3.22 Layout for the LNA with RF MEMS inductors

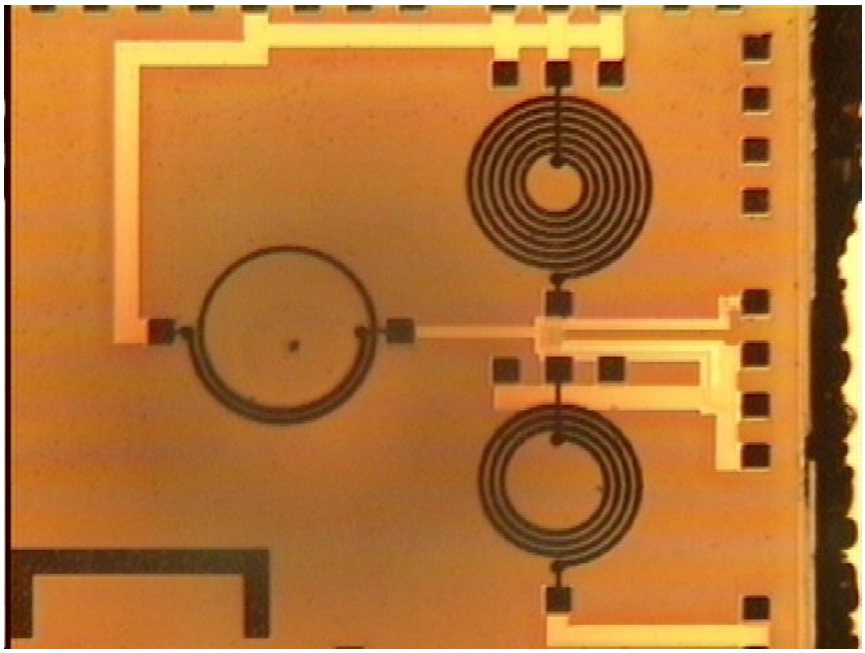


Figure 3.23 SEM microphotograph of the LNA after post-integration of micro-machined RF MEMS Inductors

3.3 Voltage Controlled Oscillator Design

In this work, the cross-coupled NMOS-only LC VCO is chosen to implement the VCO (Figure 3.24). This topology is chosen for its ease to implement, and its differential output which is often required in clock data recovery circuits. The differential-pair also helps in common-mode noise rejection. This topology has better phase noise performance as compared to other oscillators is because of the high Q of the LC tank which gives a narrower frequency response. The minimal number of active components helps in reduction of parasitics contributed by them, and the minimal number of passive components helps in ease of layout and smaller.

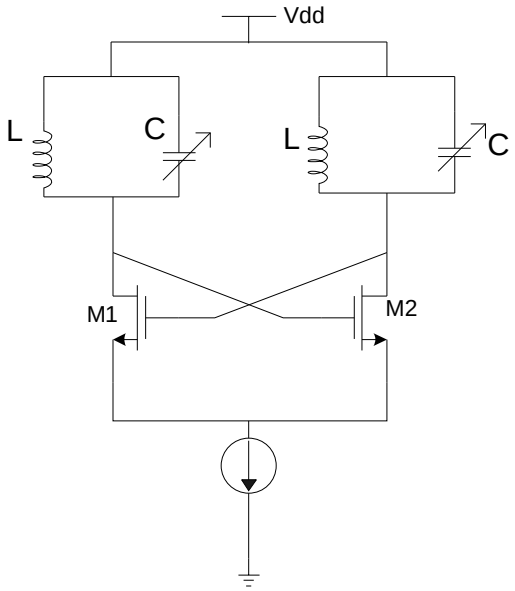


Figure 3.24 Voltage controlled oscillator topology

Target specifications are chosen within the range of specifications specified by Bluetooth and Wifi standards.

Table 3.6 Target specifications for VCO [1]

Parameter	Target Value
Frequency	2.4 GHz
Current consumption	<25mA
Voltage swing	>1V output

3.3.1 Design Procedure

3.3.1.1 Resonator tank design

The tank inductor and capacitance values decide the oscillation frequency. The inductance value is kept low to have the minimum parasitics and high-Q. The minimum value of inductance the RF MEMS inductor process provides is 1.5nH. From the frequency of oscillation formula for a parallel LC network, the capacitance value required to obtain an operating frequency of 2.4 GHz is calculated as:

$$f = \frac{1}{2\pi\sqrt{LC}} \Rightarrow Creq = \frac{1}{4\pi^2 Lf^2} = 2.9\,fF \qquad (3.27)$$

3.3.1.2 Varactor Design

The Varactor is a voltage-controlled capacitor used in microwave applications, including band-pass filter, phase shifter, voltage-controlled oscillator, mixer, non-linear transmission line and frequency multipliers. It is used as an element in an LC resonant tank so that the resonance tank so that the resonance frequency can be varied inversely proportional to the square root of the capacitance value. In VCOs, the applied bias voltage to the varactors determines the oscillation frequency through capacitance variation.

In this work, MOS varactor is implemented. It provides higher capacitance density as compared to metal-insulator-metal capacitors and varactor diodes. By tying the source, drain and bulk terminals of a MOSFET together and varying the voltage applied between the resulting terminal and the gate, the charge layer beneath the gate oxide in a standard NMOS transistor will vary. This creates a capacitance between the heavily doped n^+ polysilicon gate electrode and the drain/source/body connection that can be easily tuned by varying a single DC voltage.

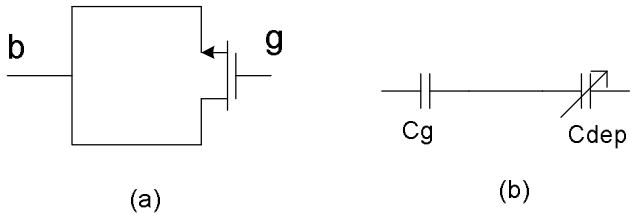


Figure 3.25 (a) MOS varactor (b) simplified MOS varactor model

From Figure 3.26, the gate terminal voltage drops below the voltage of the channel, a depletion region forms beneath the gate oxide. The width of this depletion region varies with the magnitude of the voltage difference, creating an additional capacitance, C_{dep}, in series with the gate-channel capacitance, C_g, reducing the total capacitance. This varying capacitance is roughly calculated as [37]:

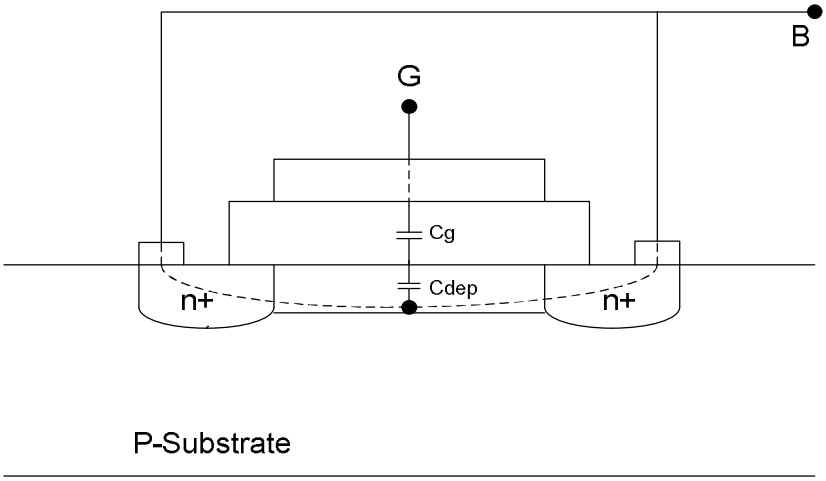


Figure 3.26 simplified MOS varactor model

$$C_{\text{var}} = W_{eff} L_{eff} \frac{C_{ox} C_{dep}}{C_{ox} + C_{dep}} \tag{3.28}$$

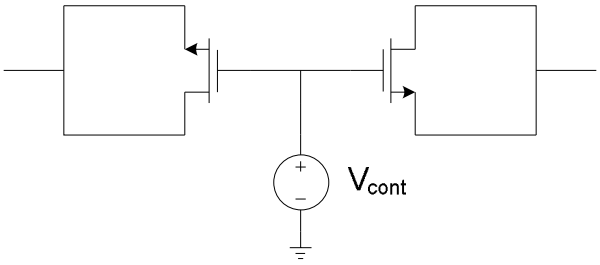


Figure 3.27 MOS varactor implemented in the VCO in this work

In this work, the two MOS varactors are designed in series to provide sufficient capacitance range to vary the operating frequency around 2.4GHz (Figure 3.27). The gate voltage is varied from 0V to 5V by a DC voltage source V_{cont}. The maximum capacitance C_{max} occurs at 5V, when the depletion region is at its thinnest width, causing C_{dep} to be very high and C_g to be the dominant capacitance (since they are in series). The transistor is chosen to give f_{min} equal to 2.2GHz, requiring C_g to be 3.5pF.

$$C_g = 2 \times W_{eff} \times L_{eff} \times C_{ox} \Rightarrow W_{eff} = \frac{C_g}{2 \times L_{eff} \times C_{ox}} \tag{3.29}$$

with L_{eff} chosen as 0.8µm and C_{ox} is 4.4fF/µm^2 for TSMC 0.35µm technology, the required W_{eff} is calculated as 500µm. Due to unaccounted series parasitic capacitances, C_g reduced to 3.1pF from simulations, and the W_{eff} is increased to 600µm to obtain the required C_g of 3.5pF. The following table shows C_{max} and C_{min} obtained from the varactor simulation.

Table 3.7 Minimum and Maximum capacitance of Varactor

	V_{cont}	Capacitance	Expected Frequency
C_{min}	0V	1.16pF	3.8 GHz
C_{max}	5V	3.5pF	2.21 GHz

3.3.1.3 Buffer design

Prior to designing the cross-coupled NMOS transistors and tail current source of the Core VCO, the required output peak to peak voltage is needed. This is decided by the value of the buffer gain. Hence, the buffer (source follower is designed first. The buffer needs to drive a 50Ω load and obtain an output voltage swing of greater than 1V, and required current is 20mA. So the driving transistor M1 in figure 3.28 is calculated to be 135µm for drain current of 30mA (targeting a voltage swing of 1.5V).

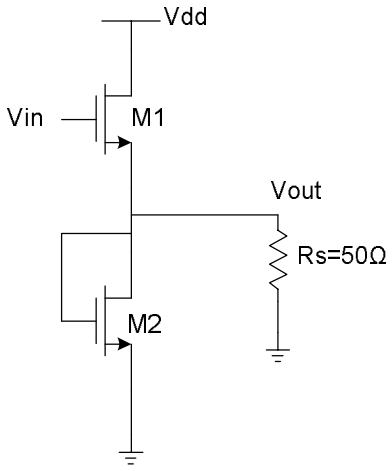


Figure 3.28 Source follower buffer

The diode-connected load of the source follower is designed for very high resistance to direct most of the current to the 50Ω load. Therefore, the diode-connected NMOS transistor M2 size is kept very small. The transistor size values are tweaked to give optimum gain and output voltage swing.

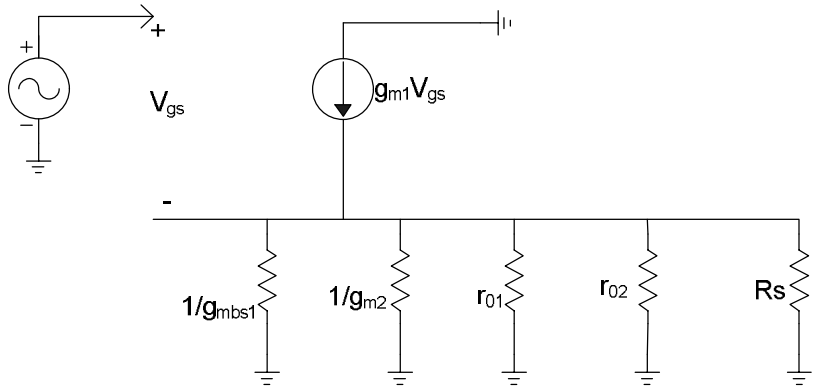


Figure 3.29 Small signal equivalent circuit of the source-follower

From the small signal model of the source follower, the gain of the buffer is calculated using:

$$Av = \frac{\dfrac{1}{g_{mbs1}} \left\| \dfrac{1}{g_{m2}} \right\| r_{01} \| r_{02} \| Rs}{\dfrac{1}{g_{m1}} + \dfrac{1}{g_{mbs1}} \left\| \dfrac{1}{g_{m2}} \right\| r_{01} \| r_{02} \| Rs} \tag{3.30}$$

With the transistor sizes M1 as 200µm, M2 as 2µm and R_s equal to 50Ω and simulated drain current of 28.8mA, the buffer gain is calculated to be 0.63.

3.3.1.4 Cross-coupled transistor and current source design

In section 3.3.1.3, the buffer gain is estimated to be 0.63. For a 2V output voltage swing for the buffer, the required input voltage swing is 3.2V. From S-parameter simulation of the LC resonator tank, the parallel resistance R_p of the tank is plotted in Figure 3.30.

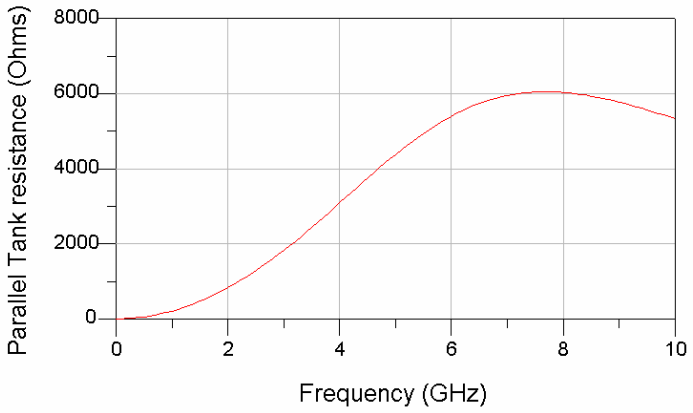


Figure 3.30 parallel resistance of resonant tank vs frequency

At the highest expected operating frequency of 2.9 GHz, the R_p is 1.6 kΩ. Targeting the output swing of the LC VCO to be 4V, the required current is calculated to be:

$$Vpp = \frac{2}{\pi} IssRp \Rightarrow Iss = \frac{Vpp}{\frac{2}{\pi} Rp} = 4.1mA \tag{3.31}$$

The current source and current mirror are designed to supply a total current of 8mA to the two branches of the LC VCO. The transistor sizes of the cross coupled transistors, is estimated from the oscillation start-up criteria [38] given by equation 3.32.

$$g_m \geq \frac{1}{Rp} \tag{3.32}$$

The transistor size is fixed to 150μm to satisfy this criterion.

3.3.2 Simulation Results

The designed voltage controlled oscillator (VCO) is simulated in Agilent's Advance Design System (ADS). TSMC 0.35 μm CMOS process models are used for simulation. For the RF-MEMS inductors the extracted model provided by University of Texas at Dallas Micro/Nano devices and systems (Minds) group. The planar monolithic inductors were designed in ADS Layout and extracted as a component to be used in the ADS schematic simulator.

3.3.2.1 VCO with RF MEMS inductor

Figure 3.31 and 3.32 show the power spectral density and transient output of the VCO with RF MEMS inductor with the DC control voltage V_{cont} at the gates of the MOS varactor at 5V. The oscillating frequency is 2.2 GHz and output swing is 1.8V.

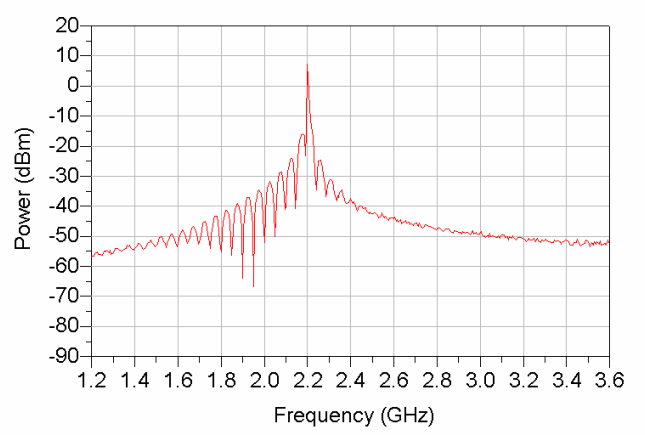


Figure 3.31 Power spectral density of VCO with RF MEMS inductor (Vcont=5V)

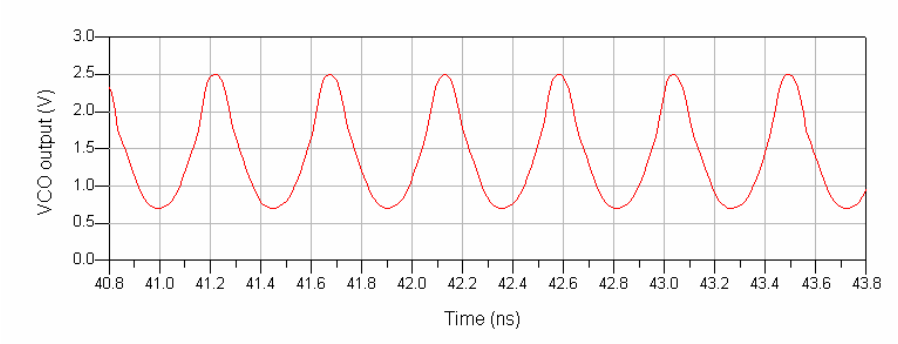


Figure 3.32 Transient output of VCO with RF MEMS inductor (Vcont=5V)

Figure 3.33 and 3.34 show the power spectral density and transient output of the VCO with RF MEMS inductor with the DC control voltage V_{cont} at the gates of the MOS varactor at 0V. The oscillating frequency is 2.94 GHz and output swing is 2.1V.

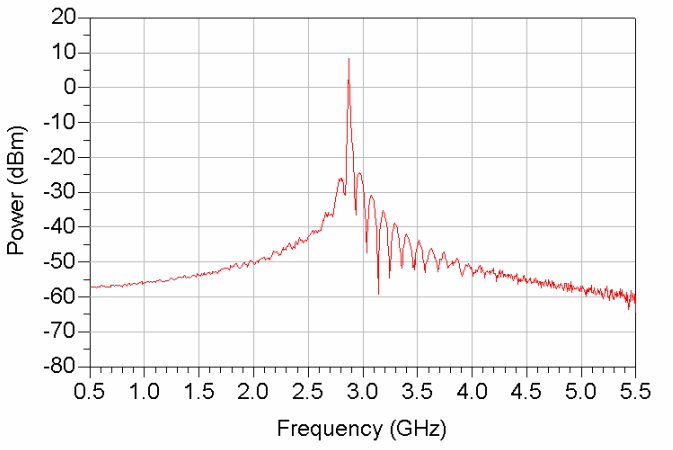


Figure 3.33 Power spectral density of VCO with RF MEMS inductor (Vcont=0V)

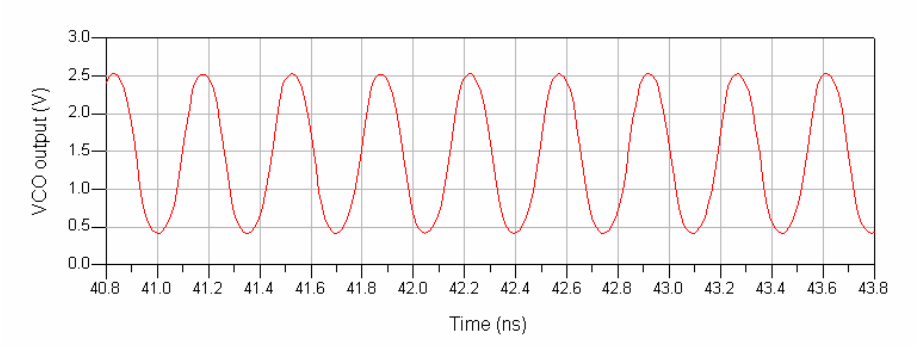


Figure 3.34 Transient output of VCO with RF MEMS inductor (Vcont=0V)

Table3.8 Tuning range of VCO with RF MEMS inductor

V_{cont}	0V	5V	Range
Frequency	2.94 GHz	2.2 GHz	740 MHz
Output swing	2.1 V	1.8 V	0.3 V

3.3.2.1 VCO with planar monolithic inductor

Figure 3.35 and 3.36 show the power spectral density and transient output of the VCO with planar monolithic inductor with the DC control voltage V_{cont} at the gates of the MOS varactor at 5V. The oscillating frequency is 2.53 GHz and output swing is 0.69 V.

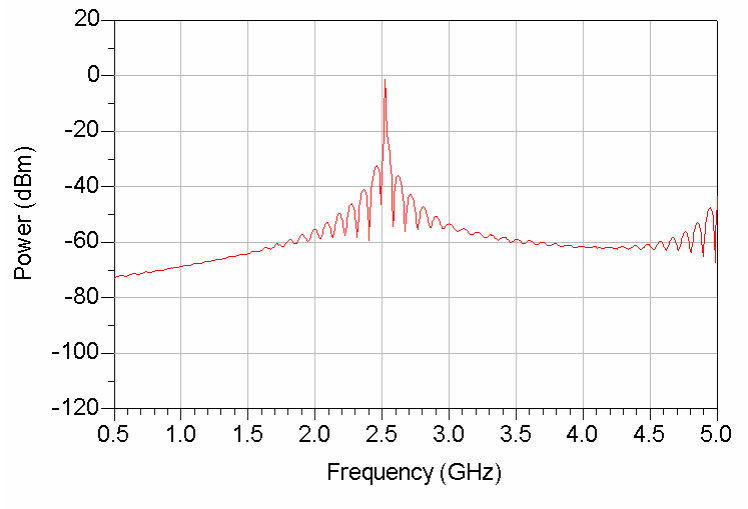


Figure 3.35 Power spectral density of VCO with RF MEMS inductor (Vcont=5V)

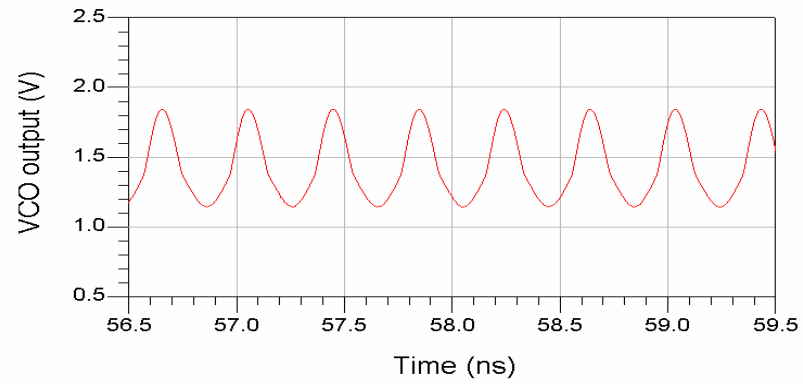


Figure 3.36 Transient output of VCO with RF MEMS inductor (Vcont=5V)

Figure 3.37 and 3.38 show the power spectral density and transient output of the VCO with planar monolithic inductor with the DC control voltage V_{cont} at the gates of the MOS varactor at 0V. The oscillating frequency is 3.03 GHz and output swing is 0.95 V.

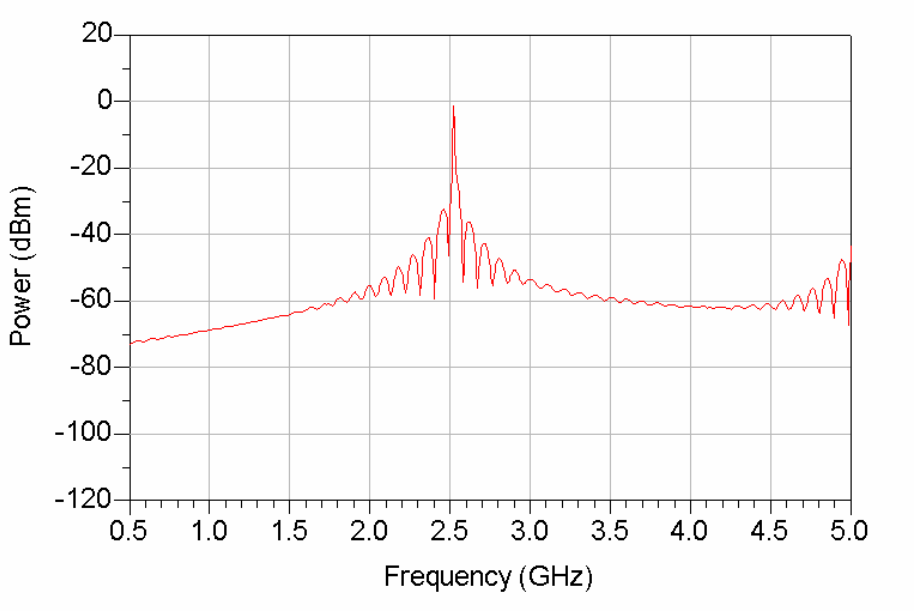


Figure 3.37 Power spectral density of VCO with RF MEMS inductor (Vcont=0V)

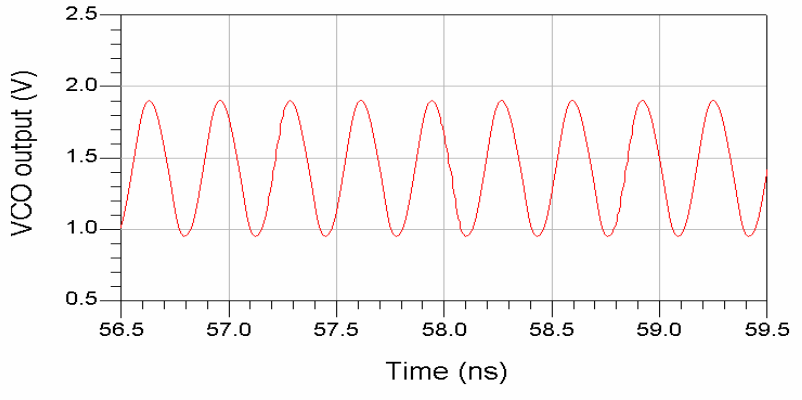


Figure 3.38 Transient output of VCO with RF MEMS inductor (Vcont=0V)

Table 3.9 Tuning range of VCO with planar monolithic inductors

V_{cont}	0V	5V	Range
Frequency	3.03 GHz	2.53 GHz	500 MHz
Output swing	0.95 V	0.69 V	0.26 V

Table 3.10 shows comparison of VCO designed with RF MEMS inductors in this work and recent 2.4GHz VCOs.

Table 3.10 Performance comparison with recent VCOs

Ref. No.	Output Voltage swing (V)	Tuning range	Power	CMOS (Tech)
[39]	1.8V	175MHz	2.2mW	0.18µm
[40]	1.8	40MHz	4.6mW	0.18µm
[41]	n/a	300MHz	52mW	0.25µm
[42]	n/a	274MHz	18mW	0.25µm
This work	1.95	740MHz	52mW	0.35µm

3.3.3 Layout and Chip photo

The layout of the VCO was done using Cadence. Figure 3.39 shows the layout of the VCO. The two empty squares with open pads were provided for post-integration of the RF MEMS inductors.

A scanning electron microscopy (SEM) microphotograph of the VCO with the post-IC integrated RF MEMS inductors is shown in Figure 3.40.

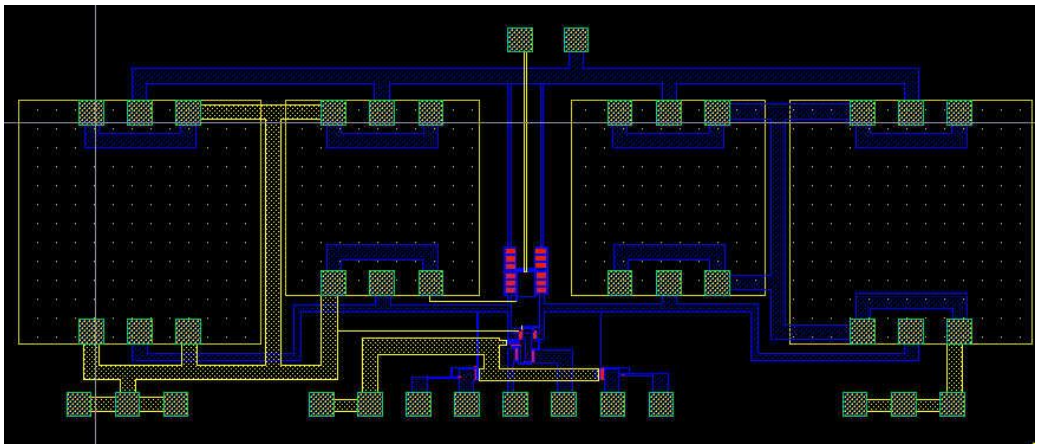


Figure 3.39 Layout of VCO

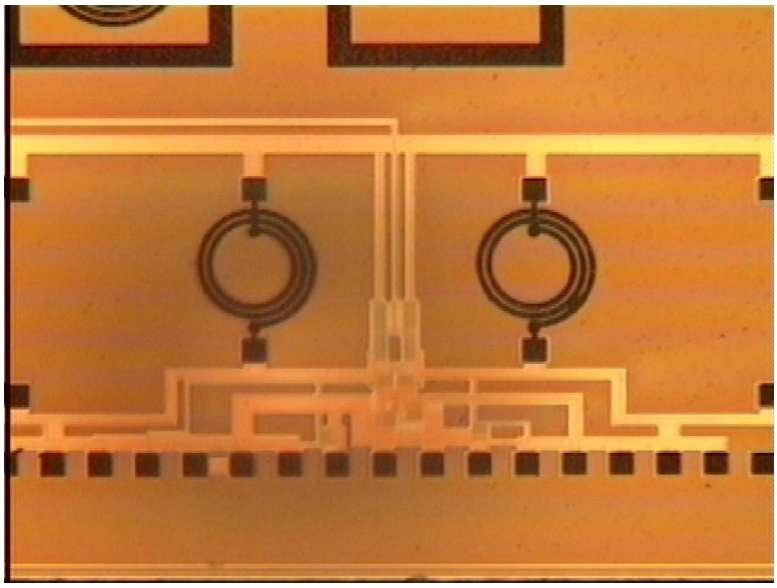


Figure 3.40 SEM microphotograph of the VCO after post-integration of micro-machined RF MEMS Inductors

CHAPTER 4

CONCLUSION

A narrow-band 2.4 GHz low noise amplifier and a 740MHz wideband voltage control oscillator with center frequency at 2.4 GHz have been designed. The circuit performance targets Bluetooth and Wifi standards. The circuits have been designed and simulated with both micro-machined MEMS inductors and planar monolithic inductors. The output parameters show a clear indication of the superior performance of high-Q RF MEMS inductors over that of relatively low-Q planar monolithic inductors. The low noise amplifier with RF MEMS inductors achieves a power gain of 10dB and noise figure of 0.8dB, compared to a power gain of 6.34dB and noise figure of 2.92dB with planar monolithic inductors.

The voltage controlled oscillator with RF MEMS inductors achieves a wider bandwidth of 740 MHz compared to that of planar monolithic inductors which achieve 500MHz. The reason for smaller tuning range is due to parasitic capacitances limiting the varactors C_{max}/C_{min} ratio. The RF MEMS inductors are air-suspended and hence have very less substrate parasitic capacitance, giving a broader tuning range. The output swing of VCO with RF MEMS inductor is 2.1~1.8V which is more than twice of that with VCO with planar monolithic inductors which has output wing of 0.9~0.6V. This is

due to high-Q of the entire parallel resonant tank containing RF MEMS inductors, giving it a large parallel resistance value and hence a larger output swing.

In this work, it is proven that RF-MEMS inductors are important and feasible for high frequency circuits with their high-Q, and give considerable increase in performance as compared to monolithic inductors.

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BIOGRAPHICAL INFORMATION

Varun K Shenoy graduated from Manipal Institute of Technology, India with his Bachelor's degree in Electrical and Electronics engineering. During his bachelor's he actively participated in activities of the IEEE student branch of his university. He developed an 'Online Voltage Event Recorder', a PC data acquisition and analyses system for monitoring of supply voltages for domestic appliances, as his undergraduate project. He is currently pursuing his Master's thesis degree under Dr. Sungyong Jung at University of Texas at Arlington. He joined Analog/Mixed-signal Integrated Circuit design lab in September, 2005. His research interests include analog and mixed-signal integrated circuit design and digital signal processing.