DISTRIBUTED MODEL FOR THERMAL CHARACTERISATION
OF OXIDE ISOLATED SILICON GERMANIUM
HETEROJUNCTION BIPOLAR
TRANSISTORS

by

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ABSTRACT

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The University of Texas at Arlington, 2011

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Demand for high-speed and cost-effective devices has resulted in the development of smaller, high frequency devices. Since semiconductor devices are getting smaller, self-heating effects have become more important. Self-heating increases the temperature of the devices and results in variations in the electrical properties of the circuit in which these devices are used. Hence, it is important to accurately characterize the self-heating effects and develop reliable models, so that these effects can be taken into consideration in the simulations during the design process. This work deals with the development of the Vertical Bipolar Inter-Company (VBIC) model parameters to characterize self-heating in SOI SiGe transistors which have been fabricated by National Semiconductors (NSC). The distributed nature of thermal impedance of the wafer has been studied. The dependence of thermal resistance on the power dissipation has also been verified by DC characterization results. The time domain, DC and frequency domain measurements provide similar results for thermal resistance. The thermal resistance varies from 2400 K/W to 4700 K/W for a 0.25x20 μm^2 device manufactured by NSC.

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CHAPTER 1

SILICON GERMANIUM HETEROJUNCTION BIPOLAR TRANSISTORS

Hetero-junction bipolar transistors (HBTs) are used in wired and wireless communication systems, optical fiber communications, disk storages, high speed high bandwidth instrumentation, etc. These devices have been produced with values of f_T nearing 240 GHz, f_{max} nearing 330 GHz and extremely low noise figure [1]. HBTs are also being used in microwave power amplifiers. HBT technology is a vehicle for high efficiency, high-gain, high-power density microwave power amplifiers [2]. Silicon Germanium (SiGe) HBTs have generally been integrated with Metal Oxide Semiconductor (MOS) transistors in Bipolar Complementary MOS (BiCMOS) technology. Radio Frequency (RF) circuits are designed with HBTs and digital CMOS circuits are designed with the MOS transistors. Hence, BiCMOS technologies incorporating SiGe HBTs are useful for producing RF systems on a single chip [1].

1.1 Hetero-junction Bipolar Transistors

Hetero-junction bipolar transistors (HBTs) are different from the normal bipolar junction transistors (BJTs) with respect to the presence of hetero-structure at the base-emitter junction. An HBT is formed by replacing the homo-junction emitter by a large energy-gap material. This enables the design freedom of independently optimizing the current gain β and the doping levels in the base and emitter regions. For most applications, high base doping and low emitter doping are preferred, whereas in a normal BJT, high current gain requires the emitter doping to be higher than base doping. High emitter-doping results in a higher base-emitter junction capacitance. Figure 1.1 illustrates the energy band diagram of an NPN HBT with an abrupt junction. The energy gap difference in base-emitter hetero-junction of a HBT causes holes from the base to experience a much higher energy barrier than the holes from the emitter.

With a voltage, V_{BE}, applied to the base-emitter junction, the electron injection from emitter to base is favored over the injection of holes from base to emitter. The difference in electron and hole-barriers is shown as ΔE_v in Figure 1.1. ΔE_v is the discontinuity in valence band [3]. The current gain in an HBT is given by [3]

$$\frac{I_{\mathrm{C}}}{I_{\mathrm{B,back-inject}}} = \frac{X_{\mathrm{emit}}}{X_{\mathrm{base}}} \frac{\mathrm{D}_{\mathrm{n,base}}}{\mathrm{D}_{\mathrm{p,emit}}} \cdot \frac{N_{\mathrm{emit}}}{N_{\mathrm{base}}} \cdot \exp\left(\frac{\Delta E_v}{kT}\right) \quad (1.1)$$

where $I_{B,back\text{-}inject}$ is the base current, I_C is the collector current, X_{emit} and X_{base} are the thickness of emitter and base regions respectively, $D_{n,base}$ and $D_{p,emit}$ are the diffusion coefficients in the base and emitter regions respectively, N_{emit} is the emitter doping, N_{base} is the base doping, ΔE_v is the valence band discontinuity and k is the Boltzmann constant [3].

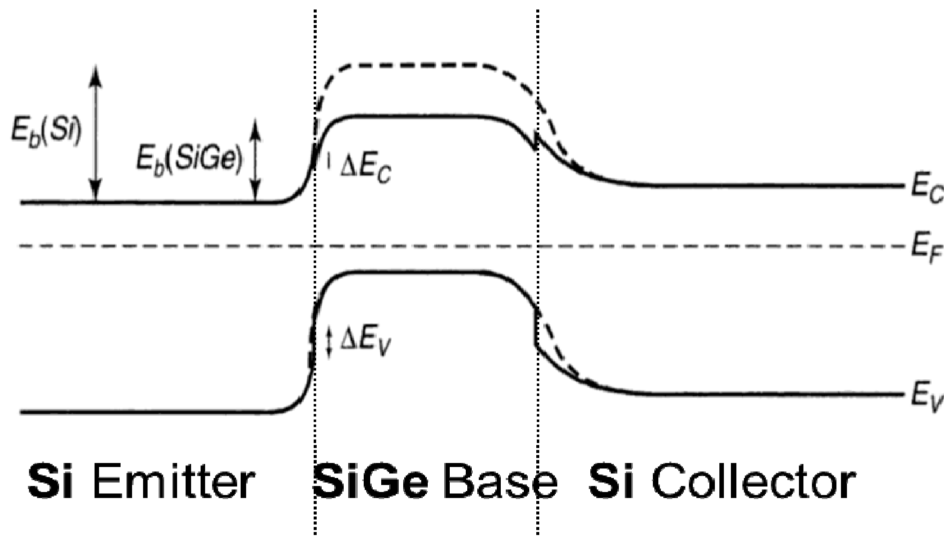


Figure 1.1 Band diagram of NPN abrupt hetero-junction bipolar transistor [3]

1.2 CBC8 Process for High-Performance Analog and RF IC Design

The CBC8 process is a 0.25 μm complementary-SiGe BiCMOS technology, developed at National Semiconductors for high speed analog and RFIC applications. A SiGe HBT is produced by sandwiching a SiGe base between a Si collector and a Si emitter [1]. For RF and low power applications, f_T of the transistors has to be improved. Silicon on insulator (SOI)

technology, integrated deep trench and shallow trench isolation offer full dielectric isolation capability. Table 1.1 highlights the important performance metrics of the technology.

Table 1.1 Typical CBiCMOS device characteristics

Device	**Parameter**	**Unit**	**LV NPN**	**HV NPN**	**HV PNP**	
SiGe HBT	AE	μm^2	0.25x1	0.25x1	0.25x1	
	β_{DC}		300	300	300	
	V_A	V	200	250	85	
	f_T @ 1.5 V	GHz	57	34	38	
	f_{max} @ 1.5 V	GHz	95	85	80	
	NF_{min} @ 2 GHz	dB	0.7	0.7	0.8	
	BVCEO	V	3.0	5.2	5.2	
	BVCBO	V	12	19	11	
	1/*f* noise – Sib @ 1Hz	A^2/Hz	5e-21	6e-21	1.5e-20	
CMOS			**LV NMOS**	**HV NMOS**	**LV PMOS**	**HV PMOS**
	W/L		5/0.24	5/0.4	5/0.24	5/0.4
	VDD	V	2.5	3.3	2.5	3.3
	V_T	V	0.60	0.70	0.65	0.70
	ID_{SAT}	µA/µm	570	500	290	260
	Off Current <	pA/µm	1.0	1.0	1.0	1.0
	f_T @ VDD/2	GHz	28	17	13	8
	f_T @ VDD	GHz	30	18	17.5	10

1.2.1 Structure of SiGe NPN HBT

A Scanning Electron Microscope (SEM) cross-section of a CBC8 SiGe HBT with a single base, emitter and collector (BEC) configuration is shown in figure 1.2. The figure highlights the full dielectric isolation with a vertical deep trench (DT) intercepting the buried oxide (BOX) and a shallow trench isolation (STI) region.

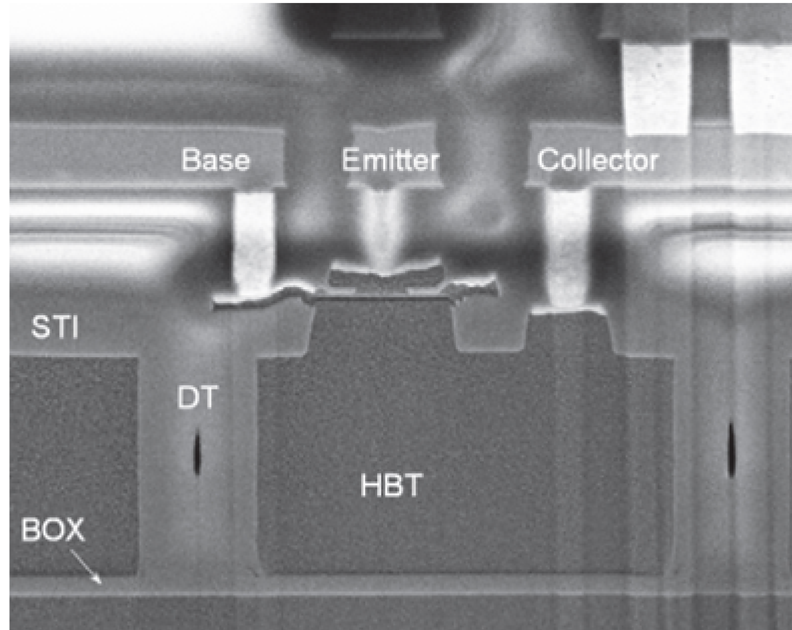


Figure 1.2 SEM cross-section showing a HBT with STI isolation on SOI [4].

In this work, the SiGe HBT devices manufactured with the CBC8 process have been used for thermal characterization.

1.3 Self-heating in SiGe NPN HBT

1.3.1 Self-heating of a transistor

Self-heating is caused by power dissipation in the p-n junctions of the device which results in an increase in junction temperature of the device. Self-heating of a transistor is characterized by its thermal resistance and thermal capacitance. Self-heating can be modeled conceptually as illustrated in figure 1.3. A thermal network is included with the electrical model of the device. The thermal network is driven by the power dissipated in the device. The

dissipated power is calculated by adding the individual powers of the non-storage branches of the electrical network.

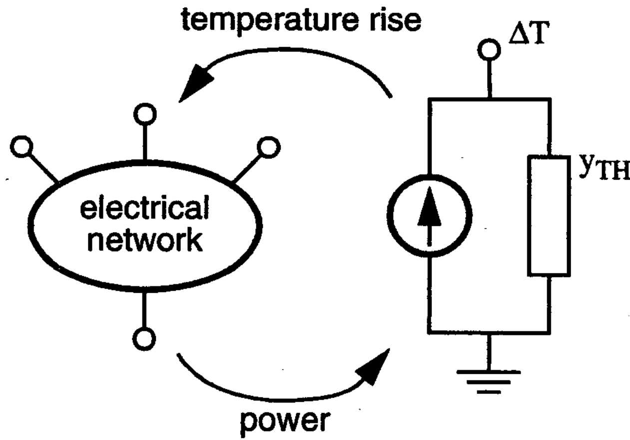


Figure 1.3 Modeling of self-heating [5]

The local temperature rise, ΔT, from the thermal network is coupled back to the constitutive elements of the electrical network [5]. In an HBT, heat dissipation occurs mainly in the collector-base depletion region that carries the bulk of the injected current. In this region, carriers attain high velocities and give up their energy to the lattice through phonon interactions [6]. The Self-heating effect is included in the Vertical Bipolar Inter-company (VBIC) model for the HBT. This is one of the major improvements of the VBIC model over the Simulation Program with Integrated Circuit Emphasis (SPICE) Gummel Poon (SGP) model. At high frequencies, the device thermal response cannot track the electrical variations, so that the output conductance $1/r_o$ is equal to the intrinsic electrical value. At low frequencies, the device temperature varies with variations in applied signal and the output conductance is different from the intrinsic electrical value. The thermal admittance, Y_{th}, can be characterized by observing the difference between the measured output conductance and the calculated intrinsic electrical conductance [5]. The small signal admittance parameters including the effects of self-heating are given by [5]

$$y_{11}(\mathrm{j}\omega) = g_{\pi} + \frac{g_{\mathrm{bt}}\left(I_{\mathrm{b}} + g_{\pi}V_{\mathrm{b}} + g_{\mathrm{m}}V_{\mathrm{c}}\right)}{y_{\mathrm{TH}} - \left(g_{\mathrm{ct}}V_{\mathrm{c}} + g_{\mathrm{bt}}V_{\mathrm{b}}\right)} + \mathrm{j}\omega\left(C_{\mathrm{be}} + C_{\mathrm{bc}}\right) \tag{1.2}$$

$$y_{12}(\mathrm{j}\omega)=\frac{g_{\mathrm{bt}}\left(I_{\mathrm{c}}+g_{\mathrm{o}}V_{\mathrm{c}}\right)}{y_{\mathrm{TH}}-\left(g_{\mathrm{ct}}V_{\mathrm{c}}+g_{\mathrm{bt}}V_{\mathrm{b}}\right)}-\mathrm{j}\omega C_{\mathrm{bc}} \tag{1.3}$$

$$y_{21}(\mathrm{j}\omega)=g_{m}+\frac{g_{\mathrm{ct}}\left(I_{\mathrm{b}}+g_{\pi}V_{\mathrm{b}}+g_{\mathrm{m}}V_{\mathrm{c}}\right)}{y_{\mathrm{TH}}-\left(g_{\mathrm{ct}}V_{\mathrm{c}}+g_{\mathrm{bt}}V_{\mathrm{b}}\right)}-\mathrm{j}\omega C_{\mathrm{bc}} \tag{1.4}$$

$$y_{22}(\mathrm{j}\omega)=g_{\mathrm{o}}+\frac{g_{\mathrm{ct}}\left(I_{\mathrm{c}}+g_{\mathrm{c}}V_{\mathrm{c}}\right)}{y_{\mathrm{TH}}-\left(g_{\mathrm{ct}}V_{\mathrm{c}}+g_{\mathrm{bt}}V_{\mathrm{b}}\right)}+\mathrm{j}\omega\left(C_{\mathrm{bc}}+C_{\mathrm{cs}}\right) \tag{1.5}$$

where $g_\pi = \partial I_b/\partial V_b$ is the intrinsic electrical input conductance, $g_o = \partial I_c/\partial V_c$ is the intrinsic electrical output conductance, $g_m = \partial I_c/\partial V_b - g_o$ is the intrinsic electrical transconductance, $g_{bt} = \partial I_b/\partial \Delta T$ and $g_{ct} = \partial I_c/\partial \Delta T$ are the thermal transconductances [5].

1.3.2 VBIC model of a transistor

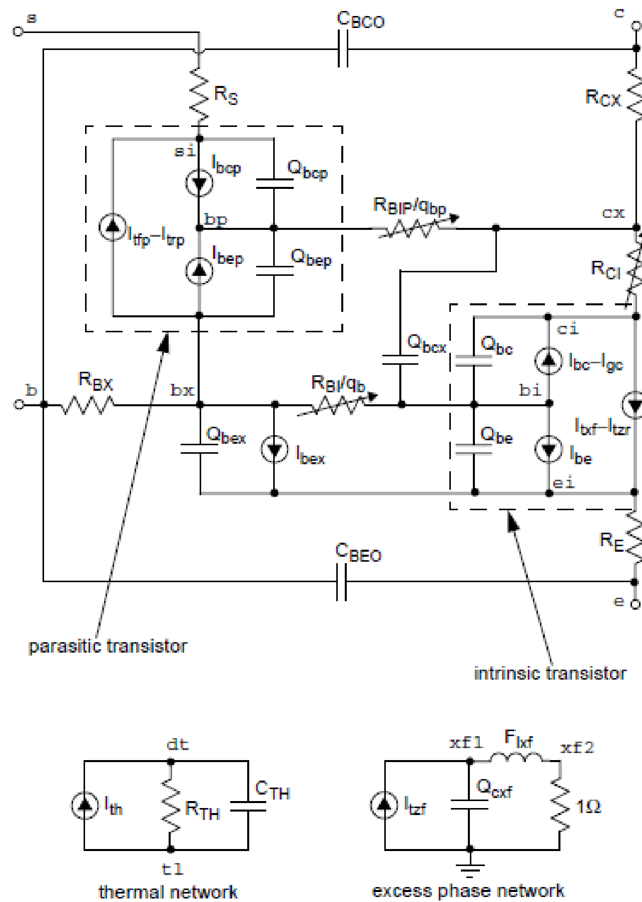


Figure 1.4 VBIC equivalent circuit [7]

The VBIC model is a public domain model for the BJT/HBT. Some of the improvements of VBIC model compared to SGP model are listed below [8]:

- improved Early effect modeling
- quasi-saturation modeling
- parasitic substrate transistor modeling
- parasitic fixed (oxide) capacitance modeling
- avalanche multiplication modeling
- improved temperature dependence modeling
- decoupling of base and collector currents
- electrothermal (self-heating) modeling
- improved heterojunction bipolar transistor (HBT) modeling.

The VBIC equivalent network of a transistor is shown in figure 1.4. The parameters which model the self-heating are R_{TH} and C_{TH}. IS is the VBIC parameter for transport saturation current [7]. At normal operating temperatures the parameters R_{TH}, C_{TH} and IS play a significant role and the temperature dependence of other parameters can be neglected [9].

1.3.3 Thermal impedance components of SiGe NPN HBT

Shown in figure 1.5 are the three significant regions of the device which are responsible for thermal impedance viz., the Si tub, buried oxide and Si wafer. The Si tub is the region extending from the collector-base junction to the oxide as shown in figure 1.5. As shown in figure 1.5, buried oxide is the region made of silicon dioxide and located below the tub. As shown in figure 1.5, the wafer is the region located below the oxide. Heat source is located at the collector-base junction with an area equal to emitter area. A 3-pole network is connected to the dT node present in the VBIC model of a HBT to include the effect of thermal impedance in simulations. The theoretical models to calculate the thermal impedance is discussed in chapter 2.

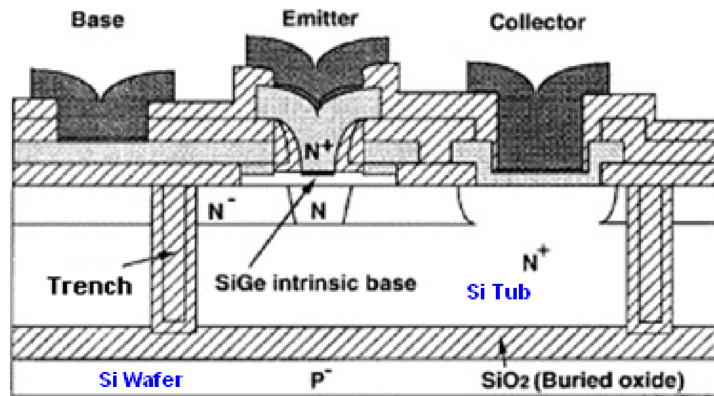


Figure 1.5 Structure of SOI SiGe HBT

1.3.3.1 Electrical network representing the thermal impedance of SiGe HBT

The analogies between electrical and thermal domain are listed in Table 1.3. Temperature in the thermal domain is analogous to voltage in the electrical domain; time rate of heat flow in the thermal domain is analogous to current flow in the electrical domain and ambient temperature in the thermal domain is analogous to ground in the electrical domain.

Table 1.3 Thermal and Electrical Analogy

Thermal		Electrical	
Temperature	T in Kelvin	Voltage	V in volt
Heat flow	P in W	Current	I in Amp
Thermal Resistance	R_{th} in K/W	Resistance	R in ohm
Thermal capacitance	C_{th} in J/K	Capacitance	C in Farad
Ambient Temperature	Kelvin (K)	Ground	Volt (V)

As shown in figure 1.6 (a), the analogy between the resistances in the thermal domain and the electrical domain is illustrated by a block of solid whose top and bottom surfaces are maintained at temperatures T_1 and T_2 respectively. The thermal resistance of the solid is given by:

$$R_{th} = \frac{T_1 - T_2}{P} \tag{1.5}$$

where P is the power flowing from the top surface to the bottom surface.

The equivalent electrical network for the block is shown in figure 1.6 (b). The heat energy stored in the thermal capacitances is calculated as shown below:

$$\begin{aligned} Q_{\text{h}} &= \left(T_1 - T_{\text{ambient}}\right)\frac{C_{\text{th}}}{2} + \left(T_2 - T_{\text{ambient}}\right)\frac{C_{\text{th}}}{2} \\ &= \left(T_{\text{avg}} - T_{\text{ambient}}\right)C_{\text{th}} \end{aligned} \tag{1.7}$$

where $T_{avg}=(T_1+T_2)/2$ is the average temperature of the solid and $T_{ambient}$ is the ambient temperature.

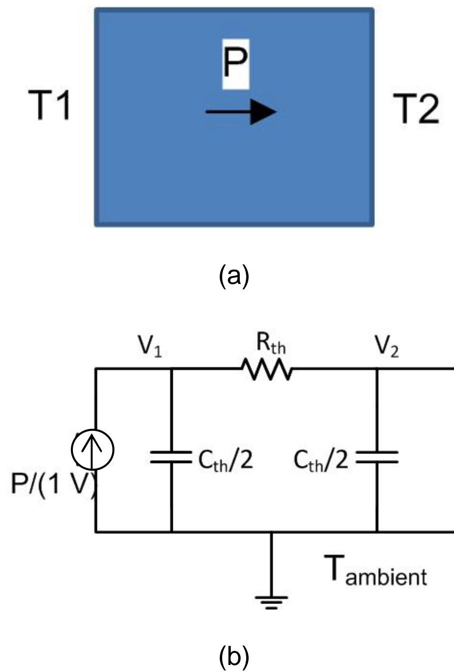


Figure 1.6 Illustration of thermal resistance (a) A block of solid (b) Equivalent electrical network

Thermal impedance of SiGe HBT can be represented using two kinds of 3-pole networks; the Cauer network and the Foster network. The Cauer network physically represents the thermal impedance of a system with the capacitances connected to ground [10]. Each section is similar to the illustration in figure 1.6. The Cauer network representing the thermal

impedance of a SiGe HBT is shown in figure 1.7. The thermal resistance and the thermal capacitance of each section – tub (R_{tub}, C_{tub}), oxide (R_{ox}, C_{ox}) and wafer (R_w, C_w) are shown in the figure. The ambient temperature is analogous to the electrical ground potential. Other analogies between electrical and thermal quantities are listed in Table 1.3. The equivalent Foster network can be calculated for a given Cauer network. Each RC product of a Foster network represents the poles of the network. A 3-pole Foster network is illustrated in Figure 1.8. Spreadsheets have been developed to calculate equivalent 3-pole Foster network from a 3-pole Cauer network and vice versa and are explained in appendix C.

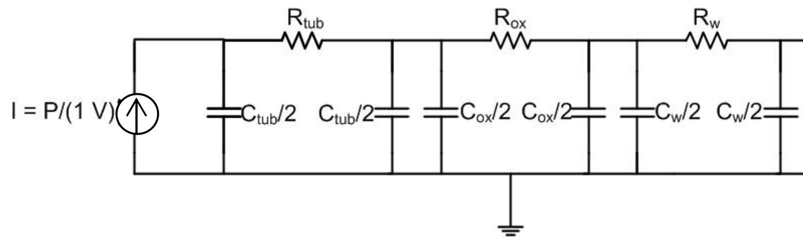


Figure 1.7 Three pole Cauer network representing thermal impedance of HBT

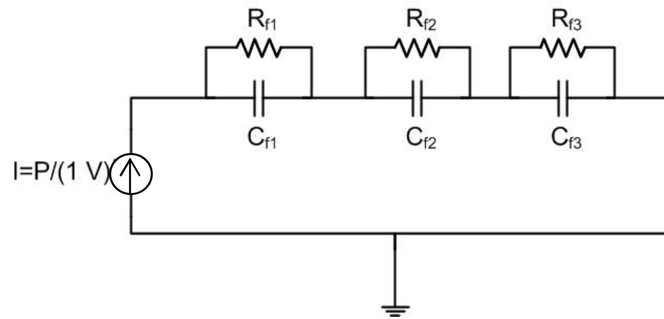


Figure 1.8 Three pole Foster network representing thermal impedance of HBT

CHAPTER 2

THERMAL IMPEDANCE CALCULATIONS

2.1 Introduction

The important contributions for thermal impedance can be attributed to three sections of the HBT as explained in section 1.3.3.1. The structure of a SiGe HBT is repeated in figure 2.1 for convenience. The methods used to calculate the thermal impedance contributions from each section are explained in this section.

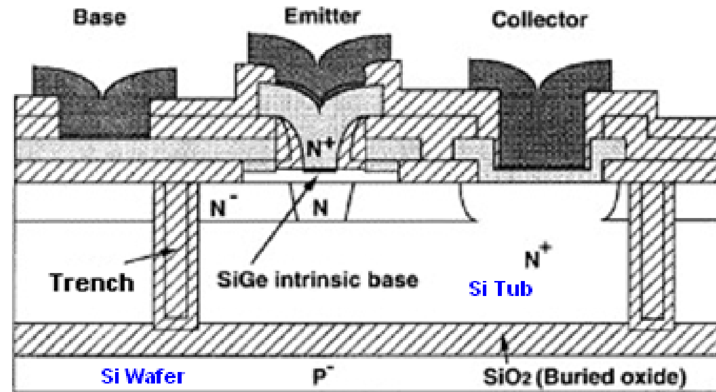


Figure 2.1 Structure of SiGe HBT

2.2 Thermal Impedance calculation of Si tub and buried oxide

The variable angle model extended to multiple layers has been used for thermal characterization of the Si tub and the buried oxide as explained in [10]. The thermal impedance of each section can be represented by lumped R_{th} and C_{th} elements. Thermal resistance is calculated using the volume sketched in figure 2.2. The heat source and its projection on the next layer boundary determine this volume. The angles α_1, β_1, α_2 and β_2 of the truncated prism are in the range of 25 to 45 degree for the Si tub and approximately equal to 0 degrees for the buried oxide. In this work, the offset in the position of the heat source at the top surface is ignored.

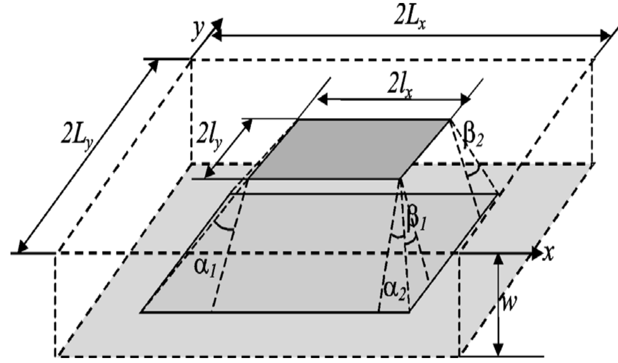


Figure 2.2. Volume considered to calculate thermal resistance [10]

In [10], the thermal resistance was shown to be equal to

$$R_{th} = \frac{1}{4kl_x} \frac{1}{\left(\gamma_e \tan\alpha - \tan\beta\right)} \ln\left(\frac{l_x + w\tan\alpha}{l_x + w\tan\beta/\gamma_e}\right) \tag{2.1}$$

where $\gamma_e = l_y / l_x$ and $\gamma_s = L_y / L_x$ are the aspect ratios of the heating element and substrate respectively. The spreading angles are given by

$$\begin{aligned}
(\tan\alpha)_i &= \frac{(\tan\alpha_1 + \tan\alpha_2)_i}{2} \\
&= \left(1 + \frac{1-\rho_L}{1+\rho_L}\frac{l_{xn}}{\varepsilon_x^2}\right)\frac{w_n + [\rho_S/(1+\rho_S)]l_{xn}}{w_n + [1/(1+\rho_S)]l_{xn}}\Bigg|_i \\
(\tan\beta)_i &= \frac{(\tan\beta_1 + \tan\beta_2)_i}{2} \\
&= \left(1 + \frac{1-\rho_L}{1+\rho_L}\frac{l_{xn}}{\varepsilon_y^2}\frac{\gamma_e}{\gamma_S}\right)\frac{w_n + [\rho_S/(1+\rho_S)]l_{xn}\gamma_e}{w_n + [1/(1+\rho_S)]l_{xn}\gamma_e}\Bigg|_i
\end{aligned} \tag{2.2}$$

where i = 1,2; $l_{xn} = l_x/L_x$, $w_n = w/L_x$ are the normalized dimensions. ε_x and ε_y are the eccentricity parameters given by:

$$\varepsilon_x = \frac{\sqrt{L_{x1}L_{x2}}}{L_x}; \qquad \varepsilon_y = \frac{\sqrt{L_{y1}L_{y2}}}{L_y}$$

The boundary dependence comes through ρ_S and ρ_L :

$$\rho_S = \frac{k_i}{k_{i+1}}; \quad \rho_L = \frac{k_i}{k_L}$$

where k_i and k_{i+1} are the thermal conductivities of the present and next layer respectively, and k_L is the thermal conductivity of side walls.

The thermal capacitance calculation is not straight forward because it is difficult to associate a given volume to the heat flow path due to the distributed nature of the problem. Thermal resistance calculated using equation (2.1) utilizes a well-defined volume. The heat flow is confined to this volume and hence their limiting walls are assumed to be adiabatic. Consequently, the same volume considered for the calculation of thermal resistance can also be used for the calculation of thermal capacitance. The volume is given by

$$\begin{aligned} V &= 4\int_0^w (l_x + z\tan\alpha)(l_y + z\tan\beta)\,\mathrm{d}z \\ &= 4\left[l_x l_y w + (l_x \tan\beta + l_y \tan\alpha)\frac{w^2}{2} + \tan\beta\tan\alpha\frac{w^3}{3}\right] \end{aligned} \tag{2.3}$$

Using the above volume, thermal capacitance can be calculated using

$$C_{th} = V\rho c_P \tag{2.4}$$

where ρ is the density of the material (used to convert volume to mass) and c_P is the heat capacity (per unit mass).

With the above formulae for R_{th} and C_{th}, the thermal impedance of the Si-tub and buried oxide of an SOI transistor are calculated. For the Si tub in figure 2.1, the top surface area is equal to the area of the emitter since it is assumed that most of the current in the base flows in an area equal to the emitter area. Heat dissipation at the collector-base junction occurs within this area, and the bottom surface area is equal to the bottom surface area of the Si-tub. The height, w, is equal the effective height of the tub which is the difference between the height of the tub and the depletion thickness. The angles are calculated using the appropriate formulae

given by equation (2.2). Similarly for the buried oxide, the dimensions of the oxide are used for thermal impedance calculations.

2.3 Thermal Impedance calculation of Si wafer

Heat conduction in a wafer is similar to the heat conduction in a semi-infinite solid since the thickness of the wafer is large compared to the thickness of the Si tub and the buried oxide. It is to be noted that the distributed models are more relevant than lumped models for the calculation of wafer thermal impedance. A suitable method to calculate the thermal impedance under such a condition has been explained in [6] by considering the solution of heat dissipation by a point source. In this method the heat dissipation occurs within a specific volume ($L \cdot W \cdot H$) at a depth D below the surface of the semi-infinite medium, as illustrated in figure 2.3.

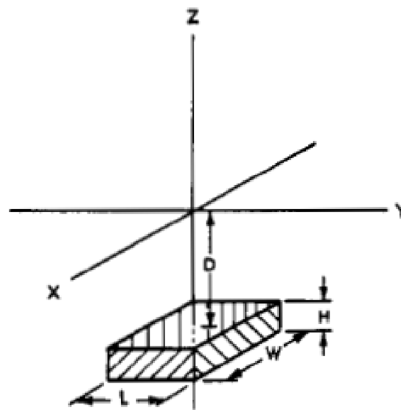


Figure 2.3 Illustration of heat source below the surface of semi-infinite medium [6]

The solution for a semi-infinite medium with an adiabatic surface can be obtained by using the method of imaging i.e. by placing an identical semi-infinite block dissipating the same amount of heat at the same distance D from the adiabatic surface so that there is no effective flow of heat across the surface. The method of images is illustrated in figure 2.4. The two heat sources are mirror images of each other, generating the same amount of heat. It has been shown in [6] that the temperature response as a function of time is given by

$$T(x, y, z, t) = \frac{P}{8C}\int_{0}^{t}\{I_1(u)\cdot I_2(u)\cdot I_3(u)\}\mathrm{d}u \tag{2.5}$$

where

$$I_1(u) = \left[erf\left(\frac{W/2+x}{\sqrt{4ku}}\right) + erf\left(\frac{W/2-x}{\sqrt{4ku}}\right)\right] \tag{2.6}$$

$$I_2(u) = \left[erf\left(\frac{L/2+y}{\sqrt{4ku}}\right) + erf\left(\frac{L/2-y}{\sqrt{4ku}}\right)\right] \tag{2.7}$$

$$I_3(u) = \left[erf\left(\frac{D+H+z}{\sqrt{4ku}}\right) + erf\left(\frac{-D-z}{\sqrt{4ku}}\right) + erf\left(\frac{D+H-z}{\sqrt{4ku}}\right) + erf\left(\frac{-D+z}{\sqrt{4ku}}\right)\right] \tag{2.8}$$

k is the thermal diffusivity of the medium and

$$C = V\rho c_P$$

where ρ is the density of the medium and c_P is the heat capacity (per unit mass). The thermal resistance is calculated by evaluating equation (2.5) as $t \rightarrow \infty$ and is given by

$$R_T(x, y, z) = T(x, y, z, \infty)/P \tag{2.9}$$

where *P* is the power dissipated in the volume.

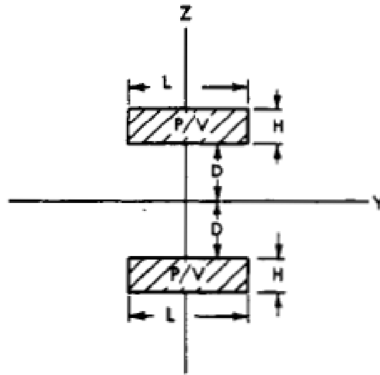


Figure 2.4 Cross-section of heat source and its image [6]

The power dissipation is assumed to be independent of position, i.e., the power is dissipated uniformly throughout the heat sources. For the calculations in equation (2.5), the source of heat is assumed to be at the interface of the buried oxide and the Si-wafer (referring to figure 2.1), and that its thickness is negligible. The detailed calculations for wafer thermal impedance are explained in chapter 3.

CHAPTER 3

DISTRIBUTED MODELS FOR THERMAL IMPEDANCE OF WAFER

Since the dimensions of the wafer region are large compared to other regions of the CBC8 HBT device [4], the lumped element models cannot be used for the calculation of wafer thermal impedance. Since a real world device consists of a continuous distribution of matter, the lumped element models may not be accurate in determining the accurate thermal impedance [11]. The wafer region can be treated as being made up of a large number of hypothetical finite elements having their own R_{th} and C_{th} values as illustrated in figure 3.1 (a). All the C_{th} are connected to thermal ground i.e., the ambient temperature. The equivalent electrical network representation consists of R and C elements connected in a Cauer fashion as shown in Figure 3.1. The thermal response is analogous to the electrical network.

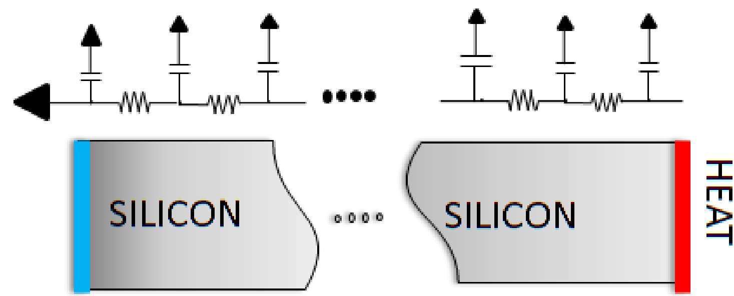
The heat equation governing the heat diffusion in an isotropic medium with no heat sources or sinks is given by

$$\nabla^2 T = \frac{1}{\alpha_P}\frac{\partial T}{\partial t} \tag{3.1}$$

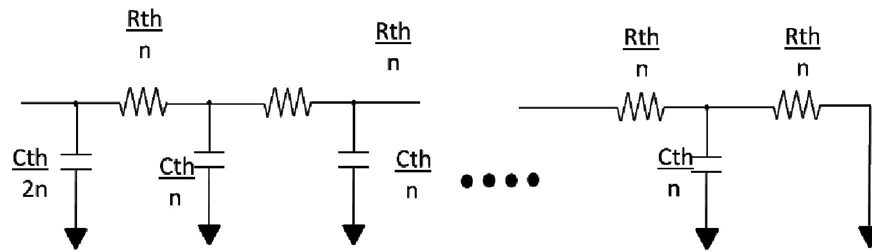
where T is the temperature, α_P is the thermal diffusivity of the material and ∇^2 is the Laplacian operator. In the electrical domain, the corresponding basic equation is the wave equation given by

$$\nabla^2 V = \frac{1}{v^2}\frac{\partial^2 V}{\partial t^2} \tag{3.2}$$

where v is the velocity of the electromagnetic wave and V is the electric potential.



(a)



(b)

Figure 3.1 Distributed model of silicon (a) Silicon being divided into sections (b) Distributed Cauer network representing the thermal impedance of the material

An important difference between the equations (3.1) and (3.2) is that the heat diffusion equation has a dependence on the first derivative with respect to time but the transmission line equation has a dependence on the second derivative with respect to time. This implies that there will be two different reactive (energy storage) elements in the electrical equivalent circuit but only one reactive element in the thermal equivalent circuit. There is a resistance to the flow of heat in a medium which is represented by *thermal resistance* and there is also storage of heat in a medium which is represented by *thermal capacitance*. However, there is no quantity analogous to the magnetic field in the thermal domain. Hence, there is no *thermal inductance* [10].

The circuit in Figure 3.1 (b) is akin to an RC transmission line with resistance per unit length equal to R_{th}/n and capacitance per unit length equal to C_{th}/n. The voltage equation in an RC transmission line is given by [10]

$$\frac{\partial^2 V}{\partial x^2} = R^{'} C^{'} \frac{\partial V}{\partial t} \tag{3.3}$$

where R' is the resistance per unit length and C' is the capacitance per unit length along the transmission line.

The above equation can be generalized in three dimensions. The equation for heat diffusion in a solid is given by [10]

$$\nabla^2 T = R_{th}^{'} C_{th}^{'} \frac{\partial T}{\partial t} \tag{3.4}$$

where R_{th}' is the thermal resistance per unit volume and C_{th}' is the thermal capacitance per unit volume.

A convenient method to determine the distributed model would be to evaluate the thermal response as explained in [6] and fit it to an equivalent distributed thermal network. The equivalent lumped element model can be developed using the principle of conservation of energy which is analogous to the principle of conservation of charge in the electrical domain. The equivalent lumped $R_{th}C_{th}$ network would be that which would store and dissipate the same amount of energy as that stored and dissipated in the distributed network. The electric charge, Q_c, stored in a capacitor is found by integrating the capacitor current $i(t)$ with respect to time t.

$$Q_c = \int i(t)dt \tag{3.5}$$

Similarly, the heat energy, Q_h, stored in a medium is given by integrating the power dissipation $P(t)$ with respect to time t,

$$Q_h = \int P(t)dt \tag{3.6}$$

3.1 Recursive distributed model for the thermal impedance of SiGe HBT

A recursive distributed model for the thermal impedance of a SiGe HBT is explained in [12]. The thermal impedance model based on the physical heat transfer equation results in a compact expression which is a fractional order (1/2 order) system [12]:

$$Z_{\mathrm{TH}}(p)=\frac{R_{\mathrm{TH}}}{\left(1+\sqrt{R_{\mathrm{TH}}C_{\mathrm{TH}}}\sqrt{p}\right)} \tag{3.7}$$

where p is the Laplace variable, R_{TH} and C_{TH} represent the thermal resistance and capacitance respectively.

An upper cutoff frequency, f_u, defined in [12] is given by [12]

$$f_u \approx \frac{1}{2\pi R_0 C_0} \tag{3.8}$$

where R_0, C_0 are the values of the first RC element in the distributed network shown in figure 3.2. The cutoff frequency f_c is dominated by the RC element having the highest capacitance. It follows that [12]

$$f_c \approx \frac{1}{2\pi k^{2n} R_0 C_0} \tag{3.9}$$

where n is the number of RC elements in the network and k is the recursivity co-efficient.

From equations (3.8) and (3.9), the cutoff frequency f_c can be estimated as

$$f_u \approx k^{2n} f_c \tag{3.10}$$

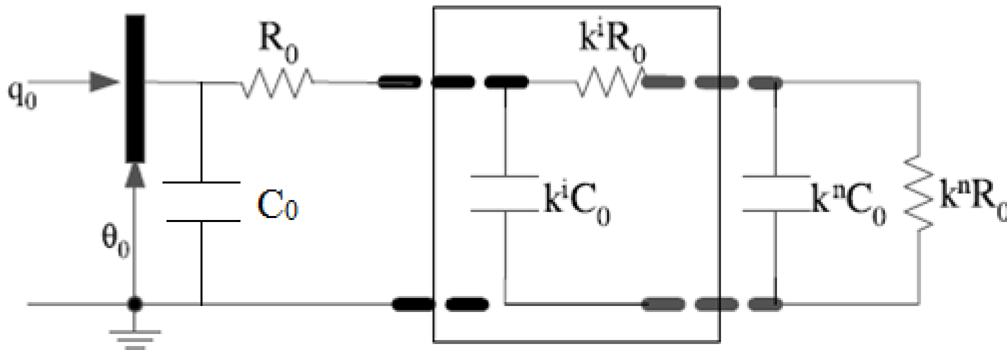


Figure 3.2 A recursive RC network for the thermal impedance. q_0 represents the power flow and θ_0 represents the temperature rise [12].

3.1.1 Finding the optimal values for parameters R_0 and k

The upper cutoff frequency f_u is helpful in establishing a relationship between *n* and *k*. For $f = f_u$, $Z_{TH} = \sqrt{2R_0}$. In the steady state, R_{TH} is given by [12]

$$R_{TH} \approx \frac{R_0\left(1-k^{n+1}\right)}{(1-k)} \tag{3.11}$$

The resistance R_0 can be calculated after fixing f_u. For a given number of cells, corresponding value of recursivity co-efficient *k* can be calculated using (3.11) once the value of R_{TH} is known. The R and C value for the ith stage is calculated recursively by multiplying R_0 and C_0 by k^i. For the calculation of optimal R_0, C_0 and *k* values, equations (3.8) to (3.11) can be used to obtain the initial values. This is followed by fine tuning using optimization schemes [12].

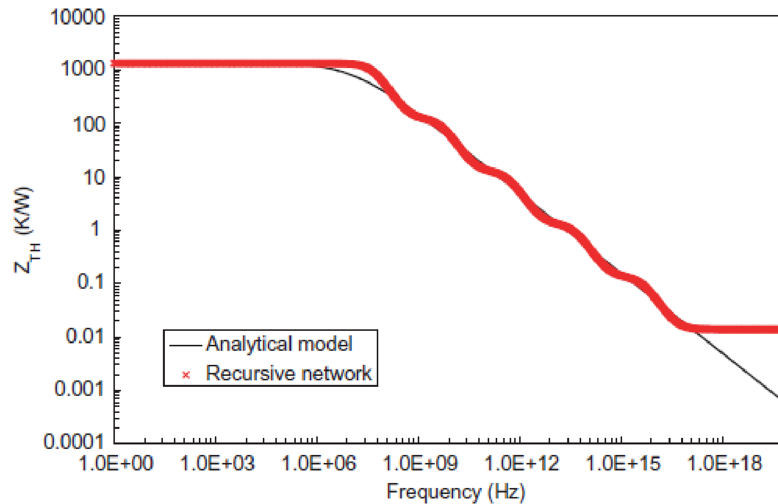


Figure 3.3 Comparison of analytical model and 5-element recursive RC model [12]

The frequency response plot of the analytical model from equation (3.7), and a 5-element recursive RC network are shown in figure 3.3. The time domain measurement result and the transient response using a single RC model and 5-element recursive RC network are shown in figure 3.4. It can be observed that the 5-element recursive RC network provides a better fit compared to the single element model [12].

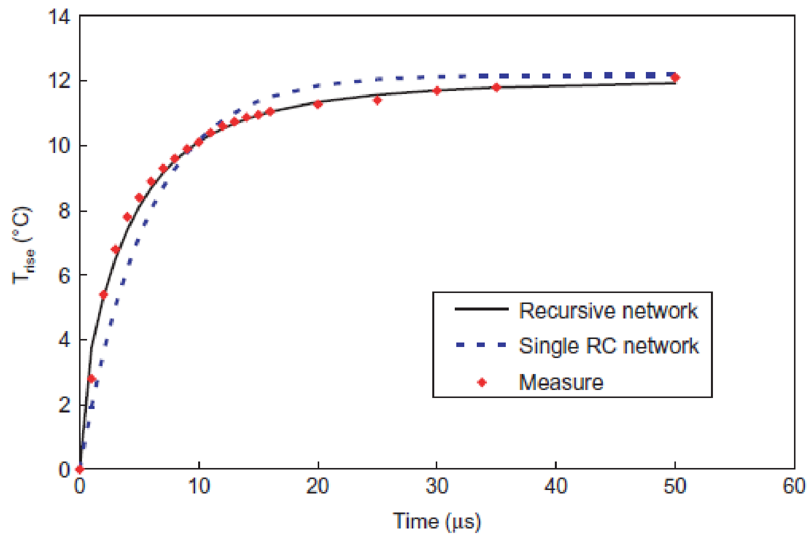


Figure 3.4 Comparison of transient temperature rise: measurement, 5-element recursive RC network and single RC network [12].

3.2 Joy and Schlig's method to calculate wafer thermal impedance

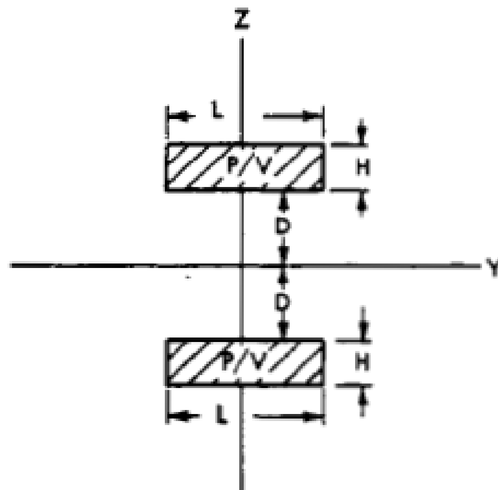


Figure 3.5 Cross-section of heat source and its image [6]

Joy and Schlig's method was briefly explained in section 2.2. Figure 2.4 is repeated here for convenience. Some changes are necessary to apply this method to calculate the wafer thermal impedance. Since the heat enters the wafer at the oxide-wafer interface, a plane surface heat source is assumed for calculations using equation (2.5). Hence, $H \rightarrow 0$ in figure 3.5.

The area of the heat source is equal to the area of the base of the Si-tub. In this case, the oxide is considered to be the adiabatic surface since it is a poor conductor of heat. The heat source is at oxide-wafer interface which implies that $D \rightarrow 0$ in figure 3.5. Also, since the objective is to find the thermal response at the oxide-wafer interface, equation (2.5) has to be evaluated at the position (x, y, z) = (0, 0, 0) [13]. With these modifications, equation (2.5) becomes

$$T(0,0,0,t) = \frac{P}{C}\int_0^t \left[erf\left(\sqrt{\frac{t_W}{u}}\right)\right] \cdot \left[erf\left(\sqrt{\frac{t_L}{u}}\right)\right] \cdot \left[erf\left(\sqrt{\frac{t_H}{u}}\right)\right] du \tag{3.12}$$

where $t_W = W^2/(16k)$, $t_L = L^2/(16k)$ and $t_H = H^2/(16k)$ and k is the thermal diffusivity of the wafer in cm^2/s [13].

The equivalent thermal resistance of the wafer is calculated by numerically integrating the above equation such where $t \rightarrow \infty$ and using

$$R_{th} = T(0,0,0,\infty)/P \tag{3.13}$$

3.3 Rinaldi's method to calculate wafer thermal impedance

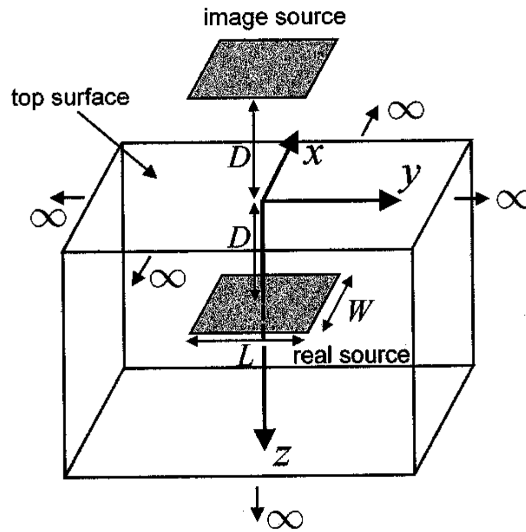


Figure 3.6 Thermal model of an integrated device with a surface heat source [14].

In [14], Joy and Schlig type of calculations have been done for a planar surface heat source dissipating $q_S(t')$ W/cm^2 of power per unit area. Image theory has been applied similar to the method in [6] as illustrated in figure 3.6. The calculations have been done assuming the

conditions similar to that in section 3.2. The temperature response at the center of the heat source, assuming that $D = 0$ in figure 3.5 is given by

$$T_P(t) = \frac{\sqrt{\alpha}P}{k\sqrt{\pi}\mathrm{WL}}\int_0^t \left[\mathrm{erf}\left(\frac{\sqrt{\pi}}{2}\sqrt{\frac{t_1}{u}}\right)\right]\cdot\left[\mathrm{erf}\left(\frac{\sqrt{\pi}}{2}\sqrt{\frac{t_2}{u}}\right)\right]\frac{\mathrm{d}u}{\sqrt{u}} \tag{3.14}$$

where α is the thermal diffusivity in cm^2/s, P is the power dissipated in watts, k is the thermal conductivity of substrate (W/cm-K) and $W{\cdot}L$ is the area of the heat source, $t_1=W^2/(4\pi\alpha)$ and $t_2=L^2/(4\pi\alpha)$. Since $L > W$, it is assumed that $t_1 < t_2$ without the loss of generality. The above equation does not have an analytical solution and hence the following approximations have been used in [14] for the evaluation of the error function:

$$\mathrm{erf}(x) \cong \begin{cases} \dfrac{2}{\sqrt{\pi}}x & for \quad 0 \le x \le \dfrac{\sqrt{\pi}}{2} \\ 1 & for \quad x \ge \dfrac{\sqrt{\pi}}{2} \end{cases} \tag{3.15}$$

By substituting equation (3.15) in equation (3.14), transient thermal impedance $Z_{th}(t)$ can be evaluated as [14]

$$Z_{th}(t) = \frac{T_P(t)}{P} = \frac{\sqrt{\alpha}}{k\sqrt{\pi}WL}\cdot\begin{cases} 2\sqrt{t} & t \le t_1 \\ 2\sqrt{t_1}\left[1 + \ln\sqrt{t/t_1}\right] & t_1 \le t \le t_2 \\ 2\sqrt{t_1}\left[2 + \ln\sqrt{t_2/t_1}\right] - 2\sqrt{t_1 t_2/t} & t \ge t_2 \end{cases} \tag{3.16}$$

The steady state value of the thermal resistance R_{th} (Z_{th} as $t\rightarrow\infty$) is given by [14]

$$R_{\mathrm{th}} = \frac{T_P(\infty)}{P} = \frac{1}{k\pi L}\left[2 + \ln\frac{L}{W}\right] \tag{3.17}$$

Equation (3.16) shows that the response consists of three phases separated by the two time constants: t_1 determined by W, and t_2 determined by L. The advantage of Rinaldi's method over Joy and Schlig's method is that it is not necessary to evaluate the numerical integration. Hence, it is easy to carry on the computations without a significant loss of accuracy.

Calculations using the Rinaldi's method are within 15% of calculations of those using Joy and Schlig's method, as shown in table 3.1 (The table can be found in section 3.4).

3.4 Calculation of wafer thermal capacitance

Joy and Schlig's and Rinaldi's methods provide appropriate ways to calculate thermal resistance, but calculation of thermal capacitance C_{th} using equation (2.4) is not accurate because of the distributed nature of the problem. Hence, C_{th} has been calculated analytically [13] using the thermal response calculations of the above two methods. The method can be explained by using the analogous electrical circuit shown in figure 3.7. If C_{eq} is the equivalent capacitor of the network, the value of C_{eq} can be calculated by the product of voltage across C_{eq} and the charge stored on it.

$$Q_C = C_{eq} \cdot V_f \quad \Rightarrow \quad C_{eq} = \frac{Q_C}{V_f} \tag{3.18}$$

where V_f is the final voltage across the capacitor.

Charge stored on the capacitor can be calculated by integrating the capacitor current with respect to time. So, C_{eq} is given by

$$C_{eq} = \frac{1}{V_f} \int_0^{\infty} \left(I - \frac{V(t)}{R} \right) dt \tag{3.19}$$

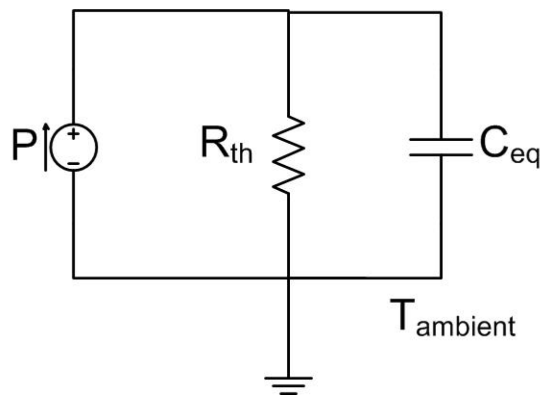


Figure 3.7 Thermal equivalent network of single pole thermal impedance

Using the analogy between thermal and electrical parameters, an expression for equivalent thermal capacitance C_{th} of the wafer can be obtained as shown below [13]:

$$C_{\text{th}} = \frac{1}{T_f}\int_0^{\infty}\left(P - \frac{T(t)}{R_{\text{th}}}\right)dt \tag{3.20}$$

where $T_f = PR_{th}$ is the final temperature reached. Using this relation in equation (3.20) and simplifying, an expression for the equivalent time constant $\tau_{\text{th}} = C_{\text{th}}R_{\text{th}}$ is obtained as given by

$$\tau_{\text{th}} = \int_0^{\infty}\left(1 - \frac{T(t)}{PR_{\text{th}}}\right) \tag{3.21}$$

C_{th} can be readily calculated from the above expression by substituting for $T(t)/P$ from either [6] or [14]. R_{th} can be calculated by the same ratio evaluated as $t \rightarrow \infty$. To evaluate the time constant, the final time was taken to be the time t at which Z_{th}(t) gives 99% of the value of R_{th} obtained by the methods from [6] or [14]. The values of thermal resistance and time constants evaluated using these methods for various devices are shown in table 3.1

Table 3.1 Thermal impedance calculations for the wafer

Device W=0.25 µm	**Dimensions of source** W=3.03 µm	**Rth (K/W) (100%)**		**Time Constant (µs)**		**Cth (J/K)**	
		J&S*	Rinaldi$^{\Psi}$	J&S*	Rinaldi$^{\Psi}$	J&S*	Rinaldi$^{\Psi}$
L=0.6 µm	L=2.34 µm	1353	1531	0.17	0.78	1.26E-10	5.09E-10
L=0.8 µm	L=2.6 µm	1287	1461	0.18	0.74	1.40E-10	5.07E-10
L=1 µm	L=2.8 µm	1242	1412	0.19	0.71	1.53E-10	5.03E-10
L=5 µm	L=6.6 µm	773	866	0.45	0.48	5.82E-10	5.54E-10
L=10 µm	L=11.8 µm	531	586	0.86	1.05	1.62E-09	1.79E-09
L=20 µm	L= 21.8 µm	344	375	1.72	2.56	5.00E-09	6.83E-09

*Calculated using Joy and Schlig's method; $^{\Psi}$Calculated using Rinaldi's method

3.5 Analytical solution for the calculation of wafer thermal impedance

Joy and Schlig's method for the calculation of wafer thermal resistance involves the evaluation of numerical integration which is not computationally efficient. So, an analytical expression was derived for the temperature response in a semi-infinite medium as shown in figure 3.4 for the special case of a square source. Using the approximation $H \rightarrow 0$ in equation (3.12), and using surface heat capacitance, C', instead of volume heat capacitance, the expression for temperature response becomes [13]

$$T(t) = \frac{P}{C'} \int_0^t \left\{ erf\left(\frac{\sqrt{\pi t_W}}{\sqrt{4u}} \right) \cdot erf\left(\frac{\sqrt{\pi t_L}}{\sqrt{4u}} \right) \cdot \left(\frac{1}{\sqrt{\pi k u}} \right) \right\} du \tag{3.22}$$

where $t_W = W^2/4\pi k$, $t_L = L^2/4\pi k$, $C' = \rho c A$ is the surface heat capacitance and $A = L \cdot W$.

The integral in equation (3.22) can be evaluated using an approximation for the error function erf(x) given by [20]

$$\mathrm{erf}(x) \approx \sqrt{1 - \exp\left(-\left(2x/\sqrt{\pi} \right)^2 \right)} \tag{3.23}$$

Using the above approximation and putting $L = W$, the expression for $Z_{th}(t) = T(t)/P$ from equation (3.22) becomes

$$Z_{\mathrm{th}}(t) = \frac{1}{C'} \int_0^t \left\{ \left(1 - \exp\left(-\frac{t_L}{u} \right) \right) \cdot \left(\frac{1}{\sqrt{\pi k u}} \right) \right\} du \tag{3.24}$$

The indefinite integral in equation (3.24) was evaluated using an online tool [15], giving an analytical expression for thermal impedance $Z_{th}(t)$ for the case $L = W$.

$$Z_{\mathrm{th}}(t) = \frac{2}{C' \sqrt{\pi k}} \left[\sqrt{t} \left\{ 1 - \exp\left(-\frac{t_L}{t} \right) \right\} + \sqrt{\pi t_L} \left\{ 1 - erf\left(\sqrt{\frac{t_L}{t}} \right) \right\} \right] \tag{3.25}$$

The value of R_{th} can be found out by putting $t \rightarrow \infty$ in equation (3.25) as given by

$$R_{\mathrm{th}} = \frac{2}{C'} \sqrt{\frac{t_L}{k}} \tag{3.26}$$

3.5.1 Adapting analytical solution for the case where L is not equal to W

Equation (3.25) was modified for the case where L is not equal to W by using $L_1 = \sqrt{L \cdot W}$. The value of R_{th} was calculated using the analytical expression and compared with the Joy and Schlig numerical calculations and the Rinaldi's method, for various values of aspect ratio (L/W) of the heat source. The thermal resistance values obtained by the three methods are shown in table 3.2. It can be observed that the error percentage between numerical and analytical expressions for Joy and Schlig's method increases as the value of the ratio L/W changes from 1. The thermal response for the wafer, calculated using Joy and Schlig (numerical and analytical methods) and Rinaldi's calculations for a low voltage NPN device of emitter length 5 μm (L = 6.6 μm and W = 3.03 μm in table 3.2) are shown in figure 3.8. It can be observed that all the three methods show a similar response.

Table 3.2 Comparison of analytical and numerical calculations for wafer thermal resistance

L **(μm)**	***W*** **(μm)**	***L/W***	R_{th} **(K/W)**			
			JS numerical	**JS analytical**	**% error between Analytical & Numerical**	**Rinaldi**
2.4	3.03	0.79	1342	1350	0.57	1512
2.6	3.03	0.86	1293	1297	0.32	1459
2.8	3.03	0.92	1248	1250	0.17	1409
3.03	3.03	1	1200	1201	0.11	1356
6.6	3.03	2.18	780	814	4.40	865
11.8	3.03	3.89	538	609	13.23	585
21.8	3.03	7.19	351	448	27.61	374

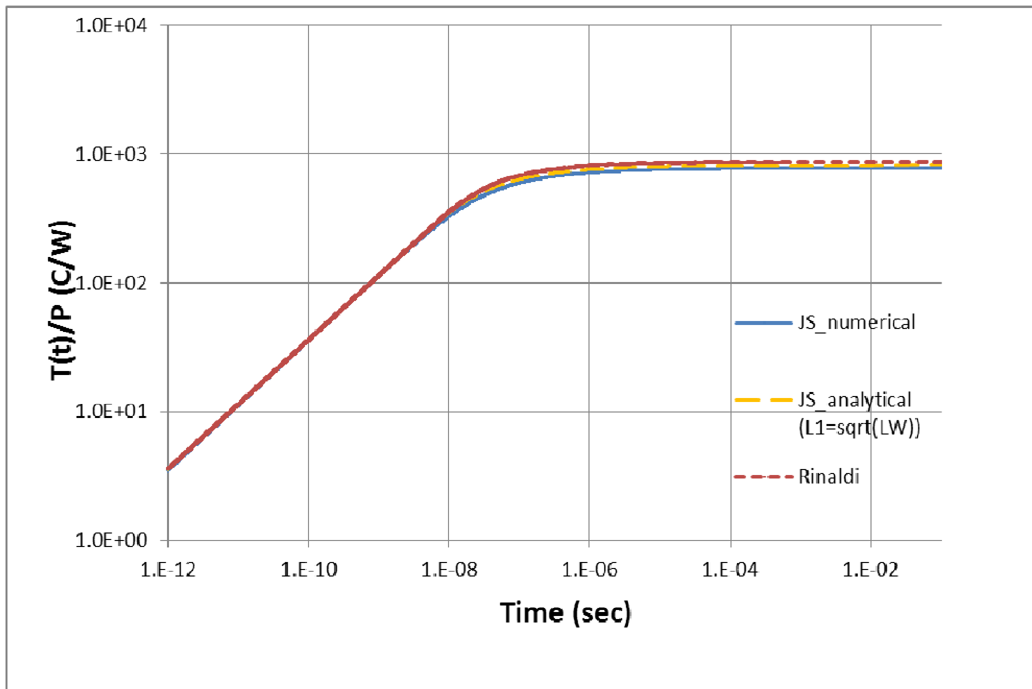


Figure 3.8 Thermal response calculated using numerical and analytical expressions.

CHAPTER 4

COMMON EMITTER AND FORWARD GUMMEL CONFIGURATION TO CHARACTERIZE THERMAL IMPEDANCE OF SILICON GERMANIUM HBT

Time domain measurements have been taken using the common base configuration by observing the V_{be} response to a pulse input at the base of the SiGe HBT as explained in appendix A. S-parameters have also been measured to characterize the thermal impedance of the devices as explained in Appendix A. In this section, a common emitter circuit has been designed which can be used for time domain measurements. Also, a method to obtain thermal resistance from forward Gummel measurements (DC measurements) [13] have been discussed.

4.1 Common emitter configuration

A common emitter circuit is shown in figure 4.1. A pulse input is given to the base through a sufficiently high resistance (to mimic a current source at the base) [13] and the V_{be} response is observed. Resistor R_B was designed to obtain higher thermal tail in the voltage V_{be}. The objective was to get a thermal tail whose magnitude is equal to at least 10% of the change in static value of V_{be}. The amplitude of thermal tail is the difference between peak voltage reached by the base emitter voltage, V_{be}, and the static value reached by V_{be}. Figure 4.3 illustrates the terms: “thermal tail” and “static delta V_{be}”.

It is required that the collector-emitter voltage, V_{CE}, be relatively constant. It is also desired to measure the collector current using the voltage drop across a resistor. For this purpose, a small resistor of 10 Ω is placed between V_{CC} and the collector terminal [13].

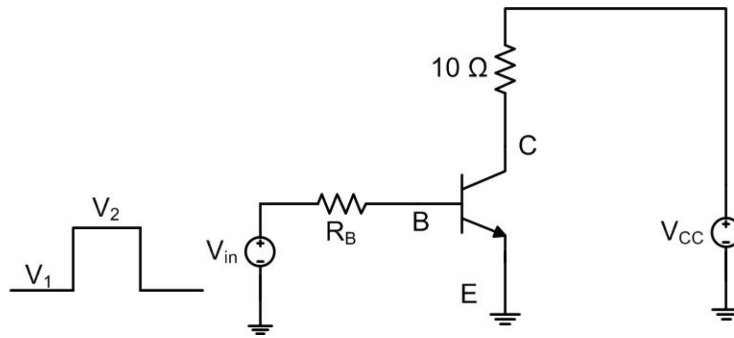


Figure 4.1 Common emitter configuration setup

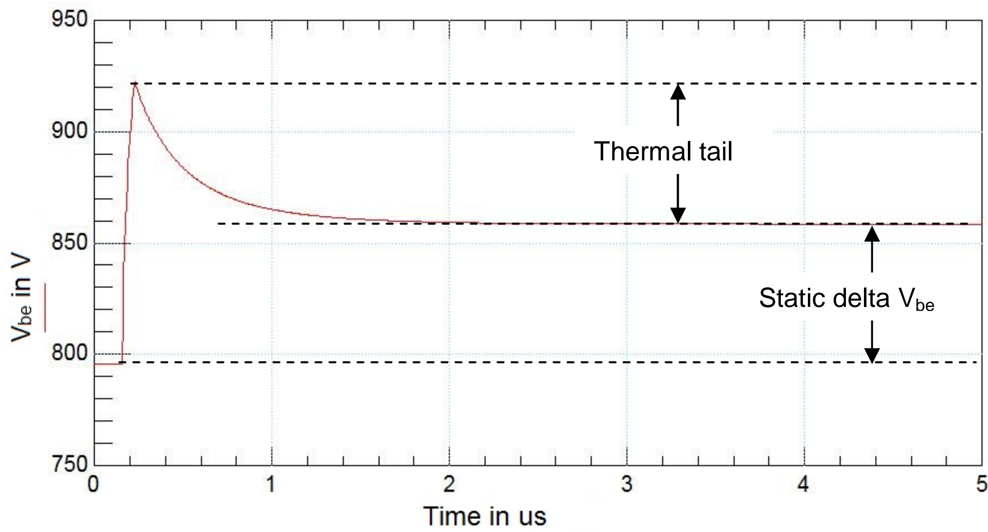


Figure 4.2 Transient simulation response observed at base emitter junction

4.1.1 Design of base resistor

Using the appropriate thermal network for a device, the forward Gummel curves are obtained by simulation. Forward Gummel data gives the required V_{BE} and I_C values to be in the safe operating area (SOA) of the device. Shown in figure 4.3 is the forward Gummel plot for a low voltage NPN device with length equal to 10 μm and width equal to 0.25 μm. The maximum I_C for this device is 5.5 mA to be in SOA (from the calculations based on maximum allowed current density). From figure 4.3, it can be observed that the maximum V_{BE} for this device is about 0.9 V. It was desired that V_{BE} should step from 0.8V to 0.9V such that V_{BE} = 0.9V when

V_{in} = 2V [13]. R_B values were designed by observing the I_B values at the required values of V_{BE} from the forward Gummel plot.

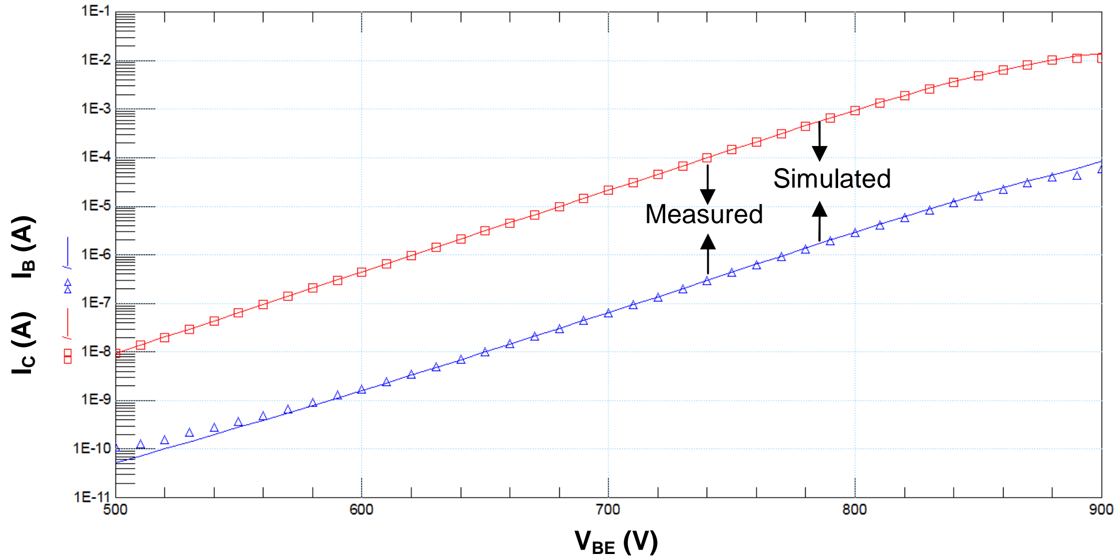


Figure 4.3 Forward Gummel plot for low voltage NPN device with W=0.25 µm and L=10 µm

4.1.2 Base resistor values for various devices

The base resistor (R_B) values and the input-pulse amplitude values for various devices are shown in table 4.1. The base resistor was planned to be implemented using 3 resistors as shown in figure 4.1 so that the ones not required could be shorted out. The values were chosen such that the total resistance gives the highest value of the required R_B. So, three resistors 283 kΩ, 51 kΩ and 29.3 kΩ were chosen such that the sum of the resistances is equal to the highest R_B required i.e. 367 kΩ as. The calculated values of the resistors and available standard resistors are shown in table 4.2.

It can be observed from table 4.3 that the magnitude of thermal tail increases as V_{CC} increases, since it results in more power being dissipated in the device. Future work involves the design of a printed circuit board for a common emitter configuration for taking time domain measurements.

Table 4.1 R_B values such that V_{BE} = 0.9 V when V_{in} = 2 V

Device L	Total RBB (kΩ)	Vin1 (V)	Vin2 (V)
1 µm	367	0.856	2
5 µm	51	0.837	2
10 µm	29.3	0.841	2

Table 4.2 Values of calculated and available standard resistors

Calculated (kΩ)	Standard resistor (kΩ)
283	300
51	51
29.3	30

Table 4.3 Thermal tail values for different devices and bias voltages

Device Length L = 0.25 µm		VCC = 1.25 V			VCC = 2.0 V		
Device width W		Thermal tail (V)	Static delta V_{be} (V)	Ratio (%)	Thermal tail (V)	Static delta V_{be} (V)	Ratio (%)
1 µm	Rise	8.2	95.7	8.6	12.7	90.1	14.1
	Fall	6.3	95.7	6.6	10.0	90.1	11.1
5 µm	Rise	43.5	88.6	49.1	62.0	64.1	96.7
	Fall	29.5	88.6	33.3	45.1	64.1	70.4
10 µm	Rise	43.6	90.3	48.3	63.4	62.7	101.1
	Fall	31.1	90.3	34.4	48.5	62.7	77.4

4.2 Forward Gummel configuration

The forward Gummel measurement setup is shown in figure 4.4. The base emitter voltage V_{BE} is swept from 400 mV to 900 mV for various values of V_{CB}. The collector current I_C and the base current I_B are measured at each value of V_{BE}. The result of a standard forward Gummel measurement (V_{CB} = 0 V) is shown in figure 4.3.

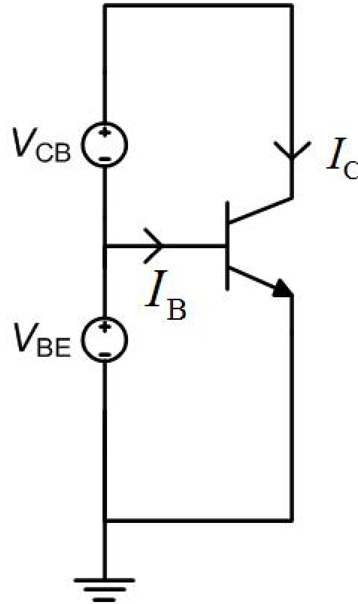


Figure 4.4 Forward Gummel measurement setup

4.2.1 Extraction of thermal resistance from forward Gummel measurements

The proposed method uses the VBIC model to estimate the temperature of the junction in the SiGe device [13]. R_{th} is set to 0 in the device model so that the simulations do not consider the effect of self-heating. The SPICE parameter TEMP, which defines the ambient temperature used for simulations in the SPICE program, is optimized using the optimization routine available in the Integrated Circuit Characterization and Analysis Program (ICCAP). At several points on the forward Gummel plot, ranging from V_{BE} = 780 mV to V_{BE} = 879 mV and V_{CE} = 0 V to 1 V, the difference dT_j between the optimized TEMP and the temperature at which measurements were taken, was calculated as shown below:

$$dT_j = \text{TEMPs} - \text{TEMPm} \tag{4.1}$$

The parameter TEMPs is the optimized temperature, and TEMPm is the temperature at which measurements were taken. The thermal resistance R_{th} is calculated as the ratio of change in temperature to the change in power dissipation in the device, using the following expression:

$$R_{\mathrm{th}} = \frac{\mathrm{d}T}{\mathrm{d}P} \tag{4.2}$$

where P is the power dissipation in the device given by

$$P = V_{\mathrm{BE}} I_{\mathrm{B}} + V_{\mathrm{CE}} I_{\mathrm{C}} \tag{4.3}$$

Here, V_{BE} is the base-emitter voltage, I_B is the base current, V_{CE} is the collector-emitter voltage and I_C is the collector current. Equation (4.2) is evaluated for various values of V_{BE}, keeping V_{CB} constant so that the artifacts of the Early effect do not appear in the calculations. This procedure was repeated for various values of V_{CB}. As a sanity check, the VBIC thermal resistance parameter, R_{TH}, was also optimized by setting TEMP to the value of temperature at which the measurements were taken. The values of R_{TH} obtained by optimization were exactly equal to the thermal resistance values calculated using equation (4.2). The results of the measurement are explained in the next chapter.

CHAPTER 5

RESULTS AND DISCUSSION

Based on the results of DC, time domain and frequency domain measurements, the low voltage NPN (LVNPN) HBT, manufactured using CBC8 process, has been thermally characterized. All the results presented in this section were measured for a LVNPN HBT of emitter length 20 μm and emitter width 0.25 μm, manufactured by NSC. In this work, Levenberg-Markquardt algorithm has been used for all the optimizations done in ICCAP.

5.1 Forward Gummel measurement results

Forward Gummel measurements were done using the setup shown in figure 4.4. The base emitter voltage V_{BE} was swept from 400 mV to 900 mV for various values of collector-base voltage V_{CB}. The collector current I_C and the base current I_B were measured at each value of V_{BE}. The VBIC parameters IS and IBEI were optimized using the optimization function in ICCAP for the case of V_{CB} = 0 V. The same IS and IBEI were used for time domain and frequency domain simulations. Shown in figure 5.1 is the plot of the change in junction temperature, dT_j, versus the power dissipated, dP, obtained by the method explained in section 4.2.1. The figure shows four curves corresponding to four different V_{CB} voltages equal to 0 V, 125 mV, 250 mV and 1 V. These curves were fit with second order polynomial trend-lines (using the option available in Microsoft Excel). Since $dT = R_{th} \cdot dP$, it is expected that the slope of various curves of dT_j versus dP be equal. However the slopes are not equal which may be the result of Early effect at the base-emitter junction of the HBT, since the base region is heavily doped which results in a smaller value for the VBIC parameter VER [13]. The thermal resistance was calculated by finding the slope of these curves.

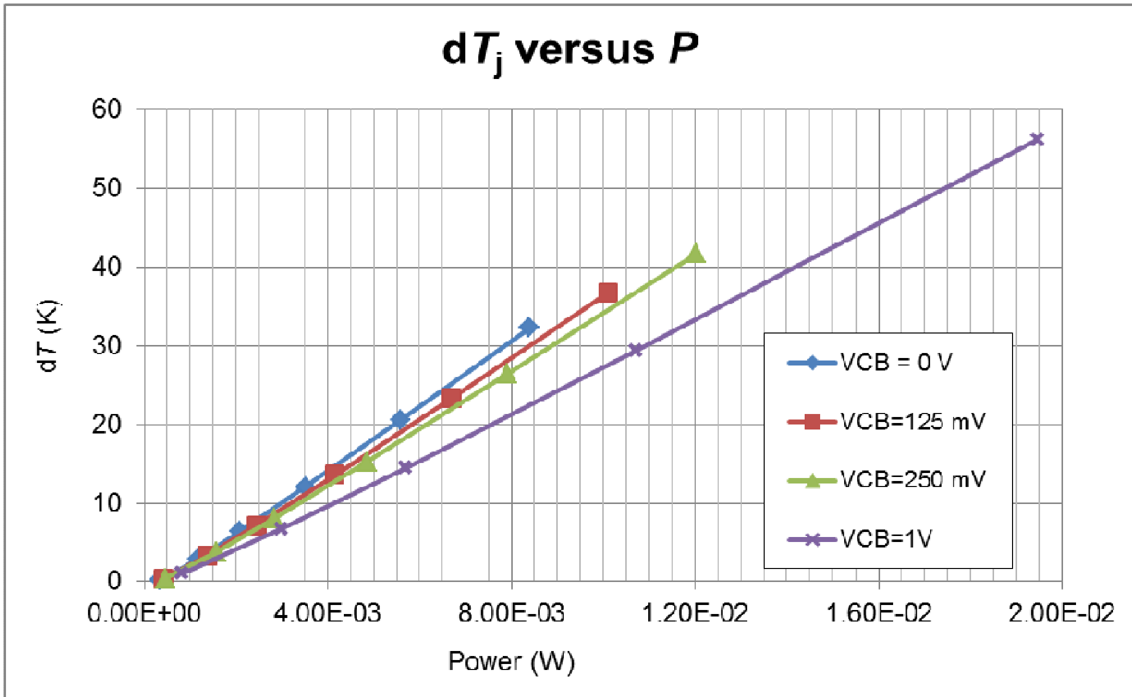


Figure 5.1 Plot of dT versus P for various values of V_{CB}

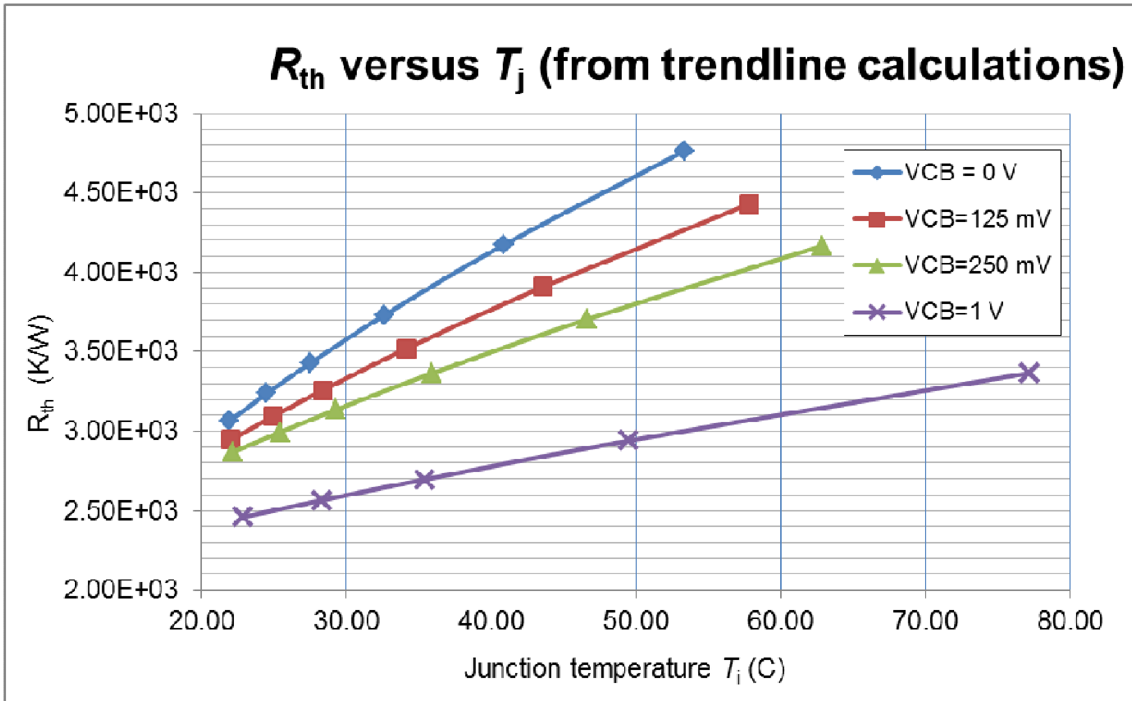


Figure 5.2 Plot of R_{th} versus T_j for various values of V_{CB}

The junction temperature $T_j = dT_j$ + TEMPm was found for various values of power P using the value of dT_j obtained from the trend-lines used to fit these curves. Thermal resistance R_{th} was calculated and plotted against the junction temperature T_j for various V_{CB} values as shown in Figure 5.2.

5.2 Time domain measurement results

Time domain measurements were taken using the common base configuration explained in appendix A. In this configuration, a pulse input is given to the emitter junction and the response at the base-emitter junction is observed. An input pulse step was chosen to give a higher thermal tail (about 16% of the change in static values of V_{be}). The input pulse was generated from a signal generator. The period and amplitude settings of the signal generator are found in table 5.1. Since the base is grounded, a negative input signal is given to the emitter.

Table 5.1 Input pulse parameters

Input type	Period	Rise/Fall time	Low voltage	High voltage
Pulse	100 μs	50 ns	-1.626 V	-792.3 mV

A 3-pole foster network was connected to the dT node in the VBIC model of the HBT. This electrical network represents the thermal impedance network of the device. The initial values for thermal resistance and thermal capacitance in the Foster network mentioned in table 5.2, were obtained from the spreadsheet which has been explained in appendix C. The measurement and simulation results for the rising edge are shown in figure 5.3. Similarly the measurement and simulation results for the falling edge are shown in figure 5.4. It is to be noted that the simulation was done using the optimized values of the Foster network elements using the “optimize” program in ICCAP. It can be observed that the simulation result matches with the measured data after optimization. The optimized values are compared with the starting values of the Foster network in table 5.2. It can be observed that there is a reduction of about 4% in the

total thermal resistance after the optimization of thermal resistance and thermal capacitance values.

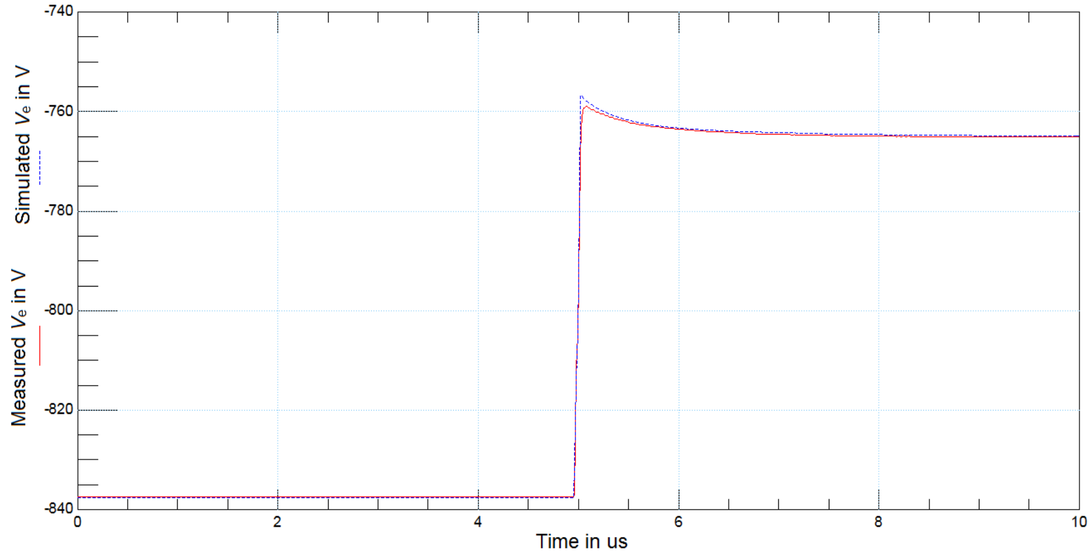


Figure 5.3 Simulated and measured result of rising edge of V_e

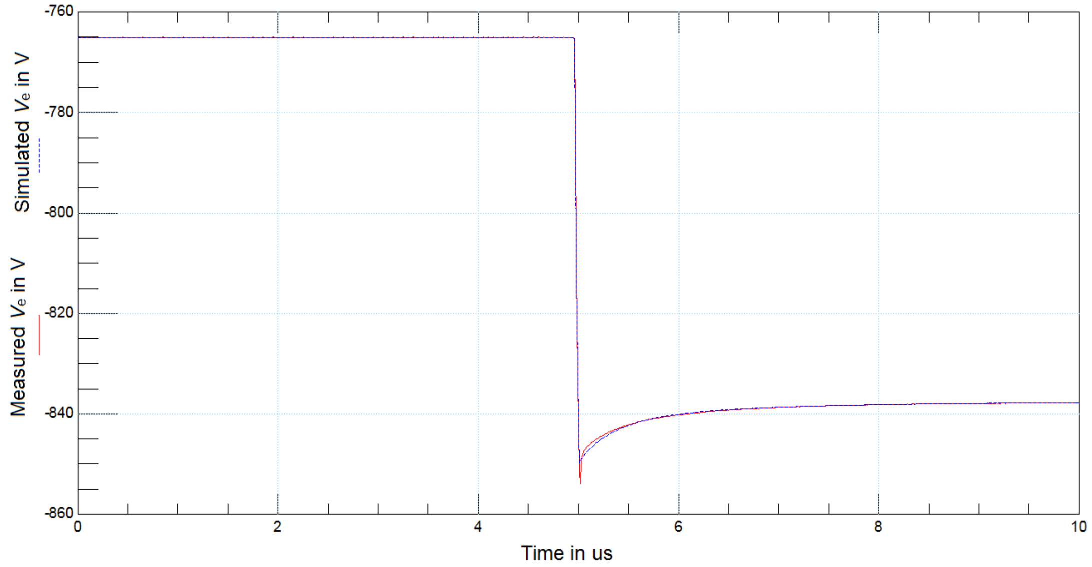


Figure 5.4 Simulated and measured result of falling edge of V_e

Table 5.2 Calculated and optimized Foster network values

	R_{f1} (K/W)	T_{f1} = $R_{f1}C_{f1}$ (s)	R_{f2} (K/W)	T_{f2} = $R_{f2}C_{f2}$ (s)	R_{f3} (K/W)	T_{f3} = $R_{f3}C_{f3}$ (s)	R_{total} (K/W)	T_{eq} (s)
Calculated*	137.5	13.5E-9	1544.9	207.9E-9	596.8	937.0E-9	2279.2	1.16E-6
Optimized	243.6	30.4E-9	567.9	1.715E-6	1382	355.2E-9	2193.7	2.10E-6

*Transformation from Cauer (calculated using Masana and Joy and Schlig's methods) to Foster network

The optimized Foster network was converted to Cauer network. The theoretical 3-pole Cauer network values (calculated using Masana and Joy and Schlig's method) were also compared with the optimized values as shown in table 5.3.

Table 5.3 Calculated and optimized Cauer network values

	R_{c1} (K/W)	C_{c1} (J/K)	R_{c2} (K/W)	C_{c2} (J/K)	R_{c3} (K/W)	C_{c3} (J/K)	R_{total} (K/W)
Calculated*	1031.5	10.5E-12	1518.6	41.7E-12	343.7	2.54E-9	2279.2
Optimized#	544.26	81.8E-12	1311.9	199E-12	337.35	4.72E-9	2193.7

*Calculated using Masana and Joy and Schlig's methods, #Transformation from optimized Foster network to Cauer network

5.3 Frequency domain measurement results

Frequency domain measurements were done using Agilent network analyzer 8753ES as explained in appendix A. S-parameters were measured and converted into Y-parameters. The inverse of Y_{11} was used for optimization instead of the impedance parameter Z_{11} to avoid the artifacts of the Early effect. The device was biased at various V_{CE} and V_{BE} voltages, always ensuring that the device operates in the active region and well within the SOA defined for the device. The 3-pole Foster network that was used for time domain optimizations was used for estimations in frequency domain also.

The low frequency part of the Y_{11} curve was matched by using the tuning function in ICCAP. The plot of inverse of Y_{11} versus frequency is plotted in figure 5.5 for the following bias conditions: V_{BE} = 862 mV and V_{CE} = 1.862 V with a DC power dissipation of 19.5 mW. It can be observed that the real part of inverse of measured Y_{11} in the low frequency region matches with

the simulated results. Optimization on the entire range of frequency i.e., 30 kHz to 3 GHz has not been possible and hence capacitance values have not been confirmed from frequency domain measurements.

It was observed that the total thermal resistance after optimization at low frequency was equal to 2816 K/W. The estimated thermal impedance parameters from the frequency domain measurements are compared with the thermal impedance parameters obtained from time domain in table 5.4. The thermal resistance calculated from DC measurements at V_{BE} = 862 mV and V_{CE} = 1.862 V as explained in section 5.1, is equal to 3367 K/W. The thermal resistances calculated from DC and frequency domain methods have an error of about 20%. It was also observed that the plots of $1/Y_{11}$ match in the low frequency region (30 kHz to 60 kHz) for the same total R_{th} as above (2816 K/W), when the thermal capacitances were removed and a single thermal resistor equal to total R_{th} was connected to the dt node.

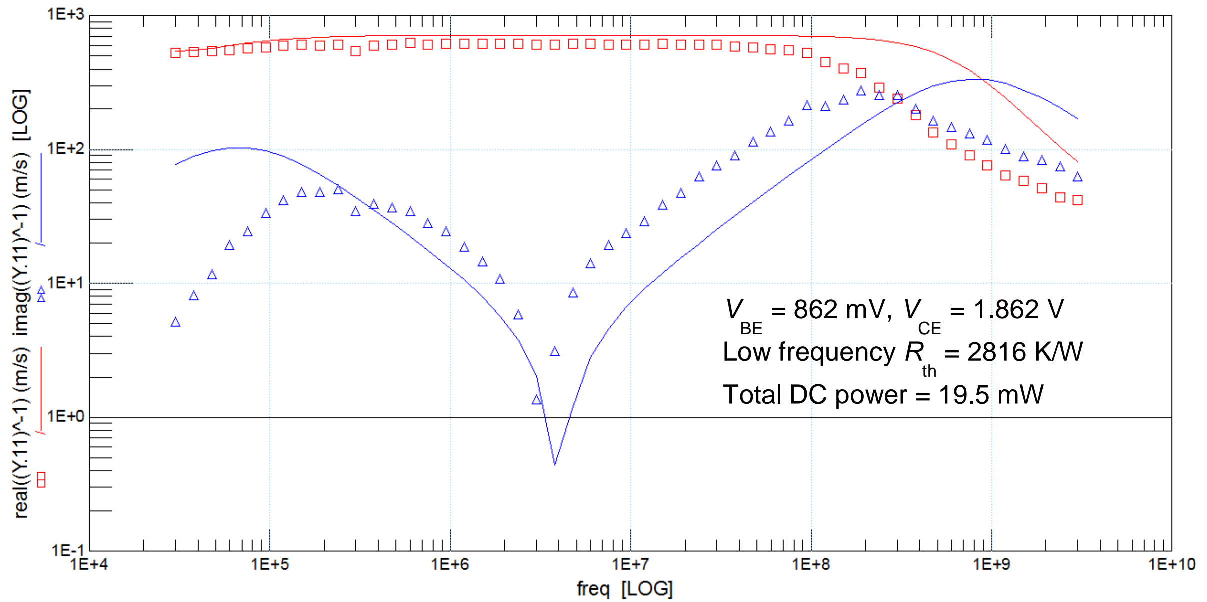


Figure 5.5 Log-log plot of inverse of Y_{11} versus frequency

Table 5.4 Comparison between thermal impedance parameters (Foster network) obtained from time domain and frequency domain

	R_{f1} (K/W)	$T_{f1} = R_{f1}C_{f1}$ (s)	R_{f2} (K/W)	$T_{f2} = R_{f2}C_{f2}$ (s)	R_{f3} (K/W)	$T_{f3} = R_{f3}C_{f3}$ (s)	R_{total} (K/W)
Calculated*	137.5	13.5E-9	1544.9	207.9E-9	596.8	937.0E-9	2279.2
Frequency domain, estimated	2195.9	7.45E-12	522.7	2.481E-6	97.39	2.521E-6	2816

*Transformation from Cauer (calculated using Masana and Joy and Schlig's methods) to Foster network

5.4 Summary

The results from DC, time domain and frequency domain measurements were compared with the theoretical value of R_{th} obtained from the spreadsheet explained in appendix C. The results are summarized in table 5.5. The thermal resistance values from time domain and frequency domain measurements are compared with the DC characterization results at the corresponding power levels as illustrated by shaded rows in table 5.5.

Table 5.5 Comparison between DC, time domain, frequency domain and theoretical methods

Condition	Total R_{th} (K/W)	V_{CB} (V)	V_{BE} (V)	Power (mW)	T_j# (C)
Theoretical*	2279	-	-	-	27
DC measurements	3367	1.0	0.862	19.5	77
Frequency domain measurements	2816	1.0	0.862	19.5	77
DC measurements	2757	1.0	0.838	6.94	38.84
Time domain measurements	2194	1.0	0.838	6.94	38.84

*Calculations using Masana and Joy and Schlig's methods; # Junction temperature inferred from trendline calculations

CHAPTER 6

CONCLUSION AND RECOMMENDATIONS

A low voltage NPN HBT device with the emitter dimensions of $0.25 \times 20\ \mu m^2$ has been characterized by utilizing the results from DC, time domain and frequency domain measurements.

It has been observed that the DC, time domain and frequency domain methods give similar results for the total thermal resistance as illustrated in table 5.5.

From the observations of DC domain measurement results, it can be concluded that the thermal resistance is a function of the junction temperature. This is in agreement with the theory since the HBT is made up of Si and SiO_2 and the thermal conductivity of Si decreases with temperature (in the temperature range of 100 K to 400 K) and the thermal conductivity of SiO_2 increases with temperature (in the temperature range of 0 K to 350 K) [17]. So, it is recommended that voltage dependent resistors be connected to the dT node in the VBIC model of the transistor so that the resistors model the temperature dependence of thermal resistance.

Due to the distributed nature of the thermal resistance of the device, the thermal resistance could be more accurately modeled by a distributed RC network than a single pole RC network present in the VBIC model.

APPENDIX A

TIME DOMAIN AND FREQUENCY DOMAIN MEASUREMENTS TO CHARACTERIZE THE THERMAL IMPEDANCE OF SILICON GERMANIUM HBT

A.1 Time domain measurements

Time domain measurements have been taken with a common base circuit configuration as shown in figure A.1. The position of the low voltage NPN device of emitter area 0.25x20 μm^2 was identified by using the wafer layout provided by NSC. The device was probed by adjusting the position of infinity probes on the wafer. The signals at the emitter node, the base node, the collector node, and the V_{in} waveform were observed on the oscilloscope and stored into a computer in a comma separated value (CSV) format. The signal at the emitter node was formatted into an output file format recognized by ICCAP and imported into ICCAP. A pulse input block is added in the ICCAP simulation setup with the step values corresponding to V_{in}.

The theoretical thermal impedance values R_{th}, C_{th} for the silicon tub, oxide and wafer regions were calculated using the spreadsheet explained in appendix C. The circuit shown in figure A.1 was simulated in ICCAP using a 3-pole Foster network to define the thermal impedance network of the device. The theoretical values of R_{th} and C_{th} in the Foster network were optimized to match the measurement results with the simulated results [17]. The optimized Foster network is transformed to Cauer network to get the thermal capacitance and the thermal resistance of the tub, the oxide and the wafer regions of the HBT.

A.2 Frequency domain measurements

Frequency domain measurements have been taken on the HBT by using the setup shown in figure A.2. The Agilent network analyzer (NWA) 8753 ES was calibrated using the calibration procedure explained in [18]. The position of the low voltage NPN device of emitter area 0.25x20 μm^2 was identified by using the wafer layout provided by NSC. The device was probed by adjusting the position of infinity probes. The two-port S-parameters were measured in the frequency range of 30 kHz to 3 GHz using the NWA 8753ES and stored into the ICCAP as explained in [18]. The theoretical thermal impedance values R_{th}, C_{th} for the silicon tub, oxide and wafer regions were calculated using the spreadsheet explained in appendix C [19].

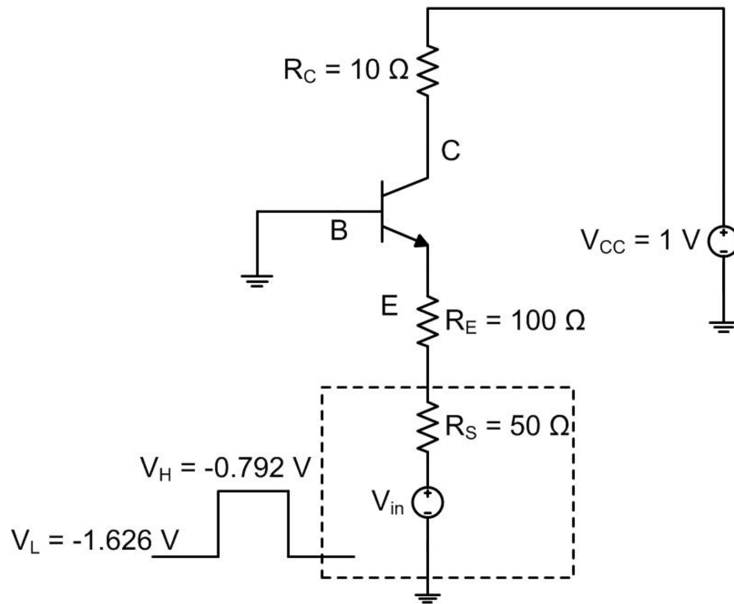


Figure A.1 Common base measurement setup

The circuit shown in figure A.2 was simulated in ICCAP using a 3-pole Foster network to define the thermal impedance network of the device. The theoretical values of R_{th} and C_{th} in the Foster network were optimized to match the measurement results with the simulated results. The optimized Foster network is transformed to Cauer network to get the thermal capacitance and the thermal resistance of the tub, the oxide and the wafer regions of the HBT.

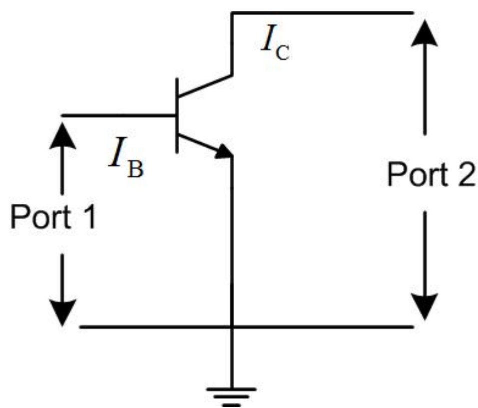


Figure A.2 Frequency domain measurement setup

APPENDIX B

COMPACT MODELS FOR THERMAL IMPEDANCE CALCULATION OF EACH LAYER

B.1 Thermal Resistance

The thermal resistance of a small section with thickness d*t* is given by

$$\mathrm{d}R = \frac{\mathrm{d}t}{kA(t)} \tag{B.1}$$

where *k* is the thermal conductivity of the solid and *A(t)* is the cross-sectional area at a depth of *t* from the top.

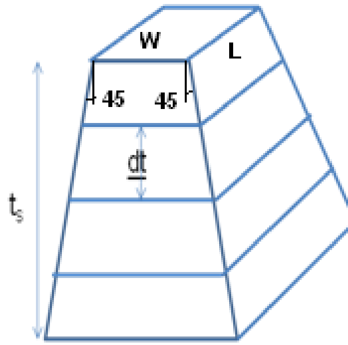


Figure B.1. Block of solid illustrating the spreading of heat.

A spreading angle of 45 degree is assumed for the derivation of total thermal resistance. *L* and *W* are lateral dimensions of the top surface of the solid. Hence *A(t)* is given by

$$A(t) = (L + 2t)(W + 2t) \tag{B.2}$$

Substituting eqn (B.2) in eqn (B.1) gives

$$\mathrm{d}R = \frac{\mathrm{d}t}{k(L + 2t)(W + 2t)} \tag{B.3}$$

Integrating equation (B.3) from $t = 0$ to $t = t_s$ will give the total thermal resistance of the solid

$$R = \int_{t=0}^{t=t_s} \mathrm{d}R \tag{B.4}$$

Carrying out the integration for *R* gives an expression as shown below:

$$R = \frac{1}{2k(L - W)} \ln\left[\frac{L\left(t_s + \frac{W}{2}\right)}{W\left(t_s + \frac{L}{2}\right)}\right] \tag{B.5}$$

B.2 Thermal Capacitance

The thermal capacitance can be calculated as shown below:

$$C_{\text{th}} = \mathrm{C}_{\text{p}} \rho V \quad \text{(B.6)}$$

where C_p is the specific heat capacity per unit mass, ρ is the density and V is the volume given by equation (B.7).

$$V = 4\left[LWt_s + \frac{(W+L)t_s^2}{2} + \frac{t_s^3}{3} \right] \quad \text{(B.7)}$$

B.3 Thermal Model of Si tub

The top surface dimensions of the Si tub are equal to the emitter dimensions [13]. The emitter dimensions and the thickness of the Si tub are substituted in equation (B.5) to give the thermal resistance of the layer. The thermal capacitance is estimated using equation (B.6) and equation (B.7).

B.4 Thermal Model of Oxide

The oxide thickness is very small compared to the lateral dimensions. Hence there is not much thermal spreading in the oxide layer. Therefore, to estimate the thermal resistance and capacitance of the oxide, the formulae to calculate thermal resistance of a slab are used. The thermal resistance of a slab is given by

$$R = \frac{t_{\text{ox}}}{\mathrm{k}LW} \quad \text{(B.8)}$$

where k is the thermal conductivity of the oxide, t_{ox} is the thickness of the oxide, L and W are the inner dimensions of the Si-tub. The thermal capacitance is estimated using equation (B.6) where V is given by

$$V = LWt_{\text{ox}} \quad \text{(B.9)}$$

B.5 Thermal Model of Si-wafer

Since the thickness of the wafer is very large compared to the lateral dimensions, the thermal resistance of the Si-wafer is estimated using equation (B.4), but in this case integrating *t* from 0 to ∞.

$$R = \int_{t=0}^{t=\infty} \mathrm{d}R \tag{B.10}$$

Therefore,

$$R = \frac{1}{2k(L-W)} \ln\left[\frac{L}{W}\right] \tag{B.11}$$

where k is the thermal conductivity of Si, *L* and *W* are the inner lateral dimensions of the Si-tub. The thermal resistance of the wafer can also be found using the approximation given by Joy and Schlig [6].

$$R_{\mathrm{th}} = \frac{1}{\mathrm{k}\sqrt{\pi L W}} \tag{B.12}$$

where k is the thermal conductivity of Si; *L* and *W* are the inner lateral dimensions of the Si-tub. If $L=W$, R_{th} is given by the following expression:

$$R_{\mathrm{th}} = \frac{1}{\mathrm{k}L\sqrt{\pi}} \tag{B.13}$$

To calculate the thermal capacitance, the thermal time constant τ_{th} is calculated as the time at which $Z_{th}(t)$ derived in [14] reaches $R_{th} \cdot (1-1/e)$. The thermal time constant τ_{th} is given by

$$\tau_{\mathrm{th}} = \frac{4 t_1 t_2}{(A-B)^2} \tag{B.14}$$

where

- $t_1 = W^2/(4\pi\alpha)$, $t_2 = L^2/(4\pi\alpha)$
- $A = 2\sqrt{t_1}\left[2 + \ln(L/W)\right]$
- $B = (1 - 1/e)\sqrt{\dfrac{LW}{\alpha}}$
- α is the *Thermal diffusivity*

The thermal capacitance of the wafer is calculated using the following expression:

$$C_{th} = \frac{\tau_{th}}{R_{th}} \tag{B.15}$$

APPENDIX C

SPREADSHEET FOR THREE-POLE NETWORK TRANSFORMATIONS AND TO CALCULATE WAFER THERMAL IMPEDANCE OF SIGE HBT

A spreadsheet was prepared to calculate the thermal resistance and capacitance of devices with various emitter areas [19]. The inputs to the spreadsheet are the dimensions of various regions of the device (tub, buried oxide and wafer). The principles used to calculate the thermal impedance parameters are explained in the chapter 2. A snapshot of the first page of the spreadsheet where the dimensions are entered and the calculated thermal impedance parameters are displayed is shown in figure C.1. The field where the dimensions are to be entered is also indicated in the figure. The conversion from 3-pole Cauer network into 3-pole Foster network using partial fraction expansion is also implemented in the spreadsheet.

	A	B	C	D	E	F	G	H
2	Length of Emitter(Le)	2.50E-07	m		Length of Emitter(Le)	0.25		R -> K/W
3	Width of Emitter(We)	5.00E-06	m		Width of Emitter(We)	5		C -> J/K
4	Inner length of Si-tub(Lt)	3.03E-06	m		Inner length of Si-tub(Lt)	3.03		
5	Inner Width of Si-tub(Wt)	6.60E-06	m		Inner Width of Si-tub(Wt)	6.6		
6	Thickness of wafer(tw)	7.00E-04	m		Thickness of wafer(tw)	700		
7	Thickness of tub(ttub)	1.35E-06	m		Thickness of tub(ttub)	1.35		
8	Thickness of Oxide(tox)	1.40E-07	m		Thickness of Oxide(tox)	0.14		
9								
10	Masana and Joy & Schilg Estimations							
11	Input		Cauer Network		Foster Network		TAU_FOSTER (n-sec)	
12	Rtub	1269.5	R1	1269.5	Rf1	434.0	Tf1	11.36
13	Rox	4996.9	R2	4996.9	Rf2	2209.0	Tf2	150.23
14	Rw	773.3	R3	773.3	Rf3	4396.7	Tf3	319.03
15	Ctub	2.999E-11	C1	1.500E-11	Cf1	2.618E-11		
16	Cox	1.900E-11	C2	2.449E-11	Cf2	6.801E-11		
17	Cw	5.855E-10	C3	3.022E-10	Cf3	7.256E-11		
18								
19	Algebraic Compact Model	(K/W)		Masana Calculations for wafer				
20	Rtub	1385.6		Rw	702.7			
21	Rox	5000.5		Cw	7.723E-04			
22	Rw	704.8						

Dimensions to be entered here

Figure C.1 Snapshot of the thermal impedance-calculator spreadsheet

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