DEVELOPMENT OF AN EXPERIMENTAL AND ANALYTICAL MODEL OF AN ACTIVE COOLING METHOD FOR HIGH-POWER THREE-DIMENSIONAL INTEGRATED CIRCUIT (3D-IC) UTILIZING MULTIDIMENSIONAL CONFIGURED THERMOELECTRIC MODULES

by

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ABSTRACT

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An increase in demand for more functionality and capacity of microelectronic components within the same logistic footprint drives the growth of three-dimensional integrated circuit (3D-IC) packaging technologies in recent years. However, the reduction in size and an increase in transistors density also intensify the heat flux of stacked-dice, which introduces many thermal challenges at both the package and cooling levels. Traditional passive cooling systems such as forced air convection cooling, phase change materials cooling and passive or active heat sinks will become inadequate to cool future processors and cannot accommodate the demand of future sub-ambient cooling of 3D-ICs. Within the past 10 years, major microprocessor manufactures have shifted their focuses toward higher bandwidth rather than frequency; however, the heat flux of current high-end CPU and GPU on the same die with parallel sequential computation is still in the order of 70 to 75 W/cm^2 with local heat flux

exceeding 1.5W/mm^2 and growing. Today, stack-dice are used widely as low-powered memory applications because thermal management of such 3D architectures as high-powered processors inherits many thermal challenges and is very costly. Heat dissipation of 3D-IC is highly non-uniform and non-unidirectional due to many factors such as material properties, power architectures, power leakage, transistor packing density, and real estate available on the processor. Inadequate thermal management of these systems leads to reduction in reliability, performance and ultimately a system's catastrophic failure. In this study, an experimental, an analytical, and a thermal cycling of an active cooling method for three-dimensional integrated circuits utilizing a multidimensional configured thermoelectric cooler were investigated. In addition, an alternative method to analyze thermoelectric cooling system employing a Modified-Graphical-Method (MGM) to eliminate the need of using proprietary fabrication information was also studied.

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CHAPTER 1

INTRODUCTION

In recent years, cooling high heat flux systems such as computer microprocessors, memory and data centers have become a global challenge because the demand for substantial real-time global communication integration, multitasking and faster computation is inversely proportional to the package size. This phenomenon has become the present and future trends for microelectronic packaging industries. The heat dissipation of microprocessors is projected to reach 360W with the maximum processor heat flux to be more than 190W/cm^2 for high performance CPU by the end of the next decade according to the International Electronics Manufacturing Initiative Technology (iNEMI) roadmap [1]. Conventional cooling methods using micro-channel, phase change material, natural and forced air convection, or liquid-cooled with nano-fluid alone might not be adequate enough for future applications especially when over-clocking processor is used. Particularly, heat dissipation of microprocessors is predominantly non-uniform and non-unidirectional due to different material properties, electrical power architectures and transistors packing density. Miniaturization combines with inadequate thermal management of these systems lead to material degradation, which causes the reduction in performance, reliability and ultimately system catastrophic failure.

Most modern computers and portable electronic devices are designed to operate above room temperature in the range of 60 to 100^{o}C. Commonly, CPU failures are due to mechanical and electrical failures such as: wire bonding failure, die cracking, electrical migration/diffusion, and gate oxidation. Using the Arrhenius equation, one can predict that the die failure rate can be reduced by approximately a factor of 2 for every 10°C reduction in operating temperature for

die temperature operating condition between -20°C to 140°C. Hence, improving computer performance and reducing failure rates can be achieved when operating microprocessors at lower than room temperature [2], [3], [4]. Consequently, the application of refrigeration cooling was introduced to high-end computer and server systems in the mid-90s by IBM™. Sub-ambient cooling using refrigeration cycles or cryogenic cooling provides higher heat dissipation than conventional forced air convection or liquid-cooled methods. Unfortunately, it also requires higher operating pressure, higher power consumption, and larger envelope to accommodate pertinent components such as compressor, pump, radiator, valves, and interconnecting pipes. Moreover, dealing with individual component reliability, insulation, and corrosion from condensation inside the housing is also a challenging task for thermal engineers. Environmental issues such as noise and refrigerant leakage are also major concerns for liquid refrigeration cycles. Furthermore, for applications that required precision temperature control such as spot cooling of laser diodes or blood analyzers…, the steady state response times of these two sub-ambient cooling methods are much longer and less accurate because of temperature overshoot compared to solid state cooling. Lastly, miniaturization of refrigeration cycles or cryogenic cooling systems to be integrated directly on the processor has been difficult and has only been attempted at the laboratory level.

Solid state thermoelectric cooler is an excellent candidate for sub-ambient operating condition, which future active-powered systems are starving for with smaller packaging envelope, orientation independent, and no mechanical moving parts. Reliability is an issue with vapor compression cycles because of high operating pressure and mechanical moving parts, but thermoelectric cooler has a continuous service life recorded of more than 200,000 hours at normal steady state operating condition. Thermoelectric cooling technology operates without the assistant of working fluids such as CFCs (chlorofluorocarbons) and HCFCs (hydro-chlorofluorocarbons) or other materials, which may require periodic maintenance or

replacement and might be harmful to the environment when leakage occurs. In addition, thermoelectric coolers are capable of controlling temperature precision to within a fraction of a degree with minimal overshoot.

The Multidimensional Heat Transfer Systems (MHTS) presented in this study are designed to provide sub-ambient cooling and to rectify the problem of high power consumption, orientation dependency, mechanical reliability, precision temperature control, noise, weight, miniaturization capability, and environmental impacts of conventional sub-ambient cooling such as liquid refrigeration cooling or cryogenic cooling for three dimensional interconnects (3D-ICs).

The cost effective Multidimensional-Thermal-Cycling-System (MTCS) utilizing thermoelectric coolers for rapid assessment of 3D-IC reliability testing was also extracted from this concept to provide sub-ambient cooling and heating to both 1D and 3D-ICs or any three dimensional electronic components in general.

In addition, the MHTS and MTCS were designed with embedded-growth consideration of future Thermoelectric (TE) technologies, which means that as the 3D-ICs and solid state cooling technologies evolve, the MHTS and MTCS concepts and designs will not become obsolete. Affordability and weight are also major focuses implanted in these designs for industries specific such as medical equipment, hybrid automotive, cooling of commercial building, data centers, military aviation applications, etc…

CHAPTER 2

LITERATURE REVIEW

All passive heat dissipation technologies such as heat sink, heat pipes, heat sink assisted heat pipe, micro-channel, thermo-syphon… at theirs best can only bring an active-powered object down to its environmental temperature due to fan speed and acoustic limitations. Passive cooling devices often have a planner bottom surface thermally in contact with the entire top surface of an active-powered system such as a processor or a logic memory chip.

Thermacore Inc. developed a closed-loop thermo-syphon system (wicked-less heat pipes), which allows the working fluid to vaporize, and travels through a tube or banks of tubes, where heat is removed by conduction and then convection. Steam is then condensed back to saturated water downstream of the tube prior to returning to the hot region [5]. The concept of thermo-syphon was investigated in detail by Garner and Patel for many commercial electronic cooling applications [6]. Davidson and Bradshaw utilized the extremely high thermal conductivity property of nano diamond particles to improve the heat transfer of cooling fluid to cool transformers [7].

In addition to conventional heat removing techniques, the concept of solid state cooling was long discovered. In 1823, a German physicist Thomas Seebeck observed that a voltage was generated in a loop containing two dissimilar metals while subjected to a temperature difference. A decade later, a French scientist Jean Peltier found that as electrons move inside a conductor, they also carry heat from one side of the material to the other. When two materials are joined together, there exists a deficiency or excess in energy at the junction because the

two materials have different Peltier coefficients. The excess energy is released to the lattice at the junction, causing heating, and the deficiency in energy is supplied by the lattice, creating cooling. Chu et al. incorporated thermoelectric modules into a two-stage cooling system, where thermoelectric modules were used either to cool the object directly, or to cool the liquid, which is then used to cool the thermoelectric module indirectly [8].

In recent years, electronic and microelectronic industries started to adopt thermoelectric technology for more applications both in cooling and power generation due to the advancement in research and development of new thermoelectric materials and method of fabrications. Still, a broader use of thermoelectric cooling for high power applications is hampered due to the lack of low efficiency. The most well-known approach to resolve this deficiency is by improving the thermoelectric materials through doping of semiconductor materials. Countless studies by Venkatasubramanian [9], Harman [10], and others [11], [12], [13], and [14] have been done in this area and yielded almost double the efficiency of today's commercial Bi-Te (Telluride Bismuth) thermoelectric materials. A second methodology is to enhance the performance of solid-state energy converter through material processing [15]. Companies such as Hydrocool utilized auxiliary components and high thermal conductivity fluid systems to assist and improve thermoelectric modules performance [16]. The efforts invested in these studies result in an increase of about 30 percent in performance of cooling using thermoelectric in the past five decades. A third approach is to improve the performance of commercial TEC through thermal isolation. The thermodynamic principles of thermoelectric cooling are identical to vapor compression cycle, except the working fluid and compressors are replaced by electrons and direct electric current (DC) respectively. Such important concepts are often neglected or even ignored when it comes to design of a cooling system using thermoelectric modules. Earlier work by Fenton, et al [17] and later analyzed by Ghoshal [18] and Tada, et al [19] show some promises, but their researches are all theoretical and physical devices have actually not been

developed commercially. Nevertheless, each of these methods of cooling has its own advantages and limitations. Single mode of heat transfer alone cannot overcome modern thermal challenges; therefore, hybrid system should be the future path for sub-ambient cooling technology.

CHAPTER 3

SOLID STATE COOLING DESIGN AND THEORY

3.1 Introduction

Thermoelectric cooling and thermionic cooling are the only two commercialized alternative solid state cooling methods, which can provide sub-ambient cooling to microelectronic components compared to the conventional vapor compression cooling and cryogenic cooling. Vapor compression cooling and cryogenic cooling require large logistic footprints and are typically not suitable to use as precision spot cooling of microelectronic devices. With the latest breakthrough in nanotechnology, vapor compression cycle was miniaturized using nanotechnology in the laboratory with the intention to integrate the refrigeration cooling system directly on the processor. However, this technology is still at its infancy and the reliability of this technology remains to be proven. In this chapter, the theories and design of thermoelectric cooling and thermionic cooling along with their material evolution and device requirements are discussed.

3.1.1 Thermoelectric cooling theory and design

3.1.1.1 Thermoelectric cooling theory

Thermoelectric cooling is based upon the Peltier effect, which was discovered by Jean Peltier, a French scientist in the early 19th century. Peltier discovered that when a DC current passes through two dissimilar conductor materials connected in series, there exists a temperature differential at the junctions. Heat is being pumped out of the hot object in parallel through series of p and n semiconductor pellets connected in series. Electrons move from p-type to n-type semiconductor materials through an electrical conductor such as thin copper

pads. Electrons leap to higher energy state causes heat absorption phenomenon, which makes this side of the thermoelectric module becomes cold. Electrons continue to move through the lattice of the material from the n-type semiconductor back to the p-type semiconductor; this time the electrons drop down to a lower energy state and therefore, releasing energy in the form of heat to the heat sinks (hot side). By varying the electrical current provided to the thermoelectric module, different heat loads can be dissipated. Figure 3.1 illustrates a schematic of a pair of P-N type semiconductor thermoelectric cooler structure. Typically, a thermoelectric module contains hundreds of these P-N semiconductor pairs with the same size or mixtures of different sizes all mounted in series as shown in Fig. 3.2, and since they are made of semiconductor materials, thermoelectric coolers can be miniaturized easily using the same microprocessor fabrication techniques.

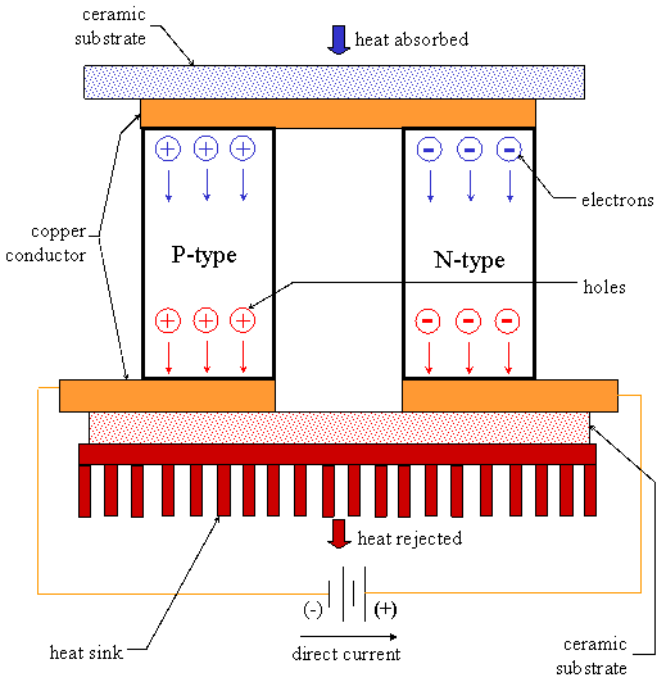


Figure 3.1 Thermoelectric cooling principle

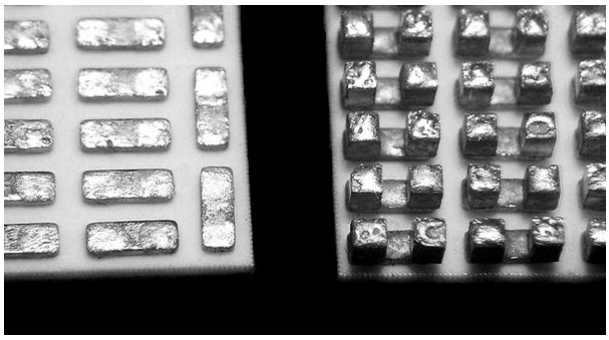


Figure 3.2 Inside structure of a thermoelectric module

Thermoelectric module can also be stacked (cascade thermoelectric modules) to handle higher heat flux. Depending on specific application, some thermoelectric module also equipped with environmental sealed as shown in Fig. 3.3 below:

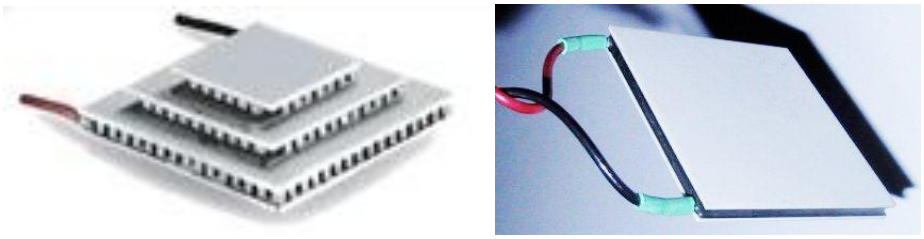


Figure 3.3 Cascade style thermoelectric module with environmental seal

Thermoelectric cooling is driven by three identified effects: the Seebeck effect, the Peltier effect and the Thomson effect. These effects were named after their founders: Thomas Seebeck, Jean Peltier and Lord William Thomson respectively between 1821 and 1855 [20].

3.1.1.2 The Seebeck effect

The concept of thermoelectric cooling started in 1823 when a German physicist, Thomas Seebeck, observed that a voltage was generated in a closed-loop containing two

dissimilar metals while subjected to a temperature difference. This phenomenon happened because each metal responds differently to the temperature gradient, which creates a current loop that produces a magnetic field. The Seebeck coefficient, *α*, is defined as the voltage generated per degree of temperature difference between two points as shown in schematic Fig. 3.4 and Eq. 1 :

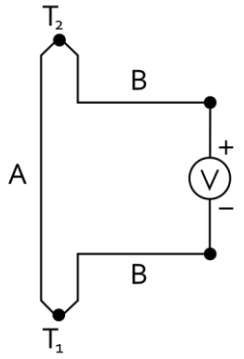


Figure 3.4 The Seebeck effect

$$\alpha = \frac{V_2 - V_1}{T_2 - T_1} \tag{1}$$

Today, one of the applications of the Seebeck effect is the thermocouples found in many temperature measuring devices. When two materials are jointed and the Seebeck coefficients of each materials are known, the temperature can be measured by measuring the Seebeck voltage differential. In a larger scale, the Seebeck effect is used as a thermoelectric power generator.

3.1.1.3 The Peltier effect

A decade later after Seebeck's discovery, in 1834 a French scientist named Jean-Charles Peltier discovered the calorific effect of an electric current at the junction of two dissimilar metals. Peltier found that as electrons move inside a conductor; they can also carry heat from one side of the material to the other. The heat current $Q_{Peltier}$, is proportional to the current, *I [A]*, and the Peltier coefficient, Π as shown in Eq. 2 below.

$$Q_{Peltier} = \Pi * I \tag{2}$$

In other word, the Peltier coefficient is defined as the difference of heat flow to current for a particular material. The Peltier coefficient represents the amount of heat current is transferred per unit charge across any given material. When two materials are joined together, there exists a deficiency or excess in the energy at the junction because the two materials have different Peltier coefficients. The excess energy is released to the lattice at the junction, causing heating, and the deficiency in energy is supplied by the lattice, creating cooling. The Seebeck and Peltier coefficients are closely related through the Thomson effect (Lord Kelvin) relation.

3.1.1.4 The Thomson effect

In 1851, William Thomson (Lord Kelvin) observed that for a given conductor when exposed to a temperature difference between two points, it will either absorb or emit heat, depending on the property of the material. The Thomson effect comprised of an irreversible Joule heating, ρJ^2, term and the Thomson heating term, $\mu J \frac{dT}{dx}$ as illustrated in Eq. 3:

$$Q = \rho J^2 \pm \mu J \frac{dT}{dx} \quad (3)$$

Where: Q *is* the heat production per unit volume *[W/m^3]*, ρ is the resistivity of the material *[Ω·m]*, $\frac{dT}{dx}$ is the temperature gradient along the material *[°C/m]*, μ is the Thomson coefficient. The second term is the Thomson heat, which changes sign when J changes direction.

Unlike the Seebeck and Peltier effects, which required a connection between two dissimilar materials in order to obtain relative coefficients; the Thomson effect is the only thermoelectric coefficient that can directly measure the absolute thermoelectric coefficient for individual material. However, the Seebeck coefficient is still the easiest one out of the three to measure. Hence, most material properties reported in the literature use Seebeck coefficient instead of Peltier or Thomson coefficients. In 1854, Lord Kelvin found the relationship between the Seebeck and Peltier effects as shown in Eq. 4, where T is the absolute temperature *[K]*; Π is the Peltier coefficient and α is the Seebeck coefficient *[V/K]:*

$$\Pi = \alpha T \quad (4)$$

3.1.1.5 Thermoelectric cooling design

Thermoelectric cooling design is a multidiscipline engineering project; it requires knowledge of mechanical engineering, electrical engineering, material science engineering, and manufacturing engineering. For any given material, it might conduct electricity or heat or both at different rate. For example, copper is an excellent electrical and thermal conductor, meanwhile glass can only conduct heat, but not electricity. Semiconductor material, however, is a material that conducts electricity intermediate between that of a conductor and an insulator.

Nevertheless, if a material allows electrons flow (i.e. electrically conductive), it will generate heat. This is called the Joule heating effect, also known as Ohmic heating or resistive heating, which was discovered in 1841 by James Prescott Joule. It is a process by which electrons while moving through a conductor, collides with the conductor lattices, which give off energy in the form of heat. Joule observed that the heat generated is proportional to the square of the current, *I [A],* multiplied by the electrical resistance, *R [Ω],* of the conductor as shown in Eq. 5:

$$Q_{Joule} = I^2 R \tag{5}$$

If a material is heated up due to electricity excitation, then the heat generated also must follow the second law of thermodynamic in the form of Fourier conduction. Heat always flows from a region of higher energy (hot) to a region of lower energy (cold). Heat is transferred by conduction when adjacent lattices vibrate against one another, or as electrons move from one atom to another. Thermal conductivity of a material is directly correlated to its density. As density of a material increases so does its conduction property. Therefore, metals are more thermally conductive compares to their counterpart fluids or gases. Joseph Fourier observed that the total heat transfer between two bodies is proportional to the thermal conductivity, *k [W/m·K]* of the medium multiply by cross-sectional area of the slab and the temperature gradient as illustrates in Eq. 6:

$$Q_{Fourier} = k A \frac{dT}{dx} \tag{6}$$

Finally, the total cooling power for a thermoelectric pair is the sum of Peltier cooling power (Eq. 2), Joule heating power (Eq. 5) and heat back flow from the hot side to the cold side - Fourier conduction power (Eq. 6) all together:

$$(Q_c)_{total} = Q_{Peltier} - Q_{Joule} - Q_{Fourier} \tag{7}$$

Substitute Eq. 2→6 to Eq. 7 to obtain Eq. 8 below:

$$(Q_c)_{total} = \alpha I T_c - \frac{1}{2} I^2 R - k A \frac{\Delta T}{L} \tag{8}$$

where: T_c is the temperature of the cold side *[K]*, electrical resistant $R = \rho \frac{x}{A}$, ρ is the electrical resistivity *[Ω·m]*, L is the length of the TE pellet *[m]*, and A is the cross-sectional area of the TE pellet *[m^2]*. In order to obtain the maximum cooling power or cooling temperature, an optimum current, I_{opt}, is required. This can be accomplished by taking the first derivative of Eq. 8 with respect to I, and set it equal to zero:

$$\frac{d(Q_c)_{total}}{dI} = 0 \quad \Rightarrow \quad I_{opt} = \frac{\alpha T_c A}{\rho L} \tag{9}$$

Now, the maximum cooling power, $Q_{c\text{-}max}$ can be obtained by substituting I_{opt} (Eq. 9) back to Eq. 8 for a set of ΔT to obtain:

$$(Q_c)_{max} = \frac{\alpha^2 T_c^2}{2R} - k A \frac{\Delta T}{L} = \frac{\alpha^2 T_c^2 A}{2 \rho L} - k A \frac{\Delta T}{L} = \frac{A}{L}\left(\frac{\alpha^2 T_c^2}{2 \rho} - k \Delta T\right) \tag{10}$$

From Eq. 10, it can be seen that the maximum temperature gradient between the hot and cold side of a thermoelectric module (ΔT_{max}) only occurs when $\Delta T_{max} = \frac{\alpha^2 T_c^2}{2 k R}$, and $\frac{\alpha^2}{2 k R}$ is strictly a material properties. The relationship $Z = \frac{\alpha^2}{k R}$ is called the thermoelectric figure of merit. Where Z has unit of inverse Kelvin [K^{-1}], and mostly appears as a product with the absolute temperature, T, (average device temperature). The dimensionless figure of merit, ZT, is often cited instead of Z. Material property is the essential factor in achieving higher figure of merit. Also from Eq. 10, it shows that the maximum cooling flux $\frac{(Q_c)_{max}}{A}$ is inversely proportional to the pellet length L, which also means that bulk thermoelectric cooler, is at a disadvantage in comparison to thin film micro coolers for higher cooling power density. From the figure of merit, it is noted that the maximum achievable cooling temperature only depends on the material properties, which means that the best candidate for thermoelectric material must be a perfect thermal insulator and a perfect electrical conductor at the same time.

Conventional thermoelectric module comprised of hundreds of P-N pellets. Equation 8 can be modified to reflect multiple thermoelectric pairs as follow:

The amount of heat Q_{te}, dissipated by a thermoelectric cooling module to perform the pumping action is given by:

$$Q_{te} = 2N(\frac{I^2 \rho}{G} + \alpha I \Delta T) \tag{11}$$

On the other hand, the heat pumping capacity Q_p of a thermoelectric module is given by:

$$Q_p = 2N(\alpha I T_c - \frac{I^2 \rho}{2G} - k\Delta TG) \quad (12)$$

where: *G* is the geometric factor, which is the cross sectional area per length $(\frac{A}{L})$ of each thermoelectric element [*m*], and *N* is the number of thermoelectric couples.

One conventional way to quantify the performance of a thermoelectric module is using the coefficient-of-performance (COP), which is the ratio of the heat pumped (Eq. 12) to the energy supplied to the thermoelectric cooler to perform the pumping work (Eq. 11) which yields:

$$COP = \frac{Q_p}{Q_{te}} \quad (13)$$

One of the methods to improve the coefficient of performance (*COP*) without altering the module physical integrity is to reduce the temperature differences (ΔT) between the hot and cold side of the thermoelectric module to a reasonable amount.

3.1.1.6 TE cooling optimization using thermal isolation

As mentioned in previous section, thermoelectric cooler operates exactly like a liquid refrigeration cycle, but instead of having a working fluid; electrons instead carry the heat, the DC current acts as the compressor, and the heat sink acts as a condenser. Inadequate thermal isolation is detrimental to both refrigeration cycle and thermoelectric cooler. Thermal leakage is analogous to trying to cool an object inside a household refrigerator with the door wide opened. The refrigerator is designed to cool a closed volume to a preset temperature inside. With the door wide opened, the volume needs to be cooled now is not the internal volume of refrigerator itself anymore, but the entire room for which the refrigerator is residing. The refrigerator now consumed much more power trying to pump the heat across an opened-volume. This problem

eventually causes the refrigerator compressor to fail because the preset temperature will never be reached, which causes the compressor to run continuously until mechanical breakdown occurs. The opened-refrigerator concept (i.e. thermal isolation principle) might seem obvious, but many commercial thermoelectric cooler products have been designed, fabricated, and sold without any insulation as seen in the following product (Fig. 3.5). One major problem with this design is the lack of insulation around the perimeter (i.e. the thickness) of the cold plate (heat spreader). The cold plate thickness is totally exposed to the hot surrounding without any insulation. In addition, this device will cause condensation in humid environment and does not utilize the thermoelectric module to its full capacity.

The cold plate has two important planar surfaces. The bottom surface is in contact with the processor, and the opposite side is in contact with the thermoelectric module. The rest of the unoccupied areas are exposed to the hot surrounding, which need to be insulated. The thermoelectric module primary function is to pump the heat from the processor below only, so without any side insulations around the perimeter of the cold plate, the thermoelectric module has to work extra hard to pump the heat generated by the processor and the heat recirculating from the heat sink above via the thickness of the cold plate. The cold plate or heat spreader cooling technology is used widely in passive cooling devices, where the entire cooling system is passive, so the cold plate actually helps to spread the heat out of the hot region. Conversely, in active cooling systems such as refrigeration cooling, or thermoelectric cooling…, if the heat spreader is not insulated, it actually will work against the direction of cooling because the thermoelectric cooler or refrigerator primary objective is to “pump” the heat away (i.e. reduced latent heat), not to spread the heat around.

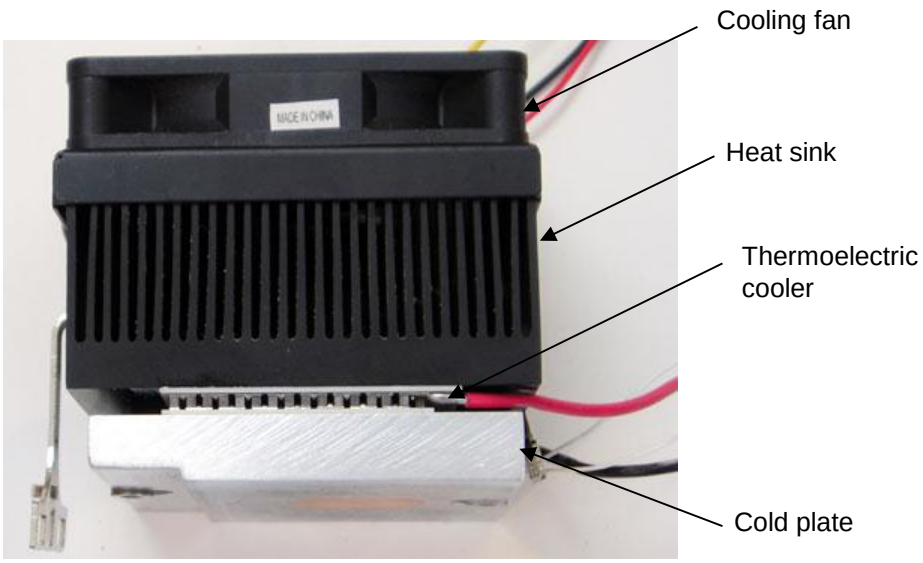


Figure 3.5 Faulty design of thermoelectric module incorporates with heat sink and cold plate

Another example of lack of insulation is illustrated in the following U.S. Patent by Novotny [21] below. The objective of this invention is to spot cooling a certain hot spot on the bottom surface using thermoelectric cooler. Using the same analogies, the areas immediately below the thermoelectric module(s) (item no. 58 on Fig. 3.6 (b) and (c)) are exposed to the hot environment (with air in Fig.3.6 (a) or with fluid in Fig.3.6 (b), (c)). The thermoelectric module has to pump the heat from both the hot spot and the unnecessary heat recirculating around the environment (air or fluid) adjacent to the extended fins for which the thermoelectric modules was mounted on. The thermoelectric module in this case might not be able to cool the targeted spot at all because of the extra heat invasion surrounding it.

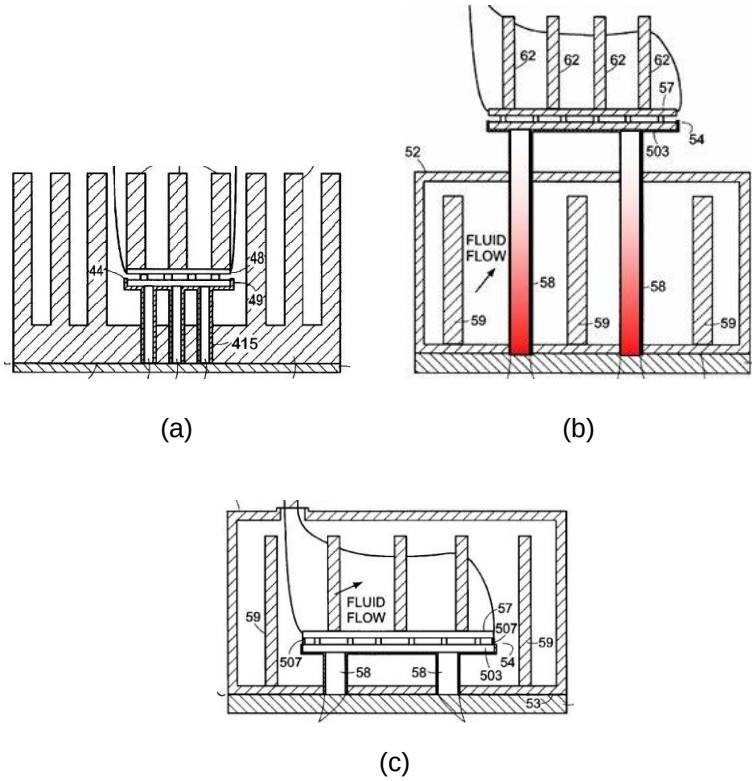


Figure 3.6 Spot cooling (a) in air, (b) outside fluid flow, (c) inside fluid flow environment.

Thermal isolation is one of the three methods that can improve the performance of a thermoelectric cooler. This can be achieved at the integration module level as discussed here or at the material physic and chemistry levels, which will be discussed in subsequence sections.

3.1.1.7 TE cooling utilizing material optimizing method

Another method to achieve higher heat pumping power is to optimize the figure of merit ZT. In order to accomplish this objective, a high Seebeck coefficient, a high electrical conductivity and a low thermal conductivity material must be found. Semiconductor material was found to be the material of choice because it has high mobility and it can be doped to high concentration, which yields higher electrical conductivity property. However, increasing in

doping concentration also reduces the Seebeck coefficient. According to Wiedermann-Franz law [22], the ratio of the electrons contribution to the thermal conductivity *k* and the electrical conductivity σ of a metal are proportional to the temperature ($\frac{k}{\sigma} = LT$), where *L* is the Lorenz number which is equal to (2.44 x 10^{-8} $W\Omega K^{-2}$). This means that through doping, the electrical conductivity is improved, but so does the thermal conductivity, which is undesirable for thermoelectric module design. Fortunately, thermoelectric materials which are heavily doped semiconductors with carrier concentrations on the order of ~10^{19}-10^{21} carriers/cm^3 can yield acceptable ZT. All of the relevant material properties depend on carrier concentration, as shown in Fig. 3.7, and an optimum carrier concentration exists for each material. It is noticed that at the lower carrier concentrations region, the electrical conductivity is too low, while at higher carrier concentrations, the material is so metallic the Seebeck coefficient becomes extremely low and the electronic component of thermal conductivity begins to dominate.

The interest of thermal and electric conversion phenomena was renewed during the 1950s when the discovery of doped semiconductors to be used in thermoelectric refrigeration [23]. Countless attempts have been done since then in the area of doping variety of materials at different concentration have been reported in the literature; however, Telluride Bismuth (Bi_2Te_3) with ZT about 1.0 at 300K is the most widely commercialized bulk material of choice for thermoelectric cooler. Unfortunately, for the past 60 years the bulk thermoelectric figure of merit is moving at snail-pace due to the lack of new bulk material discovery.

Meanwhile, in the early 20th century, superlattices were discovered, and thermoelectric engineers have utilized such discovery to achieve ZT of nearly 2.4 on p-type Bi_2Te_3/Sb_2Te_3 superlattice at room temperature [24]. This new technology helps scientists to reengineer materials at the quantum level to alter their thermal and electrical properties, which would be beneficial to thermoelectric material selection.

Since, the objective is to find the best possible thermoelectric materials that possess thermal properties similar to that of a glass and electrical properties similar to that of a perfect single crystal material (i.e. good electrical conductor and poor thermal conductor at the same time). Another branch of research that looks at a phonon-glass-electron-crystal material, which was originally researched by Slack [25] shows that a glass-like thermal conductivity coexists with high electron mobility, can be found in a crystals that has loosely bound atom scatters phonons. Skutterudites are members of a family of these phonon-glass-electron-crystal compounds, which exhibit a cage-like or open structure material. These open-structures allow atoms to be placed in the voids to reduce the material thermal conductivity while still maintaining the same electrical properties of that of semiconductor materials [26].

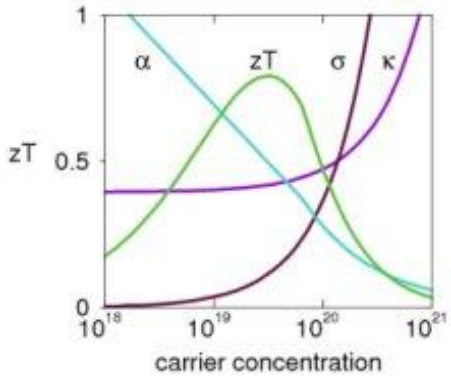


Figure 3.7 ZT as a function of carrier concentration for different α, σ, and κ

Quantum well is another technology that creates a quantum confinement of particles, which restraint particles from moving freely in three dimensions into two dimensions (2D), forcing them to occupy only in a planar region. Hicks and Dresselhaus suggested that ZT of certain materials could be improved by preparing them in quantum-well superlattice structures. Their calculation proved that layering highly anisotropic Bi_2Te_3 can enhance the thermoelectric performance provided that the superlattice multilayers are made in a particular orientation [27].

Quantum wire is another branch of condensed matter physics, which looks at quantum confinement of conduction electrons in the transverse direction (1D) of an electrically conducting wire. At the quantum level, classical formula for calculating electrical resistivity of an electrically conducting wire $R = \rho \frac{L}{A}$ is no longer valid; instead, an exact calculation of the transverse energies of the confined electrons has to be performed to calculate an electrically conducting wire's resistance. The reduction in macroscopic dimension of the 2D quantum well and 1D quantum wire increases the local density of the density of states near the Fermi energy band, which results in an increase of the Seebeck coefficient [28].

Quantum dots deal with 0D dimension systems and do not provide a conduction path, which reduces the Fourier's term significantly. Coupled quantum dots might provide adequate conduction paths for carriers but unfortunately less effective heat conduction paths for phonons. The study of quantum dots to be used for thermoelectric cooling applications has been entertained, but not yet fully understood by scientists, but it does offer an alternative and some promise for thermoelectric applications [29].

In 1998, Baladin and Wang [30] introduced the concept of phonon engineering, which opened another dimension for thermoelectric engineers to look at heat transfer of insulators and semiconductors through phonons manipulation. Spatial confinement of phonons in nanostructures can strongly affect phonons and electrons transport. Phonon confinement and boundary scattering can lead to significant decrease of the lattice thermal conductivity if semiconductor nanowires have lateral dimensions comparable to the acoustic phonon mean free path [31]. Along with these studies there are many other theoretical studies published in the literature with the attempt to improve ZT such as carrier pocket engineering, and or any combination thereof.

3.1.1.8 TE cooling optimization using current pulse method

Thermoelectric cooling load is a direct function of the input current; however, there exists a parabola-shape relationship between the input current to the optimum cooling power because as the input current continues to increase, the heat pumping power also continues to rise linearly until the Joule heating term become dominant; at which point, the Joule heating and the Fourier conduction terms will overcome the Peltier cooling term. If the input current continues to go higher, the thermoelectric module efficiency will start to decrease. This phenomenon happens at steady state, so what will happen if the input current is a step function instead of a linear function? Peltier cooling is a surface effect, which focuses at the cold junction, whereas, Joule heating is a volumetric effect and is dispersed throughout the entire volume of the TE pellet. In other words, Joule heating effect is time dependent compared to the Peltier cooling effect. This phenomenon was theoretically demonstrated by applying a high-current pulse after the minimum steady-state cold plate temperature has been established. Buist and Lau [32] demonstrated that the cold plate temperatures can be reduced by 16K below that via steady-state means.

3.1.2 Thermionic cooling theory and design

3.1.2.1 Thermionic cooling theory

Thermionic cooling is another encouraging sub-ambient cooling method. Thermionic cooling is also known as thermionic emission, which refers to any thermally excited charge emission process, when charge is emitted from one solid-state region into another due to thermal energy excitation under certain voltage bias. This occurs because the thermal energy given to the charge carriers is large enough to force the electrons to leave its carriers and jump between two electrodes over the potential barrier due to thermal excitation. After the emission

process, a charge will leave behind an electron hole in the emitting region, which creates cooling effect.

3.1.2.2 Thermionic cooling design

One of the challenges of classical thermionic emission is the operating temperature, which does not work well as a microelectronic cooling device at room temperature between the cathode vacuum structures. Recently 1997, Shakouri and Bowers proposed a thermionic devices based on semiconductor layered structures, which comprised of a, doped quantum wells separated by un-doped barriers heterostructure [33]. Heterostructure is much more ideal due to its smaller barrier gap between two layers or regions of dissimilar crystalline semiconductors, and since it belongs to the same semiconductor family as many microelectronic materials, integration of such heterostructure thermionic cooler into integrated circuits is also much easier than a cathode vacuum structure.

CHAPTER 4

3-DIMENSIONAL INTEGRATED CIRCUITS THERMAL CHALLENGES

4.1 Introduction

Dr. Gordon E. Moore of Intel™ made an astounding prediction in his 1965 paper that semiconductor transistor density would double roughly every 18 months [34]. Figure 4.1 illustrates what is referred to as Moore's Law.

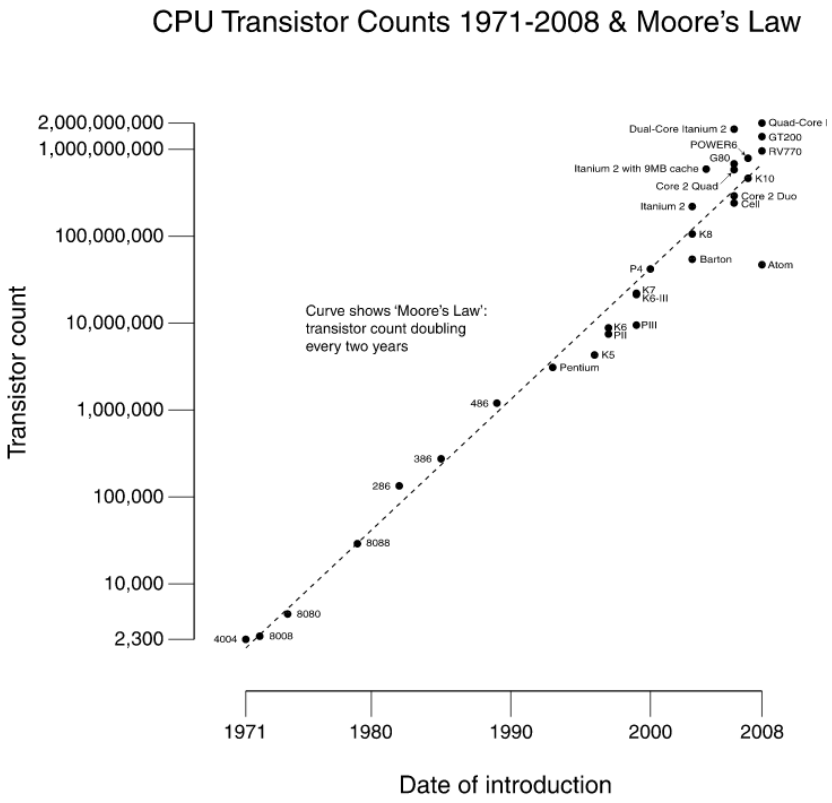


Figure 4.1 Moore's Law prediction for a period of 1971 to 2008

The microelectronic packaging industries have followed Moore's Law rather consistently until recently there have been discussions about a new "more than Moore's Law" trend. This new trend of nano packaging and much higher processing power, presents new thermal challenges to microprocessor thermal management community.

In order to keep pace with Moore's law, the transistor packaging technologies have evolved significantly as well from "Small-Scale-Integration" (SSI), which contains transistor numbering in the tens, to over hundreds as seen in "Medium-Scale-Integration" (MSI) in the late 1960s. With tremendous research and development in 1970s, the "Large-Scale-Integration" (LSI) was invented, with transistor in tens of thousands per processor. The development continued in 1980s with "Very-Large-Scale-Integration" (VLSI), which pushed hundreds of thousands of transistors in the early 1980s to several billions transistor at the end of 2009.

Not only did the number of transistors increased significantly, but also the method of packaging such devices have also evolved through the years. The early integrated circuits were packaged using ceramic substrates, which were pushed by the needs of the military; some applications today still use such technology. One of the first commercial packages was the dual in-line package (DIP); however, this technology was quickly replaced with the pin grid array (PGA) and leadless processor carrier (LCC) because DIP could not handle the increased in the number of pin counts in the 1980s. During this time, due to the increase in the number of pin counts, the lead pitch also had to be reduced, so by the late 1980s, the surface mount packaging technology such as the pin grid array (PGA) became popular and eventually replaced the gull-wing and J-lead structures.

The electronic packaging technology took a major leap during the 1990s, with many new and improved packages that can handle higher pin counts such as the small-outline integrated circuit (SOIC), plastic quad flat package (PQFP), plastic leaded processor carrier

(PLCC), thin small-outline package (TSOP)… Figure 4.2 below illustrates the evolution of many types of packages over the years.

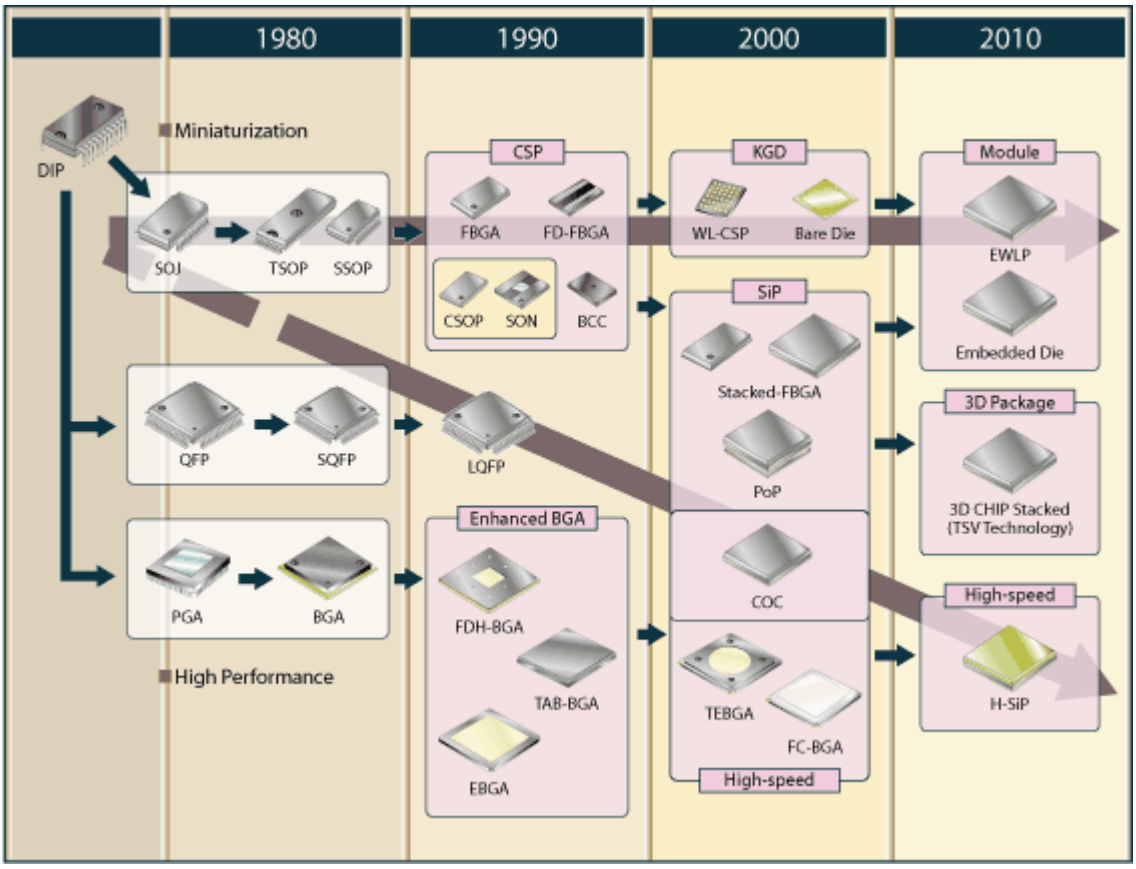


Figure 4.2 Electronic packages evolution (courtesy of Fujitsu Corporation)

As illustrated in Fig. 4.2, the ball grid array (BGA) packages were born early in the evolution of processor packaging, but quickly the flip-processor ball grid array (FCBGA) packages, which allow for much higher pin counts, took over during the 1990s. The difference between the non-flips vs. the flip-processor is the die is mounted upside-down and bonds to the package via solder balls instead of wires bonding. FCBGA package is an area input/output distribution, instead of peripherals distribution compared to other packages.

Prior to 2000s, most integrated circuits functions were unique, which means that if the device was designed as a memory module then the entire IC will be dedicated for memory logic only. The concept of system on a processor (SOP) and system in package (SiP) were invented with the intention to package more functionality into one device.

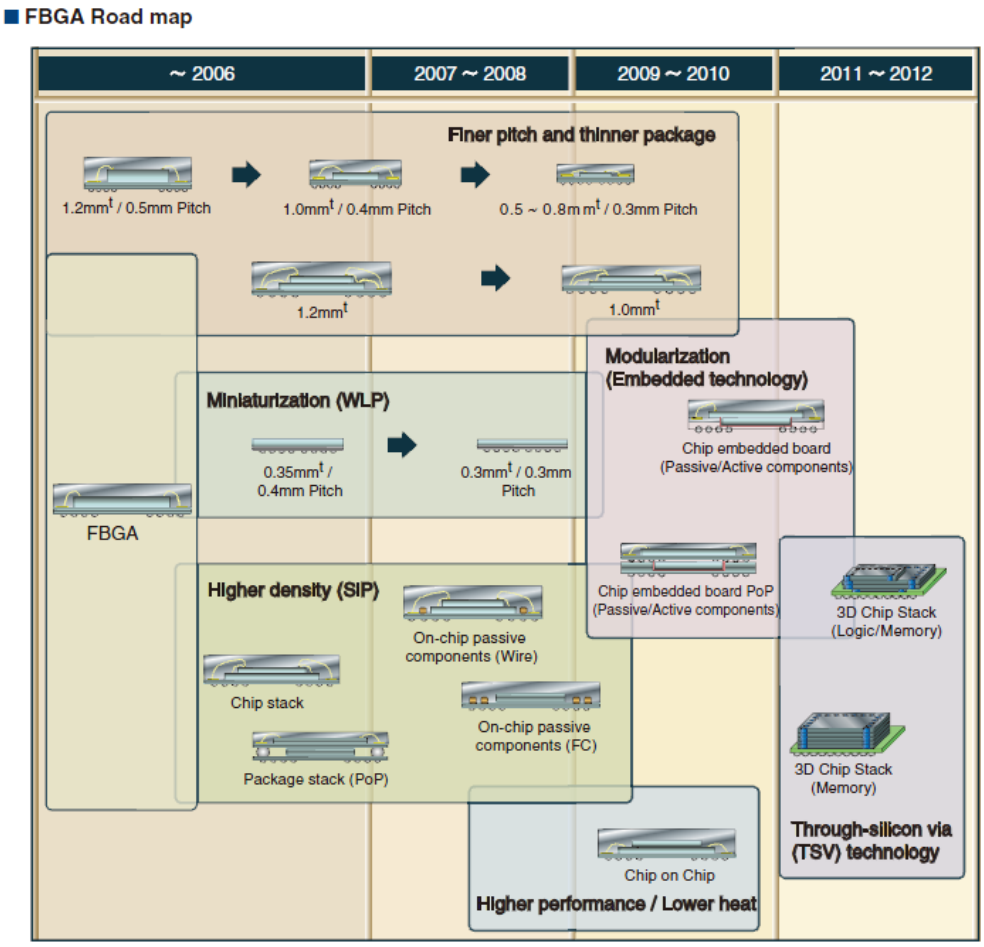


Figure 4.3 FBGA packaging road map (*courtesy of Fujitsu Corporation*)

Recently, the idea of 3D-IC is a processor with two or more layers of active powered electronic components are integrated in multidirectional structures into one single circuit has shown lot of promises to reduce interconnecting length, and increase in processing speed. 3D-

IC required different method of signal and wires routing. As shown in Fig. 4.3, the wire pitch has become smaller and smaller as time goes on. The future of microelectronic packaging lies in the area of 3D packaging. As of right now, thru-silicon via (TSV) technology is considered one of the methods of choice for routing signals in 3D packaging.

4.1.1 Thermal management of 1-D packages

Since the beginning, all integrated circuit normally would have planner top surface as shown in Fig. 4.4, which is designed to interface with a cooling device such as: a heat sink or a heat spreader and a fan. Passive cooling using a heat sink and a fan is considered adequate for earlier packages due to lower heat dissipation.

Many researches have been done to improve heat dissipation of 1D-IC since 1970s. Depending on the application, different method of cooling was used; for instance, in military application, phase-change material cooling for missiles was the method of choice because it doesn't require a metal heat sink, fan and extra power to operate, which might add undesirable weight to an airborne system. Nanofluid is another alternative used to enhance the conductivity and convective heat transfer coefficient compared to a straight coolant [35], [36]. Nanofluid is a fluid containing nanometer-sized particles, which were engineered from colloidal suspensions of nanoparticles in a base coolant.

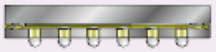
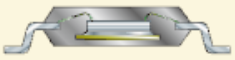
	Package type	Package structure	Pin count	I/O frequency (GHz)	Heat resistance θja(°C /W) (0m/s)	Application
High-end	FC-CBGA		450~2116	~5	7~	Routers, Servers, Workstations, Backbone transmission devices
	FC-PBGA		450~2116	~2.5	7~	
	FC-PBGA		450~1156	~2.5	9~	Routers, Personal computers, Graphics, Digital TVs, Set top boxes, Ink-jet printers
	TEBGA		256~1156	~1.6	13~	
	PBGA		256~1156	~1.6	15~	
Consumer appliances	FBGA		66~906	~1	25~40	Personal computers, Mobile phones, Digital video cameras, Digital still cameras, PDAs
	WL-CSP		42~195	~2.5	25~60	Mobile phones, Digital video cameras, Digital still cameras, PDAs
	QFP LQFP		48~304	~2.5	15~100	Personal computers, Digital TV, Set top boxes, Ink-jet printers

Figure 4.4 Anatomy of different type of packages (*courtesy of Fujitsu Corporation*)

Micro-channel is another promising method used to cool microelectronics. This technology required sophisticate manufacturing technique because in order to be classified as micro-channel, the hydraulic diameter of the channel must be less than 1mm. This technology also has drawbacks such as the high differential operating pressure in an ultra-thin and fragile wafer environment and coolant leakage potential. Microprocessor manufacturers have not seriously considered micro-channel technology because the wafer thickness is getting thinner and the probability of incorporating a microchannel on the back side of the wafer might create a reliability problem; therefore, micro-channel technology has only been entertained at the academic level.

4.1.2 Thermal management of 3D package

The future trend of 3D microelectronic packaging is embedded electronic components on a single die as shown in Fig. 4.5.

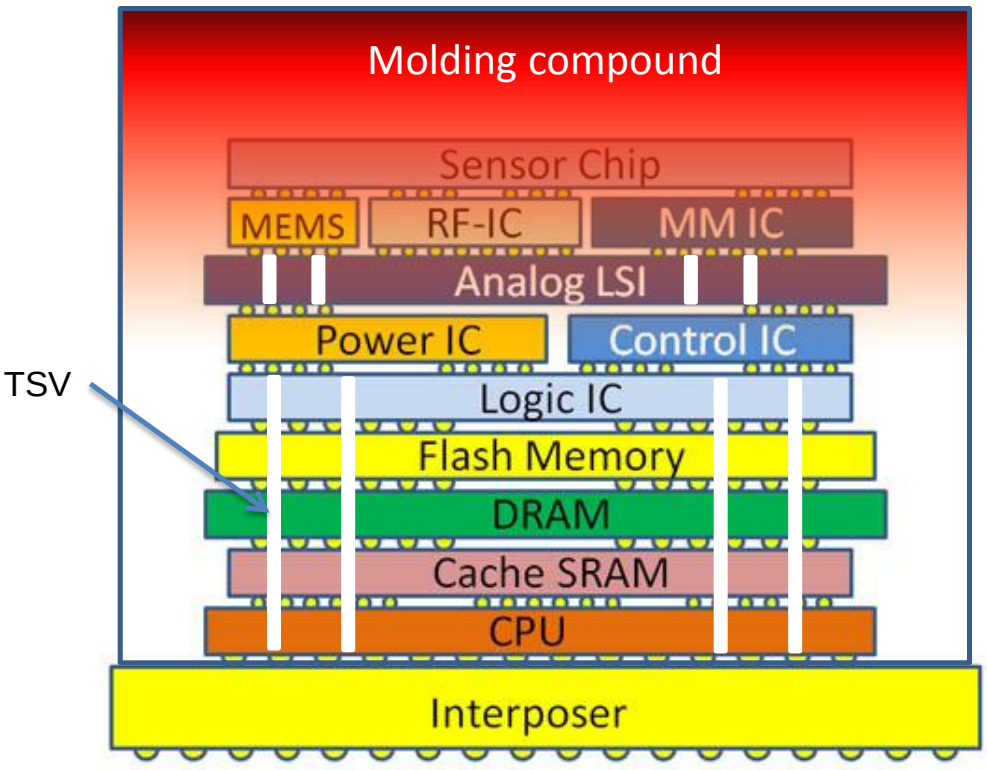


Figure 4.5 3D stack package anatomy

There are many advantages to this concept. First of all, it reduces the footprint significantly by utilizing the vertical dimension. It can add more functionality into a small space. Second, it reduces the interconnecting wires tremendously, because propagation delay is proportional to the square of the wire length; therefore, reducing the interconnect wire length will increase the overall performance. It is also unclear whether CMOS circuit can handle gates less than 32nm in the future, so stacking of system is more logical. Third, the reduction in wire length also saves on power consumption and reduces the Joule heating. Fourth, utilizing the

third dimension allows IC packaging engineers to explore many more design possibilities. And lastly, increasing in bandwidth can be accomplished by exploring the third dimension integration, which allows construction of wider bandwidth buses between functional blocks in different layers [37].

Unfortunately, 3D packages also have many disadvantages yet to be rectified. The intricate design of 3D packaging would add more cost to the overall package. Each layer has its own cost of fabrication and the layer interface cost is added when each layer is integrated with each other. The known-good-die (KGD) problem is also intensified because the risk of defects is much higher, and the repair cost will be much higher as well. The complexity of the 3D design requires more complex planning and new layout CAD software to address the 3D paradigm. Lastly, the most important problem is managing the thermal stack up within the 3D-IC architecture. Each layer in the 3D package generates certain amount of heat. In 1D package, the heat generated by the single processor has two conduction paths – down to the board via electrical wires and through the top via a heat sink. In 3D package, the bottom layer experiences the heat flux generated from the top packages and the heat flux generated by itself. The heat continues to stack up until it reaches the top layer, but unfortunately the molding compound thermal conductivity is only, k = 0.67 W/m-°C, which acts more like an insulator rather than a thermal conductor.

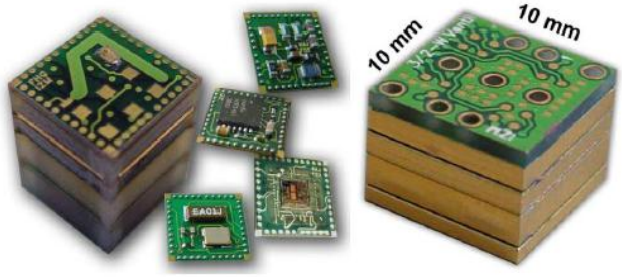


Figure 4.6 Low-power high-integration 3D-PCB-package (10x10x10 mm^3) [39].

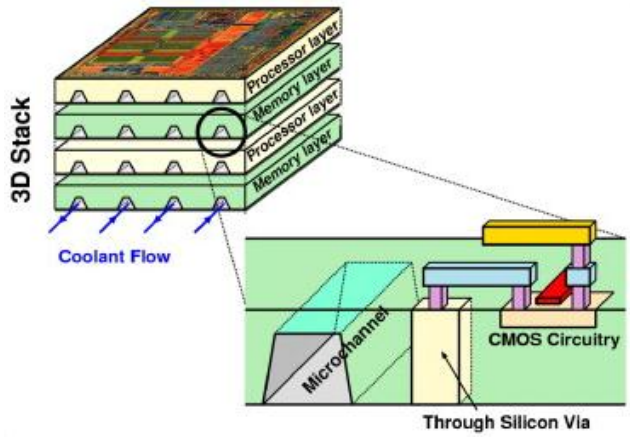


Figure 4.7 Cooling of 3D stack systems-on-processor using micro-channel [40].

Nevertheless, this thermal issue is only a temporary challenge and is not viewed as a technology road block because many studies have been done to improve the heat dissipation of 3D-IC. One such study lies in the area of thru-silicon-via (TSV), which is the first step to establish a heat flow path within a complex three-dimensional thermal and electrical architecture. Hon et al. detailed a fabrication process to build a multi-stack flip processor 3D packaging utilizing copper plated TSVs [38]. Even though, TSV studies were geared toward signal routing for 3D-IC structures, it also has potentials to rectify the heat buildup inside a 3D structure as well. Figure 4.6 illustrates the 3D-PCB package with water cooling developed by Schindler-Saefkow, et al. [39] using hollow TSVs to route fluid through the 3D-PCB or a micro-channel cooling of 3D systems-on-processor as researched by Valle and Atienza [40] as shown in Fig. 4.7. There are many researches done in this area to cool multiple systems-on-processor. Clearly, hollow thermal TSV, which carried coolant fluid inside an electrical sensitive environment are complex; in addition, coolant leakage in this type of system might potentially be a bigger problem. Furthermore, these studies are primarily concentrated at the processor-level thermal management. Beyond the processor-level, sub- ambient cooling of such 3D

architecture using solid state cooling technologies has not been widely investigated and reported thoroughly in the literature.

CHAPTER 5

THERMOELECTRIC COOLING SYSTEM INTEGRATION

5.1 Introduction

In chapter 3, it was shown that there are many macro/micro theoretical and empirical approaches to improve thermoelectric cooler performance. After all, if one such finding is successfully commercialized, the next questions would be: what would the cooling module look like and how would it integrate with the current cooling or future cooling system as a whole to cool 3D active-powered devices from a practical stand point? In this chapter, current cooling technologies integration utilizing thermoelectric cooler will be assessed.

5.1.1 Direct thermoelectric module system integration

Figure 5.1 below illustrates the difference between passive and active cooling methods for conventional 1D-ICs applications.

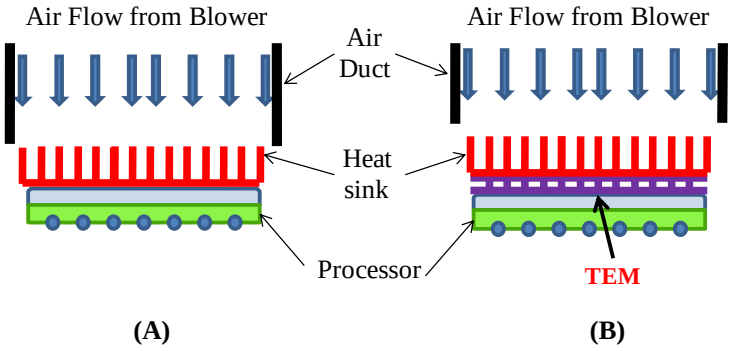


Figure 5.1 (A) passive cooling, (B) active cooling using TEC for conventional 1D-ICs.

The only difference between passive and active solid-state cooling is the utilization of a thermoelectric module (TEM) sandwiched between the processor and the passive or active heat sink.

Real estate reserved for CPU cooling inside a computer or server is horizontally challenged. In other word, the area permitted for cooling is just right above the processor because of other components occupied the surrounding areas of the motherboard (Fig. 5.2).

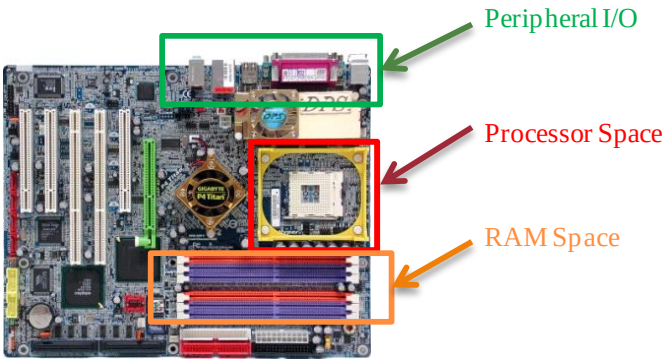


Figure 5.2 Pentium™ IV motherboard (*courtesy of Gigabyte Corporation*)

One other potential problem with local sub-ambient cooling of 3D-ICs is a slim probability of packaging a small sub-ambient cooling device or system in a tight real estate available on the motherboard dedicated to the processor and its cooling apparatus such as a heat sink and a fan. The higher the processing power, the larger the thermoelectric module must be, which leads to larger horizontal heat-sink footprint requirement. As a rule of thumb, the passive heat sink used in thermoelectric cooling is at least twice the size of the TEM in order to accommodate the heat generated by both the TEM and the processor. The growth in horizontal heat sink size will over shadow other area on the motherboard such as RAMs space and external peripheral I/O connections as illustrated in Fig. 5.2. If more than one thermoelectric were used to achieve the desired cooling target, the temperature of the processor might be

lower, but conventionally only two of the same size thermoelectric modules can be stacked at once. In the cascade-style structure as shown in Fig. 5.3 below several smaller sizes of thermoelectric modules can be stacked on top of each other, but the heat sink size will have to be double or even quadruple in size in order to handle higher heat flux output resulting from the thermoelectric power stacked up.

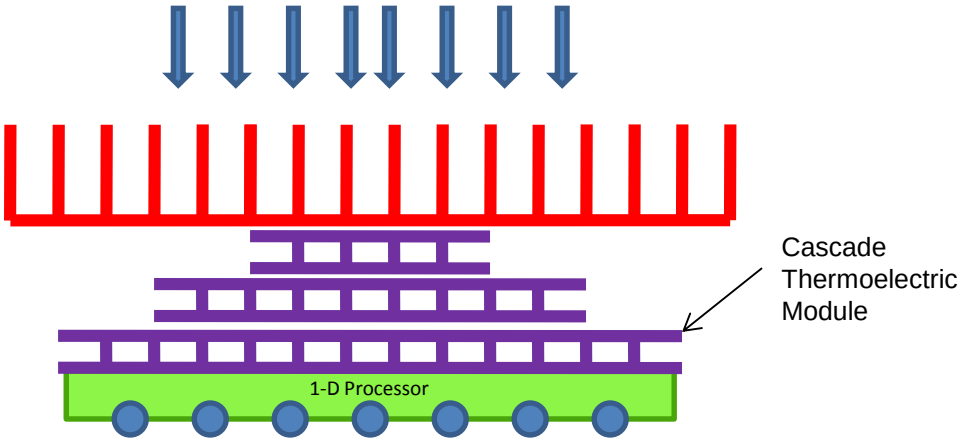


Figure 5.3 Unidirectional cascade thermoelectric cooling configuration for 1D processor

Cascading thermoelectric modules could also create a structural stability problem for high vibration applications and still not rectified the problem of larger heat sink and fan horizontal footprint. Simons et al. [41] assessed cooling of Multi-Chip-Module (MCM) using single stage and one-dimensional thermoelectric modules, but the study concluded that thermoelectric will not be a serious candidate for high performance electronic cooling application.

As the package continue to grow in the third dimension, the thermal problem intensified with 3D packages because of the thermal leakage coming from the side of the package. As mentioned in previous section, thermoelectric cooling is a heat pump; therefore, any un-insulated surfaces around the processor will provide an opportunity for heat to recirculate from

the hot surrounding environment or from the heat sink above back into the thermoelectric module. Regardless of how many cascade thermoelectric module is used, as the processor grows vertically, current cooling scheme using thermoelectric module in a one-dimensional direction will not provide any added value (Fig. 5.4).

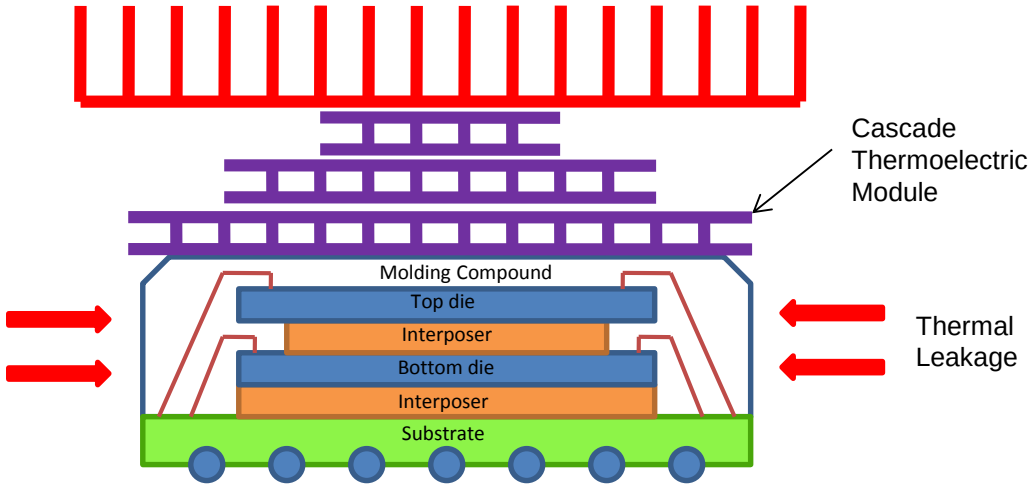


Figure 5.4 Cascade thermoelectric cooling attachment for 3D-IC

5.1.2 Unidirectional vs. multidirectional heat transfer

Most certainly, microprocessor heat flux is non-uniform and multidirectional due to the transistor packing density and the electrical layout. Cascading thermoelectric modules to handle higher heat load is somewhat considered as a one-dimensional conduction cooling method still. One principle must not be forgotten is that heat conduction is non-unidirectional, and heat diffuses in all directions in a thermal conductor. In addition, heat will flow spontaneously and irreversibly from region of higher energy state (hot) to lower energy state (cold) (second law of thermodynamic). Heat always chooses to travel down the path of least resistant. A classic example of these laws is illustrated in a schematic Fig. 5.5 below of an extended surface heat sink.

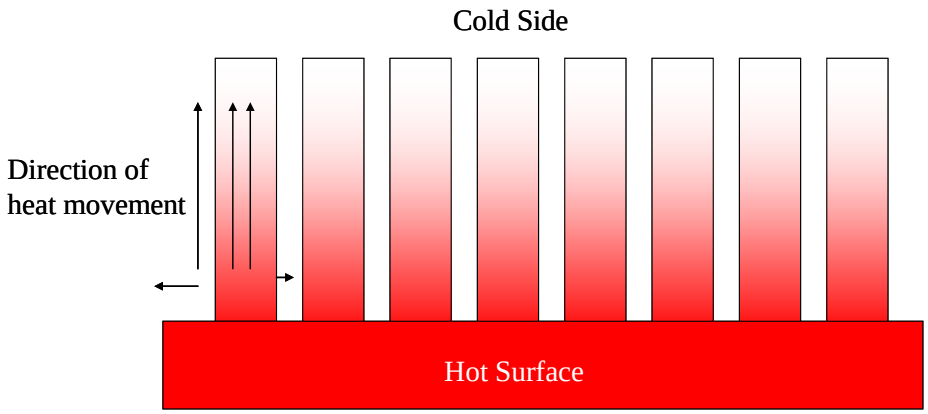
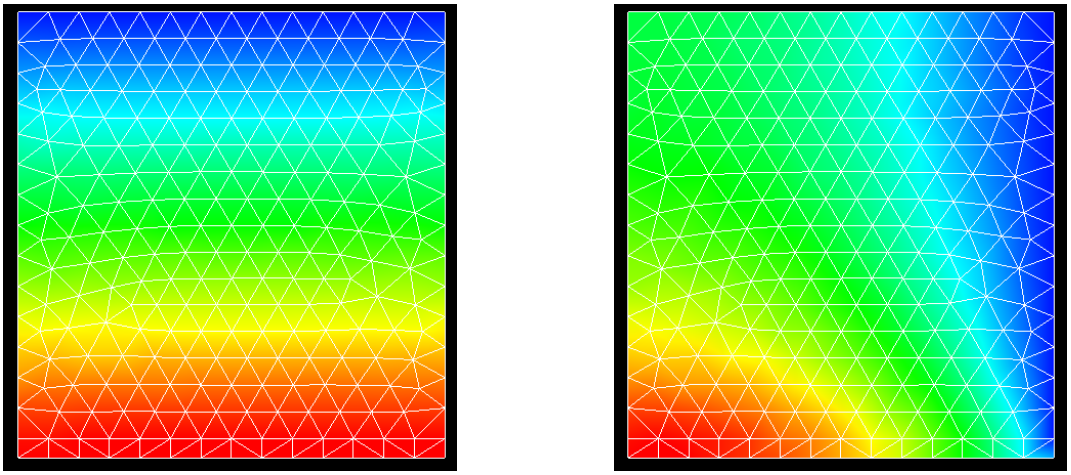


Figure 5.5 Classical extended surface heat conduction



(A)
TEC Top Attached
TEC temperature: 20°C
Chip temperature: 27.28°C

(B)
TEC Side Attached
TEC temperature: 20°C
Chip Temperature: 25.83°C

Figure 5.6 Differential temperature seen in (A) top attachment and (B) side attachment of TEC

It is observed that heat is transferred in all directions around each fin. Heat escaped the hot surface through series of fins by conduction first then convection next. The hottest region of the extended surface is exhibited at the bottom of the fins regardless of how cold the

tip of the fins might be or how tall the fins might be. Heat does not wait and orderly depart the hot surface toward the tip of the fin just because that is a cooler region, but instead heat is transfer immediately all around the fin starting from the bottom of those fins. Therefore, in order to pump the heat away from the hot surface fast and effective, the heat should be removed in all directions and toward the bottom of the fins. Figure 5.6 illustrates a reduction of 1.45°C cooler by just attaching TEC on the side versus the top of the fin. This principle is the building block for the Multidimensional Heat Transfer Systems (MHTS) design, which will be discussed in the next chapter.

CHAPTER 6

MULTIDIMENSIONAL HEAT TRANSFER SYSTEM THEORY & DESIGN

6.1 Introduction

By knowing the imperfections of commercials products and issued patents associated with cooling technology using thermoelectric coolers, a Multidimensional Heat Transfer Systems (MHTS) was designed and investigated. MHTS can be design for high and low heat flux depending on different applications. Both designs shared the same core principles, but for higher heat flux system, it is required that additional hybrid systems must be used in conjunction with the MHTS to achieve higher cooling power. The tested system is a completely solid state system, no liquid or mechanical moving parts required except for the fan to provide forced air convection. The second systems operate in the same principle, but in addition to the solid-state cooling part, a parallel system of heat pipes and liquid-cooled chiller using different amount of nano particles composition to enhance the heat transfer were filed with the U.S Patents office and will be investigated further in the future. In this chapter, the experimental and Computational-Fluid-Dynamic (CFD) of the Multidimensional-Heat-Transfer-System (MHTS) were investigated [42].

6.1.1 Solid-state Multidimensional-Heat-Transfer-System (MHTS)

A solid-state MHTS comprised of thermoelectric modules, a cold core, heat sinks and a fan. To ensure maximum heat transfer and cost effective, copper C11000 material were used instead of oxygen-free copper (C10200) to fabricate the cold core. The thermal conductivity of C11000 is about the same as oxygen-free copper C10200 in the range of 388 to 391 *[W/m·K]*, but for half of the cost. Oxygen-free copper primarily used in electrical resistance sensitive

components, which is not the case for the cold core. The cold core represents the inside volume of a household refrigerator. Instead of cooling the air inside the fridge, the thermoelectric modules are going to cool a solid thermal conductive copper block. The cold core has a planar bottom surface thermally in contact directly with the microprocessor. The surface in contact with the active powered device is recessed to ensure that the 3D-IC thickness is embedded and unexposed for thermal isolation purposes. Figure 6.1 illustrates a few examples of the custom to fit shapes of the internal volume of the cold core.

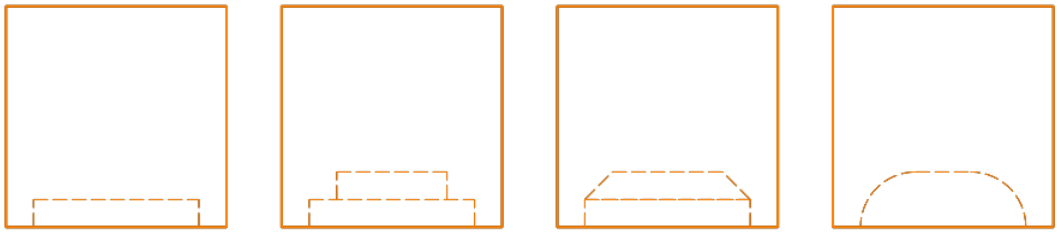


Figure 6.1 Example of cold core internal volume shapes

Single or multiple levels of recesses can be implemented to conform to specific application such as stack-processors or processor with different molding compound shapes. The recess might be small or large depending on the type of processor. Some manufactures preferred to have an Integrated-Heat-Spreader (IHS) on top of the processor some might not. Therefore, the cold core design will be unique for different processor makers. For processor without IHS, any exposed areas will be tapped off with an insulated foam tape to prevent thermal leakage as discussed previously.

The cross sectional area of the cold core can be any shapes as suggested in Fig. 6.2 depending on the applications and the real estate availability. The vertical dimension of the cold core can also be extended to any height or tapper or variable cross sections or any combination thereof to fit certain requirements. The cold core can be made out of different heat conducting

materials such as but not limited to copper, aluminum, stainless steel, graphite… Graphite heat spreader is an anisotropic material, which exhibits a high thermal conductivity in the plane of the sheet compares to a much lower thermal conductivity through the thickness of the material [43]. Graphite material would be an excellent material to be used for the cold core because of its weight to thermal conductivity ratio compared to solid copper or aluminum. Table 6.1 illustrates the comparison between copper, aluminum and graphite heat spreaders. Graphite can also be easily formed into different shapes, different contour; therefore, it might be used in lieu of copper for weight sensitive applications like aviation or automotive systems or flexible thermoelectric coolers. A hybrid cold core could be used such as copper core assisted with graphite as shown in Fig. 6.3 below to reduce the weight of a solid copper core while still maintain comparable horizontal heat transfer capability.

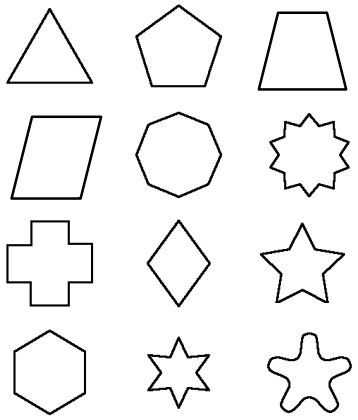


Figure 6.2 Suggested cross sectional area shapes of the cold core

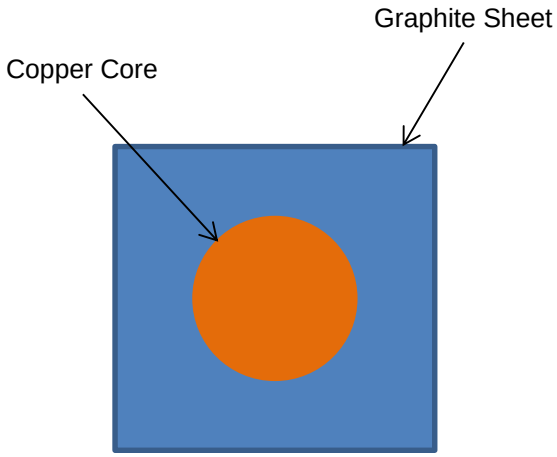


Figure 6.3 Hybrid cold core with copper center core and graphite sheet extension

Table 6.1 Thermal Properties of Heat Spreader Materials.

Property	Direction	Natural Graphite Sheet	Aluminum 1100 Alloy	Copper 11000 Alloy
Density *[g/cm^3]*	All	1.1 – 1.7	2.71	8.89
Thermal Conductivity *[W/m·K]*	X,Y	140 – 500	220	388
Thermal Conductivity *[W/m·K]*	Z	3 – 10	220	388
Specific Heat Capacity *[J/kg·K]*		846	904	385

Attaching the processor to the cold core recess area requires that the two solid surfaces must be intimately in contact to each other to reduce interface thermal resistant. Unfortunately, no matter how well prepared the machining process might be, the machined surfaces will never be perfectly flat or smooth enough to permit intimate contact. All surfaces will have a certain

roughness due to microscopic imperfections. These imperfections created air-filled gaps (hills and valleys), which allow only heat transfer through the actual contacted area. A flatness of 0.001 in/in or better is recommended for satisfactory thermal performance and it may be necessary to perform an additional lapping, fly-cutting, or grinding operation to meet this flatness specification. To rectify this problem, the surface of the recess in contact with the processor or the IHS is polished by rotary tools and by hands using number 400 to 1500 grits ultra-fine dry/wet diamond sand paper and polishing compound to achieve flatness between the two surfaces to minimize the interface resistant.

To ensure proper contact between the cold core and the processor, a nano-silver particles thermal adhesive compound produced by Arctic Silver Incorporated, Visalia, CA, was used to bond the processor to the cold core. The compound comprised of 99.8 percent pure nano size silver particles with less than 0.49 microns in spherical and non-spherical size to guarantee that any imperfections left over will also be filled. The thermal conductance of this compound is greater than 350,000 *[W/m^2·°C]* per 0.001 inch layer and the temperature range is between -50°C to greater than 130°C.

The shape of the cold core tested was a perfect cube. The bottom facet of the cube is occupied by the processor and each peripheral facet of the cube is interfaced with one thermoelectric module. As a rule of thumb, the cold core dimension should be the same exact size as the thermoelectric module; this design will ensure that the core is completely enclosed by the thermoelectric modules to prevent any thermal leakage from happening. A processor simulator (i.e. heater) (CBR-150 made by Component General, Inc. Odessa, FL) was used to simulate different heat load. The heater dimensions tested were 9.53x6.35x1.97mm^3, which has a maximum rated power of 150W. The solid state heater has a planar polished silicon surface, so it does not require polishing. Figure 6.4 shows the MHTS configuration with four thermoelectric modules attachment, and Fig. 6.5 illustrate a five thermoelectric modules

configuration. Any opened surfaces, which are not occupied by the thermoelectric modules or the processor, were thermally insulated using foam tape or polyurethane injection foam. Prior to thermoelectric module attachment, the surfaces of the copper cold core were polished using the same procedure stated above, and cleaned with surfactant and isopropyl alcohol to ensure that the cold core is free from foreign particles or oil residues left over from the polishing compound or fingerprints, which might interfere with the nano silver epoxy adhesive and the heat transfer of the system.

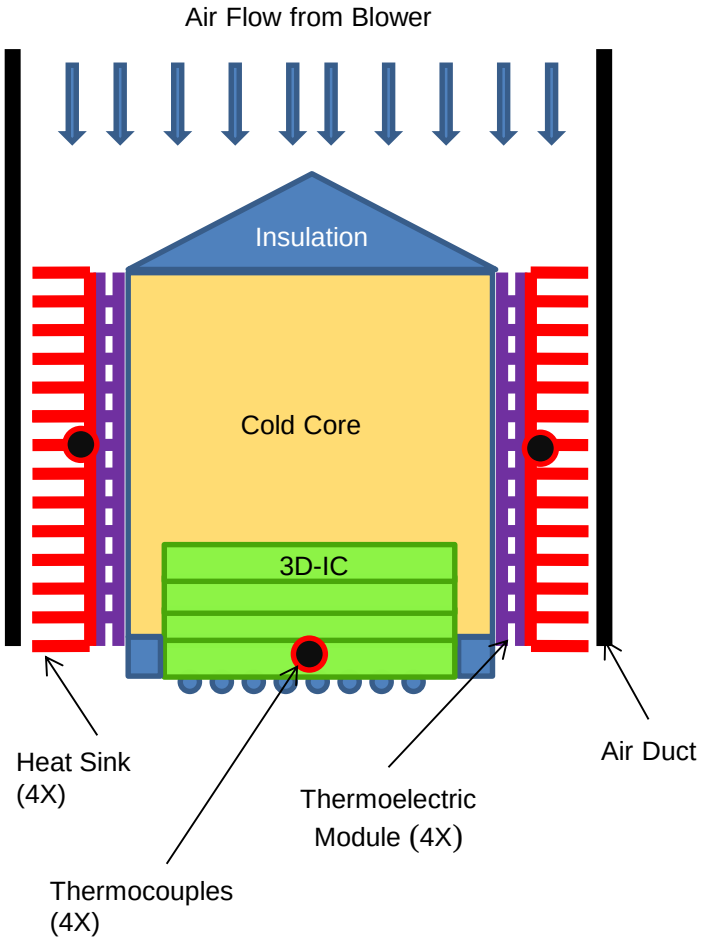


Figure 6.4 The schematic of the Multidimensional-Heat-Transfer-System using 4 TECs

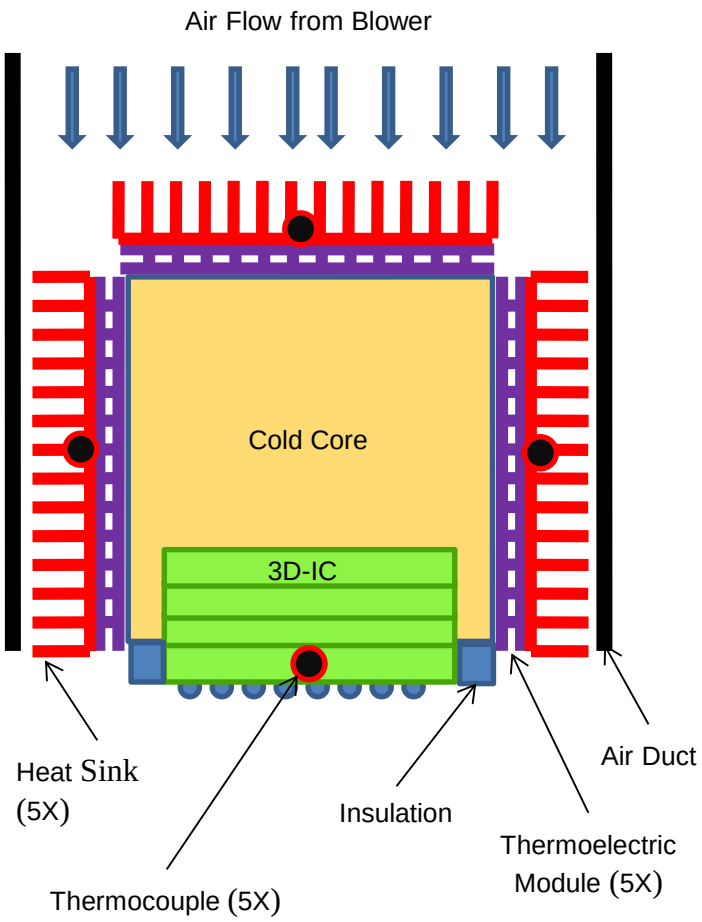


Figure 6.5 The schematic of the Multidimensional-Heat-Transfer-System using 5 TECs

Depending on the application, non-metallic screws can be used to constraint the heat sink and the thermoelectric modules to prevent delamination due to high vibration. If graphite core was used, a non-metallic mounting system could be formed within the graphite structure during the core formation process as shown in Fig. 6.6.

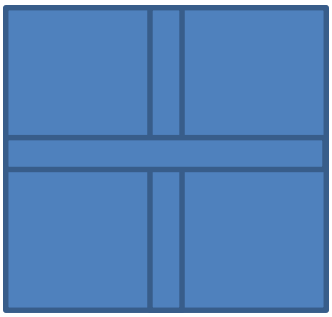


Figure 6.6 Nonmetallic threaded tubes system embedded inside a graphite core

Conventionally, the thermoelectric module is mounted in the middle of the heat sink as shown in Fig. 6.7.

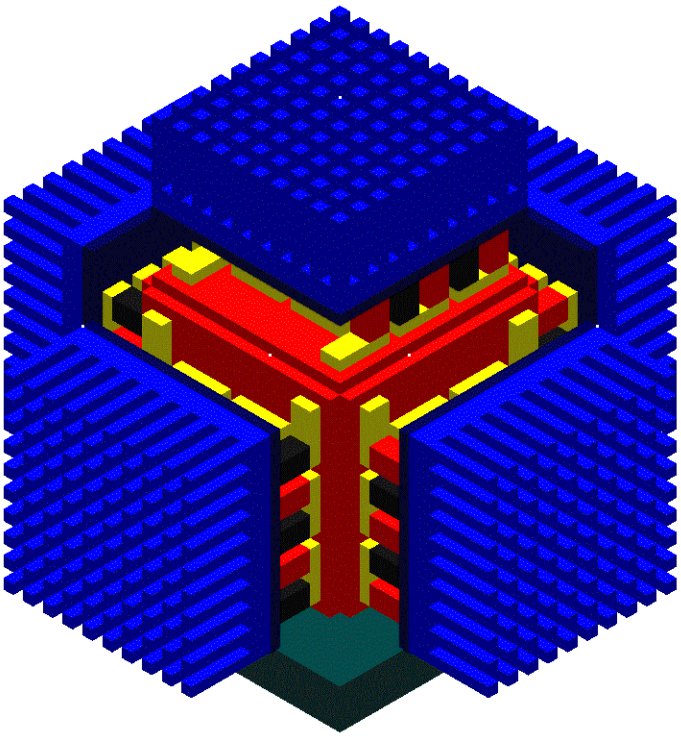


Figure 6.7 Conventional heat sink mounting configuration

In reality, the heat sink size is always going to be much larger than the thermoelectric module size in order to accommodate for the combine heat flux of both the hot object and the heat generated by the TEC, so if the center of the heat sink is coincided with the center of the thermoelectric module, interfere between the adjacent heat sink will occurs. To rectify this problem, the heat sink in the MHTS is mounted with an offset configuration as shown in Fig. 6.8. The offset configuration allows the heat sink to grow horizontally and vertically without any interference to the adjacent heat sink. The best heat sink candidate for the MHTS would be the heat pipe assisted heat sink or vapor chamber; where the heat pipe or vapor chamber section is in direct contact with the thermoelectric module.

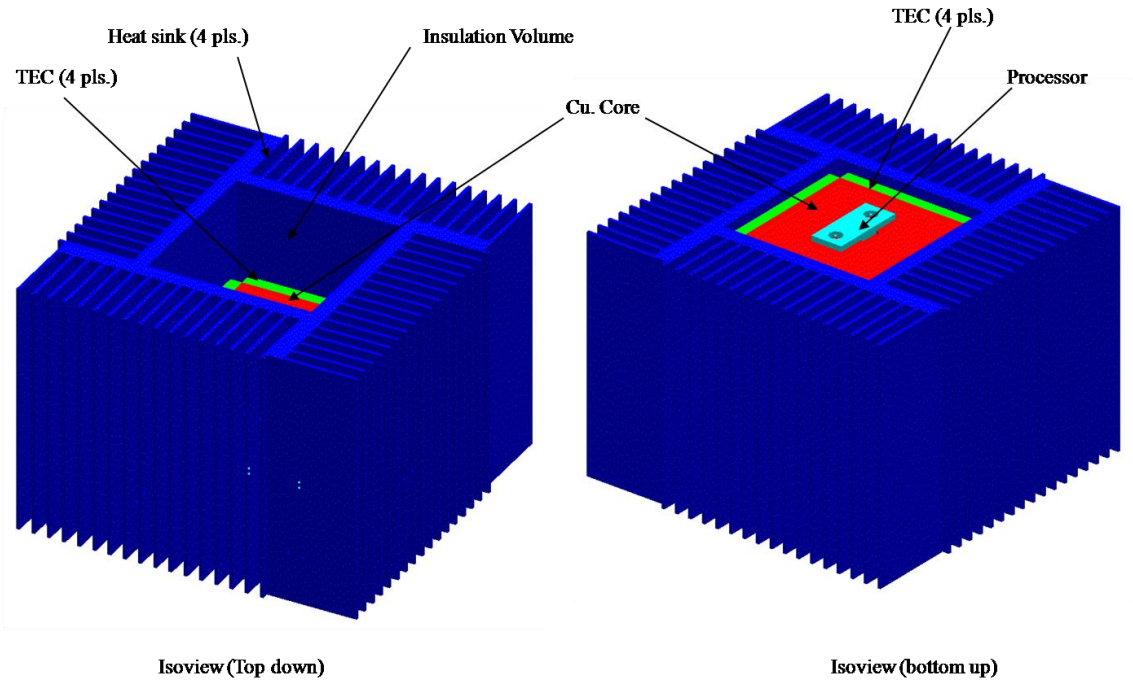


Figure 6.8 MHTS heat sink offset configuration to save horizontal real estate

The cold core acted as an extended fin, which was being cooled by series of enclosed thermoelectric modules made by Thermal Enterprise, Inc. (CP1-12710, 40x40x3.3mm^3), which

is rated at I_{max} = 10 A, V_{max} = 15.4 V, Q_{max} = 89.2 W. The thermoelectric modules used in this experiment have two ceramic surfaces, which have a flatness and parallelism of 0.002 inches, so polish or sand down was not necessary, only cleaned thoroughly using isopropyl alcohol prior to adhering to the cold core was performed. Nano particles silver adhesive compound was mixed as directly by the manufacturer and then spread evenly on both surfaces of the cold core and the thermoelectric modules respectively. The two surfaces were then intimately brought to contact by a mechanical C-clamps. The process was then repeated to the other facets of the cold core and modules. The system of cold core and thermoelectric modules spent at least 5 hours in normal room temperature tightly clamped to ensure proper adhesion. During this time, series of heat sinks (LPD70-25B Alpha Novatech, Inc) surfaces were also sanded, polished (if needed), and cleaned using the same process. After the thermoelectric modules were securely attached to the cold core, the C-clamps were removed. The second batch of adhesive compound was mixed and applied to the interface between the thermoelectric and the heat sink. The whole process was repeated until all heat sinks were attached and clamped together for the adhesive to cure. The MHTS is then set to cure for another 5 hours. This process could be streamlined by using mechanical fasteners to clamp the heat sink and the thermoelectric modules to the cold core all together at the same time and regular nano silver particle thermal interface paste could be used in lieu of adhesive to eliminate curing time during the MHTS fabrication process.

6.2 MHTS experimental apparatus and testing results

6.2.1 Experimental apparatus

In order to obtain comparable data, three separate experiments must be conducted. The first test comprised of testing a 1-D cooling using passive heat sink. The second test comprised of testing 1-D active cooling using one thermoelectric module. The third test

comprised of testing the Multidimensional-Heat-Transfer-System (MHTS). Besides comparing the cooling temperature of each system, the overall dimension of the system must also be compared in order to have a better understanding of advantage of the MHTS over the other two systems. The MHTS overall dimension also must not be larger than 100x100mm^2. It is noticed that identical heater and aluminum heat sink size (70x70x25mm^3) were used to illustrate the important of real estate limitation when active cooling system was employed on the same motherboard.

All three experimental models were tested in the air flow chamber, which was designed in accordance with AMCA 210-99/ASHRAE 51-1999 (Fig. 6.9). T-type thermocouples were embedded into the heat sink base and inside the processor and the airflow rates data were recorded through a data acquisition system. Air is forced through the air flow bench by an axial fan, through a flow straightener to ensure that the air flow approaching the nozzle area is laminar flow (Fig. 6.10). Depending on specific air flow rate, different nozzle size inside the air flow bench can be chosen (Fig. 6.11), and the rest of the unused nozzle can be block off using rubber stoppers. The air flow rate can be calculated using Eq. 14

$$Q = 60 \; x \; A \; x \; V \tag{14}$$

where: Q is the air flow rate $[m^3/min]$, A is the nozzle sectional area $[m^2]$ and V is the average flow velocity through the nozzle $[m^2/s]$.

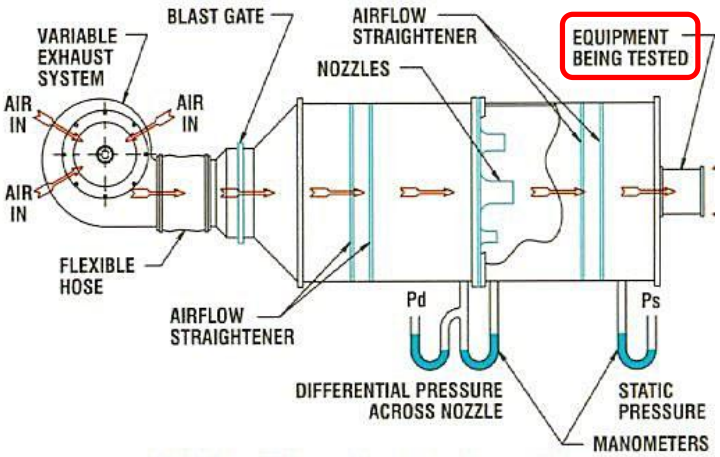


Figure 6.9 Air flow bench test set up

Figure 6.10 Air flow bench flow straightening screens

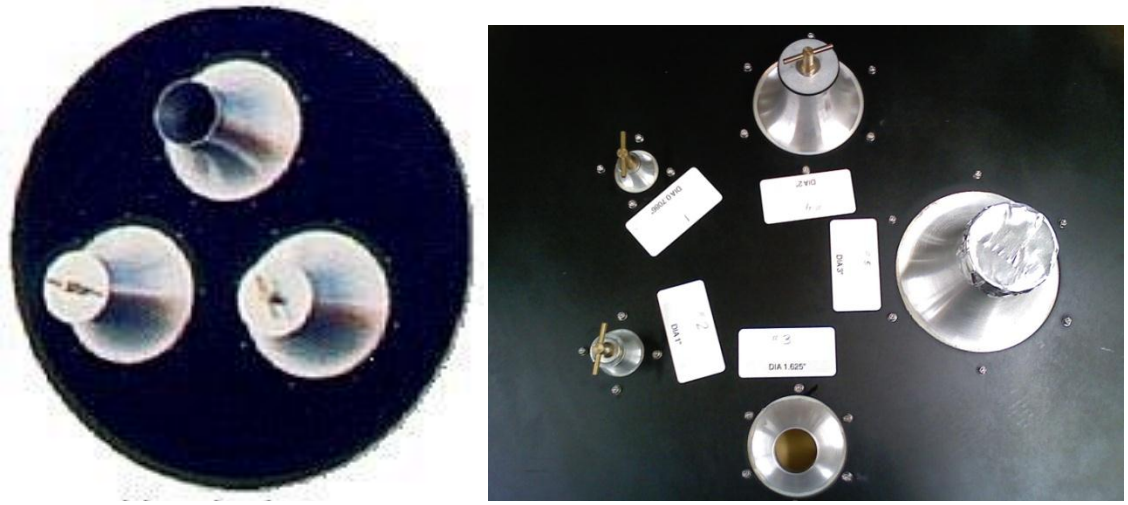


Figure 6.11 Air flow bench nozzles array

The average air flow through the nozzle can be obtained using Eq. 15 below:

$$V = \left(\frac{2gP_n}{r} \right)^{1/2} \tag{15}$$

where: g is the gravitation acceleration, 9.8 m/s^2, P_n is the differential pressure, and r is specific gravity of air, 1.2 kg/m^3 at 20°C, 1 atm.

The large end opening of the air flow bench was reduced down to a smaller square opening, which is exactly the same size as the devices to be tested to ensure that the air flow does not bypass the heat sinks (Fig. 6.12). Figure 6.13 shows the side-view of the air chamber. This chamber is constructed out of foam/foil insulation sheet to ensure that the air entering the testing device is adiabatic.

Once all the hardware were set up, the whole system was powered up and the data acquisition system started to record the air flow rate, the temperature of the processor, the

temperature of the heat sink, and the power input to the thermoelectric module(s). The 9.53x6.35x1.97mm^3 heat was tested at 25W for all test conditions.

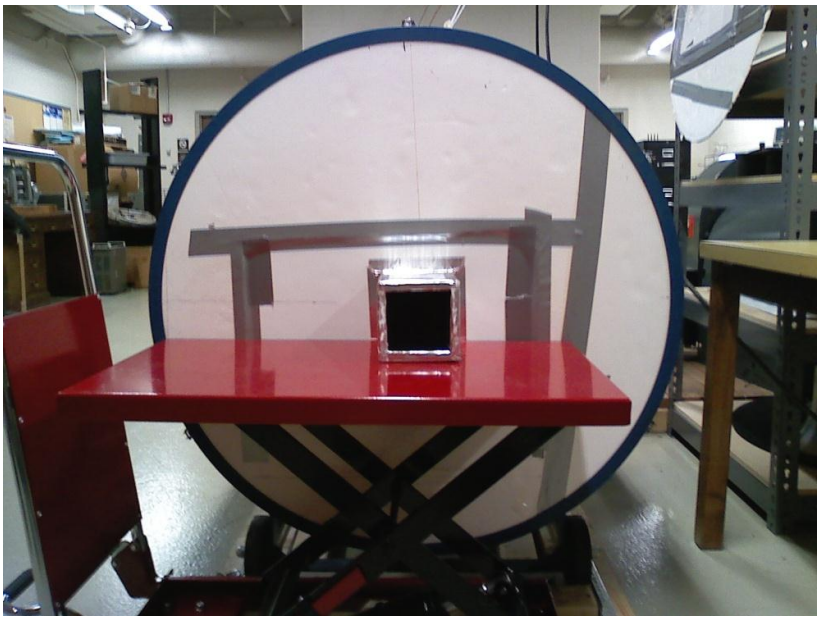


Figure 6.12 Air flow bench testing location

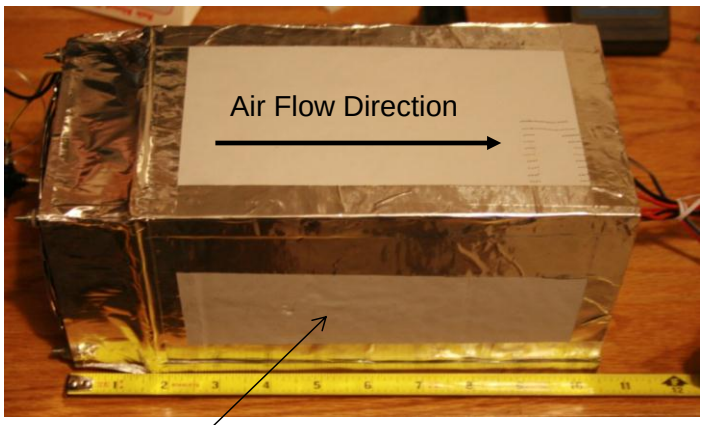


Figure 6.13 Air flow chamber

6.2.2 Thermal experimental results and discussion

The processor (heater) was first being cooled using one passive heat sink directly attached on top of the processor and the air flow rate was varied between 18.3 to 27 CFM respectively. The processor temperature corresponding to each air flow rate setting was recorded and plotted in Fig. 6.14.

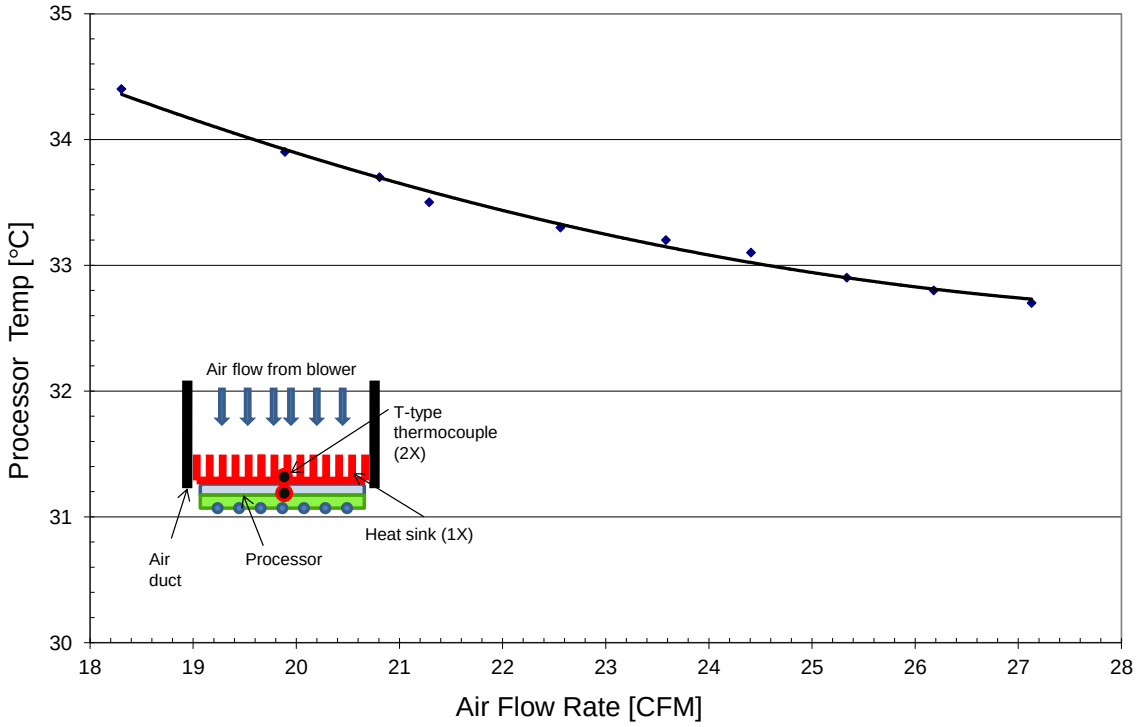


Figure 6.14 Processor temperature as a function of air flow rate for 1-D passive cooling

The ambient temperature of the air during the test was 20°C, so if the air flow were adjusted to blow beyond 27 CFM, the temperature of the processor might be able to eventually reach closer to 20°C max., but the acoustic generated by the fan would be unbearable. Therefore, in this case it is unrealistic to expect the processor temperature to get even close to room temperature in normal application and normal operating condition.

In the second test, where one thermoelectric was sandwiched between the processor and the same heat sink size in previous case was used. An additional DC power supply source was utilized to energize the thermoelectric module, and the input power was recorded for power consumption calculation later on. The lowest processor temperature was found to be approximately 52.5°C at an air flow rate of 35.6 CFM and 35W input in power to the thermoelectric module as illustrates in Fig. 6.15.

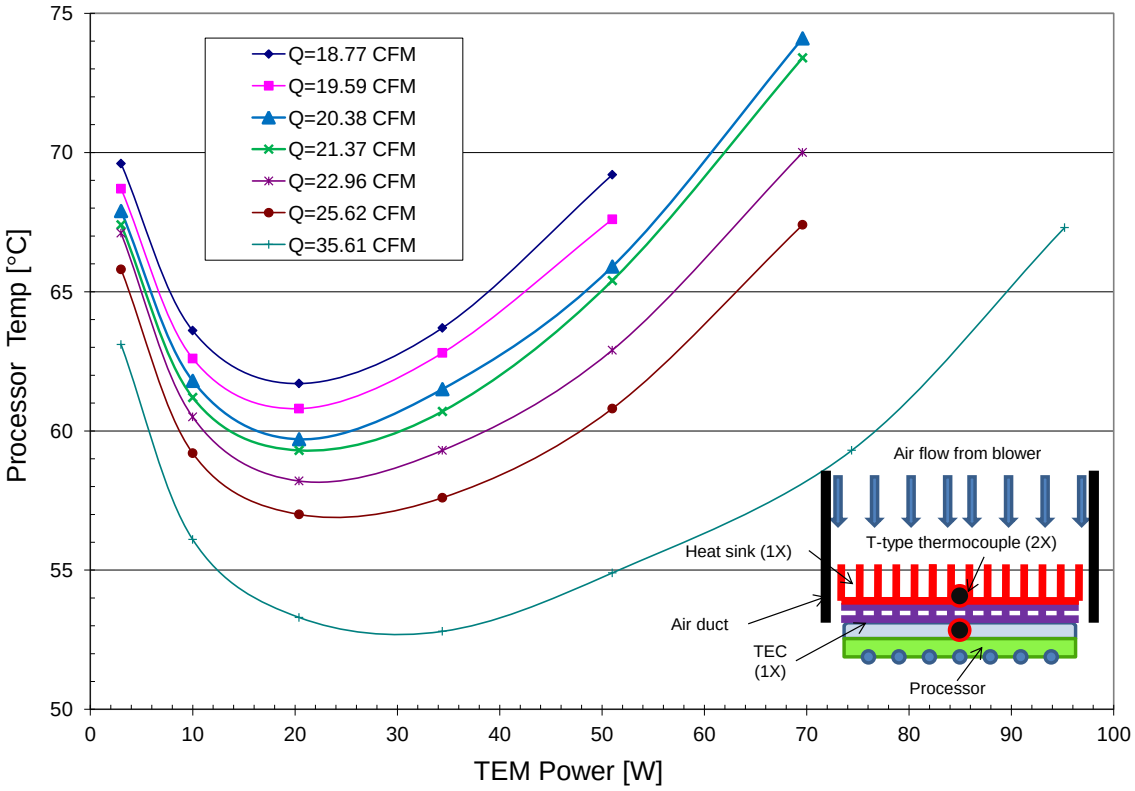


Figure 6.15 Processor temperature as a function of air flow rate for 1-D active cooling

The processor temperature recorded was more than 30°C higher than ambient temperature (20°C) with the assistant of one thermoelectric set up in 1-D configuration. At first glance, the result did not make sense because how could the processor temperature of an

active cooling be higher than the passive cooling case? In actuality, the result made perfect sense because in one-dimensional cooling using one thermoelectric in this case proved that due to the restriction of the motherboard horizontal real estate, the possibility of using larger heat sink in the horizontal configuration to accommodate extra power generated by the thermoelectric module would violate the 100x100mm^2 allocated footprint set fort earlier. If larger heat sink was used, the temperature of the processor might be lower than the passive cooling case; however, the larger heat sink would over shadow the RAM and I/O peripheral spaces on the motherboard. This test proved that the horizontal real estate restriction has negatively impacted the processor cooling performance.

In the third test, the Multidimensional-Heat-Transfer-System was tested at various thermoelectric power input from 1.3W to 230W. The temperature of the processor was found to be low ambient temperature starting at about 40W thermoelectric input power at various air flow rates as illustrated in Fig. 6.16.

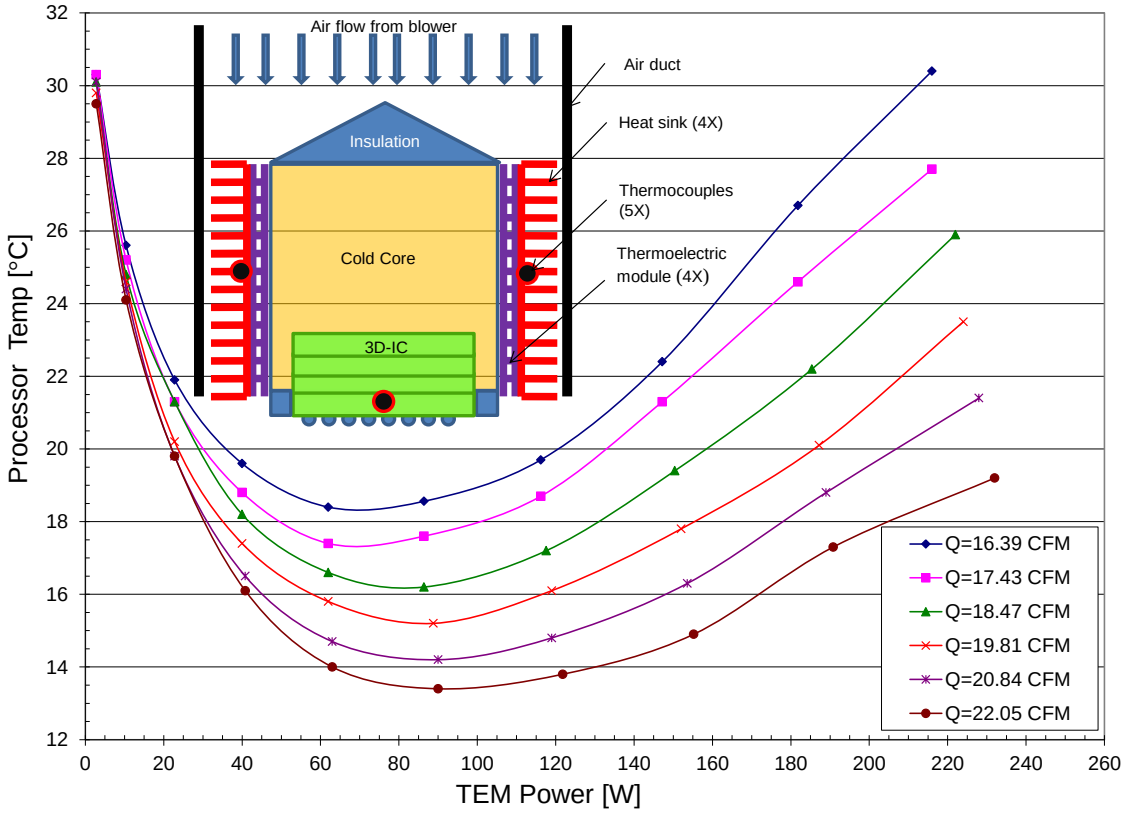


Figure 6.16 Processor temperature as a function of air flow rate for the MHTS

Even at low air flow rate (16.39 CFM) and 40W thermoelectric power input, the temperature of the processor was already dropped below ambient temperature (20°C). Subsequence conditions were tested to illustrate the range of the MHTS. The MHTS can accommodate a wide range of cooling requirements. Clearly, the MHTS can deliver the sub ambient cooling temperature with less air flow rate and thermoelectric power input compared to the conventional 1-D passive cooling and 1-D active cooling cases. At only 22 CFM and 90W thermoelectric power input, the MHTS can achieve a temperature of approximately 13°C. The advantage of the MHTS is the ability to direct the cold temperature toward the root of the cold core. The cold core in this case acted as an extended fin, which was being cooled by enclosed

thermoelectric modules. Unlike many other design cases and patents, the inventors concentrated on adding more thermoelectric modules to achieve the desire cooling temperature, but the heat transfer and leakage surrounding the thermoelectric modules was completely ignored, which severally penalized the cooling efficiency. For those cases, adding more thermoelectric modules in one dimensional configuration does not guaranteed that the processor temperature would be lower, especially when the real estate within the motherboard would not accommodate larger horizontal heat sink footprint. The unique design of the MHTS can accommodate more than four of the same size thermoelectric modules without violating the real estate allocated and still achieve the desire sub ambient cooling temperature.

6.2.3 Time response experimental results and discussion

The results obtained from the thermal test were utilized to determine how fast the MHTS can change the temperature of the processor from power up to steady state. This test is not only beneficial to 3D-ICs design with or without core hopping architecture cooling, but also to thermal cycle testing of ICs in general utilizing thermoelectric modules to obtain rapid and precision ramping control and lower set up cost comparing to conventional thermal chamber [44].

Many researches have been done in the area of transient analysis of thermoelectric cooler at the module level [45], but fewer researches were done to address how fast thermoelectric coolers response at the system integration level. At the time that this dissertation was written, the information regarding the design of sub ambient cooling system for 3D-ICs and transient calculation of such system is even more limited in current literature. However, Makino and Maruyama [46] illustrated that in one dimensional case of sub ambient cooling of a heat generating material using thermoelectric cooler, the transient response time decreases with

decreasing length of the cooled material, and the time constant decreases with increasing heat generation rate from the material.

The MHTS time response experiment was conducted in two parts. In the first test, the processor temperature was recorded at various air flow rates from 16.4 to 22 CFM and thermoelectric power input ranging from 3 to 230W. These tests established the baseline cooling temperatures for each of the thermoelectric power input cases. The whole system was then air cooled back to room temperature before each time response test was conducted. In the second test, the processor's powers were cycled on and off as the thermoelectric modules continued to be powered. This test was designed to observe the MHTS performance for the case of core hopping technology. The objective was to see how the MHTS cooling performance would affect the processor temperature as the power of the processor was switched on and off while the MHTS was powered continuously.

Core hopping is a recent development proposed by Intel in 2002 as an alternative to reduce processor temperature by having signals jump around from one core to another thereby distributing the heat around. The swapping excitation action allows the heat distribution of each core to be more uniform around the processor to avoid creating hot spots [47].

In the first test, both the MHTS and the processor were powered on at the same time and the temperature of the processor was recorded every 30 seconds using the data acquisition system. Figure 6.17 illustrates the effect of low air flow rate (16.39 CFM) and high thermoelectric input power to the time delay to reach steady state temperature. High thermoelectric input power (86.4W) drove the temperature down quickly (at 100 seconds and 17.5°C respectively), but the hot side temperature started to penetrate back to the cold side and drove the temperature back up and finally settled right above 19.5°C at about 550 seconds. The shortest response time for this test is 240 seconds, which was found at 16.39 CFM air flow

rate and 40W thermoelectric input power, but the processor temperature of 19.9°C is barely below ambient temperature.

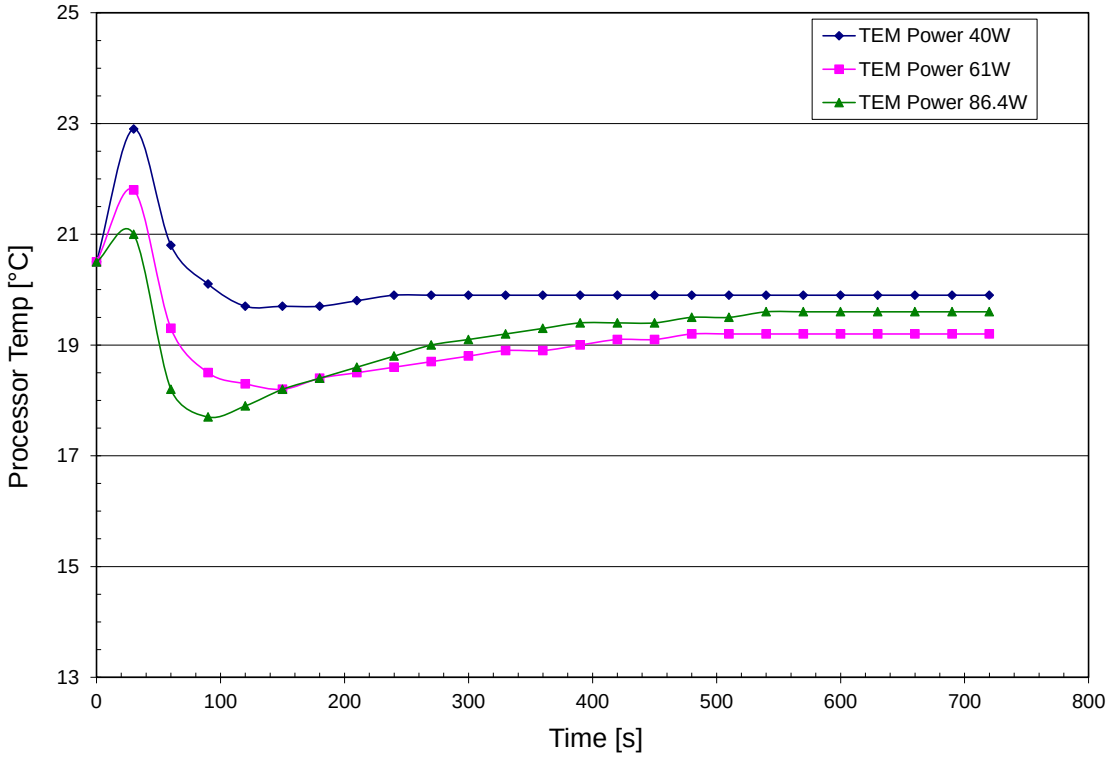


Figure 6.17 Processor temperature as a function of time at 16.39 CFM air flow rate

In the second test, the MHTS was cooled back down to room temperature and the air flow rate was adjusted to 1 CFM higher than the previous case. Figure 6.18 illustrates that at 61W thermoelectric power input and 17.43 CFM air flow rate, the processor can reach 17.6°C starting at about 120 seconds. In all three thermoelectric power input cases (40W, 61W and 86.4W), the processor temperature can reach below ambient temperature. However, at 86.4W and only 17.43 CFM air flow rate, the processor temperature took much longer than 700 seconds to reach steady state because the air flow rate of 17.43 CFM for an 86.4W thermoelectric input power is proven to be inadequate still. The air flow rate continued to

increase from 18.47 to 20.84 CFM, and the processor temperature continued to drop from approximately 17°C down to 14°C and the overshoot of the cooling temperature began to subside. The MHTS took about 400 seconds to reach steady state in all cases as shown in Figure 6.19, 6.20 and 6.21.

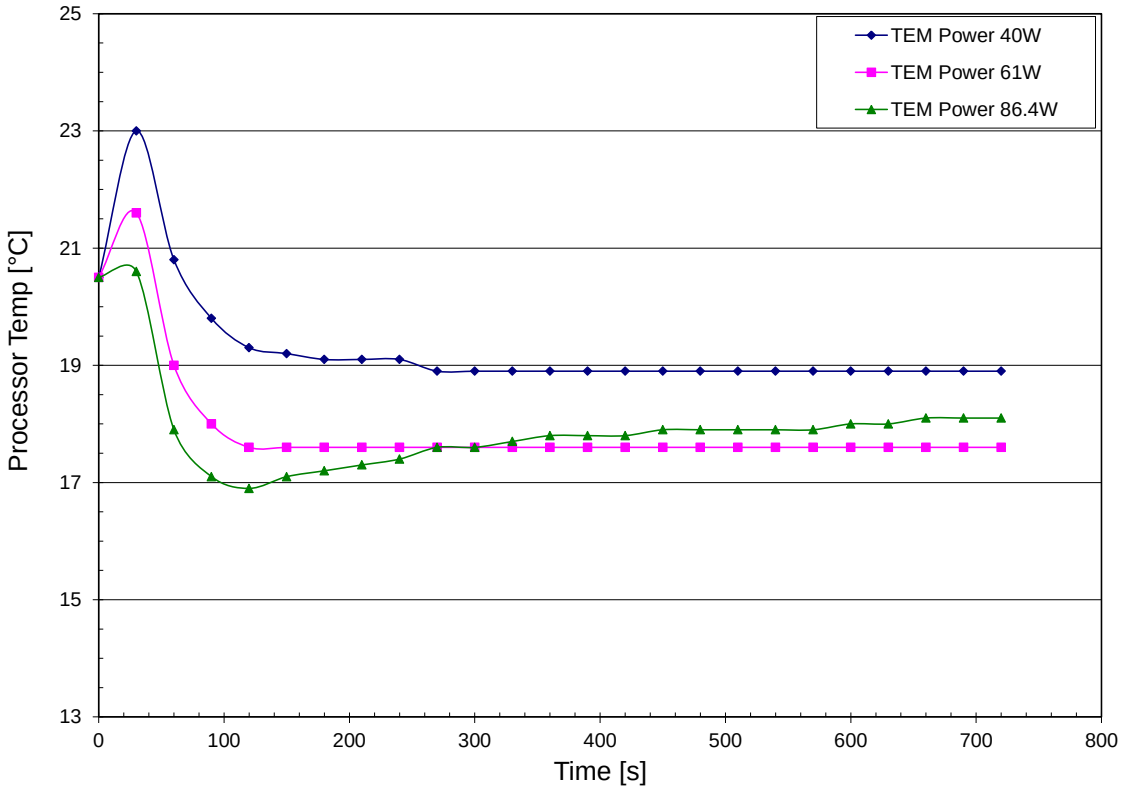


Figure 6.18 Processor temperature as a function of time at 17.43 CFM air flow rate

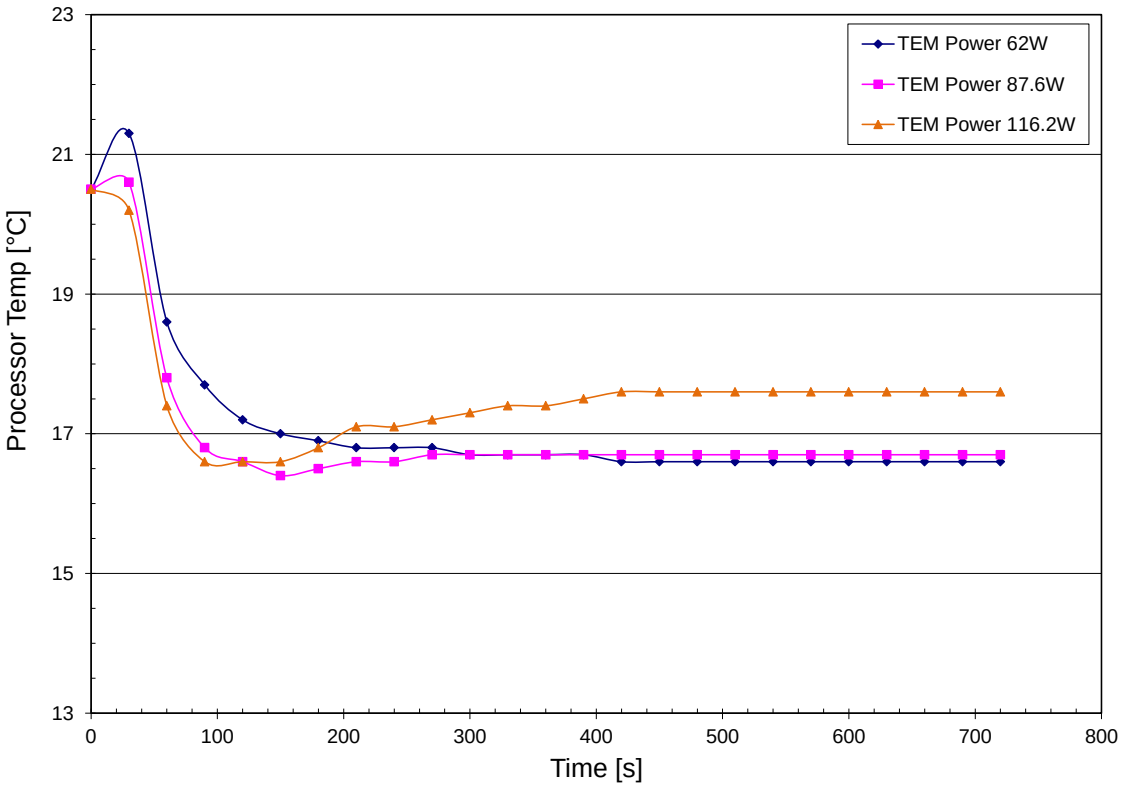


Figure 6.19 Processor temperature as a function of time at 18.47 CFM air flow rate

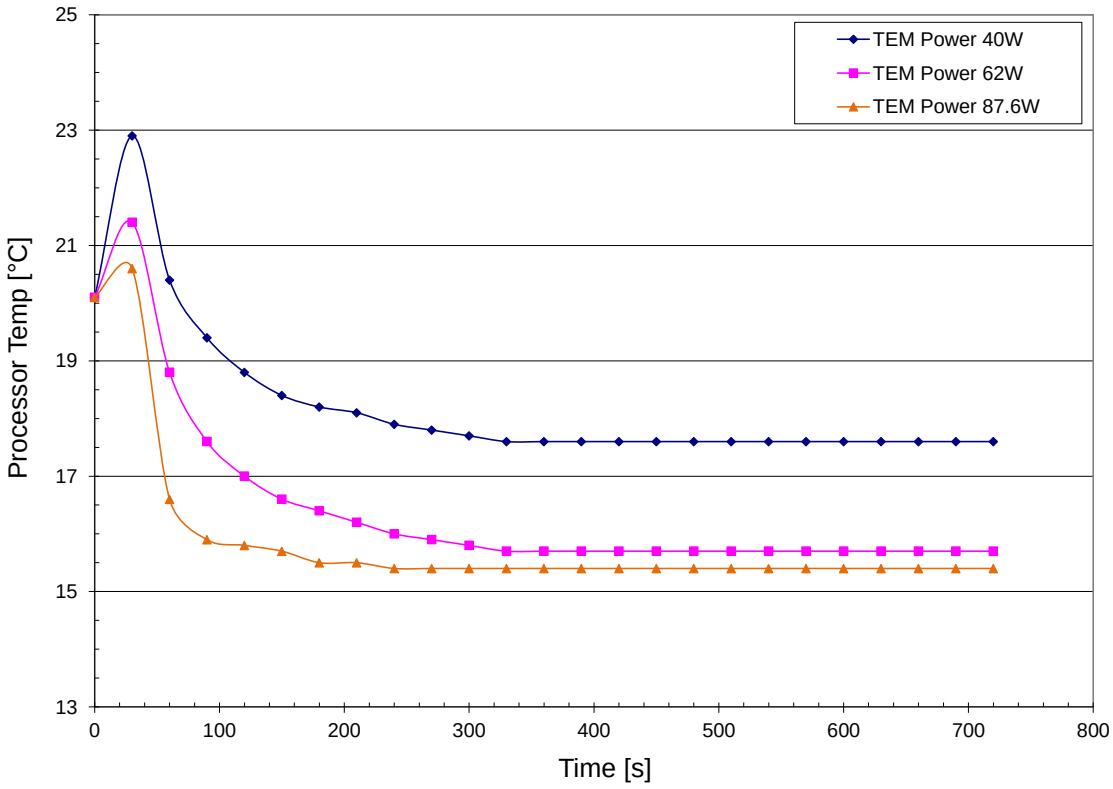


Figure 6.20 Processor temperature as a function of time at 19.81 CFM air flow rate

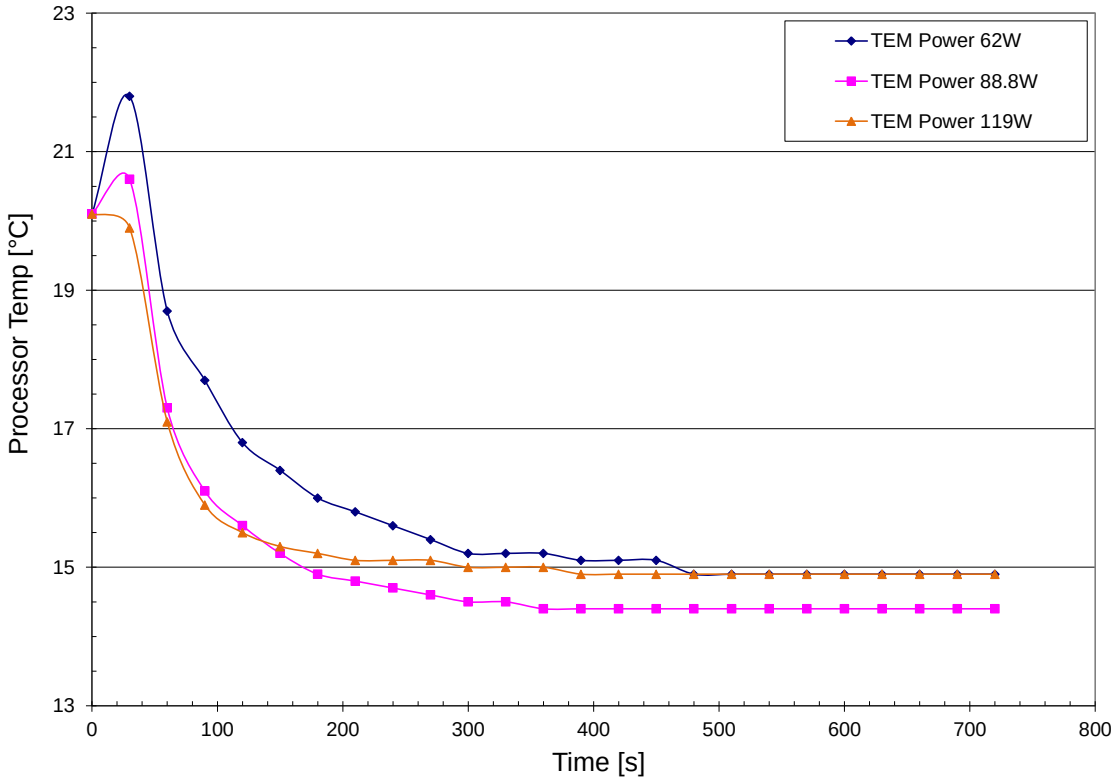


Figure 6.21 Processor temperature as a function of time at 20.84 CFM air flow rate

In the next test, the air flow rate was adjusted to 22.05 CFM to test the three cases of thermoelectric power input of 62W, 88.8W and 119W. The processor temperature reached its best temperature of about 13.4°C at approximately 400 seconds. In the case of 119W thermoelectric power in put at 22.05 CFM air flow rate (Fig. 6.22), the processor achieved faster cooling time by about 100 seconds compared to the case of 88.8W thermoelectric power input, but obviously the air flow rate for 119W TEM input out to be higher in order for the processor temperature to reach 13°C or below, but the acoustic generated by the fan would be undesirable.

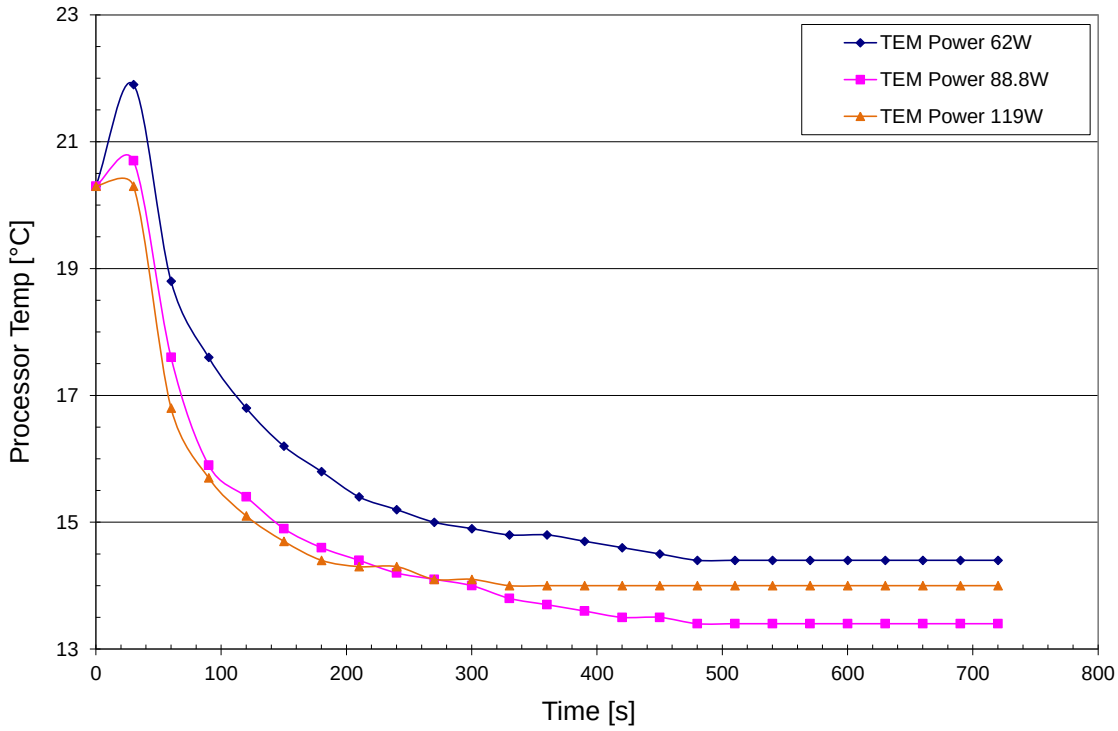


Figure 6.22 Processor temperature as a function of time at 22.05 CFM air flow rate

Finally, the MHTS was tested for core hopping technology. Core hoping test was achieved by turning on and off the power of specific core to minimize the heat buildup of that particular core within a multi-core system. Figure 6.23 shows that the temperature of the processor can achieve the lowest temperature of 10°C as the processor was turned on and off every 30 seconds. Even though a single core system was tested, but it clearly illustrated the benefit of switching on and off the power of the core can lower its temperature even more.

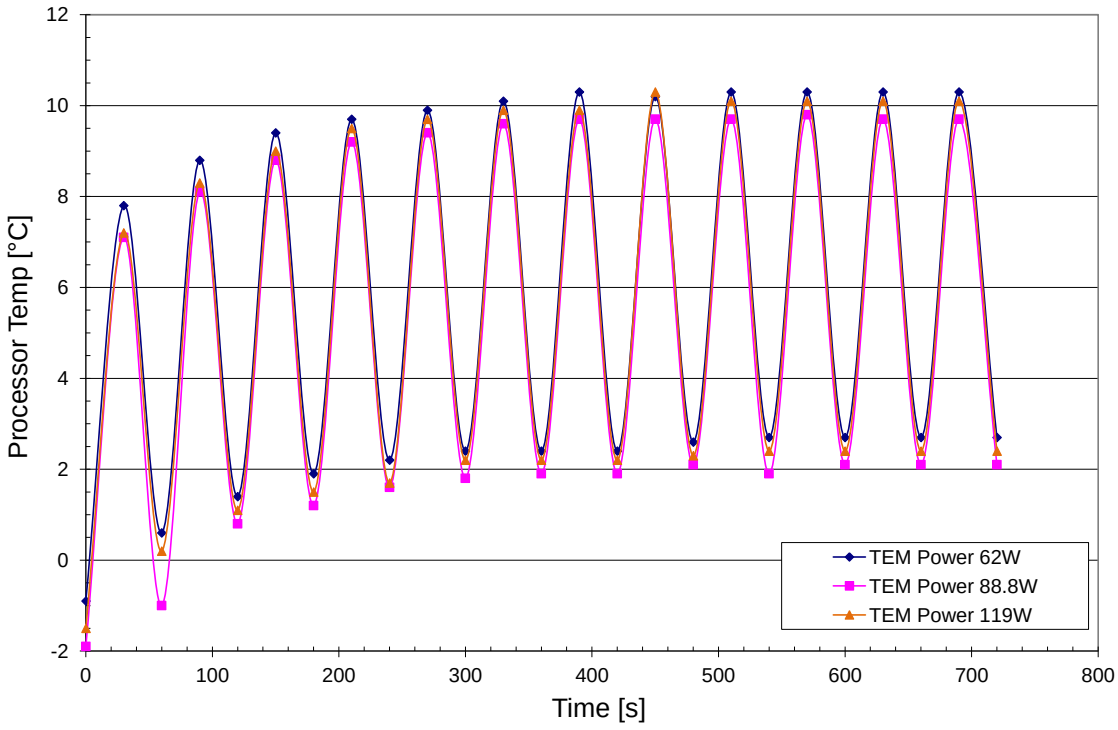


Figure 6.23 Core hopping temperature profile at 22.05 CFM air flow rate

6.3 Computational Fluid Dynamic (CFD) Studies

6.3.1 CFD Setup

The MHTS was studied further using Computational Fluid Dynamic (CFD) modeling with ANSYS® 13.0 [48]. A 10x10x10 mm^3 three dimensional stack package with five 10W output by each processor (50W total power) was built. Each processor is 8x8x1 mm^3, and stacked between each processor is a 1mm thick copper layer. For simplicity purposes, the copper layer is solid; however, in reality there will be holes going through the copper sheet for signal routing between the layers. The anatomy of the 3D-IC is illustrated below in Fig. 6.24. All layers are stacked and edge metalized with 1mm thick copper layer.

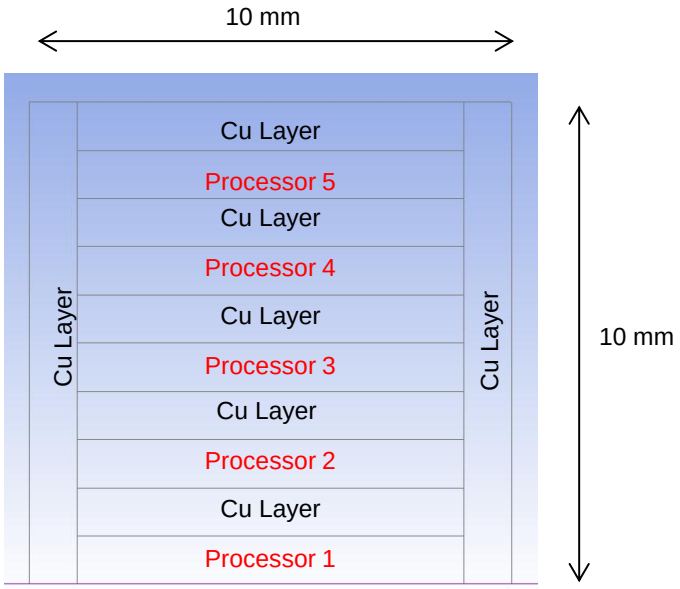


Figure 6.24 3D-IC with 5 processors 8x8x1mm^3, 10W each

The 3D-IC model was analyzed in three ways. First the 3D-IC was cooled using a 1-D passive cooling utilizing a LPD70-25B, 70x70x25 mm^3 aluminum heat sink (dimensions are shown in Appendix 1). Second, the 3D-IC was cooled using 1-D active cooling utilizing 4 thermoelectric modules, which were horizontally mounted in the same plane utilizing 4 LPD70-

25B, 70x70x25 mm^3 heat sinks and a 140x140x1 mm^3 thick copper heat spreader. Third, the 3D-IC was cooled using the MHTS with 4 thermoelectric modules and 4 LPD70-25B heat sinks in a vertical configuration. Each set up was analyzed at 20, 25, and 30 CFM respectively and the temperature of each processor was recorded and the results were plotted in the same group of air flow rate for comparison. The thermoelectric modules used in these setups are the built-in macro Melcor CP1.4-127-10L model available in ANSYS 13.0.

6.3.2 CFD Result and Discussion

Table 6.2, Table 6.3 and Table 6.4 summarized the results of three air flow rate cases (20, 25, 30 CFM respectively) for three configurations.

Table 6.2 Summarized result for **20 CFM** air flow rate case

	No TEC (1x-70x70x25mm HS)		4-TECs Horizontal Mount (1x-140x140x25mm HS)		4-TECs MHTS (4x-70x70x25mm HS)	
Processor	Chip Temp. [°C]	Δ T [°C]	Chip Temp. [°C]	Δ T [°C]	Chip Temp. [°C]	Δ T [°C]
Processor 1	95.46		107.10		28.02	
Processor 2	90.61	4.85	102.50	4.60	23.30	4.72
Processor 3	88.29	2.32	100.30	2.20	22.58	0.72
Processor 4	85.13	3.16	97.26	3.04	22.25	0.33
Processor 5	80.55	4.58	92.95	4.31	21.67	0.58

Table 6.3 Summarized result for **25 CFM** air flow rate case

	No TEC (1x-70x70x25mm HS)		4-TECs Horizontal Mount (1x-140x140x25mm HS)		4-TECs MHTS (4x-70x70x25mm HS)	
Processor	Chip Temp. [°C]	Δ T [°C]	Chip Temp. [°C]	Δ T [°C]	Chip Temp. [°C]	Δ T [°C]
Processor 1	91.44		100.40		24.54	
Processor 2	86.59	4.85	95.83	4.57	19.82	4.72
Processor 3	84.27	2.32	93.59	2.24	19.10	0.72
Processor 4	81.10	3.17	90.55	3.04	18.76	0.34
Processor 5	76.52	4.58	86.24	4.31	18.19	0.57

Table 6.4 Summarized result for **30 CFM** air flow rate case

	No TEC (1x-70x70x25mm HS)		4-TECs Horizontal Mount (1x-140x140x25mm HS)		4-TECs MHTS (4x-70x70x25mm HS)	
Processor	Chip Temp. [°C]	Δ T [°C]	Chip Temp. [°C]	Δ T [°C]	Chip Temp. [°C]	Δ T [°C]
Processor 1	88.60		95.90		21.87	
Processor 2	83.74	4.86	91.28	4.62	17.15	4.72
Processor 3	81.43	2.31	89.04	2.24	16.43	0.72
Processor 4	78.26	3.17	85.99	3.05	16.10	0.33
Processor 5	73.68	4.58	81.68	4.31	15.52	0.58

Figures 6.25, 6.26, 6.27, illustrate the comparison in graphical form for clarification.

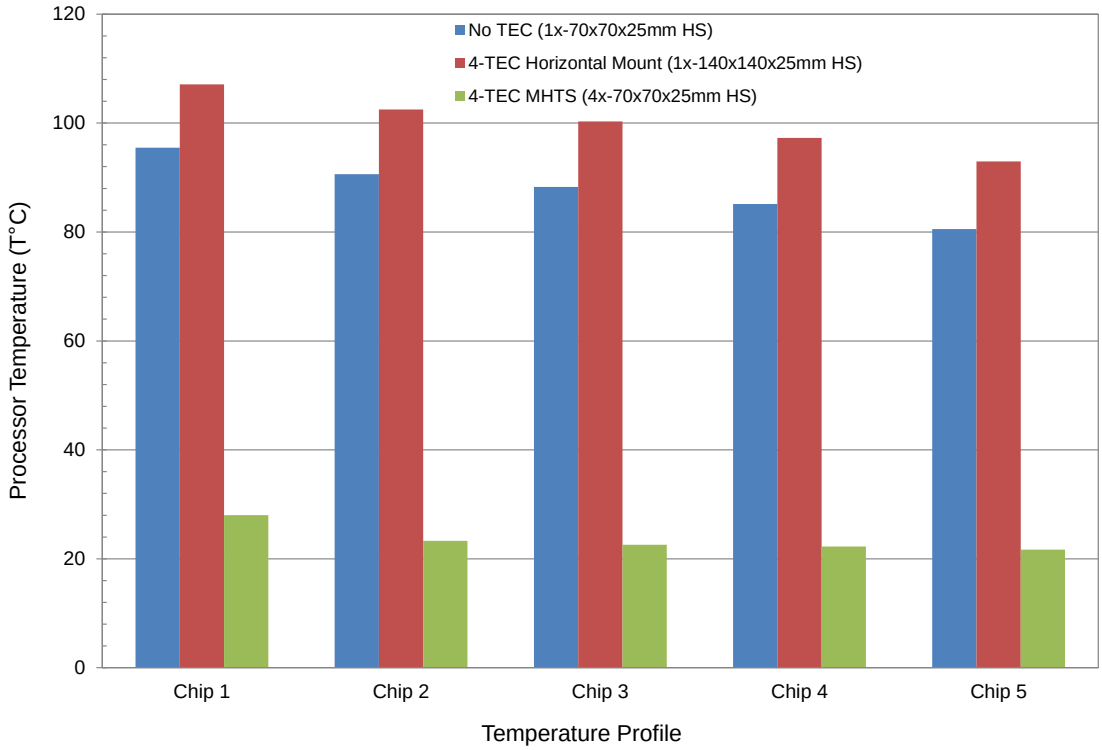


Figure 6.25 3D-IC temperature profile for 5 processors stacked at 20 CFM air flow rate

Even though, the thermoelectric modules used in the CFD models are not identical to those which were used in the actual experimental analysis, but the results obtained from the

CFD models agreed well with the experimental analysis in principle. In the first case, without using any thermoelectric coolers, the temperature of each chip is in the range of 80s to 90s degree C. In the second case, where four thermoelectric were used in horizontal configuration and four heat sinks, one would suspect that the temperature of the chip would be much lower due to the assistance of four thermoelectric modules, but instead the temperature of each layer is much higher in the range of 90s to 100s degree C. These results illustrates clearly that as the processors grow taller, adding more thermoelectric modules in 1-D configuration will not help reducing the temperature of the 3D-IC. However, when the same size thermoelectric modules and heat sinks were packaged as the MHTS, the temperature of each processor is lower by at least 60 to 80°C in all three air flow rate cases, and all of the processors temperatures are close to or at below sub ambient temperature condition.

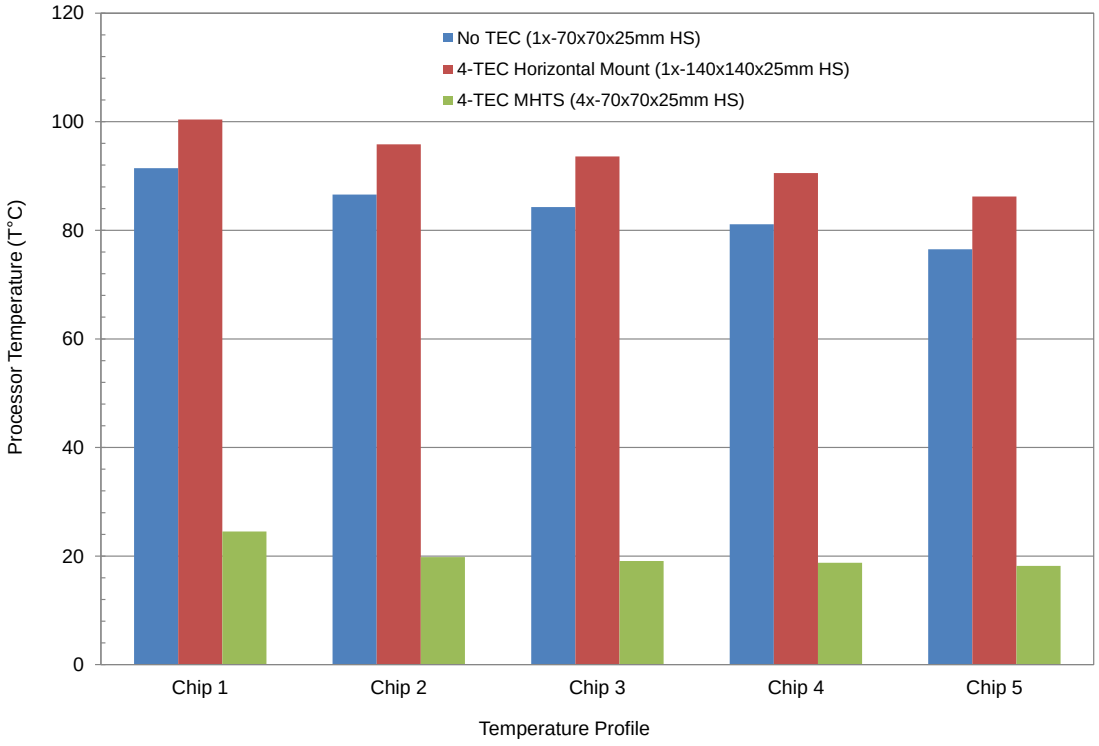


Figure 6.26 3D-IC temperature profile for 5 processors stacked at 25 CFM air flow rate

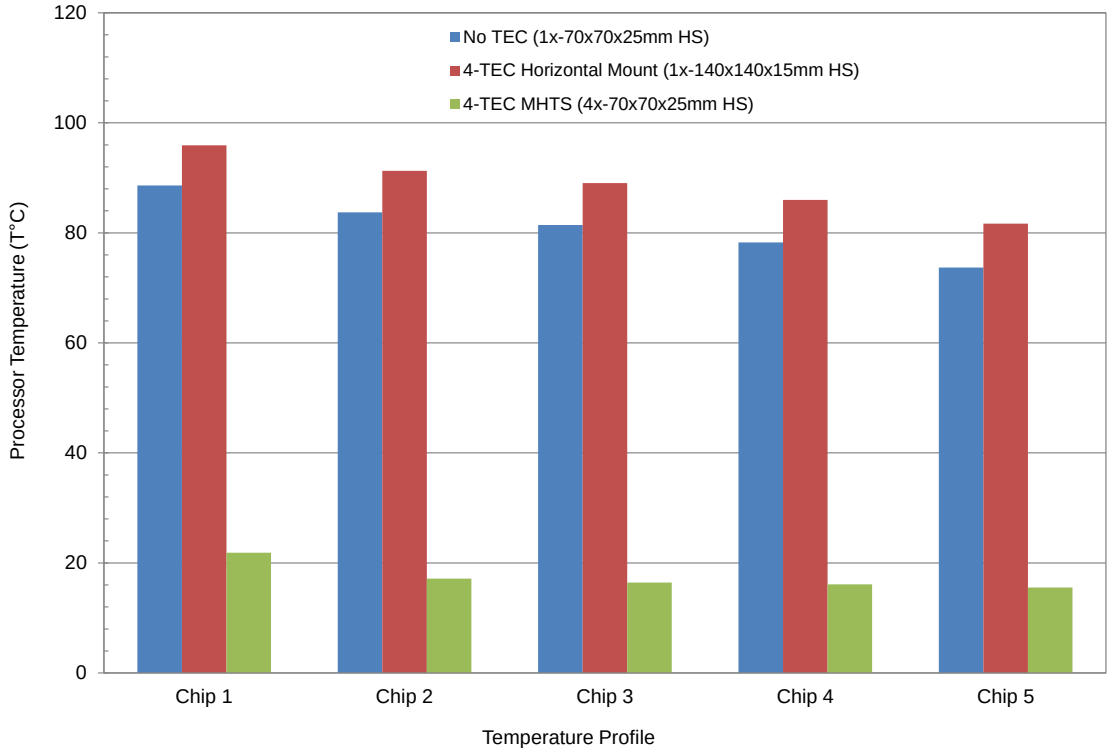


Figure 6.27 3D-IC temperature profile for 5 processors stacked at 30 CFM air flow rate

Figure 6.28, 6.29, 6.30 show the CFD results of the 1-D passive cooling. Clearly, there is a noticeable temperature gradient different between the top processor and the bottom processor.

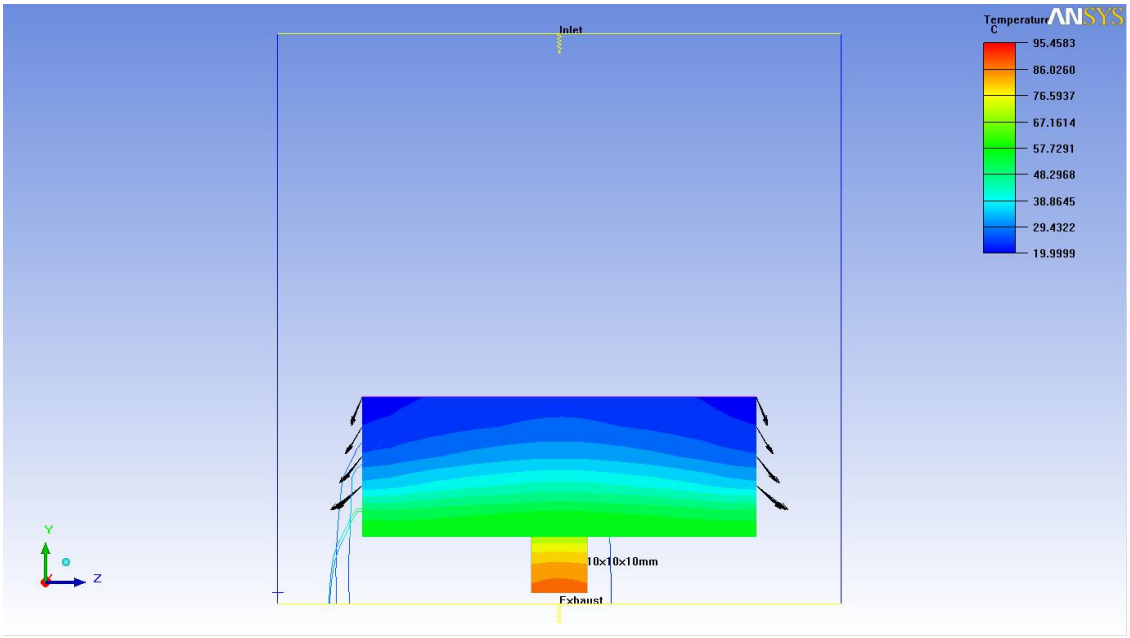


Figure 6.28 3D-IC CFD result for 5 processors stacked at 20 CFM (70x70x25 mm^3 HS)

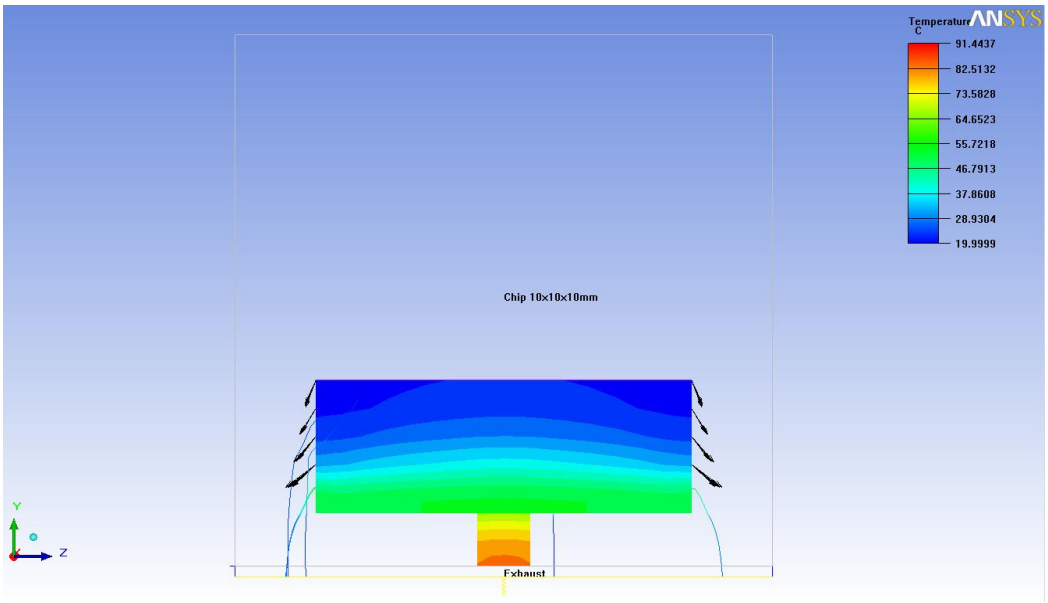


Figure 6.29 3D-IC CFD result for 5 processors stacked at 25 CFM (70x70x25 mm^3 HS)

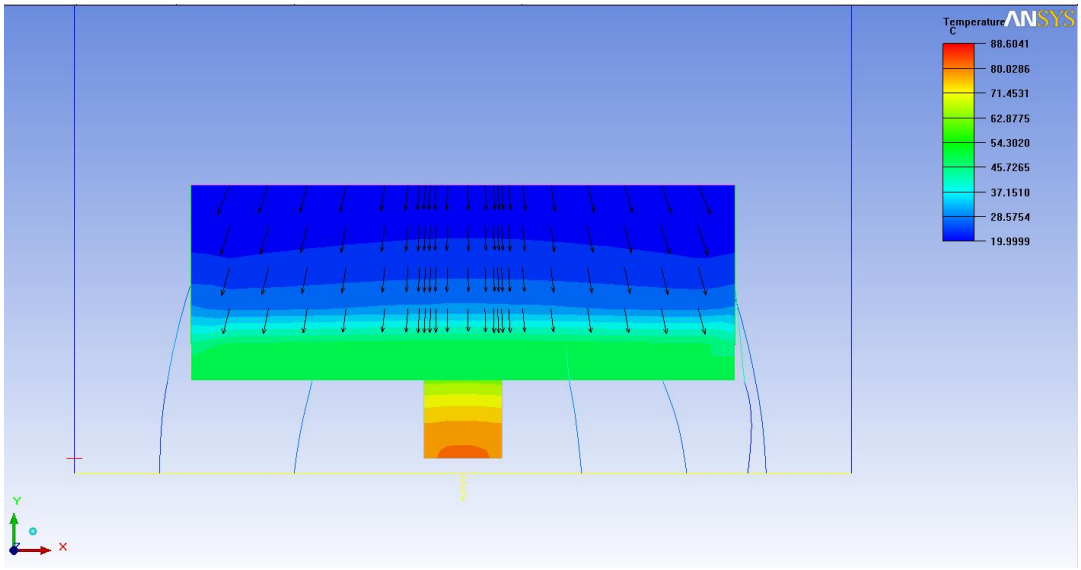


Figure 6.30 3D-IC CFD result for 5 processors stacked at 30 CFM (70x70x25 mm^3 HS)

Figure 6.31, 6.32, and 6.33 show the CFD result of the 1-D active cooling. In this case, the temperatures are more uniform, but are much higher than the 1-D passive cooling case. Both cases however, did not achieve sub ambient cooling requirement.

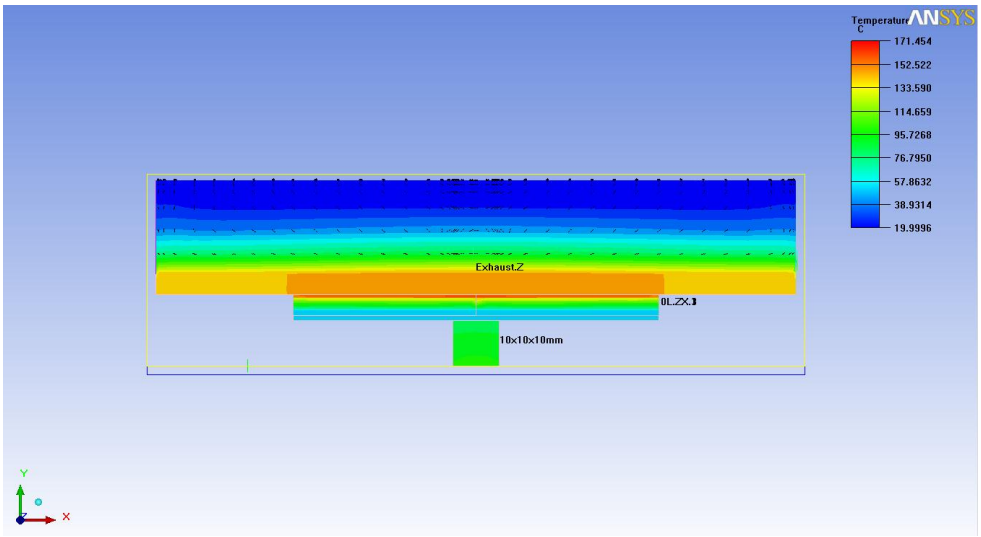


Figure 6.31 3D-IC CFD result at 20 CFM, 4 TECs mounted horizontally (140x140x25 mm^3 HS)

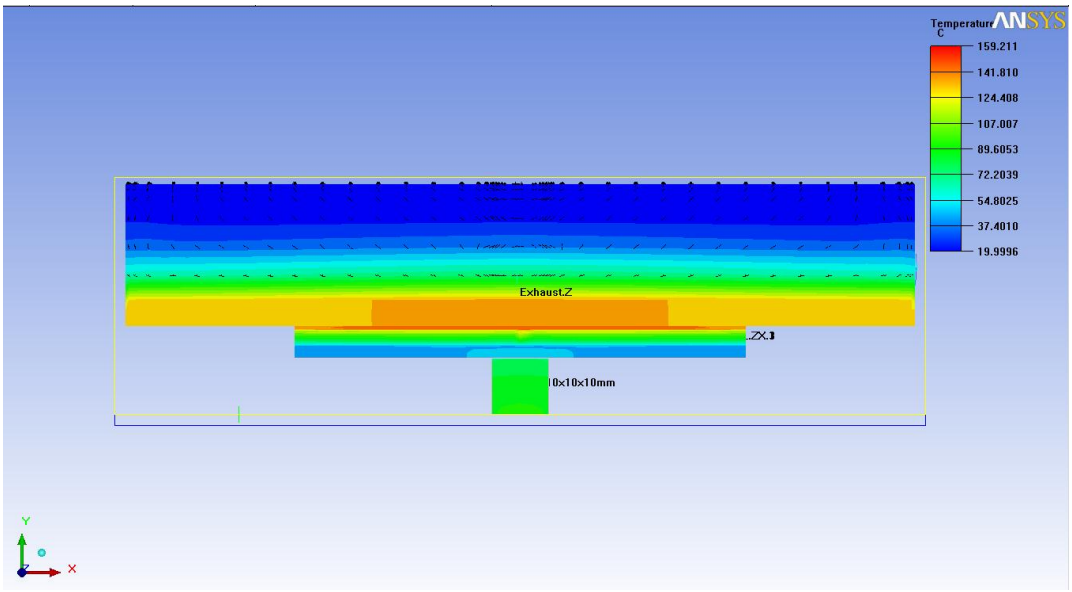


Figure 6.32 3D-IC CFD result at 25 CFM, 4 TECs mounted horizontally (140x140x25 mm^3 HS)

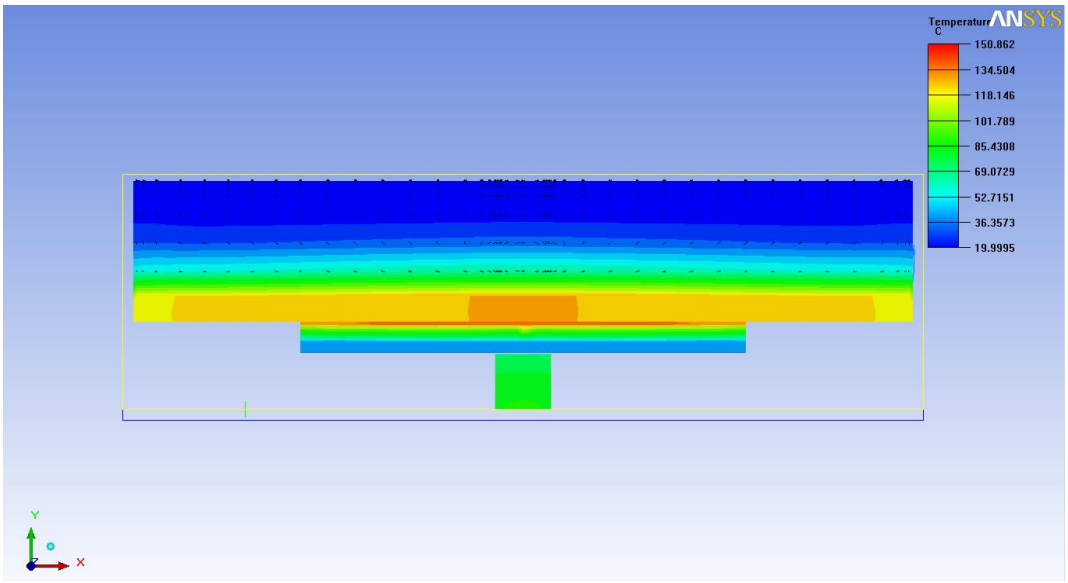


Figure 6.33 3D-IC CFD result at 30 CFM, 4 TECs mounted horizontally (140x140x25 mm^3 HS)

Figure 6.34, and 6.35 show the result of the 3D-IC being cooled by the MHTS. The temperatures in all cases are much more uniform and near or below ambient condition. The logistic footprint for the MHTS is also much smaller - 95x95 mm^2 compared to the horizontal 4-TECs case of 140x140 mm^2.

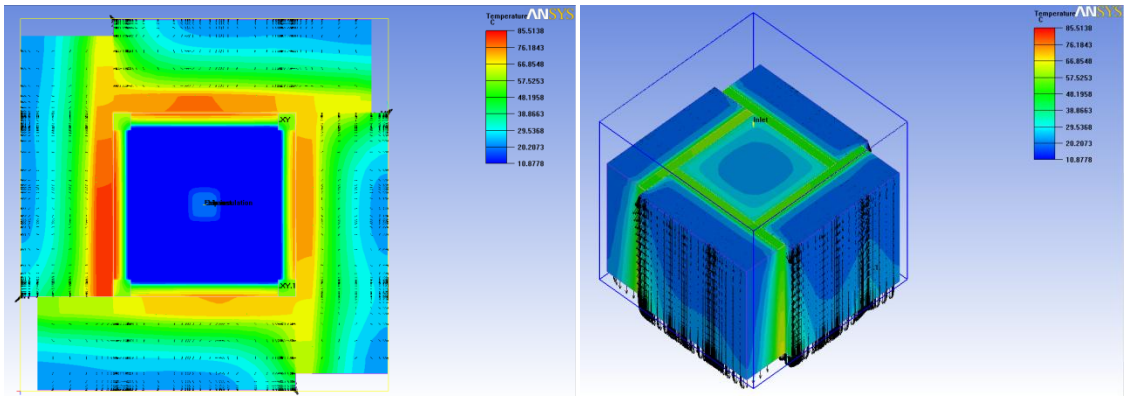
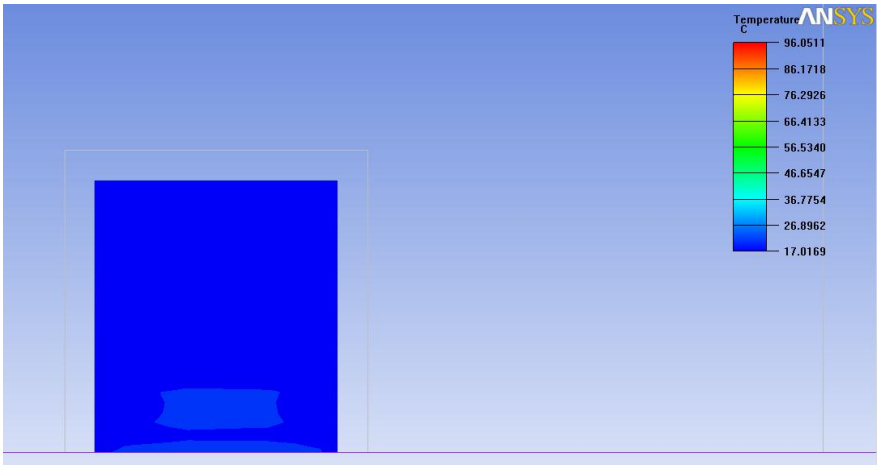
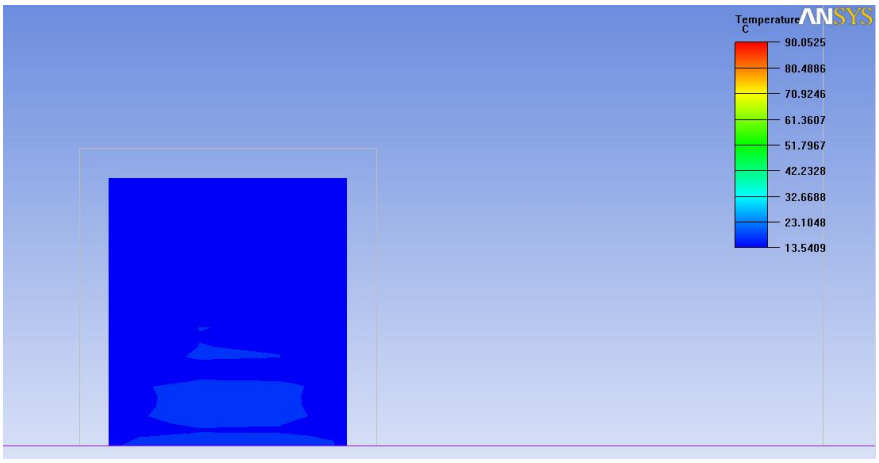


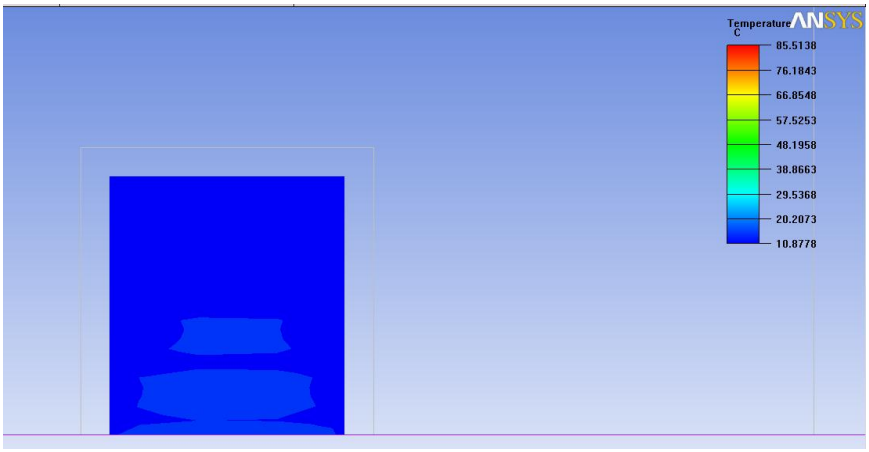
Figure 6.34 3D-IC CFD result using the MHTS (4x-70x70x25 mm^3 HS)



(20 CFM)



(25 CFM)



(30 CFM)

Figure 6.35 3D-IC CFD result at 20,25,30 CFM using the MHTS (4x-70x70x25 mm^3 HS)

6.4 Summary

The Multidimensional-Heat-Transfer-System (MHTS) presented in this section utilized the vertical dimension to accommodate four or more thermoelectric modules in order to cool a 25W and a 50W 3D-IC to approximately 7°C below ambient temperature in about 400 seconds for the experimental case and 2°C below ambient temperature for the CFD case. The MHTS also illustrated the advantage of core hopping in reducing the processor temperature down to 10°C below ambient temperature. Without the MHTS novel configuration, it is impossible to stack more than three thermoelectric modules into the same horizontal real estate and utilized the same horizontal heat sink footprint and still maintains the system structural stability and integrity for high vibration applications. This study also proved that adding more thermoelectric modules to cool a 3D-IC in 1-D horizontal configuration does not necessary improve the heat transfer because of the thermal stack up between n-numbers of thermoelectric modules and the heat sink footprint is normally twice the size of the thermoelectric module. Hence, the heat sink horizontal footprint will eventually overshadow other electronic components on the motherboard, which is undesirable and unrealistic. Since the coefficient of performance of thermoelectric is much lower than that of a compression cycle cooling, it would be unjustified to compare the two systems together, but instead the performance of the MHTS should be compared with other solid state cooling devices.

CHAPTER 7

MULTIDIMENSIONAL THERMAL CYCLING SYSTEM (MTCS)

7.1 Introduction

In recent years, there exists a need for fast and robust testing methodology, which can be utilized to assess the reliability of electronic packages rapidly due to the short product life cycles trend that the industry is employing [49]. The conventional reliability testing of current non-3D processor packages or electronic components in general is very time-consuming and costly because it required an assistant of a bulky thermal chamber as show in Fig. 7.1. Regardless of how many IC is tested, the whole thermal chamber must be energized; hence, it is not economical from a testing perspective especially during system development and demonstration phase when engineers only need to quickly test one or two ICs only.

Figure 7.1 Thermal cycling chamber (courtesy of ESPEC)

The heat dissipation of microprocessors is projected to reach 360W with the maximum processor heat flux to be more than 190W/cm^2 for high performance CPU by the next decade

as mentioned before. Unfortunately, thermal management of these packages has not followed at the same speed because the future demand for multitasking and faster computation is inversely proportional to the package size. This phenomenon introduces many challenges for microelectronic packaging industries due to high heat flux. Conventional environmental chamber might not be able to guarantee temperature penetration deep within a complex 3-dimensional structure. Solid state cooling using thermoelectric or thermal diode technologies have not been utilized and reported widely to sub-cooled 3D-ICs packages in the literature due to lack of high COP. However, due to the low thermal mass and ceramic construction, very high and effective heating and cooling rates can be achieved in the same device, which makes thermoelectric module an excellent candidate for thermal cycling application. The only question is how to integrate thermoelectric module to use as a thermal cycling device for 3D-IC architecture.

In this section, the Multidimensional Thermal Cycling System (MTCS) illustrates the advantage of utilizing the third dimension to incorporate multiple thermoelectric coolers to determine the characteristic lifetime of a 3D-IC between 0°C and 120°C. Also the reliability testing experiment was also performed on the MTCS itself to verify its structural integrity performance as it was thermally cycled between 0°C and 120°C [50].

7.2 MTCS experimental apparatus and procedures

7.2.1 Experimental apparatus

Utilizing the same concept derived from the Multidimensional-Heat-Transfer-System (MHTS), the simplest form of the MTCS comprised of a center core, which can be made out of oxygen-free copper for maximum heat transfer or other heat conducting material such as but not limited to, carbon graphite, stainless stell or aluminum… depending on specific application

and cost requirements. The center core acted as an extended fin, which was being heated and cooled by four enclosed thermoelectric modules made by Thermal Enterprise (CP1-12710, 40x40x3.3 mm^3). Each thermoelectric module is rated at 10A, 15.4V, 89.2W maximum and being cooled by one aluminum heat sink (70x70x25 mm^3). All exposed corners and surfaces were sealed with injection closed cell foam, and nano-silver particles thermal interface material was used to enhance the heat transfer between the thermoelectric module and the center core. This configuration eliminated the heat transfer leakage problem that many thermoelectric system designers have been reluctant to pay attention to, which severely penalized the cooling efficiency of the thermoelectric cooling systems in the past. Figure 7.2 illustrates the simplest form of the MTCS, which is a cubical shape core. Multiple thermoelectric modules can be integrated to a polygon cross sectional core with different height and different cross sectional areas between the top and bottom faces could be constructed depending on different thermal shock temperature requirement. A 9.53x6.35x1.97 mm^3 solid state heater, which has a maximum rated power of 150W, was used to simulate a processor. The objective of this study was to thermally shock an active powered device between 0°C and 120°C beyond the processor-level thermal management, so the detail design of the 3D-IC will not be discussed in further in this section.

The MTCS was tested in the air flow chamber similarly to the MHTS. T-type thermocouples were embedded into the heat sink bases and into the back side of the processor to ensure the temperature indeed penetrates the processor thoroughly. The air flow rate data and temperature data were recorded using a data acquisition system.

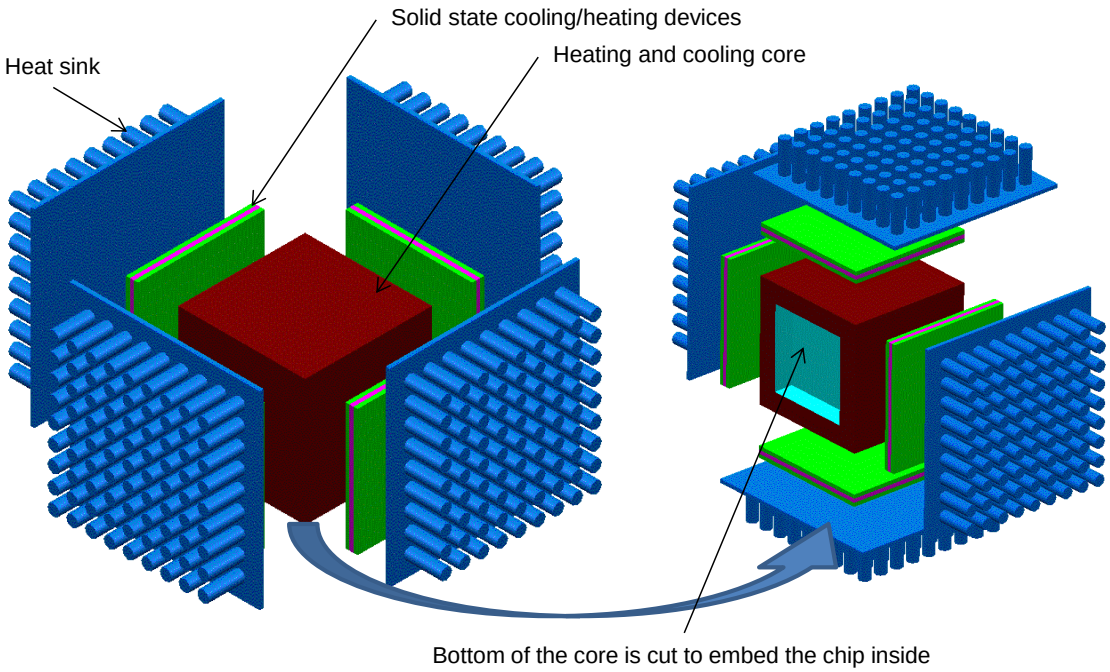


Figure 7.2 Exploded view of the Multidimensional Thermal Cycling System (MTCS)

A program code was written in order to effectively control the mechanical switching device to switch the polarity of the thermoelectric module to achieve the hot or cold requirement. Figure 7.3 illustrates the schematic of the switching action. In the heating mode, both 3-ways switches were switched to positive (+) power source to negative (-) lead of the thermoelectric modules. Once the cooling is required, the two switches were reversed, which put the positive (+) power source connected to the positive (+) lead of the thermoelectric modules. The objective of this illustration is to minimize the time delay from manually swapping the polarity of multiples thermoelectric modules, which will affect the result of the test. Note both 3-ways switches must operate in the same direction (i.e. both must be either switched to the left or both must be switched to the right).

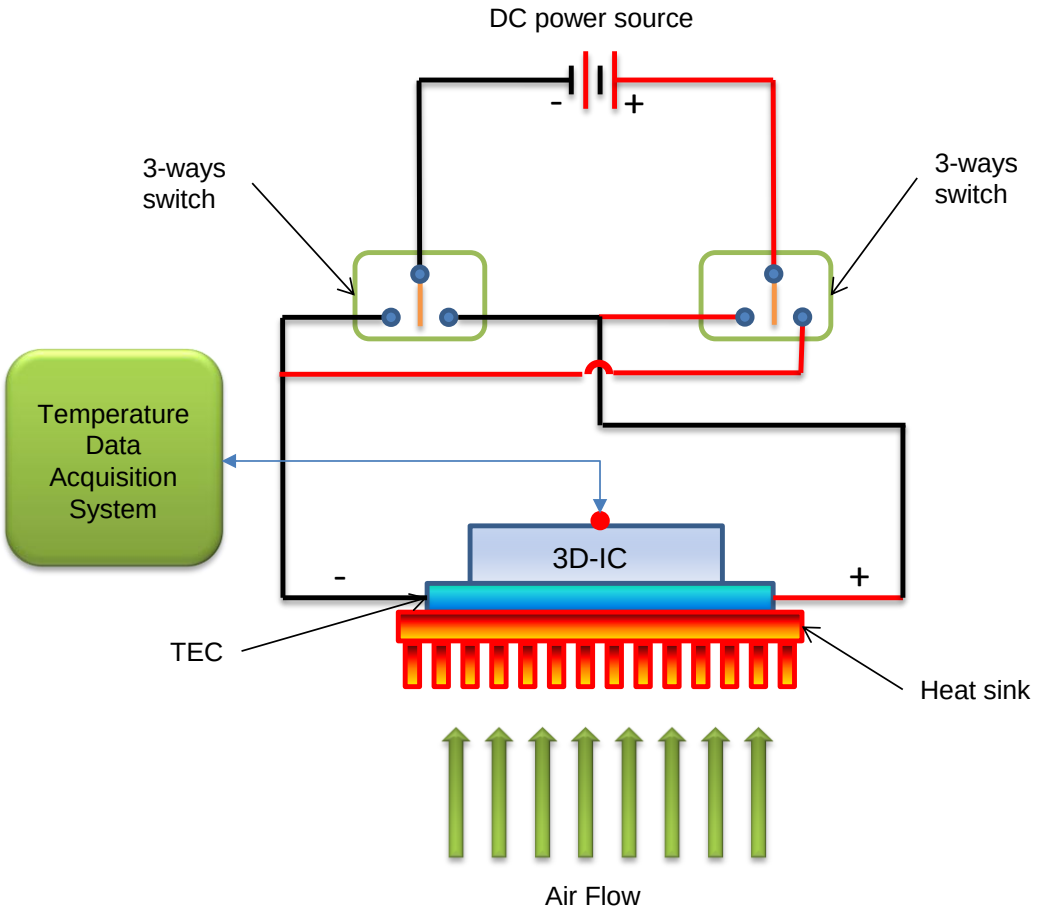


Figure 7.3 Electrical circuit setup to test the MTCS

7.2.2 Experimental procedure

Prior to the thermal cycling test, the processor was biased to ensure that the processor is in working condition. The processor power source was then disconnected and the MTCS was powered up with forward and reverse bias to create a sub ambient cooling and heating respectively to the processor. The inactive processor temperature was recorded at various air flow rates from 16.5 to 35.5 CFM and thermoelectric power input range was from 3 to 123W. These tests help to determine the optimum air flow rate corresponding to certain thermoelectric

power input, which helps to achieve 0°C and 120°C readout from the thermocouples attached at the base of the processor.

The MTCS and the processor were air cooled back to room temperature (22.7°C) prior to each thermal cycling test. Each thermal shock cycle comprised of a ramping up period from room temperature to 120°C, and then a dwelling period for 20 minutes at 120°C, and then a ramping down period from 120°C to 0°C. The temperature provided by the thermocouple embedded at the bottom of the package was recorded to ensure that the processor indeed reached the desire thermal cycling temperature. The test procedure was repeated five times to ensure data consistency.

After the thermal cycling test, the MTCS and the processor were once again air cooled back to room temperature and the processor was biased again to check for discontinuity or defects. Since this experiment was to test both the MTCS and the processor integrity, so the result is considered acceptable if the processor and the MTCS pass both the bias and the structural integrity tests. Any type of cracking of the processor, or separation, delamination of the thermoelectric modules from the core would be considered as a failure of the test.

7.3 MTCS experimental testing results and discussion

In the first test, the temperature of the processor reached 0°C or 120°C with the thermoelectric power input of 123W and an air flow rate of 35.5 CFM. The whole system was air cooled back to room temperature prior to the actual thermal cycling test. Figure 7.4 illustrates the thermal cycling result of the MTCS.

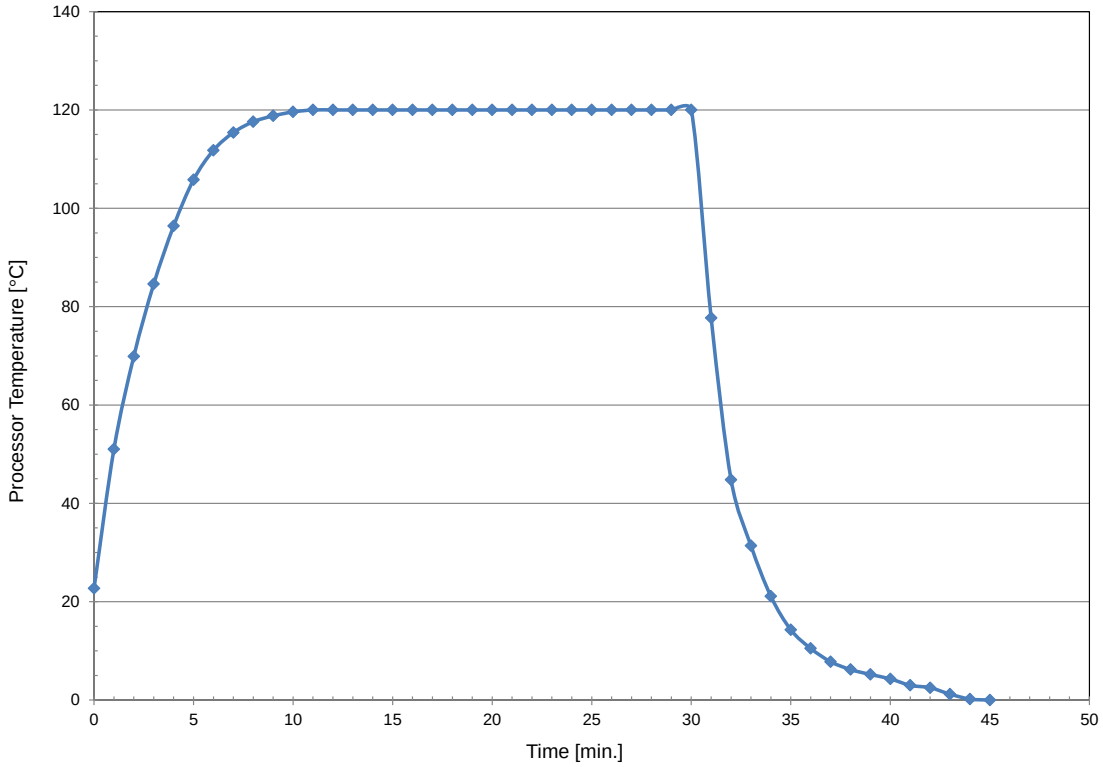


Figure 7.4 Thermal cycling result of the MTCS

For heating mode it took approximately 11 minutes to ramp from room temperature 22.7°C to 120°C. The MTCS was held at 120°C for 20 minutes and then it was switched to cooling mode from 120°C to 0°C, which took about 15 minutes to accomplish. Thermoelectric module is a solid state cooling and heating device, so multiple test will yield the same exact result as long as the input power to the thermoelectric module and the air flow rate were kept constant and consistent throughout the testing period.

The experiment can be verified using transient conduction equations as follow:

$$\rho C_p \frac{\partial T}{\partial t} = k \frac{\partial^2 T}{\partial x^2} \tag{16}$$

Where ρ represents the density *[kg/m^3]*, C_p is the specific heat *[kJ/kg·K]*, k is the thermal conductivity *[W/m·K]*, and x is the direction of the heat flow in the cold/hot core respectively *[m]*.

Equation 16 is then non-dimensionalized by using the thickness of the cold/hot core L, and T_o as the temperature of the cold/hot core at time $t = 0$, and T_∞ as the temperature of the interface between the core and the thermoelectric module as T_c approaches to time $t = \infty$ (Eq. 17, 18, and 19):

$$X = \frac{x}{L} \tag{17}$$

$$\theta = \frac{k\,t}{\rho\, C_p\, L^2} \tag{18}$$

$$T^* = \frac{T - T_\infty}{T_0 - T_\infty} \tag{19}$$

Equation 16 then becomes:

$$\frac{\partial T^*}{\partial \theta} = \frac{\partial^2 T^*}{\partial X^2} \tag{20}$$

Where:

The initial condition is now:

$$T^* = 1 \quad at \quad \theta = 0 \tag{21}$$

The boundary conditions are:

$$\frac{\partial T^*}{\partial X} = \pm Q_c \frac{L}{k}(T_0 - T_\infty) \quad at \quad X = 0 \tag{22}$$

$$\frac{\partial T^*}{\partial X} = 0 \quad at \quad X = 1 \tag{23}$$

Equation 23 indicates that the thermoelectric module is attached to the cold/hot core at $X = 0$, and the ± sign indicates whether the thermoelectric module is cooling or heating core respectively, and Q_C is the combine total power per unit area (flux) of all thermoelectric modules.

Using approximation analysis proposed by [46], Eq. 20 can be integrated about *X* from 0 to 1 by using relation:

$$\left[\frac{\partial T^*}{\partial X}\right]_1 = 0 \tag{24}$$

this yields:

$$\frac{\partial}{\partial \theta}\left(\int_0^1 T^* dX\right) = -\left[\frac{\partial T^*}{\partial X}\right]_0 \tag{25}$$

Using the following approximate relations, substitute Eq. 26 and 27 to Eq. 25:

$$T^* = T_C^* \tag{26}$$

$$T_C^* = \frac{\left[\frac{\partial T^*}{\partial X}\right]_0}{\left[\frac{\partial T^*(0)}{\partial X}\right]} \tag{27}$$

This yields the differential equation for $\left[\frac{\partial T^*}{\partial X}\right]_0$:

$$\frac{\partial}{\partial \theta}\left[\frac{\partial T^*}{\partial \theta}\right]_0 = -\left[\frac{\partial T^*(0)}{\partial X}\right]_0\left[\frac{\partial T^*}{\partial X}\right]_0 \tag{28}$$

Where the initial condition Eq. 21 is now become:

$$\left[\frac{\partial T^*}{\partial \theta}\right]_0 = \left[\frac{\partial T^*(0)}{\partial X}\right]_0 \quad at \quad \theta = 0 \tag{29}$$

The solution is expressed as:

$$\frac{\left[\frac{\partial T^*}{\partial \theta}\right]_0}{\left[\frac{\partial T^*(0)}{\partial X}\right]_0} = T_C^* = e^{\left\{-\left[\frac{\partial T^*(0)}{\partial X}\right]_0 \theta\right\}} \tag{30}$$

$$\tau = \frac{1}{\left\{\left[\frac{\partial T^*(0)}{\partial X}\right]_0 \theta\right\}} = \rho C_p L \frac{(T_0 - T_\infty)}{Q_C} \tag{31}$$

Equation 31 was used to verify the experiment result obtained. The heating cycle period time constant was found to be 11.22 minutes compared to the experimental result of 11.00 minutes. The small discrepancy between the analytical result and the experiment result is due to the fact that the analytical equations assumed perfect adiabatic condition (no thermal leakage) and the experimental system might exhibit some unforeseeable thermal leakage from inadequate system insulation.

Equation 31 can also be used to uncover how fast certain size of thermoelectric module could cool or heat certain thermal conducting material, which is firmly in contact with the thermoelectric if the power of the thermoelectric module, the properties of that material, and the desire before and after temperatures are known. In reverse Eq. 31 can also be used to find out what total thermoelectric power is needed to cool or heat certain size of material if a desire response time is a constraint.

It is noticed that, in order for this equation to agree well with the experimental data, all exposed surfaces of the cold/hot core must be insulated; otherwise, the thermoelectric cooler will continue to pump environmental temperature that leaks into the system, which will distort the result greatly.

7.4 Summary

The Multidimensional-Thermal-Cycling-System (MTCS) presented in this section utilized the third dimension to accommodate four or more thermoelectric modules in order to provide sub ambient cooling and heating of a 3D-IC from ambient to 120°C and maintained it at this temperature for 20 minutes before ramping down to 0°C. The entire process took 11 minutes to ramp up and 15 minutes to ramp down. Without the MTCS novel configuration, it is

impossible to package more than three thermoelectric modules into the same concentrated real estate surrounding the 3D-IC for thermal shock testing using multiples thermoelectric devices. The result obtained from this study was used as a foundation for the patent-pending MTCS utilizing solid state device in lieu of the bulky conventional thermal chamber to test different processor configuration to reduce overhead and infrastructure cost during development and demonstration phase of the design process.

CHAPTER 8

MULTIDIMENSIONAL THERMOELECTRIC ANALYSIS

8.1 Introduction

Comprehensive analysis of thermoelectric cooling system involves many parametric equations, which require solving complex mathematical equations or computational-fluid-dynamic (CFD) models. Conventionally, in order to analyze a thermoelectric cooling system, thermal designers relied on series of performance curves provided by the thermoelectric manufacturer. Most of the performance curves were plotted as a function of the temperature of the hot side of the thermoelectric module (T_h); however, T_h is normally neither known nor constant, so thermal designer is forced to estimate T_h and potential of error is introduced [51]. In many cases, the information needed to analyze thermoelectric module such as the height and the cross sectional area of the semiconductor pellets, or the Seebeck's coefficient are needed, but these information are considered as proprietary information, which manufacturers are reluctant to provide. In this chapter, a Modified-Graphical-Method (MGM) based on previous study by Lineykin and Ben-Yaakov was examined. The MGM provides quicker visualization of the cooling requirement using only common published parameters from any TEC manufacturers to obtain pertinent design information such as the optimum operating currents, temperature of the hot side, and coefficient of performance (COP) without the assistant of any proprietary information. Also, previous study by Lineykin and Ben-Yaakov was geared toward 1-D analysis and the MGM is designed for Multidimensional-Heat-Transfer-System (MHTS) [52].

8.2 Motivation

Lineykin and Ben-Yaakov [53], [54], [55] proposed a set of unified thermoelectric models and a graphical method was derived from this set of equations. Their methodology significantly reduced the need for multiple charts interpretation or complicated numerical method to obtain the design parameters. Also, their method claimed to have only about 5% errors or less compared to their experimental results, which is acceptable for speedy analysis by system-level thermal engineers. However, the author found Lineykin and Ben-Yaakov's graphical method is difficult to interpolate or extrapolate due to the parabola shape of the S-curve potentials. Figure 8.1 illustrates the issues of the current Lineykin and Ben-Yaakov's method.

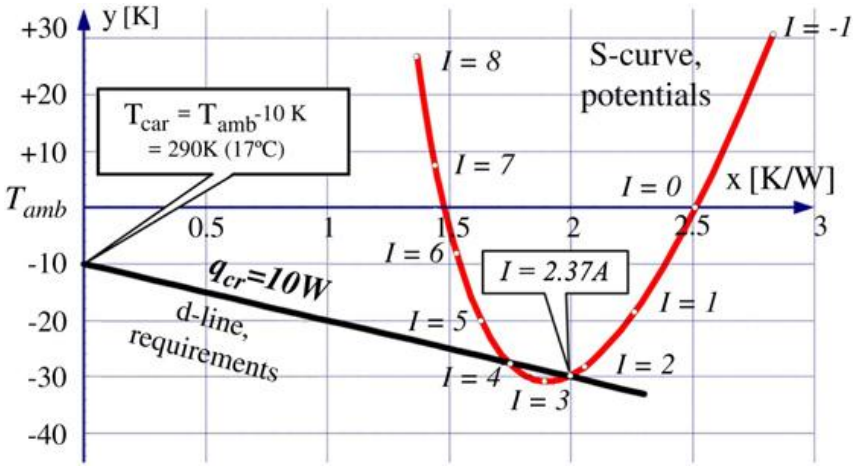


Figure 8.1 Lineykin & Ben-Yaakov's method of finding operating currents for TEC system [55]

Notice that the values of the currents (*I = -1 to I = 8*) shown on the S-curve potentials do not correspond to the values on the X-axis. Furthermore, the point of intersection between the d-line and the S-curve is the desired operating currents, but it is impossible to visually interpolate accurately the values of *I = 2.37 A* or *I = 4 A* on the parabola S-curve as illustrated

by the previous authors without searching through calculated data, which defeated the purpose of illustrating the results using a graphical method.

The objective of this study is to mathematically modified Lineykin, Ben-Yaakov's method to rectify the chart interpolation issues and to provide result-ready visualization of the required parameters for the Multidimensional Heat Transfer System (MHTS) utilizing multiple thermoelectric modules.

8.3 Modified-Graphical-Method (MGM) for single stage TEC

8.3.1 Operating current (I) calculation

Lineykin & Ben-Yaakov assumed that all thermoelectric couples are identical and the heat transfer is unidirectional along the thermoelectric pellets. All parameters are taken in first order approximation at steady state, temperature independent, and the small contribution of Thomson effect is negligible. Equation 32, 33 and 34 below were used to calculate the thermoelectric module parameters using only published manufacturer's data.

$$\alpha_m = \frac{U_{max}}{T_h} \tag{32}$$

$$R_m = \frac{U_{max}(T_h - \Delta T_{max})}{I_{max} T_h} \tag{33}$$

$$\Theta_m = \frac{\Delta T_{max}}{I_{max} U_{max}} \frac{2T_h}{(T_h - \Delta T_{max})} \tag{34}$$

Where α_m is the energy conversion of the thermoelectric cooler (TEC), U_{max} is the maximum voltage that the TEC draws at I_{max}, I_{max} is the maximum current that the TEC can handle at Q_c =

0, T_h is the hot side temperature of the TEC, R_m is the electrical resistance of the TEC, Θ_m is the thermal resistance of the TEC, and ΔT_{max} is the maximum differential temperature of the hot and cold side of the TEC. T_h is set to be the same as T_{amb} at initial condition.

The heat equations for both the cold (heat-absorbing) and the hot (heat-dissipating) sides of the TEC are shown below in equation 35 and 36 respectively:

$$Q_c = \alpha_m T_c I - \frac{\Delta T}{\Theta_m} - \frac{I^2 R_m}{2} \tag{35}$$

$$Q_h = \alpha_m T_h I - \frac{\Delta T}{\Theta_m} + \frac{I^2 R_m}{2} \tag{36}$$

The electrical section of the module is described as an electrical resistance R_m in series with an emf-source is depicted in equation 37 below:

$$V = \alpha_m \Delta T + I R_m \tag{37}$$

T_h (temperature of the hot side of the TEC) can be expressed in terms of ambient temperature T_{amb}, the amount of heat pumped Q_c, and the heat sink thermal resistance Θ_k as:

$$T_h = T_{amb} + Q_c \Theta_k \tag{38}$$

Commercial equation-solver software such as Mathematica® was used to eliminate Q_h, T_h, and V from equation 35 to 38 to obtain an expression for T_c. Finally, the temperature difference between the cold side of the TEM, T_c and the surrounding temperature, T_{amb} is shown in equation 39 below:

$$T_{ca} = (T_c - T_{amb}) = (Q_c * X_o) + \Delta T_{km}(I) \quad (39)$$

and the module thermal resistance, $\Theta_{km}(I)$, and the differential temperature of the TEC with heat sink as function of operating current, $\Delta T_{km}(I)$ are expressed in equation 40 and 41 below:

$$\Theta_{km}(I) = \frac{A^2}{B}\Theta_m \quad (40)$$

$$\Delta T_{km}(I) = \frac{C\Theta_k + A\Theta_m\left(\frac{C}{2} - I\alpha_m T_{amb}\right)}{B} \quad (41)$$

Where:

$$X_o = \Theta_k + \Theta_{km}(I) \quad (42)$$

$$A = 1 - I\alpha_m\Theta_k \quad (43)$$

$$B = 1 + AI\alpha_m\Theta_m \quad (44)$$

$$C = I^2 R_m \quad (45)$$

Figure 8.2 below is an illustration showing key parameters used in this analysis:

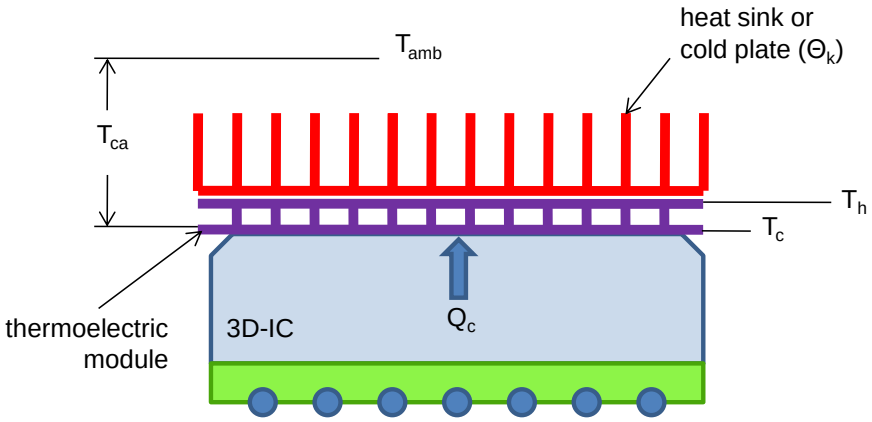


Figure 8.2 Schematic of a cooling system using TEC

A Modified-Graphical-Method (MGM) required at least two important parameters. The first parameter is the desired differential cooling temperature of the object to be cooled, which is denoted as ΔT. For instance, if T_{amb} is 300K and the processor needs to be maintained at T_c = 290K, then ΔT is equal to 10K as shown in equation 46, and N is the number of identical TEC used.

$$\Delta T = \frac{T_{amb} - T_C}{N} \tag{46}$$

The second required parameter is the power dissipation of the processor, which is denoted as Q_{req}. Once these two parameters were established, the variable X_n was calculated using equation 47, where X_o is initial value when $X_{n=0}$. The MGM solution for a desire cooling requirement is a single plot of the Targeted-Temperature-Achievable-Error (TTAE) as a function of operating current that drives the TEC to achieve the desire cooling requirement as shown in equation 48. Ultimately, the TTAE is preferred to be 0.0%, which means that for a given set of

design parameters such as the heat sink thermal resistance and desire differential temperature ΔT, the cooling target has been achieved. For a range of heat sink thermal resistances, Θ_k and TEC manufacture's parameters, a new set of curve, which is denoted as P_c-curve can be plotted for comparison purposes.

$$X_n = \frac{N\left(-\Delta T - \Delta T_{km}(I)\right)}{Q_{req}} \tag{47}$$

$$TTAE = \frac{\left|X_N - X_o\right|}{X_o} \tag{48}$$

The MGM was verified by way of an example of a one single stage TEC, which was used in previous paper by Lineykin & Ben-Yaakov. The first two major known requirements were the hot object power output, Q_{req} = 10 W, which needs to be maintained at 10K below ambient temperature (T_{amb} = 300K), so ΔT = 10K. The TEC manufacturer parameters for a TB-127-1,4-1,2 are [56]: I_{max} = 7.6A, V_{max} = 15.9V, ΔT_{max} = 70K, and heat sink thermal resistance, Θ_k = 1 K/W, and an assumption was made that $T_h = T_{amb}$ for initial condition.

The following TEC parameters were generated from equation 32, 33 and 34 respectively: Θ_m = 1.51 K/W, α_m = 53 mV/K and R_m = 1.6 Ω. These TEC parameters were then inserted into equation 40-45 to obtain Θ_{km} and $\Delta T_{km}(I)$. Equation 47 was used to obtain X_n corresponding to different values of currents I in the range recommended by the manufacturer. A plot of TTAE, equation 48, as a function of operating currents I was generated as shown in Fig. 8.3. Noticed that two optimum operating currents were found immediately from the MGM chart for this configuration (I = 2.375 A or 4.05 A). The result shown in Figure 8.1 is identical to the result shown in Figure 8.3, but interpolation was not needed when using the MGM.

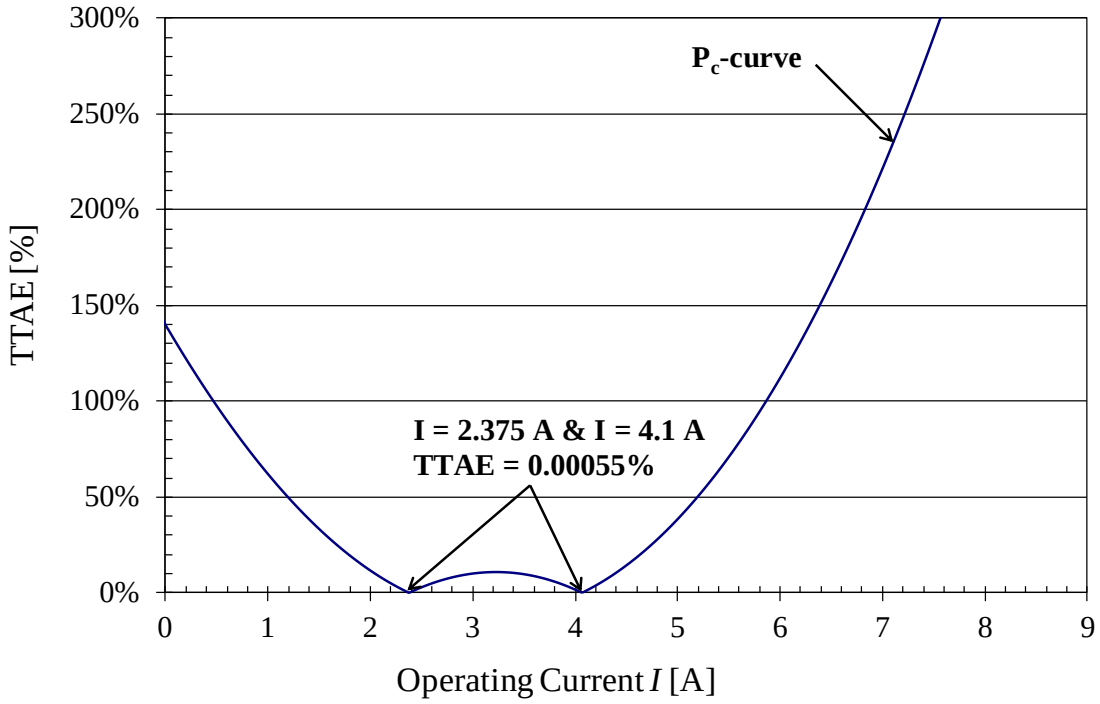


Figure 8.3 MGM test result for a single stage TEC (TB-127-1.4-1,2)

Similarly, if different heat sinks were analyzed, series of P_c-*curves* can be plotted on the same plot in order to observe different design scenarios. An example of different heat sink thermal resistances: Θ_k = 0.25, 0.5, 0.75, 1.0, and 1.25 K/W respectively is illustrated in Figure 8.4 below.

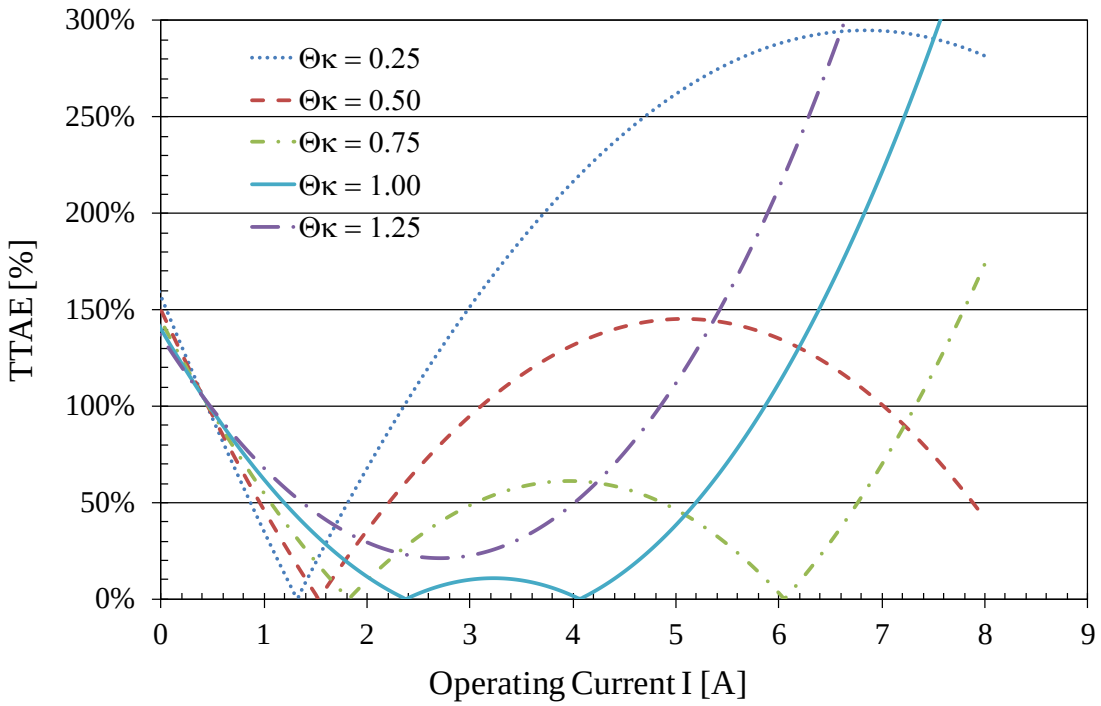


Figure 8.4 MGM graph of different P_c-*curves* for different heat sink thermal resistances θ_k

Notice: for the values of Θ_k below 1.0 K/W, the thermoelectric module required lower current because the heat sink has higher thermal conductivity. On the other hand, when the thermal resistivity, Θ_k was above 1 K/W, for instance, in the case of Θ_k = 1.25 K/W, the P-curve would never intersect with the TTAE axis of 0% because for this particular TEC (TB-127-1,4-1,2) the heat sink with Θ_k = 1.25 K/W was not capable of evacuating the total heat generated by the processor and the TEC. From this MGM multi-graph, thermal designers can immediately visualize the cooling requirement for this processor for different heat sink thermal resistivity without the need for complicated multi-graphs interpretation or interpolation of calculated data.

8.3.2 Temperature of the hot side (T_h) calculation

Overheating of the hot-side of a TEC is also a major concern for thermal design engineers, so combine the concept proposed by Lineykin/Ben-Yaakov and MGM, a temperature of the hot side (T_h) can be calculated using the following equations. Commercial equation-solver software such as Mathematica was used again to eliminate Q_c, T_c, and V from equation 35 to 38 to obtain an expression for T_h below:

$$\Delta T_{ha} = T_h - T_{amb} = Q_c \Theta_{kmh}(I) + T_{hkm}(I) \tag{49}$$

Where:

$$\Theta_{kmh}(I) = \frac{\Theta_k}{B} \tag{50}$$

$$\Delta T_{hkm}(I) = \left(\frac{I^2 R_m}{2}\Theta_k\right)\left(\frac{D+2E}{B}\right) \tag{51}$$

$$D = I\alpha_m \Theta_m \tag{52}$$

$$E = 1 + \frac{\alpha_m^2 \Theta_m T_{amb}}{R_m} \tag{53}$$

For different values of operating currents I, equation 52-53 were applied into equation 50-51 to obtain $\Theta_{kmh}(I)$ and $\Delta T_{hkm}(I)$ and ΔT_{ha} (equation 49). T_h was found by plotting equation 49 as a function of equation 48 above. The result of the same example is illustrated in Figure 8.5. The TEC hot-side temperature was found by adding the values found at TTAE (0%) on the

P_h-*curve* and the known value of T_{amb}=300 K, so $T_h = \Delta T_{ha} + T_{amb}$ = 23°C + 26.85°C = 49.85°C or 76.8°C if 49.95°C was used respectively. The result of ΔT_{ha} obtained using MGM also matched with the result presented in [55] and again no graphical interpolation or data mining was exercised. Note that for an inadequate design parameter of heat sink thermal resistance (Θ_k) neither P_c nor P_h curve will achieve a TTAE of 0% (i.e. the P_c or P_h curve would never intersect the *X-axis* in either case).

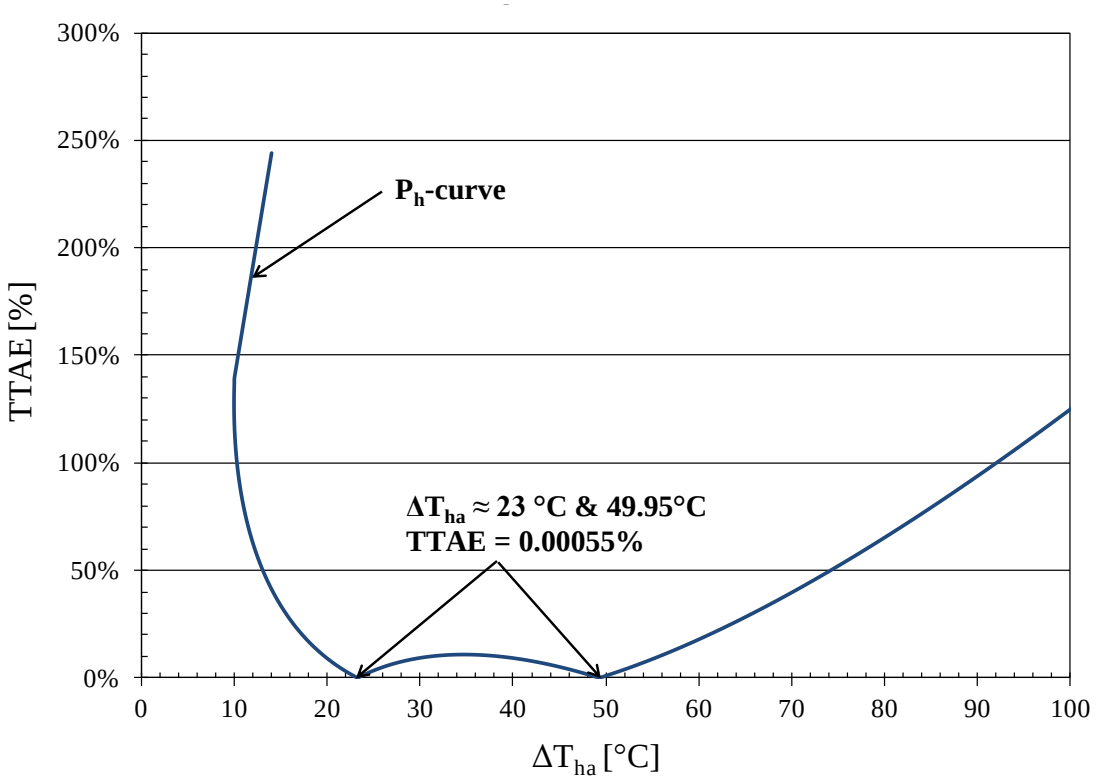


Figure 8.5 MGM graph of the P_h-*curve* to obtain the TEC hot side temperature

8.3.3 Coefficient of performance (COP) calculation

Coefficient of Performance (COP), which is the ratio of the heat pumped to the energy required to pump that heat can be represented by equation 23 below. In addition, Lineykin and Ben-Yaakov recommended multiplying the nominator and the denominator of Eq. 54 with the heat sink thermal resistivity, Θ_k [55].

$$COP = \frac{Q_c}{Q_h - Q_c} = \frac{Q_c \Theta_k}{(Q_h \Theta_k) - (Q_c \Theta_k)} = \frac{a}{T_{ha} - a} \tag{54}$$

Where: $a = Q_c * \Theta_k$

Since "a" is the heat sink surface temperature, which is above ambient temperature, when I = 0 [A], so equation 55 was further modified to:

$$COP = \frac{a}{T_{ha} - a} = \frac{\Delta T_{ha}(I = 0)}{\Delta T_{ha}(I = optimum) - \Delta T_{ha}(I = 0)} \tag{55}$$

COP is a single value corresponding to specific operating condition, so graphical method was not needed to calculate this value, instead the two values in the data that made up the P_h-*curve* (ΔT_{ha} at I = 0 and ΔT_{ha} at I = optimum condition) for equation 55 were used. At I = 0 A, ΔT_{ha} = 10°C and at I = 2.375 A, ΔT_{ha} = 23.229°C (as shown in Figure 8.5 also) the COPs were estimated using equation 55 to be 0.756 and 0.25 respectively if I = 4.1 A was used. The COP results estimated in this study also agreed with results obtained using Lineykin and Ben-Yaakov's graphical method [55].

8.4 Modified-Graphical-Method (MGM) calculation for MHTS

Similarly, the MGM was used to verify the MHTS experimental results with 4 single-stage TECs. In this case, the processor was energized at 25W, and the desire temperature of the cold side is T_c = 13.4°C, T_{amb} = 20°C. The air flow rate through the MHTS was 22.05 CFM. The heat sink thermal resistivity θ_k = 1.4 K/W can be found using heat sink data in Appendix A. The TEC manufacture data are: I_{max} = 10 A, V_{max} = 15.4 V, ΔT_{max} = 68 K, and an assumption was made that $T_h = T_{amb}$ for initial condition.

The following TEC parameters were generated from equation 32, 33 and 34 respectively: Θ_m = 1.144 K/W, α_m = 52 mV/K and R_m = 1.189 Ω. These TEC parameters were then inserted into equation 40-45 to obtain Θ_{km} and $\Delta T_{km}(I)$. Equation 47 was used to obtain X_N corresponding to different values of currents I in the range recommended by the manufacturer. A plot of TTAE, equation 48, as a function of operating currents I was generated as shown in Fig. 8.3. Noticed that two optimum operating currents were found immediately from the MGM chart for this configuration (I = 1.35 A and 3.875 A). The result shown in Figure 8.6 agreed with I = 3.9 A operating condition for the experimental case.

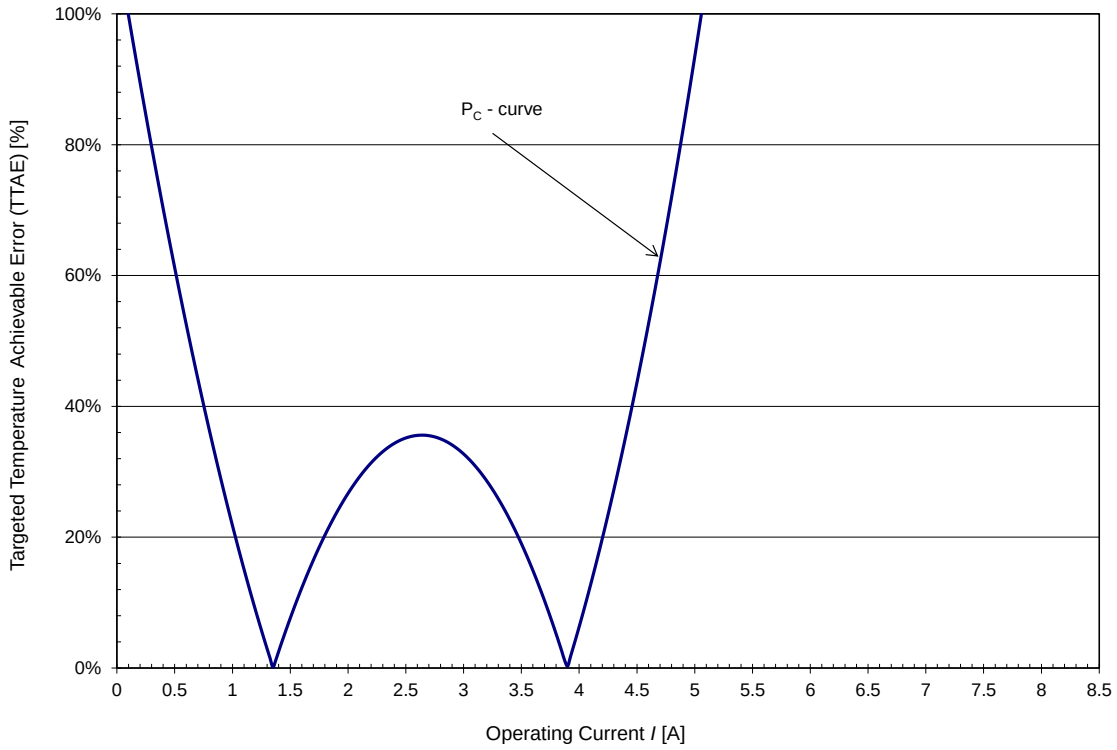


Figure 8.6 MGM test result for the MHTS

Similarly, if different heat sinks were analyzed for the MHTS, series of P_c-*curves* can be plotted on the same plot in order to observe different design scenarios. An example of different heat sink thermal resistances: Θ_k = 0.25, 0.5, 0.75, 1.40, and 2.0 K/W respectively is illustrated in Figure 8.7 below.

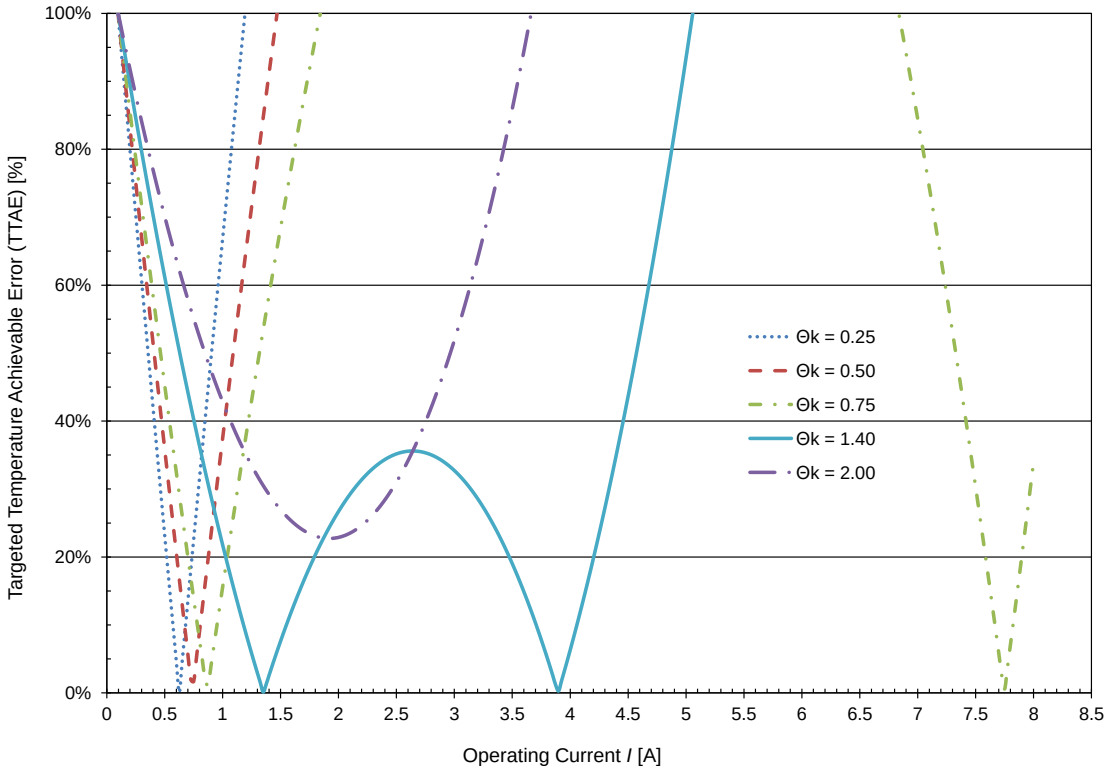


Figure 8.7 MGM graph of different P_c-*curves* for different heat sink θ_k of the MHTS

A heat sink with thermal resistant of 2.00 K/W would not be suitable for this MHTS because the targeted cold temperature will never be reached.

Next, the temperature of the hot side of the TEC can also be obtained. For different values of operating currents I, equation 52-53 were applied into equation 50-51 to obtain $\Theta_{kmh}(I)$ and $\Delta T_{hkm}(I)$ and ΔT_{ha} (equation 49). T_h was found by plotting equation 49 as a function of equation 48 above. The result of the same example is illustrated in Figure 8.8. Finally, the COP for the MHTS using the MGM method was found to be 0.222 compared to the experimental result of 0.247.

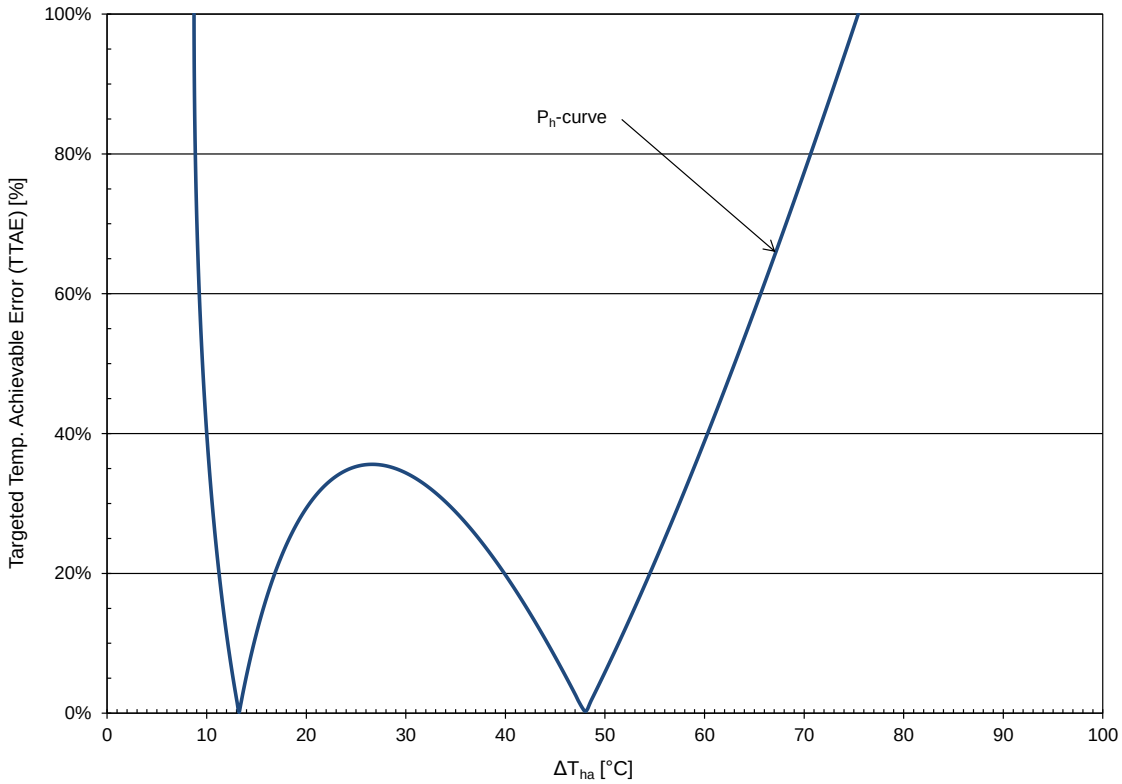


Figure 8.8 MGM graph of the *P_h-curve* to obtain the hot side temperature of the MHTS

8.5 Summary

In this chapter, an alternative method of analyzing thermoelectric cooling system using Modified-Graphical-Method (MGM) was presented. MGM method illustrated the flexibility of obtaining pertinent design parameters such as the operating current, the hot side temperature and the coefficient of performance without the need of multi-graphs interpolation or proprietary information, which normally will not be available to thermoelectric module designers. MGM can provide result-ready right on the graph and multiple design scenarios could also be studied at the same time. Thermal system designers can apply MGM to quickly estimate the adequacy of

certain heat sink or TEC sizes, but by no mean MGM replaces CFD modeling for more complex and precision systems.

CHAPTER 9

FUTURE WORK

The study of Multidimensional-Heat-Transfer-System to be used for sub ambient cooling of three dimensional integrated circuits (3D-IC) yield significant progress in addressing the difficulty of sub cooling a complex three dimensional active power systems whether it is a 3D processor or a 3D System-in- Package (3D-SiP). Several patents were or in the process to be filed with the U.S Patents office at the time that this dissertation was written:

The first patent was filed with the U.S Patents office in February of 2011, which is related to the MHTS for different heat loads as shown in Fig. 9.1 and 9.2 below. The next three patents are related to innovative ways to package 3D-IC/3D-SiP system to be integrated with the MHTS, heat pipes, nano-fluid or any combination thereof as shown in Fig. 9.3, 9.4, and 9.5. The fifth patent is related to the Multidimensional-Thermal-Cycling-System (MTCS) as shown in Fig. 9.6.

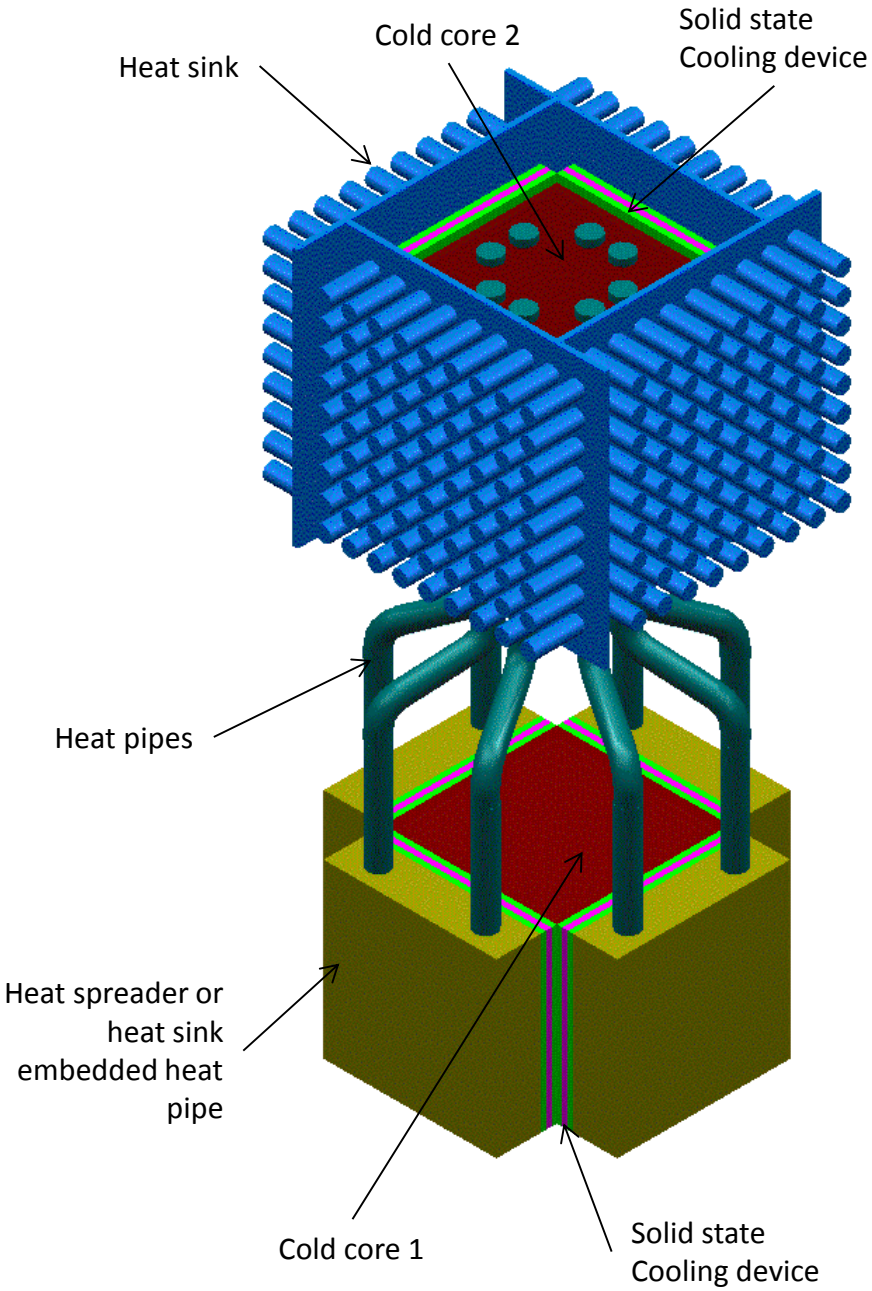


Figure 9.1 MHTS utilizing heat pipes to improve heat load

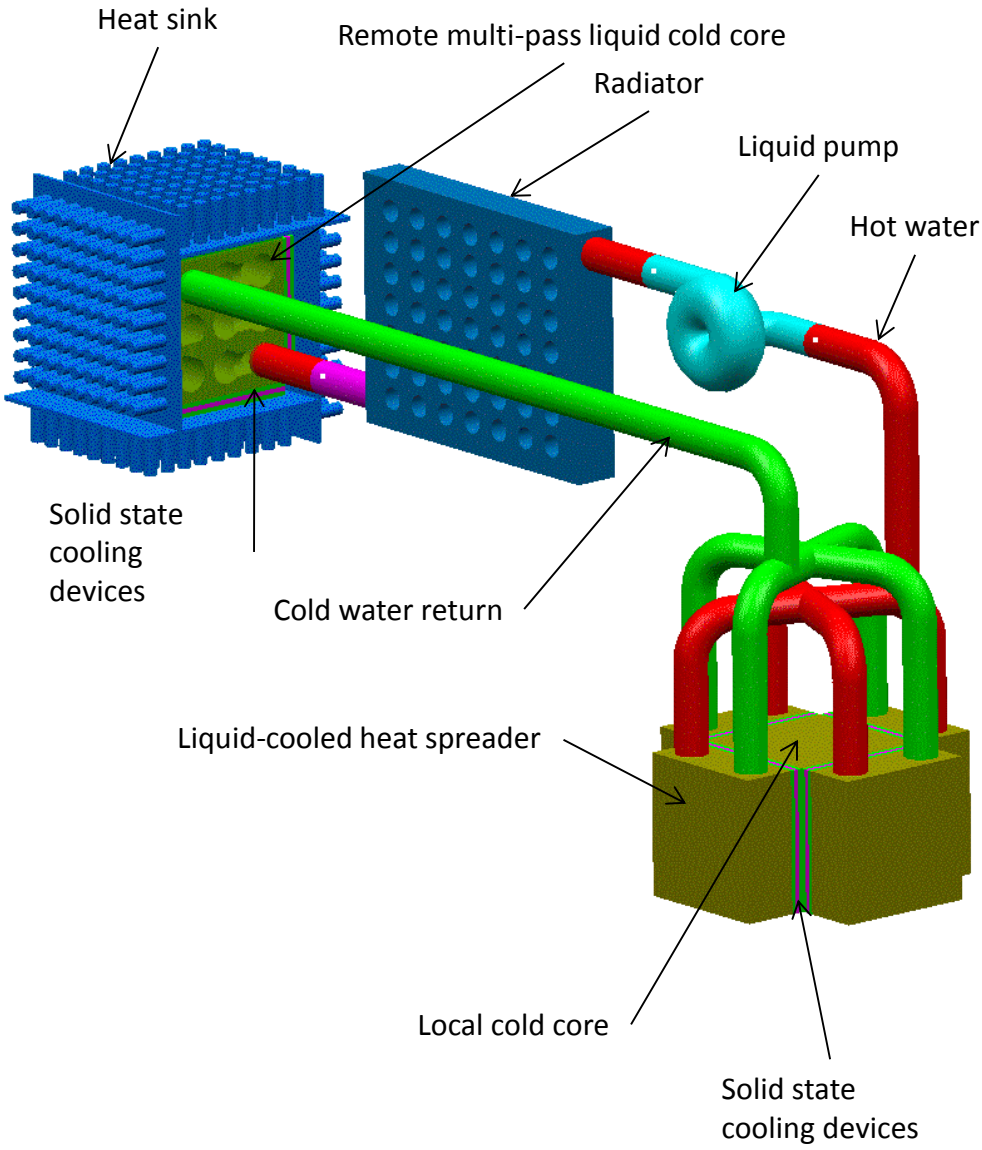


Figure 9.2 MHTS utilizing nano-fluid to improve heat load

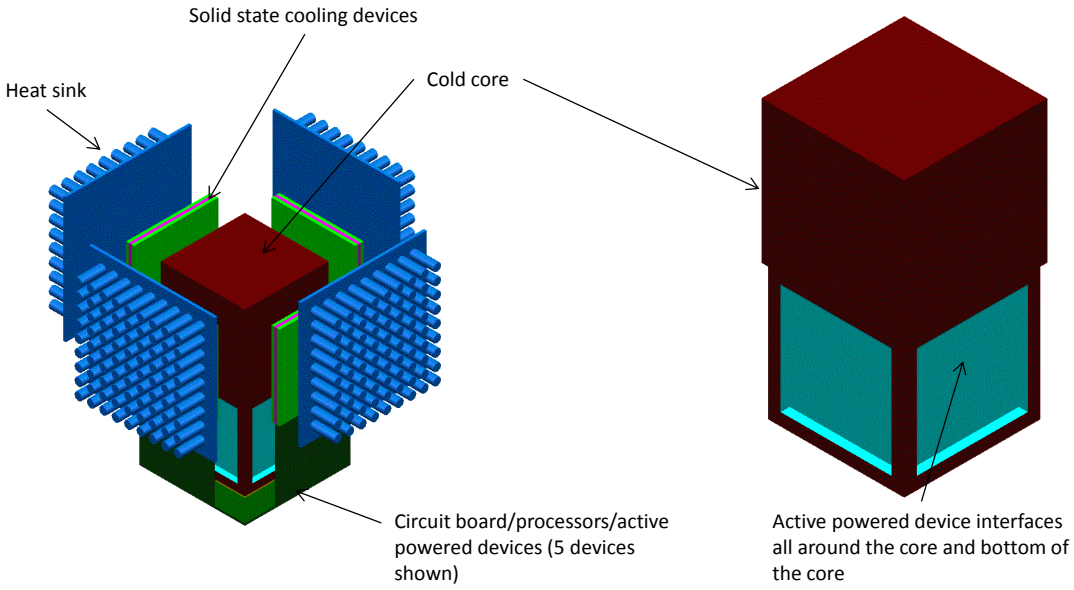


Figure 9.3 3D-IC/3D-SiP packaging with single cold core for sub ambient cooling

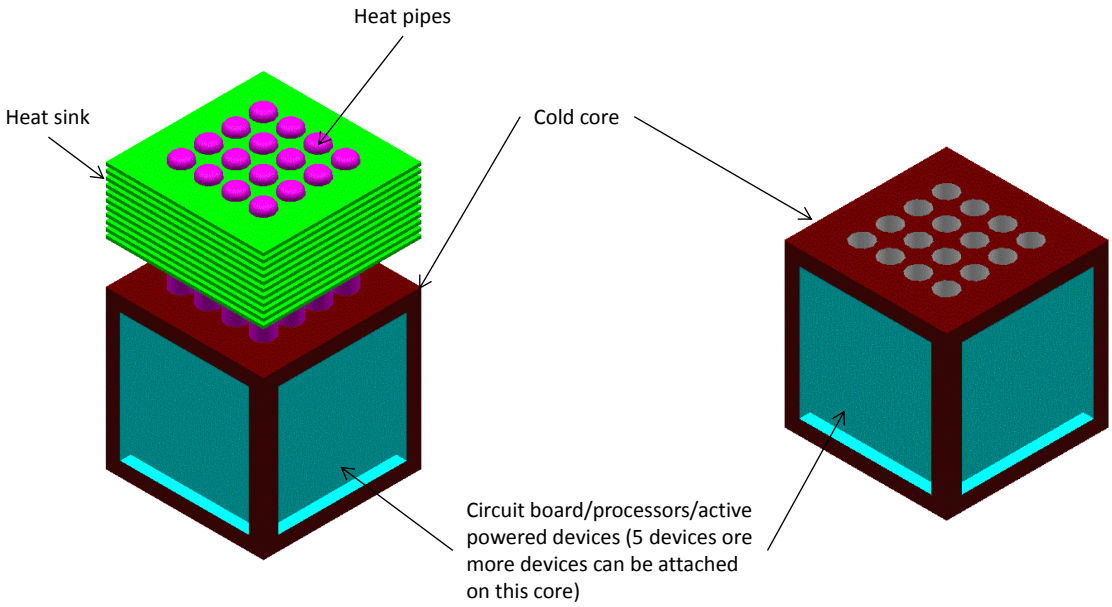


Figure 9.4 3D-IC/3D-SiP packaging with single cold core for using integrated heat pipes

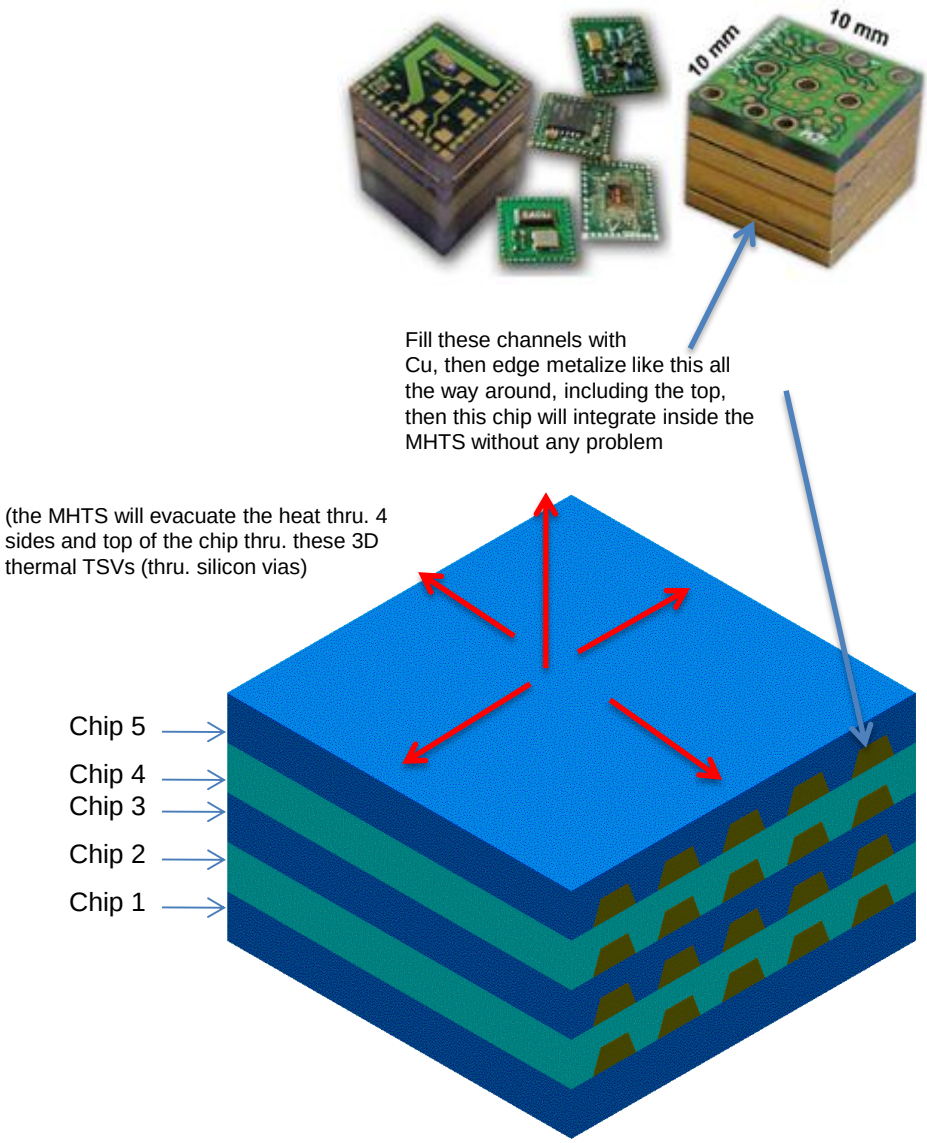


Figure 9.5 3D-IC/3D-SiP packaging sandwich with heat conducting channel or layers

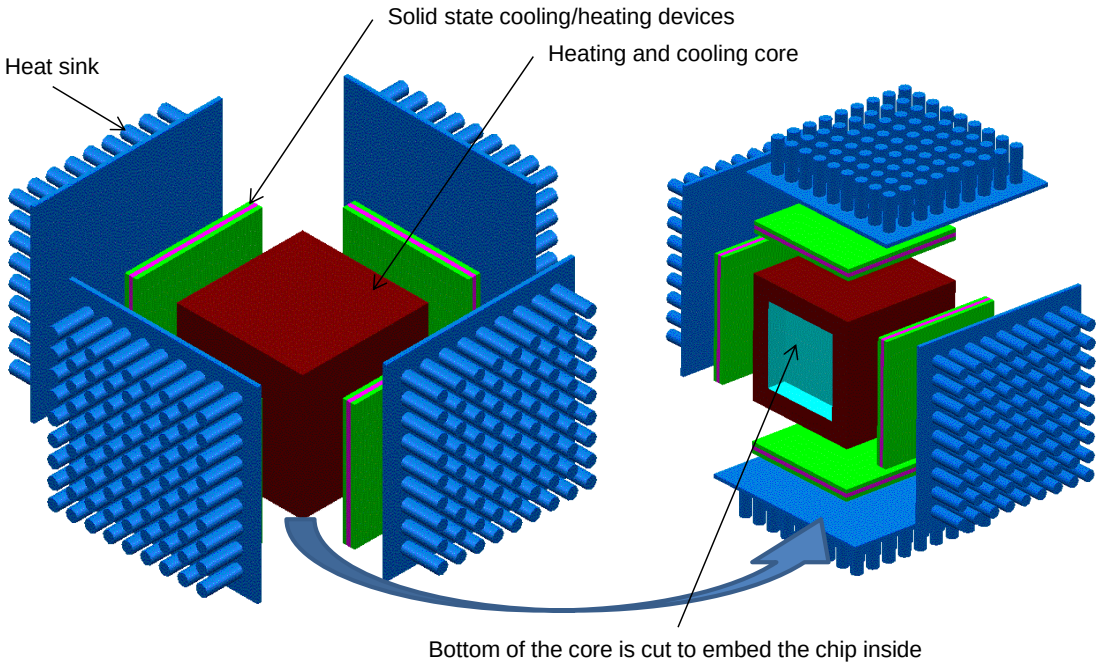


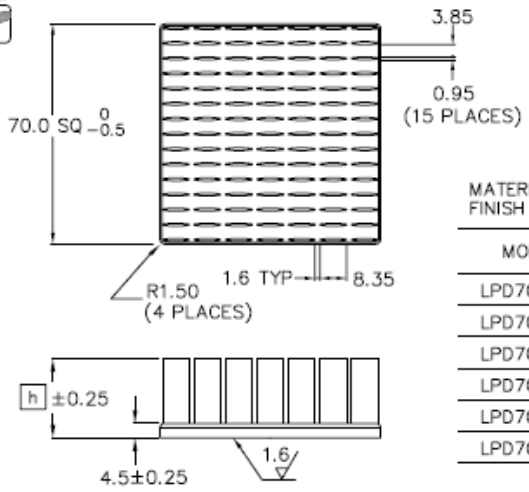
Figure 9.6 Multidimensional-Thermal-Cycling-System (MTCS) for 3D-IC/3D-SiP

APPENDIX

ALPHA COMPANY ALUMINUM HEAT SINK

ALPHA Low Pressure Drop Heat Sink LPD 70

DIM

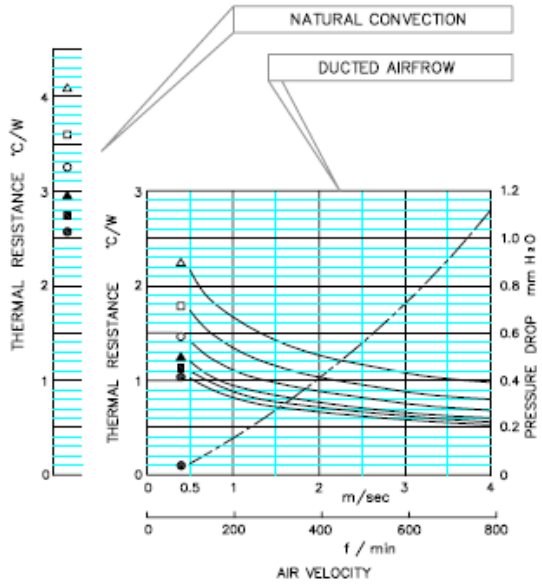


MATERIAL : A 6063
FINISH : BLACK ANODIZE

MODEL	HEIGHT h	WEIGHT (grams)
LPD70−15B	15	77.4
LPD70−20B	20	85.7
LPD70−25B	25	94.0
LPD70−30B	30	102.3
LPD70−35B	35	112.0
LPD70−40B	40	121.0

Dimensions : mm

DATA



△ LPD70−15B
□ LPD70−20B
○ LPD70−25B
▲ LPD70−30B
■ LPD70−35B
● LPD70−40B

Thermal Resistance (Ducted)
(Solid Line ———)
Pressure Drop
(Center Line —·—)

Based on Alpha's Standard Test Procedure. (Refer to page marked Technical Information.)
Dummy Heater Size : □12.7(mm)

Natural Convection Tests
Dissipated Power: 13.3(W)
Dummy Heater Size : □25.4(mm)

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