THERMAL FAILURE MECHANISM AND VOLTAMMETRY METROLOGY FOR CU/BARRIER/LOW K INTEGRATION

by

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ABSTRACT

THERMAL FAILURE MECHANISM AND VOLTAMMETRY METROLOGY FOR CU/BARRIER/LOW K INTEGRATION

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The present study investigates the thermal stability of Cu/barrier/porous low κ (PLK) integration first, and then a new characterization method based on voltammetry is developed to characterize quality of diffusion barrier and pore structure in low κ materials and its thermal stability. The study of thermal stability reveals that Cu/barrier/PLK interconnect fails by Cu out-diffusion through the defects of diffusion barrier into the PLK structure, which is driven by oxidation and stress gradient within the interconnect structure. The failure appears to be triggered by defects in diffusion barrier, however, such defects are not effectively detected by TEM observation due to their small and localized nature. This motivates the development of a new method to characterize defects of diffusion barrier and pore structure of low κ materials in as-

processed Cu/barrier/PLK interconnect. Firstly, a cyclic voltammetry-based method is developed to detect the quality of diffusion barrier by monitoring the current resulting from an applied voltage on the established cell. It utilizes a fact that electrolyte solution is able to infiltrate into the low k layer between two interconnects and creates a situation essentially the same as two-electrode electrolytic cell. When the barrier is intact (defect-free), the I-V shows simple hysteresis without the presence of current peaks. On the other hand, when the barrier is defective, Cu is exposed to electrolyte and current peak is present in the I-V curve due to Cu redox reactions. The application of the developed method on an extensive number of real interconnects provides sufficient evidence that the method is simple, fast, and accurate in detecting the defective barrier. Furthermore, it has a potential to quantify defect density based on the intensity of the current peak and the integration areas within the I-V curves. Secondly, a step voltammetry-based method is developed to characterize pore structure by measuring the effective ions diffusivity. The study produces the identical activation energy and diffusivity results for bulk solution which are in good agreement with references, and reveals that electrolyte ions migrate in dense low κ (DLK) and PLK with different mechanism. The application of the method reveals that pores in low κ materials are not thermally stable but can either collapse or coalesce depending on the stress conditions.

TABLE OF CONTENTS

ACKNOWLEDGEMENTS iii

ABSTRACT v

LIST OF ILLUSTRATIONS xiii

LIST OF TABLES xx

NOMENCLATURE xxi

Chapter

1. INTRODUCTION 1

1.1 Motivation 1

1.2 Background 1

1.2.1 Modern Interconnect Technology 1

1.2.2 Cu Metallization: Dual-Damascene Process 7

1.2.3 Challenges in Cu/PLK Interconnect 10

1.2.3.1 Diffusion Barrier 10

1.2.3.2 Low κ Materials 14

1.3 Objectives and Significance of This Thesis 20

1.4 Overview of Chapters 21

2. STUDY ON THERMAL STABILITY OF Cu/PLK STRUCTURE 23

2.1 Samples and Experimental 23

2.1.1 Samples 23

2.1.2 Experimental 25

2.2 Results … 26

2.2.1 Thermal Instability of Cu interconnect 26

2.2.1.1 Tested Under Air Ambient 26

2.2.1.2 Tested Under Inert Ambient 29

2.2.2 Microscopy Characterization 30

2.3 Discussion: Mechanism of Thermal Instability 35

2.3.1 Oxidation Mechanism 35

2.3.1.1 Source of Oxidants 35

2.3.1.2 Oxidation Mechanism 37

2.3.1.3 Kinetic Mechanism for Cu Out-Diffusion 38

2.3.2 Stress Mechanism 41

2.3.3 The Role of Diffusion Barrier on Thermal Instability 43

2.3.4 The Role of Porous Low κ Materials on Thermal Instability 44

2.4 Summary 45

3. VOLTAMMETRY-BASED METHODOLOGY FOR CHARACTERIZATION OF Cu/LOW-κ INTEGRATION 47

3.1 Motivation for a New Characterization Methodology 47

3.2 The Proposed Characterization Methodology 49

3.2.1 The Methodology for Barrier Defects Characterization 49

3.2.1.1 Cyclic Voltammetry Basic 49

3.2.1.2 Electrolytic Cell for Voltammetry 51

3.2.1.3 The Working Principle for Barrier Defect Characterization 53

3.2.2 The Methodology for Low κ Structure Characterization 57

3.2.2.1 Step Voltammetry Basic 57

3.2.2.2 The Working Principle for Low κ Structure Characterization 58

3.3 Samples and Experimental Apparatus 59

3.3.1 Samples 59

3.3.2 Experimental Apparatus 60

3.4 Summary 62

4. STUDY OF BARRIER STABILITY USING VOLTAMMETRY 64

4.1 The Development of Fundamental Theory 65

4.1.1 Sample and Test Condition... 65

4.1.2 Simulation of Various Conditions of Diffusion Barriers.......... 67

4.1.2.1 Simulation of Intact Barriers 67

4.1.2.2 Simulation of Symmetric Defective Barriers 70

4.1.2.3 Simulation of Asymmetric Defective Barriers 72

4.1.2.4 Simulation of Intact/Defective Barrier 75

4.2 Barrier Detection for Real Interconnect 78

4.2.1 Sample Preparation.. 78

4.2.2 Results.. 80

4.2.2.1 Initial Conditions of as-Received Samples......... 80

4.2.2.2 Cu Interconnect with Intact Barrier 81

4.2.2.3 Cu Interconnect with Equal Density of Defects in Barrier 83

4.2.2.4 Cu Interconnect with Unequal Density of Defects in Barrier 83

4.3 Reaction Mechanism of Cu in the Established System 86

4.3.1 Cu Reaction in the Established System 86

4.3.2 Cu Reaction in Two Asymmetric Electrodes 89

4.4 Significance and Consideration 91

4.4.1 Considerations for Industry Application................................. 91

4.4.2 The Potential Applications.. 92

4.4.2.1 Evaluation of Capping Layer Integrity 92

4.4.2.2 Evaluation of Pore-seal Integrity 96

4.4.2.3 Evaluation of Ionic Contamination for Package Substrate 96

4.5 Summary 97

5. CHARACTERIZATION AND INVETIGATION OF THERMAL STABILITY FOR LOW-κ STRUCTURE USING VOLTAMMETRY 99

5.1 Development of Characterization Technique 100

5.1.1 Samples and Test Conditions 100

5.1.2 Current Profile in the Step Voltammetry Method 101

5.1.2.1 Charging vs. Discharging Current 102

5.1.2.2 Discharging Current vs. Porosity 105

5.1.3 Analytic Model for Discharging Current................................ 106

5.1.3.1 Concentration Profile of Ions during Discharging Current 106

5.1.3.2 The Solution of Discharging Current 108

5.2 Characterization of Low κ Structure 109

5.2.1 Effective Diffusivity of Electrolyte Ion 109

5.2.2 Ion Diffusion Mechanism 111

5.3 Investigation of Structure Instability for PLK Materials........................ 113

5.3.1 Samples and Test Conditions... 113

5.3.2 Results and Discussion 114

5.4 Significance and Consideration 116

5.5 Summary 117

6. CONCLUSION AND FUTURE WORK.. 119

6.1 Conclusions 119

6.1.1 Thermal Failure of Cu/PLK Integration 119

6.1.2 Characterization Technique: Voltammetry-based Method 120

6.1.2.1 Evaluation of Defects in Diffusion Barrier 120

6.1.2.2 Characterization of Low κ Materials 121

6.2 Future Work 122

6.2.1 Characterization of Diffusion Barrier 122

6.2.2 Characterization of Low κ Structure..................................... 122

6.2.3 Extend Application of the Voltammetry Technique.............. 123

Appendix

A. I-V MODEL OF A RC CIRCUIT WITH

A LINEAR VOLTAGE SWEEP 124

B. THE SOLUTION FOR CONCENTRATION PROFILE 128

C. THE SOLUTION OF DISCHARGING CURRENT.................................... 132

REFERENCES 136

BIOGRAPHICAL INFORMATION.. 145

LIST OF ILLUSTRATIONS

Figure | Page

1.1 Gate and interconnect delay as a function of minimum feature size for Al/SiO_2, Cu/SiO_2 and Cu/low κ interconnects.. 2

1.2 The requirement metal layers for technology generation with various interconnect/low κ construction.. 4

1.3 Cu metallization characteristic of six-level structure (Courtesy of T.Way, IBM Microelectronics Division, Burlington, VT)............................ 5

1.4 A cross-section of hierarchical scaling-MPUs (Microprocessor) devices (2005 ITRS roadmap, Interconnect) 6

1.5 Process flow comparison for Al RIE vs. Cu Dual-Damascene...................... 8

1.6 Process flow comparison for Al RIE vs. Cu Dual-Damascene (Continuation of figure 1.5).. 9

1.7 Correlation of thermal conductivity and dielectric constant (dark square) represents the experimental data for the porous MSQ. Curve (a) is for the porous MSQ and (b) for the porous silica. Oval (c) includes various dense ISG materials, and (d) includes various dense polymeric low κ. 16

1.8 Interconnect line temperature increase (T_{line}-$T_{substrate}$) as a function of the dielectric thermal conductivity 17

2.1 (a) An optical image of test pattern; a cross section schematic of (b) one level (c)two level Cu/barrier/PLK structure....................................... 24

2.2 A schematic representative of the experimental apparatus 26

2.3 A plot showing resistance (ratio) of a 0.25μm single level Cu interconnect with different barrier arrangement baked at 275°C with low level intermittent current, 0.1 mA/cm^2 in air atmosphere....................... 27

2.4 A plot showing resistance (ratio) of a single level with different barrier arrangement and temperature with low level intermittent current, 0.1mA/cm^2 in air atmosphere. 28

2.5 A plot showing resistance (ratio) of a single level, 0.25μm Cu lines with 25nm Ta barrier as a function of baking time at 325°C. Note that N_2/Ar ambient substantially delays the failure, but cannot prevent the process. 29

2.6 A typical SEM top-down image taken from 0.25μm wide Cu lines with a 30SiCN/2Ta barrier after 135 hours of baking at 225°C. Note only one of Cu lines is applied current in this test pattern. 30

2.7 A typical SEM cross-section image of vias under bond pad in two-level Cu interconnect with 25nm Ta after 45 hours of baking at 225°C. Note that Cu bands from outside of each via (both sides)............................ 31

2.8 Cross-section TEM images, taken after baking (a) at 275°C in air showing the formation of dark spots contrast near to a 0.25μm Cu trench with 50 nm SiCN/0.5nm Ta arrangement. (b) at 225°C in air showing band and spots of dark contrast near to 0.25μm Cu trench with 30 nm SiCN/2nm Ta arrangement. The diffraction ring pattern analysis taken from the circle areas indicates that Cu exists outside the trench as the stable oxide phases, either CuO after 225°C baking or Cu_2O after 275°C 32

2.9 A top-down view TEM micrograph after baking at 275°C in Ar/ N_2 ambient showing no noticeable Cu out diffusion observed in PLK next to a 0.25μm Cu trench with 25nm Ta arrangement. (a) An extrusion was observed through Ta barrier of the sample tested in Ar ambient (b) No noticeable extrusion was observed of the samples tested in N_2 ambient. 34

2.10 Optical images show the micrograph of acetone infiltration into Cu/PLK structure from the edge after 5 min even with the presence of the scribe seal. Note the dark contrast indicates the infiltration of acetone (a) dark field (b) bright field.. 36

2.11 Failure mechanism driven by oxidation potential (a) Cu interconnect fails by Cu out-diffusion into PLK forming Cu_xO there and leaving

voids in the lines (b) Normal oxidation occurs by interdiffusion between Cu and O through Cu_xO without voiding formation. 37

2.12 A plot displays the reciprocal resistance ratio of 0.25μm Cu lines with different barrier arrangement and temperature as a function of the root of baking time 40

2.13 A plot showing the slope of R_0/R_t vs. $t^{1/2}$ for various temperature and barrier as a function of 1/KT. 41

2.14 (a) Cu diffuses out of the line through the defects in diffusion barrier in Ar test (b) the reaction of Ta and N_2 repairs the defects in diffusion barrier protecting Cu out diffusion in N_2 ambient. 42

3.1 The potential waveform in a cyclic voltammetry... 50

3.2 The typical current-voltage (I-V) curve in a cyclic voltammetry 51

3.3 A schematic of a two-electrode electrochemical cell..................................... 52

3.4 A schematic for working principle (a) Electrolyte solution infiltrates in the two electrodes (b) The current resulted from ionic charging under the applied voltage in the case of an intact barrier (c) The current resulted from both Cu redox reaction and ionic charging in the case of a defective barrier... 54

3.5 An intact barrier presents the hysteresis I-V curve (b) under a cyclic potential sweep (a) 55

3.6 The presence of current peaks suggests a defective barrier 56

3.7 The waveform of potential step voltammetry and the responding current as a function of time 57

3.8 A schematic diagram of (a) comb pattern (b) a cross-section comb structure test pattern 60

3.9 A picture (a) and a circuit schematic (b) of the build up apparatus 61

4.1 Schematic diagrams for idealized samples with controlled Cu fraction (0-100%) used for fundamental study

(a) top-down view (b) cross-section view 65

4.2 A schematic diagram of I-V test using idealized samples 66

4.3 The typical current data as a function of time under the applied cyclic voltage in the case of two Ta electrodes, simulating the intact diffusion barrier 67

4.4 I-Vs are taken from two Ta electrodes at various sweep rates 68

4.5 I-Vs are taken from two Ta electrodes under various sweep voltages............ 68

4.6 The typical current data as a function of time under the applied cyclic voltage in the case of electrode with symmetric Cu fraction (100% Cu on two mating electrodes in this figure) simulating the defective diffusion barrier with equal defects density. 69

4.7 A typical I-V is taken from two Cu electrodes (100% Cu)............................ 70

4.8 A typical I-V is taken from two identical electrodes with 65% Cu exposure.. 71

4.9 The peak area as a function of Cu fraction in idealized samples. 72

4.10 I-V taken from electrodes with asymmetric Cu fraction, 1% Cu vs. 5%Cu.. 73

4.11 The I-Vs taken from electrodes with asymmetric Cu fraction, 1%Cu vs. 65%Cu at (a) initial sweep cycle (b) very last sweep cycle. 74

4.12 The I-Vs taken from electrodes with asymmetric Cu fraction, 0%Cu vs. 5% Cu, at (a) sweep rate: 0.23 V/min (b) sweep rate: 0.046V/min............... 76

4.13 An I-V curve taken from two Ta electrodes with asymmetric electrodes' areas: one electrode has an area of 1×1 cm^2 and the other has an area of 10×1 cm^2 77

4.14 The optical image of Cu/DLK interconnect with comb/via chain Structure (a) low magnification (b) high magnification 79

4.15 A typical I-V taken from the initial condition of single level Cu/PLK interconnects with comb structure 80

4.16 A typical I-V taken from the initial condition of two-level Cu/DLK interconnects with comb/via chain structure 81

4.17 The representative I-Vs show a simple hysteresis, indicating an intact barrier, taken from (a) two level Cu/10nmTa/DLK with comb/via chain structure (b) single level Cu/25nmTa/PLK interconnect with comb structure. 82

4.18 I-V curves, taken from singel level comb structure Cu/25nmTa/PLK interconnect, show show symmetric current peaks, suggesting defective barrier with equal defects density 84

4.19 The I-Vs, taken from taken from single level comb structure Cu/25nm/PLK interconnect, shows asymmetrical current peaks, suggesting that one barrier is more defective than the other 85

4.20 I-V, taken from single level comb structure Cu/25nmTa/PLK interconnect, shows a single peak for forward sweep, suggesting one intact and one defective barrier. 85

4.21 The I-V, taken from two level comb/via chain structure Cu/10nmTa/DLK interconnect, shows a single peak for forward sweep, suggesting one intact barrier and one defective barrier 86

4.22 Plots of Cu redox reaction as a function of time and applied voltage (a) I/V-t curves for the first half-cycle (0V-0.7V-0V) potential sweep (b) I/V-t curves for a half-cycle potential sweep (after the first cycle) (c) I-V curve for 0V-0.7V potential sweep 88

4.23 An optical image of capping layer test pattern and its schematic representative cross section. Note both M1 and M2 are Cu 93

4.24 A representative I-V, taken from the samples after immersed into electrolyte solution, does not show any current signal, suggesting an intact capping layer. 94

4.25 A representative I-V shows a simple hysteresis, suggesting a defective capping layer 95

4.26 An example of a defective capping layer shows a current peak 95

5.1 Current as a function of time under double step voltage sweep taken from single level 0.25µm Cu/PLK interconnects with 0.30µm space........... 101

5.2 A comparasion of current decay during charging and discharging process, taken from single level 0.25µm Cu/PLK interconnects with 0.30µm space.. 102

5.3 The impact of applied voltage on discharging current, taken from 0.175µm single level Cu/PLK interconnects with 0.175µm space. The initial current values responding to various voltages are given in the plot. 103

5.4 The impact of applied voltage on charging current, taken from 0.25µm single level Cu/PLK interconnects with 0.30µm space. The initial current values responding to various voltages are given in the plot.. 104

5.5 Normalized discharging current as a function of time measured at 25°C for three different sample groups. For clarity, the high current spike is runcated. Note also that the all cell currents diminish to zero at the long time limit.. 105

5.6 Discharging current is taken from Cu/DLK and its fitting data..................... 109

5.7 Discharging current as a function of time with varying porosity of dielectrics between two mating electrodes: Group 1 is Cu/DLK with ~10% porosity; Group 2 is Cu/PLK with ~45% porosity and group 3 is idealized sample with 100% porosity 110

5.8 Diffusivities of ions as a function of reciprocal temperature......................... 112

5.9 Diffusivity in DLK as a function of the annealing temperature. Circles represent comb structure patterns of 0.25µm Cu line and 0.20µm low κ spacing, while squares represent those with 0.35µm low κ................. 114

A.1 A Schematic of an RC circuit.. 125

A.2 Curent-time (i-t) behavior resulting from a linear

potential sweep applied to an RC circuit 126

A.3 Curent-time and current potential (i-E) resulting from a cyclic linear potential applied to an RC circuit 127

LIST OF TABLES

Table | Page

1.1 ITRS Roadmap 2005 Edition. 6

5.1 The effective ions diffusivity of three groups of samples 110

5.2 Effective diffusivity of electrolyte ions measured at three different temperatures 111

NOMENCLATURE

BTS	biased thermal stressing
C	capacitance
CMP	chemical-mechanical polishing
CTE	coefficient thermal expansion
CVD	chemical vapor deposition
DLK	dense low κ
EM	electromigration
IC	integrated circuit
ILD	interlayer dielectric
ITRS	International Technology Roadmap for Semiconductor
I-V	current-voltage
κ	dielectric constant
MPU	microprocessor
MSQ	methyl silsesquioxane
PALS	positronium annihilation lifetime spectroscopy
PLK	porous low κ
Ps	positronium

PVD	physical vapor deposition
R	resistance
RIE	reactive-ion etching
SAXN	small angle x-ray and neutron
SEM	scanning electron microscopy
SXR	specular x-ray reflectivity
TEM	transmission electron microscopy
TDDB	time dependent dielectric breakdown
ULSI	ultra-large scale integration

CHAPTER 1

INTRODUCTION

1.1 Motivation

The transition to Cu/low κ interconnect from Al/SiO_2 creates many challenges for future microelectronic devices. Among those, the development of a reliable diffusion barrier and successful implementation of porous low κ (PLK) are considered as two of the most critical challenges for a reliable Cu interconnect. The continuous shrinking in thickness of the diffusion barrier coupled with the incorporation of pores in low κ materials enables new failure mechanisms which are not found in Cu/SiO_2 and Cu/dense low κ (DLK) interconnect structures. Therefore it is necessary to investigate the potential factors that create new failure mechanisms in this structure to optimize the manufacturing processing and achieve a reliable and functional device. However, the efforts are slowed by the conventional characterization techniques that used to be suitable for Al/SiO_2 and/or Cu/DLK. Therefore it is extremely critical to develop new metrologies for advanced Cu/PLK integration.

1.2 Background

1.2.1 Modern Interconnect Technology

Since Jack Kilby demonstrated integrated circuit (IC) in 1958, the feature size continuously has scaled down and the density of devices will keep increasing in modern

IC as long as fundamental limits allow. The miniaturization coupled with high devices density results in a tremendous cost advantage and faster transistor switching times, and thereby improves the performance [1, 2]. However, the aggressive miniaturization of IC devices as well as the requirement for multiple metallization layers creates lots of challenges, and one of the most fundamental challenges is known as interconnect RC (product of resistance and capacitance) delay.

With the continuous reduction in the dimension of devices, the conducting wires, referred to as interconnects, are becoming narrower and more-closely spaced. Consequently, the resistance (R) of an interconnect increases due to the reduction in its cross-sectional area and the capacitance (C) of interlayer dielectric (ILD) materials increases because of the closer space between the interconnects. This phenomenon is

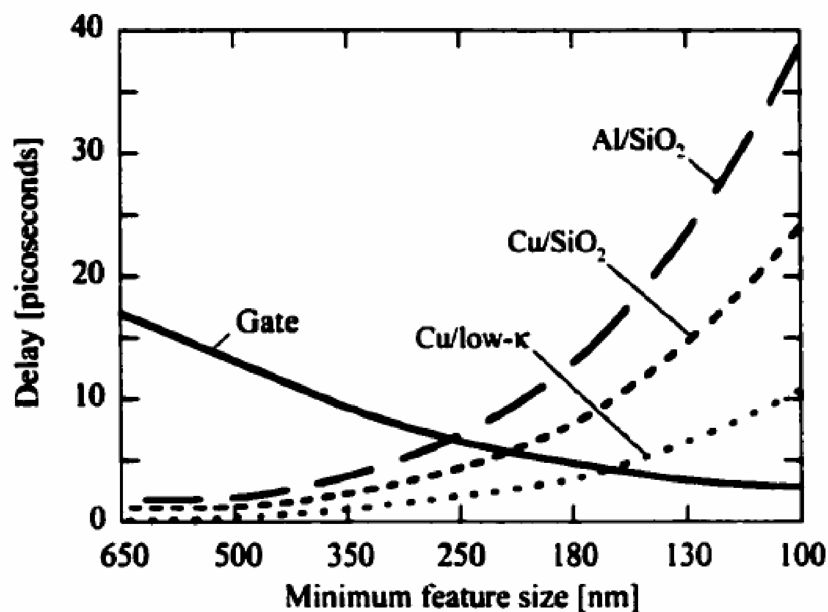


Figure 1.1 Gate and interconnect delay as a function of minimum feature size for Al/SiO_2, Cu/SiO_2 and Cu/low κ interconnects [4]

referred as interconnect RC delay, which becomes the bottleneck and limits the speed of logic devices instead of gate delay as the devices scale down into the submicron regions [3,4] , as shown in figure 1.1.

The attempt to reduce the interconnect RC delay initiated an extensive study of new materials in the microelectronics industry to replace the Al/SiO_2 interconnect that suffers from major limitations in RC delay due to its relatively high electrical resistivity. The selection of proper materials for advanced ICs is guided by the definition of RC delay, which is given by equation 1.1 [8]

$$RC = \frac{\rho}{t^M}\frac{L^2\kappa\varepsilon_0}{t_{ILD}} \tag{1.1}$$

where ρ, t^M, L are the resistivity, thickness, length of the interconnection, and ε_0, κ and t_{ILD} are permittivity of free space, interlevel dielectric (ILD) constant and thickness, respectively. As implied in the equation, the RC delay can be reduced by choosing the materials with low resistivity (ρ) as the interconnect and low dielectric permittivity (ε) as the insulator.

Of the metals with lower resistivity than Al (Ag, Cu and Au), Cu has been considered to be the best candidate to replace Al as interconnects due to its low resistivity, high electromigration (EM) resistance and its simple and low cost processing [6-9]. Its lower resistivity of 1.67μΩ-cm versus 2.69μΩ-cm for Al, provides significant benefit to RC delay. Although Ag has the lowest room temperature resistivity of any metal (1.60μΩ-cm), the difficulties in processing and rapid diffusion in dielectrics especially in the presence of an electric field make it less desirable than others.

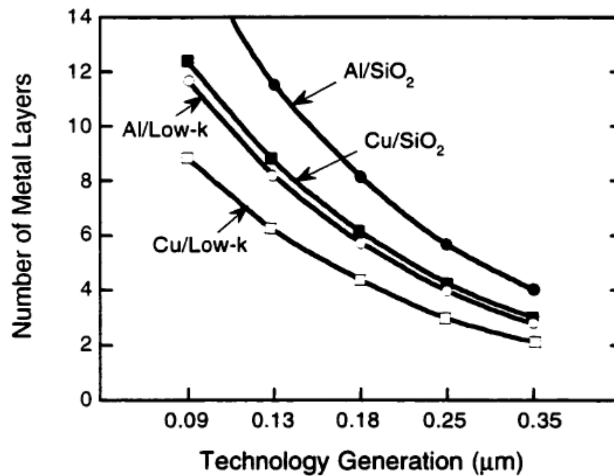


Figure 1.2 The requirement metal layers for technology generation with various interconnect/low κ construction [5]

In the past years, Cu has been used as interconnects in commercial chips primarily due to its low resistivity [10-11]. By using Cu, narrow lines can be used to carry the same amount of current, and a tighter packing density can be achieved per interconnect level. This means that fewer levels of metal are needed for the entire interconnect structure, leading to significant reduction of manufacturing costs. As seen in figure 1.2, it requires 8 to 9 metallization layers for 90nm technology node if using Cu/low κ instead of 11 to 12 layer if using Al/low κ [5]. The early chip technology combined up to six Cu wiring levels at ULSI (ultra-large scale integration) densities, as shown in figure 1.3.[12-13]. Figure 1.4 shows a cross-section of hierarchical scaling-MPUs (Microprocessor) devices presenting in 2005 International Technology Roadmap for Semiconductors (ITRS) in Interconnect section. It shows a high number of metal layers with a hierarchical wiring approach of steadily increasing pitch and thickness at each conductor level to alleviate the impact of interconnect delay on performance[14].

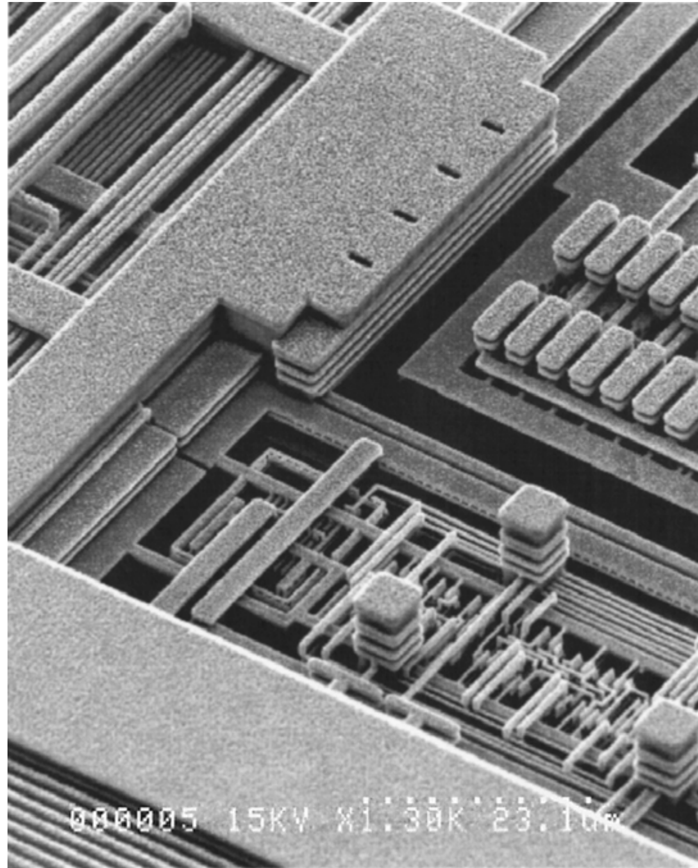


Figure 1.3 Cu metallization characteristic of six-level structure (Courtesy of T.Way, IBM Microelectronics Division, Burlington, VT)

Meanwhile, extensive study has been conducted to investigate low dielectric constant (κ) materials, both organic and inorganic, to replace conventional SiO_2 [15-17]. Based on 2005 ITRS for interconnect (table 1.1), the target for κ value of the low κ materials is less than1.6 in 2020 [14]. None of the dense dielectric low κ (DLK) materials is found to achieve such low κ, and therefore pores are being introduced into the low κ materials to further reduce the κ value to meet the needs for future technology

since vacuum has the lowest κ value of 1 [18-21]. They are termed porous low κ (PLK) materials.

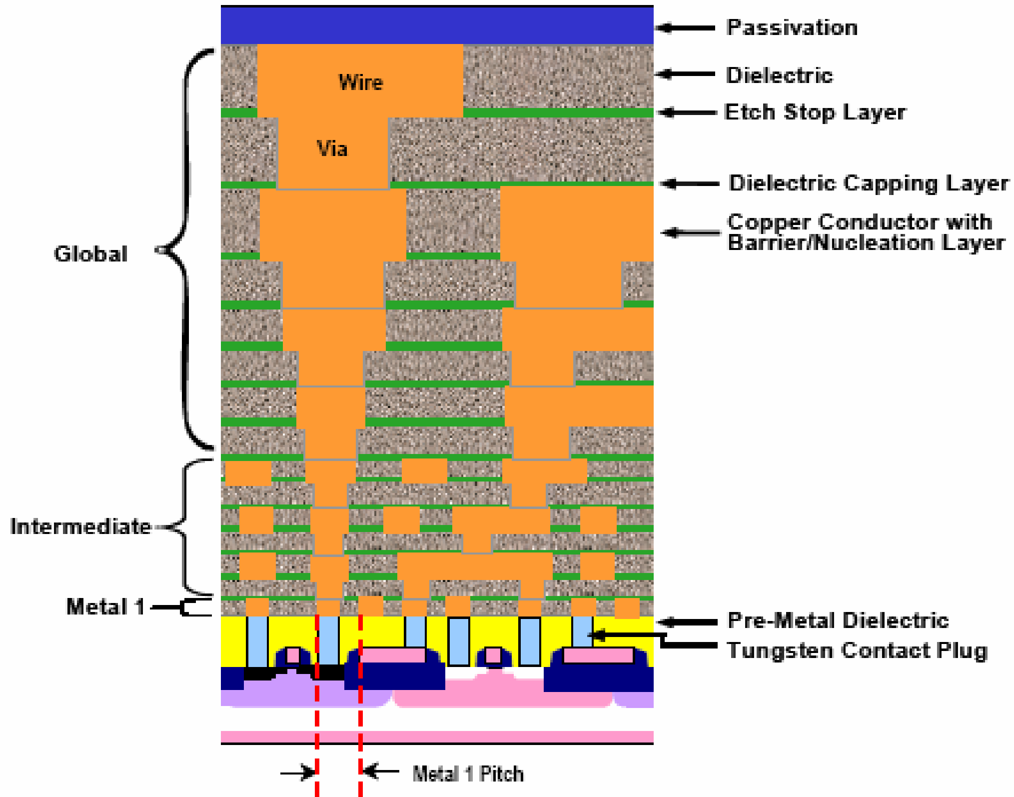


Figure 1.4 A cross-section of hierarchical scaling-MPUs (Microprocessor) devices (2005 ITRS roadmap, Interconnect)

Table 1.1 ITRS Roadmap 2005 Edition [14]

Year	2007	2008	2009	2010	2011	2013	2015	2017	2020
Technology Node (nm)	65	57	50	45	40	32	25	20	14
Metal Levels	11	12	12	12	12	13	13	14	14
Barrier thickness (nm)	4.8	4.3	3.7	3.3	2.9	2.4	1.9	1.5	1.1
ILD-κ_{bulk}	≤2.4	≤2.4	≤2.2	≤2.2	≤2.2	≤2.0	≤1.8	≤1.8	≤1.6

1.2.2 Cu Metallization: Dual-Damascene Process

The flow of dual-damascene processing has been well established for Cu fabrication during the past years because the conventional reactive-ion etching (RIE) of Cu films has an unacceptably low etching rate due to the low vapor pressure of Cu halides at room temperature [22].

The dual-damascene process flow is illustrated schematically in figure 1.5. For comparison, the conventional Al RIE process is also described. In the dual damascene process, the planar dielectric layer is deposited first and the metallization pattern is etched into this dielectrics. Metals, including a thin diffusion barrier layer and a thin seed layer for the subsequent Cu deposition process, are then deposited by either physical vapor deposition (PVD) or chemical vapor deposition (CVD). A Cu layer is deposited by electroplating to fill the metallization patterns, and the excess metal and barrier layer are then removed by a chemical-mechanical polishing (CMP) process, which provides a planar surface with in-laid interconnect patterns. Finally, a thin layer of silicon nitride is deposited to form a passivation layer [23].

As is seen in figure 1.5, the dual Damascene process involves fewer steps than the RIE process used to fabricate Al interconnects. It eliminates or reduces the need for some of the most difficult and costly steps. For example, dielectrics (ILD) CMP is eliminated. Some steps are simiplified: ILD gap-fill, a challenging issue in Al process, is replaced by simple planar deposition in Cu damascene, Al RIE is replaced by the simpler and higher-integrity ILD RIE in Cu damascene, and W CVD is replaced by Cu electroplating, which costs only about 1/3-1/5 of W CVD. In addition, Cu lines and vias

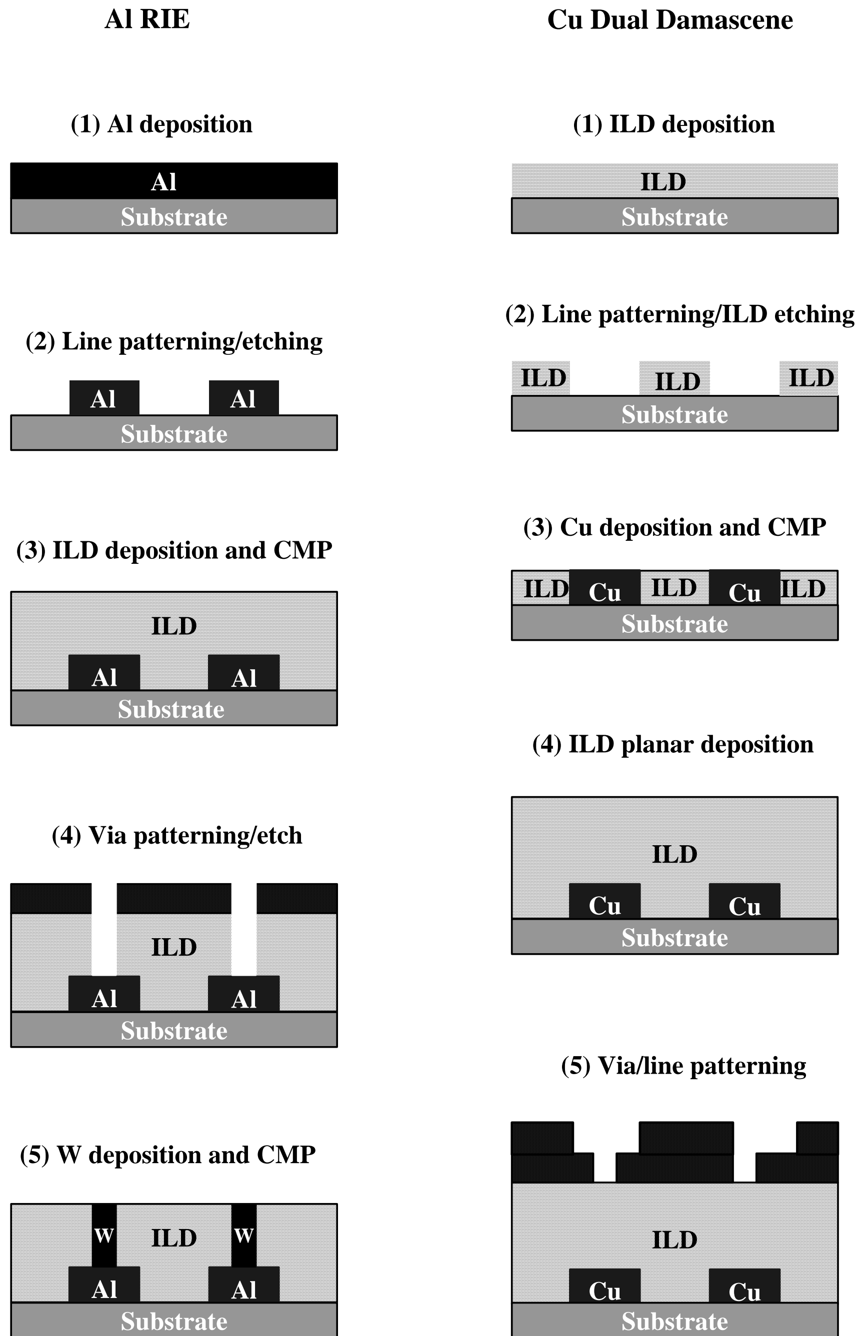


Figure 1.5 Process flow comparison for Al RIE vs. Cu Dual-Damascene

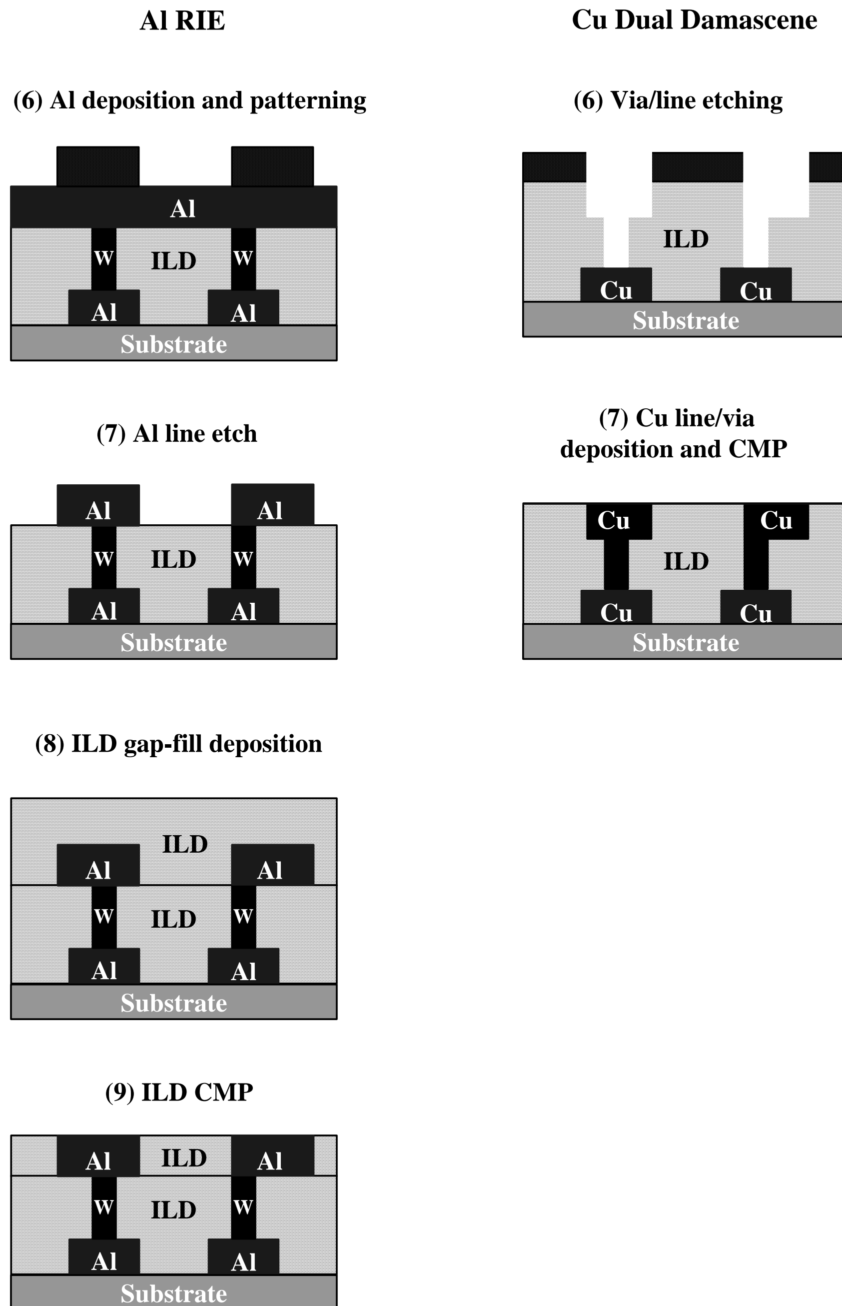


Figure 1.6 Process flow comparison for Al RIE vs. Cu Dual-Damascene. (Continuation of figure 1.5)

can be formed simultaneously in the dual-damascene process, which offers the added benefit of 50% reduction in the number of line-via interfaces.

The dual-damascenc process significantly reduces manufacturing cost. At the same time, the application of Cu/low κ integration improves performance of the devices. Such benefits drive the semiconductor industry inevitably to Cu interconnects.

1.2.3 Challenges in Cu/PLK Interconnect

Although the basic process flow for Cu/low κ interconnects has been well defined over the past few years, several technical challenges of an unforeseen nature have arisen when introducing the new materials into manufacturing.

1.2.3.1 Diffusion Barrier

The shift to the Cu interconnect brings about many benefits for advanced IC due to its low resistivity and its simple and low cost processing, however, the integration of Cu requires the presence of a diffusion barrier because of the high diffusivity of Cu into dielectrics and silicon, which seriously degrades the electronic properties of silicon devices [24-26]. Unfortunately, Cu does not form a stable native oxide layer to act as a diffusion barrier (as Al_2O_3 does in Al based interconnect) to prevent Cu from diffusion into the dielectrics and silicon. Therefore a diffusion barrier for Cu interconnect must be inserted. Also such a layer is needed to enhance the adhesion between Cu and the various low κ materials [27-29].

A barrier is important in improving eletromigration (EM) performance, one of the primary reliability failure mechanisms in IC devices. EM is a result of the momentum exchange between conducting electrons and metal atoms that causes a net

diffusion of metal atoms in the direction of electron flow. The resultant metal flux divergence causes the formation of voids at the cathode and/or extrusion at the anode. Voiding at the cathode can result in an electrical resistance increase or open circuit in the interconnect line, and metal extrusion at the anode can cause an electrical short to the neighboring lines [30-32].

EM basically is a diffusion phenomenon, so any efforts to reduce diffusion could improve the EM performance. It was well known that the fastest diffusion paths for Cu in the damascene interconnects structure occur at two interfaces: Cu/diffusion barrier and Cu/cap layer. A barrier providing good adhesion to Cu as well as low κ materials minimizes Cu diffusion along the Cu/barrier interface, and therefore improves the EM performance [32, 34]. Furthermore, the good barrier coverage in the trenches is a prerequisite for uniform Cu seed layer deposition and good Cu fill by electrochemical plating, and therefore reduces the probability for void formation during Cu deposition, which can significantly degrade the EM performance. In addition, the barrier also directly impacts EM by shunting current when void formations interrupt the current path. For this function, the barrier should be a good electrical conductor, such as Ta, and have good coverage and a reasonable thickness [33-35].

A desirable diffusion barrier is the material that provides excellent performance in preventing the diffusion and intermixing of Cu with the adjacent low κ material. Diffusion, regardless of the pathway, basically is “thermally activated”, and follows the Arrhenius relationship. It was found experimentally that diffusion rate is proportional to the melting temperature T of the host material, given by equation 1.2,

$$Rate = A\exp(-\frac{E_a}{kT}) \tag{1.2}$$

where E_a is the activation which is the amount of energy needed for the desired event to occur, T is the absolute temperature, k is Boltzmann's constant and A is a constant that depends on a variety of factors, including lattice structure and type of material. The relationship provides a reasonable guideline in the selection of appropriate materials for diffusion barrier. It indicates that materials with high melting temperature could act as better barriers. Accordingly, refractory metallic systems with characteristically high melting points and chemical inertness serve as viable candidates for diffusion barrier applications in Cu based metallization schemes. Currently, the most popular diffusion barriers are Ta as well as its compounds. From the material properties point of view, Ta is one of the most desirable diffusion barriers. It has a high melting point, 3020 °C, providing a high activation energy for both lattice and grain boundary diffusion. Also it does not form intermetallic compounds with Cu, thus providing a relatively stable interface between Cu and Ta. The reaction between Si and Ta is also known to require rather high temperatures 650 °C, which, in effect, provides a reasonably stable Si/Ta interface. [36].

A diffusion barrier with integrity, conformality and stability is critical to effectively block Cu diffusion into the low κ materials and subsequently into the Si devices. The quality of diffusion barrier is becoming a challenging issue. The aggressive miniaturization of IC devices makes the thickness of the diffusion barrier to be only a few nanometers, yet it has to be of near perfect quality in order to effectively

prevent Cu out-diffusion from Cu lines. Meanwhile, the introduction of pores into low κ materials makes it even difficult to deposit a continuous defect-free diffusion barrier layer. It was reported that the barrier deposited onto porous low κ films with thickness below 20nm are typically found to be permeable due to the presence of pores or pinholes [37-40].

The improvement of diffusion barrier quality is being extensively investigated [41-44], however, the struggle to achieve the needed high-quality barrier is slowed by cumbersome conventional characterization methods in this aggressively miniaturized situation.

The quality of diffusion barrier has been investigated primarily using electrical test methods, such as biased thermal stressing (BTS) and EM testing, and followed by a direct observation of the barrier microstructure using microscopy, especially transition electronic microscopy (TEM). However, these methods are time-consuming (generally taking a couple of months) and ineffective for detecting such small and localized defects. Typically, after a thermal test, a couple of samples are selected from test groups, and prepared (cross-section or top-down plane) for TEM characterization. Unless the defect density is very high, it is very difficult to find the tiny and localized defects on a massive area of diffusion barrier using TEM for the following reasons. First of all, TEM is only able to characterize one local area where it is possible that no any defects exist at all. Secondly, the defects are becoming very tiny as the extreme reduction of barrier thickness, making the characterization difficult. Unfortunately, one tiny defect may degrade the device performance and cause the device failure eventually as the thickness

of diffusion barrier keeps scaling down to a few nano-meters. Lately, time dependent dielectric breakdown (TDDB) test method, a conventional reliability test of the low κ structure, is being investigated to characterize the quality of diffusion barrier by monitoring the current resulted from Cu contamination into the low κ materials [45]. However, the method developed for interconnects integrated with DLK are also time-consuming and ineffetive. It is not designed to exclusively examine the barrier quality, increasing the potential for false diagnosis. For example, it is possible that defects are produced during a TDDB test since it is an accelerated test, conducted at high temperature and voltage. It is, therefore, imperative to develop a method for evaluating the barrier integrity exclusively.

1.2.3.2 Low κ Materials

Generally, there are two approaches to reduce κ of a material: incorporate atoms and bonds that have a lower polarizability and lower the density of atoms and bonds in the materials. The polarization components usually considered are the electronic and nuclear responses of the material. The nuclear dielectric response results from polarization of both permanent and transition dipoles in the material, and the response is often dominated by polar substituents, such as hydroxyl and carbonyl groups. When designing low κ materials, it is desirable to use material with C-C and C-F bonds, which have the lowest electronic polarizability, and avoid using highly polar substituents that attract and bind water, which increase κ significantly due to the large permanent dipole moment of water. The dielectric constant of any material can also be reduced by decreasing the density. As a result, low κ can be obtained by using lighter atoms, such

as C and H, and incorporating more free space, such as pores, into the structure. Organic polymers are often used in low κ materials because of their low material density and low individual bond polarizabilities [46].

A particularly difficult challenge for low κ material development is to obtain the combination of low dielectric constant and good thermal and mechanical stability. Generally, the types of chemical structures that impart structural stability are those having strong individual bond that often have strong polarizability and high density of such bonds. It is those two factors (the strong bond and the high density) that offer a high dielectric constant.

To further reduce κ value for advance interconnects, low κ materials with pore structure (PLK) are being integrated with Cu interconnects. However, the high degree of porosity in the PLK materials creates a number of integration reliability challenges. Generally, porous films are considered to further deteriorate reliability compared to their dense counterpart. Although there has been significant progress in the last years regarding the integration of PLK materials, more work is still needed [46-47].

The introduction of pores achieves the goal of lowering κ at the cost of degradation in mechanical strength, thermal conductivity, resistance to chemical attack [47-50].

First of all the mechanical properties degrade significantly with the introduction of pores in solid materials, and the weak mechanical properties often lead to poor adhesion of the PLK materials to other layers, poor CMP compatibility and difficulty in package assembly. In addition, the thermal conductivity drops rapidly as the pores are

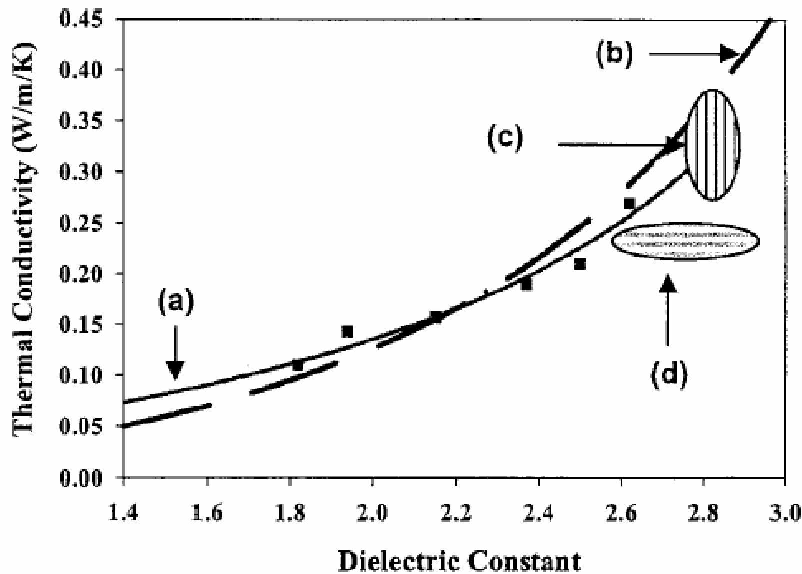


Figure 1.7 Correlation of thermal conductivity and dielectric constant (dark square) represents the experimental data for the porous MSQ. Curve (a) is for the porous MSQ and (b) for the porous silica. Oval (c) includes various dense ISG materials, and (d) includes various dense polymeric low κ [54].

incorporated in the matrix material, as seen in figure 1.6 [51]. The thermal conductivity drops to ~0.05W/m/K for porous MSQ/silica from ~0.3 W/m/K for dense polymeric materials. The poor thermal conductivity of porous low κ severely reduces the thermal conduction in interconnect structures, and therefore aggravates joule heating and increases EM reliability concern. As seen in figure 1.7, interconnect temperatures increase from ~5K to 30~80K as PLK replaces SiO_2 due to its poor thermal conductivity [52]. Furthermore, pores in low κ materials can contain contaminants from processing gasses and liquids or ambient, any of which may have a detrimental effect on the dielectric electrical properties or instigate unwanted chemical changes [53-54]. It was reported that the pores can be highly interconnected if porosity is greater than

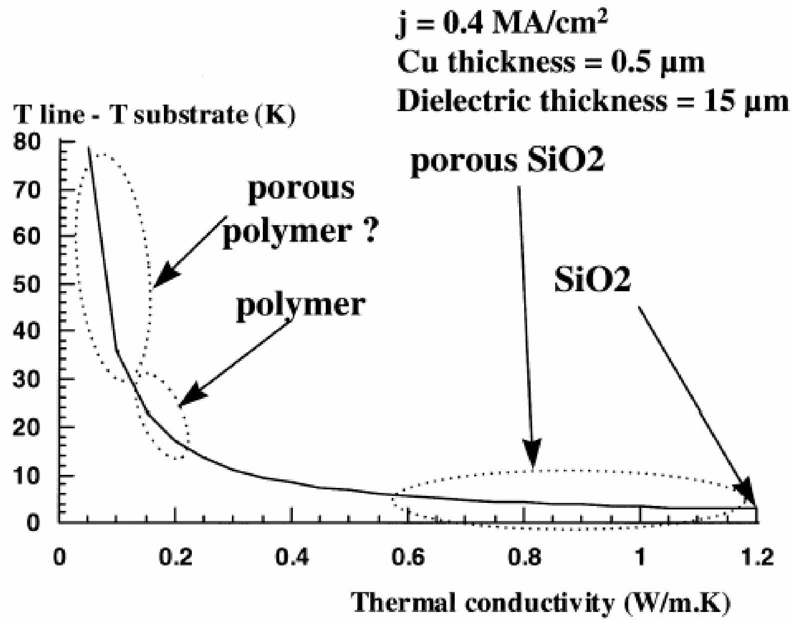


Figure 1.8 Interconnect line temperature increase (T_{line}-$T_{substrate}$) as a function of the dielectric thermal conductivity [52]

~25% [55-57], which may open new failure mechanism in Cu/PLK materials that not found in Cu/DLK structure [58-59].

The reliability of Cu interconnects becomes even more complicated and demanding with the introduction of pores into low κ structure.

The weak mechanical strength of PLK materials aggravates the EM performance [32, 36].

$$J = \frac{DC}{kT}\left(z^{*}e\rho j - \Omega \frac{d\sigma}{dx} \right) \tag{1.3}$$

As seen in equation 1.3, EM performance is the result of two competing factors [60]. The first term, z*eρj, referred to as electron wind, is the driving force for EM, where z* is the apparent effective charge number, e is the absolute value of the electronic charge,

ρ is the metallic resistivity, and j is the current density. The second term, $\Omega d\sigma/dx$, referred to as the metal accumulation back-stress gradient, is the force to resisting EM, where Ω is the effective atomic volume. The equation highlights the reliability challenges with the scaling of Cu interconnect integrated with low κ materials. On the one hand, the demand for higher current density significantly increases the driving force for EM, and therefore accelerated the EM failure. On the other hand, the PLK materials provide less confinement, or less back-flow stress due to their lower elastic modulus, and further shorten EM failure times. In addition, the pore structure in the PLK materials can aggravate joule heating problem due to poor thermal conductivity and further degrades EM performance [61-63].

The introduction of pores in low κ materials creates a serious TDDB reliability concern. In the past with SiO_2, TDDB has not been a reliability concern. SiO_2 has a high breakdown strength, ~~10MV/cm, and the operating fields in a typical damascene structure are below 0.5MV/cm. For this reason, TDDB is unlikely to be a reliability concern even if the thickness is very thin. Also the robustness of SiO_2 is partially due to good oxide confinement to the metals and good adhesion between the cap and copper, making it difficult for copper to diffuse out from the line. On the other hand, low κ materials including DLK and PLK (PLK is the worst), generally have less breakdown strength, and less confinement of Cu/barrier, which can result in higher electronic leakage from Cu diffusion and premature TDDB [64, 65].

Extensive studies are being conducted to characterize pore structure, such as positronium annihilation lifetime spectroscopy (PALS), a combination of specular x-ray

reflectivity (SXR), small angle x-ray and neutron (SAXN) scattering and measurement of solvent diffusivity [66-70]. Low energy PALS is able to determine the average pore size and pore structure. In porous films, the formation of positronium (Ps) occurs preferentially in the voids of the film, and the Ps annihilation life time is shortened from the vacuum lifetime (~142ns) owing to collisions with the pore walls. This effect provides a means of determining the average pore size from the Ps lifetime in the porous film. PALS is also able to detect the onset of an interconnected pore network (pore interconnectivity) because the Ps has a single lifetime if all the pores are connected. Moreover, if the pores are isolated, the Ps has many lifetime components, each corresponding to a different pore size. Therefore, in a closed pore structure, PALS has the potential to provide pore size distribution. SXR is able to measure the porosity by comparing the average film density to an assumed density of the non-porous material. SANS is not a direct technique for pores structure characterization. It measures the density of the connecting material, and therefore mesoporosity can be calculated from the average film density (measured by SXR) relative to the pore wall density (measured by SANS). Measurement of solvent diffusivity is a simple method developed recently for predicting the pore interconnectivity by measuring effective diffusivity of solvent as a function of porosity.

Regardless of the high cost of the equipment and requirement of complex model to extract desired data (except measurement of solvent diffusivity), each technique has its own limitation. Even PALS, the most powerful technique for pore structure characterization, can not characterize the pore size distribution if the low κ material has

an open pore structure. However, as modern devices are continuously shrinking down, ultra low κ materials with higher porosity are required to further lower RC delay. When the porosity is greater than 25~30%, the pore interconnection occurs [56,57].

Most important, all those techniques are only effective on blanket films (unpatterned wafer). However, the pore morphology of PLK materials in as-processed interconnect is found not to be thermally stable but alter its characteristics during thermal annealing [65, 71], and the current methods mentioned above are not able to trace its thermal stability. Therefore, it is essential to have a method to characterize the pore morphology with multiple functions for patterned wafer instead of blanket film in order to understand the impact of the pore structure on the product reliability and thereby optimize processing conditions and the resulting properties.

1.3 Objectives and Significance of This Thesis

This study has three major objectives: (1) to investigate the thermal failure mechanism for Cu/PLK interconnect structures, which raises the issue of effectiveness of conventional characterization metrologies, (2) to develop a new metrology for barrier quality detection in fine scale barrier thickness, (3) to develop a new metrology for characterization of pore structure in low κ materials and using the method to investigate the stability of the pore structure in PLK.

The metrology developed in this study is able to characterize both the defects in diffusion barrier and the pore structure in low κ materials of Cu/barrier/PLK integration. This specific technique is simple, fast and effective with low cost. For barrier defects detection, the conventional methods require TEM observation after lengthy electrical

tests. This is time-consuming and of questionable effectiveness due to the localized and tiny defects within massive area of barrier layers, as discussed in 1.2.3.1. On the other hand, the developed method is a room temperature test, and does not require long time baking and intensive microscopy examination to find the tiny defects in massive area of barrier. It is very sensitive due to the intrinsic characterization for chemical reaction. Regarding the characterization of pore structure, unlike the other available methods that are only effective on the blanket film, the developed method is able to characterize and trace the stability of the pore structure in low κ materials on as-processed wafer.

1.4 Overview of Chapters

Chapter 2 is devoted to the study on thermal stability of diffusion barrier in Cu/PLK interconnects. The investigation is conducted on Cu interconnects with various barrier arrangements at elevated temperature with various ambient, and then the failure mechanisms and the leading factors are evaluated by a combination of TEM, SEM (Scanning Electron Microscopy), and electrical resistance signal in Cu/PLK structure.

Chapter 3 describes the developed characterization method (voltammetry-based) for both barrier defect detection and pore structure evaluation in low κ materials, including the fundamental concepts of voltammetry and the principle of developed metrology.

Chapter 4 investigates the quality of diffusion barrier in Cu/low κ interconnects using the developed “voltammetry” technique after the fundamental study of the method, in which idealized samples are prepared to simulate various condition of diffusion barriers.

Chapter 5 develops the characterization technique and the analytic model for evaluation of the pore structure in low κ materials. Its thermal stability is investigated using the developed method, too.

Finally, conclusions and the future research are presented in Chapter 6.

CHAPTER 2

STUDY ON THERMAL STABILITY OF Cu/PLK STRUCTURE

In this chapter, a series of thermal stability investigations are conducted on Cu/PLK interconnects with various types of barrier arrangements at elevated temperature with various ambient to understand thermal failure mechanism as well as the impacts of barrier and ambient on thermal failure process.

Cu interconnect stability is determined by resistance of Cu lines with intermittent application of low current (0.1MA/cm^2, far lower than a typical current density for EM test). It is only applied on samples when taking data. The purpose for this is to minimize the influence of current on the failure process of interconnects.

The thermal and kinetic failure mechanisms and their factors are assessed by a combination of TEM, SEM, and electrical resistance signal. It is found that Cu/PLK interconnect can fail by Cu out-diffusion into the pore structure simply by thermal baking, and the failure seems to be driven by the mechanism that is not seen in Cu/DLK structure.

2.1 Samples and Experimental

2.1.1 Samples

Thermal stability tests are performed on 0.25μm wide, single-level and two-level Cu interconnect structures processed by SEMATECH. The intra- and inter-leve

dielectric is a porous MSQ-based material with κ value of ~2.2 and estimated porosity of ~45%. An optical image of the test pattern and the cross-section schematic of one and two level Cu/barrier/PLK structure are present in figure 2.1

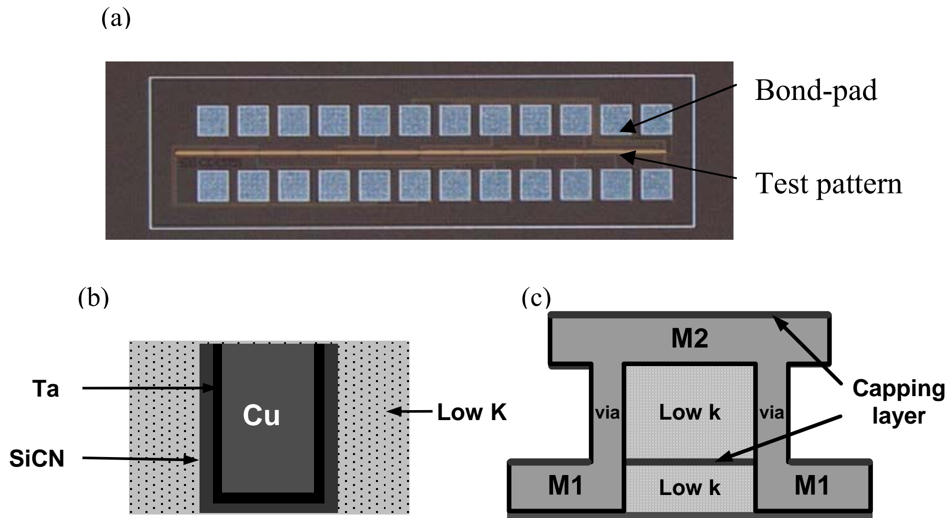


Figure 2.1 (a) An optical image of test pattern; a cross section schematic of (b) one level (c) two level Cu/barrier/PLK structure

The single level samples are 400μm long lines on M2, with no vias and M1 in the resistance measurement circuit. The two-level samples are of multiple M2 segments, 0.25μm wide, 150μm long connected by vias through M1. Between each layer of metal metallization, a 100nm SiN layer (a capping layer) is deposited by plasma enhanced chemical vapor deposited (PECVD). Each layer Cu/PLK interconnect structure consists of 400nm of low-κ material between 250nm Cu with various barrier arrangements, as seen in figure 2.1 (c). Two types of barier arrangement are used in this study. In the first type, a PECVD SiCN layer with a thickness range of 30-50nm SiCN spacer is deposited on lowκ material first and then a Ta layer with a thickness range of 0.5-25 nm is

sequentially deposited. In the second type, a 25nm Ta layer is deposited on low κ material directly without any SiCN spacer in between. After completion of M2 metallization, a dielectric passivation stack of 100nm SiN/200nm SiO_2 is deposited, followed by TaN and Al protection layers over the bond pad openings. Samples are cleaved to get the test pattern, and then chip with test pattern is mounted in a chip carrier and gold wires are bonded to connect the test pattern circuit to a chip carrier [72].

2.1.2 Experimental

The thermal stability is investigated on the EM lifetime testing set-up built up at UT-Arlington. The detailed description of the equipment, including the particular circuit design and the working principle, can be obtained in the reference [73], but a brief description is given here: The set-up consists of a convection oven, high temperature circuit boards, a special circuit design to allow multiple samples to be tested with one constant current source, and a computer controlled data acquisition system, as shown in figure 2.2. The set-up can conduct simultaneously up to 100 samples at elevated temperature and the resistance is recorded by applying a constant current. The increase in resistance up to 100% is used as a failure criterion instead of 10% increase in industry. For the thermal stability test in a controlled ambient environment, a sealed stainless steel box connected to N_2 or Ar gas is put inside the oven, and serving as an environmental chamber.

In the thermal stability investigation, Cu/PLK interconnects with various barrier arrangements are baked at elevated temperature 150-325°C in air/Ar/N_2 ambient, and the thermal stability is monitored by the resistance of Cu lines with occasional

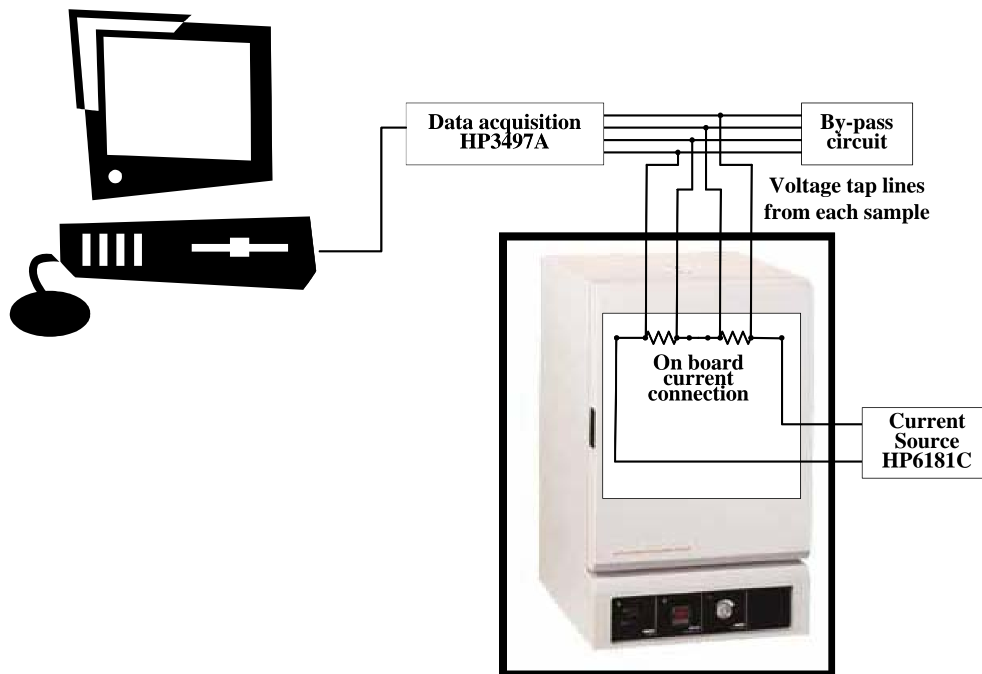


Figure 2.2 A schematic representative of the experimental apparatus

application of low-level current. The microstructure investigation has been performed with a JEOL 845 SEM and a 1200EXX JEOL TEM to reveal the failure mechanism of Cu/PLK interconnects. TEM samples, prepared as the normal procedure, are diced from wafer and attached to 3mm Cu grid; thinned from Si substrate; followed by dimpling and argon ion milling to the interested area thin enough for electron transimision.

2.2 Results

2.2.1 Thermal Instability of Cu Interconnect

2.2.1.1 Tested Under Air Ambient

Figure 2.3 and 2.4 present the representative electrical resistance of Cu/PLK with various barrier arrangements baked at different temperatures. The results show that

Cu interconnects fail by two-step process: (1) incubation period where the resistance is pretty stable (2) steady-state increase period of resistance where the resistance gradually increases with time. The failure time of Cu/PLK interconnect is found to be dependent on the barrier arrangement and the test temperature.

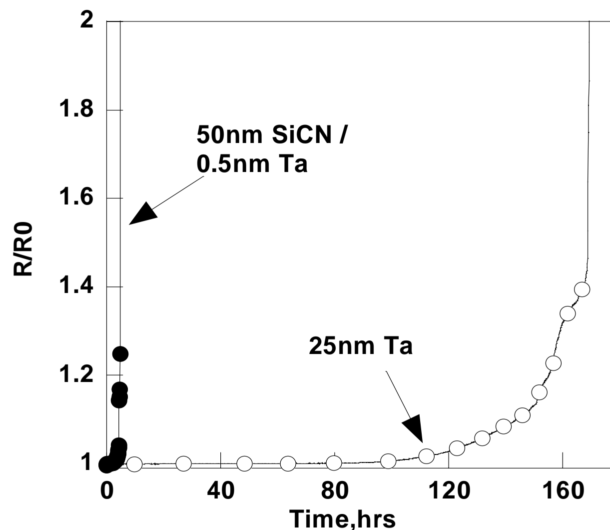


Figure 2.3 A plot showing resistance (ratio) of a 0.25um single level Cu interconnect with different barrier arrangement baked at 275°C with low level intermittent current, 0.1 mA/cm^2 in air atmosphere.

As seen in figure 2.3,which presents the typical electrical resistance data resulted from the single level Cu interconnect with two barrier arrangements, 25nm Ta and 50nm SICN/0.5nm Ta, baked at 275°C in air, the failure process is significantly affected by the barrier arrangement. The failure time can be retarded from a couple of hours for Cu integrated with 50nm SiCN/0.5nm Ta to ~140 hours for Cu integrated with 25 nm Ta. Also a clear incubation period (~100 hours) in the sample with thick Ta (25nm) can be seen while almost no incubation period exists in the sample with thin Ta

barrier (50nm SiCN/0.5nm Ta) even through a thick SiCN layer (50nm) is present. The results suggest that the failure time, as well as the incubation period, is affected significantly by the thickness of the Ta layer and a SiCN layer is not as a good barrier for Cu interconnects as a Ta is.

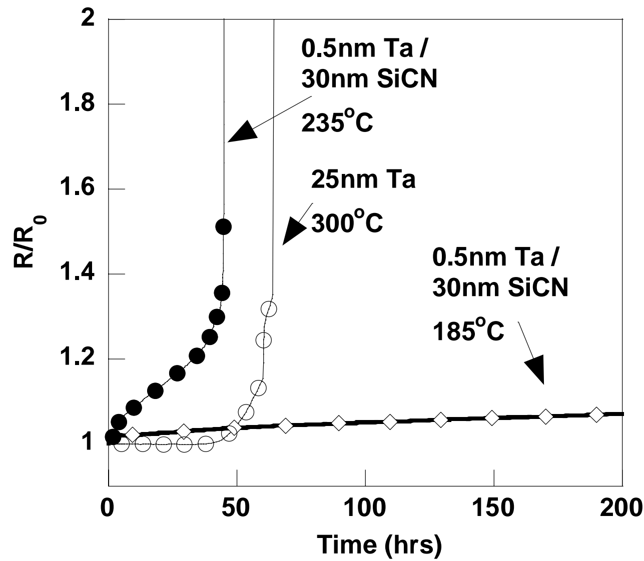


Figure 2.4 A plot showing resistance (ratio) of a single level with different barrier arrangement and temperature with low level intermittent current, 0.1mA/cm^2 in air atmosphere.

Figure 2.4 presents representative electrical resistance data taken from two groups of Cu/PLK interconnects. The two groups of samples have different barrier arrangements, 25nm Ta and 30nm SiCN/0.5nm Ta and were baked at different temperature in air. As is seen, there is a clear incubation period in the sample with thick Ta (25nm) even at 300°C, however, even at a very low temperature, 185°C , the resistance of the samples with thinner Ta(0.5nm) begins to slowly increase immediately with no discernable incubation period. This result also indicates that the incubation

period is affected significantly by the Ta thickness and the thick SiCN layer seems not to provide the same benefit. The absence of incubation period in thin Ta may indicate that defects are present at as-received condition. On the other hand, the second stage seems less dependent on Ta barrier thickness as seen in figure 2.3 and 2.4.

2.2.1.2 Tested Under Inert Ambient

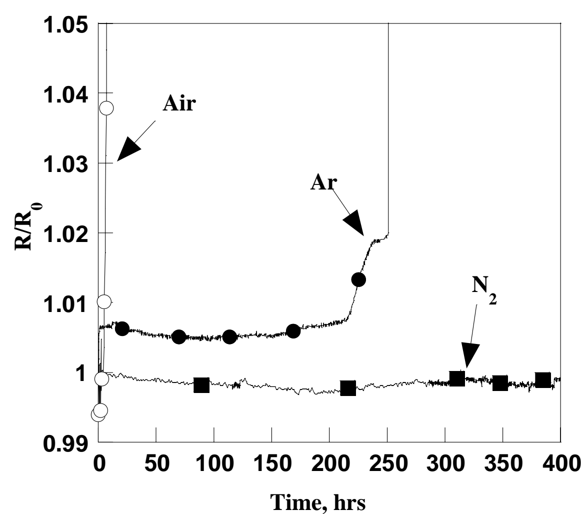


Figure 2.5 A plot showing resistance (ratio) of a single level, 0.25µm Cu/ 25nm Ta barrier as a function of baking time at 325°C. Note that N_2/Ar ambient substantially delays the failure, but cannot prevent the process.

In an attempt to evaluate the impacts of test ambient on thermal stability of interconnects, single level Cu interconnect with different barriers have been investigated in Ar and N_2 ambient. Figure 2.5 shows representative results of resistance in air, Ar and N_2 as a function of time at 325°C for 0.25µm wide single level Cu with 25nm Ta barrier. In air, the interconnects fail very fast, about 10 hours, whereas the failure is substantially retarded in Ar ambient and retarded further in N_2 ambient, but the process of Cu leakage cannot be completely prevented. Although complete failure did not occur

in either Ar or N_2 ambient in the test period for this group of samples, the increase in resistance indicates that the failure process has begun and will occur eventually. This may be because inert ambient is helpful to protect Cu from out-diffusion, and will be discussed later in section 2.3.2

2.2.2 Microscopy Characterization

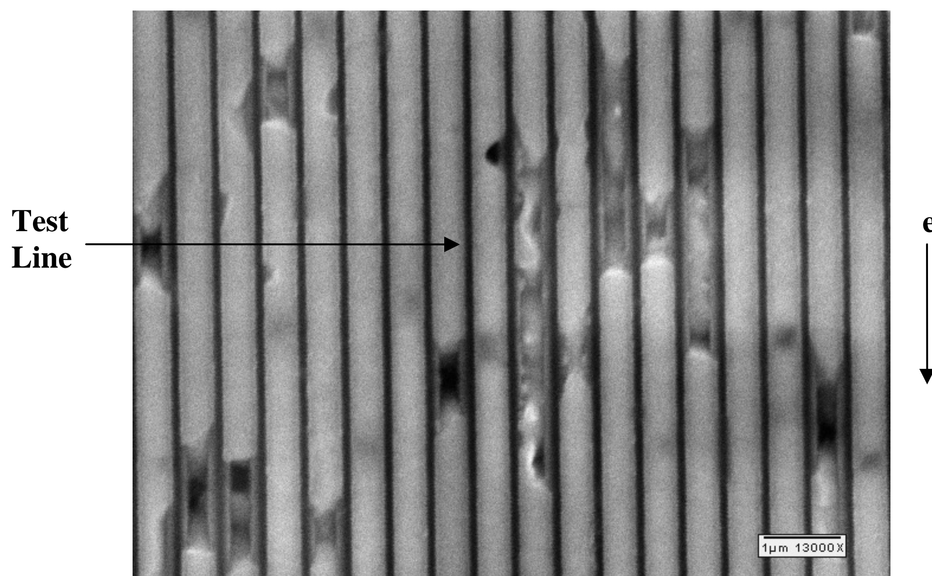


Figure 2.6 A typical SEM top-down image taken from 0.25µm wide Cu lines with a 30SiCN/2Ta barrier after 135 hours of baking at 225°C. Note only one of Cu lines is applied current in this test pattern

When the samples baked in air are observed under SEM, it is noticed that extensive voids are consistently seen along the entire length of not only the tested lines where low level current is applied occasionally but also the untested lines where no current is applied at all. Such behavior is seen in all sets of sample in the thermal study. Figure 2.6 presents a typical SEM top-down image of 0.25µm wide Cu lines with a 30SiCN/2Ta barrier after 135 hours of baking at 225°C. It is voiding that is believed to

be the reason for the Cu lines resistance increase and cause of the complete failure (open circuit). This result suggests that a new failure mechanism exists, rather than EM damage. Figure 2.7 presents a typical SEM cross-section image of vias under bond pad in two- level Cu interconnect with 25nm Ta after 45 hours of baking at 225°C. It is noted that Cu diffuses out from vias forming Cu bands (under bond pad) into the PLK dielectric layer.

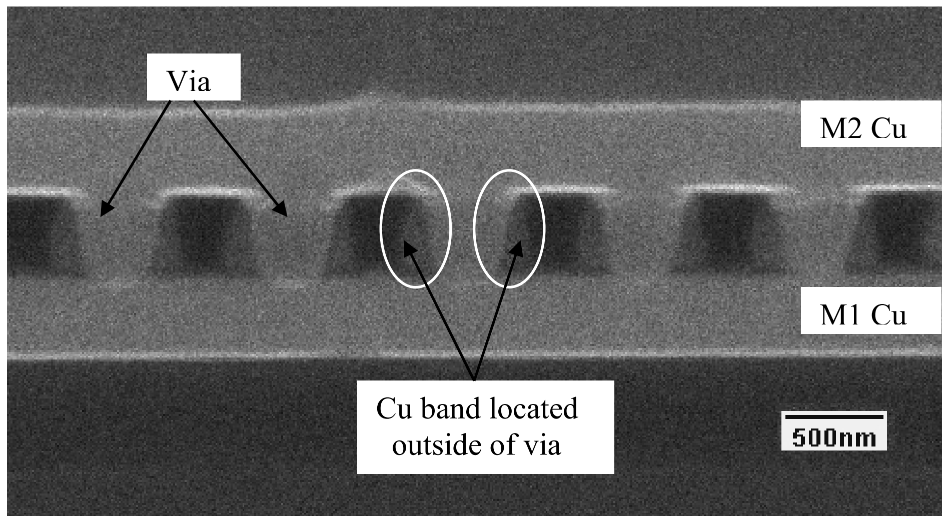
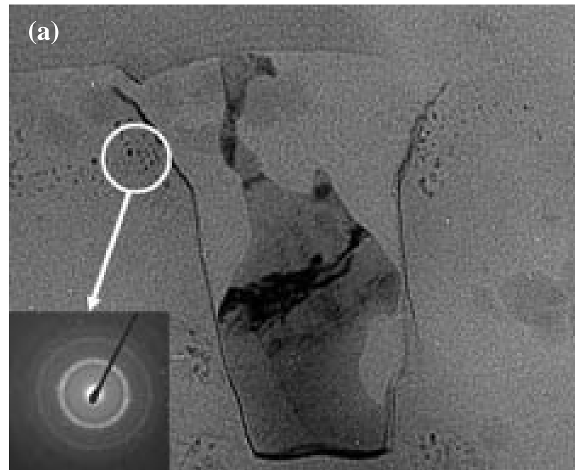


Figure 2.7 A typical SEM cross-section image of vias under bond pad in two-level Cu interconnect with 25nm Ta after 45 hours of baking at 225°C. Note that Cu bands form outside of each via (both sides)

TEM analysis also reveals that Cu diffuses out of lines into the PLK layer leaving voids in the lines. Cu bands or clusters of particles are clearly observed dispersed within the PLK forming the stable oxide there. Figures 2.8-a,b shows such feature found in a cross-section TEM micrograph of an M2 level Cu interconnect with



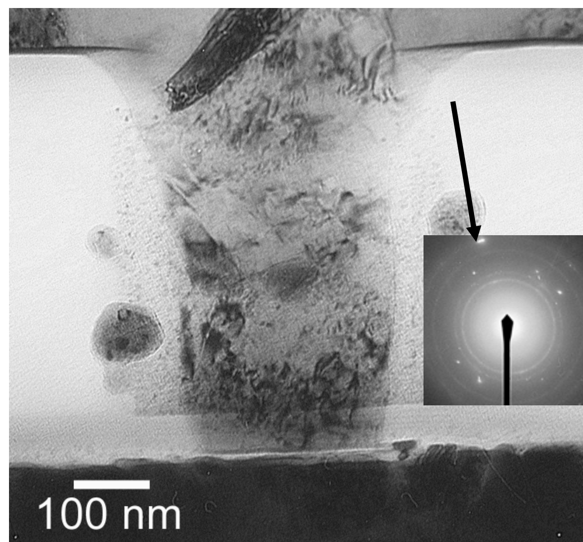
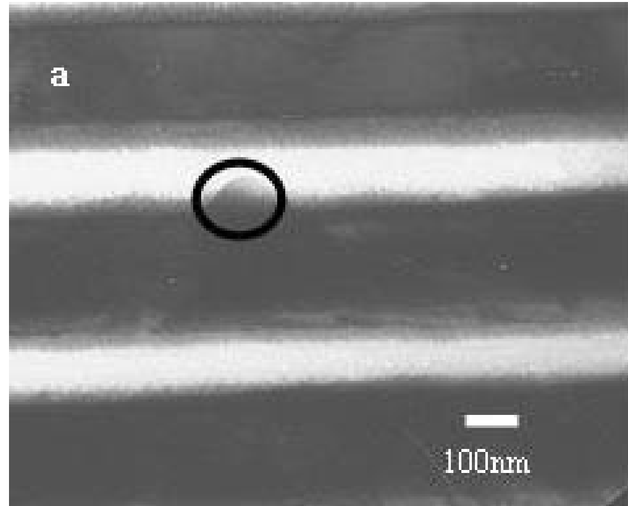


Figure 2.8 Cross-section TEM images, taken after baking (a) at 275°C in air showing the formation of dark spots contrast near to a 0.25µm Cu trench with 50 nm SiCN/0.5nm Ta arrangement. (b) at 225°C in air showing band and spots of dark contrast near to 0.25µm Cu trench with 30 nm SiCN/2nm Ta arrangement. The diffraction ring pattern analysis taken from the circled areas indicates that Cu exists outside the trench as stable oxide phases, either CuO after 225°C baking or Cu_2O after 275°C.

(a) 50nm SiCN/0.5nm Ta baked at 275°C for 274 hours (b) 30nm SiCN/2nm Ta baked at 225°C for 20 hours in air [74]. The analysis of the selected area diffraction pattern of the circled area indicates that Cu exists as an equilibrium Cu oxide phase, and the type of oxide formed is found to vary with temperature: CuO formed after a 275°C bake and Cu_2O formed after a 225°C bake. The difference in phase with temperature disagrees with bulk Cu oxidation behavior, in which CuO is favored at low temperature, but agrees with recent reports on Cu thin film oxidation [75-76]. The formation of stable Cu oxide suggests that contaminants, including oxidants, are presented in PLK and may act as a driving force for pulling Cu out of the trenches.

In a thermal investigation to eliminate the influence of air ambient that may infiltrate and supply oxidants to the PLK, single level Cu interconnects samples are baked at elevated temperature in an inert ambient. Figure 2.9 displays top-down TEM micrographs of single level Cu interconnects with 25 nm Ta barrier baked at 325°C in N_2 and Ar ambient. Cu is observed spiking through the Ta barrier into the PLK in Ar, as seen in figure 2.9-a. Numerous such extrusions are observed in the samples tested in Ar ambient, indicating that the degradation of Cu lines still occurs by out-diffusion into the PLK even when the impact of oxidants from the test ambient is minimized. However, Cu appears to remain at the interface of barrier/PLK instead of dispersing into the PLK. In this case, the stress gradient across the Cu interconnect structure may provide a potential for Cu out diffusion through the barrier, but it appears not to be strong enough for pulling Cu into the PLK. An interesting fact is that no noticeable extrusion is



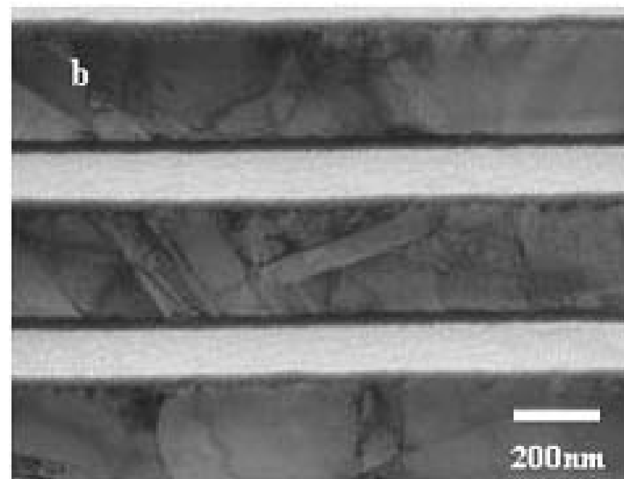


Figure 2.9 A top-down view TEM micrograph after baking at 325°C in Ar/ N_2 ambient showing no noticeable Cu out diffusion observed in porous PLK next to a 0.25μm Cu trench with 25nm Ta arrangement. (a) An extrusion was observed through Ta barrier of the sample tested in Ar ambient (b) No noticeable extrusion was observed of the samples tested in N_2 ambient

observed in the samples tested in N_2 ambient as shown in figure 2.9-b, although the Cu lines subjected the same conditions

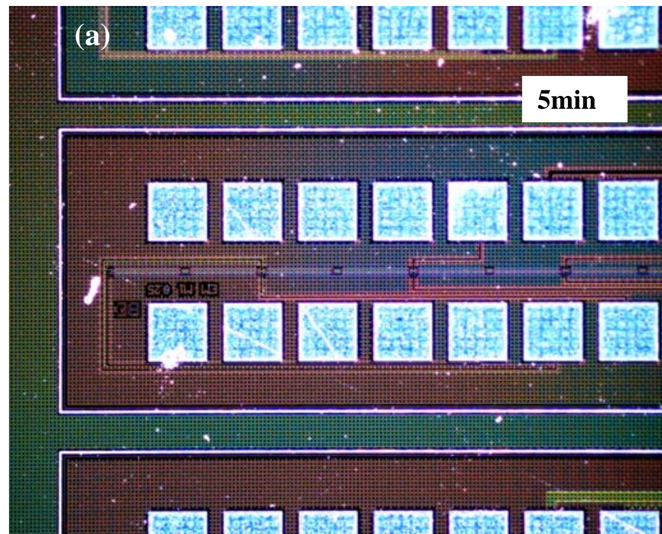
2.3 Discussion: Mechanism of Thermal Instability

A series of electrical and microstructural examinations of Cu interconnects integrated with PLK indicates that Cu interconnects suffered from thermal activated instability regardless of the barrier arrangements and test ambients. After baking in air, Cu diffuses out of the lines forming a stable oxide in the PLK, and leaves extensive voids behind causing the increase of line resistance. The formation of Cu oxides in PLK indicates that oxidants present in PLK may provide a driving potential for Cu out-diffusion. Furthermore, the formation of Cu extrusions in the samples baked at Ar ambient at the interface of barrier/PLK suggests that there may exist another driving force for Cu out-diffusion.

2.3.1 Oxidation Mechanism

2.3.1.1 Source of Oxidants

The TEM images for samples baked in air reveal that oxidants appear to be present in the test structure. The possible sources of oxidants are considered to be from the processing and the test ambient. An investigation of the possibility for ambient oxidants to infiltrate into low κ structure is conducted on the sample groups used for the thermal stability study. Samples are cleaved to get patterns with an intact scribe seal, and then acetone is introduced along the edges of the samples. It is found that moisture is able to infiltrate into the test structure quickly, a few minutes, as is seen in figures



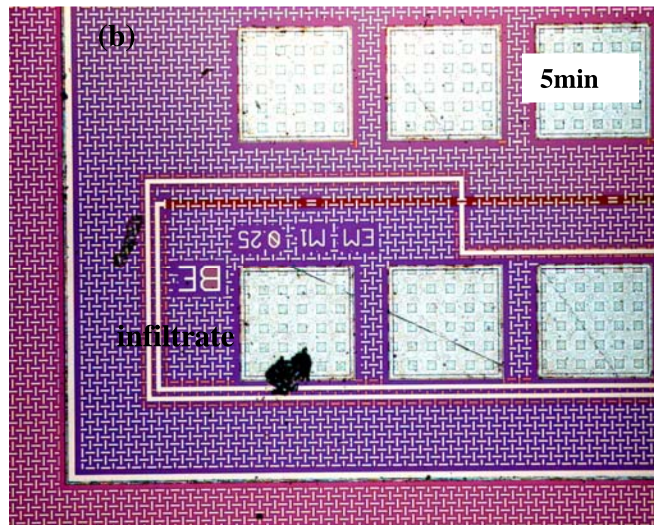


Figure 2.10 Optical images show the micrograph of acetone infiltration into Cu/PLK structure from the edge after 5 min even with the presence of the scribe seal. Note the dark contrast indicates the infiltration of acetone (a) dark field (b) bright field

2.10-a,b. The dark contrast is created in the test structure after 5 min infiltration of acetone from the edge of the samples. This result indicates that moisture is able to penetrate the scribe seal into the PLK within the test structure, and therefore we believe the ambient gas (air) is able to infiltrate into the PLK through the highly interconnected porous network during thermal test and provides sufficient potential for drawing out of Cu lines.

2.3.1.2 Oxidation Mechanism

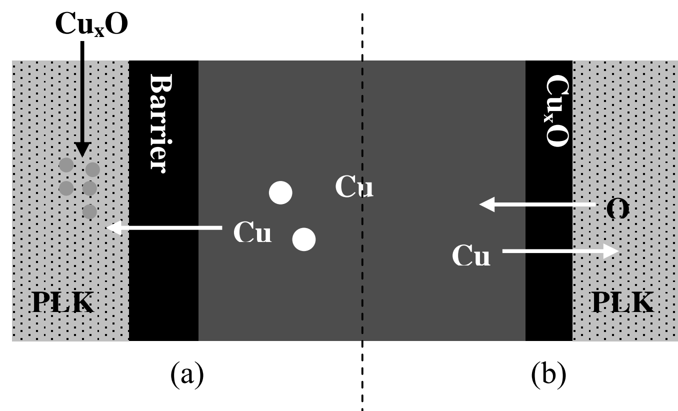


Figure 2.11 Failure mechanism driven by oxidation potential (a) Cu interconnect fails by Cu out-diffusion into PLK forming Cu_xO there and leaving voids in the lines (b) Normal oxidation occurs by interdiffusion between Cu and O through Cu_xO without voiding formation.

The oxidation mechanism is different from the normal procedure of bulk oxidation, which typically occurs by the inter-diffusion between Cu and oxygen through the initial Cu oxide thin film at the Cu/low κ interface and no voids are left behind [75-76], as shown in figure 2.11. In this study, the formation of Cu oxide far away from Cu trenches and the presence of voids in the trenches indicate a Cu out-diffusion

mechanism. The abundant oxidants infiltrated in the PLK provide a strong oxidation potential. By consuming free Cu continuously and thereby reducing Cu concentration at the interface, oxidation is a steady driving force pulling Cu continuously through the barrier, leaving extensive voids in the lines. It is these voids that cause the increasing of the resistance and ultimately line failure.

It is noted in TEM images that the stable oxide particles are sometimes separated from the Cu lines. It is possible that Cu may not be exposed to oxidants until it diffuses some distance away from the line edge. In this case, we postulate that oxidants are not present at the Ta barrier/PLK interface because the structure at the edges of PLK is much denser than the structure far away from the edges of PLK, which may result from the collapse of the pores due to compressive stress created by the mismatch of CTE of between Ta (6.5 ppm/°C) and PLK (~20 ppm/°C for MSQ-based PLK with ~50% porosity) during test or processing [77]. The compressive stress is likely to concentrate at the interface of Ta/PLK (the edges of PLK structure) instead of the center of PLK (bulk area) because Ta barrier is much stiffer than PLK. Therefore, oxidants prefer to stay at the more open structure (the bulk area) rather than the interface of Ta/PLK.

2.3.1.3 Kinetic Mechanism for Cu Out-Diffusion

As was mentioned in 2.1.1, electrical examination in air ambient indicates that Cu interconnects fail by two steps: incubation and steady-state resistance increasing period. The incubation period is found to be greatly dependent on Ta thickness. The microscopy observation indicates that the resistance increase of a Cu interconnect occurs as Cu diffuses out of the line by the oxidation potential, leaving voids behind.

The diffusion rate of Cu, corresponding to the slope of second stage in figures 2.3 and 2.4, can be controlled either by a diffusion or oxidation reaction mechanism.

In order to determine the dominant mechanism, a simple kinetic model is employed to correlate the resistance change and diffusion rate during the second stage. The model assumes Cu diffusion through the sidewall, but not through the top and bottom, consistent with SEM and TEM observations. Thus the resistance (R) of interconnects is a function of resistivity (ρ), length and cross sectional area of the conductor,

$$R = \rho \frac{L}{(W \times H)} \qquad 2.1$$

where L, W, and H are the length, width and height of the Cu lines respectively. H and L have no change during the test and the resistivity (ρ), as an intrinsic property, is also assumed to be a constant at test temperature. Consequently, the resistance is proportional to reciprocal of W,

$$R \propto f(\frac{1}{W}) \qquad 2.2$$

W is a function of the square root of the product of diffusivity (D) of Cu into the PLK and baking time (t),

$$W \propto f(\sqrt{D \times t}) \qquad 2.3$$

When D is assumed constant, the reciprocal resistance is proportional to the square root of baking time:

$$\frac{1}{R} \propto f(\sqrt{t}) \qquad 2.4$$

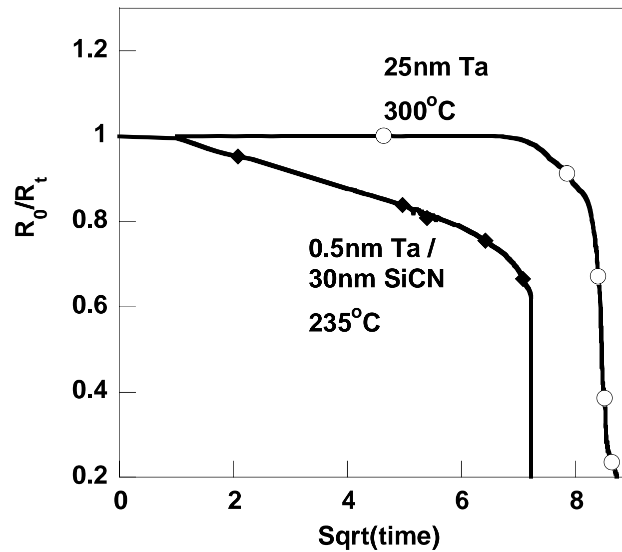


Figure 2.12 A plot displays the reciprocal resistance ratio of 0.25μm Cu lines with different barrier arrangement and temperature as a function of the root of baking time

When the reciprocal resistance ratio, R_0/R_t, of the data in figure 2.4 is plotted as a function of $t^{1/2}$, a linear relationship is found, as shown in figure 2.12, consistent with a diffusion-controlled instead of oxidation-controlled reaction where the rate of oxidation at equilibrium condition is known to be linear function of t not $t^{1/2}$[78]. Figure 2.13 summarizes the slope from three sample groups with different barrier arrangements, 25nm Ta, 2nmTa/30nm SiCN and 0.5nm Ta/30nm SiCN, tested at various temperatures, 185~300°C. The slopes are seen to fall into a single Ahrrenius fit with a slope of 0.6 and the diffusion activation energy is found to be 1.2eV. The result suggests that the diffusion rate of Cu in second stage is independent of Ta thickness, and also may

indicate that the same mechanism governs this stage regardless of the Ta thickness and the incubation period.

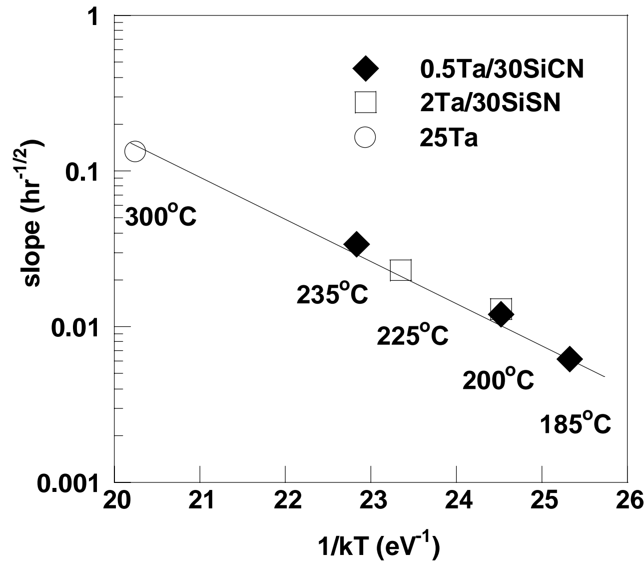


Figure 2.13 A plot showing the slope of R_0/R_t vs. $t^{1/2}$ for various temperature and barrier as a function of 1/KT.

2.3.2 Stress Mechanism

The degradation of Cu lines tested in inert environments suggest that there may exist another potential acting as a driving force for Cu interconnect failure during baking. Although an inert test ambient provides a protection for test sample against the infiltration of ambient oxidants, Cu still diffuses through the barrier and resides at the interface of barrier/PLK. It is known that Cu is subjected to a large compressive stress during thermal baking as a result of the mismatch of CTE between Ta (6.5 ppm/°C) and Cu (11.7 ppm/°C) [77]. In the absence of abundant oxidants, this compressive stress becomes a main driving force for Cu out-diffusion. Pores in PLK provide empty space, and therefore the Cu can be drawn from the high compressive stress area inside the line

through the barrier to the pores without creating stress in the PLK or encountering back-stress from the PLK. However, the stress potential seems not sufficient to draw Cu into the PLK leaving voids behind as oxidation potential does in air ambient. This may be because once stress is locally relaxed, there is no driving force for pulling additional Cu from the lines.

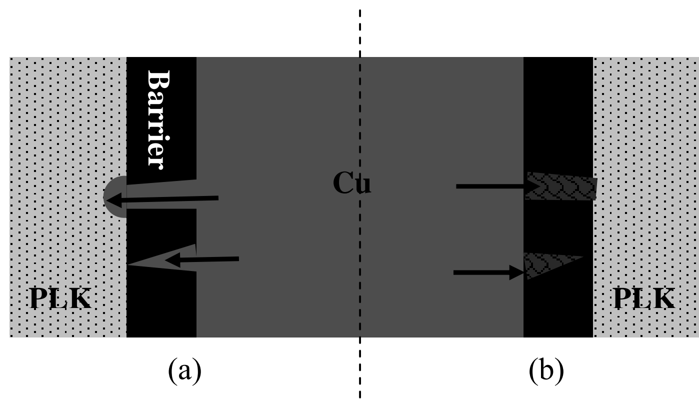


Figure 2.14 (a) Cu diffuses out of the line through the defects in diffusion barrier in Ar test (b) The reaction of Ta and N_2 repairs defects in diffusion barrier protecting Cu out diffusion in N_2 ambient

Interestingly, Cu extrusions found in samples baked at Ar ambient are not seen in samples tested in N_2 ambient. It is expected that the Cu line should experience the similar failure characteristics in both N_2 and Ar ambient since the mechanical conditions are the same for both. However, the fact that no noticeable extrusion is observed in the samples tested in N_2 ambient suggests that N_2 may be helpful in preventing Cu leakage. This can also be supported by the electrical resistance results: the samples tested in N_2 survive much longer than those in Ar. Although further evidence is required, N_2 may react with Ta forming TaN_x during the test in N_2 ambient, which partly repairs the defects in the barrier and provides further protection. It is

reported that TaN_x is likely to have an amorphous-like or stuffed polycrystalline face-centered (fcc) structure, which could provide better protection for Cu diffusion since such structures reduce the number of grain boundaries [79-80].

2.3.3 The Role of Diffusion Barrier on Thermal Instability

The thermal stability investigation in air ambient shows that the incubation period is mainly driven by the thickness of Ta, as discussed in section 2.1.1. The thicker the Ta layer is, the longer the incubation period is. The near absence of an incubation period in the samples with the thinner Ta (0.5nm) barrier, as shown in figures 2.3 and 2.4, suggest that the defects, such as pin-hole or grain boundary, may exist in Ta diffusion barriers in the as-received condition. These defects may be produced during deposition or subsequent processing, and develop further during the thermal test since Cu suffered large compressive stress as a result of mismatch in the CTE of Cu and Ta during baking. As the defects grow, high diffusivity paths in the Ta are established and extensive Cu is pulled from the lines by oxidation (if abundant oxidants are present) and stress potential. Although the incubation period in samples with thick Ta (25nm) is much longer than that in thin Ta (0.5nm) (figure 2.4), Cu out-diffusion still occurs at unexpected speed. It is our belief that such defects in diffusion barrier trigger the failure of Cu interconnects. The formation of extensive voids in samples tested in air and the formation of extrusions at the interface of Ta/PLK in samples tested in Ar ambient provide the evidence for insufficient quality of diffusion barrier in Cu/PLK interconnect structures. This is consistent with some published research. Jia–Ning Sun, et al, reported that 25nm Ta layers deposited using the SEMATECH baseline deposition process do

not form continuous barriers on a porous organosilicate film and numerous pinholes were observed on their sample [41].

However, our efforts to identify the defects in diffusion barrier using conventional method (TEM observation after thermal test) failed. This is thought to be because the defects are too tiny and localized in the large diffusion area, as discussed in 1.2.3.1.

Furthermore, the high quality diffusion barrier is becoming even more difficult to achieve as the thickness keeps shrinking down to a few nano-meters and pores are introduced into the low κ structure. In that case, a tiny defect may degrade a device and cause the device failure eventually. Therefore, it is very critical to have an effective characterization technique for detecting such tiny defects in diffusion in order to facilitate the seeking of the diffusion barrier with near perfect quality.

2.3.4 The Role of Porous Low κ Materials on Thermal Instability

Although defects in the barrier may be sufficient to create a Cu interconnect reliability problem, it is when they are combined with PLK that Cu reliability suffers most. First of all, pores can be highly interconnected when the porosity is greater than 25~30%, providing a unique situation. Rapid Cu diffusion can occur along pore surfaces and Cu can be relocated to pores where it can reside without concern about solubility or creating stress. Secondly, contaminants from processing or ambient can travel deep into the pore structure, creating instability factors, such as oxidation potential. Thirdly, it is reported that the pore morphology may alter during thermal

baking [65,71]. With the open structure of PLK, any thermodynamic instability, such as contaminants and collapse or coarsening of pore structure, may accelerate Cu interconnect failure, for example, more Cu out-diffusion through diffusion barrier if the barrier is not adequate. In addition, the roughness of the pore structure of PLK makes it very difficult to deposit a continuous defect-free barrier layer. Therefore, a combination of the insufficient diffusion barrier and pore structure in PLK initiates Cu/PLK integration to fail by thermal baking only.

2.4 Summary

A series of thermal tests of Cu interconnects integrated with PLK in various ambient have been investigated in this study in order to understand the failure mechanism of Cu/PLK interconnects. A combination of electrical examination and microscopy observation indicates that Cu interconnects fail due to Cu out-diffusion through diffusion barrier by thermal baking only, and the speed of out-diffusion is a function of driving force, barrier integrity, openness of the porous PLK structure, and temperature.

The out-diffusion of Cu is driven by two mechanisms: oxidation mechanism with the presence of abundant oxidants and stress. In air ambient, abundant oxidants are infiltrated into the pores of PLK and provide a primary driving force for Cu out-diffusion. Once through the barrier, Cu quickly disperses and forms stable Cu oxide in the PLK, leaving extensive voids in the lines and causing the increase in resistance. In the absence of abundant oxidants, the stress gradient becomes the primary driving force for Cu out-diffusion, but it is not strong enough to create extensive voids because the

local stress is released as the Cu diffuses out and therefore no driving force for pulling additional Cu from the lines.

The integrity of diffusion barrier and the openness of PLK structure are considered to be two leading factors affecting the reliability of Cu/PLK interconnects. On the one hand, pre-existing defects in the diffusion barrier can further develop during thermal baking and open a high diffusion path for Cu out-diffusion. On the other hand, the open structure of PLK enhances thermodynamic instability. Firstly, the ambient gas is found to be able to infiltrate into PLK and provides a driving force for Cu diffusion through the barrier if it is not robust enough. Also a highly interconnected pore network in PLK provides sufficient space for Cu to reside without concern about the solubility and back-stress issue. Therefore, it is important to have an effective methodology to detect the integrity of diffusion barrier and characterize the structure of low κ material. However, there is no effective characterization technique to evaluate both diffusion barrier quality and low κ structure for as-processed wafer.

CHAPTER 3

VOLTAMMETRY-BASED METHODOLOGY FOR CHARACTERIZATION OF Cu/LOW-κ INTEGRATION

3.1 Motivation for a New Characterization Methodology

The study on thermal stability of Cu interconnects integrated with PLK in chapter 2 reveals that Cu/PLK interconnect reliability depends heavily on the quality of the diffusion barrier and the stability of the pore structure in PLK. However, the conventional characterization methods for detection of barrier defects are ineffective and time consuming while currently available techniques for characterization of low κ structure are only effective on blanket film, not the patterned wafer.

Currently, the integrity of the diffusion barrier is examined using electrical test methods, such as BTS, EM testing and TDDB, followed by a direct observation of the barrier microstructure using TEM. However, these methods are time-consuming and ineffective. In sum, all the electrical tests are long time tests, and conducted with accelerated conditions, such as, high temperature, high current density, high bias, etc. All those factors have the potential to produce false diagnosis. Also TEM is a technique to characterize very small area, and not very effective to characterize tiny and localized defects on a very large area. It is highly possible that the examined area does not contain any defects at all. However, as the thickness of barrier reaches the nanometer scale, a tiny defect in the barrier may degrade the device and cause failure eventually.

On the other hand, although several techniques for characterizing pore structures are available, such as PALS, SXR, SAXN, and measurement of solvent diffusivity [67-70], they are all effective only for blanket films, not for patterned interconnects. Regardless of the high cost and requirement for complex modeling, each technique has very limited functions. For example, SXR is only useful for determination of porosity and film density; SANS is another way to determine porosity. PALS has more functions. It is able to determine porosity, pore interconnectivity, and even pore size distribution, but only for isolated pore structure. But pores will tend to be highly interconnected in future devices due to the aggressive requirement of ultra low κ value to further reduce RC delay. Measurement of solvent diffusivity is a simple, low cost method but it is only for predicting pore interconnectivity. Moreover, low κ structure suffers from thermal instability and alters its characteristic during thermal annealing [65, 71]. The current methods mentioned above are not able to trace its change in patterned structures. Therefore, it is essential to develop a method to characterize low κ structures in patterned wafers instead of blanket film in order to understand the impact of low κ structure on the product reliability and thereby optimize processing conditions and the resulting properties.

This chapter introduces a simple voltammetry-based methodology which appears to meet the need for both the detection of defects in diffusion barriers and the characterization of low κ structure including PLK and DLK in as-processed Cu/barrier/low κ integration. The concept of the method is simple and straightforward, resembling a conventional two-electrode electrolytic cell, consisting of two Cu/barrier

interconnects acting as two electrodes and electrolyte that infiltrates into the low κ structure. By using different types of voltammetry techniques, the conditions of diffusion barrier as well as low κ structure can be characterized quickly at room temperature.

3.2 The Proposed Characterization Methodology

3.2.1 The Methodology for Barrier Defects Characterization

3.2.1.1 Cyclic Voltammetry Basic

Voltammetry is a common technique in electrochemistry that deals with the transfer of electrons from one substance to another. This transfer creates a current resulting from the application of voltage. The simplest voltage waveform used in the voltammetry technique is linear sweep, in which the voltage is changed as a linear function of time [81-83].

Cyclic voltammetry is the most widely used technique for acquiring qualitative information about electrochemical reactions. The power of cyclic voltammetry results from its ability for the determination of formal redox potentials, detection of chemical reactions that precede or follow the electrochemical reaction and evaluation of electron transfer kinetics. In particular, it offers a rapid location of redox potentials of the electroactive species, and convenient evaluation of the effect of the electrolyte media upon the redox process. It also has the advantage that the product of the electron transfer reaction that occurred in the forward scan can be probed again in the reverse scan [81-82].

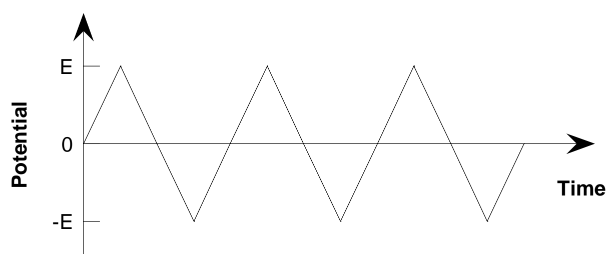


Figure 3.1 The potential waveform in a cyclic voltammetry

In a cyclic voltammetry, the applied voltage is ramped as a linear function of time, and then ramped linearly in reverse back to the initial voltage, showing an isosceles triangle shape (figure 3.1), and the responding current under the applied voltage (I-V) is recorded in a cyclic voltammogram. The cyclic voltammogram is a complicated, time-dependent function of a large number of physical and chemical parameters, such as, the rate of electron transfer reactions, the mass transport, the voltage sweep rate, etc. Figure 3.2 illustrates a typical I-V of a reversible redox couple during a single cycle. It is assumed that only reduced form (R) is present initially. Thus, a positive voltage scan is chosen for the first half cycle, starting from a value where no reduction occurs. For the forward scan (in the range of positive voltage sweep), there is no net conversion of R into the oxidized form (O) at voltages lower than the redox potential (point A). As the redox potential is approached, there is a net anodic current which increases exponentially with voltage. As R is converted into O ($R \rightarrow O$), concentration gradients are set up for both R and O, and diffusion occurs down these concentration gradients. At the anodic peak (point B), the redox potential is sufficiently positive that any R that reaches the electrode surface is instantaneously oxidized to

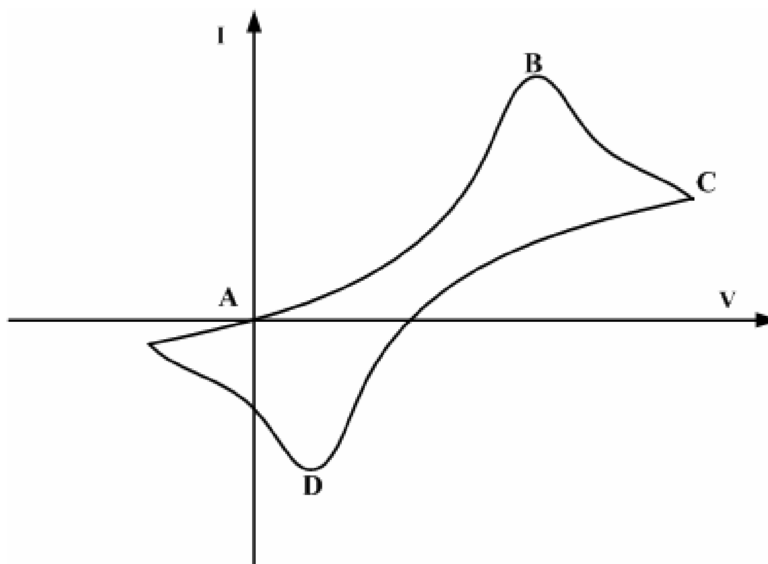


Figure 3.2 The typical current-voltage (I-V) curve in a cyclic voltammetry

O. At this point, the rate of mass transfer to the electrode surface (diffusion) is becoming the limit factor because the flux of reactant to the electrode is not fast enough to satisfy the conversion rate of R to O. Therefore, the current starts to decrease as the concentration of R decreases while O increases near to the electrode. As the applied voltage is reversed to the negative polarity (backward scan), it will reach a potential that will reduce the product formed in the first oxidation reaction and produce a current of reverse polarity from the forward scan. This reduction peak will usually have a similar shape to the oxidation peak for the forward scan.

3.2.1.2 Electrolytic Cell for Voltammetry

Voltammetric measurements utilize an electrolytic cell that consists of at least two electrodes and one electrolyte, as shown in figure 3.3. An electrode may be considered to be an interface at which the mechanism of charge transfer changes

between electronic (movement of electrons) and ionic (movement of ions). An electrolyte is a medium through which charge transfer can take place by the movement of ions.

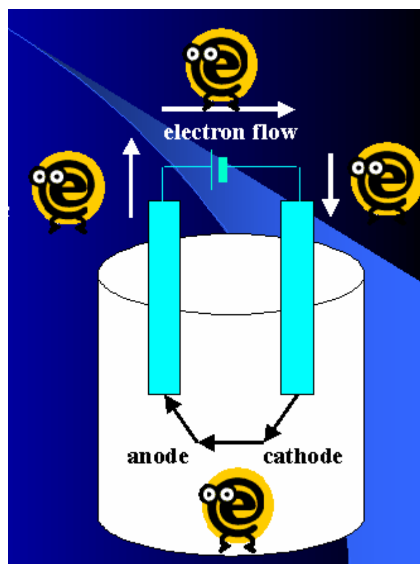


Figure 3.3 A schematic of a two-electrode electrochemical cell [83]

By connecting a power supply to a cell, the energy of the electrons can be raised by imposing a more negative potential on the cathode (negative electrode). They can reach a level high enough to transfer into vacant electronic states on species in the electrolyte. In this case, a flow of electrons from electrode to solution (a reduction current) occurs. Similarly, the energy of the electrons can be lowered by imposing a more positive potential on the anode (positive electrode), and at some point electrons on solutes in the electrolyte will find a more favorable energy on the electrode and will transfer there. Their flow, from solution to electrode, is an oxidation current. The more

critical potentials at which these processes occur are related to the standard potentials, which is specific for the chemical substances in the system.

Under conditions when the potential drop resulting from the solution resistance is small (less than 1-2mV), a two-electrode cell can be used to determine the I-V curve, The voltage is either taken as equal to the applied voltage or corrected for the small potential drop. In experiments where the potential drop resulting from the solution resistance may be high (e.g., in experiments involving nonaqueous solutions with low conductivities), a three-electrode (working, counter and reference electrode) cell is preferable in order to obtain the correct responding current across the cell by precisely controlling the external applied potential. A working electrode, also named as the test electrode, is where the redox reaction takes place. A reference electrode is used to monitor the potential of a working electrode relative to a reference electrode. A counter electrode, also named as an auxiliary electrode, serves as a source or a sink for electrons so that current can be passed from the external circuit through the cell [81].

3.2.1.3 The Working Principle for Barrier Defect Characterization

The working principle of the method for detection of barrier defects is simple and straightforward, sharing some similarities with a conventional two-electrode electrolytic cell for cyclic voltammtry. It utilizes the fact that liquid, including an electrolyte, can infiltrate into a low κ layer. When an electrolyte infiltrates the area between two barrier/Cu interconnect structures, it creates a situation essentially the same as a two-electrode electrolytic cell. The two interconnects act as the electrodes, and they are electrically connected through ions in the electrolyte. When an external

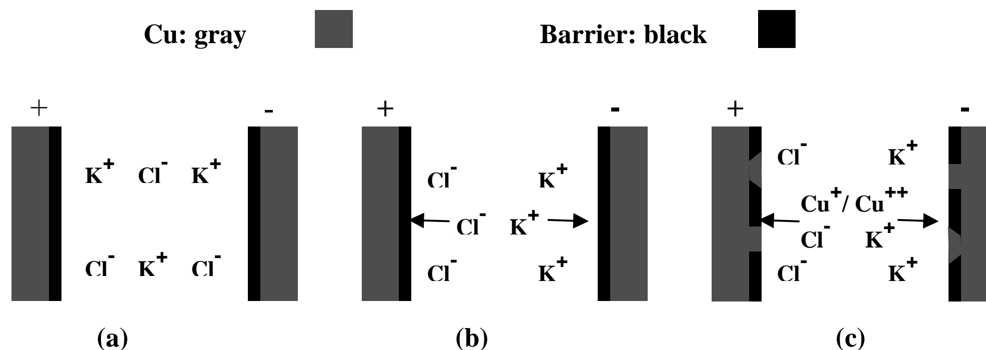


Figure 3.4 A schematic for working principle (a) Electrolyte solution infiltrates in the two electrodes (b) The current resulted from ionic charging under the applied voltage in the case of an intact barrier (c) The current resulted from both Cu redox reaction and ionic charging in the case of a defective barrier

bias is applied to these two electrodes, ionic current and/or reaction current are produced. Ionic current is a result of ion drift in electrolyte under electric potential. For example, in the case of KCl electrolyte, K^+ drifts to cathode while Cl^- drifts to anode with the applied voltage. The reaction current is a result of redox/electrochemical reaction when the electrodes are electrochemically active. The reaction, depending on the type of metals exposed to the electrolyte and the level of the external potential, adds/drains the ions to/from electrolyte, producing a current additional to the ionic current.

When a barrier is intact (defect-free), the electrolyte is connected to Ta. During the voltage sweep less than ±1V, Ta is electrochemically inert and dose not undergo a reaction [84-85]. Therefore, only ionic current resulting from electrolyte ion migration contributes to the net current. This is analogous to an RC circuit, which is described in Appendix A. When a cyclic potential is applied on two interconnects, the ionic current

increases initially as the voltage increases and then reaches a steady value as ions accumulate and saturate at each electrode because the concentration gradient acts against the external bias. When the bias direction is reversed, it will produce a current of reverse polarity from the forward scanning and show a similar I-V shape (0-E-0). As a result, the I-V shows a simple hysteresis in the case of an intact barrier as seen in figure 3.5

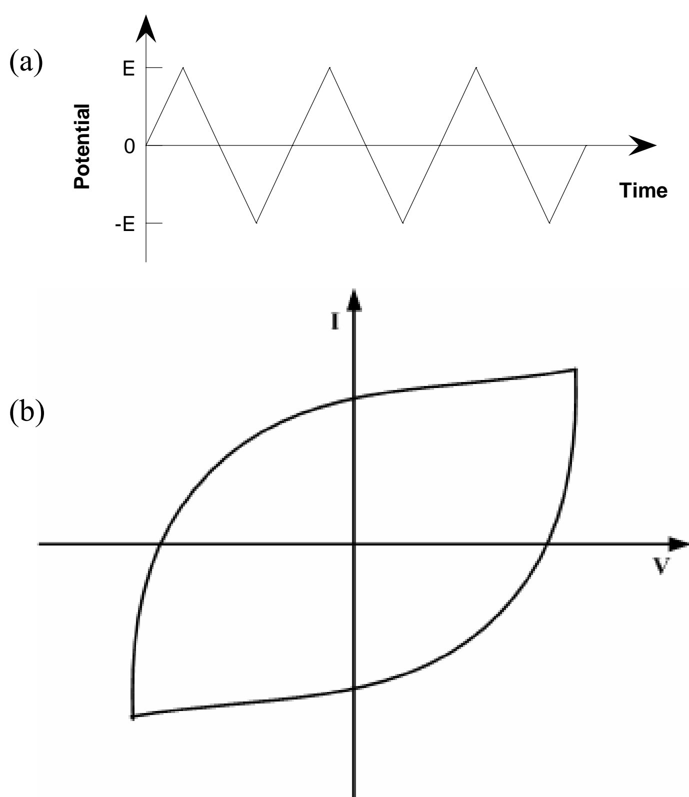


Figure 3.5 An intact barrier presents hysteresis I-V curve (b) under a cyclic potential sweep (a)

On the other hand, when the barrier is defective, the electrolyte is also connected to Cu through the defects and Cu redox reactions are induced [87-88] during the designed test voltage. Similar to a conventional cyclic voltammetry for a reversible

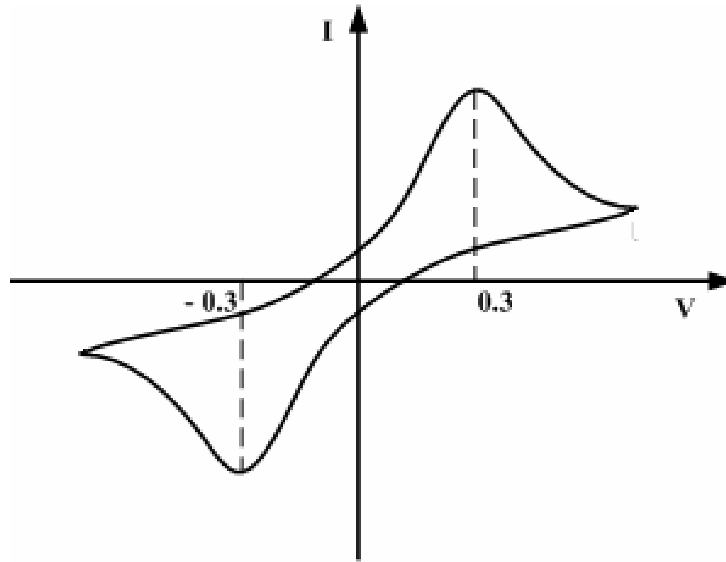


Figure 3.6 The presence of current peaks suggests a defective barrier

redox couple mentioned in 3.2.1.1, the reaction peaks should be present at the redox potential of Cu in the I-V results, as shown in figure 3.6. As the voltage starts sweep, initially, only the current resulting from ion drifting (K^+ and Cl^-) increases linearly with the applied voltage until Cu reaction occurs (Equation 3.1) adding a huge extra current in the cell as the voltage approaches to the redox potential of Cu (0.34V). As the voltage sweep further, the net current reaches to the peak and starts decreases as the concentration of Cl^- decreases and Cu^{++} increases closely to the positive Cu interconnect, which shift the equilibrium in Cu reaction system to the left side:

$$Cu - 2e \rightarrow Cu^{++} \text{ (at 0.34V)} \qquad 3.1$$

As the polarity of the voltage is reversed, a same current profile is produced resulting from the other Cu interconnect. Therefore, in the case of defective barrier, the current peaks are present in the I-V result due to the Cu redox reaction while a simple hysteresis

I-V with the absence of the current peaks is present in the case of intact barrier due to the lack of a condition for initiating the redox reaction.

3.2.2 The Methodology for Low κ Structure Characterization

3.2.2.1 Step Voltammetry Basic

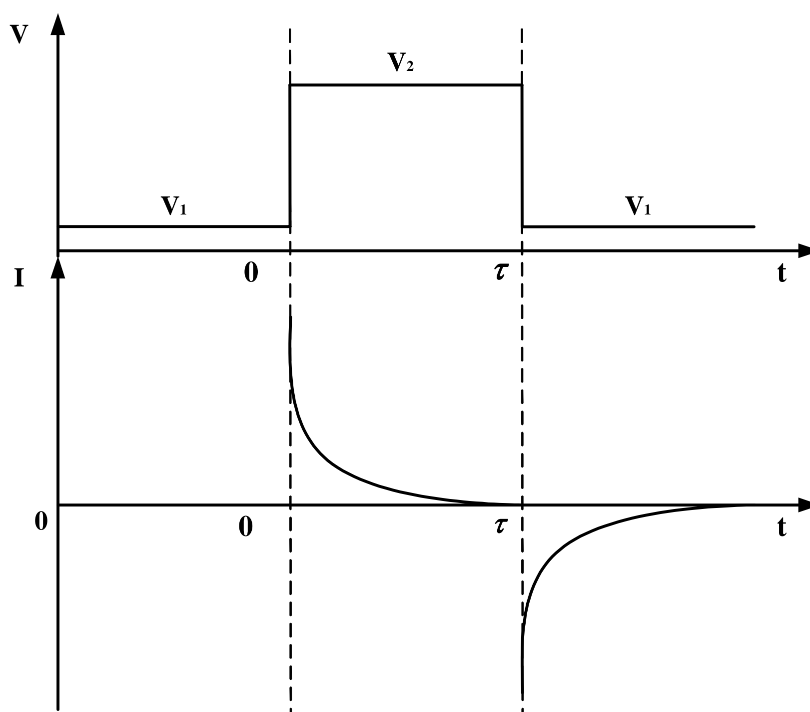


Figure 3.7 The waveform of potential step voltammetry and the responding current as a function of time

In the potential step voltammetry the applied voltage is instantly jumped from one value V_1 to another V_2, as shown in figure 3.3. Generally, one (V_2) is set to be in the potential range where charge-transfer process occurs while the other (V_1) is set to be

in the potential range that charge-transfer process does not occur. When t<0; $V=V_1$, no charge-transfer occurs, and so no current is flowing. As voltage reaches to V_2, the charge-transfer process occurs, and a large current begins to flow and then starts to drop dramatically. The current response to the potential step is controlled by the diffusion rate of ions/reactants in the bulk solution to the electrode surface, and the diffusion rate is controlled by the concentration gradient of reactants between the bulk solution and the electrode surface. This provides an explanation for the decrease in the current as a function of time, that is, the decrease in the concentration gradient between the bulk solution and the electrode surface as a function of time [81-83].

3.2.2.2 The Working Principle for Low κ Structure Characterization

The working principle of pore structure characterization shares some similarities with that used for detection of barrier defects: a two-electrode electrolyte cell is formed by the full infiltration of electrolyte solution into an interconnect test pattern having two parallel barrier/Cu interconnects spaced with low κ material. However, the study focuses on the low κ structure. For this reason, the prerequisite for the test is that the samples must have an intact barrier and no Cu exposed to the electrolyte. As a result, the current in the cell is only a result of the ion drifting when an external bias is applied and reflects the condition of the low κ layer between two interconnects.

Instead of cyclic voltammetry used for barrier defects detection, step mode voltammetry is used for low κ structure characterization. In our method, a constant bias is applied across the electrodes for a time sufficient for ion saturation (termed as charging process) to occur, followed by the abrupt removal of the bias for completely

discharging (termed as discharging process). The responding current generated by ion drifting under the electrical field (named as charging current) and restoration of ionic equilibrium (named as discharging current) is measured. The behavior of the discharging current resembles that of an electrical capacitor because, in both cases, the current results from variation in charge density at the electrode surfaces. However, in step-mode voltammetry, the variation in the surface charge density is the result of the migration of electrolyte ions not polarization of dipoles. Generally, the net current in an electrolytic cell consists of migration (electric field related), diffusion (chemical potential related, for example, a concentration gradient), and convection (stirring or hydrodynamic transport) current. When the convection of the electrolyte solution in the cell is ignored, the discharging current is only driven by diffusion of the electrolyte ion. As a result, by monitoring the diffusivity of electrolyte ion in solution infiltrated in low κ structure, the structure of low κ layer is able to be characterized.

3.3 Samples and Experimental Apparatus

3.3.1 Samples

Among various patterns existing in the wafer, standard comb structure is selected to be the typical samples for the characterization of diffusion barrier and low κ structure. Figure 3.8 presents the schematic diagrams of the pattern with comb structure. With the large interface area provided by the comb structure, the current is relatively easy to detect without interference from background noise, making it an ideal choice.

A couple of electrolytes, including HCl, KCl and NaCN, are attempted for Cu/barrier/low κ integration system, and the dilute KCl is selected to be the standard electrolyte due to its relative stability with the materials in the test structure.

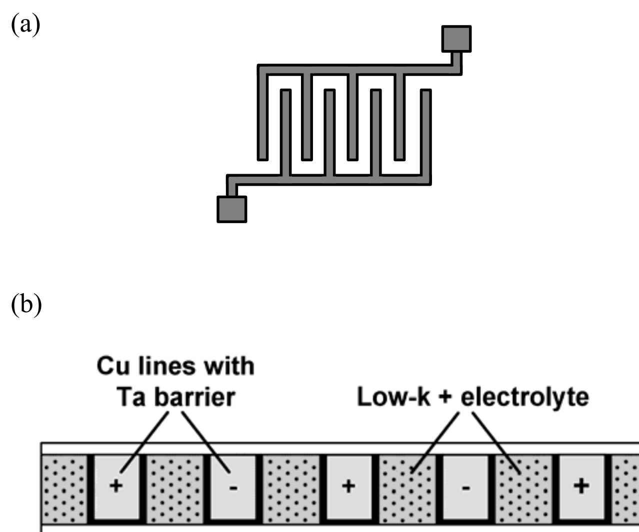


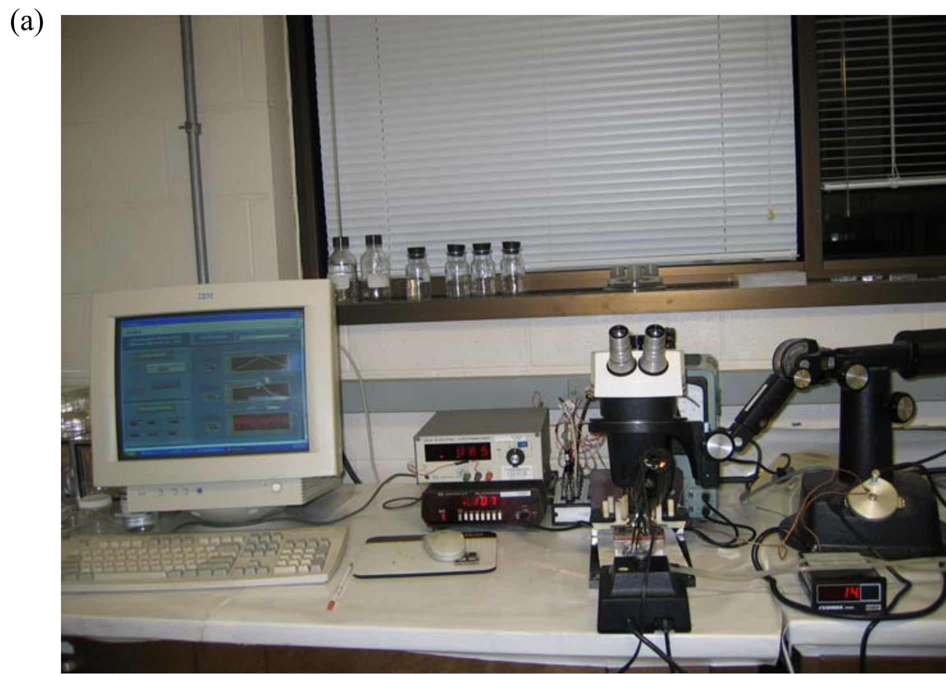
Figure 3.8 A schematic diagram of (a) comb pattern (b) cross-section comb structure test pattern.

3.3.2 Experimental Apparatus

The voltammetry-based technique does not require any special instruments, and a couple of common instrument is able to implement the tasks. As seen in figure 3.9, which presents a picture of the experimental set-up and its circuit schematic, the setup consists of a voltage sweep generator, a pico-ammeter and a capacitor. The pico-ammeter measures the current while bias is applied with a constant rate [86]. Although our study (in chapter 2) found that the liquid infiltration into PLK structures can occur quickly, it is important to ensure that the infiltration is completed before data collection.

For this reason, capacitance change of the comb structure is continuously monitored, and it increases as infiltration proceeds because it adds ionic dipoles between the electrodes.

(a)



(b)

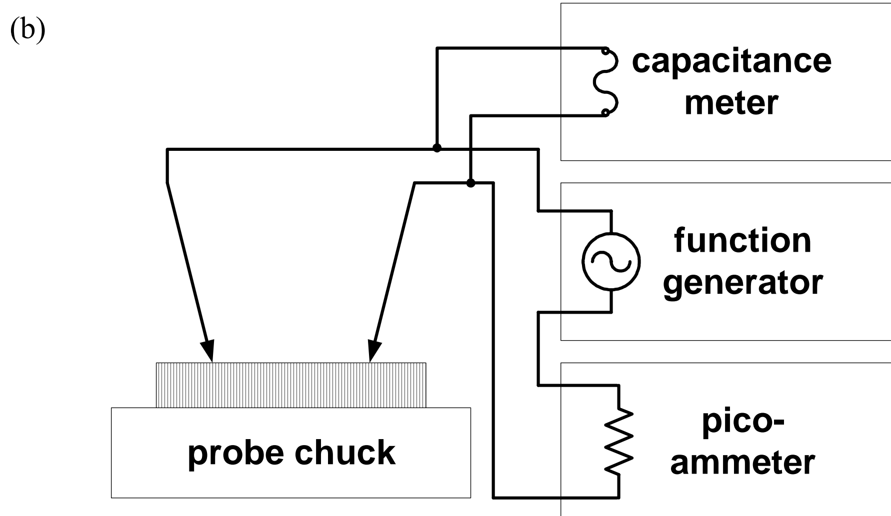


Figure 3.9 A picture (a) and a circuit schematic (b) of the buildup apparatus.

3.4 Summary

This chapter introduces a voltammetry-based methodology which has a potential to detect the defects in diffusion barrier and evaluate low κ structure. In the proposed method, a particular two-electrode electrolytic cell is established. The liquid, including an electrolyte, infiltrates the low κ layer of Cu interconnect and acts as an electrolyte while the two barrier/Cu interconnects act as two electrodes in this cell.

The condition of the barrier is characterized by monitoring the current resulting from an applied voltage with triangle waveform (I-V curve). When the barrier is intact (defect-free), the I-V shows simple hysteresis because the barrier is electrochemically inert and thus does not undergo reaction during the test sweep voltage (< ±1V), and therefore only ionic charging contributes to the current. On the other hand, when the barrier is defective, Cu redox reactions are induced during the test voltage because of the exposure of Cu to electrolyte, and consequently reaction peaks are present in the I-V results.

The characterization of low κ structure utilizes step voltammetry. The samples with intact barrier are subjected to a constant voltage for sufficient time to fully drive electrolyte ions to the electrodes. Then the voltage is removed abruptly and discharging current is generated by the restoration of ionic equilibrium. Since no external voltage is applied during the discharging process, the discharging current is controlled by the diffusion of electrolyte ion and reflects the condition of low κ structure. Therefore, the

low κ structure is able to be characterized by measuring the diffusivity of ions in the electrolyte.

CHAPTER 4

STUDY OF DIFFUSION BARRIER STABILITY USING VOLTAMMETRY

In this chapter, the integrity of diffusion barrier in Cu interconnect integrated with low κ material is investigated using the method proposed in chapter 3. Although the method shares some characteristics with conventional two-electrode electrolyte voltammetry, such as a measurement of current-voltage (I-V), it has somewhat different operating principles. For example, both electrodes are working electrodes and no reference electrode is present in this set-up. Also Cu/barrier/low κ integration provides the unique situation, such as varying dielectric density, porosity, and pore distribution. All these affect the Cu reaction as well as diffusion mechanism and consequently the characteristic shape of the voltammogram. These contributing factors lead to I-V results that are complex and somewhat counter-intuitive to interpret. Therefore, in this chapter, idealized samples are used first to better understand the working principle of the proposed method, and also to simulate various barrier conditions that may serve as the reference I-V curves for Cu/barrier/ low κ integration. Afterwards, the samples with fully fabricated interconnect structure are evaluated using the method. Finally, the significance as well as the limitation of the method is discussed.

4.1 The Development of Fundamental Theory

4.1.1 Sample and Test Condition

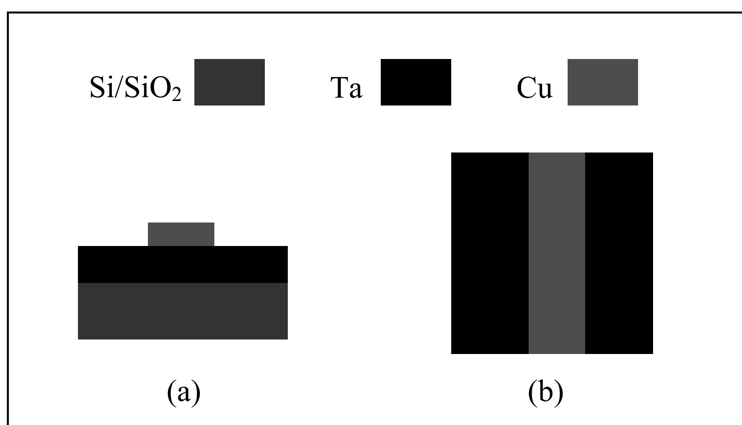


Figure 4.1 Schematic diagrams for idealized samples with controlled Cu fraction (0~100%) used for fundamental study (a) top-down view (b) cross-section view

The fundamental study for the voltammetry method is conducted on idealized samples with controlled Cu/Ta ratios using the built-up system seen in figure 3.9. The idealized samples are made by firstly depositing a 1500Å Cu film on Si/SiO_2 substrate coated with 2000Å Ta film, then patterned with various line-widths of Cu (the range of Cu fraction is from 0% to 100%), and cleaved into 1 cm^2 pieces. Figures 4.1-a,b present schematic diagrams of the idealized samples used for fundamental study.

Three possible barrier conditions are simulated using idealized samples. First of all, the case of an intact barrier is simulated by samples made of Ta blanket film (Ta electrode). Ta electrodes are also used to study the effects of primary test parameters on the feature of I-V curves. Secondly, the case of a defective barrier with equal defect

density (symmetrically defective barrier) is simulated by samples containing the equal Cu fraction. Lastly, the case of defective barrier containing unequal defect density (asymmetrically defective barrier) is simulated by samples coated with unequal Cu fractions.

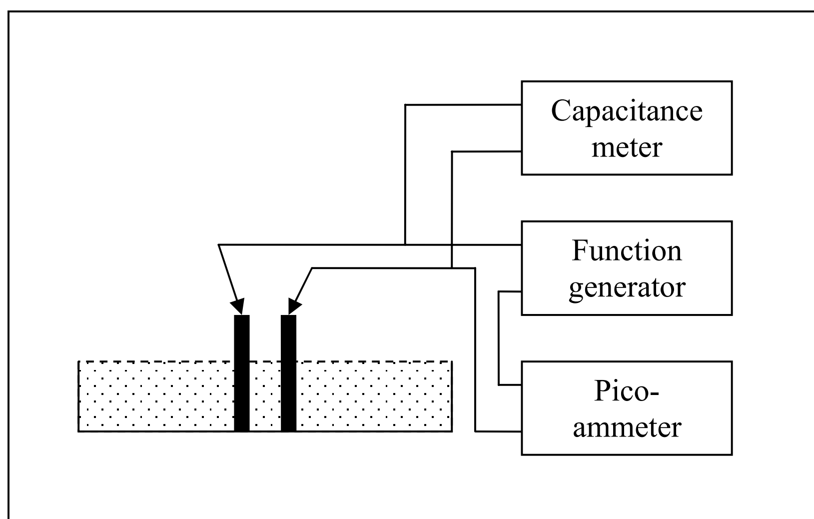


Figure 4.2 A schematic diagram of I-V test using idealized samples

In the fundamental study, as seen in figure 4.2, which shows a schematic diagram of the I-V testing, two idealized samples acting as two electrodes (electrode samples) are placed in a cell that has the same width and half the height of the electrode samples. Note that no dielectric layer is present between two electrode samples. An electrolyte solution of deionized (DI) water containing 2% KCl (weight percent) is then injected into the cell. The two electrode samples are subjected to a triangle waveform potential scan (cyclic voltage) with the maximum sweep voltage of ±0.7V at a sweep rate of (7/3)V/min, and the current between the two electrodes is monitored with time. .

4.1.2 Simulation of Various Conditions of Diffusion Barriers

4.1.2.1 Simulation of Intact Barriers

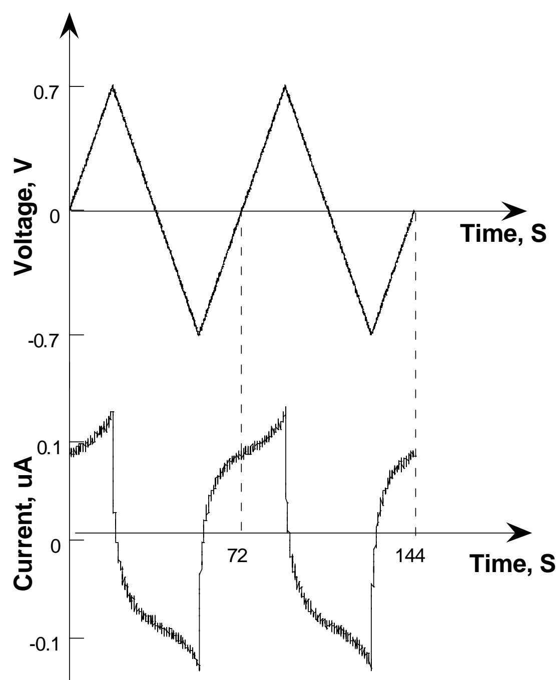


Figure 4.3 The typical current data as a function of time under the applied cyclic voltage in the case of two Ta electrodes, simulating the intact diffusion barrier

The samples used for the simulation of intact barrier are two Ta electrodes, that is, only Ta contacts with electrolyte. Figure 4.3 presents the typical data of the current as a function of time under the applied cyclic voltage of triangle waveform. As is seen, current increases gradually as the voltage ramps up from 0V to 0.7V due to the ionic charging and then drops quickly as the voltage starts decreasing from 0.7V toward 0V because the concentration gradient generated during up-ramp (0 to 0.7V) starts working against the applied external voltage, and the current is zero when the two potential cancels each other (Note that zero current is not produced at zero external voltage).

When the voltage is reversed (0~-0.7V and -0.7~0V; backward sweep direction), it produces a current of reverse polarity from the forward scanning (0~0.7V and 07V~0V) but shows the same current profile with as that for the forward sweep.

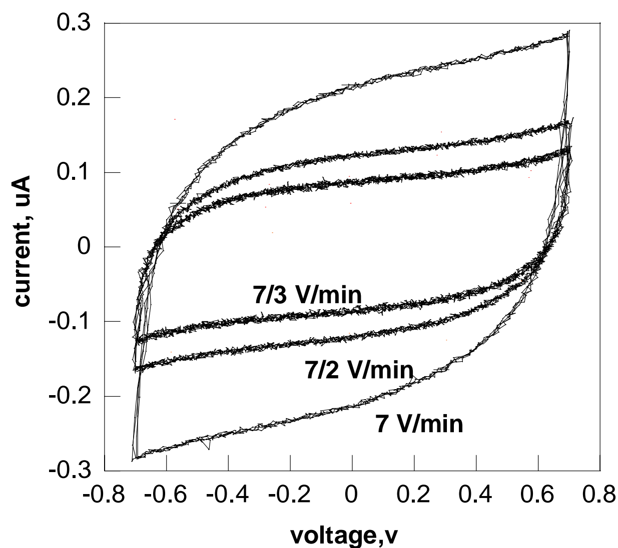


Figure 4.4 I-Vs are taken from two Ta electrodes at various sweep rates

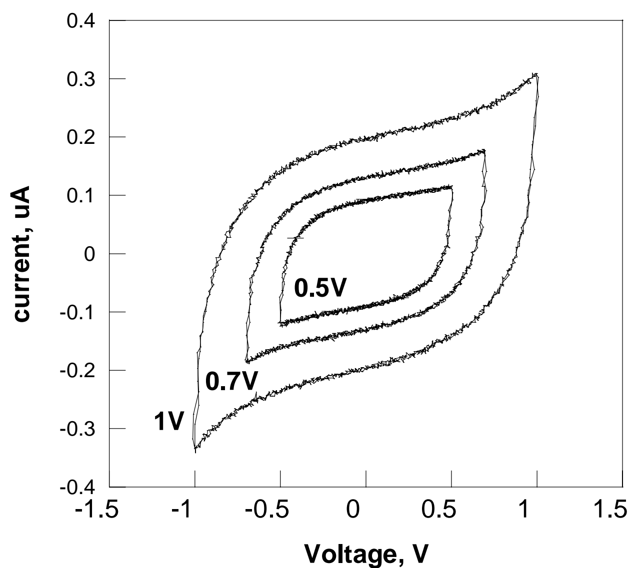


Figure 4.5 I-Vs are taken from two Ta electrodes under various sweep voltages

The I-V curves taken from two Ta electrodes present a typical simple hysteresis without the presence of peaks because Ta is electrochemically inert and no reaction current is produced in this case, as discussed in 3.2.1.3. The slope of the I-V curve increases with the increasing of the sweep rate, as seen in figure 4.4. The increasing of the applied voltage increases the magnitude of the current at the same slope since more charging ions are created as voltage continues to increase, as shown in figure 4.5. Neither sweep voltage nor sweep rate changes the inherent I-V feature.

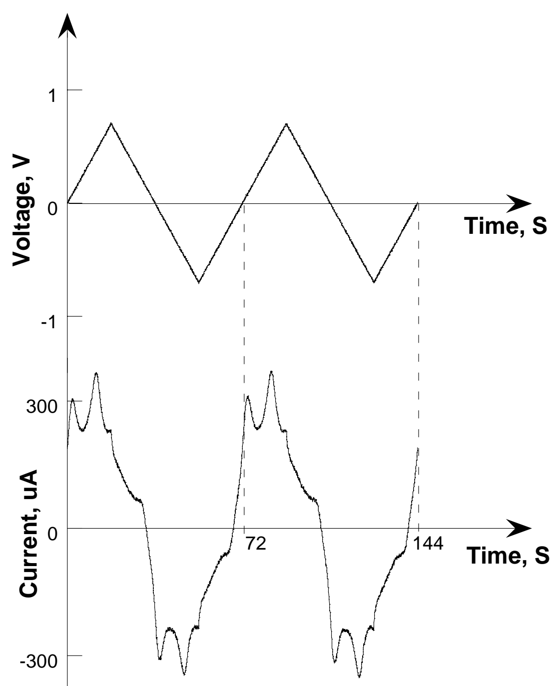


Figure 4.6 The typical current data as a function of time under the applied cyclic voltage in the case of electrodes with symmetric Cu fraction (100% Cu on two mating electrodes in this figure) simulating the defective diffusion barrier with equal defect density.

4.1.2.2 Simulation of Symmetric Defective Barriers

When Cu is present on the Ta blanket film (Ta-Cu electrode), the current peaks produced by various Cu redox reactions are observed. For simulation of symmetric defective barriers, two samples having the same Cu/Ta ratio act as two electrodes (symmetric Cu-Ta electrodes). In this case, two peaks are present for each |V| increasing period (0→0.7V and 0→-0.7V), as shown in figure 4.6, which presents an example of current as a function of time for the case of symmetric Cu fraction exposure.

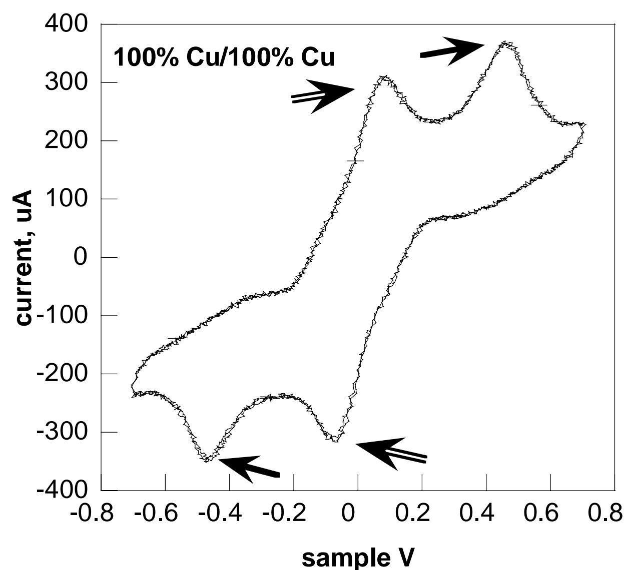


Figure 4.7 A typical I-V is taken from two Cu electrodes (100% Cu)

Figure 4.7, presents a typical I-V curve taken from two Cu electrodes (100% Cu is exposed to the electrolyte). As is seen, two current peaks during both sweep

directions can be identified by the voltage. The first peak, identified around ±0.45V, is determined by the reaction of Cu → Cu^{+} + e (Cu/Cu^{+}) while the second peak, identified around ±0.1V, is determined by the reaction of Cu^{+} → Cu^{++} + e (Cu^{+}/Cu^{++}) [82]. Such two symmetric peaks are consistently observed in all samples with equal Cu fractions (ranging from 1% to 100%) on two mating electrodes in the fundamental study. Figure 4.8 shows another example resulted from two electrodes with symmetric Cu fraction (65%). Note that the magnitude of current peaks drops from about 300~400μA in figure 4.7 (100% Cu electrodes) to 30~40μA in figure 4.8 (65% Cu electrodes), suggesting that the magnitude of current peak is likely to be an indicator of the Cu fraction on Ta layer.

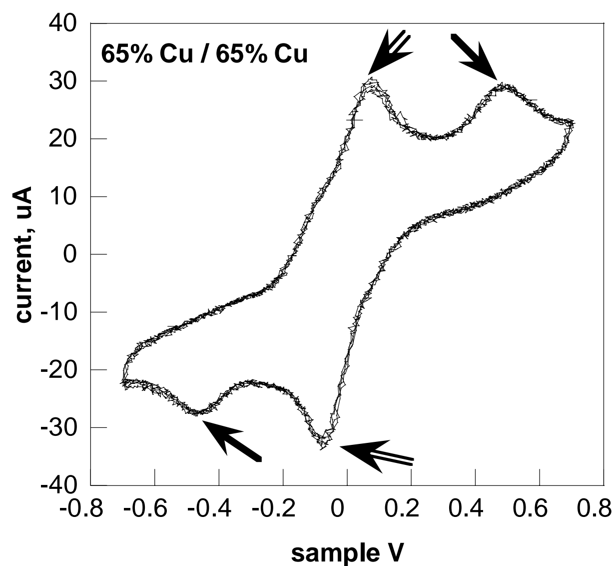


Figure 4.8 A typical I-V is taken from two identical electrodes with 65% Cu exposure

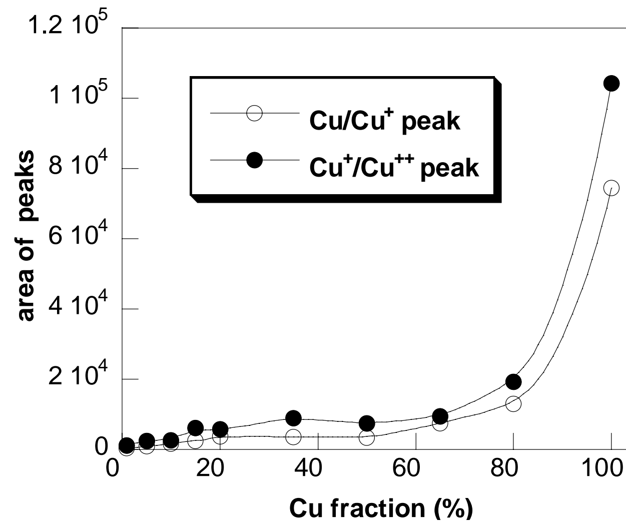


Figure 4.9 The peak area as a function of Cu fraction in idealized samples

Figure 4.9 presents the peak area as a function of Cu fraction. Note that all samples in this figure have equal Cu fraction on two mating electrodes. Each peak area is determined using KaleidaGraph by integrating the area underneath the peak curve that starts from the most bottom point at the left side of the curve and ends at the most bottom point at the right side of the curve. It is clearly seen that the area of the peaks increases dramatically with the increasing of Cu fraction, from 300 units of 1% Cu to 10,000 units of 100% Cu patterned on Ta blanket film. This result suggests the possibility of quantifying the defect density in the case of real interconnects.

4.1.2.3 Simulation of Asymmetrically Defective Barriers

The simulation of varying asymmetrically defective barrier conditions using idealized samples with a different Cu fraction patterned on each of two mating electrodes (asymmetric Cu-Ta electrodes) suggests that the asymmetrical Cu fraction

not only produces asymmetrical peaks in an I-V curve, but also appears to affect the dominant redox reaction.

Figure 4.10 shows the case where one electrode is patterned with 1% Cu and the other electrode is patterned with 5% Cu. It can be seen that the Cu/Cu^{+} peak at 0.45V is stronger than the Cu^{+}/Cu^{++} peak at 0.1V during the forward sweep (0~0.7V) while the Cu^{+}/Cu^{++} peak (-0.1V) is stronger than Cu/ Cu^{+} (-0.45V) during the backward sweep (0 ~ -0.7V). This trend becomes more noticeable with increasing asymmetrical Cu fraction on the two mating electrodes. Figure 4.11-a shows an extreme case. In this case, one electrode has 1% Cu exposure while the other electrode has 65% Cu exposure. It can be seen that the Cu/Cu^{++} (0.1V) peak is completely absent in the forward sweep (0 ~ 0.7V) while Cu/Cu^{+} peak (0.5V) disappears in the backward sweep (0 ~ -0.7V. In

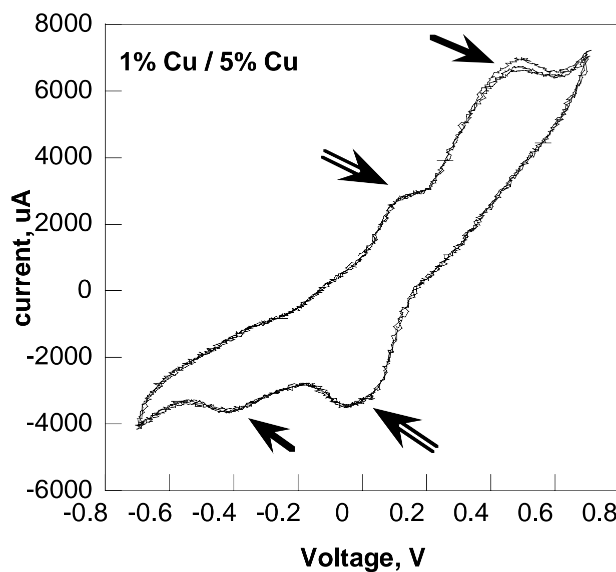
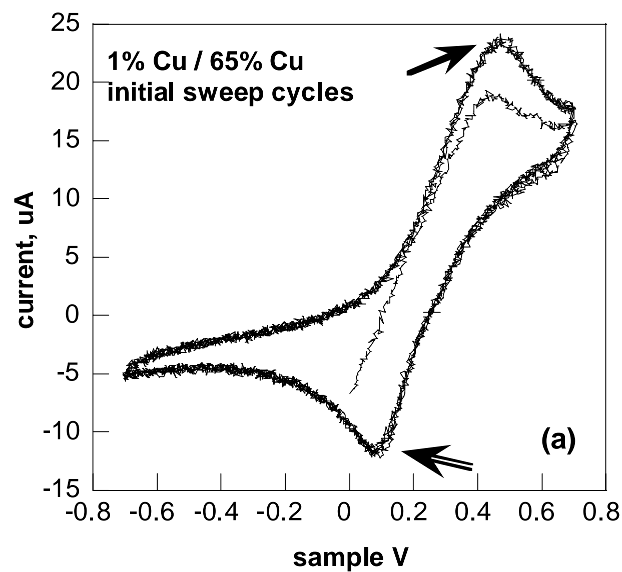


Figure 4.10 An I-V is taken from electrodes with asymmetric Cu fraction, 1% Cu vs. 5%Cu



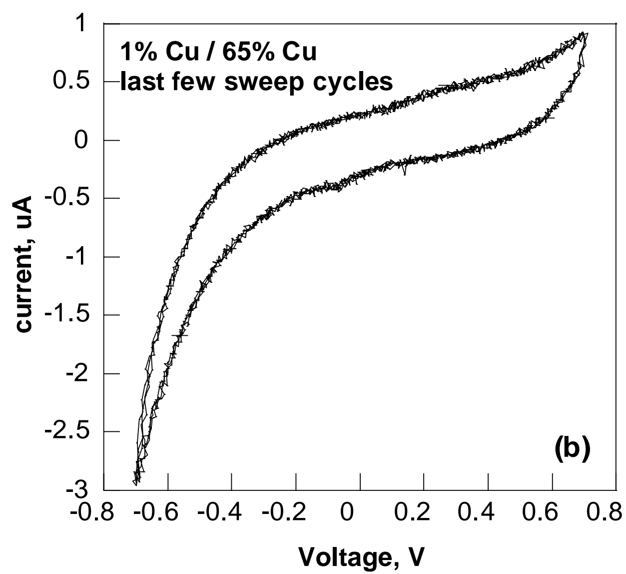


Figure 4.11 The I-Vs taken from the electrodes with asymmetric Cu fraction, 1%Cu vs. 65%Cu at (a) initial sweep cycle (b) very last sweep cycle

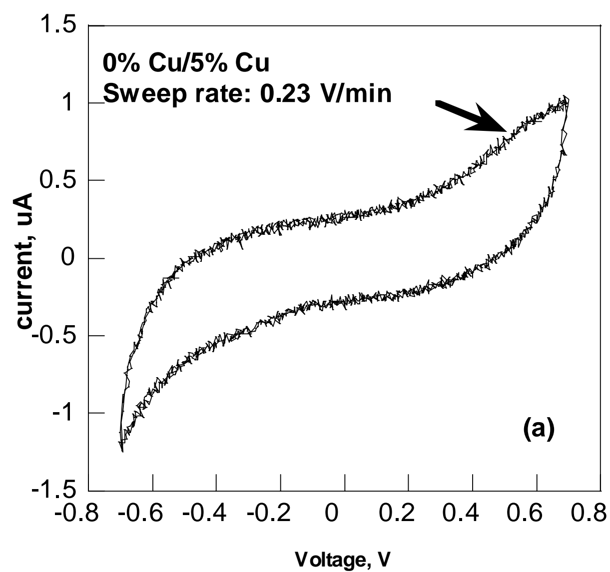
addition, Cu/Cu^+ peak position shifts to the positive potential side. Furthermore, the reaction peaks for both sweep directions are eventually disappear with time, as seen in figure 4.11-b. This may be a result of the complete depletion of electrolyte ions with time.

4.1.2.4 Simulation of Intact/Defective Barrier

Figure 4.12 presents a very interesting result in the fundamental study. In this case, one electrode is pure Ta (Ta electrode) while the other is patterned with 5%Cu on Ta film (Ta-Cu), which simulates the case of one intact barrier and one defective barrier on two interconnects. Instead of asymmetric peaks produced for forward and backward sweeps, the I-V result shows an asymmetric hysteresis. This is unlike the simple hysteresis I-V curve in figure 4.5 in which the upper curves (-0.7V to +0.7V) and bottom curve (+0.7V to –0.7V) mirror each other, a so called symmetric hysteresis. However, the upper curve and bottom curve in figure 4.12a do not overlap. In addition, a near invisible peak at around +0.5V is observed for the forward sweep (0 ~ 0.7V), and the peak becomes clear when a very slow sweep rate (0.046 V/min) is utilized, as is seen in figure 4.12b.

Asymmetric hysteresis I-V curves are consistently observed in all the cases with one Ta electrode and one Ta-Cu electrode, however, the peak becomes invisible even when a very slow sweep rate is used if the Cu fraction on Ta/Cu electrode decrease further. Unfortunately, asymmetric hysteresis alone is not sufficient to suggest one defective barrier because it is possible for other factors to produce asymmetric

hysteresis.



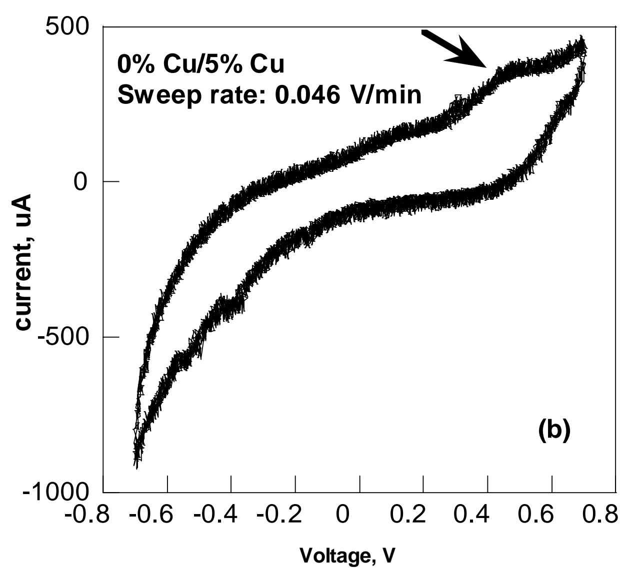


Figure 4.12 The I-Vs taken from electrodes with asymmetric Cu fraction, 0%Cu vs. 5% Cu, at (a) sweep rate: 0.23 V/min (b) sweep rate: 0.046V/min

Asymmetric hysteresis means that the current produced at each electrode is different. This may result from a pair of Ta and Ta-Cu electrodes if the Cu ratio is very small: the net current increases due to Cu reaction, however, the peak is not detected due to the limit of instrument resolution. The different current at the two electrodes may also be created by asymmetrical electrodes area, which provides different charging areas. However, the asymmetric electrodes area should not change the net magnitude of current much because it does not add ions to the solution. This is proven by an investigation on I-V profile produced by two Ta electrodes with asymmetrical electrodes areas.

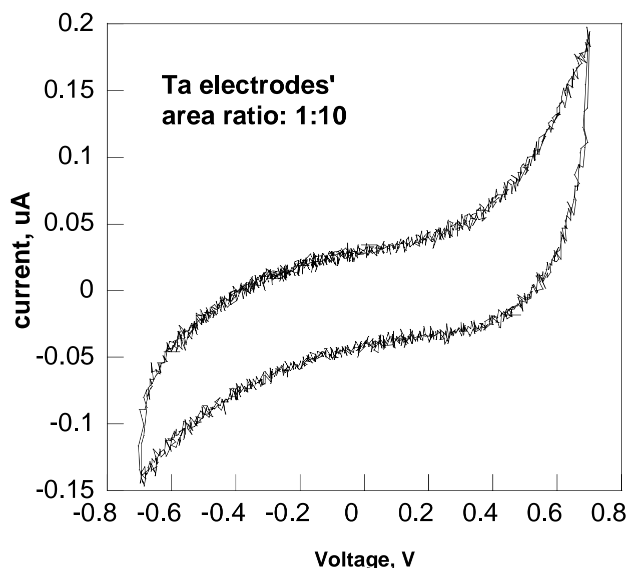


Figure 4.13 An I-V curve taken from two Ta electrodes with asymmetric electrodes' areas: one electrode has an area of 1×1 cm^2 and the other has an area of 10×1 cm^2

Figure 4.13 presents an example of such a symmetric hysteresis created by two Ta electrodes with asymmetric areas (1:2.5). In this case, one electrode has an area of

0.1X0.25 cm^2 while the other has an area of 2.5×1 cm^2. As is seen, the magnitude of the net current in this case is the same order with that produced by two identical Ta electrodes (figure 4.4) at the same sweep rate (~0.15-0.2µA vs. ~0.12µA). The extra current is created by the ionic charging resulting from extra electrode area, which does not greatly change the magnitude of the current. On the other hand, the presence of Cu on one electrode significantly increases the magnitude of net current due to Cu reaction, as is seen in figure 4.12-a, The current is10 times greater than that produced by two identical Ta electrode (figure 4.4) at same sweep rate (~1.2µA vs.~0.12µA). Although it is possible to distinguish the asymmetric hysteresis I-V results created by one defective barrier from those due to asymmetric electrode areas based on the magnitude of the net current, it needs experience.

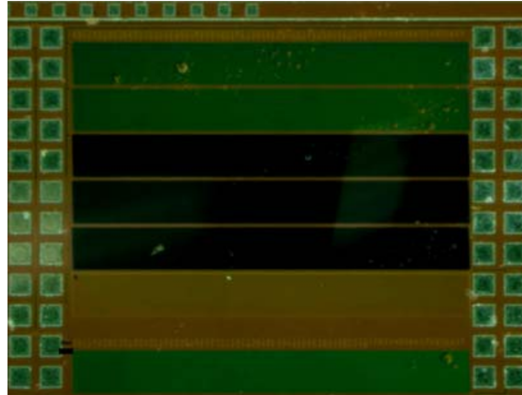
4.2 Barrier Detection for Real Interconnect

The fundamental study makes the working principle of the proposed method more straightforward. By simulating various possible conditions of barrier, it provides reference I-V curves for evaluating the diffusion barrier. In this section, the quality of the diffusion barrier for fully processed interconnect structures will be evaluated using the proposed method based on the understanding from the fundamental study.

4.2.1 Sample Preparation

Two sets of as-received real interconnects are evaluated by the method, as seen in figure 4.14, which presents optical images of the test patterns. One set is the single level comb structure Cu/Ta with porous MSQ-based interconnect, which has a κ value of ~2.2 and estimated porosity of ~45%. The comb structure is of 0.125µm line-width

(a)



(b)

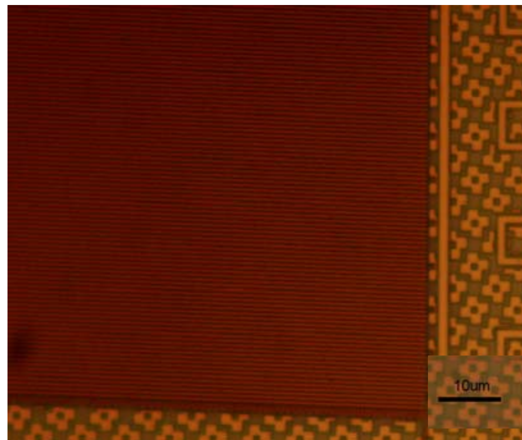


Figure 4.14 The optical images of Cu/DLK interconnect with comb/via chain structure (a) low magnification (b) high magnification

and various spaces (0.175μm~0.35μm). The other group includes comb structure consisting of via chain (comb/via chain) integrated with DLK, which has a κ value of ~2.9 and estimated porosity of <10%. The comb structure is of 0.14μm line-width and 0.13μm space and the via-chain structure is of 0.14μm line-width and various spaces (0.15~0.37μm). The real interconnects samples are fully immersed in an electrolyte solution of 2%KCl (weight percent) for hours/days depending on the density of the low

κ layer, then the I-V measurement is conducted at the same test conditions as the fundamental study.

4.2.2 Results

4.2.2.1 Initial Condition of as-Received Samples

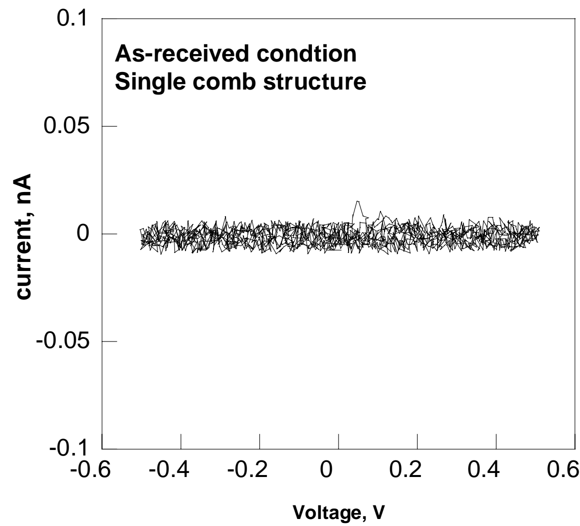


Figure 4.15 A typical I-V taken from the initial condition of single level Cu/PLK interconnects with comb structure.

Figure 4.15 presents a typical I-V of the initial condition of single level Cu interconnects with comb structure. For the initial condition, no electrolyte solution is present. As is seen, almost no current is flowing with the applied voltage because no electrochemical cell is formed with the lack of electrolyte.

Figure 4.16 presents a typical I-V of the initial condition of comb/via chain structure. The small amount of current in this case is attributed to the capacitive charging in the comb/via chain structure because the structure has more electrodes area compared to the single level interconnect comb structure (~4:1).

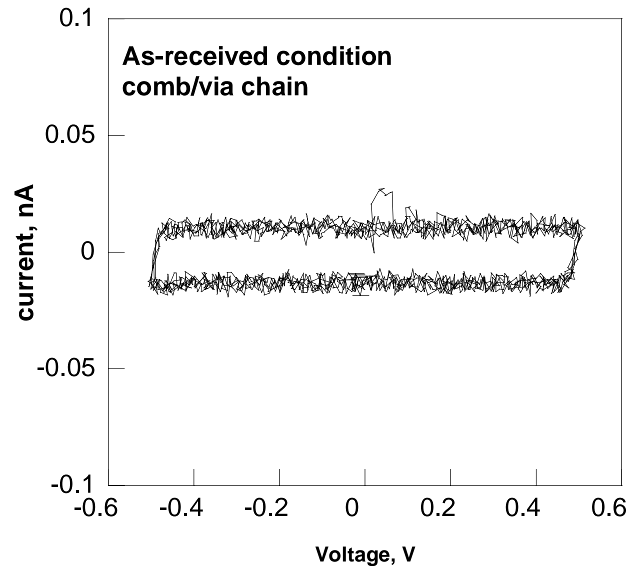
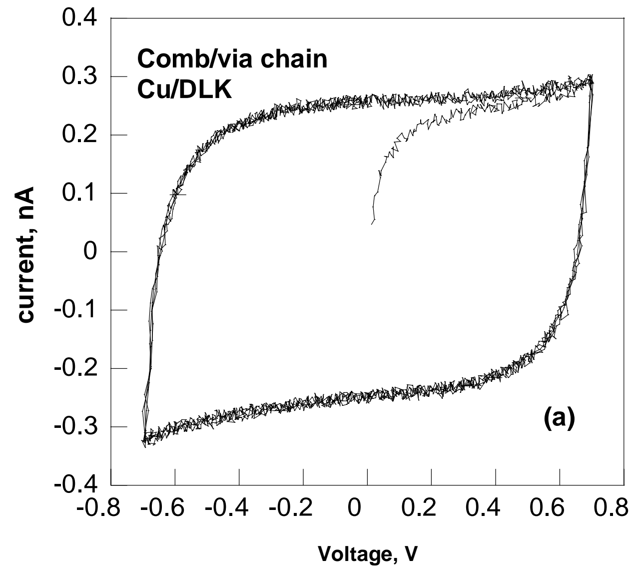


Figure 4.16 A typical I-V taken from the initial condition of two-level Cu/DLK interconnects with comb/via chain structure.

4.2.2.2 Cu Interconnect with Intact Barrier

The I-V curves seen in figure 4.17 a, b, which are taken from (a) two level Cu/10nmTa/DLK with comb/via chain structure and (b) single level Cu/25nmTa/PLK interconnect with comb structure, show simple hysteresis, resembling the results taken from two Ta electrodes in the fundamental study (figure 4.4), and therefore indicate an intact Ta diffusion barrier. Note the overall magnitude of current is dramatically reduced compared to that in the case of the idealized samples in the fundamental study. We believe it is due to the sluggish ion motion in low κ materials and the small cross-section area of interconnects/barrier for ion accumulation.



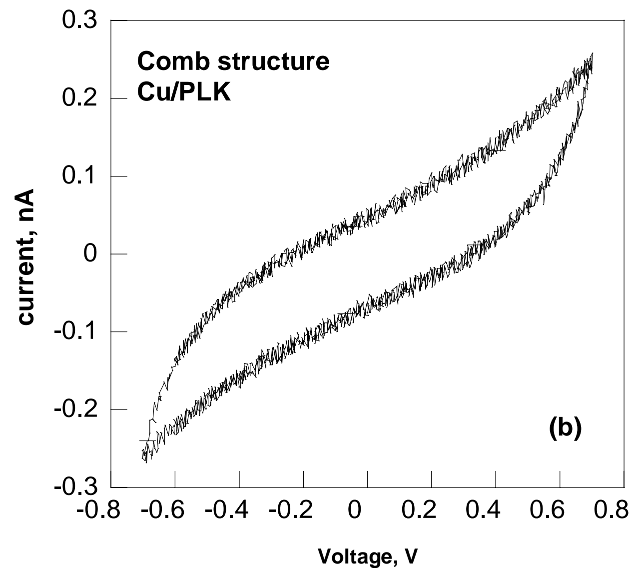


Figure 4.17 The representative I-Vs show a simple hysteresis, indicating an intact barrier, taken from (a) two level Cu/10nmTa/DLK with comb/via chain structure (b) single level Cu/25nmTa/PLK interconnect with comb structure

4.2.2.3 Cu Interconnect with Equal Density of Defects in Barrier

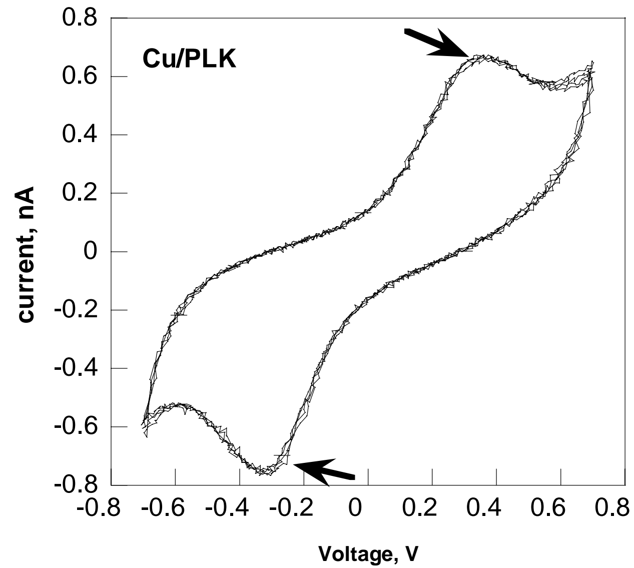
The I-Vs in figure 4.18 are taken from two samples having the same test pattern, a single level comb structure Cu/25nm/PLK interconnect. These show symmetrical current peaks at around ±0.3V. This result suggests an equal defect density on the two Cu/Ta interconnects. Note that a single symmetric peak is produced at a potential of ~0.3V, instead of double symmetric peaks seen in the fundamental study (figure 4.7 and 4.8). The single peak corresponds the Cu redox reaction $Cu \rightarrow Cu^{++} + 2e$ (Cu/Cu^{++}). This can be attributed to the reduced ion motion in the dielectric layer between the two interconnects/barrier, and will be discussed later in section 4.3.

Note that the magnitude of the current in figure 4.18-a is much higher than that that in figure 4.18-b, which may suggest the sample (a) has a higher defect density in its barrier than the sample in 4.18 (b) since the current magnitude is found to be proportional to the defect density in the fundamental study.

4.2.2.4 Cu Interconnect with Unequal Density of Defects in Barrier

The I-V in figure 4.19, taken from single level comb structure Cu/25nm/PLK interconnect, shows asymmetrical current peaks, resembling the I-V result produced by asymmetric Ta-Cu electrodes in the fundamental study (figure 4.11), and therefore suggest that one barrier is more defective than the other.

Figure 4.20 presents a representative I-V result taken from a single level comb Cu/25nmTa/PLK interconnect. As is seen, a single peak at ~+0.5V is observed only in the forward sweep (0~0.7V).This resembles the result for the case of one Ta electrode and one Cu-Ta electrode in the fundamental study (figure 4.2), suggesting an intact



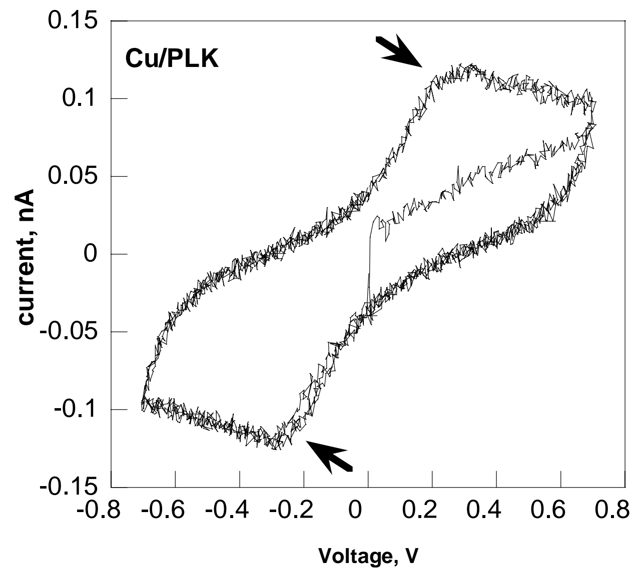


Figure 4.18 I-V curves, taken from single level comb structure Cu/25nmTa/PLK interconnect, show symmetric current peaks, suggesting defective barrier with equal defects density

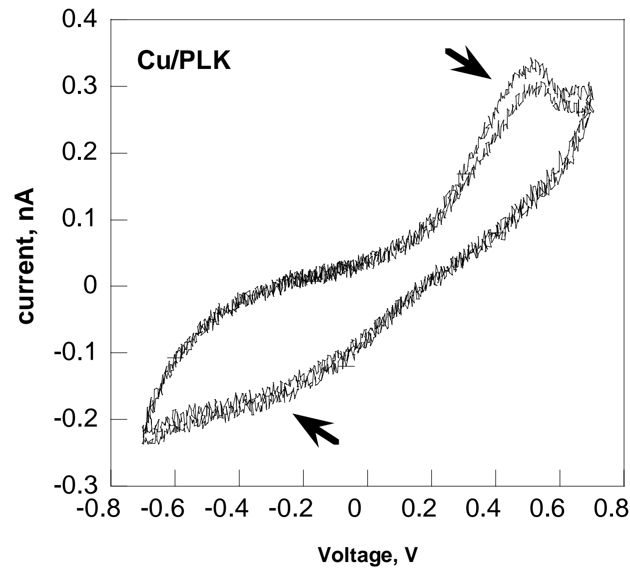


Figure 4.19 The I-V, taken from single level comb structure Cu/25nm/PLK interconnect, shows asymmetrical current peaks, suggesting that one barrier is more defective than the other.

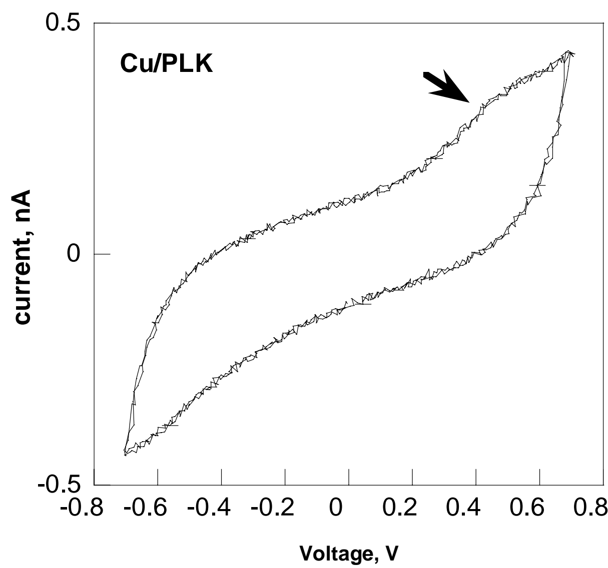


Figure 4.20 I-V, taken from single level comb structure Cu/25nmTa/PLK interconnect, shows a single peak for forward sweep, suggesting one intact and one defective barrier.

barrier on one interconnect and a defective barrier on the other one. Another example showing one intact barrier and one defective barrier is seen in figure 4.21. The data is taken from the comb/via chain Cu/10nmTa/DLK interconnect. The peak is much clearer in this case than that in figure 4.20, and may suggest that the defective barrier in this case has a higher defects density than that for the sample in figure 4.21.

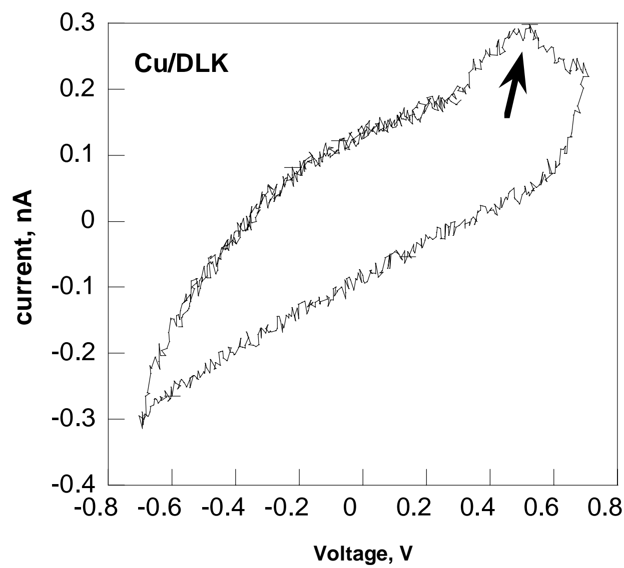
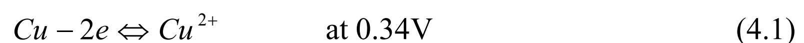


Figure 4.21 The I-V, taken from two level comb/via chain structure Cu/10nmTa/DLK interconnect, shows a single peak for forward sweep, suggesting one intact barrier and one defective barrier.

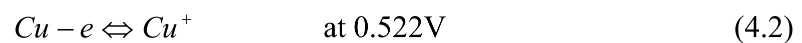
4.3 Reaction Mechanism of Cu in the Established System

4.3.1 Cu Reaction in the Established Cell

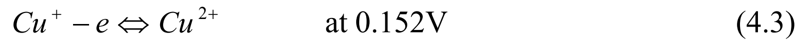
Theoretically, the Cu reaction can be treated as either a simple reaction (equation 4.1) or an elementary reaction (equations 4.2 and 4.3) [87-90].



$$Cu - 2e \Leftrightarrow Cu^{2+} \quad \text{at } 0.34\text{V} \qquad (4.1)$$



$$Cu - e \Leftrightarrow Cu^{+} \quad \text{at } 0.522\text{V} \qquad (4.2)$$



$$Cu^{+} - e \Leftrightarrow Cu^{2+} \qquad \text{at } 0.152\text{V} \qquad (4.3)$$

In a simple reaction, the Cu reaction occurs by a single step at a potential of 0.34V, and a stable Cu ion, Cu^{++}, is formed. However, a reaction consisting of a single elementary step alone is uncommon, and most reactions involve a number of elementary steps with reaction intermediates. According to Mattsson and Bockris [88], Cu reaction is likely to occur by two elementary steps: Cu/Cu^{+} at 0.522V and Cu^{+}/Cu^{++} at 0.152V. The first step reaction, Cu/Cu^{+}, occurs at a potential of 0.522V, and the intermediate cuprous ions, Cu^{+}, which are not completely unstable, tend to diffuse away from the electrode with positive polarity (where they decompose) because both concentration gradient and electrical field drive Cu^{+} to the electrode with negative polarity. Therefore, the second reaction Cu^{+}/Cu^{++} appears not to initiate on the same electrode once each Cu/Cu^{+} that occurs, but preferably occurs in the following sweep cycle when the voltage approaches 0.152V. The Cu^{+}/Cu^{++} reaction is inherently much slower than the Cu/Cu^{+} reaction, therefore it determines the overall reaction rate.

In our established system, Cu seems to experience both a simple and elementary reaction depending on the dielectric layer between the two electrodes. In the idealized samples for the fundamental study, two electrodes are spaced with air, i.e. no dielectric layer is present between them, and an elementary reaction occurs. The presence of double peaks in the idealized sample with symmetric Cu/Ta ratio provides the evidence. As is seen in figure 4.22-(b), which presents a half-cycle potential sweep (0V to 0.7V to 0V), the Cu oxidation reactions Cu^{+}/Cu^{++} and Cu/Cu^{+} occur at ~0.1V and ~0.47V respectively and produce two current peaks (point A and B) for up-ramp potential

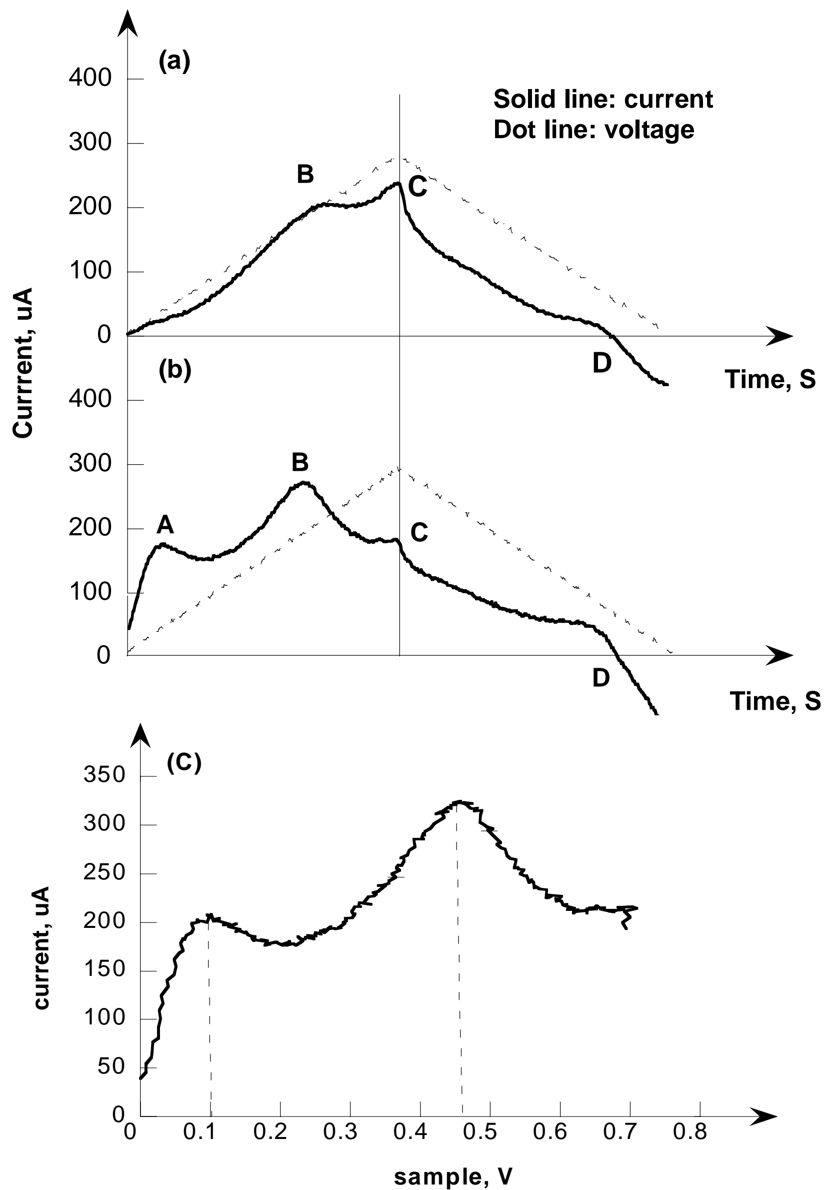


Figure 4.22 Plots of Cu redox reaction as a function of time and applied voltage (a) I/V-t curves for the first half-cycle (0V-0.7V-0V) potential sweep, (b) I/V-t curves for a half-cycle potential sweep (after the first cycle), (c) I-V curve for 0V-0.7V potential sweep

sweep (0-0.7V), corresponding to equations 4.2 and 4.3. It is noted that only one peak identified at ~0.47V is present for the first half-cycle sweep, as is seen in figure 4.22-(a). This is because the initial bulk solution does not contain any Cu^{+} and therefore only Cu/Cu^{+} occurs in the first sweep. The oxidation reaction of Cu^{+}/Cu^{++} is produced only after the first half-cycle, as seen in 4.22-(b). The shift of the potential of peaks from the standard oxidation potential may be because the reaction rate is faster than voltage sweep rate.

On the other hand, in the Cu/barrier/low κ integration system, Cu is likely to undergo a simple reaction, showing a single peak in I-V result. It seems that the presence of a low κ layer between the interconnects encourages a simple Cu reaction mechanism. In this situation, after the reaction Cu/Cu^{+}, a Cu^{+} appears not to diffuse away immediately from the electrode, and has a chance to have the reaction Cu^{+}/Cu^{++}, i.e. the reaction Cu^{+}/Cu^{++} is likely to be proportional to the reaction Cu/Cu^{+}. Therefore the Cu reaction is likely to be a simple reaction (Cu/Cu^{++}).

4.3.2 Cu Reaction in Two Aymmetric Electrodes

The study of Cu reaction mechanism in the established set-up provides a reasonable explanation for various types of I-V curves. In the case of symmetrically defective barriers, symmetric peaks are always observed in the I-V results for both idealized sample (double peak) and Cu/barrier/ low κ structure (single peak). This is because the two identical electrodes produce an equal amount of Cu redox reaction current and ionic charging current during each cycle, and therefore the same current intensity.

On the other hand, the I-Vs show quite different features for the case of asymmetrically defective barriers. It is found that not only asymmetric peaks are observed but also the reaction is dominated by different redox reactions on the two electrodes. The fundamental study for simulating the case of defective barriers with the mating electrodes containing asymmetric Cu/Ta ratios suggests that the reaction Cu^{+}/Cu^{++} is likely to be the dominant reaction for the electrode with small Cu fraction while the reaction Cu/Cu^{+} is likely to be the dominant reaction for the electrode with greater Cu fraction. This is because the amount of Cu/Cu^{+} is determined by availability of Cu atom, i.e. Cu fraction on Ta film while the reaction amount of Cu^{+}/Cu^{++} is determined by the availability of Cu^{+} ions, which are dispersed in the bulk solution and are likely to be shared by two electrodes. The availability of Cu^{+} ions is greater than that of Cu atoms near/on the electrode with small Cu fraction and the availability of Cu^{+} ions is less than that of Cu atom near/on the electrode with greater Cu fraction. As a result, the Cu^{+}/Cu^{++} peak at ~0.1V is dominant on the electrode with small Cu fraction while the peak Cu/Cu^{+} at ~0.47V is dominated on the electrode with big Cu fraction. It is noticed that the weaker peak on each electrode can still be seen if the difference of Cu fraction on two mating electrodes is small enough (figure 4.10) while they are nearly invisible if the difference of Cu fraction on two mating electrodes is large. (figure 4.11)

Asymmetry adds complexity to I-V data analysis, especially in the Cu/barrier/ low κ integration system, but it also suggests the possibility of identifying the electrode barrier with higher defect density. Such information may help identify the problem and help to improve the barrier quality. It is our belief that a kinetic interplay among ion drift, reaction

and geometry produces such complexity. When the defects density on two mating electrodes is not equal, the availability of reaction sites is also asymmetrical, and the number of cations produced or reduced will be unequal at the two electrodes. The unequal but intact Ta area also provides a differing polarization voltage, contributing to ion drift unequally.

4.4 Significance and Consideration

The proposed voltammetry-based method for evaluating diffusion barriers has proven simple, fast and effective. Instead of only examining a very local area by intensive TEM observation after lengthy electrical tests at elevated temperature, this method 'observes' the whole diffusion barrier in the test pattern within a few hours to days. Furthermore, the effectiveness of the method is found not to be limited to the detection of barrier defects, it also has potentials to be a characterization technique in other areas of IC industry, for example, the integrity of capping layer, the integrity of pore sealing, the ionic contamination in package substrate, etc.

4.4.1 Considerations for Industry Application

The cyclic voltammetry method is very effective in detecting the presence of barrier defects, however, the lack of quantification capability retards the further application of the method. Ideally, the defect density in diffusion barrier can be quantified based on the intensity of peak current since it is proportional to the defect density (figure 4.9), however, such quantification in real interconnects is very difficult due to the complicated structure of Cu/barrier/ low κ integration. Therefore, a model as well as the reference test pattern is required to make the quantification possible.

In addition, infiltration is the prerequisite for the application of the voltammetry method. Therefore, it is critical to infiltrate the electrolyte without any difficulty for successfully application of the method. Although our investigation reveals that both PLK and DLK can be infiltrated with electrolyte solution, a test pattern particularly designed for the voltammetry method will improve infiltration of the electrolyte, especially for the patterns with extremely small geometry.

Furthermore, as a new technique, few references can be used to assist full understanding of the method in the complicated Cu/barrier/low κ integration system. Knowledge and experience are needed to explain the data accurately, which restricts the method from a broad application. Therefore, lots of work needs to be done to make the method a standard characterization technique for industrial application.

4.4.2 The Potential Applications

4.4.2.1 Evaluation of Capping Layer Integrity

With the aggressive miniaturization of devices, the capping layer is becoming thinner, yet still subjected to stress during chemical mechnical polish (CMP) processes. This creates the concern for the integrity of capping layer, and currently there is no very effective way to detect the problem in the capping layer in the as-processed condition.

The voltammetry method for detecting barrier defects has the capability of detecting the integrity of the capping layer. A full investigation is being conducted in our lab, but the feasibility study has already been conducted on two-level Cu interconnects structures processed by Texas Instruments. The test pattern, as seen in figure 4.23b, has a comb structure for the bottom Cu (M1) spaced by low κ material and

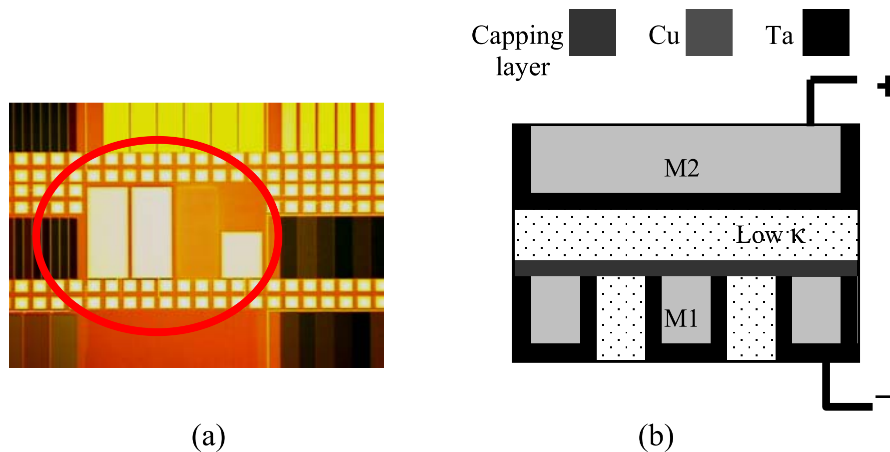


Figure 4.23 An optical image of capping layer test pattern and its schematic representative cross section. Note both M1 and M2 are Cu

a plate for the top Cu (M2). The capping layer consists of 0-60nm SiCN/0-60nm SiCO and is patterned on the top of M1, following a low κ material and M2.

Similar to the detection of barrier detects, the integrity of capping layer is evaluated by monitoring the current in the established cell under cyclic voltage. In this case, the M2 plate and M1 comb act as two electrodes and D I water containing 2%wt KCl is infiltrated into the structure. If the capping layer is intact, the electrolyte solution can not penetrate through it. In this case, even when the electrolyte is fully loaded within all the low κ layer, the capping layer serving as an insulator opens the overall circuit, and therefore, no current is flowing when applying a voltage, as is seen in figure 4.24. On the other hand, if the capping layer is defective, electrolyte is able to connect through it, and an electrolytic cell is established when a voltage is applied. Consequently, the presence of current signal indicates a capping layer is broken.

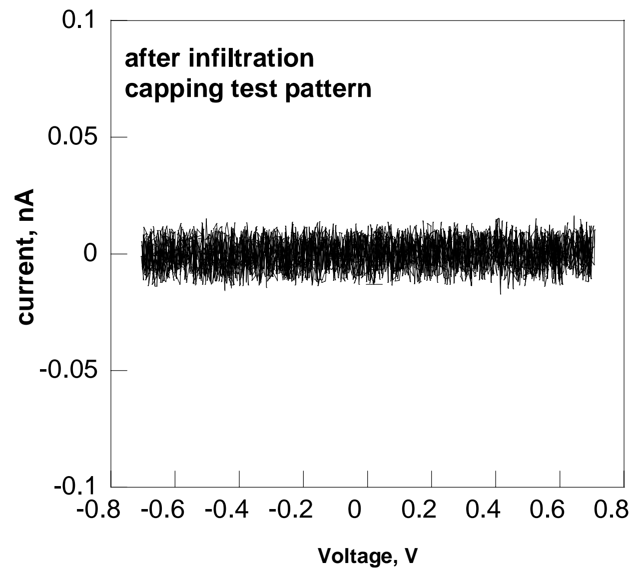


Figure 4.24 A representative I-V, taken from the samples after immersed into electrolyte solution, does not show any current signal, suggesting an intact capping layer

Figures 4.25 and 4.26 present two examples of defective capping layers. The hysteresis I-V in figure 4.25 suggests the current is likely to be produced by electrolyte ion drifting under an electrical field. The presence of current peak in figure 4.26 indicates that Cu is exposed to the electrolyte and produces a reaction current. We believe that either the capping layer right on the top of M1 or/and the bottom barrier layer of M2 is broke in this case.

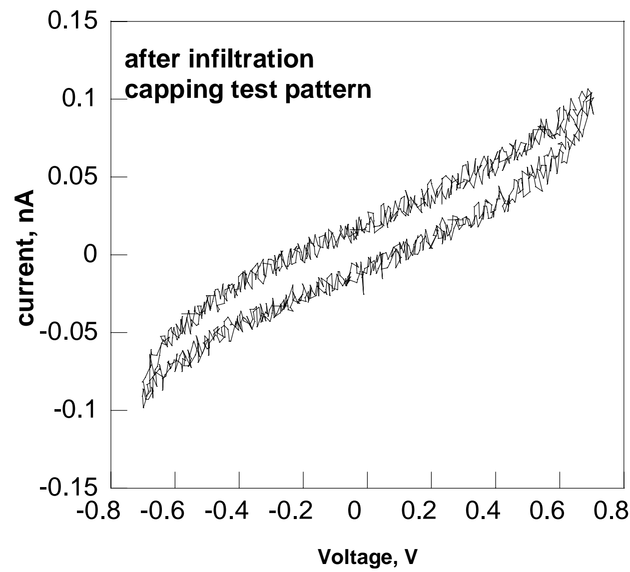


Figure 4.25 A representative I-V shows a simple hysteresis, suggesting a defective capping layer.

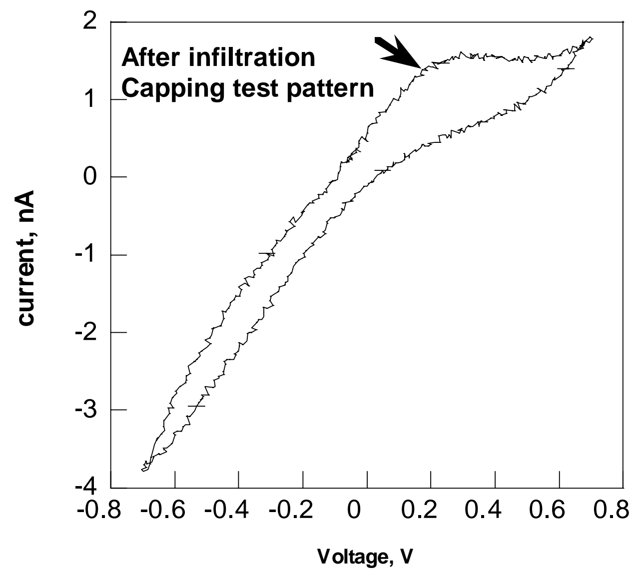


Figure 4.26 An example of a defective capping layer shows a current peak

4.4.2.2 Evaluation of Pore-Seal Integrity

As discussed in 1.2.3.2, low κ materials with high degree of porosity are needed for advanced IC devices. However, aside from degrading the intrinsic properties of materials, highly interconnected pore networks enable the infiltration of contaminants from processing/ambient gases and liquids, and seriously degrade the device performance. For this reason, a pore seal is incorporated to protect low κ structures from contamination. The pore seal also requires a fast and effective method to detect its integrity, and we recommend the voltammetry method. As in the case of capping layer, when a pore seal is intact, the electrolyte is not electrically connected with the electrode, and therefore no current is flowing in the structure. On the other hand, when pore seal is not intact, the electrolyte can be infiltrated in the structure forming an electrochemical cell, and current signal will be detected.

4.4.2.3 Evaluation of Ionic Contamination for Package Substrate

Ionic contamination is a serious reliability concern for non-hermetically sealed IC package because the contaminants on the substrate, mostly Cl^- and Na^+, cause Cu leads corrosion and migration in the presence of moisture, and thereby facilitate either open or short circuit failure. Currently, secondary ion microscopy spectroscopy (SIMS) is used to characterize the contaminant ions after highly accelerated stress testing (HAST). Even though it is costly and time-consuming, this method is not able to quantify the contaminants level. The voltammetry method has a potential to characterize as well as quantify ionic contaminants without the need for accelerated conditions. In this case, an electrolytic cell is established by Cu leads on the substrate and infiltrated D

I water or electrolyte ion infiltrated. When a substrate does not have any ionic contamination, no current flows with the applied voltage because neither ionic current nor reaction is produced. When a substrate has ionic contaminants that do not react with Cu, ionic current is produced. When a substrate has ionic contaminants that do react with Cu, reaction current is produced. Therefore, by monitoring the I-V profile, the presence of contamination ions can be detected. Also, it is possible to distinguish the types of contaminants. Moreover, it has a potential to quantify the contaminants based on the current intensity since it is dependent on the drift and/or reaction of contaminants.

4.5 Summary

A cyclic voltammetry-based methodology is developed to characterize the barrier defects in Cu/barrier/low κ interconnect structures in this chapter. In the method, an electrolytic cell is established in the interconnect structure: two Cu/barrier interconnects act as two electrodes while dilute KCl solution is introduced into the low κ layer acts as an electrolyte. The condition of the diffusion barrier can be detected by a measurement of current resulting from the applied voltage. A fundamental study is implemented by simulating possible barrier conditions using idealized samples, and the results provide the references to properly explain the data resulting from the real Cu interconnect structure.

Generally, a symmetric hysteresis I-V suggests an intact barrier while the presence of current peaks in an I-V curve suggests a defective barrier. Regarding a defective barrier, symmetric peaks suggest that two Cu/barrier interconnects are

defective with equal defect density while asymmetric peaks suggest that one barrier is more defective than the other. The barrier with more defect density can be identified by the dominant Cu reaction. In addition, an asymmetric hysteresis with the absence of peaks, may suggest one intact barrier and one defective barrier. However, one has to take considerable care to analyze the data with an asymmetric hysteresis because it could be produced by the complicated geometry.

An intensive investigation on real interconnects reveals the voltammetry-based method is simple, fast and accurate for detecting the presence of defects in the whole diffusion barrier in Cu/barrier/low κ interconnect structures, and has the potential for quantifying the defect density. In addition, the method has a potential to evaluate the integrity of capping layer, pore seal in the interconnect structures and contamination in package substrate.

CHAPTER 5

CHARACTERIZATION AND INVESTIGATION OF THERMAL STABILITY FOR LOW-κ STRUCTURE USING VOLTAMMETRY

Although several techniques with high cost and complex modeling are available for characterizing pore structures in thin film, such as PALS, SXR, SAXN, etc[67-70] discussed in 1.2.3.2, they are all effective only for blanket films, and not able to trace the stability of low κ structure for as-processed interconnect structure. However, low κ structure is found to suffer structure instability during thermal annealing, and small change in the structure may degrade device performance. For example, local coarsening of pore structure further degrades mechanical properties of low κ material and increase the chance for contaminant infiltration. Therefore, in order to understand the impact of the structure instability of low κ material on the product reliability and optimize the design and processing, it is imperative to have an effective characterization method to characterize low κ structure and trace its stability for as-processed wafer.

In this chapter, low κ structure and thermal stability in fully processed interconnect structures are characterized by measuring effective diffusivity of electrolyte ion infiltrated into low κ layer. The results provide sufficient evidence that the method is very effective in characterizing and tracing low κ structure both in DLK and PLK materials because the diffusivity is strongly affected by pore size, porosity, pore interconnectivity, etc.

5.1 Development of Characterization Technique

5.1.1 Samples and Test Conditions

The three groups of samples used in this study are basically the same as the samples used for barrier detection in chapter 4. However, the condition of the dielectric materials between two electrodes, instead of the barrier condition, will be the subject to be investigated in this chapter using step-mode voltammetry. As a brief description of the samples from the angle of the dielectrics between the interconnects is given here. The first group is used to examine the accuracy of the diffusivity measurements by comparing the ion diffusivity obtained in the bulk solution with other published diffusivity data. The samples in this group consist of a pair of identical Si/SiO_2 plate electrodes coated with 2000Å Ta, separated by a ~1mm spacer. Note that no dielectric layer is present between two electrodes. The second and third groups are used to investigate the sensitivity and effectiveness of diffusivity measurements on characterizing the low κ structure. The samples in both groups are single level Cu interconnect comb structures, with the primary difference between them being the low κ material. In the second group (PLK), processed at SEMATECH, the low-κ layer is MSQ-based PLK (κ~2.2) having a porosity of ~45% with a known average pore size of ~2nm. The third group (DLK) has a higher κ value (κ-2.9) and is believed to have a closed pore structure with less than 10% porosity. The standard comb structure test patterns, consisting of 0.125~0.14 μm wide Cu spaced 0.13~0.35μm apart, are cleaved and immersed in a 2wt.% KCl electrolyte solution to reach complete infiltration. Cyclic voltammetry is used to select the samples without barrier defects, and then the

discharging current is measured with a pico-ammeter after charging at 0.7V. In all tests, a 4 minutes period is used for monitoring restoration current.

5.1.2 Current Profile in the Step Voltommety Method

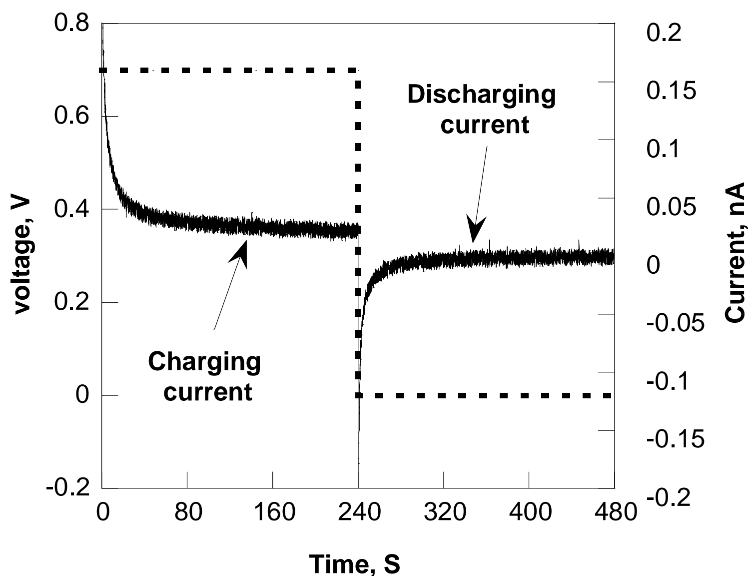


Figure 5.1 Current as a function of time under double step voltage sweep taken from single level 0.25μm Cu/PLK interconnects with 0.30μm space

Figure 5.1 presents the typical data of current as a function of time for a single level 0.25μm Cu/PLK pattern with 0.30μm space. When an external potential (V=0.7V) is applied, initially, a great current is created by ion drifting under the applied voltage, and then declines with time due to depletion of electrolyte ion in bulk solution. The non-zero current value is attributed to leakage current through low κ materials. This process is termed as charging and the corresponding current is termed as charging current. When the applied voltage is removed abruptly after the electrolyte ion is fully stored at the electrodes, the current is produced as a result of electrolyte ions diffusion

down concentration gradient to restore the chemical equilibrium in the system. This is termed as discharging process, and the corresponding current is termed as discharging current. The discharging current is of an initial high value and then decays to zero as the chemical equilibrium is reached in the bulk solution.

5.1.2.1 Charging vs. Discharging Current

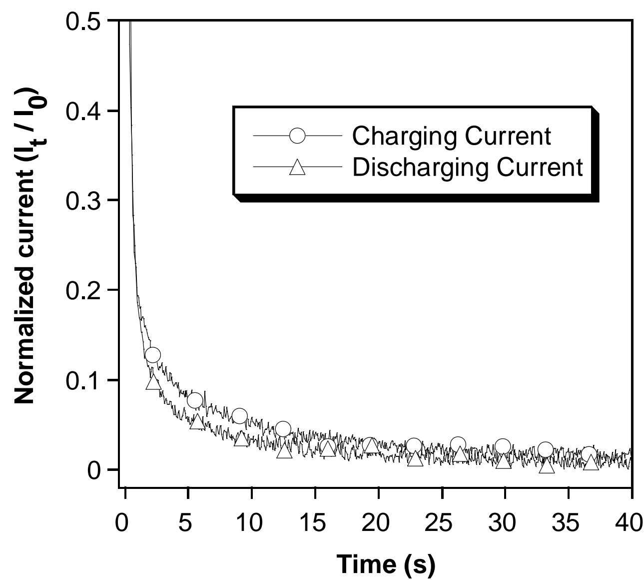


Figure 5.2 A comparasion of current decay during charging and discharging process, taken from single level 0.25μm Cu/PLK interconnects with 0.30μm space

When the charging and discharging current in figure 5.1 are plotted in the same time period after subtracting the leakage current in charging process, the charging and discharging current can be compared as a function of time in figure 5.2. As is seen, the current decay in the discharging process is faster than that in the charging process, and this is seen in all three groups of samples tested at the same voltage. The result can be

attributed to the different ion migration mechanism between charging and discharging process in an electrochemical cell.

Theoretically, the current in an electrolytic cell consists of migration (resulting from applied voltage), diffusion and convection, as mentioned in 3.2.2. Therefore, if the convection current is ignored, the charging current is a combined result of migration and diffusion while discharging current is a result of diffusion only.

Figure 5.3 presents the normalized discharging current after various charging voltages as a function of time for single level 0.25μm Cu/PLK interconnects with 0.30μm space. As is seen, the decay of current in the discharging process is independent of the applied voltage except for the initial current value. Therefore, discharging current is likely to be a result of ion diffusion only.

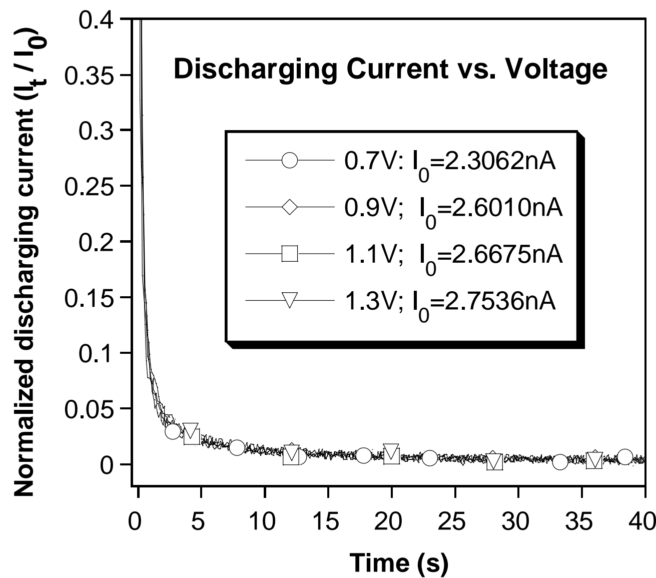


Figure 5.3 The impact of applied voltage on discharging current, taken from 0.175μm single level Cu/PLK interconnects with 0.175μm space. The initial current values responding to various voltages are given in the plot

On the other hand, the decay rate of current during the charging process is likely to be controlled by both the applied voltage and the ion diffusion. As is seen in figure 5.4, which presents the normalized charging current under various voltages as a function of time for single level 0.25μm Cu/PLK interconnects with 0.30μm space. The applied voltage not only changes the initial current value but also the profile of the current during charging process. In this work, the study of the step voltammetry method for low κ structure characterization will only focus on the discharging process to investigate the accuracy and effectiveness of the method for characterization of low κ structure.

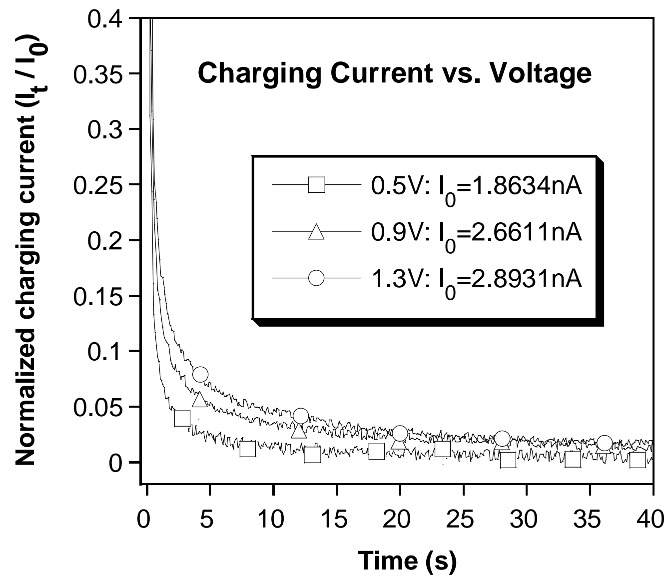


Figure 5.4 The impact of applied voltage on charging current, taken from 0.25μm single level Cu/PLK interconnects with 0.30μm space. The initial current values responding to various voltages are given in the plot

5.1.2.2 Discharging Current vs. Porosity

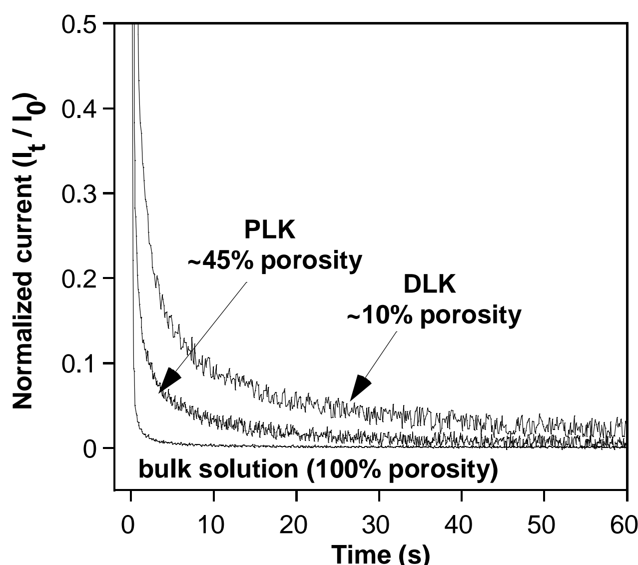


Figure 5.5 Normalized discharging current as a function of time measured at 25°C for three different sample groups. For clarity, the high current spike is truncated. Note also that the all cell currents diminish to zero at the long time limit.

The study of the voltage effect on the responding current suggests that the discharging current is driven by the effective diffusivity of electrolyte ion, which is strongly affected by the condition of dielectric layer. This is confirmed by the investigation of discharging current on three groups of samples with varying low κ dielectric conditions, as is seen in figure 5.5, which presents the representative normalized discharging current data as a function of time for three groups. The decay of the current is fastest in the bulk solution which has a 100% porosity (no dielectric layer in between); slowest in DLK material which has the smallest porosity (<10%) with a closed pore network, and in-between in PLK material which has a porosity of ~45% with an average pore size of 2nm and an interconnected pore network. This result

indicates that the discharging current is very sensitive to low κ structure including porosity, pore size, pore interconnectivity, etc.

5.1.3 Analytic Model for Discharging Current

5.1.3.1 Concentration Profile of Ions During Discharging Process

In order to yield the effective diffusivity of electrolyte ions, a simple model is established to model the ion diffusion. By fitting the experimental current vs. time data to an analytic equation produced by the model, the effective diffusivity of electrolyte ion can be extracted.

In the case of the defect-free barrier, the discharging current can be predicted by solving Fick's second law, which gives the time variation of surface charge density at each electrode.

$$\frac{\partial C(x,t)}{\partial t} = D\frac{d^2C(x,t)}{dx^2} \qquad (5.1)$$

where D is diffusivity and C is the concentration of ions in the electrolyte solution. Here, *D* is assumed to be independent of the concentration, which is true in a dilute solution. In reality, there are two diffusing species to consider, anions and cations. Because their migration is equal and opposite in direction, they create an equal contribution to the cell current with the diffusion limited by the slowest specie. In the case of KCl aqueous solution, the diffusivity of K^+ (1.957×10^{-5}cm^2/s) and Cl^- (2.032×10^{-5}cm^2/s) are the limited factors compared to H^++ (9.312×10^{-5}cm^2/s)and OH^-(5.273×10^{-5}cm^2/s) Thus, we can simplify, without loss of accuracy, by solving equation 5.1 for either K^+ or Cl^- [91-93], and consider this half the current.

The defect-free barrier provides an impermeable, non-reacting boundary for electrolyte ion, therefore a zero flux condition at each electrode surface is created, as seen in equations 5.2

$$J(0,t) = (\frac{dC}{dx})_{x=0} = 0 \tag{5.2a}$$

$$J(l,t) = (\frac{dC}{dx})_{x=l} = 0 \tag{5.2b}$$

The initial condition of discharging current is determined from the stationary profile of the charging process. Therefore, the final concentration profile of the charging current has to be discussed. The flux equation during charging is given by

$$J(x,t) = -D\frac{dC}{dx} + vC \tag{5.3}$$

where ν is the anion drift velocity resulting from the externally applied voltage.

At t = ∞, the flux becomes zero and thus the concentration profile becomes

$$C(x,\infty) = M\exp(\frac{vx}{D}) \tag{5.4}$$

where integration constant M is given by

$$M = C_0[\frac{D}{vl}(\exp(\frac{vl}{D}) - 1)]^{-1}.$$

and the initial condition of the discharging current is given by equation (4):

$$C(x,0) = C_0[\frac{D}{vl}(\exp(\frac{vl}{D}) - 1)]^{-1}\exp(\frac{vx}{D}) \tag{5.5}$$

where C_0 represents the initial concentration of ions before application of the bias, and l is the space between two electrodes.

The solution of the second order partial differential equation with the given boundary and initial conditions is a classical diffusion problem, which is presented in many places and described in Appendix B [94-95]. But the final solution of concentration profile is given by equation 5.6

$$C(x,t) = C_0 + \frac{2M}{l}\sum_{n=1}^{\infty}\exp\left(-(\frac{n\pi}{l})^2 Dt\right)\left(\frac{(\frac{v}{D})[(-1)^n \exp(\frac{vl}{D}) - 1]}{(\frac{n\pi}{l})^2 + (\frac{v}{D})^2}\right)\cos(\frac{n\pi x}{l}) \qquad (5.6)$$

5.1.3.2. The Solution of Discharging Current

The behavior of the circuit here is analogous to that of a capacitor, and the discharging current can be calculated from the difference in the time variation of ions concentration at two electrodes, that is

$$j(t) = \frac{dQ_t}{dt} \qquad (5.7)$$

where Q_t represents the total charge accumulated (deviation from equilibrium), and it is determined by the net concentration change of ions with time:

$$j(t) = \frac{d}{dt}(C(0,t) - C(l,t)) = \frac{dC(0,t)}{dt} - \frac{dC(l,t)}{dt} \qquad (5.8)$$

The simplified solution of equation 5.8 is obtained by applying the normalized current, *j(t)/j(0)*, and the detail is described in Appendix C.

$$j_n(t) = \frac{j(t)}{j(0)} = \sum_{n=1}^{\infty} B_n \exp\left(-\frac{n^2\pi^2}{l^2}Dt\right) \quad \text{(n=1, 3, 5, 7…)} \qquad (5.9)$$

where B_n is a constant for integration and normalization. Equation 5.9 indicates that the discharging current decreases exponentially with time consisting with the experiment

data seen in figure 5.1~5.5, with kinetics determined by the diffusivity *D* and the low-κ layer width *l*.

The solution of discharging current (equation 5.9) is found to fit the experimental data very well, as seen in figure 5.6, which presents the experimental discharging current data taken from Cu/DLK interconnect and its best fit curve.

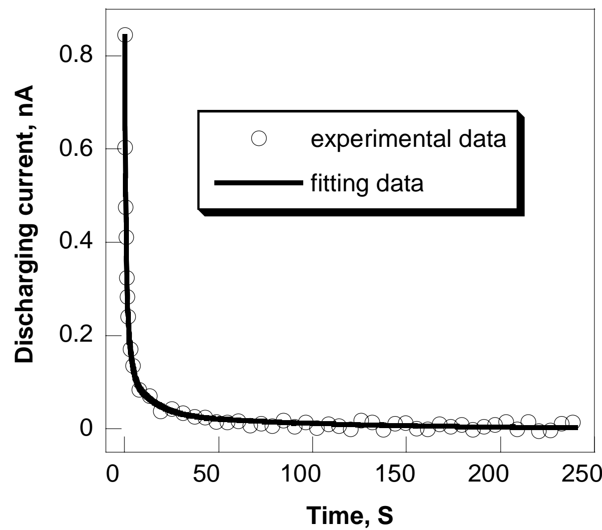


Figure 5.6 Discharging current is taken from Cu/DLK, and its fitting data

5.2 Characterization of Low κ Structure

5.2.1 Effective Diffusivity of Electrolyte Ion

The data from all three groups are found to fit exceptionally well to the model equation 5.9, as seen in figure 5.7, which present the experimental data and the best fit for the samples in figure 5.3. In the figure, the current is referenced to the initial value and plotted as the relative discharging current I(t)/I(0), and the high current spike is truncated for clarity.

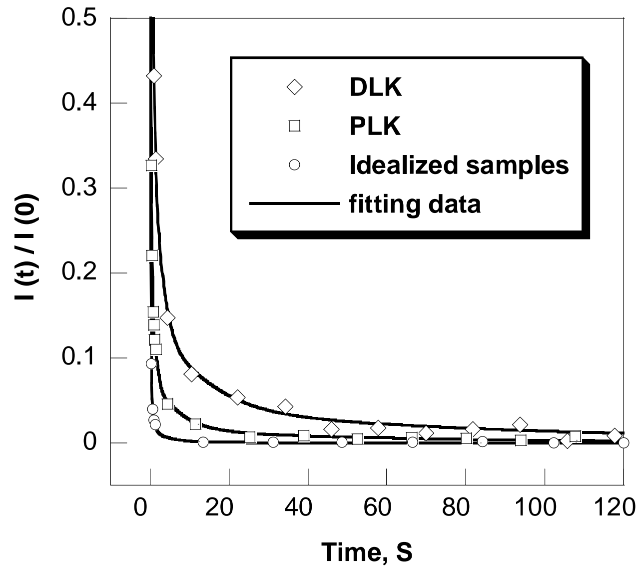


Figure 5.7 Discharging current as a function of time with varying porosity of dielectrics between two mating electrodes: Group 1 is Cu/DLK with ~10% porosity; Group 2 is Cu/PLK with ~45% porosity and group 3 is idealized sample with 100% porosity

Table 5.1 The effective ion diffusivity of three groups of samples

Sample	Effective ion diffusivity (cm^2/s)
Bulk solution	3.151×10^{-5}
PLK	3.264×10^{-13}
DLK	1.322×10^{-13}

Using the solution of the discharging current (equation 5.9), the effective ion diffusivity can be extracted by the formula of the best fit curve. Table 5.1 gives the effective ion diffusivity of three groups determined by the developed model. Note that 10-25 samples are tested for each condition, allowing confident determination of the diffusivity. As is seen in table, the diffusivity in the PLK (group 2) is more than 7

orders of magnitude lower than that in the bulk solution (group 1) and 2.5 times higher than that in dense low κ (group 3), indicating that the ion diffusivity is strongly dependent on the condition of dielectrics between two electrodes, which consists with the results of experimental data.

5.2.2 Ion Diffusion Mechanism

When the ion diffusivity is plotted as a function of reciprocal of test temperature (T), as seen in figure 5.8, the activation energy of ion diffusion can be obtained by the slope of the exceptional fit curve. Table 5.2 summarizes the ion diffusivity values tested at three different temperatures, 25, 45, and 65°C and the activation energy of ion diffusion of the three groups of samples, and the results present several interesting and noteworthy facts.

Table 5.2 Effective diffusivity of electrolyte ions measured at three different temperatures.

Sample	Effective ion diffusivity (cm^2/s)			E_a (eV)
	25C	45C	65C	
Reference [98,99]	$1.920 x 10^{-5}$	$2.983 x 10^{-5}$	$4.484 x 10^{-5}$	0.18
Bulk solution (100% porosity)	$3.151 x 10^{-5}$	$5.241 x 10^{-5}$	$7.381 x 10^{-5}$	0.18
PLK (~45% porosity)	$3.264 x 10^{-13}$	$5.241 x 10^{-13}$	$7.935 x 10^{-13}$	0.19
DLK(~10% porosity)	$1.322 x 10^{-13}$	$3.570 x 10^{-13}$	$5.546 x 10^{-13}$	0.31

The fact is that this method yields data that is in good agreement with the available reference [96-99]. In spite of fundamental differences in measurement methods, the bulk diffusivity values are in close proximity and the activation energy is

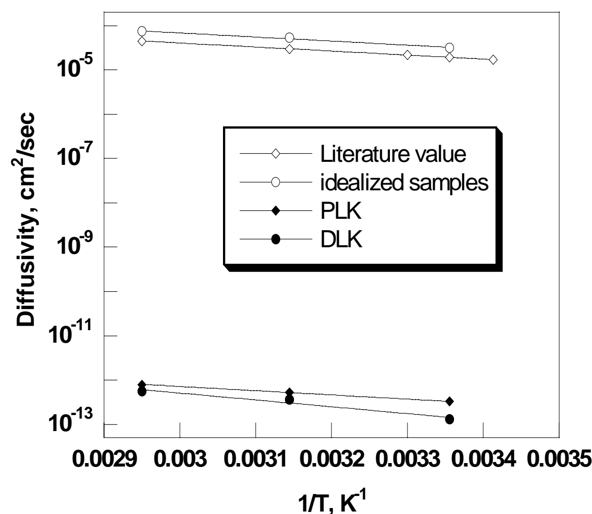


Figure 5.8 Diffusivities of ions as a function of reciprocal temperature

identical, 0.18eV. Notice also that activation energy exhibits a similar value (0.19eV) with that in the bulk solution (0.18eV), although the diffusivity in PLK (group 2) is more than 7 orders of magnitude lower than those in the bulk solution. This result is consistent with current understanding of molecule/ion diffusion mechanisms in porous media where diffusion takes place through pores that are filled with water molecules. The ion effective diffusivity in a porous media is a function of reciprocal tortuosity, which is a geometric parameter of void space, or what might be referred to as the pore morphology and used to describe the longer connecting path imposed by obstacles within porous solid relative to that for motion in unconstrained free space [100-101]. In such a case, the tortuosity of the diffusion path through the pore network reduces the measured diffusivity from that of the bulk solution, while its activation energy is unaffected. Furthermore, the results from group 3 suggest that the ion diffusivity in

dense low κ dielectric is further reduced. In this case the large intramolecular space in the dense low κ is believe to act like a network of small interconnected pores and provide a diffusion path sufficiently large to allow migration of small molecules and ions. However, with its closed pore structure, the diffusion of ion, not to mention the electrolyte infiltration itself, is not likely occur in dense low-κ unless the open space in the bond network provides an alternate diffusion path. The fact that the activation energy of the diffusivity is significantly higher in dense low κ, 0.31eV, may be because the intramolecular space is not entirely free from molecular bond force.

5.3 Investigation of Structure Stability for PLK Materials

With the availability of this simple yet sensitive porosity characterization method, numerous investigations are possible. While many such studies are underway in our laboratories, the first finding is that pore structure in PLK changes in fully fabricated interconnects after additional moderate annealing.

5.3.1 Samples and Test Conditions

The samples used in this investigation are the second group of samples: single level Cu interconnects of comb structures integrated with PLK layer having a porosity of ~45% with a known average pore size of 2nm. The comb structures here have identical 0.25μm Cu interconnect patterns, but with different low-κ spacing, 0.20 and 0.35μm.

The samples are baked at different temperature, 250°C, 300°C, 350°C and 400°C , in N_2 for 1 hrs, and then the comb structure test patterns are cut and immersed in a 2 wt.% KCl electrolyte solution to reach complete infiltration. Then the

characterization test is conducted at 25°C after the samples with barrier defect-free are selected using cyclic voltammetry. In order to obtain the reliable diffusivity data, more than 10 samples are tested at each condition.

5.3.2 Results and Discussion

Figure 5.9 shows the diffusivities of two comb patterns with PLK material after annealing at various temperatures in N_2 for 1 hr. As seen in the figure, the diffusivities do not remain constant but change with annealing temperature. More interestingly, the direction of the change is pitch dependent, with diffusivity decreasing for the 0.25/0.20 pattern but increasing for the 0.25/0.35 pattern. While the details behind such a

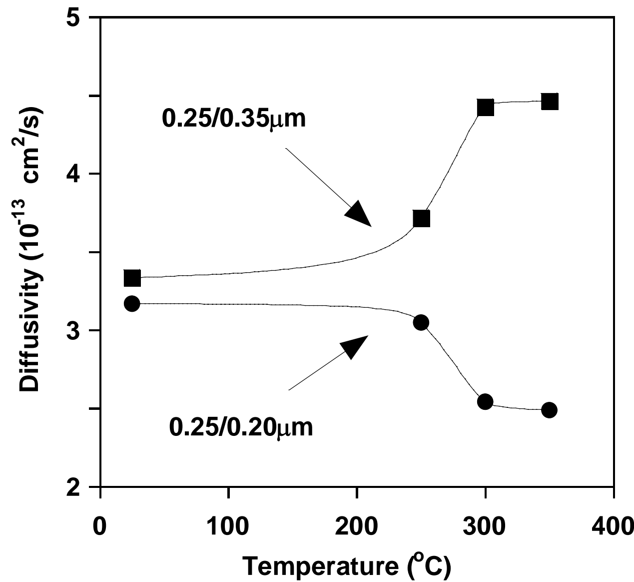


Figure 5.9 Diffusivity in PLK as a function of the annealing temperature. Circles represent comb structure patterns of 0.25μm Cu line and 0.20μm low κ spacing, while squares represent those with 0.35μm low κ.

dramatic difference need to be further investigated, we attribute the results to two competing instability mechanisms: collapse and coarsening of the pores.

During thermal annealing, PLK structure is subjected compressive stress due to a mismatch of coefficient of thermal expansion (CTE) mismatch among the materials in the interconnect structure. It is known that the CTE of MSQ-based PLK (20.0ppm/°C) is much higher than Ta (6.5 ppm/°C) while the modulus of MSQ based PLK (6.3GPa) is much lower than Ta (185.7GPa) [77]. As a result, the PLK material is subjected to a great compressive stress created by confinement of Ta. This compressive stress collapses the pores in PLK and condenses the PLK structure during thermal annealing, resulting in a more closed structure compared to the structure before annealing. Consequently, the effective ion diffusivity is reduced since ions have to travel a longer path in a more closed structure. As is found in 5.2, the effective diffusivity of electrolyte ion is lower in DLK structure than that in PLK structure. On the other hand, thermal heating tends to coarse pore structure of PLK, which opens more diffusion path by increasing spaces or interconnectivity of pores, and consequently increase the effective ion diffusivity in the PLK structure. The result presented in figure 5.9 suggests that the two factors competes each other during thermal annealing. The compressive stress is the dominant factor for small patterns (0.25/0.20 patter) because the confinement effect of Ta is stronger in a small pattern, and PLK material has less room to expand. As a result, the pores in PLK are partially closed by the compressive stress, causing the decrease of diffusivity. On the other hand, when the space between interconnects increases, the PLK material has more room to expand due to the less confinement of Ta. Therefore the

impact of compressive stress is reduced in big patterns (0.25/0.35 pattern), and coarsening becomes the dominant factor, causing the increase of diffusivity. Although the pitch dependence of low κ stress state is expected [77,102] and pore structure change during pattern processing has been postulated, the divergent but measurable changes in diffusivity over a small pitch range have implications beyond physical reliability, perhaps to include a non uniform κ value throughout a chip.

5.4 Significance and Consideration

The step voltammetry method is proven to be a very effective method for characterizing low κ structures. The good agreement of the diffusivity and activation energy data resulted from bulk solution with other published work indicates that the method is an accurate method. In addition, the different diffusivities of electrolyte ion in samples with varying porosity suggests that ion diffusivity is very sensitive to the low κ structure, revealing that the method is an effective method to characterize low κ structures. The application of the method to investigate the pore structure stability further suggests that the method is also effective in tracing the structural stability of PLK. As is well known, low κ structure is the weak part in the Cu/ low κ integration, and any change in its structure may cause a big reliability issue. Therefore, the capability of the method for tracing the structure stability makes the technique worthy of effort for further development. Our lab is putting much effort into making the method fully mature, such as, development of a model as well as references for determining the actual porosity, pore size and distribution. In addition, the evidence of the change of pores in low-κ structure with annealing suggests additional work is needed to be able to

predict and accommodate change in the pore structure during interconnect processing and packaging operations.

5.5 Summary

A step-mode voltammetry method is used to characterize pore structure in both dense and porous low low κ in patterned interconnect structures using a measurement of ion diffusivity. It produces the identical activation energy and diffusivity results in good agreement with references in bulk solution. The ion diffusivity in porous low-κ is found to be 7 orders magnitude lower than in the bulk solution while exhibiting a similar activation energy. This result is consistent with current theory of diffusion through a porous network, and the reduction of the ions diffusivity is attributed to the tortuosity of the diffusion path through the pore network. The higher diffusivity and significantly higher activation energy in dense low k suggest that the large intramolecular space in the dense low κ, acting like a network of small interconnected pores, provides a diffusion path sufficiently large to allow migration of small molecules and ions, however, the diffusion of ions is not likely occur in dense low κ unless the open space in the bond network provides an alternate diffusion path due to its closed pore structure.

The application of the method reveals that the pore structure in a patterned interconnect is not stable but undergoes measurable change resulting from two competing processes: the collapse of pores created by compressive stress due to the different thermal expansion among materials in the interconnect structure and the coarsening of the pores due to heating. The collapse of pores reduces the diffusivity

value and is dominant in the patterns with small pitch, while the coarsening of the pores increases the diffusivity value and is dominant in the patterns with large pitch.

CHAPTER 6

CONCLUSIONS AND FUTURE WORK

6.1 Conclusions

The application of Cu/low κ interconnects in future IC devices creates serious reliability and characterization metrology concerns. In this study, an investigation of Cu/PLK interconnects indicates that Cu interconnects fail simply by thermal baking, which also raisess questions about the effectiveness of conventional characterization techniques. Therefore, a voltammetry-based characterization method is developed, and the method is proven to meet the needs for detecting barrier defects and characterizing low κ structure and stability on fully executed interconnect structures.

6.1.1 Thermal Failure of Cu/PLK Integration

The study on thermal stability of Cu/PLK interconnects reveals that the interconnect fails by Cu out-diffusion through the defects in the diffusion barrier into the PLK structure during thermal baking. The out-diffusion is found to be driven by oxidation potential (if abundant oxidants are present in the pores of PLK) and stress gradient created by a mismatch of CTE in the interconnect structure. Such failure is considered to be highly dependent on the integrity of diffusion barrier and the presence of pores in low κ materials. A tiny pre-existing defect can be developed during thermal baking providing a diffusion channel, and then a highly interconnected pore network in

PLK materials provides sufficient room for Cu to reside without concern about creating back stress. However, such defects are not successfully detected by the TEM observation due to their small and localized nature. In addition, the interconnected pore structure is proven to be less resistant against contaminants infiltration, which can initiate thermal instability factors, such as oxidation potential, and accelerate the interconnect failure. Therefore, it is essential to develop a characterization technique to evaluate both diffusion barrier quality and the low κ structure for as-processed wafer.

6.1.2 Characterization Technique: Voltammetry-based Method

A voltammerty-based method is developed in this work to characterize the integrity of diffusion barriers and the pores structure in low κ materials. The method has been proven to be able to accurately detect defects in the diffusion barriers of an entire test pattern in a few hours or days. Meanwhile, it has the capability to characterize low κ structure, and application of the method indicates that pore structure in fully processed Cu/low κ interconnects suffers structure instability during thermal annealing.

6.1.2.1 Evaluation of Defects in Diffusion Barrier

A cyclic voltammetry-based method is developed to characterize defects in the diffusion barrier by monitoring the current resulting from an applied voltage after an electrolyte is infiltrated into the pattern. The evaluation is performed based on the fundamental study which simulates various possible barrier conditions using idealized samples. In general, a simple hysteresis I-V suggests an intact (defect-free) barrier while the presence of current peaks in the I-V curve indicates a defective barrier. Instead of examining a few local areas using TEM after lengthy electrical stressing tests, the

method is able to detect the defects in massive area of diffusion barrier with a potential for quantifying the defect density in a simple timely, effective manner. Furthermore, the cyclic voltammetry method also has the potential for characterizing the integrity of capping layer, pore seal in Cu/low κ interconnects and contamination of ions in package substrate. However, as a new technique, there is still much work needed in order to fully apply the method in industry, for example, quantification of defects, a better test pattern, etc. Nevertheless, the capability of the method in detecting the presence of defects in diffusion barrier has been clearly shown, and makes it a valuable technique to further develop regardless of other potential applications.

6.1.2.2 Characterization of Low κ Materials

A step-mode voltammetry-based method is developed to characterize low κ structure in both dense and porous low κ in patterned interconnect structures by measuring the effective ion diffusivity in the electrolyte solution. The results indicate that electrolyte ions diffuse through porous and dense materials by different mechanism. The application of the method to thermal treated samples reveals that the pore structure in a patterned interconnect is not stable but experiences two competing processes: the collapse of pores created by compressive stress due to a mismatch of CTE in the interconnect structure and coarsening of the pores due to heating. Also the thermal alteration of pore structure is found to be pitch-dependent. Although lots of effort is still needed to make the method fully mature, such as, development of a model and reference for determining the actual porosity, pore size and distribution, the capability

of tracing the structure stability of PLK suggests the method may be an attractive technique for IC industry.

6.2 Future Work

This study is proven that the voltammetry method is a very attractive characterization technique for IC industry. Furthermore, the basic concept is found to have the potential to become a multiple function method. However, there is much work needed before it can be fully mature and serve as a standard characterization technique.

6.2.1 Characterization of Diffusion Barrier

The defect density in diffusion barrier is a very important parameter for industry to predict the lifetime of the devices. The cyclic voltammetry method for detecting barrier defects appears to have the capability to quantify the defect density since the intensity and the area of current peak is proportional to the defect density of the defective barrier: the more defects are present, the more current is produced. However, to quantify defects, a model as well as a reference test pattern is required, which remain as future work.

6.2.2 Characterization of Low κ Structure

The study on the characterization of pore structure clearly evidences that the step-mode volatmmetry method has a capability to provide valuable information related to pore structure, and much effort is needed to make this valuable technique more attractive for IC industry. Among these, the quantitative connection between the measured diffusivity and the physical pore structure, including pore size, pore distribution, pore interconnectiviy, etc. is one of the priority tasks for the further

development of step voltammetry method In addition, the study of pore thermal instability in low κ structure has been started in this work, but additional work is needed to be able to predict and accommodate change in the pore structure during interconnect processing and packaging operations.

6.2.3 Extend Applications of the Voltammetry Technique

It is noticed that the application of the developed method is not limited to the detection of diffusion barrier defects and the characterization of pore structure in low κ materials. The method is also found to have potentials to evaluate the integrity of the capping layer and the pore seal in as-fabricated Cu/ low κ interconnects as well as a potential to characterize ion contamination and Cu migration in the substrate of microelectronic packages. Those potential applications are worth to develop and also be remained as future work.

APPENDIX A

I-V MODEL OF A RC CIRCUIT WITH A LINEAR VOLTAGE SWEEP

When a linear potential sweep is applied to an RC circuit (figure A.1), that is, the potential increases linearly with time at a sweep rate υ (in V s^{-1}), the equation A.1 can be obtained.

$$E = \upsilon t = R_s(dq/dt) + q/C_d \qquad (A.1)$$

If q = 0 at t = 0,

$$i = \upsilon C_d\left[1 - \exp(t/R_sC_d)\right] \qquad (A.2)$$

The current rises from zero as the scan starts and attains a steady value, υC_d, as seen in figure A.2. If a cyclic linear potential is applied to a RC circuit, then the steady-state current changes from υC_d to $-\upsilon C_d$ for the voltage sweep with opposite polarity, as is seen in figure A.3.

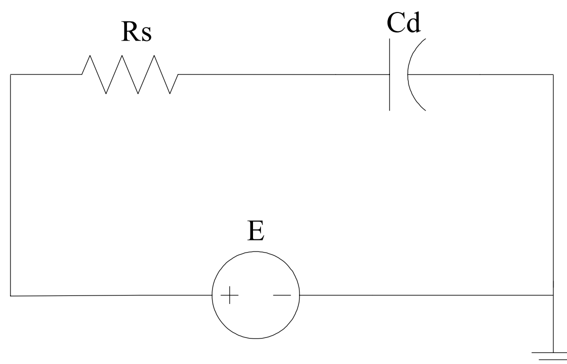


Figure A.1 A schematic of an RC circuit

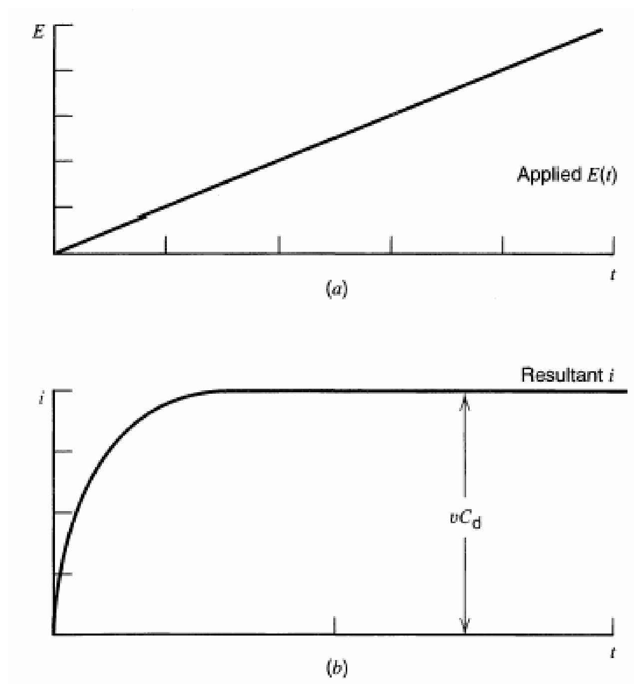


Figure A.2 Current-time (i-t) behavior resulting from a linear potential sweep applied to an RC circuit [81]

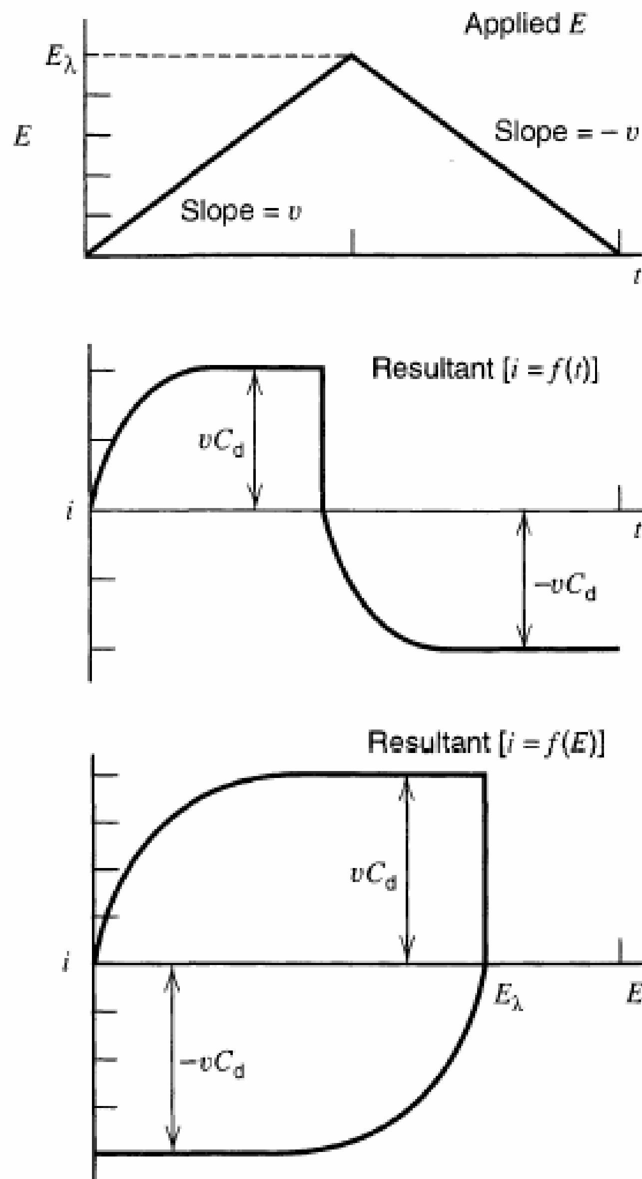


Figure A.3 Current-time and current-potential (i-E) resulting from a cyclic linear potential applied to an RC circuit [81]

APPENDIX B

THE SOLUTION FOR CONCENTRATION PORFILE

In the case of the defect-free barrier, the discharging current can be predicted from a simple diffusion model. The time variation of the surface charge density at each electrode can be modeled by solving Fick's second law,

$$\frac{\partial C(x,t)}{\partial t} = D\frac{d^2C(x,t)}{dx^2}, \tag{B.1}$$

The defect-free barrier provides an impermeable, non-reacting boundary for electrolyte ion, therefore a zero flux condition at each electrode surface is created, as seen in equation (B.2)

$$J(0,t) = (\frac{dC}{dx})_{x=0} = 0 \tag{B.2a}$$

$$J(l,t) = (\frac{dC}{dx})_{x=l} = 0 \tag{B.2b}$$

The initial condition of discharging current is determined from the stationary profile of the charging process. Therefore, the final concentration profile of the charging current has to be discussed. The flux equation during charging is given by

$$J(x,t) = -D\frac{dC}{dx} + vC \tag{B.3}$$

At t = ∞, the flux becomes zero and thus the concentration profile becomes

$$C(x,\infty) = M\exp(\frac{vx}{D}) \tag{B.4}$$

where integration constant M is given by

$$M = C_0[\frac{D}{vl}(\exp(\frac{vl}{D}) - 1)]^{-1}.$$

and the initial condition of the discharging current is given by equation (B.4):

$$C(x,0) = C_0[\frac{D}{vl}(\exp(\frac{vl}{D}) - 1)]^{-1} \exp(\frac{vx}{D}) \tag{B.5}$$

where C_0 represents the initial concentration of ions before application of the bias, and v is the anion drift velocity resulting from externally applied voltage between the two electrodes separated by width l.

The solution of the second order partial differential equation with the given boundary and initial conditions is a classical diffusion problem, and is already developed in many places [94-95].

$$C(x,t) = \frac{1}{l}\int_0^l C(x,t)dx + \frac{2}{l}\sum_{n=1}^{\infty}\exp(-Dn^2\pi^2 / l^2 t)\cos(\frac{n\pi x}{l})\int_0^l C(x,0)\cos(\frac{n\pi x}{l})dx . \tag{B.6}$$

Note that the addition of the factor of 2 accounts for both cation and anion contributions

The first term in equation B.6 is turn out to be

$$\frac{1}{l}\int_0^l C(x,t)dx = C_0 \tag{B.7}$$

The second term in equation B.6 is more complex and includes an integration term which is turned out to be a double integration combined with equation B.5,

$$\int_0^l C(x,0)\cos(\frac{n\pi x}{l})dx = M\int_0^l \exp(\frac{vx}{D})\cos(\frac{n\pi x}{l})dx \tag{B. 8}$$

Let $I = \int \exp(\frac{vx}{D})\cos(\frac{n\pi x}{l})dx$

Then, $I = (\frac{l}{n\pi})\exp(\frac{vx}{D})\sin(\frac{n\pi x}{l}) - (\frac{v}{D})(\frac{l}{n\pi})\int \exp(\frac{vx}{D})\sin(\frac{n\pi x}{l})dx$ (B.9)

Let $I_2 = \int \exp(\frac{vx}{D})\sin(\frac{n\pi x}{l})dx$

Then, $I_2 = -\frac{l}{n\pi}\exp(\frac{vx}{D})\cos(\frac{n\pi x}{l}) + (\frac{v}{D})(\frac{l}{n\pi})\int \exp(\frac{vx}{D})\cos(\frac{n\pi x}{l})dx$.

Thus, equation (B.9) becomes

$$I = (\frac{l}{n\pi})\exp(\frac{vx}{D})\sin(\frac{n\pi x}{l}) + (\frac{v}{D})(\frac{l}{n\pi})^2 \exp(\frac{vx}{D})\cos(\frac{n\pi x}{l}) - (\frac{v}{D})^2(\frac{l}{n\pi})^2 I. \qquad \text{(B.10a)}$$

and

$$I = \int_0^l \exp(\frac{vx}{D})\cos(\frac{n\pi x}{l})dx = \left|\exp(\frac{vx}{D})[(\frac{n\pi}{l}\sin(\frac{n\pi x}{l}) + (\frac{v}{D})\cos(\frac{n\pi x}{l}))/[(\frac{n\pi}{l})^2 + (\frac{v}{D})^2]\right|_{x=0}^{x=l}$$

or

$$I = \frac{v}{D}\left((\exp(\frac{vl}{D})\cos n\pi - 1\right)\Big/\left((\frac{n\pi}{l})^2 + (\frac{v}{D})^2\right)$$

$$= -\frac{v}{D}\left((-1)^n \exp(\frac{vl}{D}) - 1\right)\Big/\left((\frac{n\pi}{l})^2 + (\frac{v}{D})^2\right) \qquad \text{(B.10b)}$$

The final solution of concentration profile is given by putting all together into equation (B.6),

$$C(x,t) = C_0 + \frac{2M}{l}\sum_{n=1}^{\infty}\exp\left(-(\frac{n\pi}{l})^2 Dt\right)\left(\frac{(\frac{v}{D})[(-1)^n \exp(\frac{vl}{D}) - 1]}{(\frac{n\pi}{l})^2 + (\frac{v}{D})^2}\right)\cos(\frac{n\pi x}{l}) \qquad \text{(B.11)}$$

APPENDIX C

THE SOLUTION OF DISCHARGING CURRENT

The discharging current can be calculated from the difference in the time variation of ions concentration at two electrodes, that is

$$j(t) = \frac{dQ_t}{dt} \tag{C.1}$$

where Q_t represents the total charge accumulated (deviation from equilibrium), and it is determined by the net concentration change of ions with time:

$$j(t) = \frac{d}{dt}(C(0,t) - C(l,t)) = \frac{dC(0,t)}{dt} - \frac{dC(l,t)}{dt} \tag{C.2}$$

where

$$\frac{dC(0,t)}{dt} = \frac{2M}{l}\sum_{n=1}^{\infty}\left(-(\frac{n\pi}{l})^2 D\right)\left(\exp\left(-(\frac{n\pi}{l})^2 Dt\right)\right)\left(\frac{(\frac{v}{D})[(-1)^n \exp(\frac{vl}{D}) - 1]}{(\frac{n\pi}{l})^2 + (\frac{v}{D})^2}\right)$$

$$\frac{dC(l,t)}{dt} = \frac{2M}{l}\sum_{n=1}^{\infty}\left(-(\frac{n\pi}{l})^2 D\right)\left(\exp\left(-(\frac{n\pi}{l})^2 Dt\right)\right)\left(\frac{(\frac{v}{D})[(-1)^n \exp(\frac{vl}{D}) - 1]}{(\frac{n\pi}{l})^2 + (\frac{v}{D})^2}\right)\cos(n\pi)$$

Therefore, the discharging current becomes

$$j(t) = \frac{2M}{l}\sum_{n=1}^{\infty}\left(-(\frac{n\pi}{l})^2 D\right)\left(\exp\left(-(\frac{n\pi}{l})^2 Dt\right)\right)\left(\frac{(\frac{v}{D})[(-1)^n \exp(\frac{vl}{D}) - 1]}{(\frac{n\pi}{l})^2 + (\frac{v}{D})^2}\right)(1 - \cos(n\pi))$$

or

$$j(t) = \frac{2M}{l}\sum_{n=1}^{\infty}\left(-(\frac{n\pi}{l})^2 D\right)\left(\exp\left(-(\frac{n\pi}{l})^2 Dt\right)\right)\left(\frac{(\frac{v}{D})[(-1)^n \exp(\frac{vl}{D}) - 1]}{(\frac{n\pi}{l})^2 + (\frac{v}{D})^2}\right)(1 - (-1)^n) \tag{C.3}$$

Since $(-1)^n - 1 = 2, 0, 2, 0, \ldots$ (for n=1, 2, 3, 4, …), the discharging current solution can be changed to

$$j(t) = \frac{4M}{l}\sum_{n=1}^{\infty}\left(-\left(\frac{(2n-1)\pi}{l}\right)^2 D\right)\left(\exp\left(-\left(\frac{(2n-1)\pi}{l}\right)^2 Dt\right)\right)\left(\frac{(\frac{v}{D})[(-1)^{2n-1}\exp(\frac{vl}{D})-1]}{\left(\frac{(2n-1)\pi}{l}\right)^2 + (\frac{v}{D})^2}\right)$$

Now, the normalized discharging current becomes

$$j_n(t) = \frac{j(t)}{j(0)} = \frac{\sum_{n=1}^{\infty}(2n-1)^2\exp\left(-\left(\frac{(2n-1)\pi}{l}\right)^2 Dt\right)\Big/\left(\left(\frac{(2n-1)\pi}{l}\right)^2 + (\frac{v}{D})^2\right)}{\sum_{n=1}^{\infty}(2n-1)^2\Big/\left(\left(\frac{(2n-1)\pi}{l}\right)^2 + (\frac{v}{D})^2\right)}$$

$$j_n(t) = \frac{j(t)}{j(0)} = \frac{\sum_{n=1}^{\infty}\exp\left(-\left(\frac{(2n-1)\pi}{l}\right)^2 Dt\right)\Big/\left(\left(\frac{\pi}{l}\right)^2 + \frac{1}{(2n-1)^2}(\frac{v}{D})^2\right)}{\sum_{n=1}^{\infty}1\Big/\left(\left(\frac{\pi}{l}\right)^2 + \frac{1}{(2n-1)^2}(\frac{v}{D})^2\right)} \qquad \text{(C.4)}$$

The solution becomes simple to apply when the normalized current, *I(t)/I(0)*, is defined and it is found to be [10]

$$j_n(t) = \sum_{n=1}^{\infty} a_n \exp\left(-\left(\frac{(2n-1)\pi}{l}\right)^2 Dt\right)\Big/\sum_{n=1}^{\infty} a_n \qquad \text{(C.5)}$$

where $a_n = 1\Big/\left(\left(\frac{\pi}{l}\right)^2 + \frac{1}{(2n-1)^2}(\frac{v}{D})^2\right)$ (n=1,2,3…)

$$j_n(t) = \sum_{n=1}^{\infty} B_n \exp\left(-\frac{n^2\pi^2}{l^2}Dt\right) \quad \text{(n=1,3,5,7…)} \qquad \text{(C.6)}$$

where $B_n = a_n \Big/ \sum_{n=1}^{\infty} a_n$ and $\sum_{n=1}^{\infty} B_n = 1$

The series constant B_n contains constants for integration and normalization.

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