STUDY ON THE LEAKAGE CURRENT BEHAVIOR AND CONDUCTION MECHANISM OF POROUS LOW-K IN CU/POROUS LOW-K INTERCONNECTS: THE INFLUENCE OF EXTRINSIC FACTORS

by

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ABSTRACT

STUDY ON THE LEAKAGE CURRENT BEHAVIOR AND CONDUCTION MECHANISM OF POROUS LOW-K IN CU/POROUS LOW-K INTERCONNECTS: THE INFLUENCE OF EXTRISNIC FACTORS

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The University of Texas at Arlington, 2010

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This study investigates the influence of extrinsic factors including moisture and impurities trapped in porous low-k (PLK) and defective diffusion barrier on the leakage current behavior and the associated conduction mechanism of PLK in advanced Cu/PLK interconnects. For this purpose, a voltammetry technique that was previously developed for diffusion barrier characterization was extended to detect the trapped impurities in PLK. With this technique in hand, the influence of extrinsic factors was then studied.

Cu was found to diffuse out into PLK through barrier defects in the presence of electric stress. Its out-diffusion and subsequent migration in PLK manifested as a unique hump behavior in the leakage current under moderate testing conditions, i. e. room temperature and intermediate electrical field (0.2 – 0.8MV/cm). The mechanism behind such a current hump was revealed to be the space-charge-limited (SCL) transient current. With the theory of SCL mechanism, the mobility of Cu ions in the PLKs used in this study was estimated to be as high as $10^{-13}cm^2/V\text{-}sec$ at room temperature. Due to the high mobility of Cu ions in PLK, aggressive

testing conditions tend to make the signature of Cu out-diffusion in the leakage current too short to detect.

With the understanding on the influence of Cu out-diffusion in the leakage current, a step mode current-time method was developed to study the electrical stress induced barrier failure in Cu/PLK interconnects. The barrier failure was found to be triggered by a critical electrical stress: only when the applied stress was above a critical point can diffusion barrier failure take place. Interestingly, the critical stress was further revealed to be pattern-density dependent, which was attributed to the pattern-density dependent barrier quality created during fabrication processes: due to the thermomechanical property mismatch between Cu and PLK, compressive stress that is primarily determined by the mechanically stronger Cu is developed and acts on the diffusion barrier during thermal loading cycles, creating barrier roughing with weak spots that favor Cu out-diffusion.

When impurities and defective barrier presented, moisture was found to create a current peak in voltage-ramp measurement. The mechanism for this current peak was revealed to be the electrochemical reaction between moisture activated impurities and the metallic electrode. Such an electrochemical reaction can happen in two different situations. For samples with defective barrier, reaction takes place between exposed Cu and moisture-impurity electrolyte. For samples containing some specific impurities in PLK, reaction can take place between activated impurities and Ta electrode. However, in order to observe the reaction current peak, both impurities and moisture are needed because only with conductive electrolyte can reaction current be effectively delivered when reaction takes place.

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INTRODUCTION

1.1 Research Motivation and Achievements

The transition of interconnect metallization from Al/SiO_2 to Cu/porous low-k dielectric (Cu/PLK) has spurred extensive research on the material and technical development as well as the fundamental understanding on the properties of materials. Among many active studies, the subject of leakage current behavior and its associated conduction mechanism in PLK is of particular interest, not only because it is an area that is less explored and least understood but also because it is closely correlated to the electrical reliability of modern Cu/PLK interconnects.

While various studies have been done and numbers of conduction mechanisms have been suggested in literature, the understanding of current transport in PLK is still far from complete. It is a customary assumption in current studies that the leakage current in PLK is an electrical response based on its intrinsic properties and free of impact from extrinsic factors. Due to the incorporation of new materials and the adaptation of new fabrication processes, however, several extrinsic factors can be introduced into Cu/PLK interconnects. Such factors include (1) chemical impurities and moisture trapped in PLK, and (2) defective diffusion barrier either from unoptimized fabrication processes or external stresses after completing package, through which Cu may diffuse out into adjacent PLK. All these factors are expected to play an important role in the current transport in PLK and thus have to be considered in the leakage current behavior study and conduction mechanism investigation. Additionally, these extrinsic factors also have adverse effect on Cu interconnect reliability. It is therefore essential to study their influence on the leakage current behavior and reveal the associated conduction mechanism so that the potential threats to Cu interconnect reliability can be early detected.

In this study, the leakage current behavior and conduction mechanism in PLK in modern Cu/PLK interconnects have been investigated. The primary focus is the influence of the extrinsic factors on the current transport in PLK. A practical method, based on the previous voltammetry technique that has been proven to be simple yet effective in characterizing the defective diffusion barrier, was developed to characterize the impurities and moisture trapped in PLK first. With the tools for characterizing the extrinsic factors in hand, the signature of Cu out-diffusion in leakage current was identified, and the impact of moisture and impurities on the leakage current behavior was investigated. More importantly, the associated conduction mechanisms were revealed. With the gained understandings in this study, several techniques in detecting the potential threats to Cu/PLK interconnect reliability have been proposed.

In this chapter, the advanced technology of modern Cu/PLK interconnects will be briefly introduced first to provide some basics for this study. The incorporated new materials and the newly adapted integration scheme will be emphasized. The sources of extrinsic factors and raised reliability concerns will be discussed.

1.2 Background: Technology of Advanced Cu/PLK Interconnects

1.2.1 Intrinsic Gate Delay vs. Interconnect Delay

Interconnects refer to the wires connecting functional devices on the silicon substrate. In the past generations of technology nodes where Al and Al-Cu alloy were commonly used as the on-chip interconnection wires and SiO_2 served as the inter- and intra-layer insulating dielectrics. At that time, the performance of microelectronics was primarily limited by the intrinsic gate delay arising from the switching speed of electronic devices. With the successful miniaturization of advanced technology node, the physical size of electronic devices, especially the gate length in the basic Metal-Oxide-Semiconductor (MOS) unit, has been dramatically reduced in the past decades. Accordingly, the interconnection wires have become smaller and longer and the dielectric space has become narrower. While significant progress in reducing the intrinsic gate delay has been made due to the aggressive physical size reduction, the delay

from the electrical signal propagating through the interconnected circuits, so called RC delay originating from the effective resistance (R) of the metallic interconnection and the capacitance (C) associated with the insulating dielectric, starts to dominate over the intrinsic gate delay, becoming the bottleneck that limiting the overall performance of modern microelectronics [1-4]. As seen in Figure 1.1, when the technology node advanced into deep sub-micron regime, the interconnect delay became increasingly significant compared to the intrinsic gate delay [4].

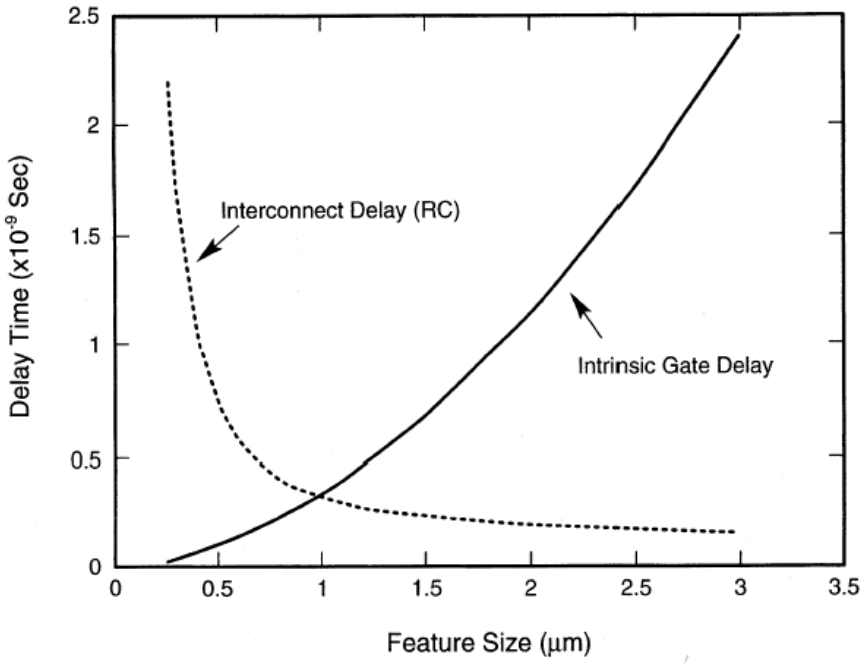


Figure 1.1 The intrinsic gate delay and the interconnect delay as a function of feature size

Mathematically, the interconnect delay can be approximated by the product of R and C, leading to an expression [5]

$$RC = \frac{\rho}{t_M}\frac{L^2 \varepsilon_{ILD}}{t_{ILD}} \tag{1.1}$$

where ρ, t_M, and L are respectively the resistivity, the thickness and the length of interconnected wires; ε_{ILD} and t_{ILD} are respectively the permittivity and the thickness of interlevel dielectric (ILD). Notice that $\varepsilon_{ILD} = k\varepsilon_0$, where k is the dielectric constant and ε_0 is the permittivity of free space.

From the perspective of material property, it is obviously seen from Equation (1.1) that in order to reduce RC delay, two approaches or a combination of both are needed. One is to utilize metallic wires with lower electrical resistivity (ρ) to replace conventional Al and Al alloys and the other is to develop new dielectric materials with lower dielectric constant (k) to substitute SiO_2.

1.2.2 Cu Replaces Al as Metallic Conductor

Solely from the aspect of electrical resistivity, three elements, silver (Ag), gold (Au) and copper (Cu), appear to be the ideal candidates to replace Al as the metallic conductor in advanced interconnects. However, in addition to the electrical resistivity, other considerations including anti-corrosion performance, resistance to electromigration and stress migration, thermal conductivity, adhesion to and diffusion into adjacent dielectrics and silicon substrate, manufacturability, and cost also have to be taken into account. Even though Ag has the lowest bulk resistivity at room temperature, several drawbacks such as extremely poor resistance to corrosion [6-8], morphology instability at elevated temperature [9, 10], poor adhesion to SiO_2 [11, 12] and fast diffusion in silicon substrate [13, 14], impede its utilization as the metallic conductor in advanced interconnects. Au possesses excellent anti-corrosion performance and good resistance to electromigration but has only slightly lower electrical resistivity yet considerably high cost compared to Al. On the other hand, Cu offers several advantages over Al and other candidates. As see in Table 1.1 [15-18], Cu has very low electrical resistivity at room temperature, about 60% that of Al. In addition, Cu has the highest melting temperature (1084^oC), which gives Cu a potentially superior performance in electromigration [19-26]. Moreover, with the newly established integration scheme called dual damascene (see section 1.2.5), the total number of metallization steps, compared to that required in conventional Al patterning, can be reduced, which, in turn, significantly reduces the manufacturing cost. Therefore, despite certain limitations such as poor adhesion to dielectrics and poor corrosion resistance, which can be improved by a thin layer of diffusion barrier materials, Cu clearly

demonstrates its superiority over others, making it an ideal candidate for replacing conventional Al and Al alloys.

Table 1.1 Comparison of some material properties of possible metallic conductor candidates for advanced interconnects

	Al	Ag	Au	Cu
Resistivity (uΩ-cm)	2.66	1.59	2.35	1.67
Melting point (^{o}C)	660	962	1064	1084
Young's modulus (GPa)	70.6	82.7	78.5	129.8
Adhesion to SiO_2	good	poor	poor	poor
Corrosion resistance in air	good	poor	excellent	poor
Electromigration resistance	poor	very poor	good	good
Sputtering deposition	ok	ok	ok	ok
Electroplating	ok	ok	ok	ok
Dry etching	ok	no	no	no
Wet etching	ok	ok	ok	ok

With Cu introduced into interconnect, significantly lower resistance, higher allowed current density, and increased scalability relative to conventional Al wire, can be achieved, which enables the further scaling of pitch size and thickness. This means a higher package density and higher complexity of wiring structure can be obtained for on-chip interconnects, which is also consistent with high-performance and high-density needs [27]. Since IBM first announced its entry into Cu interconnect technology in 1997, Cu has substituted Al, becoming the mainstream on-chip interconnect conductor in advanced integrated circuits. Shown in Figure 1.2 is a micrograph displaying the complexity of Cu wire pattern for the 32-bit RISC central process unit (CPU) announced by IBM [27, 28].

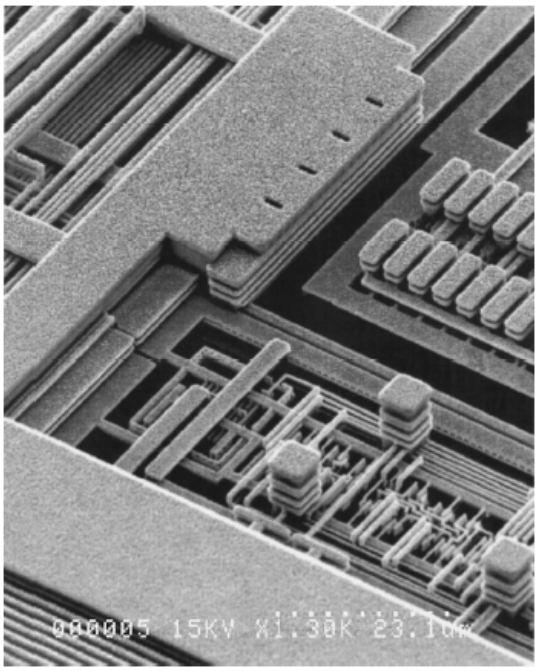


Figure 1.2 The characteristics of a six-level Cu interconnect with dielectrics removed.

1.2.3 Low Dielectric Constant (Low-k) Materials

The interconnect delay can also be reduced by the incorporation of dielectrics with lower dielectric constant (low-k) to replace SiO_2 (k~4.0). While the selection for metallic conductor is relatively clear because the choices of interconnect metal are rather limited, developing suitable dielectrics for successful integration into advanced interconnects is, however, extremely difficult, primarily owing to the stringent requirements on material properties [29, 30]. Ever since the decision of the implementation of low-k dielectrics, the development of low-k materials and related integration technical issues have become and will continue to be one of the most challenging and extensively researched areas in microelectronic community.

Physically, the dielectric constant, or equivalently the permittivity of a dielectric, is its polarizability in response to the applied electrical field [31-34]. The dielectric polarization typically consists of three components: electronic polarization, distortion polarization and orientation polarization. The electronic component describes the response of the electronic

cloud bound around the nuclei to electrical field. Distortion polarization comes from the distortion (displacement) of nuclei induced by electrical field. The orientation polarization occurs only in polar molecules that have permanent electric dipole moment. Without electrical field, these dipoles are randomly pointing to all possible directions in space due to thermal vibration caused disorder, effectively resulting in a zero dipole moment. However, in the presence of electrical field, the thermally activated dipoles are aligned to the direction of the applied field, producing orientation polarization. When subjected to an AC electrical field, the electronic component can generally follow instantaneously to field change as only the displacement of electronic cloud is involved. In contrast, the distortion component can not respond so rapidly since it involves the distortion of entire atomic bond. The orientation component has the slowest response because it requires the rotation of whole molecule to align to the direction of electrical field. Typically, when the signal frequency is beyond visible light at ~10^{15}Hz, only electronic component dominates in the dielectric permittivity; between ~10^{13} to 10^{15}Hz, both electronic and distortion components contribute to polarization; below ~10^{9}Hz, orientation component starts to play a role in the dielectric constant [35]. Because the current device operating frequency is less than ~10^{9}Hz, the contribution from all three components needs to be considered when developing low-k dielectrics.

The reduction of dielectric constant relative to SiO_2 can therefore be achieved in two ways. The first is to incorporate substitutes that have lower polarizability and the second is to decrease the atomic density in dielectrics.

With respect to the first method, several strategies have been taken in low-k material development. Polar groups such as hydroxyl (OH) and carbonyl (CO) with permanent dipole moment should be eliminated, or at least minimized because they contribute orientation polarization, and more adversely, make dielectric susceptible to uptake moisture. It is well known that moisture is extremely detrimental to interconnect dielectrics not only because it has large permanent dipole that increases dielectric constant but also because moisture adsorption

significantly increases the line-to-line leakage current, resulting in the decrease of lifetime of microelectronic devices. Conversely, methyl (CH_3) group is desired as it is non-polar and hydrophobic. Because of its large size, the incorporation of CH_3 group can also lower atomic density of dielectrics, leading to the further reduction of dielectric constant. The electronic contribution can be decreased by introducing atomic bonds with lower electronic polarizability. The distortion polarization can be reduced by the components with stronger bonding strength.

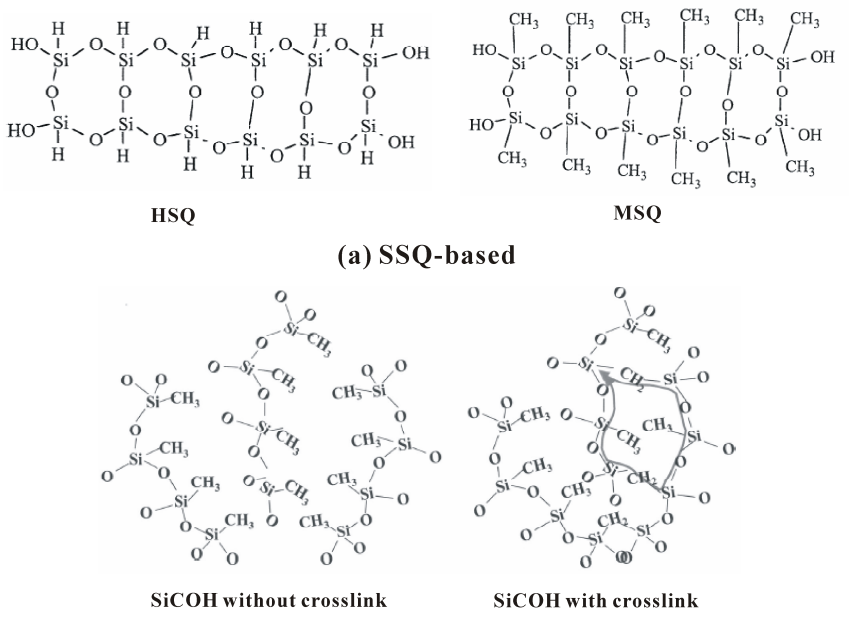


Figure 1.3 Elemental units of (a) SSQ-based HSQ and MSQ; and (b) silica-based SiCOH without and with crosslink.

Various low-k dielectrics have been developed by the substitutional method. For example, in the first generation of low-k dielectric that has been widely used for both 180nm and 130nm technology nodes, Si-O bonds are replaced by less polarized Si-F bonds to form fluorine-doped silicate glass (FSG) [36-39]. In the second generation of low-k materials, the low permittivity is achieved by the breakage of Si-O bond and substitution with large-sized organic terminating groups such as $–CH_3$ to lower dielectric density as well as molecular polarizability.

These materials are generally called dense low-k materials. The representatives include silsesquioxane-based hydrogen-silsesquioxane (HSQ) [40-42], and methyl-silsesquioxane (MSQ) [43-45], and silica-based organosilicate glass (carbon-doped silica: OSG or SiCOH) [46-48], and their elementary units are depicted in Figure 1.3.

The possible reduction of dielectric constant by substitutional method, however, is limited by the intrinsic properties of materials. There is currently no dense low-k material available for semiconductor applications with a dielectric constant below 2.5. Further reduction of dielectric constant has to rely on the decrease of atomic density in dielectrics. This can be readily inferred and understood from the structure of organic polymers. The reason that organic polymers have lower dielectric constant relative to solid SiO_2 is partly due to the fact that most polymer chains have large space instead of dense cross-linked network.

Technically, the dielectric constant is further reduced by the introduction of nano-sized pores into dielectrics [49-55]. Such materials are called porous low-k dielectrics (PLK) and have been widely used in the new generations of Cu interconnects. For example, in the process of porous SiCOH film by plasma-enhanced chemical vapor deposition (PECVD) technique, hydrocarbon fragments is firstly incorporated into the deposited film through the reaction of the organic precursor and tetramethylcyclotetrasiloxane (TMCTS). A thermal annealing is then applied to the deposited film to remove carbon and hydrogen by the fragmentation and the loss of incorporated organic fragments, which creates a large fraction of cage structure, forming nano-pores in SiCOH films [55].

The PLK materials can be viewed as a two-component system with solid dielectrics and open free space. According to Bruggeman, the effective dielectric constant in such a system can be approximately predicted by [30, 56]

$$f_1 \frac{k_1 - k_e}{k_1 + 2k_e} + f_2 \frac{k_2 - k_e}{k_2 + 2k_e} = 0 \tag{1.2}$$

where f_1 and f_2 are the volume ratio of these two components, respectively; k_1 and k_2 are their dielectric constants; k_e is the effective dielectric constant of the entire dielectric system. Since the dielectric constant of free space is unit, the higher the porosity introduced, the lower the dielectric constant is. Therefore, in order to further reduce the dielectric constant, a large volume ratio of pores is desired. The incorporation of open pores into low-k materials, however, also has adverse effect on material properties. With the increase of porosity, the PLK strength against external electrical, chemical and thermomechanical loads significantly degrades, which has raised significant integration challenges and extensive reliability concerns in advanced Cu/PLK interconnects. Such integration challenges and reliability concerns will be discussed in more details in section 1.3.

1.2.4 Diffusion Barrier

Other than the metallic conductor and the dielectric materials, another key difference of Cu interconnects in comparison to Al interconnects is the requirement of diffusion barrier. Unlike Al that can form a native layer of oxide that can prevent Al from corrosion and diffusion into adjacent dielectrics, Cu is lacking of such self-passivation layer and hence prone to corrosion and can readily diffuse into dielectrics, leading to severe degradation of electronic devices. Practically, in order to solve these problems, a thin layer of diffusion barrier is deposited between Cu and dielectrics. In Al interconnects, the native oxide also enables good adhesion between Al lines and dielectric layers. Therefore, the diffusion barrier in Cu interconnects is also required to provide good adhesion. Such a good adhesion has also been proven to be of critical importance in the electromigration performance of Cu lines [57-62]. Aside from the requirements mentioned above, there are several other considerations that need to be taken into account, including chemical and thermal stability, i. e. non-reactive with Cu and substrates, enhanced resistance to thermal and mechanical stresses that are inevitable during fabrication processes, good step coverage with respect to trench and via, and excellent compatibility with integrated circuit fabrication flows [63]. For diffusion barrier covering the side and bottom walls that is

usually referred to as liner, low resistivity is desired so that effective resistance of metal lines can be reduced. For the barrier capped at the top surface of Cu lines that is usually called capping layer, low dielectric constant is preferred because this reduces the overall effective capacitance of Cu/PLK interconnects.

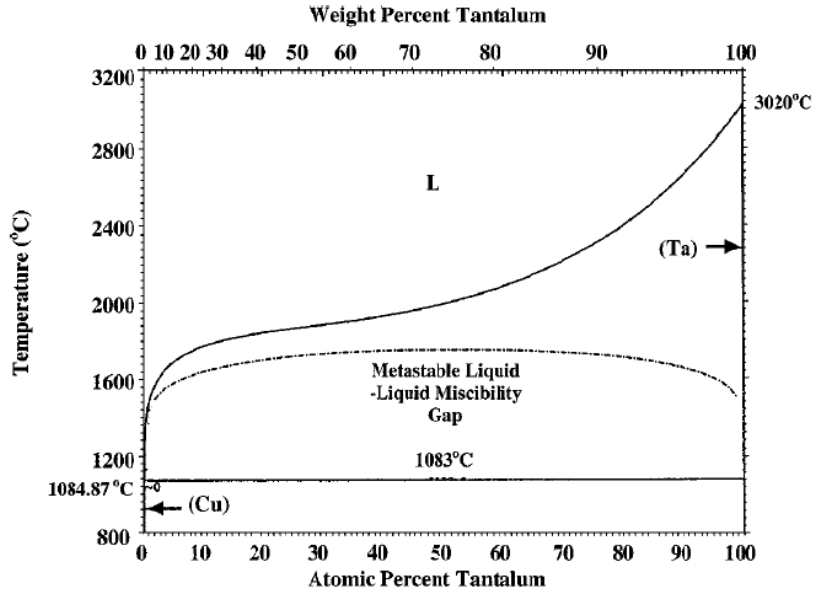


Figure 1.4 The phase diagram showing the excellent thermodynamic stability of Cu-Ta at elevated temperature.

Typically, these requirements are achieved by appropriately selecting diffusion barrier material to clad Cu lines. As low-k dielectrics, various diffusion barrier materials have been suggested [64]. Since the melting temperature of a metal, to a certain degree, is a good indication of its effectiveness in preventing Cu out-diffusion, choosing refractory metals and their compounds with high melting temperature as diffusion barrier is intuitively straightforward. Numbers of refractory metal candidates have been extensively investigated [65-82]. Currently, the most widely employed diffusion barrier films are tantalum (Ta) and its binary nitride compounds. In terms of diffusion prevention effectiveness, Ta has a melting temperature as high as 3017^{o}C and therefore is expected to be an excellent diffusion barrier material. In the

regard of thermal and chemical stability, Ta is thermodynamically stable with both Cu and Si substrate, providing stable Ta/Cu and Ta/Si interfaces at relative high temperature. As seen in the Ta-Cu phase diagram in Figure 1.4, Ta and Cu are almost completely immiscible up to their melting point and do not react to produce any compounds [83]. Furthermore, deposition of Ta by either PVD or CVD techniques can provide reasonable conformality of barrier films in both trench and via in current Cu interconnects. Finally, it has been shown that a small fraction of nitrogen doping into Ta film, typically produced by reactively sputtering Ta in the presence of N_2 ambient, can effectively suppress the fastest diffusion path, i. e, grain boundary diffusion in diffusion barrier: with an appropriate percentage doping of nitrogen, a polycrystalline microstructure of tantalum nitride film with fine-sized grains can be produced, which effectively elongates the diffusion path through grain boundaries and thus enhances its effectiveness in preventing Cu out-diffusion [76-78].

1.2.5 Cu Metallization Scheme: Dual Damascene Process

Accompanied with the transition from Al/SiO_2 to Cu/PLK interconnect is the development of new integration schemes for creating highly accurate, manufacturable and highly integrated interconnects. In Al interconnects the metallization was typically done by the subtractive patterning technique using reactive ion etching (RIE), which, however, is not applicable to Cu interconnects, primarily due to the fact that Cu is lacking of volatile reactive by-products at low temperature and thus acceptable Cu etching rate can not be achieved [84, 85]. As an alternative technique, Cu dual damascene process has been developed and gained manufacturing acceptance in microelectronic industry [86, 87].

Several dual damascene integration schemes have been established in the past years. Depending on the trench and via patterning sequence, these schemes can be basically classified as being either via-first or trench-first, both of which are commonly used and have their own advantages and disadvantages. Nevertheless, regardless of the slight variations in different integration schemes, the common advantage of dual damascene process compared to

the Al RIE patterning, as will be seen below, is the lower cost due to the fact that trenches and vias are defined separately but filled with metals together [88]. This reduces the cost of manufacturing, especially in multi-level interconnect structures.

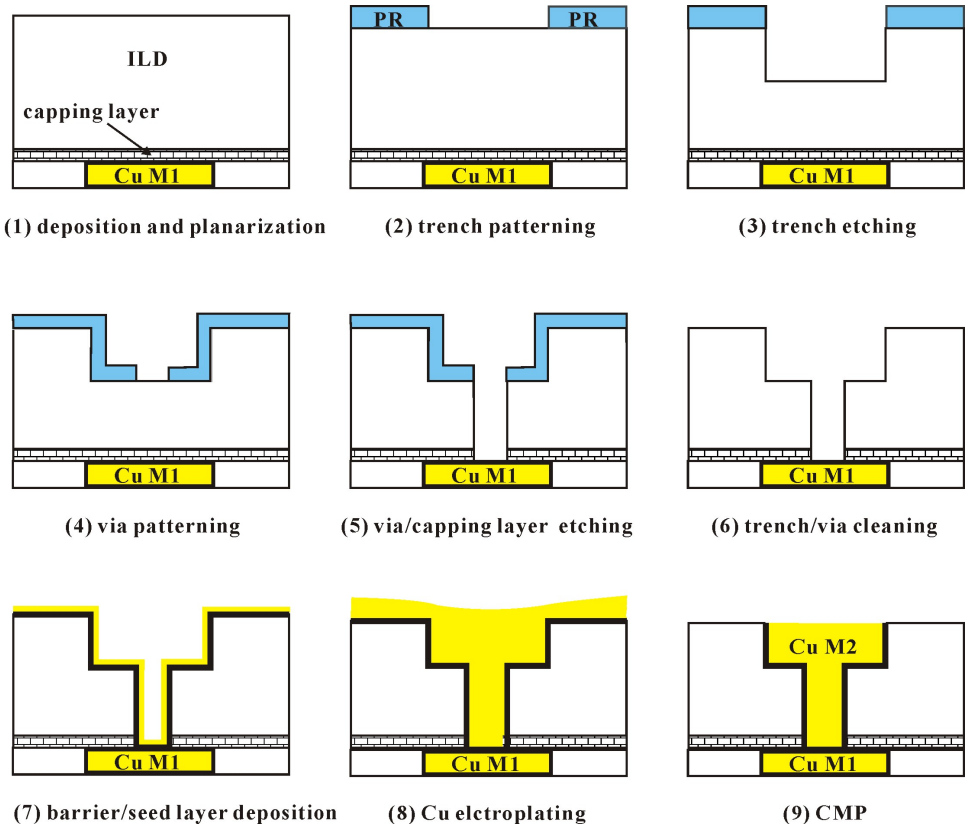


Figure 1.5 A schematic plot showing the basic steps in the trench-first dual damascene integration scheme.

As an example, the basic steps of dual damascene process for a trench-first two-level Cu interconnect structure are schematically illustrated in Figure 1.5. The trench-first technique starts with the deposition and planarization of capping layer and ILD. Silicon nitride (SiN) or silicon carbon nitride (SiCN) is typically used as capping layer material for preventing Cu diffusion into PLK and Si substrate as well as for protecting the bottom Cu trench M1 from overetching. The wafer is then coated with photoresist (PR), lithographically patterned and etched into the ILD to define the trench and subsequently the via (step 3-5 in Figure 1.5). After

trench and via cleaning processes to remove PR strip and etching residuals, two thin metal layers, the diffusion barrier followed by a Cu seed film that is required for the subsequent Cu electroplating, are deposited by either PVD or CVD techniques. Next, the via and trench are filled together with Cu by electroplating. The excessively deposited Cu and diffusion barrier film are removed and planarized by CMP with in-laid Cu M2 pattern. Finally, another thin dielectric layer such as silicon nitride, silicon carbide or silicon carbon nitride is deposited to create a passivation layer. Figure 1.6 schematically shows the cross-section of a multi-level Cu/PLK interconnect structure where each individual component can be seen [89]. In Figure 1.7, a SEM micrograph of Intel 45nm Cu/PLK interconnect structure is shown [90].

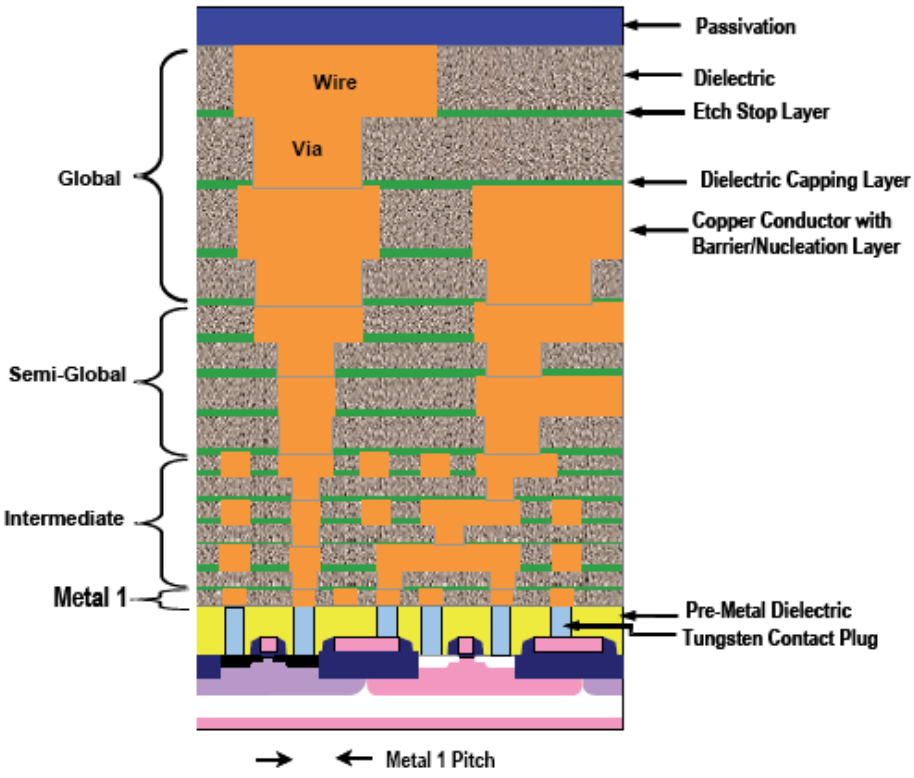


Figure 1.6 A schematic plot showing the cross-section of a multi-level Cu/PLK interconnect structure

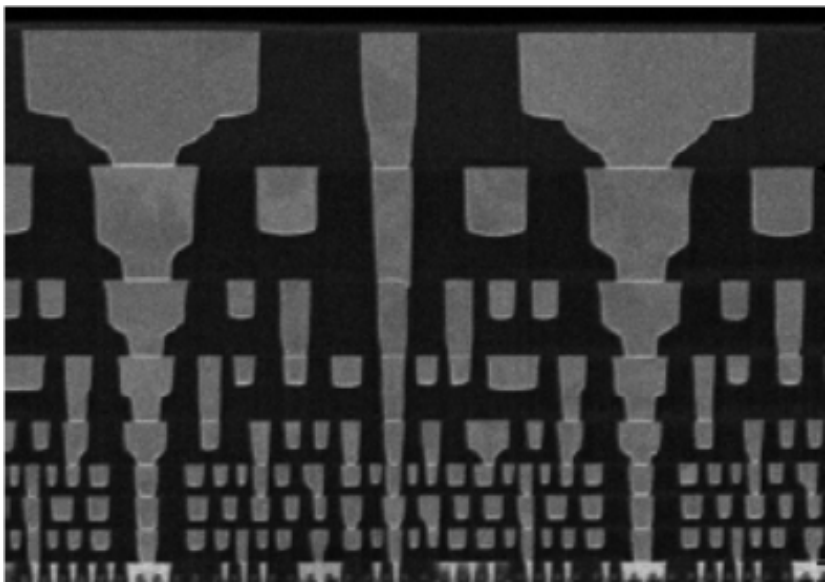


Figure 1.7 A SEM image showing Intel 45nm Cu/PLK interconnect structure stacking up to metal-8.

1.3 Integration Challenges and Sources of Extrinsic Factors

Even with the well established dual damascene process flow in the past years, the incorporation of new materials as well as the requirement of aggressive miniaturization of technology node has created a number of integration challenges and reliability concerns. The integration challenges come from several aspects, including: (1) the weak mechanical strength of PLK that usually exhibits poor adhesion to surrounding layers and PLK film delemination when subjected to thermal and mechanical loads during CMP, assembly and electromigration reliability test; (2) the weak chemical compatibility of PLK with chemicals used in wet or dry etching and ashing processes; (3) step coverage and barrier film uniformity in Cu trenches and vias, especially these with high aspect ratio. The reliability concerns primarily arise from the intrinsic properties of materials in the interconnect structure, including: (1) the electromigration reliability of Cu lines due to the increasingly high current density in advanced technology nodes; (2) the electrical reliability of the whole Cu interconnect structure due to the intrinsic weakness of PLK against electrical load. While these challenges and reliability concerns have been

comprehensively reviewed by numbers of papers [18, 24, 59, 91-95], this section concentrates on the extrinsic factors possibly introduced during integration processes that are expected to affect the leakage current behavior and conduction mechanism of PLK, and adversely impact the reliability of fully patterned Cu/PLK interconnects.

The extrinsic factors are the direct results of two major causes: the unoptimized fabrication processes and the inherently inferior properties of newly introduced materials such as PLK and diffusion barrier films. In this section, several integration challenges that may be responsible for the origins of extrinsic factors will be introduced. Concerns on Cu/PLK interconnect reliability caused by these challenges and the introduced extrinsic factors will also be addressed. However, it should be pointed out that these sources of extrinsic factors are probably the most commonly encountered but not limited to the ones introduced here.

1.3.1 Defective Diffusion Barrier: Cu Out-diffusion

One of the particular concerns in advanced Cu interconnects is the integrity of diffusion barrier films. Uniform step coverage is essential to Cu interconnect reliability because barrier failure usually occurs in the thinning areas in barrier films .On the other hand, a thin barrier film is desired to reduce the effective resistance of interconnect, which is especially mandatory in future technology nodes in terms of interconnect delay reduction. As seen in Table 1.2 where the parameters of several key materials are shown, in order to reduce the effective resistance, extremely thin diffusion barrier is demanded in the future technology nodes [89]. While diffusion barrier is thinning down, concerns on the adequate step coverage have imposed significant challenges on diffusion barrier deposition, and impeded the further scaling of advanced Cu/PLK interconnects.

Diffusion barrier films in current Cu/PLK interconnects are almost exclusively deposited by PVD (sputtering) techniques due to its simple nature and low cost. Conventional PVD fails to provide uniform step coverage because of its isotropic deposition profile. The large angular distribution of sputtered atomic flux usually deposits more materials on the up corners of

trenches and vias, which blocks the further filling at the bottom and sidewall during deposition, resulting in overhang formation and subsequent void formation even at moderate aspect ratio. Modified PVD techniques by the use of collimator [96-98], or in-flight ionization [99-102], can enhance the step coverage and conformity of diffusion barrier films in moderate aspect ratio but fails in high aspect ratio via due to its intrinsic directional nature. Alternatively, CVD techniques provide better deposition uniformity but often at the cost of high concentration of impurity contamination and high process temperature, both of which are undesired in process flow [79, 103]. A great deal of effort has been invested in atomic layer deposition (ALD) technology with which the diffusion barrier thickness and step coverage can be better controlled [103-106]. However, the self-limitation of ALD process where deposition is done in a discrete, time-separated manner intrinsically limits the deposition rate of this technique, yielding unacceptably low throughout and thus preventing its application in large-scale fabrication.

Table 1.2 Parameters of several key materials in advanced Cu/PLK interconnect

Year	2007	2008	2009	2010	2011	2012	2013
Technology node (nm)	65	59	52	45	40	36	32
Barrier thickness (nm)	4.8	4.3	3.7	3.3	2.9	2.6	2.4
Metal effective resistance (uΩ-cm)	3.51	3.63	3.80	4.08	4.30	4.53	4.83
ILD k_{bulk}	2.5~2.9	2.5~2.9	2.3~2.7	2.3~2.7	2.3~2.7	2.1~2.5	2.1~2.5

Figure 1.8 shows a non-uniform diffusion barrier deposited by self-ionized plasma physical vapor deposition (SIP-PVD) technique [18]. With the presence of such non-uniformity in diffusion barrier, the thinning areas can usually act as the weakest spots that fail to effectively prevent Cu out-diffusion under external stresses. This is especially troublesome when moisture or oxygen is trapped in PLK to provide oxidation driven potential inducing Cu to diffuse out. Such a failure mechanism has been demonstrated by a recent thermal annealing experiment where oxidized Cu is observed in PLK matrix in the areas adjacent to the diffusion barrier in fully

executed Cu interconnect patterns [107]. Secondly, as has been reported in structures including metal-dielectric-metal sandwich [108-110], as well as Cu/low-k interconnects [111-113], the interface roughness may also lead to a locally concentrated electrical field when an external bias is applied, resulting in the increase of leakage current, and ultimately, the degradation of device lifetime. In an even worse situation when the diffusion barrier deposition is not well controlled, structural defects such as pinholes and microcracks can be developed. Even if the as-deposited diffusion barrier is intact, the subsequent series of mechanical stress cycles from CMP and thermal residual stress developed during thermal cycles (from film deposition and annealing) due to the large mismatch of coefficient of thermal expansion (CTE) between PLK and metal lines, may also result in such diffusion barrier defects. The presence of such defective barrier has also been evidenced by a recently developed voltammetry technique [114-117]. In such a case, Cu is directly exposed and readily diffuses out into adjacent PLK. All these situations are potentially threatening the reliability of Cu/PLK interconnects.

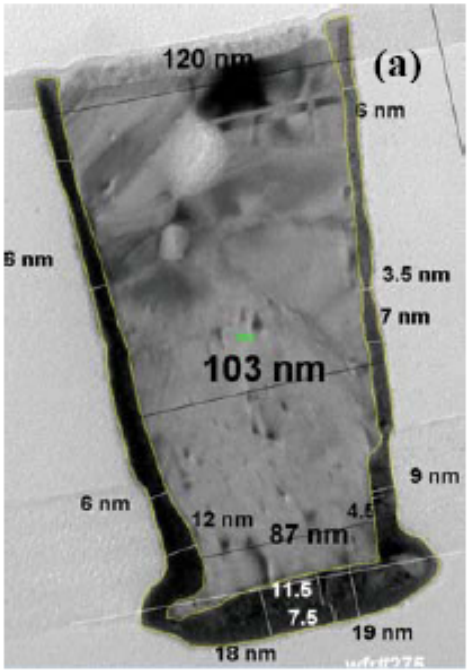


Figure 1.8 A TEM picture showing the non-uniformity of the via diffusion barrier film deposited by SIP-PVD technique

1.3.2 Chemical Impurity and Moisture Contamination in PLK

The incorporation of pores is greatly helpful in reducing dielectric constant of low-k materials yet at the same time dramatically degrades their mechanical, chemical, thermal and electrical strength. These inferior properties make PLK tend to be instable when subjected to external stresses.

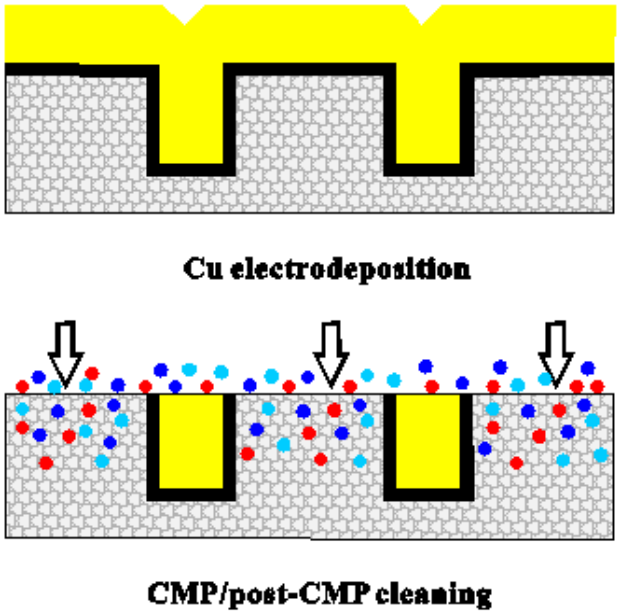


Figure 1.9 A schematic plot showing the impurity contamination possibly introduced during CMP and post-CMP processes

Due to the small physical size of trench and via lines, plasma-based etching are widely used for dielectric etching in advanced Cu/PLK interconnects by virtue of their capability of anisotropic etching and small feature size definition. Because of the concerns regarding moisture uptaking of PLK during wet chemical cleaning, plasma-based ashing is also used as a dry cleaning process to remove the residues after PR strip and etching. The involvement of ionic bombardment and the possible chemical reaction between PLK and the ionized species in plasma-based treatments, however, can significantly degrade the properties of PLK [118-128]. Although low-k materials are designed to reduce moisture adsorption by incorporating

hydrophobic groups such as CH_3 (see section 1.2.3), oxygen plasma etching/ashing has been found to oxidize most of low-k materials, removing hydrophobic components such as Si-H and Si-CH_3 bonds, forming hydrophilic silanol group (Si-OH) and making PLK become hydrophilic and thus prone to moisture uptaking in the subsequent processes when directly exposed to humid environment [127, 128].

Due to its open pore nature, PLK also readily traps chemical impurities (including moistures). This contamination issue can possibly take place via a few fabrication processes such as plasma-based treatments, CMP and post-CMP cleaning. CMP is a planarization process accomplished by a combination of chemical and mechanical interaction between the polishing chemical slurry and the material that needs to be removed. In CMP, the excessively electroplated Cu and the underlayer diffusion barrier are sequentially removed such that the wet chemical slurry directly contacts and easily diffuses into PLK through its open pores, as schematically depicted in Figure 1.9. Such trapped impurities and moisture may not only increase the dielectric constant and the leakage current of PLK but also cause the corrosion of metallic wires, giving rise to another reliability concern in Cu/PLK interconnects. As even higher porosity is required to further reduce dielectric constant in future technology nodes, pores in PLK are expected to be highly interconnected. In such a case, impurity contaminants will be easier to diffuse into PLK matrix, causing even more severe and problematic reliability issues in Cu/PLK interconnects.

1.4 Objective of This Study and Organization of This Thesis

As mentioned earlier, although studies on the leakage current behavior and conduction mechanism in PLK in Cu/PLK interconnects have been extensive and various conduction mechanisms ranging from electrode controlled to bulk-controlled (see Appendix A) have been suggested, the influence of extrinsic factors such as impurities and moisture trapped in PLK and the defective diffusion barrier, which are expected to impact the leakage current behavior and conduction mechanism in PLK, are not considered in available literature, probably due to the

difficulties in detecting such extrinsic factors. As a voltammetry method has been developed to characterize the diffusion barrier in previous studies, the first objective of this study is, therefore, to develop a practical method to characterize the presence of impurities trapped in PLK in Cu/PLK interconnects. The second objective, which is also the primary focus of this study, is to investigate the impact of such extrinsic factors on the leakage current and reveal the associated mechanism.

Whereas the voltammetry technique for diffusion barrier characterization has been introduced in details elsewhere, chapter 2 will first introduce the basic working principle of the voltammetry technique, including the previously developed for diffusion barrier characterization and its new variation for impurity and moisture detection developed in this study, followed by the description of experimental samples that will be used and their voltammetry characterization results. Chapter 3 is devoted to the investigation on the influence of Cu out-diffusion on the leakage current behavior of PLK in the presence of electrical field. Revealing the characteristic feature of Cu out-diffusion in the leakage current and understanding the associated mechanism are the major foci in this chapter. With the understanding of the impact of Cu out-diffusion in the leakage current, a simple yet practical method named step mode I-t technique, is developed in chapter 4 to further study the electrical stress induced Cu out-diffusion. In chapter 5, the moisture effect on the leakage current behavior and the associated mechanisms will be investigated. To summarize this study, chapter 6 will present the conclusions and future work.

CHAPTER 2

VOLTAMMETRY TECHNIQUE AND EXPERIMENTAL SAMPLE CHARACTERIZATION

2.1 Introduction

To investigate the influence of extrinsic factors on the leakage current behavior and conduction mechanism in PLK, the presence of extrinsic factors needs to be decisively evidenced. Due to its small pitch size, however, the detection of extrinsic factors in advanced Cu/PLK interconnects is extremely difficult. Adding more difficulties and complexities to the characterization method is the possible coexistence of multiple extrinsic factors from various sources discussed in chapter 1. For diffusion barrier defects, a practically routine characterization method is the conventional transmission electron microscope (TEM) technique. The advantage of TEM lies in the fact that it possesses the capability of physically visualizing the defects with extremely small size, owing to its high resolution capability in current microscope technology. Ironically, for the same reason, TEM is intrinsically limited to small area feature scan and loses the effectiveness in large-scale characterization. Therefore, TEM is time-consuming and not suitable for the characterization of diffusion barrier defects because pinholes and cracks may be localized in the tiny defective spots in a massive area of barrier films. Detection difficulties also apply to the characterization of trapped impurities in PLK by conventional methods. Secondary ion mass spectrometry (SIMS) is applicable to blanket wafers but not fully patterned interconnects, again because of their small pitch size. Other common techniques such as energy dispersion X-ray analysis (EDX) and Auger electron spectroscopy (AES) are limited by their detection resolution. Other than these mentioned above, the particular characterization difficulty that may be encountered come from the possibility that the impurities have the same elements as PLK. In such a case, characterization and quantification of trapped impurities by conventional methods become practically impossible.

In order to characterize defective diffusion barrier, new techniques are needed. For this purpose, a voltammetry technique has been introduced and proven to be very simple yet effective in detecting defective barrier in fully patterned Cu/PLK interconnects. In this technique, the PLK is first fully infiltrated with dilute electrolyte, e. g. 2wt% KCl solution, and the characteristics of diffusion barrier are reflected in a voltammogram achieved by a simple current-voltage measurement. In this study, the voltammetry technique is further extended to characterize chemical impurities trapped in PLK. However, instead of dilute electrolyte, degassed deionized (DI) water is used as infiltration medium in the newly extended voltammetry technique. Due to the conductivity change of PLK matrix by DI water activated impurities, the presence of impurities in PLK can also be reflected in the voltammogram variation and thus simply detected.

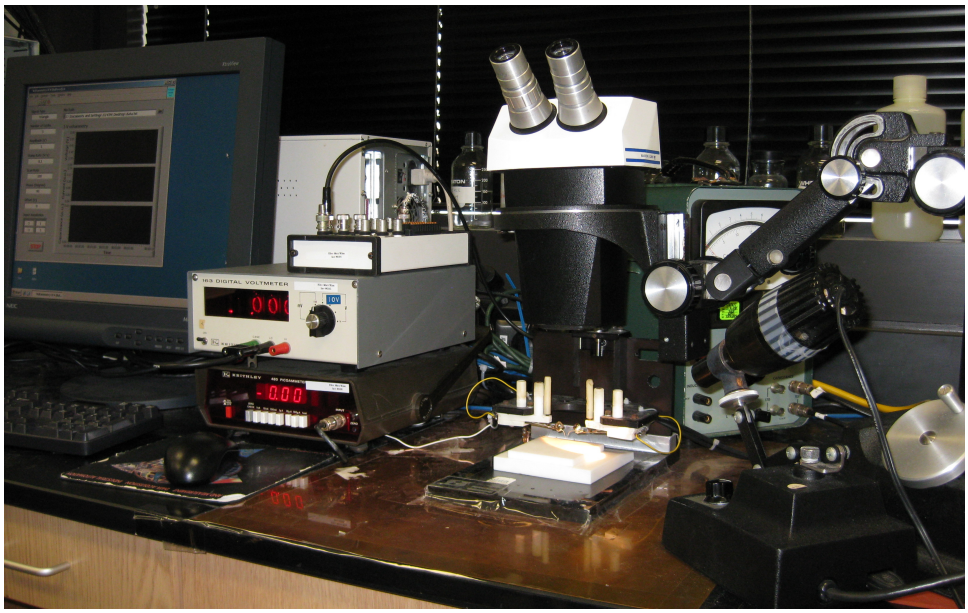
In this chapter, the working principle of voltammetry technique will be introduced first. Although the voltammetry technique for diffusion barrier characterization has been developed and introduced elsewhere, its working principle will be detailed first in this chapter because it will be used as a tool throughout this study. This is also helpful to understand the newly developed voltammetry technique for impurity characterization. The experimental samples will then be described and characterized by voltammetry technique at as-received condition.

2.2 Voltammetry Technique: Barrier Defect and Impurity Characterization

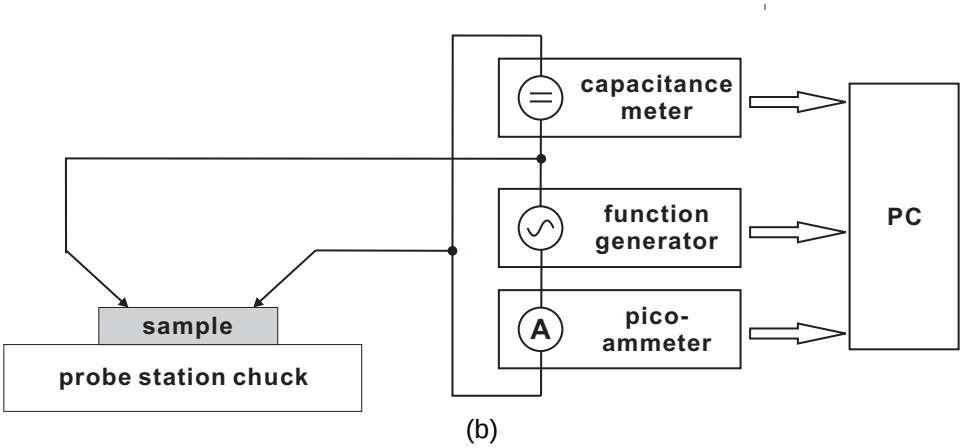
2.2.1Voltammetry Apparatus

Voltammetry setup consists of a function generator, a picoammeter, a capacitance meter, a probe station and a personal computer. Figure 2.1 displays the picture of the home-made voltammetry setup and a schematic plot showing the electrical connections between its major components. The electrical connection between the testing sample and the external circuit is established through two tiny needle probes contacting to a pair of bond pads on the sample. The capacitance meter is used to assure good electrical contact between probes and bond pads. The function generator produces cyclic voltammetry potential applied to the sample

and the resultant current response is detected by the picoammeter. The potential, resultant current response and capacitance are recorded and saved in the PC programmed with a labview-based interface.



(a)



(b)

Figure 2.1 (a) a picture of voltammetry setup and (b) a schematic plot showing the electrical connections between its major components

2.2.2 Characterization of Defective Barrier Films

2.2.2.1 Working Principle and Voltammogram Examples [114-117]

The working principle of voltammetry technique in defective barrier characterization is based on the fundamentals of electrochemistry. This technique takes the advantage of the fact that dilute electrolyte, e. g. 2wt% KCl solution, can penetrate into PLK in the standard interconnect test structure, i. e. comb or serpent pattern, essentially turning it into a two-electrode electrochemical cell where the interdigitized mating metal lines serve as the electrodes, as seen in Figure 2.2. The purpose of using dilute electrolyte is to minimize the electrolyte induced corrosion of the diffusion barrier yet makes the water electrically conductive so that when electrochemical reaction takes place the reaction current can be sustained. After PLK is fully infiltrated with electrolyte (see section 2.4 for the determination of full infiltration stage), a cyclic potential is applied to the electrodes. Typically, the applied potential starts from an initial linear sweep from 0 to +0.7V, followed by a full reverse sweep from +0.7V to -0.7V and a full forward from -0.7V to +0.7V, as shown in Figure 2.3. This potential sweep is repeated for a number of cycles during which the current response from the test pattern is simultaneously monitored. The acquired I-t and V-t data is then replotted into I vs. V curve, resulting in an I-V voltammogram from which the conditions of diffusion barrier can be characterized.

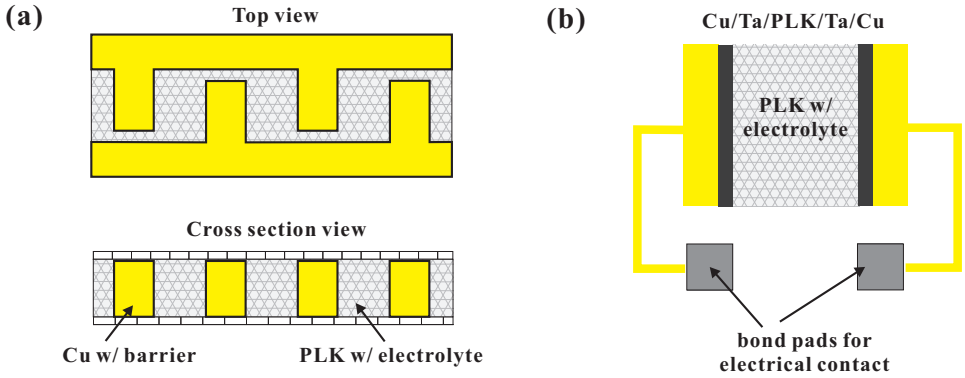


Figure 2.2 Schematic plots showing (a) top view and cross-section view of a comb structure, and (b) its two-electrode electrochemical cell model.

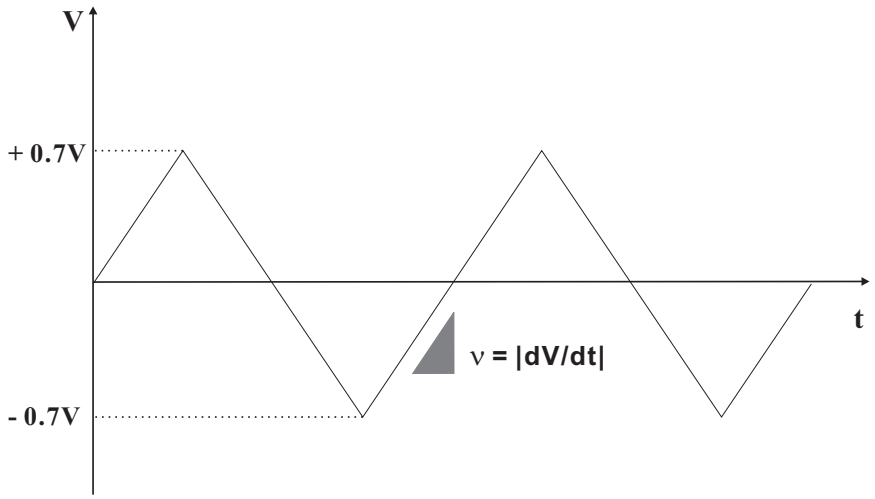


Figure 2.3 The cyclic potential profile in voltammetry technique. The linear sweeping (ramping) rate is defined as $\nu = |dV/dt|$

Typically, two categories of voltammograms can be observed. The first one is a simple symmetrical I-V hysteresis as exemplified in Figure 2.4. This type of I-V response indicates that the diffusion barrier is defect-free without Cu exposure. In this case, due to the electrochemical inertness of diffusion barrier films such as Ta and TaN, there is no electrochemical reaction taking place upon the application of cyclic potential, and therefore, the current response is simply a result of the polarization of infiltrated mobile ions, i. e. K^+ and Cl^-, in the electrolyte. Under the influence of electrical field that varies with time, these ions move back and forth in PLK, giving rise to the drift current. Simultaneously as they move, mobile ions are accumulated toward the electrodes, resulting in ionic concentration gradient and thus diffusion current. These two current components, the drift current driven by the applied electrical field and the diffusion current driven by the concentration gradient, are involved together with the voltage ramping rate (that determines the variation rate of the electrical field) to determine the kinetics of overall current response.

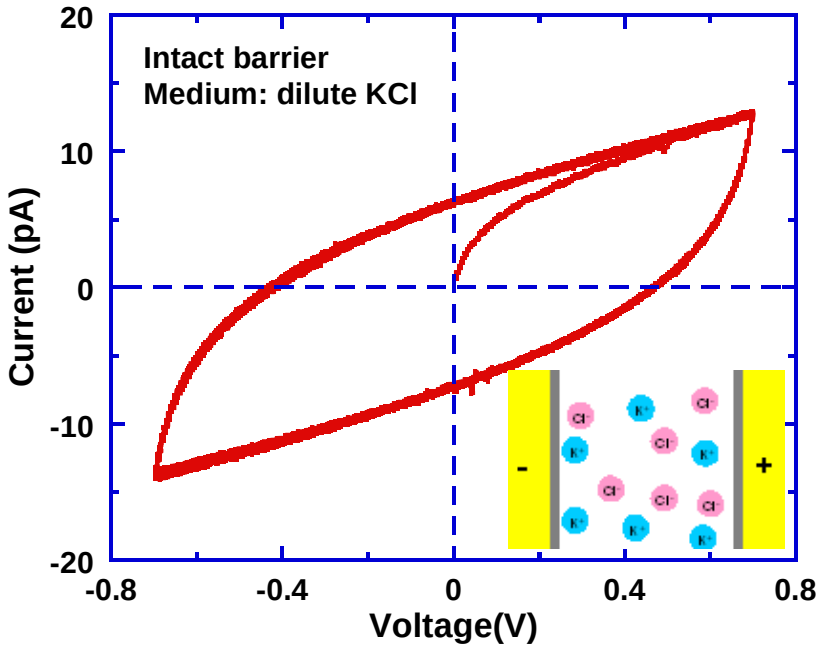


Figure 2.4 A typical voltammetry hysteresis from the samples with intact diffusion barrier after dilute KCl infiltration

When the barrier films are defective with Cu directly exposed to the infiltrated electrolyte, the current response, however, is distinctively different from the one shown in Figure 2.4. In this case, Cu redox reactions take place at some specific potential, resulting in an extra reaction current component in addition to the ionic (polarization) current. Possible Cu electrochemical reactions include

(1) Cu oxidation into cuprous ions

$$Cu \leftrightarrow Cu^{+} + e \ (E^{0} = 0.52V) \qquad (2.1)$$

(2) Cuprous ion oxidation into cupric ions

$$Cu^{+} \leftrightarrow Cu^{++} + e \ (E^{0} = 0.15V) \qquad (2.2)$$

(3) Cu oxidation into cupric ions

$$Cu \leftrightarrow Cu^{++} + e \ (E^{0} = 0.34V) \qquad (2.3)$$

where E^0 represents the standard reaction potential relative to the standard hydrogen electrode. The positive sign in the standard potential indicates that in order to induce Cu oxidation reaction (in forward direction in above reaction equations) a positive potential relative to the hydrogen electrode must be provided.

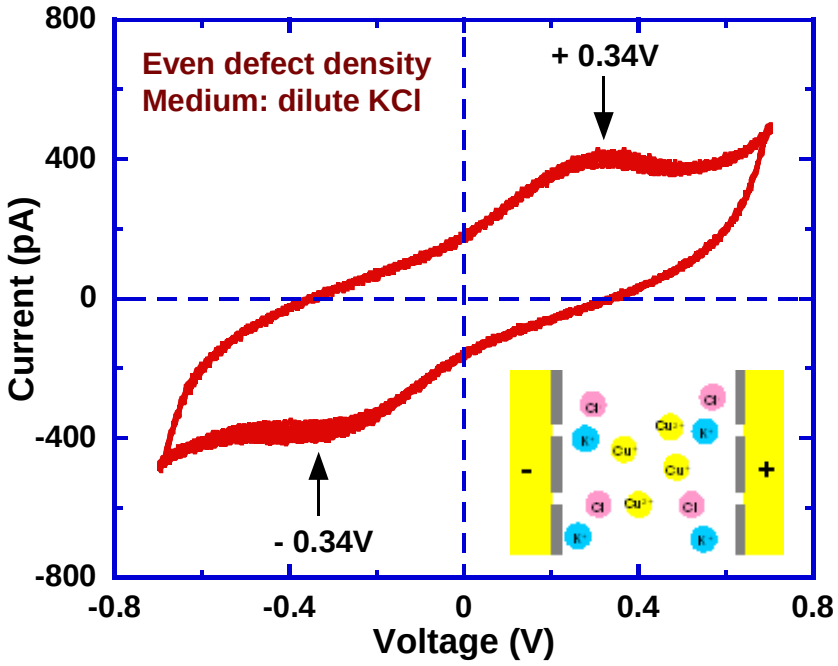
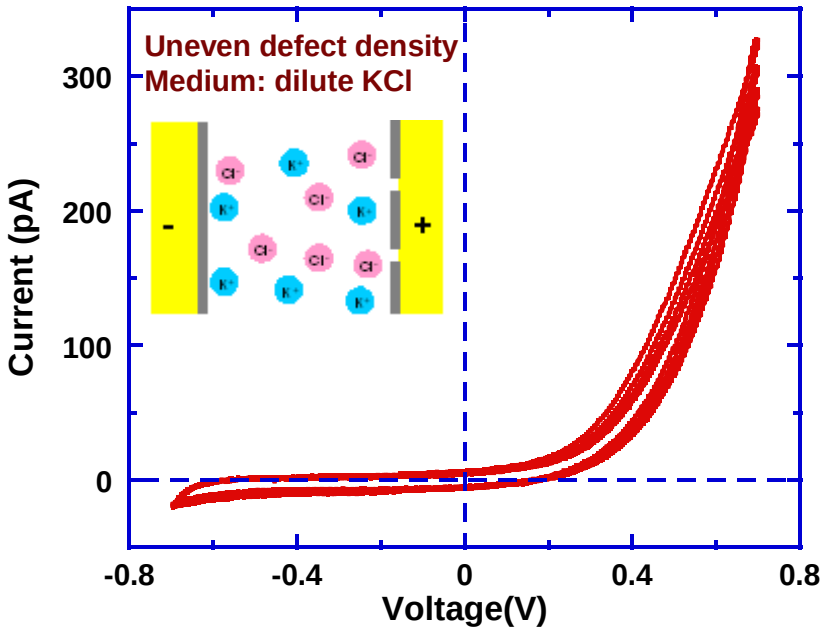


Figure 2.5 An example of I-V hysteresis from the samples with comparable areal density of exposed Cu on the two electrodes

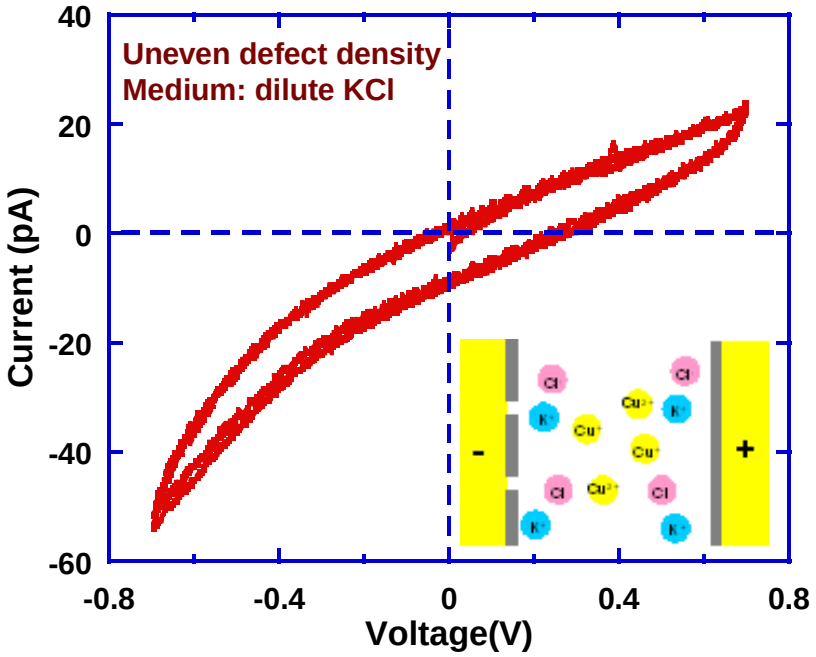
With the additional Cu reaction current, current peaks usually appear in the I-V hysteresis. A voltammogram example from patterns with defective diffusion barrier is shown in Figure 2.5 where current peaks symmetrical with respect to zero potential are clearly seen at ~+/-0.34V (indicated by the arrows). A hysteresis with this shape can be observed only in a specific case that the diffusion barrier films at the two electrodes have comparable areal density of defect, which, however, does not appear frequently in fully patterned Cu interconnects. The most frequently observed hysteresis is asymmetrical, as exemplified in Figure 2.6. These voltammograms correspond to uneven areal density of barrier defect at the two electrodes. The

current long tail on the positive potential side indicates that the initial positively biased electrode has a higher areal density of barrier defect than the other, as in Figure 2.6 (a), while the current long tail on the negative potential side suggests that the initial positively biased electrode has a less areal density of barrier defect than the other, as in Figure 2.6 (b). As has been detailed in Ref. [116], this is because in the present two-electrode electrochemical cell configuration, the total current is primarily controlled by the Cu oxidation reaction that happens only at the electrode whose potential is higher relative to the other, as seen from Reactions (2.1) to (2.3). When the electrode with a larger defective area is initially positive relative to the other, more Cu is exposed to the electrolyte and readily supplied for oxidation reaction, resulting in higher density current. Notice that the electrodes will exchange their polarities as the applied voltammetry potential evolves (see the voltammetry potential profile in Figure 2.3). Therefore, when the applied potential becomes negative, the initial anode (the one with larger exposed Cu area) becomes the cathode and the initial cathode (the one with smaller exposed Cu area) becomes the anode. While this occurs, the electrode with lower areal density of barrier defect has higher potential with respect to its counter electrode. Since at this stage the current-controlling process, i. e, the Cu oxidation reaction, takes place at the electrode with smaller exposed Cu area, the resultant current is much smaller because less Cu is supplied for oxidation reaction. This explains the current long tail on the positive potential side shown in Figure 2.6 (a). In the reversed case such that the electrode with less areal density of barrier defect is initially positively biased, the same analysis can be applied to explain the current long tail on the negative potential side shown in Figure 2.6 (b).

With this understanding, the qualitative analysis of barrier defect at the two electrodes can be obtained by the voltammetry hysteresis. This is rather simple and especially useful in studying the diffusion barrier failure induced by the applied electrical stress, as will be more detailed in chapter 4.

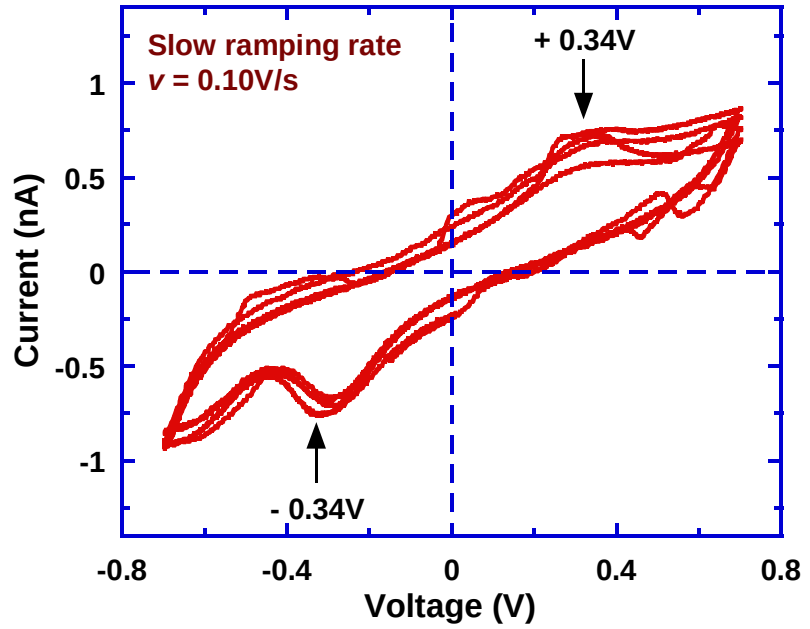


(a)

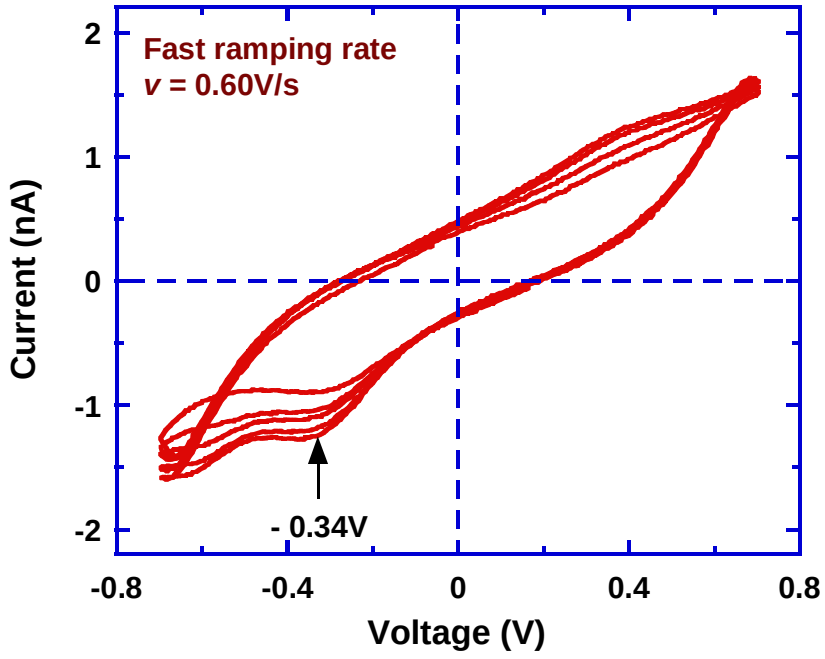


(b)

Figure 2.6 Examples of asymmetrical hysteresis due to the uneven defective areal density on the two electrodes



(a)



(b)

Figure 2.7 A comparison of hysteresis showing the ramping rate effect: (a) a slow ramping rate at 0.10V/s and (b) a fast ramping rate at 0.60V/s.

2.2.2.2 Ionic Current and Reaction Current

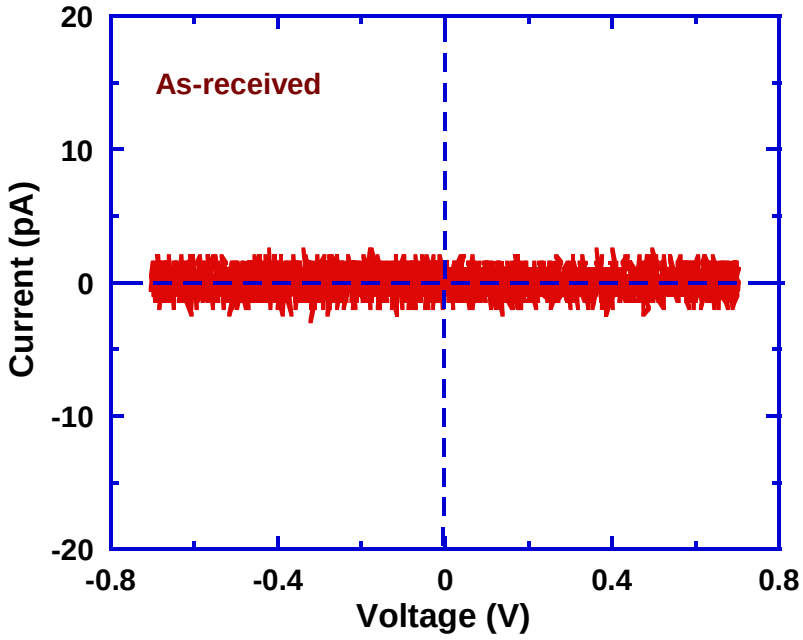
As discussed earlier, in the case of defective barrier, there are two current components contributing to the total current: the ionic current and the reaction current. While the reaction current initiates at some specific potential and is proportional to the area of exposed Cu at the electrodes, the ionic current increases with the increase of potential ramping rate. If the ionic current is dominant over the reaction current, reaction current peaks may not be observed even if Cu reaction takes place. This is especially true when the area of barrier defect is tiny such that the reaction current is too small to be visualized. Therefore, in order to improve the resolution of voltammetry technique, extreme care should be taken when conducting diffusion barrier characterization. Generally, fast ramping rate is not encouraged because it usually gives rise to high ionic current. Figure 2.7 (a) and (b) compares the voltammograms taken from the same pattern measured at two different ramping rates. It is seen in Figure 2.7 (a) that the two reaction current peaks at ~+/-0.34V can be clearly observed at slowing ramping rate 0.10V/s. However, when the ramping rate is increased to 0.60V/s, the current peak at +0.34V is almost invisible although Cu reaction does occur at this voltage. Under normal circumstances, a raping rate at 0.05V/s is slow enough to capture the signal of reaction current, and generally, this ramping rate is used in this study when diffusion barrier characterization is needed.

2.2.3 Characterization of Impurities Trapped in PLK

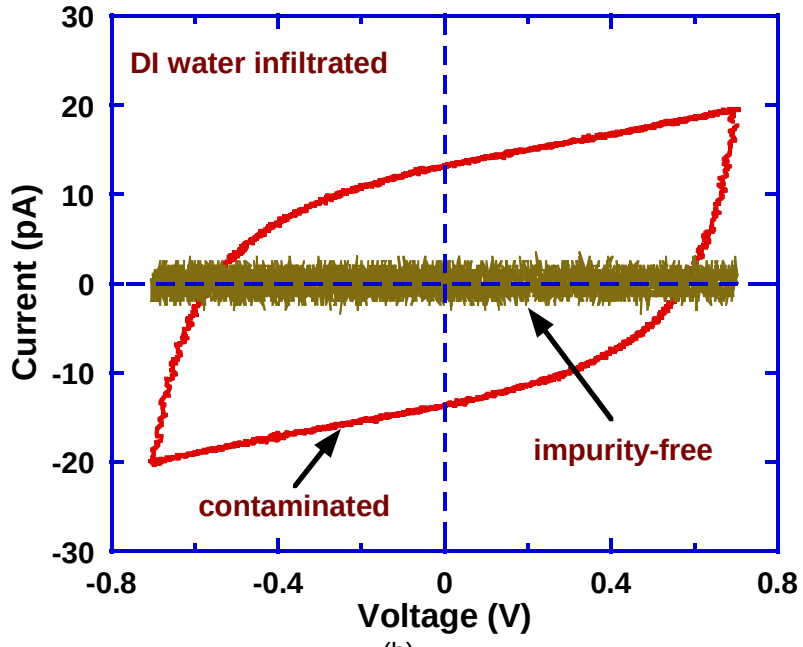
Similar to electrolyte, degassed DI water is able to penetrate into PLK matrix as well. If, however, when there is a sizable amount of water-soluble impurities trapped in PLK, DI water, although not electrical conductive alone, may activate and mobilize the trapped impurities, essentially turning itself into conductive electrolyte. The infiltration of DI water in such a case is therefore not much different from the infiltration of dilute electrolyte. Upon the application of cyclic potential, the current responses from as-received and infiltrated patterns are expected to be different, if impurities are trapped in PLK. Thus, by a simple comparison of the hysteresises at as-received and infiltrated conditions, whether impurities present in PLK can be determined.

This is the whole ideal based on which the voltammetry technique is extended to characterize chemical impurities trapped in PLK in fully patterned Cu/PLK interconnects [129].

The experimental procedures for impurity characterization are similar to these of diffusion barrier characterization. Voltammetry measurement is usually performed on the as-received sample prior to DI water infiltration to obtain the reference hysteresis. After DI water infiltration, voltammetry measurement is carried out again. Sample characterization is then done simply by comparing the hysteresis at infiltrated condition with the reference hysteresis. A characterization example is shown in Figure 2.8 where the hysteresises from as-received and infiltrated samples are demonstrated in (a) and (b), respectively. At as-received condition, the I-V curve is flat with negligible current due to the low electrical conductivity of PLK. After DI water infiltration, two completely different hysteresis behaviors may be observed, as seen in Figure 2.8 (b). The first one is similar as the one measured at as-received condition while in the second type the current magnitude dramatically increases and a sizable hysteresis appears. The reason for the different I-V responses is simple to understand. When PLK is free from impurities, the current response does not show any measurable change compared to that at as-received condition because the infiltrated DI water remains electrically non-conductive and the current is predominated by the small leakage current. In contrast, when PLK contains a large amount of water-soluble impurities, the I-V curve becomes a symmetrical hysteresis because the infiltrated DI water can react with trapped impurities, producing mobile ions. With defect-free Ta electrodes, no electrochemical reaction takes place upon the application of cyclic potential and the current is dominated by the polarization current that has been discussed earlier. This is exactly the same case as patterns with intact diffusion barrier infiltrated with dilute KCl solution (see Figure 2.4).



(a)



(b)

Figure 2.8 An example showing the impurity characterization by voltammetry technique: (a) as-received samples; (b) infiltrated samples.

It should be noted that the voltammograms exemplified above are only a few limited cases. More I-V behaviors may appear in fully patterned Cu/PLK interconnects, depending on the conditions of diffusion barrier and PLK. For example, if the diffusion barrier is defective and PLK is contaminated, Cu redox reactions can also happen, resulting in similar I-V hysteresis elaborated earlier (see Figure 2.5 - 2.7). In another case where there are water-soluble impurities and moistures trapped in PLK, sizable I-V hysteresis can be observed from patterns even at as-received condition. Such I-V behaviors will be seen in the later section where the experimental samples used in this study are characterized.

When combined with a theoretical model, the extended voltammetry technique can go beyond impurity detection. Since the hysteresis current is a reflection of impurity concentration and their diffusivity in PLK, the variation of potential sweeping rate will give different hysteresis current as well as different shapes. By modulating the current flow using different sweeping rates and combining with proper modeling, the concentration of mobile ions and their diffusivity in PLK can be extracted from experimental data. The theory for the extraction of impurity concentration and their diffusivity is beyond the scope of this dissertation. More details can be found in Ref. [130].

Finally, it should be pointed out that although voltammetry technique is successful in detecting the presence of water-soluble impurities trapped in PLK and quantifying their amount when combined with an appropriate model, identifying the impurity species is currently beyond its capability. Further improvement on voltammetry technique is clearly needed.

2.3 Experimental Samples

Samples used in this study were standard interconnect comb patterns taken from fully executed dual-damascene Cu interconnect test wafers in courtesy of various industry companies. Due to its structural simplicity, the comb pattern can be modeled as a two-electrode capacitor (see Figure 2.2) and has been commonly used as the testing structure for fundamental studies.

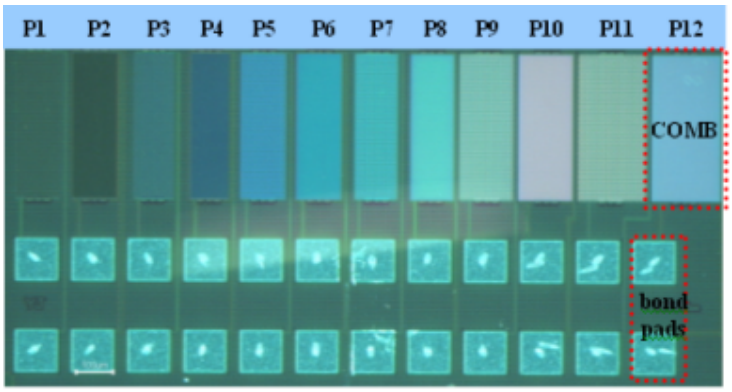


Figure 2.9 The optical image of a MSSQ wafer I unit. The odd-numbering patterns are located in level one and the even-numbering patterns are in level two.

Table 2.1 Geometry of MSSQ I patterns

	P1/P2	P3/P4	P5/P6	P7/P8	P9/P10	P11/P12
Cu line width (nm)	175	250	250	250	350	450
PLK space (nm)	225	200	300	350	400	500

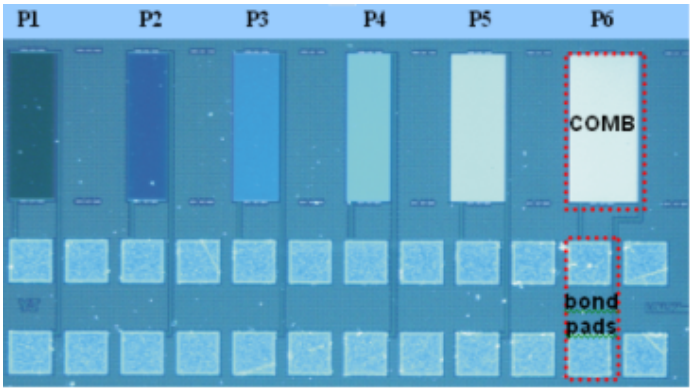


Figure 2.10 The optical image of a MSSQ wafer II unit

Table 2.2 Geometry of MSSQ II patterns

Pattern	P1	P2	P3	P4	P5	P6
Cu line width (nm)	175	250	250	250	350	450
PLK space (nm)	225	200	300	350	400	500

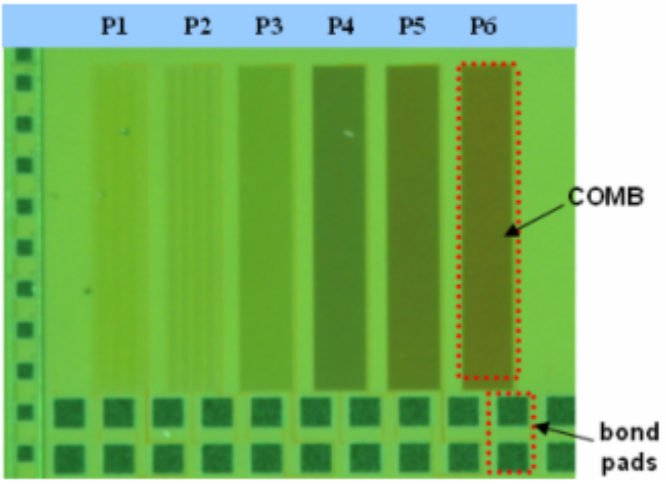


Figure 2.11 The optical image of a SiCOH wafer unit with six patterns and their bond pads

Table 2.3 Geometry of SiCOH patterns

Pattern	P1	P2	P3	P4	P5	P6
Cu line width (nm)	70	70	70	70	70	70
PLK space (nm)	1235	585	260	150	95	60

Two types of PLK materials have been used in this study. The first type is spin-on MSSQ PLK processed by SEMATECH with nominal porosity ~45% and a dielectric constant ~2.4. The second is PECVD processed SiCOH PLK by Texas Instruments with nominal porosity ~35-40% and dielectric constant k ~ 2.4-2.6. Other than the difference in PLK materials and their process techniques, both PLK samples are structurally similar: a ~10nm PVD processed Ta film is used as diffusion barrier; after completion CMP process, a ~10-20nm SiCN layer is deposited by PECVD as capping layer, on top which is another layer of dielectric passivation, followed by a metallic TaN/Al stack as bond pads to establish electrical contact between buried comb patterns and external circuits.

Two different MSSQ wafers have been tested. MSSQ wafer I is a two-level interconnect structure with six patterns on each level. MSSQ wafer II is also a two-level structure but the

bottom level is empty while the top level is patterned. All the comb patterns in both wafers have roughly the same pattern density (defined as the ratio of the Cu line width to the PLK space). The optical images of wafer units from MSSQ wafer I and wafer II are displayed in Figure 2.9 and Figure 2.10, respectively, and their pattern geometry, i. e. the Cu line width and the PLK space, is tabulated in Table 2.1 and Table 2.2, respectively. SiCOH wafers have a simple one-level structure. Each wafer unit also has six comb patterns that have fixed Cu line width (~70nm) but varying PLK space and thus varying pattern density. The optical image of a SiCOH wafer unit is shown in Figure 2.11 and the pattern geometry is tabulated in Table 2.3.

2.4 Characterization of Experimental Samples

2.4.1Determination of Infiltration Condition

In voltammetry technique, one of the important steps is to determine the infiltration condition of samples so that full infiltration is reached prior to voltammetry characterization. This is critical because only at full infiltration stage can the accuracy of characterization be ensured. This is understandable because infiltration into PLK is essentially a diffusion process [117, 131], infiltration without reaching full saturation obviously means that not all the trapped impurities are activated (for impurity characterization) or not the whole area of diffusion barrier is contacting with electrolyte (for diffusion barrier characterization), both of which will lead to inaccurate characterization of experimental samples.

An example to illustrate this point is shown in Figure 2.12 where the hysteresis change as DI water infiltration proceeds can be clearly seen. This result is taken from a MSSQ I pattern that will be seen later to have a large amount of impurities trapped in PLK. At the initial stage of infiltration, only a small fraction of trapped impurities participate the current delivery in the PLK in response to the voltammetry potential, and therefore, a relatively small hysteresis shows. With infiltration gradually proceeding, the hysteresis is continuously enlarged because more impurities are activated and involved in the current transport. The hysteresis enlargement

continues till the PLK is fully saturated with DI water. At this stage, the hysteresis is saturated because all the trapped impurities are activated and involved in the current transport.

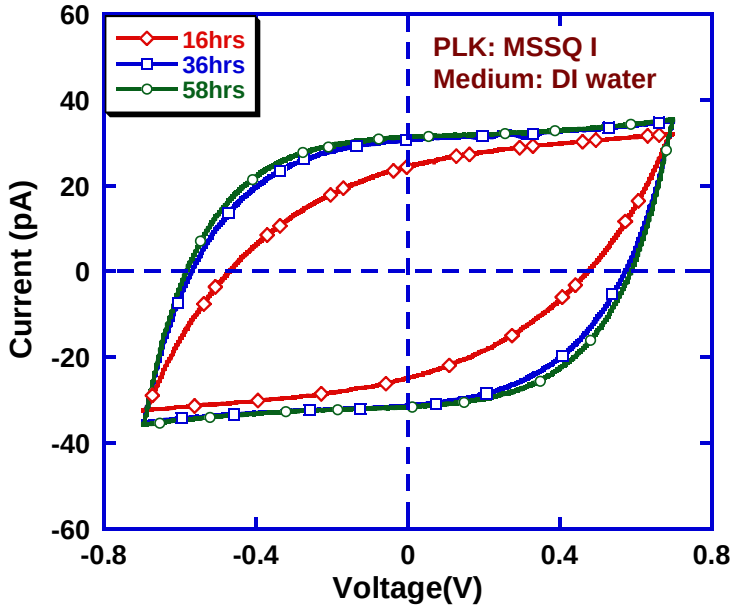


Figure 2.12 A plot showing the hysteresis change of a MSSQ I pattern as DI water infiltration proceeds

The result shown here also presents a way to determine the full infiltration condition of samples. Experimentally, samples are soaked in DI water or dilute electrolyte for infiltration to take place. Voltammetry measurement is then constantly carried out on selected samples with intact diffusion barrier. Continuous enlargement of hysteresis shown in Figure 2.13 will typically be observed. Once the saturation of hysteresis current is observed, the full infiltration of samples is determined. For samples used in this study, SiCOH PLK usually takes ~24 hours to reach full saturation and MSSQ PLK (including both wafer I and II) takes ~48 hours.

2.4.2 Characterization of Experimental Samples

2.4.2.1 SiCOH Samples

A large number of SiCOH PLK samples, totaling 72, were tested to gain statistical evaluation. At as-received condition, no noticeable current was observed. However, with DI

water infiltration, all the testing samples showed standard symmetrical hysteresis, as seen in Figure 2.13. A few important inferences can be made from this observation. The first indication is that water-soluble impurities are trapped in SiCOH PLK. This reason has been explained in the section 2.1. Secondly, moisture contamination is absent or at least too small to be measured by voltammetry because if so, noticeable hysteresis is expected to be observed at as-received samples. Furthermore, since the infiltrated DI water turns into electrolyte due to its reaction with trapped impurities, the absence of Cu reaction peaks suggests that the diffusion barrier films in SiCOH samples are intact. This conclusion was also confirmed by the additional voltammetry test with 2wt% KCl as infiltration medium.

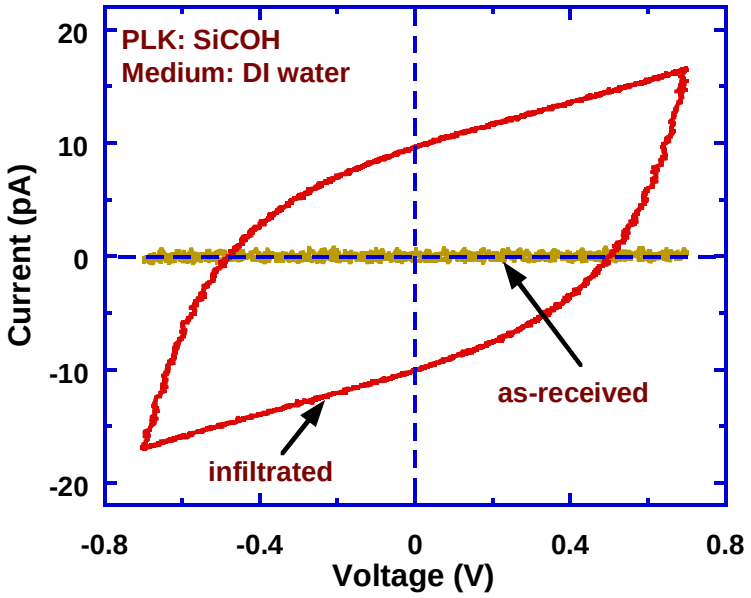
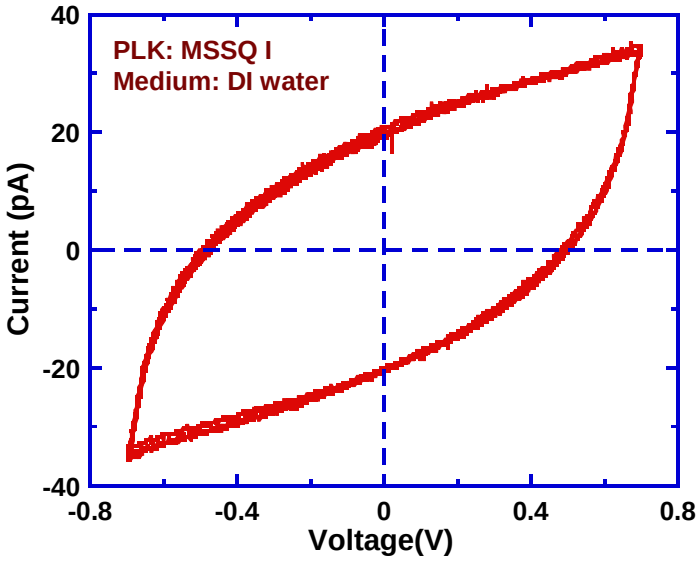


Figure 2.13 The typical voltammetry results from SiCOH samples at as-received condition and DI water infiltrated condition.

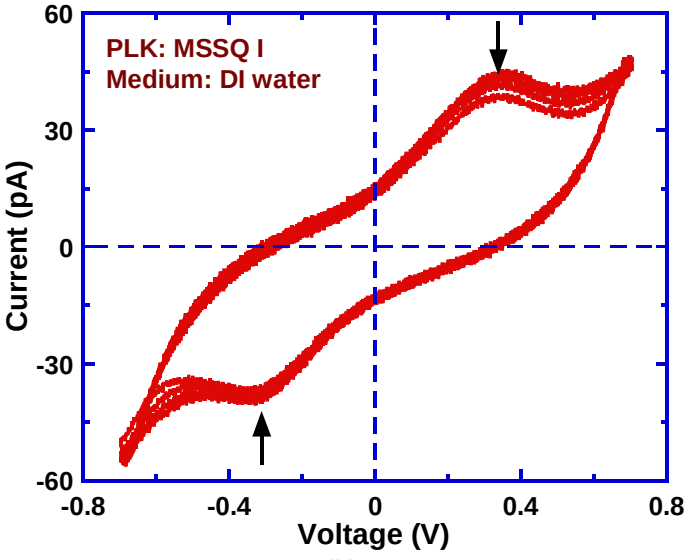
2.4.2.2 MSSQ Wafer I

The PLK and diffusion barrier condition in MSSQ patterns were found to be more complicated that SiCOH wafers. All samples, totally 48, showed sizable hysteresis current even at as-received condition, indicating that MSSQ I wafer have both impurities and moisture

trapped in PLK. In order to further characterize the diffusion barrier, these samples were tested by voltammetry after DI water infiltration till saturation. Among 48 samples, 28 had symmetrical hysteresis and others showed Cu reaction peaks, as seen in Figure 2.14 (a) and (b), respectively, indicating that defective diffusion barrier also exists in MSSQ I wafer.



(a)



(b)

Figure 2.14 The voltammetry results from DI water infiltrated MSSQ I samples, indicating: (a) contaminated PLK but intact barrier, and (b) contaminated PLK and defective barrier

Based on statistical results from testing samples, patterns with defective barrier were found to follow two general trends: (1) when tracing the linkage between the barrier condition and the wafer unit location, it was found that defective barrier appeared more frequently in units taken from the wafer edge; (2) within the same sample unit, defective barrier was found more in patterns in the first level. The first trend is expected since it is well known that the diffusion barrier in samples at the wafer edge have inferior step coverage and conformity [132, 133]. Secondly, since the diffusion barrier in the first level patterns undergoes more thermal and mechanical cycles during fabrication process that degrades the barrier integrity, the second trend is also not a surprising result.

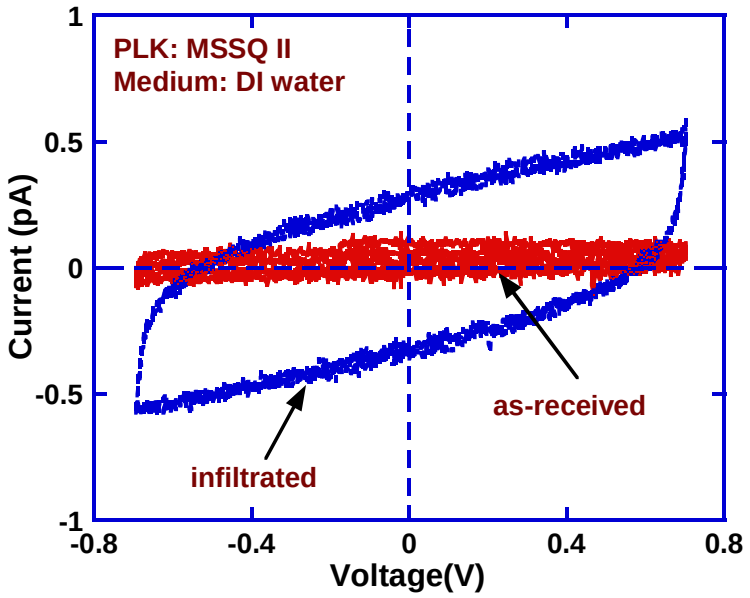
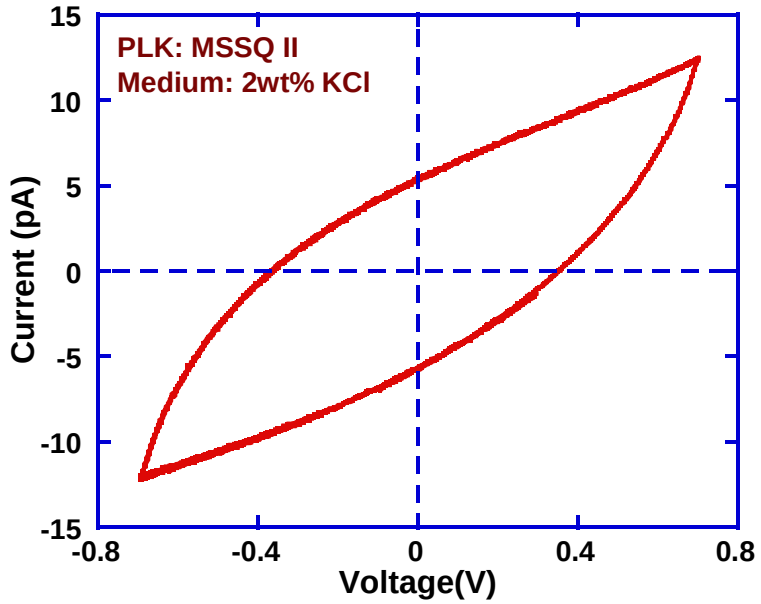


Figure 2.15 The typical voltammetry results from MSSQ II samples at as-received condition and after DI water infiltration.

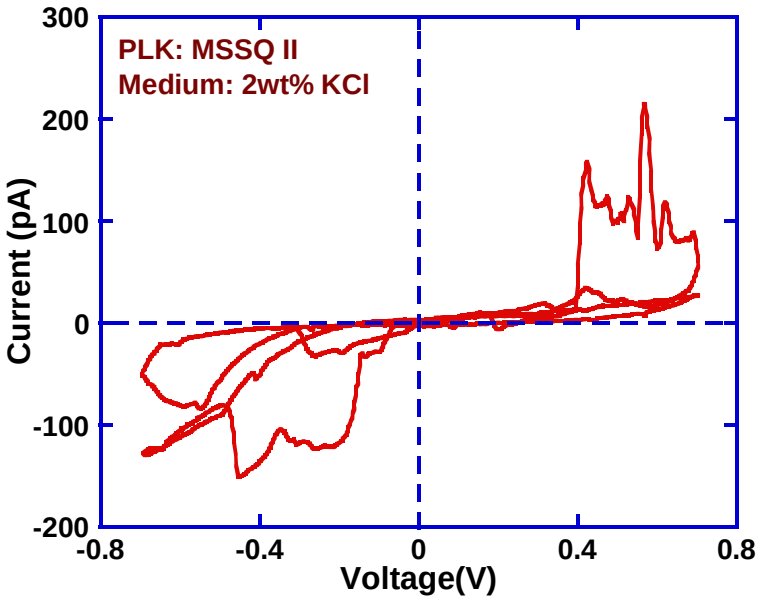
2.4.2.3: MSSQ Wafer II

Figure 2.15 shows the voltammetry measurements from MSSQ wafer II samples at as-received condition and after DI water infiltration. As seen in this plot, an extremely small

hysteresis (~pA scale) can be observed with DI water infiltration, indicating that the MSSQ II samples may be contaminated with water soluble impurities but with an extremely small amount.



(a)



(b)

Figure 2.16 The typical voltammetry results from MSSQ II samples after 2wt% KCl infiltration, indicating (a) intact diffusion barrier; and (b) defective diffusion barrier.

In order to characterize barrier condition, 2wt% KCl solution was used as infiltration medium and the voltammetry characterization results are shown in Figure 2.16. While 16 out of 40 tested samples presented symmetrical hysteresis as in Figure 2.16(a), indicating their diffusion barrier was defect-free, other samples showed Cu reaction current in the hysteresis as in Figure 2.16(b), suggesting that their diffusion barrier was defective.

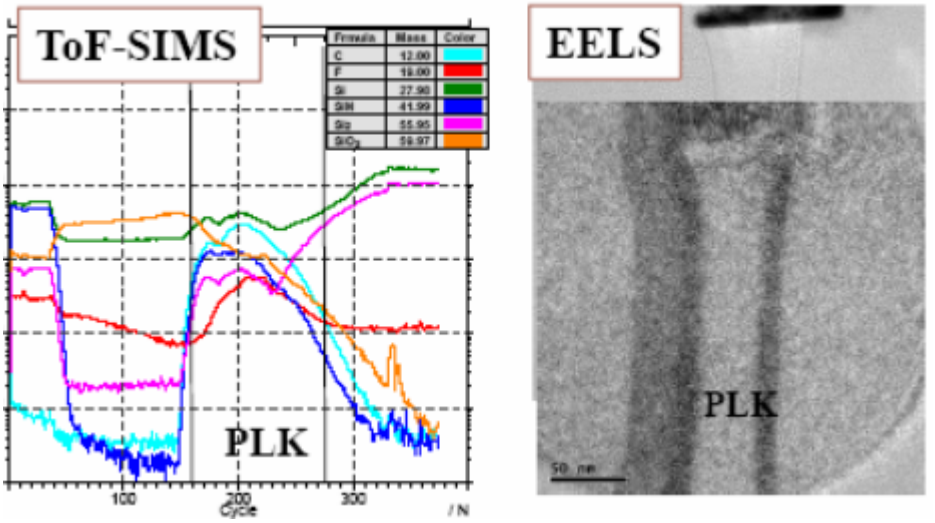


Figure 2.17 ToF-SIMS and EELS results from experimental samples showing a near background level of fluorine signal in the PLK matrix.

2.4.3 Discussion: Impurity Identification and Source

Although the presence of chemical impurities in PLK has been decisively evidenced, the species and sources of these impurities have not been clearly identified. In an attempt to identify the impurity species by time-of-flight SIMS (ToF-SIMS) and electron energy loss spectroscopy (EELS), both techniques indeed found a near background level of fluorine signal, as shown in Figure 2.17. However, due to the intrinsic resolution limitation of SIMS and EELS as well as the possibility that the contaminants share same elements with PLK, other possible contamination species can not be excluded at present stage. The root cause of the contaminants seen in the experimental samples has not been recognized as well. As discussed in chapter, various sources including the chemicals in CMP slurry and the gases used in plasma-based treatments

may contribute to PLK contamination. Without knowing the processing details, finding the source(s) of such contaminants is extremely difficult.

2.5 Summary of This Chapter

In this chapter, the basic working principle of voltammetry technique, including the previously developed and the newly extended, has been introduced. This technique utilizes the fact that electrolyte or degassed DI water can diffuse into PLK matrix, making the standard interconnect test pattern into a two electrode electrochemical cell and thus allowing the characterization of extrinsic factors such as defective diffusion barrier and trapped impurities simply by detecting the current response upon the application of cyclic potential. The typical I-V hysteresises observed in fully patterned Cu/PLK interconnects were exemplified and the associated mechanisms have been elaborated. In addition, two types of PLK samples that will be used in this study, SiCOH and MSSQ, have been described and samples at as-received condition have been characterized by voltammetry technique. The characterization results reveal (1) SiCOH samples do not have defective barrier films and moisture contamination but contains a large amount of water-soluble impurities in PLK; (2) MSSQ I samples not only have defective barrier films but also have impurity and moisture contaminants; and (3) MSSQ II samples are impurity-free yet have defective barrier. Although the presence of impurities has been decisively evidenced, the species of such contaminants and their sources have not been clearly identified. ToF-SIMS and EELS techniques indeed found near background fluorine signal in PLK, other possible contaminants beyond the detection capability of these techniques can not be presently excluded. Without knowing the processing details, identifying the possible sources of contaminants is also difficult.

CHAPTER 3

MECHANISM OF Cu OUT-DIFFUSION INDUCED LEAKAGE CURRENT INSTABILITY

3.1 Motivation and Major Findings

Among many potential threats to the reliability of modern Cu/PLK interconnects, of particular concern is the possible Cu out-diffusion into adjacent PLK that contributes various forms of interconnect failure. Although a thin layer of diffusion barrier is deposited between Cu lines and PLK films to prevent Cu diffusing out, structural defects may be developed in diffusion barrier films, allowing Cu out-diffusion into PLK and eventually resulting in breakdown of Cu/PLK interconnects (see section 1.3).

Since Cu is most likely to enter PLK in the form of positive ion [134-136], Cu out-diffusion and its migration in PLK is expected to play a significant role in the current conduction. While studies focusing on the electrical reliability of dielectrics related to Cu out-diffusion have been extensive [137-152], the impact of Cu out-diffusion on the behavior of leakage current and the associated conduction mechanism, which is fundamental yet practically important, has not been well understood yet. It has been reported in the conventional electrical reliability tests, i. e. time dependent dielectric breakdown (TDDB) and bias temperature stress (BTS), that Cu out-diffusion and its subsequent migration in PLK can be characterized by the bumpy current signals at the early stage of dielectric breakdown [153, 154]. However, in an accelerated test at elevated temperature and high electrical field like TDDB and BTS, several factors may contribute contamination to the experimental results and obscure their correct interpretation. First of all, under normal TDDB test condition ($T > 100^{o}C$ and $E > 1.0MV/cm$), the effect of electrical and thermal stress induced dielectric failure can not be eliminated. As a matter of fact, due to the intrinsic inferior electrical and thermal strength of PLK, dielectric breakdown under thermal and electrical stresses has been proposed to be one of the dielectric failure

mechanisms in the accelerated reliability test [155-164]. Secondly, with high temperature and high stress field, plus the fact that PLK has open pore structure, Cu ions may have high diffusivity when drifting in the PLK matrix. Therefore, monitoring current evolution by normal time-resolution in a long-time reliability test may not be able to capture the characteristic feature of Cu out-diffusion in the leakage current. With these complexities and uncertainties, whether the bumpy current signals reported in previous studies truly arise from Cu out-diffusion remains questionable. The influence of Cu out-diffusion on the leakage current and its associated mechanism thus need to be further explored and better understood.

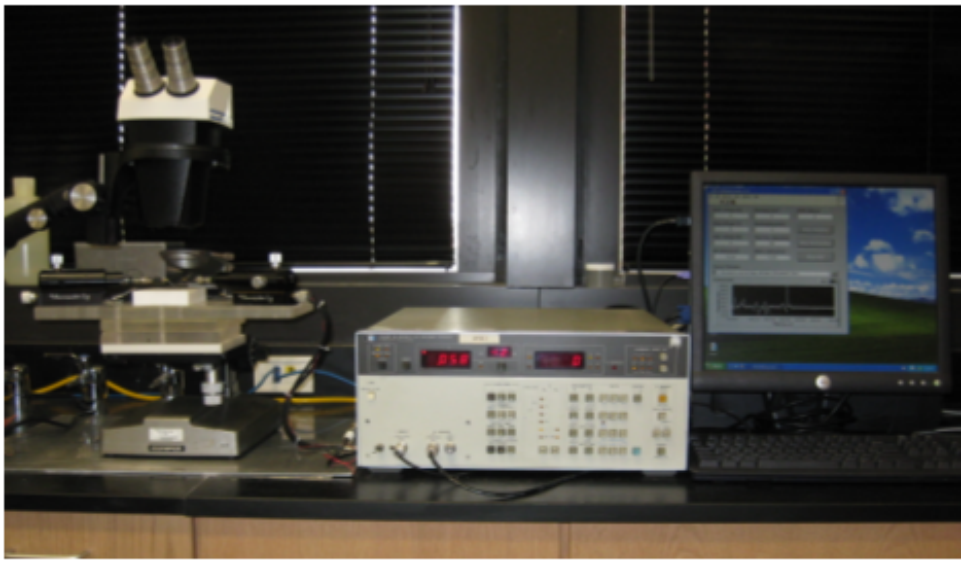
This chapter presents our efforts in the investigation into the influence of Cu out-diffusion on the leakage current behavior and the associated conduction mechanism. The primary means used for this investigation is to monitor the time-dependent leakage current behavior upon the application of a moderate constant electrical stress at room temperature. Under such testing conditions, a unique hump behavior that appears only at low temperature and under moderate electrical stress was observed in the time-dependent leakage current evolution. With the help of voltammetry technique, it was revealed that such current instability could be always associated with Cu out-diffusion without exception. Further analysis discovered that the current hump could be explained by the space-charge-limited (SCL) transient current theory where the current hump arises from Cu out-diffusion and its subsequent migration in PLK in the presence of electrical field. From the proposed transient current theory, the drift mobility of Cu ions in PLKs used in this study was estimated to be as high as $10^{-13}cm^2/sec\text{-}V$ even at room temperature.

3.2 Experiment and Experimental Apparatus

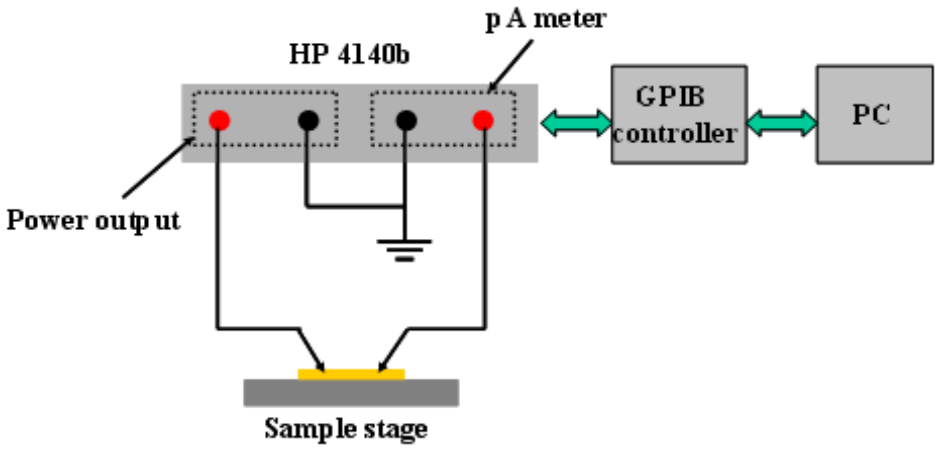
3.2.1 Experiment

Comb patterns from both MSSQ and SiCOH PLKs described in chapter 2 were used in this study. In order to avoid PLK failure as well as to capture the signature of Cu out-diffusion in the leakage current, several strategies have been taken: (1) moderate electrical fields were

used to stress patterns, typically ranging from 0.2 – 0.8MV/cm; (2) experiments were conducted at room temperature in room ambient; and (3) time-dependent leakage current evolution is recorded at a fast data acquisition rate, typically 4 data/sec, which is limited by the data acquisition rate of the used instrument yet fast enough to detect the impact of Cu out-diffusion on the leakage current under our testing conditions.



(a)



(b)

Figure 3.1 (a) the home-made leakage current measurement setup and (b) a schematic plot showing connections between its major components

Unless otherwise specified, electrical measurements were generally performed on fresh (as-received) patterns. However, in order to investigate the role that the moisture plays in Cu out-diffusion, a few samples were annealed at 120^{o}C in a vacuum chamber with pressure ~10^{-6} torr for 24 hours and tested under the same vacuum environment after they cooled down to room temperature. In addition, to investigate the electrical field effect, a few samples were tested under slightly high electrical fields (>1.0MV/cm). After electrical stress, samples were characterized by voltammetry technique with 2wt% KCl solution as infiltration medium to inspect the condition of diffusion barrier. In order to assure the detection accuracy, a slow potential sweeping rate, 0.05V/s, was used (see section 2.2.2).

3.2.2 Experimental Apparatus

The apparatus for leakage current measurement is similar to that used in voltammetry technique. A major change in this setup is the HP4140B pA meter/DC voltage source that is used as function generator as well as ammeter. Voltage output and current response are simultaneously monitored and transferred through a GPIB controller to a labview-programmed PC where the data is saved. Figure 3.1 shows a picture of the home-made setup and a schematic plot of the electrical connections between the major components. The advantage of using HP4140B is that multiple choices of voltage output such as DC, single/double ramp wave, and single/double staircase wave can be easily programmed. With appropriate shielding and electrical grounding, the current measurement resolution can reach ~0.1pA.

3.3 Experimental Results

3.3.1. General Observation of Leakage Current Hump Behavior

3.3.1.1 Test under Moderate Electrical Field

Figure 3.1 and Figure 3.2 respectively display two typical modes of time-dependent leakage current behaviors observed at room temperature under moderate electrical field. The example data shown here was measured from two identical MSSQ patterns with 400nm PLK from two different wafer units. In the first mode, the current flow is initially high, followed by a

monotonic decay as time elapses, as seen in Figure 3.2. This leakage current behavior is commonly observed at the early stage of normal TDDB test. The short period of high current flow at the beginning is believed to stem from the intrinsic capacitive effect and the following continuously decaying current is generally attributed to the dielectric relaxation processes including electron trapping/detrapping and thickening of the interfacial barrier from electrode to the conduction band of PLK [142, 143]. The second mode seen in Figure 3.3, however, contains an abnormal current hump behavior: shortly after the initially high capacitive effect, the current momentarily rises up to 2%-10% of base current and then falls down again to follow the normal decaying behavior observed in the first mode.

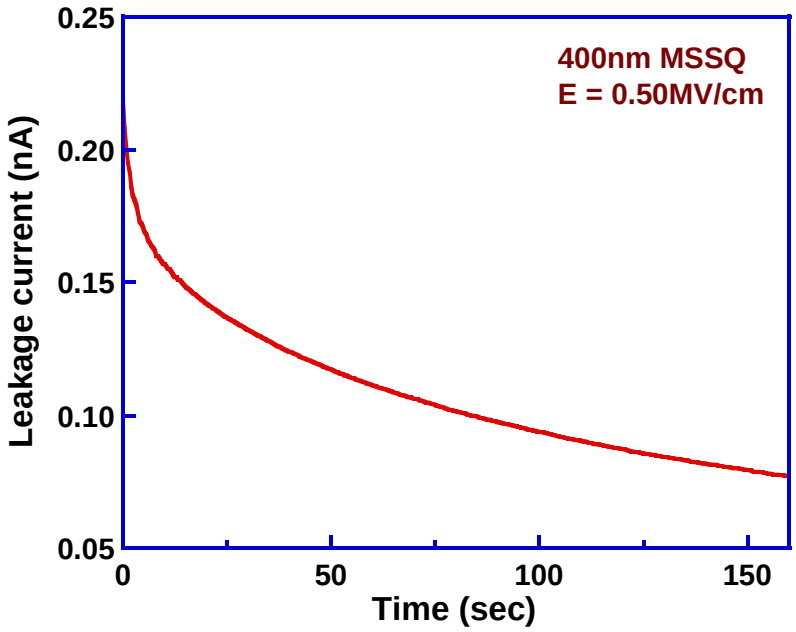


Figure 3.2 A plot showing the leakage current behavior as a function of time taken from a MSSQ comb pattern with 400nm PLK space.

These two current modes were observed in both SiCOH and MSSQ (wafer I and II) PLKs. A large number of samples, totaling 130, taken from different locations in testing wafers were examined. Among 60 MSSQ PLK samples, 23 showed the second mode while of 70 SiCOH PLK samples, 38 showed the second mode. Based on experimental data from these

samples, general trend was found, that is, the second mode tended to be observed more frequently in samples taken from the wafer edge in all PLK wafers or in the patterns located in the first level in MSSQ I wafer. Since it is well known that the step coverage of Ta diffusion barrier film is inferior in patterns in the interconnect structure in the bottom levels and in areas in the wafer edge (see the discussion in section 2.4), this observation, which is also consistent with the diffusion barrier characterization results achieved from as-received MSSQ PLK samples in chapter 2, indicates that the current hump behavior may be correlated to the Cu out-diffusion through barrier defects.

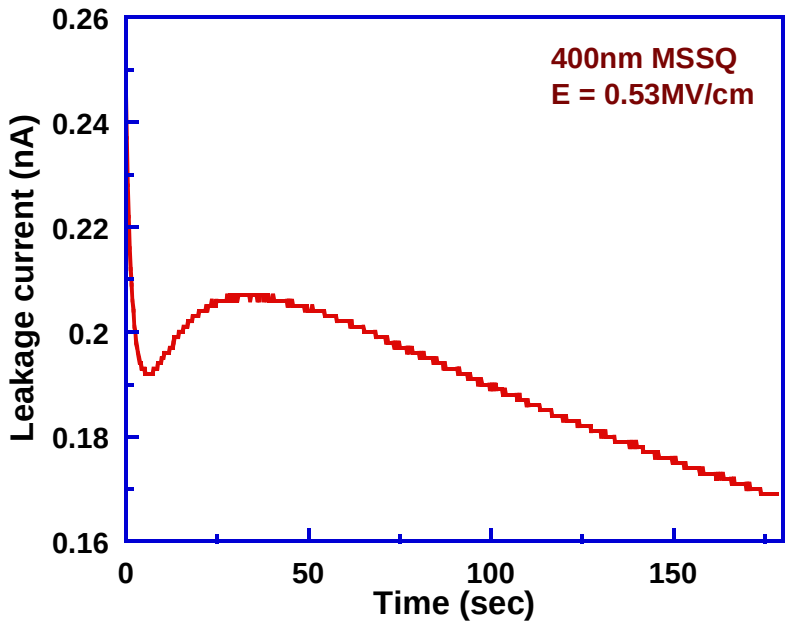


Figure 3.3 A plot showing the leakage current behavior as a function of time taken from a MSSQ comb pattern with 400nm PLK space where a current peak appears shortly after the initial capacitive current.

3.3.1.2 Electrical Field Effect

The effect of electrical field on the current hump behavior was also investigated. It was found that the applied electrical field has pronounced impact on the time to the current peak τ. As the electrical field increases, the time to reach the current peak decreases. Figure 3.4

displays the representative results showing the effect of electrical field. The data was taken from two identical SiCOH PLK patterns with 95nm PLK width in the same wafer tested under two different electrical fields at room temperature. It is clearly seen from this plot that the as the electrical field increases, the time to the current peak decreases. Notice that in this plot the leakage current measured at the lower electrical field (0.60MV/cm) is amplified 5-fold for comparison clarity.

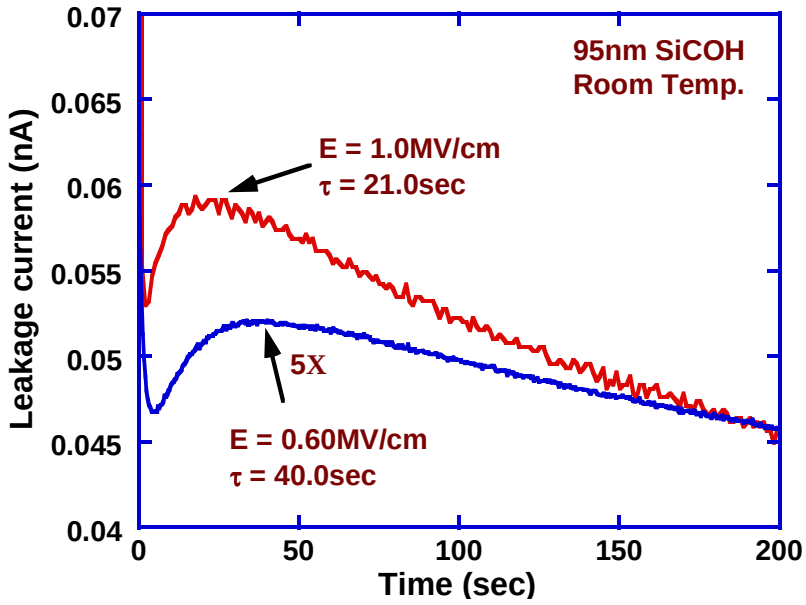


Figure 3.4 A plot showing the electrical field effect on the time to current peak.

3.3.2 Current Hump Mechanism: Space-Charge-Limited (SCL) Transient Current

3.3.2.1 Moving Species Responsible for the Current Hump Behavior

While the current hump that is distinctively different from normal decay behavior clearly indicates that there are extra mobile charge carriers injected or created in the interconnect pattern during electrical stress, the identity of the moving species is however not readily apparent. Many factors may create extra charges in the interconnect structure. Aside from the extrinsic factors such as moistures and impurities trapped in PLK and Cu out-diffusion from defective diffusion barrier, other factors such as electrical stress induced PLK failure may also

contribute to the creation/generation of extra mobile charges. In order to identify the moving species responsible for the current hump, all possible factors need to be carefully examined.

Since the electrical measurements were carried out at room temperature under moderate electrical field, electrical stress induced PLK failure is very unlikely to be the source of extra charges. In addition, when applying the same testing conditions to identical patterns, the fact that the current hump behavior is observed in some samples yet absent in others strongly implies that the PLK failure is not the mechanism for extra charges.

Due to the same reason, impurities trapped in PLK as the possible charge carrier sources can also be eliminated. Since all the samples from both MSSQ I and SiCOH wafers, as characterized by voltammetry technique to have impurities in PLK, if the impurities are the extra charge sources, identical patterns are expected to show similar current hump behavior when tested under the same conditions, which however was not observed in the experiment (see, e.g. Figures 3.3 and 3.4). The fact that the impurity-free samples in MSSQ wafer II shows similar current hump also supports this argument.

According to the voltammetry results from as-received samples, no measurable moisture contamination was found in as-received SiCOH and MSSQ II samples. While a tiny amount of moisture or moisture components may be trapped in these samples yet beyond the detectability of voltammetry technique, such moisture or moisture components may contribute to the increase of dielectric permittivity and thus the leakage current decay (relaxation current) but is not expected to significantly alter the behavior of leakage current [165, 166]. The presence of current hump behavior in both SiCOH and MSSQ II samples, therefore, indicates that moisture trapped in PLK is also not the source of extra charges. In addition, even more solid evidence to eliminate moisture mechanism was obtained by the following experiment. After deliberately breaking the scribe cells (a solid dielectric material, usually SiN or SiCN deposited at the edge of wafer unit to prevent the attack of ambient gases and moistures on the patterned PLK) of a few samples that exhibited normal decaying current, the leakage current behavior were retested

while the samples were exposed to a variety of humidity environment. None of the tested sample produced the current hump behavior, providing decisive evidence to rule out the possibility of moistures as the source of extra charges.

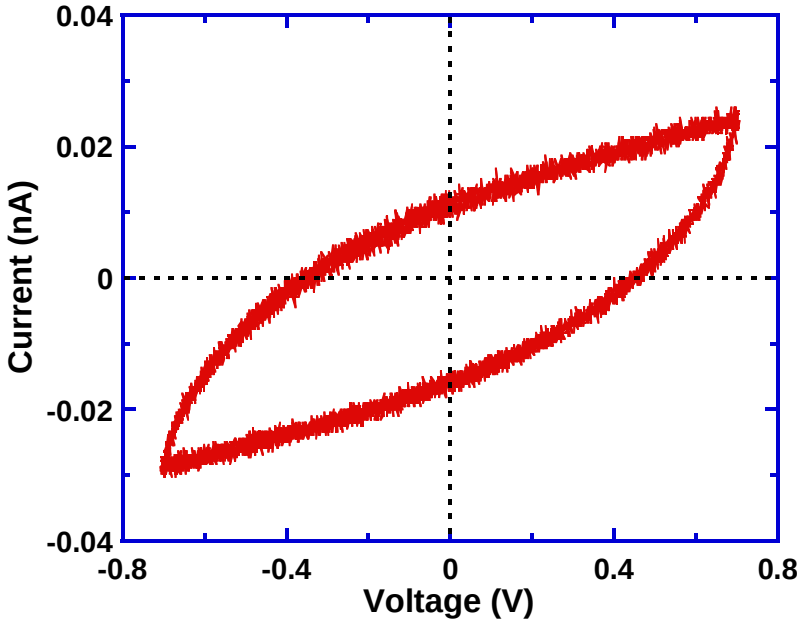


Figure 3.5 A plot showing the example of voltammetry results taken from electrical stressed samples with normal decaying current.

Based on above analysis, the out-diffusion Cu ions appear to be the most possible extra charges responsible for the current hump. The first indication supporting Cu out-diffusion mechanism was the general trend that the current hump behavior was observed more frequently in the samples taken from the wafer edge and these located in the first interconnect level in MSSQ II wafer. In order to attain more solid evidence to confirm this mechanism, voltammetry technique characterization was performed on the electrical stressed samples to inspect the integrity of Ta diffusion barrier films. Examples of voltammetry results are shown in Figure 3.5 and Figure 3.6, respectively. While all samples with normal decaying leakage current showed symmetrical hysteresis, indicating the intactness of diffusion barrier films, samples with current hump behavior displayed clear Cu reaction peaks, suggesting that the Ta diffusion barrier is

indeed defective. The perfect correlation between the defective diffusion barrier film and the current hump behavior, therefore, leads to the conclusion that the moving species responsible for the current hump behavior have to be out-diffused Cu ions.

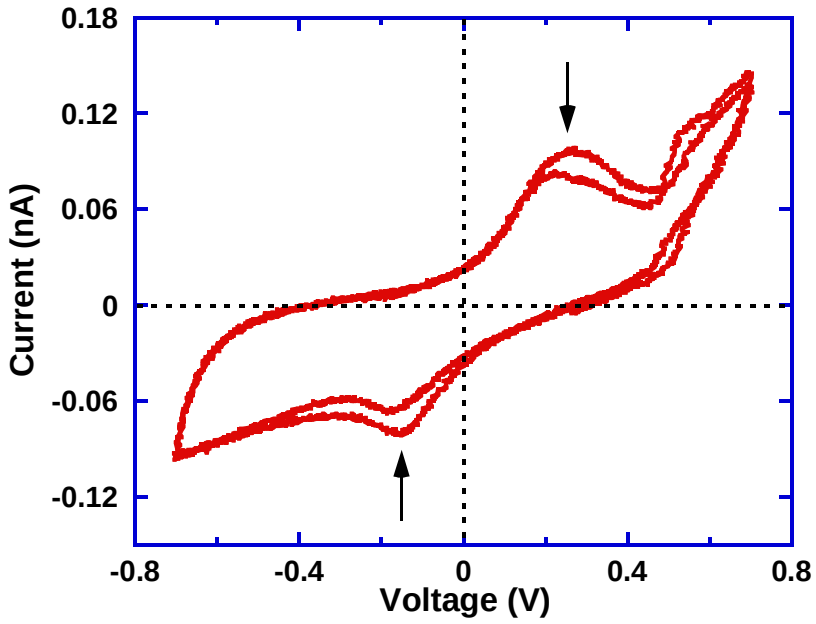


Figure 3.6 A plot showing the example of voltammetry results taken from electrical stressed samples with current hump behavior.

3.3.2.2: Barrier Failure: Source of Cu Injection

Without structural defects such as pinholes and microcracks in the diffusion barrier, it is impossible for Cu to diffuse out into PLK. Since it is well known that Ta is more stable than Cu, the barrier structural defects with Cu directly exposed to PLK are expected to be the weak spots in preventing Cu out-diffusion under electrical stress, and this Cu injection mechanism is most likely to be the case in MSSQ samples that have barrier defects at as-received condition. However, the fact that the current hump behavior also appears in SiCOH samples, which have been proven by voltammetry technique to have intact barrier films and without pre-trapped Cu residuals at as-received condition, suggests that electrical stress may also induce barrier failure

through which Cu can diffuse out. As will be investigated in more details in chapter 4, this barrier failure mechanism does occur in Cu/PLK interconnects.

3.3.2.3 Controlling Mechanism for Current Hump Behavior

It is clear that the current hump behavior seen in this study is associated with the Cu ionic injection at the Ta/Cu electrode and subsequent Cu ion migration in PLK matrix under the influence of applied electrical field. However, it is also important to notice that two possible mechanisms may control the current transport, and thus the behavior of current hump, since two separate processes are involved. The first one is the injection rate of Cu ions at the electrode-PLK interface while the other is the migration of Cu ions in PLK. As seen in Appendix A, the former is essentially interface-controlled and thus independent on PLK width while the latter is bulk-controlled and thus dependent on PLK width.

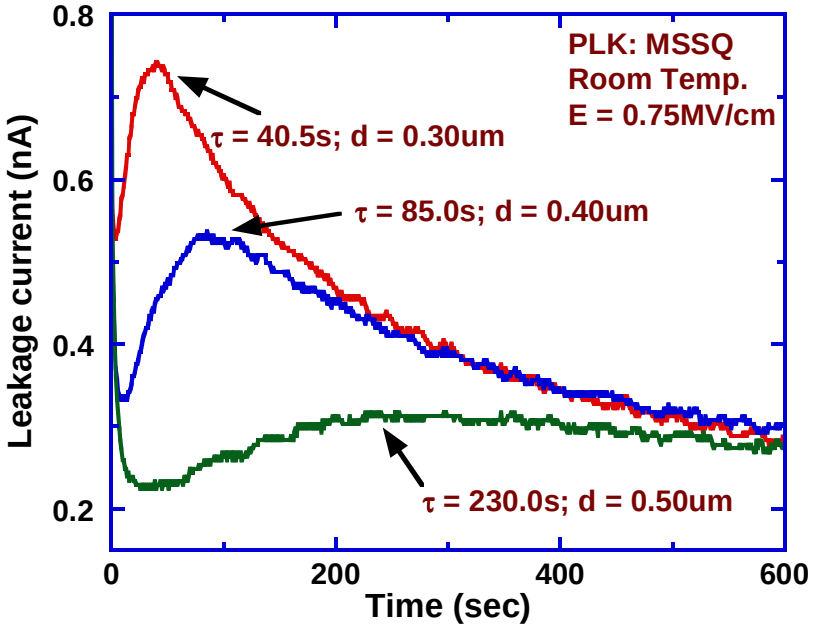


Figure 3.7 A plot showing the comparison of the time to the current peak from MSSQ patterns with different PLK widths tested at the same electrical field.

In order to distinguish these two controlling mechanisms, the time to the current peak as a function of PLK width was studied. Patterns with different PLK widths were tested at the same

electrical field and the time to the current peak was compared, as in Figure 3.7. It is clearly seen from this plot that as the PLK width increases, the time to the current peak increases. With this result, it readily concludes that the controlling mechanism for the current hump behavior is migration-controlled instead of injection-controlled.

3.3.2.4 Proposed Mechanism for Current Hump Behavior

Similar current instability has been observed in many prior studies where the current hump was attributed to the space-charge-limited (SCL) transient current induced by the continuous generation or injection of excessive mobile charges at the metal-dielectric interface and their subsequent drift in the dielectric bulk in the presence of external electrical field. Various excessive charge carriers have reported to be responsible for the transient hump current, including injected electrons into iodine from the tin oxide ohmic electrode contact [167], the released alkaline ions at the nickel-silicon dioxide interface [168], the injected holes at ITO/m-MTDATA interface [169], and more recently, the positively charged oxygen vacancies generated at the metal-dielectric interface of high-k capacitors [170-173]. It will be demonstrated that the same SCL mechanism can be applied to explain the current hump behavior observed in this study. However, instead of any other types of excessive charges, it is Cu ions injected at the metal-PLK interface that are responsible for the observed current instability.

The SCL transient current theory was first proposed in electronic system and its physics can be found in numerous early studies [174-179], as well as in the monograph by Lampert and Mark [180]. The theoretical details of this mechanism are also summarized in Appendix A, yet for the sake of readability, its physical essential will be briefly introduced here.

The SCL transient current is essentially a time-dependent current arising from the extra charge carriers injected or generated at the electrode-dielectric interface migrating from their original electrode toward the other in the presence of external electrical field. Because the extra carriers are charged, their injection and subsequent migration will disturb the electrical field distribution as well as the voltage drop inside the dielectric, which in turn affects the charge

density distribution, the time for the charges to travel through the dielectric and thus the current flow. While exact solution to this problem requires solving Poisson's equation and continuity equation simultaneously and self-consistently, the characteristics of the transient current evolution can be achieved by carefully examining the process for the injected charge carrier traveling through the dielectric.

Consider a simple metal-insulator-metal (MIM) structure with one electrode as injection interface. As the injection starts with the application of electrical stress, excessive charge carriers are allowed to enter the dielectric, giving rising to an initial current increase. As injection continually proceeds, the initially injected charges move to the counter electrode, followed by a uniform charge carrier cloud between the moving front and the original electrode. As this takes place, a space charge area is developed. Since there are no charges between the leading front and the counter electrode, the field between the leading front and the counter electrode is constant and equals to the field at the counter electrode, which is readily understood from Gaussian theorem. As more charges advance into the dielectric, the field at the counter electrode, which is also the field that pulls the leading front moving toward it, keeps growing, and thus more current can flow. This can be viewed as a MIM capacitor whose dielectric space is continuously narrowing down yet the two electrodes are maintained at a constant voltage. This current increase, however, can only persist up to time τ, a timing point at which the leading front reaches the counter electrode. This is because when the leading front reaches the counter electrode, a uniformly distributed charge cloud area is left behind inside the dielectric. The amount of charges in this developed space charge area is far more than allowed at the steady state. An analytic solution based on a simple model showed that the total space charge overshoot at time τ is approximately 10% larger than the steady-state charge density [180]. Therefore, once the leading front arrives at the counter electrode, the dielectric contains the maximum amount of space charges and the current reaches its peak value. Thereafter, the current has to decay to its steady-state and the space charge distribution relaxes to it steady-

state configuration as well. As the time for the leading front to reach the anode depends on the migration rate of the injected charge carriers, the time to the current peak is a reflection of the charge mobility in the dielectric. In addition, since this mechanism essentially describes a migration-controlled current transport process, the peak position is very sensitive to temperature, the electrical field and the dielectric width. According to the simplified model with trapping effect ignored, the time to reach the current peak is given by [179, 180]

$$\tau = 0.78\frac{d^2}{\mu V} = 0.78\frac{d}{\mu E} \tag{3.1}$$

where τ, μ, d and V are the time to reach the current peak, the mobility of injected charge carriers, the dielectric width and the applied voltage, respectively. Based on experimental data, the mobility of injected charge carriers can be extracted.

In order for SCL transient current to be observed, several conditions are required. Firstly, a metal-dielectric interface that can serve as charge carrier reservoir is needed. For electron injection, this is normally realized by creating an ohmic contact at the interface. Secondly, the current transport should be controlled by the migration of injected charge carriers in the dielectric bulk rather than by the injection rate at the interface, that is, the injection rate at the interface is fast enough to provide sufficient charge carriers to deliver current. This is understandable because if the current is limited by the interface, every injected charge will then be relaxed by dielectric relaxation process and thus no space charge area can be developed. Finally, the trapping of injected charges in the dielectric bulk should not be significant because the trapping will effectively reduce the number of mobile charges, and consequently, the space charge are can not be created either.

From above discussion, it appears that the SCL transient current mechanism can be applied to explain the current hump behavior in this study. First, the voltammetry results clearly suggest that Cu ions are injected into PLK under the applied electrical stress, providing excessive charge carriers for current transport. In addition, the fact that the time to the current

peak increases with the increase of PLK width indicates that this current hump behavior arises from a migration-rate-controlled transport mechanism (see Figure 3.7). Furthermore, from Equation (3.1), it can be predicted that the increase of testing electrical field will shorten the time to the current peak, which is also consistent with the observations in this study (see Figure 3.4).

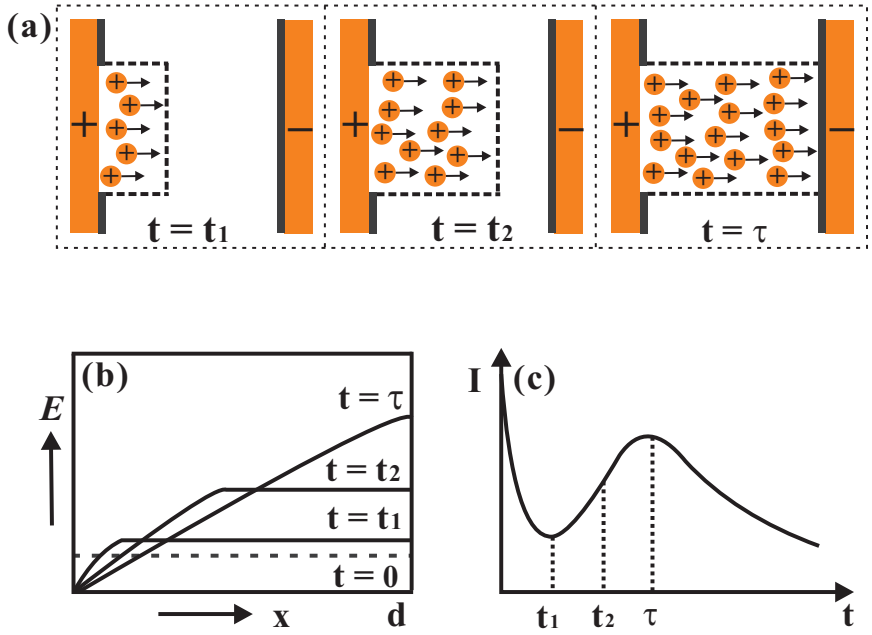
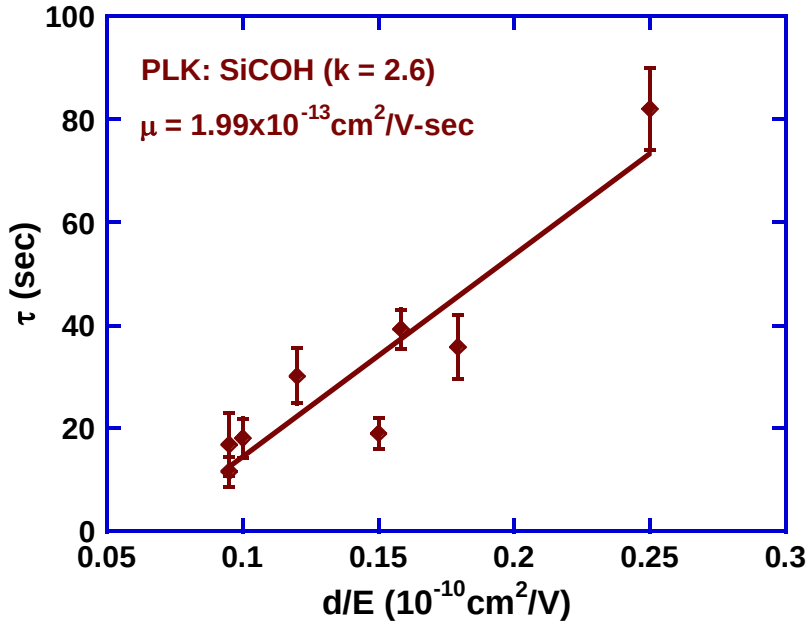


Figure 3.8 Schematic representations of SCL transient current mechanism leading to the current hump behavior by injected Cu ions. (a) creation of a space charge area by the injection of Cu ions through diffusion barrier; (b) increase of electrical field in PLK due to the electrical field disturbance by the space charges; (c) the time-dependent current evolution

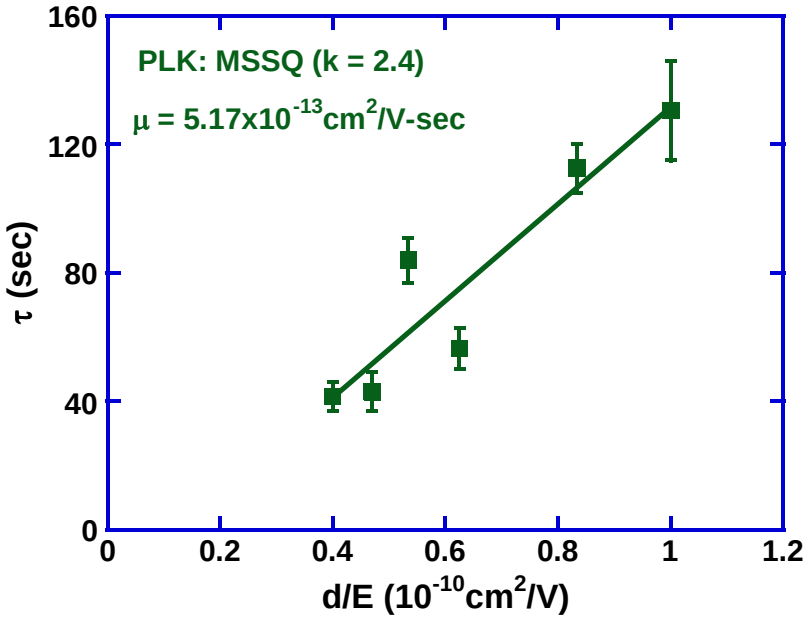
The mechanism behind the current hump behavior observed in this study is thus proposed as follows and Figure 3.8 presents a schematic representation of the proposed mechanism. The PLK, initially free of Cu ions, develops a space charge area at the anode interface when the positively charged Cu ions are injected into the dielectric in the presence of electrical field. Notice that before the Cu ionic cloud reaches the cathode, no ionic current can be detected since the charges physically carried by Cu ions remain in the dielectric bulk. However, the advancement of the leading front of Cu ionic cloud displaces the electrical field, resulting in higher electrical field between the leading front and the cathode and thus current

flow increases. The current continuously increases until the leading front reaches the cathode. At this point, a maximum amount of space charge is developed and the current attains its maximum value. Thereafter, the current by SCL transient current mechanism diminishes and is re-dominated by the relaxation current because of the dielectric relaxation process that relaxes the injected excessive charges.

With the theory of SCLTC mechanism, the mobility of Cu ions in PLKs can be estimated from Equation 3.1. Figure 3.9 (a) and (b) respectively display the collected data of the time to the current peak from SiCOH and MSSQ samples with varying PLK widths and applied electrical fields. It can be seen in these plots that the time to the current peak in both PLKs can be linearly fit to d/E (see the straight lines). This provides additional evidence supporting the conclusion that the hump behavior can be explained by the SCL transient current mechanism. From the slope of the fitted straight lines, the mobilities of Cu ions are estimated to be 1.99×10^{-13}cm^2/V-sec and 5.17×10^{-13}cm^2/V-sec in SiCOH and MSSQ PLKs, respectively. Notice that few data points are somewhat slightly deviated from the linear fits. As Cu migration is sensitive to the microstructure of dielectrics, it is believed that this deviation is due to the microstructure deformation of dielectrics (e. g. pore deformation) arising from the mismatch of thermal-mechanical properties between Cu and PLK. During standard interconnect processes where many thermal and mechanical cycles are applied, slightly different microstructure changes are expected in samples from different wafer positions and with different pattern densities (the ratio of Cu line width to PLK width). Such a pore deformation has also been observed in a prior study on the thermo-mechanical instability of pores in fully executed Cu/PLK interconnects [181].



(a)



(b)

Figure 3.9 The plots showing the data of the time to the current peak as a function of d/E from the two PLKs with varying PLK widths and applied fields: (a) SiCOH PLK and (b) MSSQ PLK.

3.4 Discussion

3.4.1 Detection of Cu Out-diffusion under Electrical Stress

3.4.1.1 Testing Conditions to Visualize the Current Hump Behavior

The perfect correlation between Cu out-diffusion and the current hump behavior has clearly demonstrated that the current hump can represent the characteristic feature of Cu out-diffusion in leakage current, which thus provides several technical insights that are helpful in the research into the electrical reliability of modern Cu/PLK interconnects. First of all, this provides decisive evidence on Cu out-diffusion into adjacent PLK by electrical stress. This potential reliability threat, though long suspected, has not been decisively evidenced by conventional reliability tests such as TDDB. More importantly, the results made in this study suggest that Cu out-diffusion under electrical stress can be simply detected without disturbing the conditions of as-received samples, which is practically impossible by microscopic observations and TDDB due to their intrinsic destructive nature. However, it should be noted that because of the high mobility of Cu ions in PLKs, care must be taken when attempting to visualize the current hump behavior. As has been estimated, the mobility of Cu ions in both PLKs has an order as high as $10^{-13}cm^2/V\text{-sec}$ even at room temperature. When tested at middle electrical field, the typical time to the current peak is about tens of seconds. Under aggressive testing conditions such as these used in normal TDDB test, the current hump period may be too short to detect. A simple mathematical calculation can be used to illustrate this point. Under TDDB testing temperature at 150^{o}C, the diffusivity of Cu ions can be expressed as

$$D_T = D_{RT} \exp\left[\frac{E_a}{k}\left(\frac{1}{300} - \frac{1}{423}\right)\right] \tag{3.2}$$

where D_T and D_{RT} are respectively the diffusivity of Cu ions at 150^{o}C and at room temperature in PLK matrix; E_a and k are the activation energy and Boltzmann constant, respectively. Assume that the activation energy for Cu ions to moving in PLK is ~1.0eV, the ratio of the diffusivity at 150^{o}C to that at room temperature will be

$$D_T / D_{RT} = \exp\left[\frac{E_a}{k}\left(\frac{1}{300} - \frac{1}{423}\right)\right] \sim 10^4 \quad (3.3)$$

According to Einstein-Nernest equation: $kT\mu = qD$, the corresponding mobility ratio is

$$\mu_T / \mu_{RT} = \frac{D_T}{D_{RT}} \cdot \frac{300}{423} \sim 10^4 \quad (3.4)$$

From Equation (3.1), the ratio of the time to the current peak will be

$$\tau_T / \tau_{RT} = \mu_{RT} / \mu_T \sim 10^{-4} \quad (3.5)$$

Since the time to the current peak at room temperature is ~100s, if tested the same electrical field as the one used in this study, the time to the current peak at 150^{o}C will be ~10ms. This requires extreme fine resolution recording of leakage current for the transient current peak to be observed! Therefore, in order to visualize the current hump behavior and thus enables the detection of Cu out-diffusion, testing at low temperature under moderate electrical field is strongly recommended.

3.4.1.2 Other Possible Current Behaviors Related to Cu Ionic Drift

It is worth pointing out that the SCL transient current by Cu ionic migration is not limited to the case of Cu injection through the barrier defects into PLK. As suggested by the physics of SCL transient current mechanism, the transient current can be observed provided that a Cu reservoir exists at the electrode-PLK interface. Due to the unoptimized fabrication processes of Cu/PLK interconnect, such a Cu ionic reservoir may exist in Cu/PLK interconnects even if they have excellent diffusion barrier integrity. In addition, because of the different quantity of Cu ions available in the reservoirs, other transient current behaviors that appear in different forms from the current hump shown above but share the same mechanism may also be observed.

One of the possible sources of Cu ions at the Ta electrode-PLK interface is the resputtered Cu residuals during etching process. If the capping layer on top of the Cu trench is overetched, Cu metal is directly exposed to the etching plasma and therefore can be

resputtered out into the PLK. If, however, the following cleaning process is not sufficiently effective, even with a good diffusion barrier without structural defects, such Cu residuals will be left behind, as schematically shown in Figure 3.10 [182]. Under electrical stress, these Cu residuals can serve as the Cu ionic reservoir and may result in similar SCL transient current. However, because the quantity of Cu ions from this origin is usually small and there is a lacking of continuous ion source (if the barrier quality is good enough to prevent Cu out-diffusion), no noticeable current hump behavior is expected. Instead, a small and short pulse of current that occurs only during the drift of the Cu ionic packet from the interface to the cathode is most likely to be seen. Although this current behavior has not been observed in samples used in this study, such a mechanism was suggested by the SCL transient current theory and experimentally visualized in iodine single crystal where an electron carrier reservoir was created at the cathode interface by the illumination using a short intense flash light [167].

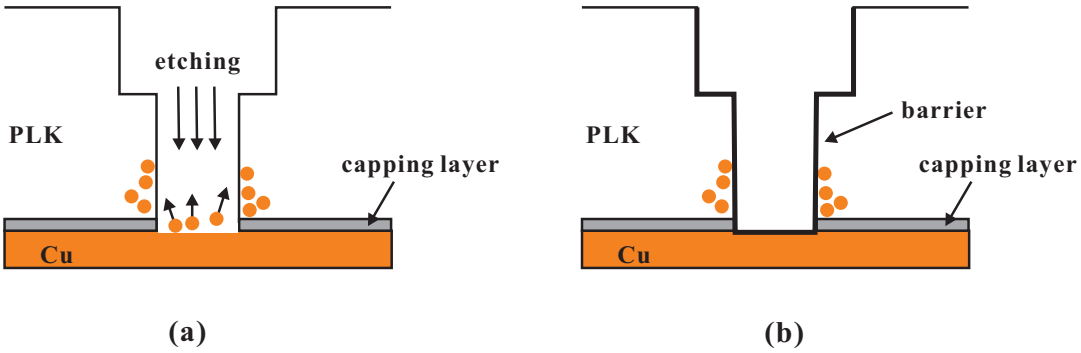


Figure 3.10 Schematic plots showing how the Cu residuals are created: (a) the capping layer is overetched and Cu atoms are resputtered out into PLK; (b) Cu residuals are left behind the diffusion barrier films.

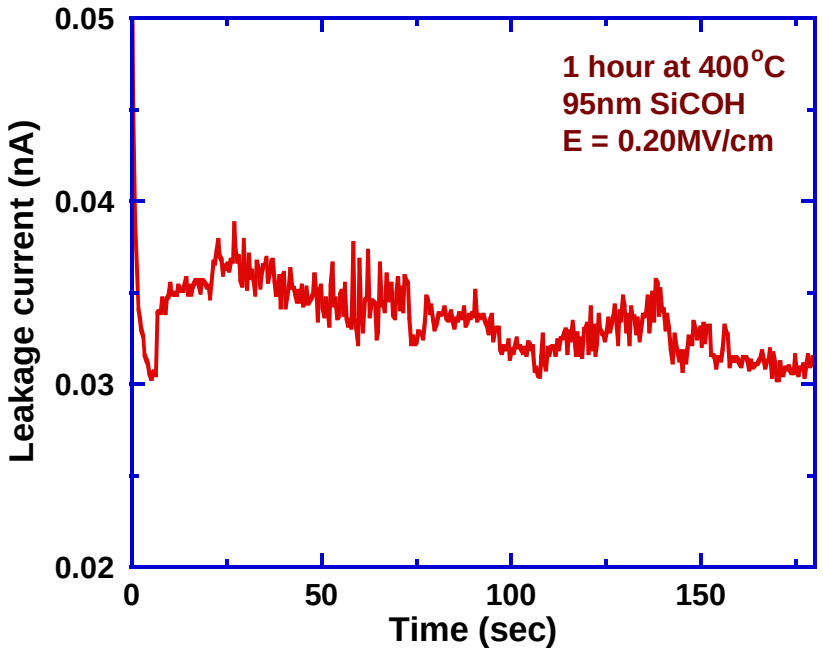
Another type of leakage current behavior, though observed and believed to be related to the Cu out-diffusion, has not been fully understood. In the leakage current measurements on both SiCOH and MSSQ samples that were annealed at 400^{o}C for one hour in the forming gas environment, a multiple-hump-like current behavior was observed, as shown in Figure 3.11(a).

These samples, when characterized by voltammetry technique at as-annealed condition as well as post-stress condition, showed extremely instable current signal with Cu reaction peaks, as seen in Figure 3.11(b). Such an unstable signal in voltammogram certainly indicates that a large area of Cu has been exposed to PLK after thermal annealing, and therefore, the multiple-hump behavior is most likely to be related to the migration of Cu ions in PLK. While the full understanding on the mechanism for such a multiple-hump-like behavior is presently unclear, it is highly suspected this current behavior is due to the Cu injection from multiple weak spots in the barrier films under electrical stress: thermal annealing creates multiple microstructural defects in diffusion barrier and these defects serve as Cu ion reservoirs; with time difference in the initiation of Cu injection from different defect spots, the multiple-hump-like behavior shown in Figure 3.11 is observed.

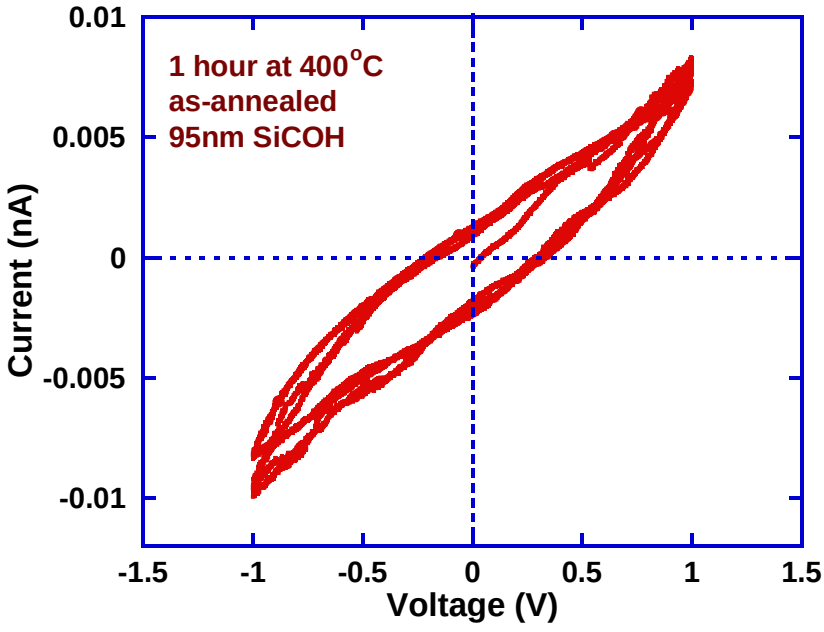
3.4.2 Several Key Questions for Open Discussion

Although this study is successful in finding a current component that originates from the Cu ion injection and its drift in PLK, it leaves several key questions unanswered.

The first question is the critical amount of injected Cu ions to produce the SCL transient current. It is believed that the level of Cu injection is indeed small because 10nm Ta barrier film should have provided reasonable good interface coverage. Furthermore, since the increased percentage of the peak current relative to the base current is far less than the theoretically predicted value (~172%, see Ref. [180]), the current hump behavior observed in this study seems to arise from a reservoir that can not supply the full amount of Cu ions prescribed by the theory. Moreover, the relative stable voltammogram signal from post-stress samples appear to also supports the argument of small amount of Cu injection because if the quantity of injected Cu ions is indeed significant, a short-circuit-like (linear) I-V curve with Cu reaction peaks should have been observed.



(a)



(b)

Figure 3.11 (a) The multiple-hump-like behavior from annealed SiCOH samples; (b) the voltammogram from as-annealed SiCOH samples.

The second question is the requirement of moisture or its components on the Cu out-diffusion. Although the experimental results and analysis made in this study clearly evidence that the current hump behavior observed in this study is not related to the trapped moisture but Cu out-diffusion, a question, i. e. whether or not moisture is required to induced Cu out-diffusion, has not been well clarified yet. In an attempt to answer this question, a few samples, both MSSQ and SiCOH PLKs, were thermally annealed at 120^{o}C for 24 hours in a vacuum chamber with pressure below 10^{-6} torr and then leakage current measurements were performed in the same vacuum environment after the samples were cooled down to room temperature. These samples exhibited similar current instability as these shown in Figures 3.3 and 3.4. With these observations, moisture appears not to be required to induce Cu out-diffusion. However, as suggested by Wood et al [183], two forms of moisture, a free form and a hydrogen-bonded form, may exist in dielectrics. In the first form, the moisture is unbound in the dielectric while in the second the moisture is chemically bound to the hydrophilic group such as silanol through hydrogen bonds and can be easily formed in dielectrics with a high density of pores and voids. On drying at relatively low temperature (150 ~ 500^{o}C), a significant loss of free form moisture can be achieved but much of the hydrogen bonded moisture remains. Removal of hydrogen bonded moisture will occur only at relatively high temperature (above 900^{o}C). In our annealing process, although most of the free form moisture is expected to be removed, the hydrogen bonded moisture may still remain in PLK. Since high temperature annealing is not applicable to PLK due to the possible microstructure damage caused by thermal stress, whether these moisture components are required to produce the current hump behavior or not is still a question for open discussion.

3.5 Summary

In this chapter, the leakage current behavior of Cu/PLK interconnects has been investigated at room temperature under moderate electrical field. A unique current hump behavior has been observed upon the application of electrical stress. With the aid of

voltammetry technique, this current hump has been revealed to be associated with Cu out-diffusion without exception. It is further demonstrated that the SCL transient current theory, a mechanism that arises from the extra charge carrier injection at the electrode interface and its subsequent drift in dielectrics, can be applied to explain the abnormal leakage hump current. However, rather than any other forms of injected charges that have been discovered in prior studies, it is the Cu ions that are responsible for the current hump in present case, and therefore, the signature of Cu out-diffusion in the leakage current has been characterized. With the theoretical analysis of a simplified SCLTC theory, the mobility of Cu ions in the PLKs used in this study has been estimated to be as high as $10^{-13}cm^2/V$-sec even at room temperature. The technique importance of this study has also been discussed. The Cu out-diffusion under electrical stress may be detected by a simple electrical measurement without disturbing the conditions of as-received Cu/PLK interconnects, which is practically impossible by conventional electrical reliability test methods. However, because of the high mobility of Cu ions in PLK, the current hump is easy to miss if (1) aggressive testing conditions, i. e, high electrical stress and temperature, are applied and (2) low-resolution current signal recording is used. Therefore, in order to effectively detect the Cu out-diffusion, high-resolution current tracing, moderate electrical stress and low temperature are suggested in the leakage current measurement.

CHAPTER 4

STUDY ON ELECTRICAL STRESS INDUCED DIFFUSION BARRIER FAILURE USING STEP MODE CURRENT-TIME METHOD

4.1 Motivation, Objectives and Major Findings

Although research on the diffusion barrier has been active and various barrier materials have been studied and proposed for future Cu/PLK interconnects, the extreme thinness requirement on the diffusion barrier film makes them prone to failure under electrical stress. Such a barrier failure and the consequent Cu out-diffusion into PLK will not only result in device instability but also accelerate the failure of Cu/PLK interconnects, and therefore, the electrical stress induced barrier failure has become and will continue to be a major concern in microelectronic industry. In spite of significant efforts, the current understanding on the electrical stress induced barrier failure is still very limited, which, to a large extent, is due to the lacking of a simple yet effective method in detecting such a barrier failure in Cu/PLK interconnects. In particular, a key question that may be closely related to the electrical reliability issue of Cu/PLK interconnects, i. e. whether there is critical stress that triggers barrier failure to induce Cu out-diffusion, has not been answered yet.

There are several major difficulties in detecting the electrical stress induced barrier failure using conventional methods. As discussed in the last chapter, physical visualization of failed barrier or out-diffused Cu by microscopic observations is extremely difficult and time-consuming because the barrier failure may occur at a localized tiny spot in a large area of barrier films and the out-diffused Cu may be tiny, which however may result in the failure of entire interconnects. Also discussed in the last chapter are the difficulties for conventional reliability tests such as time dependent dielectric breakdown (TDDB) and bias temperature stress (BTS) to detect the electrical stress induced barrier failure. Although it has been

demonstrated that when barrier failure takes place, Cu will diffuse out under the influence of electrical stress in the form of Cu ions whose drift in PLK manifests as a unique hump behavior in the leakage current, such a signature of Cu out-diffusion is too short to detect by TDDB and BTS, primary owing to the application of elevated temperature and high electrical field in these techniques and the fast diffusivity of Cu ions in PLK. However, with the understanding achieved in the last chapter, it is possible to develop a technique to detect and thus further study the electrical stress induced barrier failure in modern Cu/PLK interconnects.

This chapter presents our attempts to investigate the electrical stress induced barrier failure, particularly aiming to answer the question whether there is a critical stress triggering barrier failure. A step mode current-time (I-t) technique for this purpose is introduced. This technique shares some similarities with TDDB since both monitor the time-dependent leakage current behavior of testing samples under constant electrical field. However, instead of stressing the sample at elevated temperature and high electrical field, the electrical measurements in this technique are performed at room temperature with a step by step increased stress that initially starts from a low field. In each step, the testing sample is stressed for a certain period of holding time during which the time-dependent leakage current is monitored. After the electrical measurement in one step is done, the field is then increased to the next step and the similar leakage current measurement is performed. The electrical stress and measurement are repeated till an electrical field at which the characteristic feature of Cu out-diffusion in the leakage current has been achieved. Between each step, a few minutes bias-off is allowed to eliminate the effect of relaxation current on the current measurement in the next step. As the time-dependent leakage current behavior in every single step is monitored, the occurrence of barrier failure can be detected simply by detecting the initiation of Cu out-diffusion which, as mentioned above, demonstrates a unique hump behavior in the leakage current. With this technique, the better understanding on electrical stress induced barrier failure is thus enabled.

The application of step mode I-t method in conjugation with the voltammetry measurement made several interesting observations. A similar current hump behavior that has been investigated in chapter 3 was observed in the testing samples whose barrier films, according to the statistical evaluation at as-received condition by voltammetry technique, were originally intact. This provides decisive evidence that barrier failure indeed takes place in our testing samples by the applied electrical stress. Interestingly, the current hump, originating from the Cu out-diffusion as a result of electrical stress induced barrier failure, was found to appear only above a critical electrical field. Moreover, it was further revealed this critical stress field was strongly dependent on pattern density (defined as the ratio of Cu line width to the PLK space). This pattern-density dependent behavior is believed to arise from the pattern-density dependent barrier quality created during fabrication processes. This chapter will detail our findings as well as the introduced method.

4.2 Experiment Samples and Step Mode I-t Method

In order to study the electrical stress induced barrier failure, samples with intact barrier films and without any pre-trapped Cu in PLK at as-received condition should be used. Thus, SiCOH samples that have been proven by voltammetry technique in chapter 2 to have intact barrier and Cu-free PLK at as-received condition were used in this study. As also described in chapter 2, there are 6 patterns with same Cu line width (70nm) but various PLK space in one sample unit. As will be seen in this chapter, two categories of leakage current behaviors are observed from the step mode I-t measurements, depending on the PLK width (pattern density). Usually, patterns with relatively large PLK width (1235nm, 585nm and 260nm) fall into one category while these with relatively small PLK width (150nm, 95nm and 60nm) fall into the other. Therefore, for the sake of convenience, the former is defined as “big pattern” while the latter is defined as “small pattern”.

The leakage current measurements were carried out by the same system described in chapter 3. The major measurement component, a HP4140B pA meter/DC voltage source, acts

as function generator as well as ammeter. However, different from the method used in chapter 3 where a single constant voltage was programmed as the output, a step-by-step increasing voltage output was applied to the testing sample and in each step the time-dependent leakage current was recorded. A schematic illustration of the applied stress and current measurement is shown in Figure 4.1. Typically, the electrical stress starts from 0.10MV/cm with a 0.10MV/cm increment in the following step; the holding time for each step is 3 minutes, followed by a 5-minute bias off interval that is sufficiently long to relax the discharging current down to the measurement resolution of our instrument (~0.1pA). The field stress stops when either the barrier failure, i.e. the initiation of Cu out-diffusion, is detected or the testing pattern breaks down. However, in order to achieve the evidences to support the conclusion that there is a critical field triggering barrier failure, various starting stresses, stress step increment and holding time were used. After electrical stress, samples were inspected by voltammetry technique to characterize the diffusion barrier films. All electrical measurements were performed at room temperature.

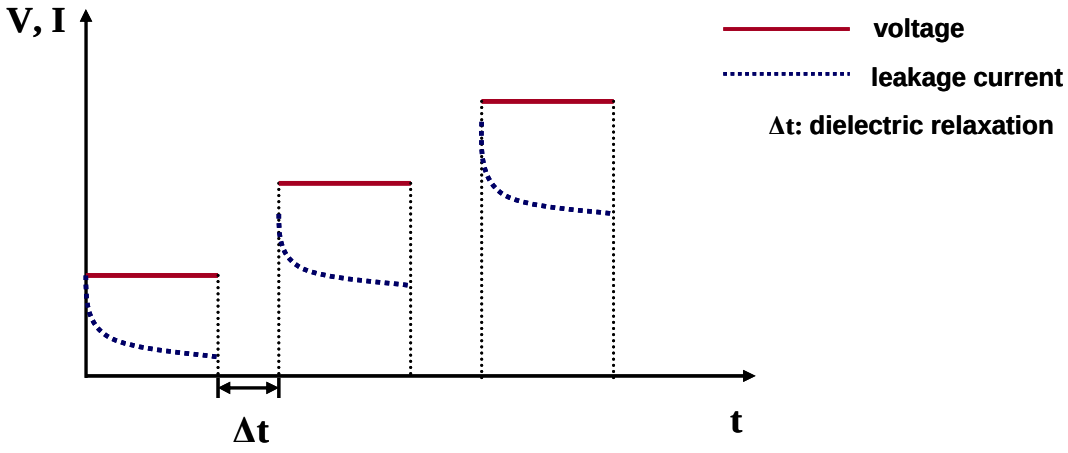


Figure 4.1 A plot schematically showing how the electrical stress is applied to the testing sample in step mode I-t method

4.3 Experimental Results

4.3.1 Time-dependent Leakage Current Behaviors by Step Mode I-t Method

Figure 4.2 displays the typical time-dependent leakage current behavior from small patterns measured by the step mode I-t method. The data is taken from a 150nm PLK pattern. As seen in this plot, at low electrical stress steps, monotonically decaying leakage current appears. However, when the electrical stress increases up to 0.67MV/cm, a small current hump can be observed. Further increase of electrical stress makes the current hump behavior more prominent: the increased percentage of the peak current with respect to the base current increases with the increase of electrical stress and meanwhile the time to the current peak increases.

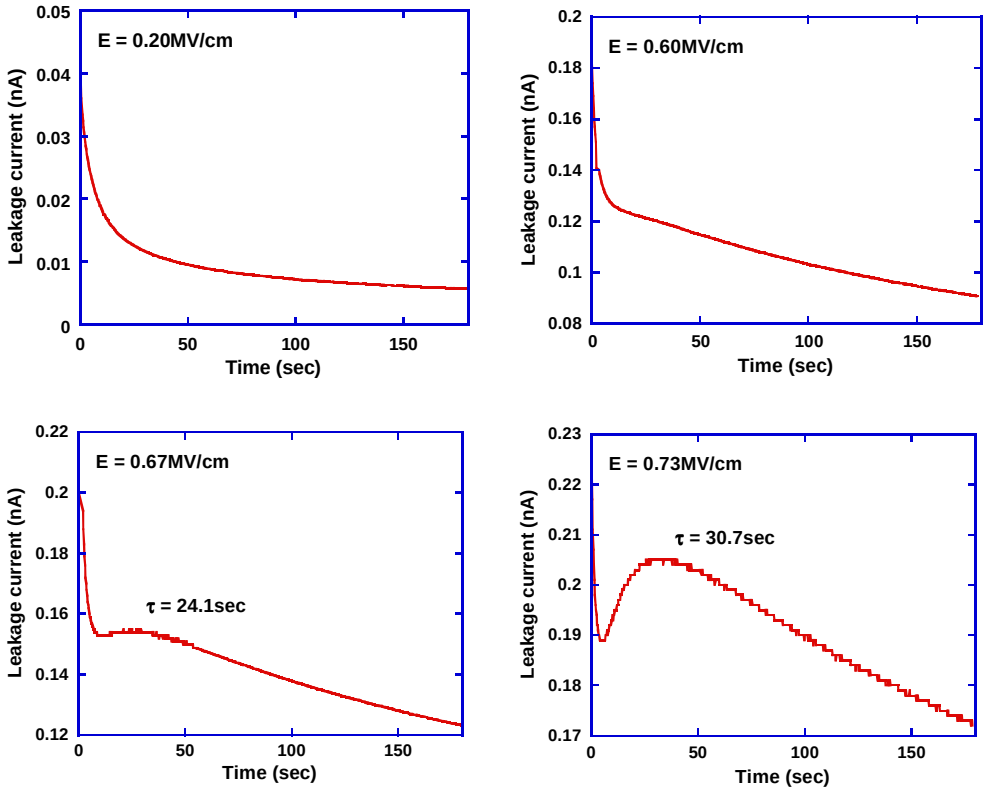


Figure 4.2 A plot showing the typical time-dependent leakage current behavior from patterns with relatively small PLK width.

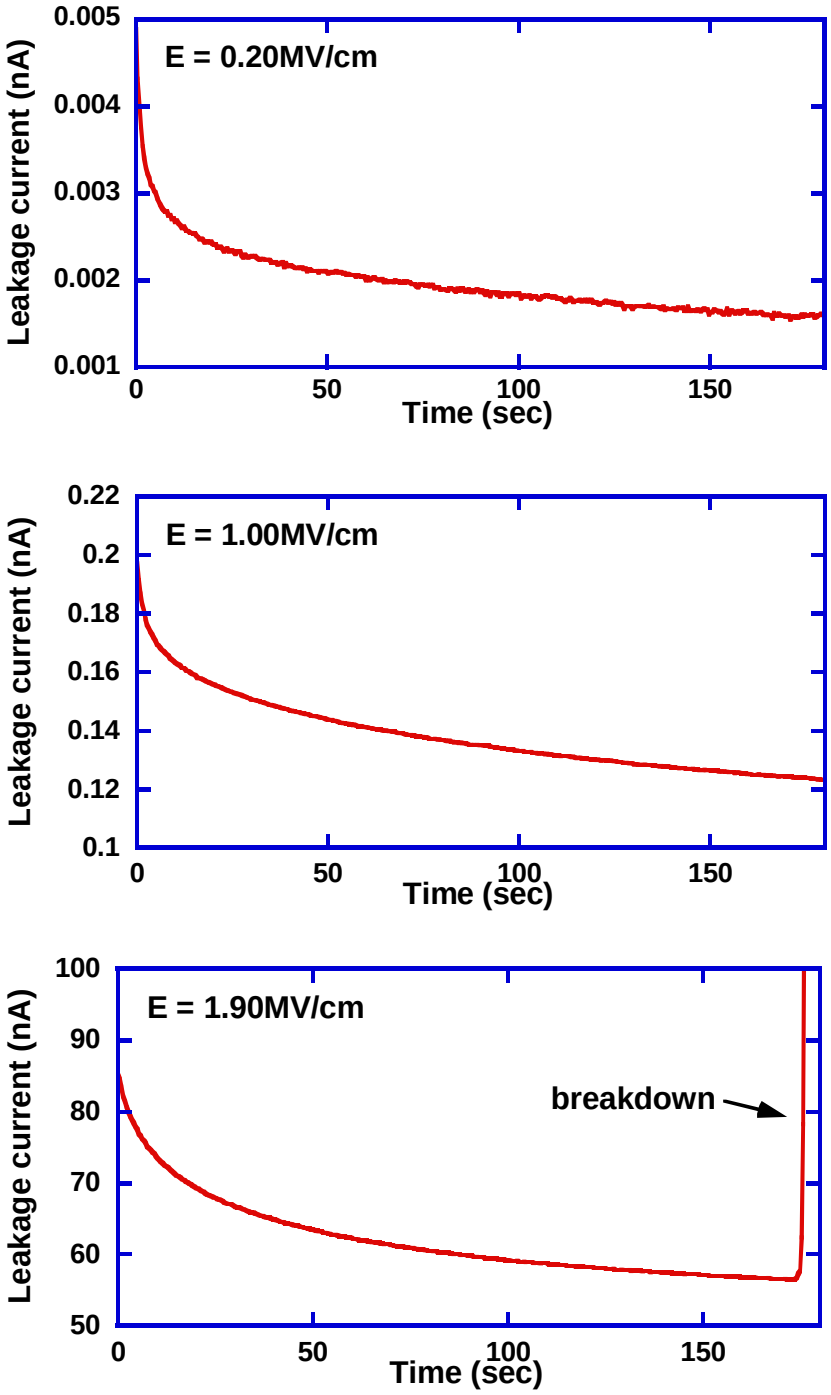


Figure 4.3 A plot showing the typical time-dependent leakage current behavior from patterns with relatively large PLK width.

While the current hump behavior was observed in most small patterns, especially these with relative narrower PLK space, big patterns exhibited a distinctively different current behavior in step mode I-t measurement. Although the current hump behavior also appeared in a few big patterns with relatively small PLK width (585nm and 260nm), most of the big patterns only showed normally decaying current behavior till pattern breakdown. Figure 4.3 shows the representative data taken from big patterns. As presented in prior studies [142, 143], this monotonically decaying leakage current upon the application of a constant electrical stress is usually observed at the initial stage of TDDB test and has been attributed to the electron trapping and detrapping effect in dielectrics.

As demonstrated in chapter 3, this unique current hump behavior can always be correlated to the Cu out-diffusion into PLK and be explained by the SCL transient current theory where the momentary current rise and fall is attributed to the Cu ion injection at the electrode-PLK interface and their following drift in PLK in the presence of electrical field. However, without barrier failure, Cu can not diffuse out. The data shown in Figure 4.2, therefore, presents a strong indication that defective barrier exists in the stressed patterns showing current hump.

Although it is practically impossible to use voltammetry or any other method to pre-characterize diffusion barrier in testing samples without disturbing their as-received condition, the statistical evaluation results obtained at as-received condition by voltammetry technique (see chapter 2), based on a large number of tested samples, implies that the diffusion barrier in SiCOH samples is intact prior to electrical measurement. The presence of current hump behavior in small patterns, therefore, is believed to be associated with the barrier failure caused by electrical stress. With the aid of voltammetry technique, several additional solid evidences to reinforce this belief have been achieved.

4.3.2 Voltammetry Results: Evidences of Electrical Stress Induced Barrier Failure

All patterns stressed by a few low-field steps and showing normal decaying current were pulled out and examined by voltammetry technique with 2wt% KCl as infiltration medium.

As exemplified in Figure 4.4, these patterns were found to have symmetrical I-V voltammogram, suggesting that the diffusion barrier in these patterns remains intact after electrical stress. When testing small patterns that were stressed to high electrical fields till the hump behavior appeared, two probe configurations were used in voltammetry measurements. In the first configuration the anode used in the step mode I-t test was set as the anode when voltammetry bias is positive, while in the second it was set as the cathode. The typical voltammograms corresponding to these two configurations are shown in Figure 4.5 (a) and (b), respectively. The first indication from these plots is that the barrier failure does occur during electrical stress, as clearly evidenced by the Cu reaction peaks (indicated by the arrows) in the hysteresises. This is the obvious evidence to support the conclusion of electrical stress induced barrier failure. Furthermore, based on the discussion on the voltammetry technique in chapter 2, the asymmetrical hysteresis with higher current on one side (positive voltage side in Figure 4.5

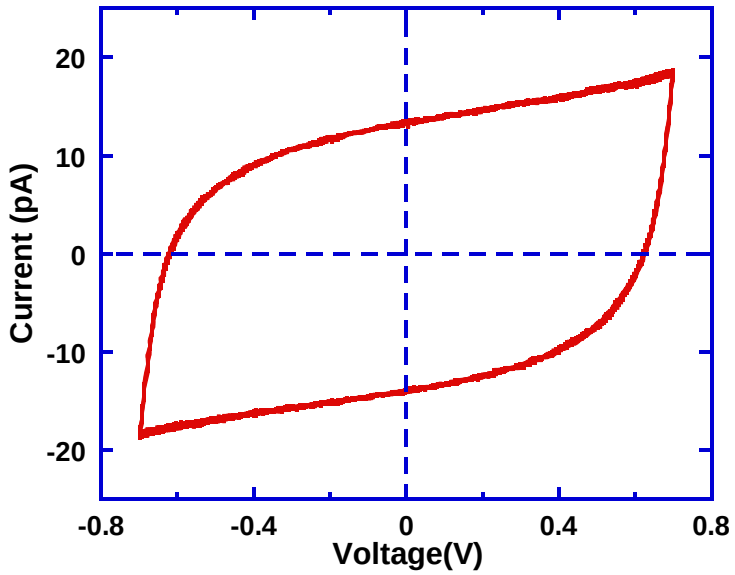
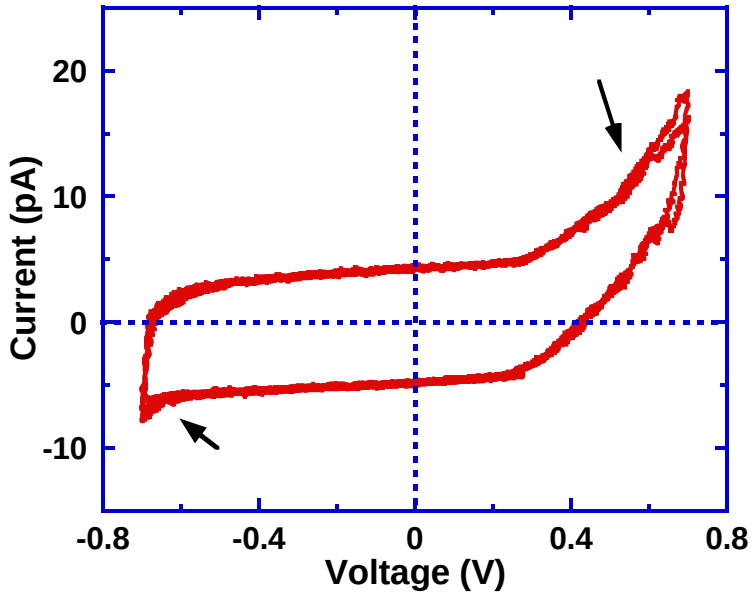
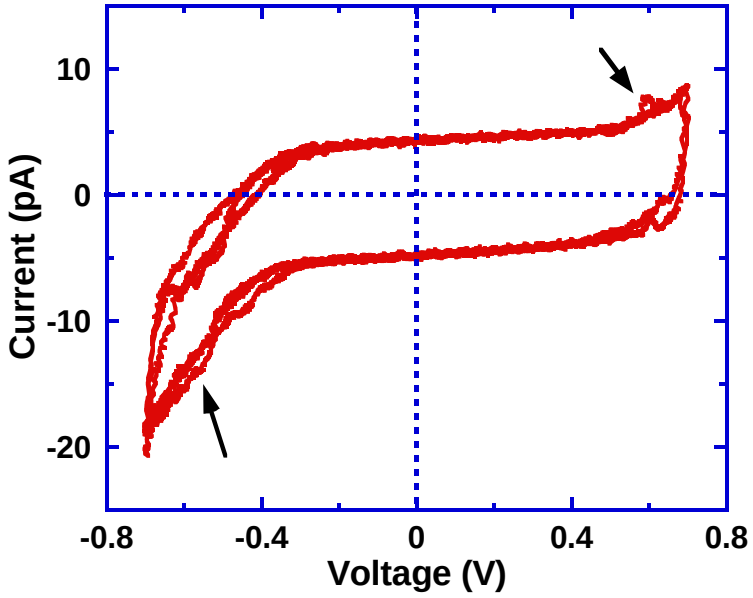


Figure 4.4 A plot showing the typical I-V voltammogram from the post-stress patterns showing normally decaying current in the step mode I-t test.



(a)



(b)

Figure 4.5 The typical I-V voltammograms corresponding to two different voltammetry probe configurations from post-stress patterns with current hump behavior in the step mode I-t test: (a) the anode in the I-t test is set as the anode in the voltammetry measurement when the bias is positive; and (b) the anode in the I-t test is set as the cathode in the voltammetry measurement when the bias is positive.

(a) and negative voltage in Figure 4.5 (b)) than the other clearly implies that the areal density of exposed Cu at the two electrodes is asymmetrical. Finally, when reversing the polarity of voltammetry bias, it is clearly seen by comparing Figure 4.5 (a) and (b) that the more pronounced Cu reaction current is reversed from one side to the other, that is, the more pronounced reaction current always appears on the side where the anode in the step mode I-t test is at positive voltammetry bias. All these observations are perfectly consistent with the scenery of stress induced barrier failure. Since as-received patterns have intact diffusion barrier and Cu injection (barrier failure) only takes place at the anodic electrode during step mode I-t test, when this anode is at positive bias, there is a massive amount of Cu readily available for electrochemical reaction from the area of failed barrier, resulting in significant large oxidation current from the reaction of Cu into Cu ions. However, when the voltammetry bias is reversed such that the cathode in the step mode I-t test becomes positive, somehow the reaction current also appears but almost unnoticeable. This is because in this case the amount of Cu available for oxidation at this electrode is less and the only Cu source is the drifted Cu ions from the failed barrier to the counter electrode during voltammetry measurement and the step mode I-t test.

With the observations and their analysis discussed above, it is expected that if the diffusion barrier on both electrodes fail, relatively symmetrical hysteresis with Cu reaction peaks will be observed. To confirm this speculation, several patterns showing hump behavior on one electrode were tested by the bias-flip test, i. e. conduct similar step mode I-t test but with a reversed bias polarity to induce the barrier failure on the other electrode. These samples were then tested by voltammetry technique. It was found that the onset fields of current hump on the two electrodes in the same pattern were very close. Demonstrated in Figure 4.6 are the onset current hump behaviors from a 260nm PLK pattern. The leakage current at negative bias is flipped here for comparison clarity. As will be discussed later, such a results is not surprising because in a standard interconnect test pattern with symmetrical MIM structure, the barrier quality of both electrodes is close to each other.

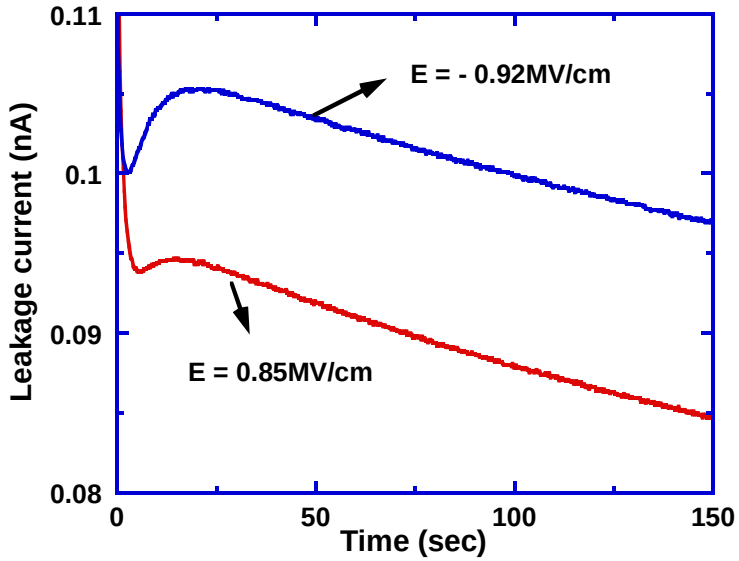


Figure 4.6 A plot showing the current hump behaviors from a 260nm PLK pattern at the onset fields of its two electrodes.

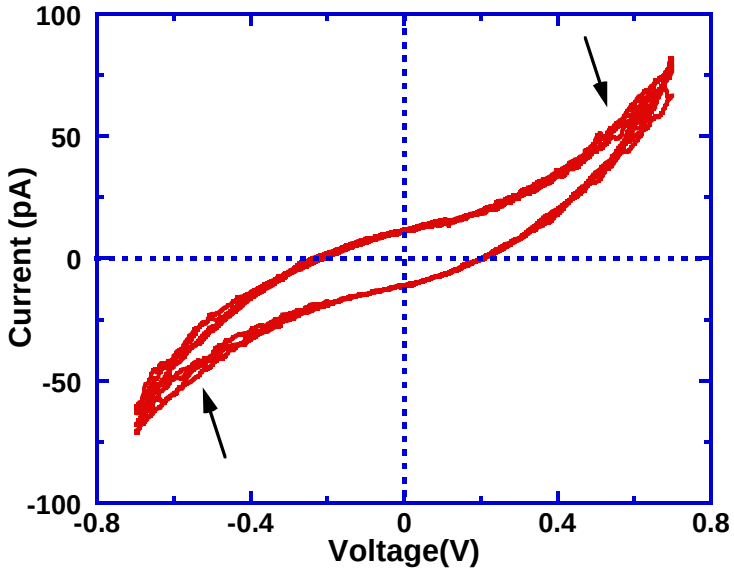


Figure 4.7 A plot showing the typical voltammogram taken from the patterns after the bias flip step mode I-t test.

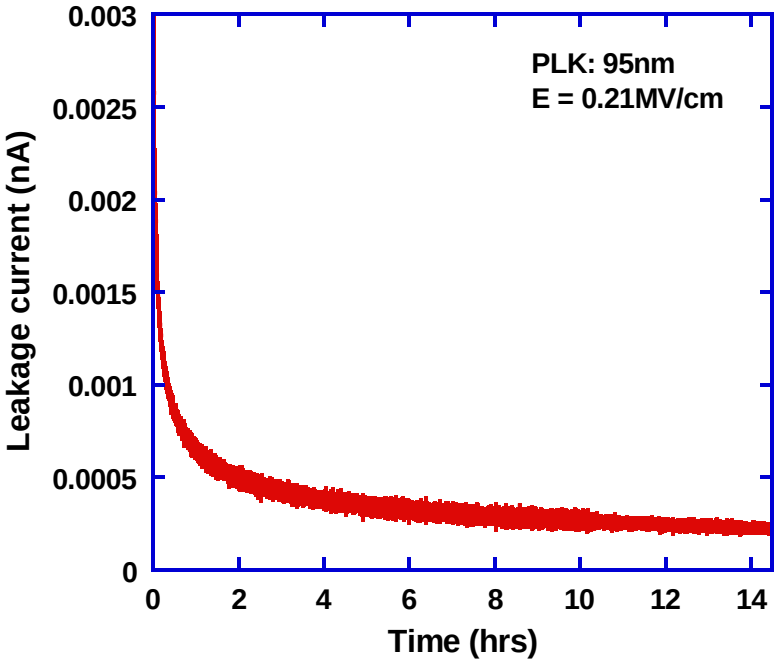
When inspected by voltammetry measurement, the hysteresis from these samples was found to be relatively symmetrical but with clear Cu reaction peaks observed on both electrodes.

The representative data is shown in Figure 4.7. This clearly indicates that after bias-flip stress the two electrodes have comparative areal density of barrier failure, as expected.

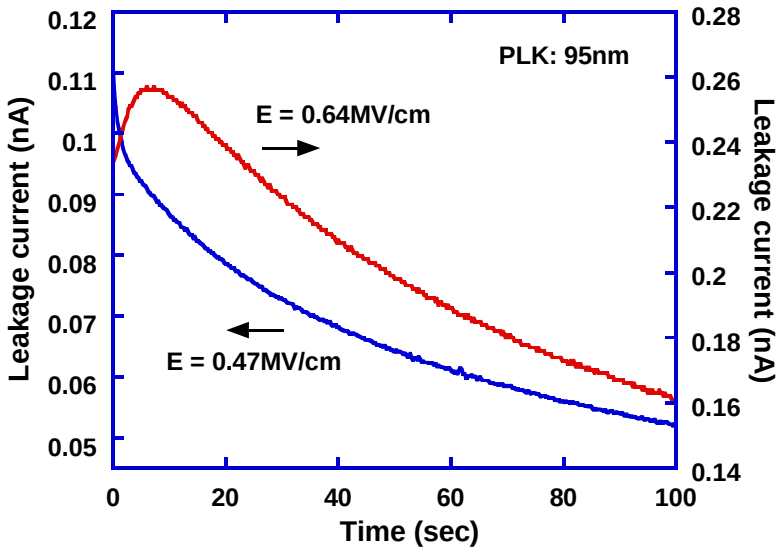
The observations made by voltammetry inspection on post-stress samples, plus the barrier integrity evaluation results on as-received patterns, leads us to conclude that hump behavior observed in this study has to be associated with the barrier failure induced by the applied electrical field.

4.3.3 Critical Electrical Stress to Induce Barrier Failure

One of the most common and interesting observations made in this study is that the hump behavior appears only when the applied stress increases to a certain electrical field. The consistent observation in all tested samples showing hump behavior, strongly suggests that there may be a critical stress that triggers barrier failure. In order to verify this argument, various initial stresses, stress steps and holding time have been used in the step mode I-t test. Interestingly, regardless of the testing parameter variations, it was found that the stress field initiating the hump behavior in the patterns with same low-k width fell into a reasonable close range. This is the first evidence leading us to believe that the critical stress does exist. The other evidence that may best support this point was found by the following experiments. Samples were first stressed at low electrical field for a long time and then switched to the normal step mode I-t test. If there is a critical stress triggering barrier failure, low field stress even with a long period of time will not induce barrier failure and thereby the monotonically decaying leakage current decay should be observed. When switch to normal step mode I-t test and once the applied field reaches the critical point, the hump behavior is expected to immediately come out. In contrast, if the critical stress does not exist, the current hump behavior is expected to present during low-field stress, though the time to the current peak may be far away from the stress starting point. Figure 4.8 presents the leakage current behaviors taken from a 150nm PLK pattern tested by the low-field stress and then normal step mode I-t measurement. As can be seen in this plot, with more than 10 hours stress at 0.20MV/cm, the current decays normally and



(a)



(b)

Figure 4.8 The typical leakage current behaviors measured by (a) long time stress at a low electrical field (0.20MV/cm); and then (b) normal step mode I-t test.

no current hump appears. Similar decaying current was observed at the initial low field stress steps in normal I-t test. However, when the electrical stress reaches 0.74MV/cm, the initiation of Cu out-diffusion immediately appears, as seen in Figure 4.8(b). With these results, we can conclude that there is a critical stress field triggering barrier failure.

4.3.4 *Pattern-density Dependent Barrier Failure by Electrical Stress*

The pattern density dependent critical stress was found by simply plotting the onset electrical filed for current hump behavior as a function of PLK width, as shown in Figure 4.9. Due to the slight difference in samples from different locations in the testing wafer, data scattering does exist. Nonetheless, the general trend of the relationship between the critical stress and the pattern density was found, i. e, the critical stress increases with the increase of PLK width (or the decrease of pattern density). Since the electrical stress induced barrier failure is strongly correlated to the barrier quality, this result also suggests that quality of barrier films in the testing wafer is pattern density dependent.

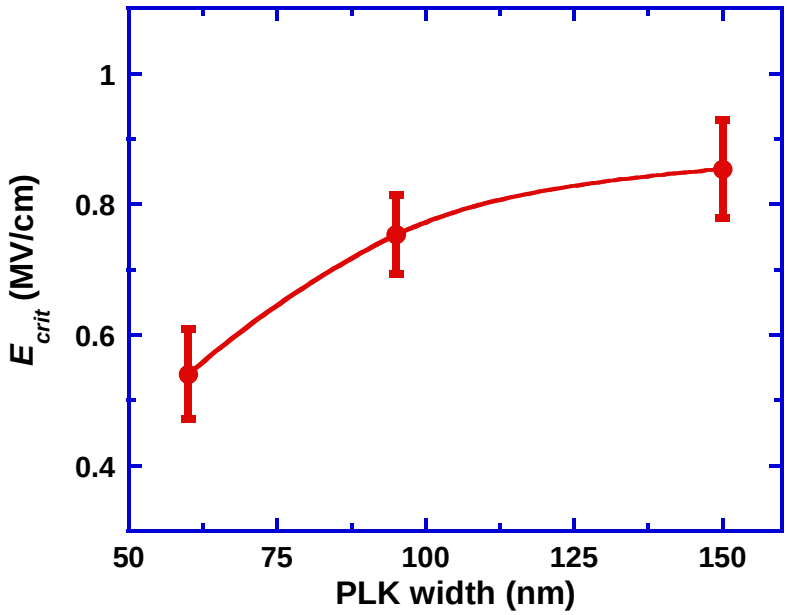


Figure 4.9 A plot showing the critical stress as a function of PLK width (pattern density).

4.4 Discussion

4.4.1 Technical Implications

This study has clearly demonstrated the capability of the step mode I-t method in detecting the electrical stress induced barrier failure in Cu/PLK interconnects that is difficult by conventional methods such as microscopic techniques and TDDB. The step mode I-t method takes the advantages of the full understanding of the characteristics of Cu out-diffusion in leakage current and thus enables the detection of electrical stress induced barrier failure simply by monitoring the time-dependent leakage current behavior in a step by step increasing electrical field. It is practically simple yet effective because such a barrier failure can be detected from a single electrical measurement.

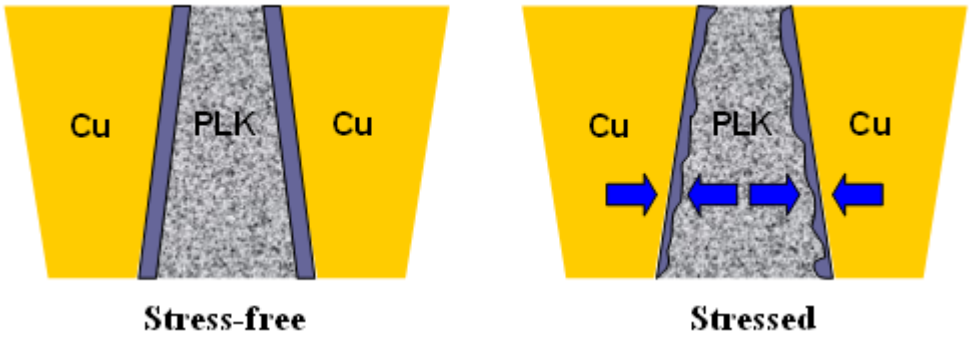


Figure 4.10 A schematic plot showing the barrier morphological roughing mechanism due to the compressive stress interaction between Cu lines and PLK developed by thermal loading

With the application of step mode I-t method, a pattern-density dependent critical stress that triggers barrier failure has been found. This observation, we believe, is due to the pattern-density dependent barrier quality created during fabrication processes, and the most possible cause is the barrier roughing by thermo-mechanical mechanism. Although it is well known that controlling the thickness uniformity of diffusion barrier is technically difficult, especially in the Cu trench with narrow width or high aspect ratio where the diffusion barrier is usually found to be thicker at the trench top compared to that at the trench bottom, the uneven thickness of the

barrier film created by PVD, seems unlikely to be the cause of barrier quality difference because the tested patterns used in this study have same Cu trench width (70nm) and aspect ratio. A most reasonable explanation is the barrier roughing arising from the thermo-mechanical stress developed at metal-PLK interface due to the thermal expansion coefficient mismatch between the PLK and Cu lines. With thermal loading during fabrication process, both Cu and PLK will experience compressive stress due to the thermal expansion. This mechanical stress interaction gives rise to the morphological change of the in-between diffusion barrier film, creating barrier roughing as schematically shown in Figure 4.10. Since Cu is mechanically stronger than PLK, the developed stress is mainly determined by Cu volume ratio in the testing pattern. Compared to the patterns with lower pattern density, higher density patterns with smaller PLK width and higher volume ratio of Cu can develop higher stress during thermal loadings in fabrication processes, resulting in rougher barrier films. A direct evidence of barrier roughing by thermal loading can be achieved by microscopic observation. An investigation in this lab has revealed that thermal stress can significantly deform PLK as well as the interfacial morphology of diffusion barrier film in fully executed Cu/PLK interconnects. A result of this study is shown in Figure 4.11, where the TEM micrographs of the barrier morphology in a Cu/PLK pattern are compared before and after annealing at 400^{o}C. It can be seen that barrier roughing indeed occurs during thermal annealing. Although a quantitative linkage between the thermal stress caused barrier roughing and the pattern density has not been made, the TEM result shown here indicates that this thermomechanical mechanism is the most likely origin responsible for the pattern density dependent barrier quality seen in this study. The rough barrier may favor Cu out-diffusion in two ways. The first is the fact that the thinning area in the diffusion barrier is inherently weaker in preventing Cu out-diffusion [184]. In an extreme case that the pattern is annealed at high temperature for a long time, barrier failure with Cu direct exposure to PLK can be developed. This has been shown and proven by voltammetry technique in chapter 3. The second is that when electrical stress is applied, locally enhanced electrical field can be

developed at the rough barrier interface [108-113]. The concentrated field spots will also accelerate the barrier failure and Cu out-diffusion.

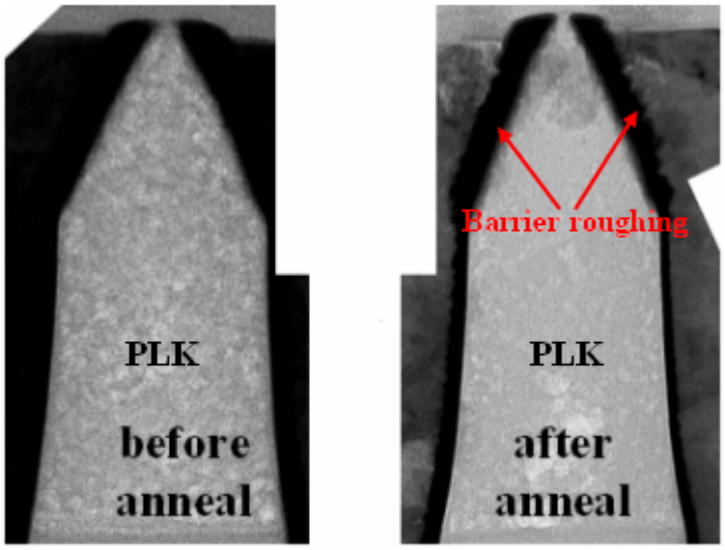


Figure 4.11 TEM micrographs comparing the interfacial morphology of barrier films at as-received condition and after thermal annealing at 400^0C for one hour.

The results made in this study also have important technical implications in the electrical reliability test in modern Cu/PLK interconnect. The absence of current hump behavior till pattern breakdown in the big patterns, in addition to the barrier quality dependent critical stress for barrier failure suggests that there may be two electrical failure mechanisms in Cu/PLK interconnects, depending on the barrier quality. When tested under electrical stress, dielectrics in patterns with high quality barrier films may break down before barrier failure while for patterns with low quality diffusion barrier, barrier failure may occur first and the out-diffused Cu becomes the major factor leading to the failure of Cu/PLK interconnects. Such a mixed mode failure mechanism has been suggested in a BTS analysis of Cu/ultra thin Ta/SiO_2/Si interconnect structure [185]. The coexistence of these two possible failure mechanisms even in the same testing wafer, e. g. the one used in the study, requires careful analysis in investigating the root of failure in electrical reliability test, which is especially important in the lifetime assessment of

Cu/PLK interconnects, because the correctness of a lifetime prediction model is entirely determined by whether or not the root of failure has been correctly identified. A possible solution to this issue may be the step mode I-t method used in this study. In order to identify the root of failure in advanced Cu/PLK interconnects, performing the step mode I-t measurement prior to conventional reliability test is strongly recommended.

4.4.2 Questions for Open Discussion

Firstly, although a critical electrical stress that triggers barrier failure has been found, two features related to the exhibited current hump in the step mode I-t test have not been well understood. The first one is the increase of the peak current with respect to the base current increases with the increase of electrical stress. According to the simplified SCL transient current theory, the peak current is ~172% larger than the base current (see Figure A.4). The increase of the peak current with the increase of electrical field therefore seems to be inconsistent with the theoretical prediction at first glance. Notice, however, that in the simplified theory of SCL transient current, the trapping effect has been ignored. The trapping of Cu ions, especially at the onset field for barrier failure when the amount of injected Cu ions is small, may significantly reduce the amount of mobile charges (Cu ions) in PLK, resulting in a smaller peak current than the simplified theory predicts. With the increase of electrical stress, more Cu ions can be injected, which effectively increases the amount of mobile charges in PLK and thus more current can flow. The second observation that appears to conflict with the SCL transient theory is the increase of τ with the increase of electrical stress. In the case that a single constant electrical filed was applied to the testing samples to induce Cu out-diffusion, as demonstrated in chapter 3, an opposite behavior of the time to the current peak was observed: as the electrical stress increased, the time to the current peak decreased. The different behaviors of the time to the current peak, therefore, seem to be due to difference in the test method. In the case of direct application of single electrical stress to induce barrier failure and Cu out-diffusion, there is no Cu ion preexisting in PLK. The time to the current peak is therefore perfectly consistent with the

theory. However, in the application of electrical stress in a step mode manner, the situation may be completely different. At the onset field for barrier failure, Cu starts to diffuse out and remains in PLK upon the removal of electrical stress. With the further increase of electrical stress in the next step, these Cu ions may decrease the effective field in PLK, resulting in the increase of the time to the current peak.

Secondly, the observations in this chapter indicate that barrier failure can take place simply by the application of electrical stress. The mechanism for such a barrier failure, however, has not been fully understood yet. Generally, two mechanisms of barrier failure by applied stress have been suggested and well accepted. The first one is the thermal stress assisted Cu diffusion through grain boundaries or microcracks in the diffusion barrier [30, 107], and the other is the barrier failure, e. g. barrier extrusion or fracture, by the thermo-mechanical stress developed at the dielectric-metal interface [186, 187]. None of these two mechanisms, however, seems to fit the observations made in this study because both require a high testing temperature yet our experiments are carried out at room ambient. In addition, Cu out diffusion through diffusion barrier is essentially a time-dependent process. The existence of critical stress as well as the sudden appearance of hump behavior in patterns that have been long-time stressed but only showed normal decay at low electrical field clearly does not support the diffusion mechanism. In order to better understand the electrical stress induced barrier failure, further investigations are obviously needed.

4.5 Summary

Based on the understanding of the characteristic feature of Cu out-diffusion in leakage current in chapter 3, this chapter has introduced a step mode I-t method to study the electrical stress induced barrier failure in advanced Cu/PLK interconnects. With the help of voltammetry technique, the barrier failure by the application of electrical stress has been decisively evidenced. A critical stress that triggers barrier failure and Cu out-diffusion has been found. Interestingly, such a critical stress has been revealed to be pattern density dependent, which

has been attributed to the pattern density dependent barrier quality created during fabrication processes, i. e. the pattern density dependent barrier roughing arising from the mismatch of thermomechanical properties between Cu lines and PLK. The technical implications from the results made in this chapter have also been discussed. Apart from its simplicity and effectiveness in detecting the electrical stress induced barrier failure, the step mode I-t method may be used as a powerful tool in identifying the root of failure in the electrical reliability test in modern Cu/PLK interconnects. In order to correctly identifying the root of failure so that the lifetime of advanced Cu/PLK interconnects can be better assessed, it is recommended that the step mode I-t measured should be performed prior conventional electrical reliability test.

CHAPTER 5

STUDY ON THE MECHANISM OF MOISTURE AFFECTING THE LEAKAGE CURRENT BEHAVIOR OF POROUS LOW-K IN Cu/PLK INTERCONNECTS

5.1 Motivation, Objectives and Major Findings

Among many reliability issues in advanced Cu/PLK interconnects, the moisture adsorption in PLK is probably one of the most concerned subjects in microelectronic industry because the moisture adsorption will not only effectively increase the dielectric constant and thus increase RC delay, but also lead to the degradation of interconnect reliability [92, 120, 188-190]. In spite of considerable efforts, the mechanism of moisture effect on the leakage current behavior in advanced Cu/PLK interconnects has not been well explored and fully understood. While prior studies generally believed that the leakage current behavior in moisturized dielectrics is dictated by the decomposition (electrolysis) of moisture [191-195], the moisture effect in Cu/PLK interconnects, however, may not be as simple as traditionally considered. Several factors may complicate the analysis of moisture effect in Cu/PLK interconnects. As evidenced by voltammetry technique, such factors include water-soluble impurities trapped in PLK that can be simply activated by moistures and the defective barrier film where the exposed Cu area can easily react with infiltrated electrolyte, both of which are expected to have a significant impact on the leakage current behavior and thus can not be excluded in the mechanism investigation of moisture effect. In order to better understand the mechanism of moisture effect, a complete set of characterization information on the testing samples as well as careful examination on these factors is needed.

This chapter aims to achieve a thorough understanding of the mechanism of moisture affecting the leakage current behavior of PLK in Cu/PLK interconnects. How the moisture, when combined with impurities and defective barrier films, affects the leakage current behavior of

Cu/PLK interconnects will be specifically considered. The primary means of investigating the moisture effect in this chapter is the measurement of leakage current by conventional voltage-ramp (I-V) method that has been widely used in the moisture effect investigation in previous studies. In order to characterize the impurities and diffusion barrier in as-received and post-test samples, the developed voltammetry technique will also be used.

The voltage-ramp method, in conjugated with the voltammetry technique, made several interesting observations related to moisture effect. Specifically, a current peak, similar as the one observed in several previous studies, has been observed in the moisturized Cu/PLK interconnect patterns in voltage-ramp test. Whereas prior studies generally attributed such a current peak to the electrolysis of moisture, our finding in this study revealed that the electrolysis of moisture did occur during voltage ramp but not the mechanism responsible for the observed current peak, because such a current peak appeared only in some specific samples. These samples, characterized by voltammetry technique, were found to either have the coexistence of impurities and defective diffusion barrier or have intact barrier but contaminated with some specific impurities. Although the impurity species are presently unknown, it is our belief that the similar current peak behaviors in these two cases may share the same mechanism, that is, the electrochemical reaction of moisture activated impurities with exposed Cu or diffusion barrier films. This chapter will detail our findings along with the analysis leading to these conclusions.

5.2 Samples and Experiment Details

Samples of all three types described in chapter 2 were used in this study for the purpose of comparison investigation. According to the characterization results in chapter 2, at as-received condition, SiCOH PLK samples have contaminated PLK but intact diffusion barrier films; MSSQ samples in wafer I have contaminated PLK (with both water-soluble impurities and moisture) as well as defective diffusion barrier films; MSSQ samples in wafer II is impurity-free but the diffusion barrier in some patterns is defective;

Moisturization was done simply by soaking the cleaved samples cleaved into degassed DI water, similar as in voltammetry measurements. Samples were infiltrated for sufficiently long time to ensure that the PLK was saturate with moisture. The saturation time is determined in a manner introduced in chapter 2. However, in order to simulate the situation of contaminated PLK or to enhance the conductivity of electrolyte, KCl solution with different concentrations was also used as an infiltration medium.

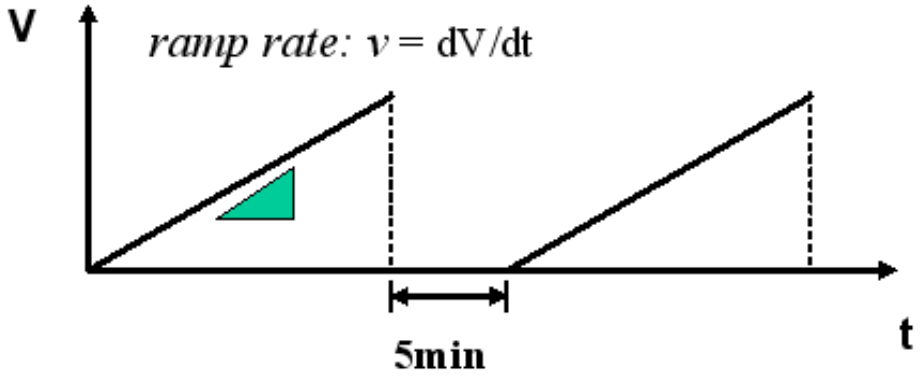


Figure 5.1 A schematic plot showing the applied voltage potential in the consecutive voltage-ramp test.

The voltage ramp measurements were carried out by a HP4140B pA meter/DC voltage source unit. Unless otherwise specified, the voltage output in this study was programmed to increases linearly with time from zero to a desired voltage, typically 25.0V, and the current is synchronically measured. The voltage ramp rate is defined as $v = dV/dt$. Samples were generally tested by a consecutive voltage ramp measurement to study the history-dependent variation of leakage current behavior. A five-minute bias off interval was set between each single measurement to eliminate the discharging current effect on the leakage current measurement in the next voltage-ramp test. The application of voltage is schematically shown in Figure 5.1. Five minutes have been proven to be long enough to relax the discharging current down to the instrument resolution (~0.1pA). To obtain a reference, the leakage current from as-received samples was firstly measured prior to moisturization.

Voltammetry characterization was typically carried out twice. The first one was performed on every individual samples prior to voltage-ramp test. Recalling that in the case of samples with contaminated PLK, voltammetry with DI water infiltration is also capable of characterizing diffusion barrier (see chapter 2), this voltammetry inspection therefore can achieve the information on the conditions of both diffusion barrier and PLK of each as-received sample. After voltage ramp test, voltammetry measurement was conducted again on post-test samples. There are two purposes for this measurement. This first one is to inspect the diffusion barrier to check the possibility of barrier failure by electrical stress. The second is to investigate the hysteresis change by voltage-ramp test. Since the hysteresis current is sensitive to the impurity concentration and the mobility of ions, any variation of electrolyte in PLK caused by voltage ramp test will be reflected into the hysteresis change. The ramp rate in all voltammetry measurements were fixed at 0.05V/s to ensure the defective barrier characterization sensitivity.

All the tests, including both voltammetry and voltage-ramp measurements, were performed at room temperature.

5.3 Experimental Results and Discussion

5.3.1 Current Peak in SiCOH Samples with Contaminated PLK and Intact Diffusion Barrier

The leakage current measurement was first performed on SiCOH PLK samples. Figure 5.2 shows the representative data where the moisture effect on the leakage current behavior is clearly seen. At as-received condition, the leakage current increase smoothly and monotonically with the increase of voltage. After moisturization, several interesting behaviors appear in the leakage current. The first noticeable behavior is that compared to as-received condition, moisturization substantially increases the leakage current magnitude. Many factors can be responsible for this current increase. The major factor is probably the fact that the infiltrated moisture will activate and mobilize the trapped impurities, significantly enhancing the electrical conductivity of PLK matrix. Other factors such as the polarizability increase of PLK components by the infiltrated moisture may also contribute to the increase the intrinsic leakage current but

very insignificant. The most important feature from this plot, however, is the current peak during voltage ramp. Such a current peak shows initially at a low voltage; consecutive measurements noticeably shift the current peak to higher voltages and simultaneously decrease the current peak intensity.

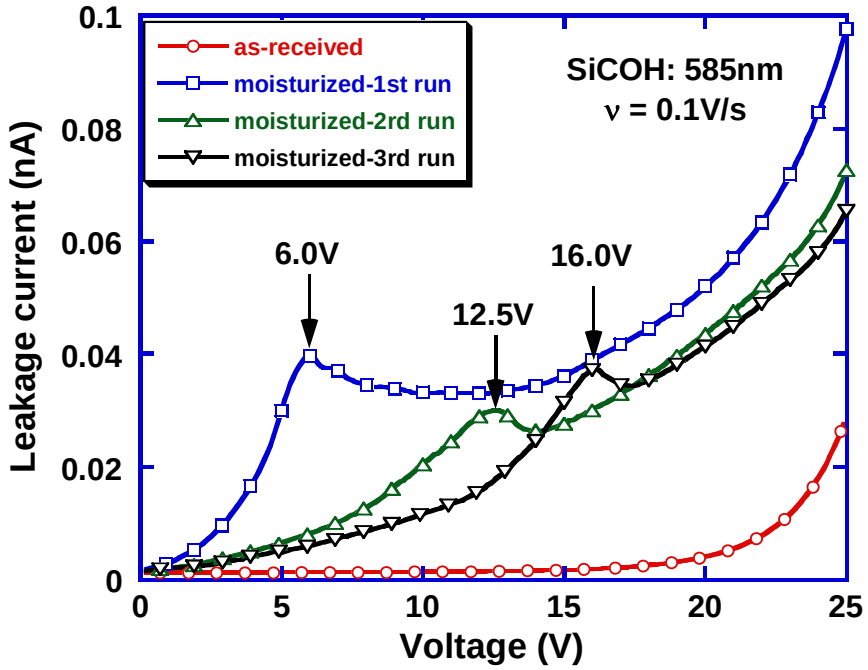


Figure 5.2 A plot showing the typically leakage current behavior from SiCOH samples

Similar current peaks have been observed and usually attributed to the electrolysis of moisture in low-k dielectrics in prior studies [194, 195]. While it is certain that the current peak observed in this study is associated with the moisture effect, the underlying mechanism is much more complicated than it appears. Several possible mechanisms can be responsible for the peak current, including: (1) the electrochemical reaction of exposed Cu in defective barrier films with impurity-moisture electrolyte. Though the diffusion barrier film at as-moisturized condition is intact, the possibility that the applied electrical stress during voltage ramp induces barrier failure can not be excluded, especially in an environment with the presence of moisture that may provide oxidation potential to induce Cu diffusing out. This barrier failure mechanism has been

discovered and studied in chapter 4; (2) the electrolysis (decomposition) of moisture, same as the one proposed in previous studies; and (3) the electrochemical reaction of moisture activated impurities with Ta (most likely to be in the form of oxides in the moisture environment) diffusion barrier. With these complications, which mechanism is truly responsible for the current peak needs to be individually examined.

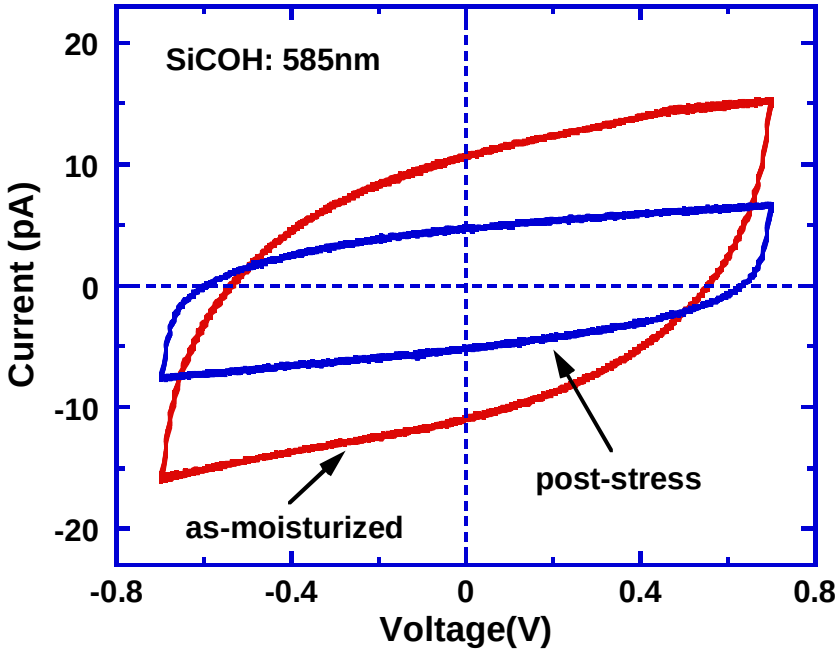


Figure 5.3 A plot showing the voltammograms from SiCOH PLK samples at as-moisturized and post-stress conditions.

In order to examine the first possibility, SiCOH samples at as-moisturized condition and after voltage-ramp test were inspected by voltammetry measurements. While several samples indeed showed defective diffusion barrier due to the electrical stress induced barrier failure, the diffusion barrier in most samples remained intact. Figure 5.3 displays an example of the I-V voltammograms measured from these SiCOH PLK samples at as as-moisturized and post-stress conditions. Two important indications can be seen in this plot. The first one is that Cu reaction is not the mechanism for the observed current peak, at least in SiCOH PLK samples,

since the hysteresises at both conditions are symmetric without showing any sign of Cu reaction peak(s). More interestingly, this plot also presents a surprising hysteresis behavior: with the progress of consecutive voltage ramp measurements, an appreciable hysteresis collapse can be observed. Notice that such a hysteresis collapse has never been observed in the low voltage cyclic voltammetry measurements. The hysteresis collapse here therefore indicates that some interesting changes have been made to the test pattern by the applied stress during voltage-ramp measurements. In addition, the consistent observation of this hysteresis collapse accompanied with the shift of current peak and its intensity attenuation in each cycle of voltage ramp in all testing samples, also presents a strong indication that these interesting behaviors are closely correlated. This correlation, as will be seen later, is the decomposition of moisture by electrical stress.

With above evidences and analysis, the Cu reaction mechanism has been clearly eliminated. The other two possibilities can be examined by the experimental results from MSSQ PLK samples with different PLK and diffusion barrier conditions.

5.3.2 Mechanism Investigation: MSSQ Samples with Contaminated PLK and Defective Barrier

Although it is well known that the electrolysis rate of pure moisture is extremely slow because of its low electrical conductivity, the moisture decomposition mechanism is possible especially when a large amount of water-soluble impurities presents in PLK such that conductive electrolyte can be created by moisturization to delivery high-density current. If such a mechanism is true, similar current peak behavior is expected to appear in MSSQ I samples with intact diffusion barrier but contaminated PLK, because they are structurally similar as SiCOH samples.

In order to examine the electrolysis mechanism, similar voltage ramp measurements were conducted on MSSQ I samples that were pre-examined by voltammetry technique to have intact diffusion barrier. Samples with moisture infiltration as well as purposely infiltrated with KCl at various concentrations (up to 15wt%) to enhance the electrolyte conductivity were also tried.

Regardless of infiltration medium, however, none of the tested samples showed current peak in voltage ramp measurement, strongly indicating that the current peak in SiCOH samples is not due to the electrolysis of moisture. Interestingly, a decrease of leakage current was observed in the consecutive voltage-ramp measurements, as clearly seen from Figure 5.4 where the data was taken from a 500nm MSSQ I PLK with 2wt% KCl solution as the infiltration medium. When comparing the voltammograms at as-moisturized and post-stress conditions, a hysteresis collapse, though not as significant as that in SiCOH PLK samples, can also be observed, as shown in Figure 5.5. The first indication from these results is that KCl solution does not react with Ta diffusion barrier within our experimental voltage range. Secondly, the decrease of leakage current and the collapse of hysteresis in the consecutive voltage-ramp test appear to be independent on the occurrence of current peak.

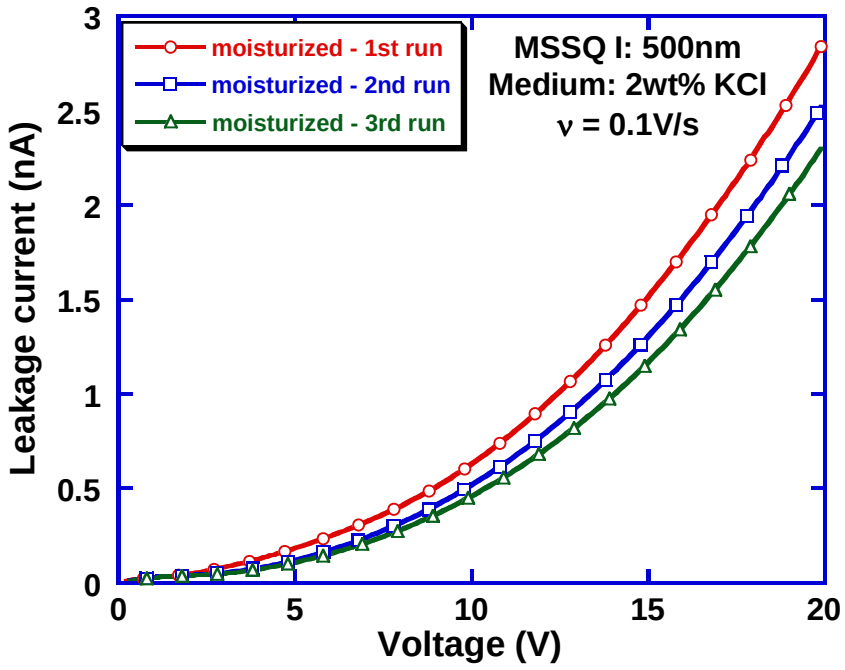


Figure 5.4 A plot showing the typically leakage current behavior from 2wt% KCl infiltrated MSSQ I samples with intact diffusion barrier

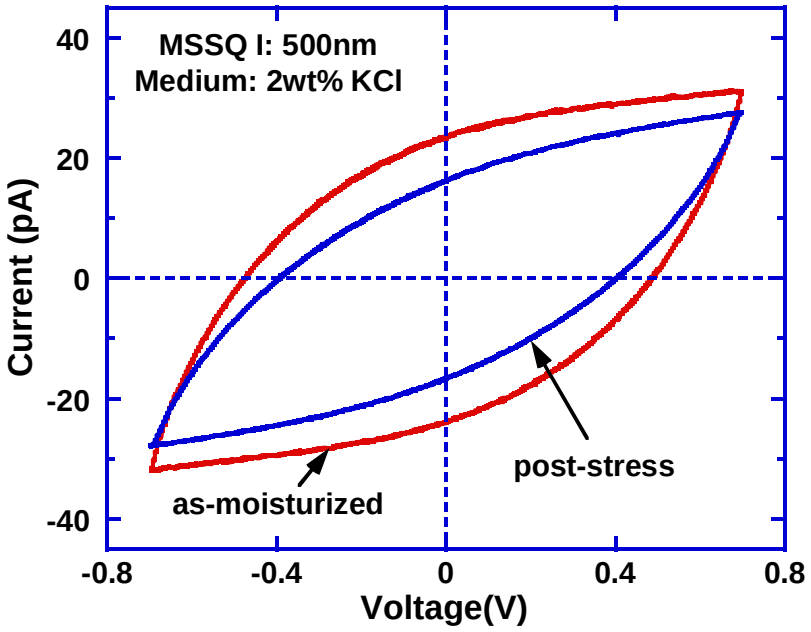


Figure 5.5 A plot showing the comparison of voltammograms from 2wt% KCl infiltrated MSSQ I samples with intact barrier at as-moisturized condition and after voltage-ramp test

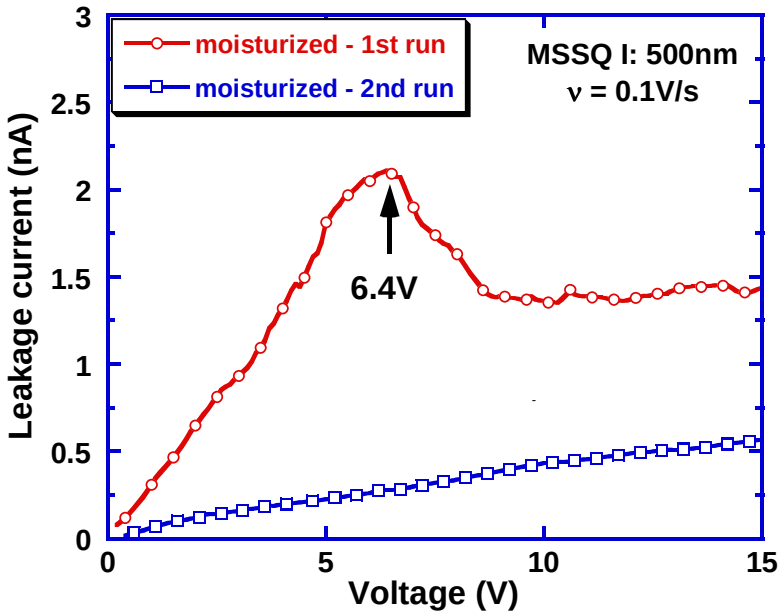


Figure 5.6 A plot showing the typically leakage current behavior from moisturized MSSQ I samples with defective diffusion barrier

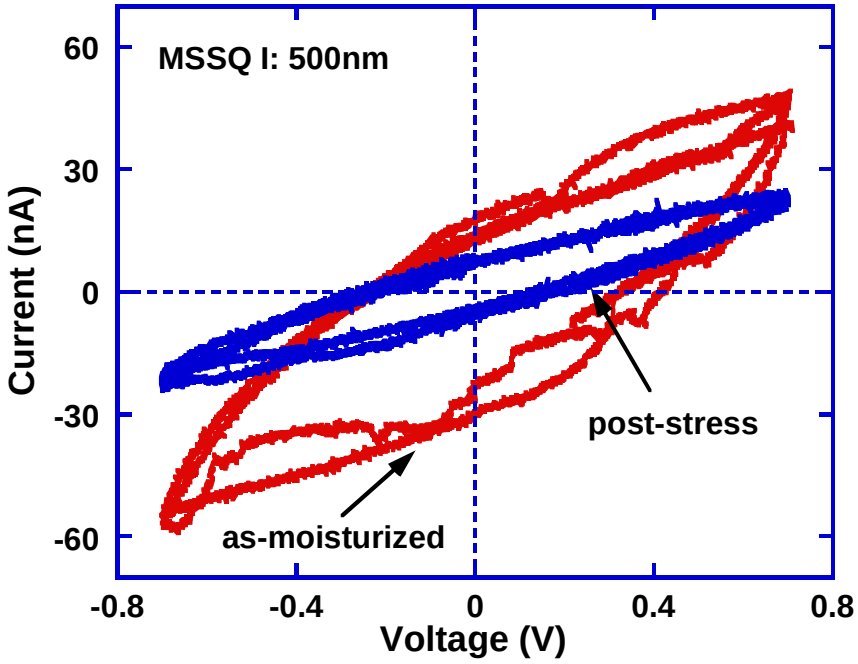


Figure 5.7 A plot showing the comparison of voltammograms from MSSQ I samples with defective diffusion barrier at as-moisturized condition and after voltage-ramp test

The absence of current peak in MSSQ I samples with intact diffusion barrier, combined with the elimination of Cu reaction mechanism, leaves the third possibility, i. e. electrochemical reaction of diffusion barrier film with the moisture activated impurities, as the most likely mechanism for the current peak observed in SiCOH PLK samples. Since the impurity species are currently unknown, plus fact that the current peak occurs at a relatively high voltage, it is impossible to utilize the basic principles of electrochemical reaction to identify which reaction takes place during voltage ramp test. Nevertheless, the experiments on MSSQ I samples with defective diffusion barrier provided better evidences to support this mechanism. Figure 5.6 exemplifies that leakage current behavior from MSSQ I samples with defective diffusion barrier. As can be seen in this plot, the leakage current behavior in these samples is quite similar to that in SiCOH PLK samples: a current peak shows in the first cycle of voltage ramp measurement but disappears in the second. When inspected by voltammetry measurement, a similar

hysteresis is also observed, as plotted in Figure 5.7. From the results made from MSSQ I samples with intact diffusion barrier, it is known that the activated impurities in MSSQ I samples do not react with Ta barrier films (see Figures 5.4 and 5.5) within the experimental voltage. The current peak and hysteresis collapse in MSSQ I samples with defective diffusion barrier, therefore, have to be attributed to the electrochemical reaction of exposed Cu with moisture-impurity electrolyte. These observations also lead us to conclude that the observed current peak in SiCOH PLK samples, though not due to Cu reaction, may share the same mechanism. The electrochemical reaction in this case, however, takes place between Ta diffusion barrier and some specific impurity species.

5.3.3 Role of Impurities: MSSQ Wafer II Samples with Impurity-free PLK and Defective Barrier

It is clear from above results that the current peak arises from the electrochemical reaction between the electrode and the moisture-impurity formed electrolyte. Two different reactions were observed. In the case of SiCOH samples, it is the specific impurity species that react with Ta diffusion barrier, giving rise to the reaction current peak in voltage-ramp test. In the second case of MSSQ I samples, although they do not have impurities that can react with Ta barrier, the electrochemical reaction between the exposed Cu in diffusion barrier with moisture activated impurities can also result in current peak in voltage-ramp measurements. There is no doubt that moisturization plays a critically important role in the occurrence of current peak. Without moisture, impurities can not be activated and reaction current can not be effectively transport with PLK matrix, and consequently, no current peak will be observed. This has already been proven by the voltage-ramp results measured in as-received SiCOH samples, as seen in Figure 5.2. In this regard, equally important is the impurities trapped in PLK. Not to mention the direct electrochemical reaction between the trapped impurities and Ta diffusion barrier in SiCOH samples, in all samples with reaction current peak, the formed moisture-impurity electrolyte serves as the medium delivering reaction current. Without impurities, current peak will not be visualized either, even if the sample has defective diffusion barrier.

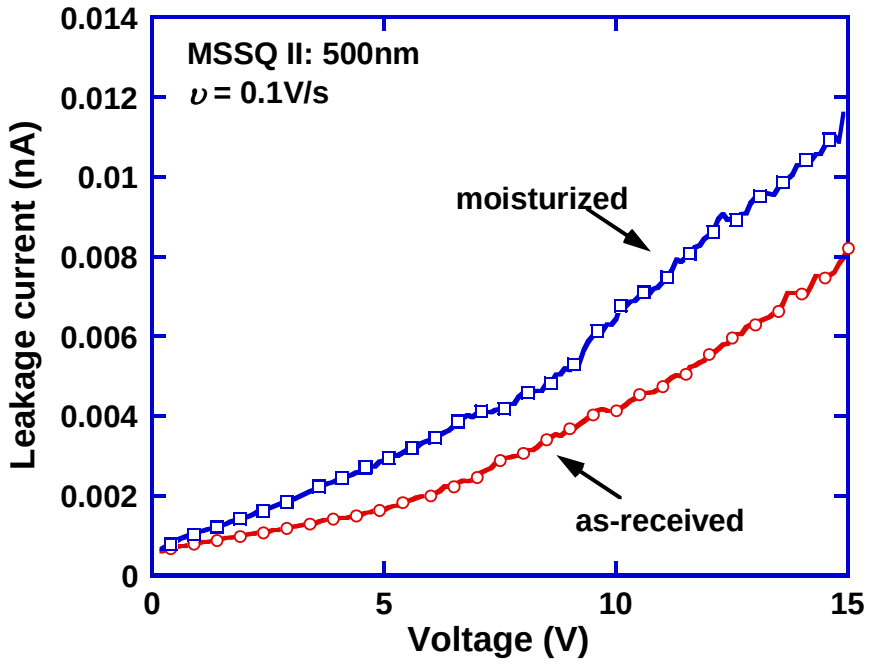


Figure 5.8 A plot showing the typical leakage current behavior in voltage-ramp measurement from moisturized MSSQ II samples

The importance of impurities may be best evidenced by the experiments conducted on MSSQ II samples that have impurity-free PLK but defective diffusion barrier. The typical leakage current behaviors measured from MSSQ II samples at as-received and as-moisturized conditions are shown in Figure 5.8, where it can be seen that the moisturization increases the leakage current, which is consistent with our previous observations. However, in contrast to the significant increase in SiCOH samples, the current increase by moisturization in these samples is substantially small, due to the lacking of water soluble impurities trapped in PLK. Furthermore, notice that some samples in this wafer have defective diffusion barrier, the absence of current peak in all testing samples, regardless of the condition of diffusion barrier films, clearly proves the importance of impurities in the occurrence of electrochemical reaction and thus the current peak in voltage ramp test.

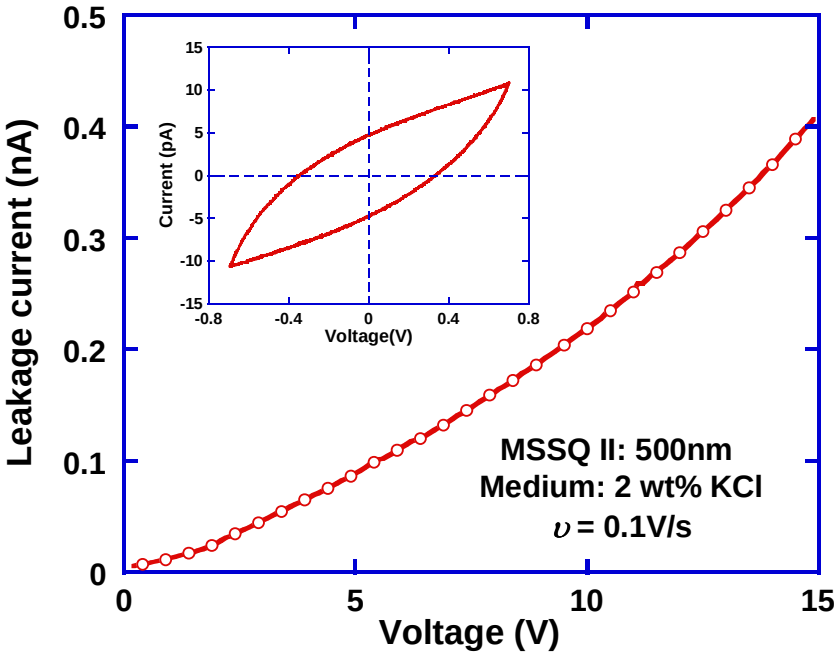


Figure 5.9 A plot showing the typical leakage current behavior from dilute KCl infiltrated MSSQ II samples with intact diffusion barrier.

Even decisive evidences to support this argument can be achieved by the voltage-ramp measurements on KCl solution infiltrated MSSQ II samples. Since it has been demonstrated that KCl solution will not react with Ta diffusion barrier by the results in MSSQ I samples, a few MSSQ II samples were infiltrated with 2 wt% KCl solution to simulate the case of contaminated PLK. Voltammetry measurements were then done to characterize the condition of diffusion barrier, followed by voltage-ramp test. As expected, both intact and defective barrier films were detected. As seen in Figure 5.9, the leakage current from samples with intact diffusion barrier shows a smooth increase with applied voltage and a significantly large magnitude, compared to that in DI water moisturized samples, both of which are consistent with our earlier observations. This also confirms that KCl solution will not react with Ta diffusion barrier in MSSQ II samples. However, when the voltage-ramp measurement is switched to the samples with defective diffusion barrier, a current peak can be observed, as presented in Figure 5.10. This result,

therefore, clearly evidences that the impurities trapped in PLK is equally as important as moisture in inducing the electrochemical reaction and visualizing the reaction current peak in Cu/PLK interconnects.

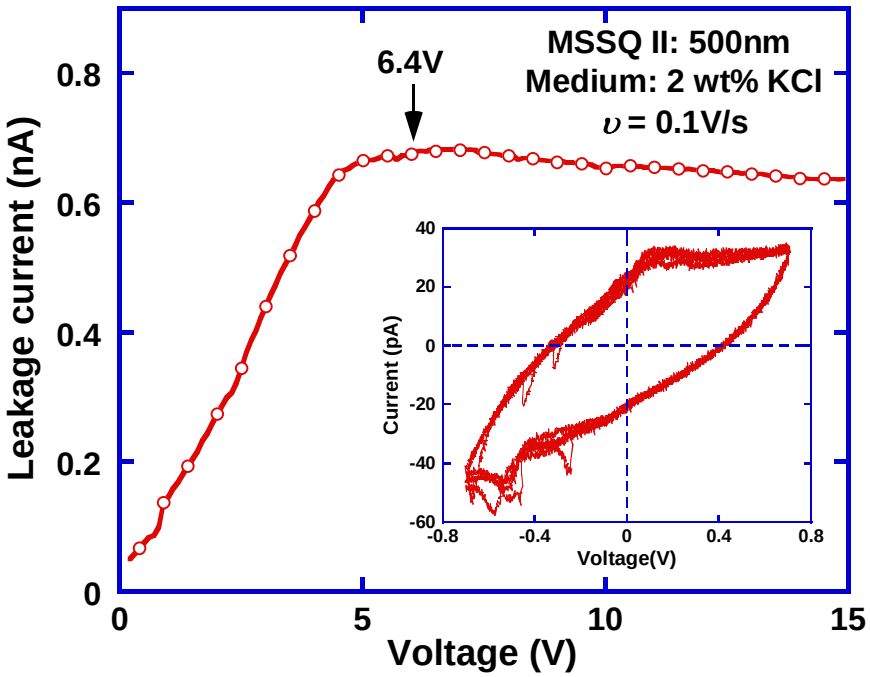


Figure 5.10 A plot showing the typical leakage current behavior from dilute KCl infiltrated MSSQ II samples with defective barrier.

5.3.4 Hydrolysis of Moisture: Hysteresis Collapse

One of the most interesting observations made in this study is the hysteresis collapse after voltage ramp test. Such a behavior, though more significant in reactive samples (with reaction current peak) than in non-reactive samples (without reaction current peak), was consistently observed in all tested samples, suggesting that other than electrochemical reaction, other processes may also take place during voltage-ramp test, and that such processes may be closely related to the behaviors of current peak observed in the consecutive leakage current measurement.

As has been discussed in chapter 2, the hysteresis current is affected by three factors. At fully infiltration condition, the hysteresis current is a reflection of the concentration of activated impurities (mobile ions) and their mobility. Another factor that affects the hysteresis current is the infiltration level in PLK. As infiltration proceeds, more impurities are activated and participate in current delivery in response to the applied voltammetry potential, giving rising to hysteresis enlargement. This hysteresis change continues till the PLK is fully saturated. At this stage, all the trapped impurities in PLK are involved in current transport and the voltammetry hysteresis is saturated as well.

Since all the testing samples are inspected by voltammetry to ensure full infiltration prior to electrical measurements, the hysteresis collapse seen in this study indicates that the impurities, the infiltrated moisture (as the media activating the impurities) or both are lost during voltage ramp test. A way to identify the lost material may be to reinfiltrate the post-stress samples and then conduct similar voltammetry and voltage-ramp measurements. If moisture is lost, it is expected that both the hysteresis in voltammetry measurement and the reaction current peak in voltage ramp test will be partially recovered to as-moisturized condition by moisture reinfiltration, if not fully. If, however, only impurities are lost, such a recovery is not expected to be observed.

In order to gain more insights into the hysteresis collapse, a few post-stress samples were remoisturized and retested at conditions same as the previous test cycles and by the same sequence, i. e. voltammetry and then voltage ramp measurements. Figure 5.11 shows an example of the comparison of voltammetry hysteresises typically from SiCOH samples at as-moisturized, after voltage ramp test, and after reinfiltration conditions. It is clearly seen from this plot that after remoisturization the hysteresis is partially recovered. Similar recovery was also found in the voltage-ramp measurement. As shown in Figure 5.12, both leakage current and current peak voltage are found to be close to the as-moisturized condition.

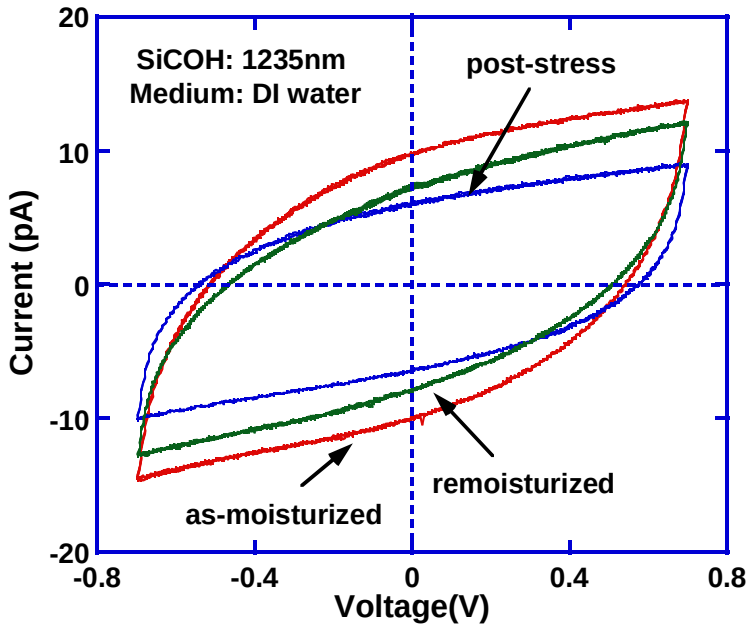


Figure 5.11 A plot showing the comparison of voltammograms in SiCOH samples at as-moisturized, after the first voltage-ramp test, and after DI water reinfiltration conditions

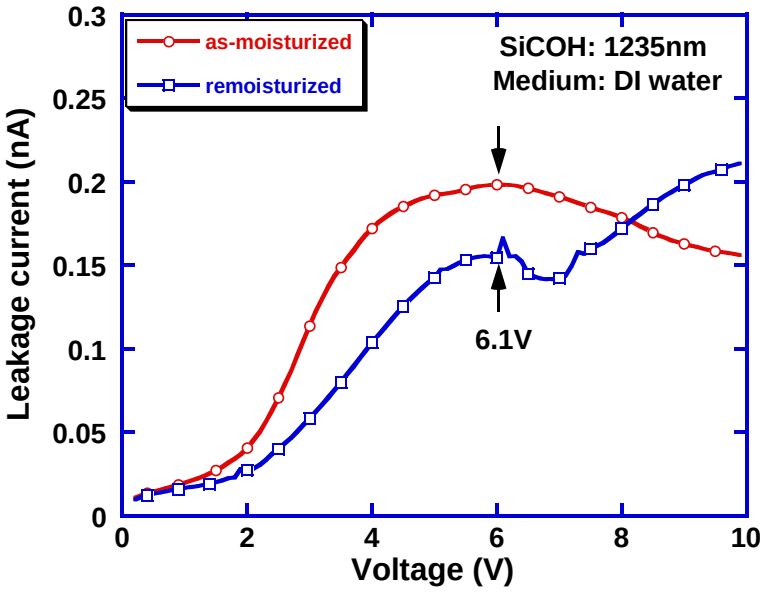


Figure 5.12 A plot showing the comparison of typical leakage current behavior from SiCOH samples at as-moisturized and post-stress remoisturized conditions

A very important inference that can be made from these observations is that the decomposition of moisture does occur during voltage-ramp stress. This is also understandable because though the decomposition rate of pure water is very slow due to its low conductivity, with the presence of a large amount of water-soluble impurities, the conductivity of water can be substantially enhanced, leading to the significant increase of its decomposition rate and thus the loss of moisture in PLK. As this occurs, the electrolyte in PLK may experience two possible changes. The first one is the mobility decrease of impurities and the other is the loss of mobile impurities (by retrapping to PLK). The second case can be viewed as the reverse process of moisture infiltration. In either case, the hysteresis current will decrease and hysteresis collapse can be observed. Although not presented here, similar hysteresis recovery behavior was also observed in non-reactive MSSQ samples. Because there is no reaction occurring in these samples, the loss of impurities by electrochemical reaction is impossible to take place. The collapse of voltammetry hysteresis in both reactive and non-reactive samples, therefore, can be at least partially attributed to the decomposition of moisture during voltage-ramp test.

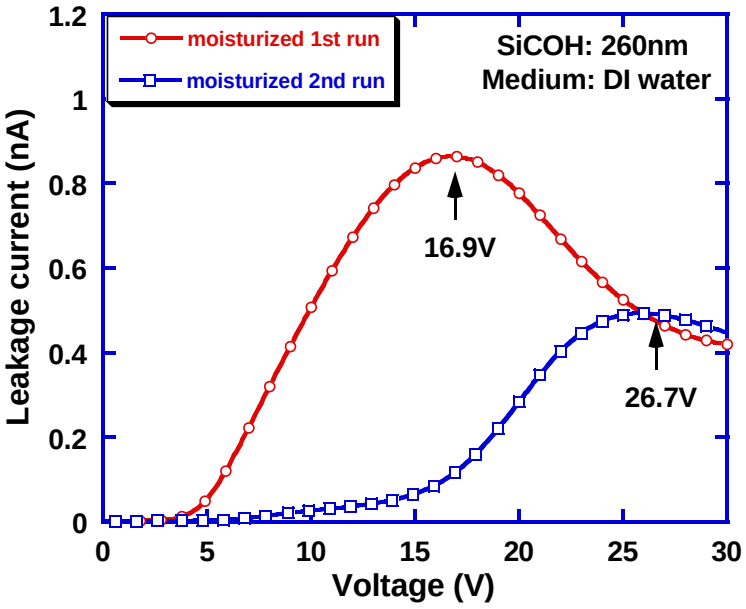
5.3.5 Reaction Kinetics and Current Peak Behaviors

The fact that the current peak shift and peak intensity attenuation is always accompanied with the hysteresis collapse in consecutive voltage-ramp test indicates that there may be an internal relation linking these behaviors. It is our belief that this internal linkage is the change of electrochemical reaction kinetics by the decomposition of moisture, and here we present our understandings at current stage.

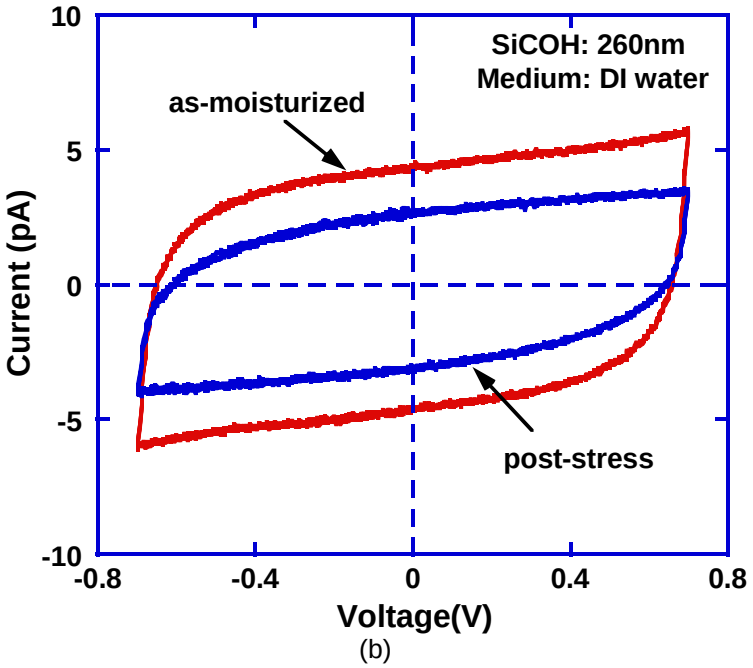
It should be noticed that the standard interconnect structure in the present situation is a two-electrode electrochemical cell. In such a configuration, one electrode is referring to the other and both are acting as working electrode, counter electrode as well as reference electrode when external potential is applied. Since the current seen in the external circuit must go through the electrolyte in PLK from one electrode to the other, the current is a result of the collective behavior of electrochemical reactions at the two electrodes and the migration of ions in the

electrolyte that carrier the overall current. Therefore, totally three processes may control the voltage-current behavior: the reduction and oxidation reactions simultaneously occurring at the electrodes and the drift of ions in PLK to transport the resultant current. Among these processes, we believe that the slow diffusion of ions in PLK is the cause for the high current peak voltage, the current peak shift and the peak intensity attenuation in the consecutive voltage-ramp test. With low ionic concentration and/or diffusivity in PLK, the majority fraction of applied voltage drops inside the PLK bulk (ohmic drop) because the electrolyte is incapable of delivering a high-density current. Such a high voltage drop effectively lowers the voltage seen by the reaction electrodes; only when the applied voltage is high enough such that the voltage drop at the reaction electrode passes the reaction triggering point (standard reaction potential) can electrochemical reaction take place, giving rise to the current peak.

With this theory, the current peak shift and peak intensity attenuation in consecutive voltage ramp measurements can thus be explained. In each single measurement, the loss of moistures by the decomposition decreases the diffusivity or/and the amount of mobile impurities in PLK. As a result, more voltage drop will be taken by PLK in the next measurement and thereby a higher voltage is required to trigger electrochemical reaction, resulting in current peak shift and peak intensity attenuation in the consecutive measurement. Furthermore, this reaction kinetic theory also appears to be consistent with the current peak observed in some SiCOH samples. Exemplified in Figure 5.13 are the leakage current behavior and corresponding voltammetry hysteresis from these samples. Other than the commonly observed characteristics, i. e. the current peak shift, the peak intensity diminishing and the hysteresis collapse, two noteworthy features that are different from the signals in other SiCOH samples shown in Figures 5.2 and 5.3 can be seen in these plots. Compared to the voltammogram in Figure 5.3, these SiCOH samples have much smaller hysteresis current, although exactly same voltammetry test conditions such as ramp rate and potential amplitude have been used. Correspondingly, the current peak occurs at a much higher voltage in the voltage ramp measurement. It should be



(a)



(b)

Figure 5.13 (a) The leakage current behavior from moisturized SiCOH samples with small area hysteresis in voltammetry measurement, and (b) the corresponding voltammetry hysteresis comparison at as-moisturized and post-stress conditions.

pointed out that this difference in hysteresis current is not limited to a specific pattern but observed in different samples randomly picked from the same testing wafer. While the cause for such a difference is presently unclear, possible reasons includes the difference of impurity amount trapped in PLK as well as the porosity change (e. g. pore collapse) during manufacturing processes that decreases the diffusivity of mobile impurities inside. Nonetheless, the consistent observation of the hysteresis current in relation to the current peak voltage strongly indicates that the impurities in PLK will change the reaction kinetics of current peak in voltage ramp measurement, which also seems to be supportive to the theory proposed above.

5.4 Summary

In this chapter, the voltage-ramp method was used to investigate the mechanism of moisture effect on the leakage current behavior in PLK in modern Cu/PLK interconnects. A current peak was observed in the voltage-ramp leakage current measurement. In contrast to previous studies where such a current peak was usually interpreted as the decomposition of moistures, the present work revealed that mechanism of moisture effect on the leakage current behavior of porous low-k is not as simple as previously thought. With the aid of voltammetry technique in characterizing the conditions of PLK and diffusion barrier in testing samples, it has been clearly demonstrated that the mechanism behind the current peak is the electrochemical reaction between the moisture activated impurities and the metal electrode. Two cases, though the materials involved are different, have been found to generate similar current peak by electrochemical reaction in moisturized Cu/PLK interconnects. In the first case that the diffusion barrier film is defective and PLK is contaminated with water-soluble impurities, the electrochemical reaction occurs between exposed Cu and impurity-moisture electrolyte. In the second case where the Ta diffusion barrier is intact but some specific impurity species are trapped in porous low-k, the electrochemical reaction can also take place between the impurities and Ta electrode. The occurrence of such electrochemical reaction and thus the current peak in linear voltage ramp, however, has been further revealed to be impossible if water soluble

impurities do not present in PLK because of the lacking of medium to carrier the resultant high density current. In this regard, the impurities play a role as critical as moisture in the creation of reaction current peak.

Also found is the decomposition of moisture in voltage-ramp test. Due to the presence of impurities, the decomposition of moisture was revealed to substantially accelerated, which is evidenced by the appreciably hysteresis collapse in the consecutive voltage-ramp measurement. Due to the loss of moisture by voltage-ramp stress, the kinetics of electrochemical reaction is changed: a large portion of the applied potential is taken by the electrolyte in PLK, resulting in the current peak shift to a high voltage and peak intensity attenuation in the consecutive voltage-ramp measurement.

CHAPTER 6

CONCLUSIONS AND FUTURE WORK

6.1 Conclusions

The presence of extrinsic factors including moisture and impurities trapped in PLK and the defective diffusion barrier has been decisively evidenced inCu/PLK interconnects by voltammetry technique. In this study, the influence of the extrinsic factors on the leakage current behavior of PLK as well as the associated conduction mechanism has been investigated.

6.1.1 Characterization of Diffusion Barrier and PLK in Cu/PLK Interconnects

The extrinsic factors may commonly exist and coexist in fully executed Cu/PLK interconnects, regardless of the processing techniques and PLK materials. The voltammetry technique with dilute KCl electrolyte as the infiltration medium found that the defective barrier was more frequently observed in the samples located in the wafer edge and in the first level of interconnect patterns because of their inferior diffusion barrier quality. The voltammetry technique with degassed DI water demonstrated that a large amount of water-soluble impurities were trapped in PLK. The sources of such impurities are presently unknown, yet it is highly suspected that several fabrication steps including etching (especially wet etching), ashing and CMP where the PLK with open pore structure is directly exposed to chemicals can introduce such impurities. Due to the existence of water soluble impurities in PLK, the moisture trapped in PLK was also detected by voltammetry technique. Therefore, with appropriate infiltration media, voltammetry technique can be used as a simple yet effective method to characterize the diffusion barrier as well as PLK in advanced Cu/PLK interconnects.

6.1.2 The Signature of Cu Out-diffusion in Leakage Current and Its Associated Mechanism

Cu diffuses out in the form of Cu ions from the diffusion barrier defects into adjacent PLK in the presence of electrical field. The Cu out-diffusion and its subsequent migration in PLK

manifest as a unique current hump that momentarily rise up and fall down in the time-dependent leakage current. Such a current hump behavior appears only at moderate testing conditions, i. e., room temperature and moderate electrical field. Aggressive testing conditions at high temperature and electrical stress tend to make the current hump disappear. The mechanism for this current hump behavior is the space-charge-limited transient current: the out-diffusion Cu ions and their migration interferes the electrical field distribution and thus the voltage drop in PLK, creating a short period of current increase before the arrival of Cu ions to the counter electrode, followed by the current falling down due to the relaxation toward a steady state. Since the current increase reflects the time for Cu ions to migrate from one electrode to the other, the time to the current peak can be used to estimate the Cu ionic mobility in PLK. The Cu ions mobility in the PLKs used in this study is estimated to be as high as $10^{-13}cm^2/V\text{-}sec$ even at room temperature. With such a high mobility and without high-resolution tracking of current, Cu out-diffusion can not be detected by the conventional electrical reliability tests such as TDDB and BTS, because the time to the current peak is too short to detect under their testing conditions.

6.1.3 Study on Electrical Stress Induced Barrier Failure by Step Mode I-t Method

Since the Cu out-diffusion can be characterized as a unique current hump behavior in the time-dependent leakage current, a step mode current-time technique is developed to study the electrical stress induced barrier failure in Cu/PLK interconnects. The diffusion barrier failure is triggered by a critical electrical stress: below a critical point barrier failure will not take place even with a long time stress; above this point, barrier failure and Cu out-diffusion immediately appears, as characterized by the current hump behavior in the step-by-step monitored time-dependent leakage current. Such a critical stress is pattern density dependent due to the pattern density dependent barrier quality created by the thermal cycles during fabrication processes. Due to the thermomechanical property mismatch between Cu and PLK, compressive stress that is primarily determined by the mechanically stronger Cu is developed and acts on the diffusion

barrier during thermal stress, creating barrier roughing and weak spots that favor Cu out-diffusion. For patterns with smaller pattern density, the volume ratio of solid Cu is small and the diffusion barrier experiences less compressive stress and thus has better barrier quality. In contrast, for patterns with higher Cu volume ratio, the developed stress is higher and thus weaker spots can be developed in barrier films.

The proposed step mode I-t method can be used as a technique to detect the barrier quality of Cu/PLK interconnects. It is simple because the barrier quality can be simply characterized by a single electrical measurement. However, in order to effectively utilize this technique, aggressive testing conditions should be avoided because of the high mobility of Cu ions in PLK.

6.1.4 Study on the Mechanism of Moisture Affecting the Leakage Current Behavior

In the presence of impurities and defective diffusion barrier, moisturization creates current peak in the leakage current by voltage-ramp stress. The current peak arises from the electrochemical reaction between the moisture activated impurities and the metallic electrode. For samples with specific impurities trapped in PLK, the electrochemical reaction takes place between impurities and Ta diffusion barrier. For samples with defective barrier films, the electrochemical reaction can occur between the exposed Cu and the electrolyte composed of any impurities that can be activated by moisture. Because high conductive electrolyte is required to carrier the reaction current, the impurities are as equally important as moisture in inducing the electrochemical reaction and thus current peak. Without impurities trapped in PLK, electrochemical reaction will not take place and hence no current peak can be observed.

Although proven not to be the mechanism for the current peak, decomposition of moisture by voltage-ramp stress also occurs and is accelerated due to the presence of moisture in PLK. This is evidenced by the voltammetry hysteresis collapse after voltage ramp test and its partial recovery after moisture reinfiltration. The process alters the kinetics of electrochemical

reaction, resulting in the current peak shift to a higher voltage and the attenuation of current peak intensity in the consecutive voltage ramp measurement.

6.2 Future Work

6.2.1 Electrical Reliability Assessment of Cu/PLK Interconnects

Since the collection of experimental data of time to failure (TTF) under normal operating conditions takes extremely long time and thus is practically impossible, conventional electrical reliability tests, e. g. TDDB, are usually carried out at aggressive testing conditions to accelerate physical failure. Typically, a series of tests at various temperature and electrical filed are performed on the representative interconnects randomly selected from testing wafers. TTF at aggressive testing conditions is then achieved by the resulted statistical failure distribution, which can be used to determine the dependence of failure on testing parameters such as temperature and electrical field. The extracted phenomenological parameters is then used to extrapolating the electrical reliability of interconnects at normal operating conditions. In this extrapolating process, a basic assumption is that the physics of the failure mechanism remains the same under all conditions, ranging from the normal operating conditions to the aggressive testing environments. This assumption, however, may not be true, according to our results made in this study. As has been discussed in chapter 4, two electrical failure mechanisms may coexist in modern Cu/PLK interconnects, depending on the quality of diffusion barrier as well as the applied electrical field. For samples with high quality diffusion barrier, PLK fails prior to barrier failure and Cu out-diffusion. This is the electrical field caused PLK physical failure mechanism. However, for samples with low quality diffusion barrier, diffusion barrier failure followed by Cu out-diffusion occurs before PLK fails. With sufficient Cu out-diffusion, short circuit can be formed inside PLK matrix, resulting electrical failure in Cu/PLK interconnects. This appears to be consistent with the Cu out-diffusion assisted interconnect failure mechanism.

The coexistence of two failure mechanism in Cu/PLK interconnect requires extreme care when carrying out the electrical reliability test, because the failure mechanism may differ

from one testing condition to another and any misjudgment on the failure mechanism will introduce erroneous extrapolation to the accelerated test data, leading to either overoptimistic or overconservative reliability prediction of Cu/PLK interconnects.

In order to ensure the accuracy of lifetime prediction, revealing the true failure mechanism is the key. For this purpose, the step mode I-t method used in this study is recommended prior to reliability test at aggressive conditions. That is, carry out step mode I-t test starting from low electrical stress and room temperature till targeted aggressive testing conditions to determine the possible failure mechanisms. For example, if the current hump behavior is observed below normal operating temperature, Cu out-diffusion is expected to be the failure mechanism from normal use conditions to aggressive testing conditions, and there is no failure mechanism change in this testing range. However, if Cu out-diffusion takes place between the normal use conditions and targeted testing conditions, failure mechanism change is expected. To solve this issue, the target testing conditions has be to adjusted to a more moderate level such that Cu out-diffusion is avoided and PLK failure dominates the failure mechanism in Cu interconnects.

6.2.2 The Influence of Impurities on Leakage Current Behavior and Associated Mechanism

In the conventional electron conduction theory, the influence of defects trapped in dielectrics is usually described by the well-known bulk-controlled FP mechanism where they are assumed to be tightly trapped and thus immobile under the application of an electrical field (see Appendix A). This assumption may hold true for defects tightly trapped by chemical bonds in some dielectrics, but may not be applicable to the impurities trapped in PLK. As has been demonstrated in this study, the impurities trapped in PLK can be easily activated by moisture. Under the application of electrical stress, such impurities can also act as the charge carriers delivering electrical current, and in some specific case, e. g. these trapped in SiCOH PLK samples, react with Ta diffusion barrier. Theoretically, these impurities may also be activated and drift in PLK by the application of electrical stress, though their diffusivity may be slow due to

the high activation energy. When this occurs, not only the properties of PLK bulk will be changed, but also the properties of Ta/PLK interface. This is especially true if reaction occurs between the accumulated impurities and Ta diffusion barrier. It is therefore expected that the conventional FP mechanism may not be able to correctly describe the influence of impurities on the conduction of PLK in Cu/PLK interconnects. Instead, SE may be the true conduction mechanism due to the interface modification by the impurities.

It should be noted however that there are several complications when investigating the influence of trapped impurities on the conduction mechanism of PLK. Other than the conduction mechanism, the drift of impurities will also affect the leakage current behavior when a constant stress is applied. Because of their slow diffusivity, a long time slow decaying current may be observed before the leakage current reaches a steady state. This means that the voltage-ramp method, a technique commonly used for the conduction mechanism investigation in dielectrics, may not be applicable to this special case, because the stress time in the voltage ramp is usually too short for the stressed dielectric to reach the steady state, and therefore, a history dependent leakage current behavior will most likely be observed if consecutive voltage ramp measurements are performed. A possible solution to this problem is the step mode I-t method used in this study. When applying this method, it is strongly recommended that the time-dependent leakage current behavior is monitored in each stress step till the steady state. The leakage current corresponding to each applied stress then takes the steady state value. The current-voltage relationship is obtained by replotting the data from a series of steady-state leakage current verse voltage. In this way, the current decay caused by the impurity drift can be eliminated and the true conduction mechanism can be revealed. A second complication may arise from the fact that it is very difficult to distinguish SE mechanism and FP mechanism, because their similarity in the I-V relationship. Nevertheless, because of the symmetrical structure of comb patterns, a bias flip method may be used to distinguish these two mechanisms. In this method, a positive bias is first applied to the test pattern till steady state,

followed by the removal of bias for a sufficient long time bias off to relax dielectric. A flipped bias is then applied and the time-dependent current is monitored again. Theoretically speaking, because of the symmetrical structure of comb patterns, a symmetrical leakage current behavior is expected, regardless of bias polarity. However, due to the possible modification of Ta/PLK interface by the reaction with arriving impurities during electrical stress, asymmetrical leakage current behavior may be observed. Therefore, if a symmetry time-dependent leakage current behavior is observed, the governing conduction mechanism should be bulk-controlled, i. e. FP mechanism, regardless the presence of impurities and their possible drift in PLK. However, if asymmetrical leakage current behavior appears, the conduction mechanism must be interface-controlled, i. e. SE mechanism.

Combining the two methods discussed above, the influence of impurities on the conduction mechanism may be revealed.

APPENDIX A

CONDUCTION MECHANISMS IN DIELECTRICS

It has been recognized that the current transport in a dielectric can occur via a number of processes including Schottky emission (SE), Frenkel-Poole (FP) emission, direct tunneling (DT), Folwer-Nordheim (FN) tunneling, space-charge-limited (SCL) conduction, ionic conduction as well as some others [196]. These processes can be generally classified as being either bulk-controlled or electrode-controlled. If the current transport is limited by the properties of metal-dielectric interface, e. g. interfacial barrier, the conduction mechanism is said to be electrode-controlled. Instead, if the current transport is limited by the property of the dielectric bulk, the mechanism is bulk-controlled. SE and tunneling processes (both direct tunneling and FP tunneling) belong to interface-controlled mechanism, while SCL conduction, FP emission and ionic conduction fall into bulk-controlled mechanism. In this appendix, the physics of these conduction mechanisms will be briefly introduced. The theory of SCL mechanism will be emphasized because it is adapted to explain the influence of Cu out-diffusion on the leakage current behavior in this study.

A.1 Schottky Emission [196, 197]

Schottky emission is a field enhanced thermionic emission across a metal-dielectric interface where electrons overcome the interfacial barrier and emit into the dielectric. The electron in the dielectric close to the metal plane experiences an electrostatic field as if there were an equal and opposite charge located at the mirror image position of the electron in the metal. The attractive force between the electron and its image charge thus lowers the potential barrier height for electron emission. This image-force-induced barrier lowering is called Schottky effect which is schematically illustrated in Figure A.1. The barrier lowering depends on the electrical field in the dielectric and is therefore a function of applied bias. As a result, the current density of Schottky emission is strongly dependent on two factors: the original interfacial barrier height without image force effect and the electrical field, given by

$$J_{SE} \sim AT^2 \exp\left(\frac{-q\phi_B + \sqrt{q^3 E / 4\pi\varepsilon_i}}{k_B T}\right) \quad \text{(A.1)}$$

where $q\Phi_B$, ε_i, E and A are the original barrier height without image force effect, the dynamic dielectric permittivity, the applied electrical field and the effective Richardson constant, respectively. Other symbols have their usual meanings. The second term in the exponential function arises from Schottky effect. As seen in equation (A.1), the current density of SE is strongly dependent on the interfacial barrier height and hence it is interface-controlled controlled mechanism. When SE dominates current transport, the interfacial barrier height and dynamic permittivity of the dielectric can be extracted by the experimental ln(J) vs. $E^{1/2}$ plot.

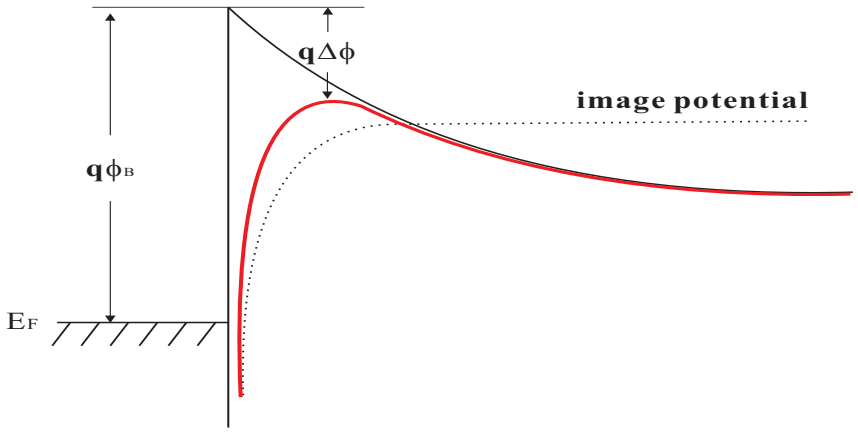


Figure A.1 Energy-band diagram of a metal-dielectric interface illustrating Schottky effect.

A.2 Direct Tunneling and Fowler-Nordheim Tunneling [198, 199]

Tunneling process is another interface-controlled conduction mechanism and essentially a quantum-mechanical effect. When an external bias is applied to a metal-insulator-metal (MIM) structure, the Fermi level of the cathode rises up relative to the anode. If the applied bias is less than the interfacial barrier height, the electron tunneling through a trapezoidal barrier from cathode to anode is called direct tunneling effect. However, if the bias is high enough to exceed the effective barrier height, a triangle barrier is formed and the barrier

thickness is effectively reduced. When this occurs, electrons tunnel through a much thinner barrier into the conduction band of a dielectric and then relax to the counter electrode, yielding Fowler-Nordheim (FN) tunneling. Figure A.2 demonstrates the physical difference between these two tunneling mechanisms.

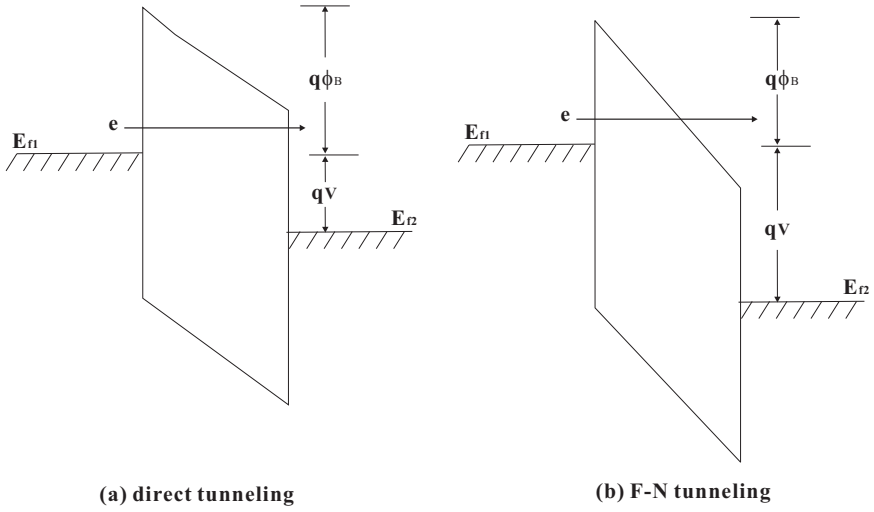


Figure A.2 The physical difference between direct tunneling and F-N tunneling: (a) Direct tunneling, and (b) F-N tunneling

For direct tunneling to occur, an extremely thin layer of dielectric is required (less that 5nm in SiO_2). A typical example where direct tunneling current dominates is the gate oxide in nowadays advanced technology node with extreme thinness. The direct tunneling mechanism, however, is unlikely to take place in current Cu/PLK interconnect due to its relative wide dielectric space. On the other hand, FN tunneling needs very high electrical field such that the barrier is effectively thinned down enough. Since tunneling process is a quantum-mechanical effect (probability issue), the tunneling probability and thus tunneling current are strongly dependent on the energy of tunneling electrons, interfacial barrier height and barrier thickness. Therefore, tunneling mechanisms usually dominate at low temperature regions (usually below room temperature) where thermal energy is not enough to activate other current transport processes. Also because of this, a characteristic that makes the tunneling processes distinctive

from other mechanisms is their “insensitivity” to temperature. A simplified FN tunneling model where the temperature effect is neglected gives the current density

$$J_{FN} = AE^2 \exp(-B/E) \tag{A.2}$$

where A is a proportionality constant and

$$B = 8\pi\sqrt{2m}\phi_B^{3/2}/3hq \tag{A.3}$$

with m the electron effective mass and ϕ_B the interfacial barrier height.

A.3 Space-charge-limited Current [177-180]

The space-charge-limited (SCL) current is a result of the excessive charge carrier injection at the electrode in the presence of electrical field at which the transit time of injected carriers is too short to be relaxed by ohmic dielectric relaxation before they exit the dielectric. In order to observe SCL current, two requirements generally need to be fulfilled: (1) at least one of the electrodes takes ohmic contact so that the excessive charge carrier injection is sufficient as needed; and (2) the dielectric should be relatively free from trap defects because if not so, many injected carriers will occupy empty trap states and thus do not contribute to current flow.

In SCL mechanism, the injected charge carriers are generally not uniformly distributed within the dielectric, which in turn affects the distribution of electrical field and thereby the voltage drop inside. To solve the current transport problem, the current continuity equation and Poisson’s equation need to be solved simultaneously and self-consistently.

A.3.1 Dielectric Relaxation

Dielectric relaxation is a process for a dielectric to relax excessive charge carriers by opposite mobile charges either from material boundary or from a charge reservoir. The dielectric relaxation time can be derived by solving the basic electromagnetic equations

$$dD/dx = \rho_f \tag{A.4}$$

$$D = \varepsilon E \tag{A.5}$$

$$J = \sigma E \tag{A.6}$$

$$dJ / dx = -d\rho_f / dt \tag{A.7}$$

where D, ρ_f, σ, and J are the electrical displacement field, the free charge density, the dielectric conductivity and the current density, respectively. Equation (A.4) is Gauss's law in classic electromagnetic theory and equation (A.7) is the current continuity equation. By solving above equations, the time-dependent charge carrier distribution is

$$\rho_f(x,t) = \rho_f(x,0)\exp[-t/\tau_r] \tag{A.8}$$

with $\tau_r = \varepsilon/\sigma$, the dielectric relaxation time. Equation (A.8) indicates that the injected excessive charges will be neutralized to 1/e with a time period of τ_r.

Consider a MIM structure where the sandwiched dielectric is at thermal equilibrium and has uniformly distributed charge carriers with density n_0. Generally speaking, at any voltage maintained between the cathode and the anode, there is always injection of excessive charge carrier injection from the electrodes. At low voltage (or low current) with a low density of charge injection (i. e., $n_{inj} << n_0$) such that the total amount of charges is not significantly deviated from the equilibrium density, the charge distribution uniformity will not be much disturbed and ohmic conduction is still valid with current density $J = qn_0E$. However, if high voltage is applied such that a large amount of charges are injected, the ohmic conduction is not valid any more because the injected charges can not be relaxed via dielectric relaxation before they exit. While this occurs, the charge distribution and electrical field are not uniform in the dielectric, and the SCL current commences with current flow far in excess of ohmic current, yielding a super linear current-voltage relation.

A.3.2 SCL Steady-state Current

SCL conduction is governed by the current flow equation and Poisson's equation. In a simplified SCLC theory ignoring diffusion current and trapping effect, these two equations are

$$J = q\mu n(x)E(x) \tag{A.9}$$

$$d^2\phi(x)/dx^2 = qn/\varepsilon \tag{A.10}$$

where ϕ is the electrical potential. For the sake of simplicity yet not lose the generality, only one carrier injection (e. g. electron) at the cathode is considered, which is also called unipolar injection in SCL theory. In addition, the charge carrier velocity is assumed to be linearly proportional to electrical field v(x) = μE(x). This holds true provided that the applied electrical field is not too high. Since the injection electrode is ohmic contact and diffusion current is neglected, boundary condition E = 0 applies to this electrode. Notice that at steady-state, J = constant (continuity equation), the above equations can then be solved

$$J = \varepsilon\mu\frac{V^2}{L^3}; \qquad n = \left[\frac{\varepsilon J}{2q^2\mu}\right]^{1/2} x^{-1/2}; \qquad E = -\left[\frac{2J}{\varepsilon\mu}\right]^{1/2} x^{1/2} \tag{A.11}$$

here V is the applied voltage between the two electrodes

$$V = -\int_0^L E(x)dx \tag{A.12}$$

It is clear seen from the results in (A.11) that the electrical field and the charge distribution are not uniform in the dielectric, which significantly differs from ohmic behavior. The current-voltage relation derived above is called Mott-Guerney law.

A.3.3 SCL Transient Current

While the steady-state SCL current reflects the time-independent current flowing in dielectrics, the transient current is a result of a time-dependent process for the injected charges to relax toward the steady-state, during which the field inside the dielectric, the charge distribution and thus the current flow are functions of time.

The basic equations that govern the time-dependence of the injection current are the total current equation

$$j(t) = j_{cond} + j_{displ} \tag{A.13}$$

and the Poisson equation

$$\varepsilon \partial E(x,t)/\partial x = qn(x,t) \tag{A.14}$$

where

$$j_{cond}(x,t) = qn(x,t)\mu E(x,t), \qquad j_{displ}(x,t) = \varepsilon \partial E(x,t)/\partial t \tag{A.15}$$

are the conduction current and the displacement current, respectively. Physically, the first equation is the electrical current of moving charges and the second equation is the variation of electrical field but not necessarily involves any movement of charges. As will be seen later, in the transient process before the injected charges reach the other electrode, only the displacement current contributes to the total current, because over this time interval the conduction current whose evaluation involves both electrodes is identically zero.

When charges, for example, electrons, are injected from the cathode, the electrical fields at the cathode and the anode are related to each other through the total amount of injected charges Q(t) per unit area. From Gauss's theorem

$$E_c(t) = E_a(t) - Q(t)/\varepsilon \tag{A.16}$$

Substituting Eq. (A.14) into Eq. (A.15)

$$j(t) = \varepsilon\left[\frac{\mu}{2}\frac{\partial^2 E(x,t)}{\partial t} + \frac{\partial E(x,t)}{\partial t}\right] \tag{A.17}$$

Integrating this equation from the cathode to the anode

$$j(t) = (\varepsilon\mu/2L)\left[E_a^2(t) - E_c^2(t)\right] \tag{A.18}$$

Here the relation dV/dt=0 is used, since the applied voltage is maintained at constant. Eq. (A.18) can be rewritten as

$$j(t) = \left[\mu Q(t)/2L\right]\left[2E_a(t) - Q(t)/\varepsilon\right] \tag{A.19}$$

From this equation it can be seen that the transient current variation is determined by two factors: the injected charges and the electrical field at the anode, both of which are time-dependent.

A.3.3.1 Space-charge-free Transient

Two extreme cases will be discussed here. The first case is a small amount of charge injection from the cathode where Q(t) is constant, independent of time. Since Q is very small, the electrical field in the dielectric will not be much interfered by the injected charges and can be assumed to be uniform, and therefore, $E_a=E_c=V/L$. Using the relation $Q=\varepsilon E=\varepsilon E_a=\varepsilon E_c$, then

$$j(t) = j = \mu QV / L^2 \tag{A.20}$$

Since the charges are injected at the cathode interface, the transit time for them to reach the anode is determined by

$$L = \int_0^t \mu E dt$$

which gives

$$t_0 = L^2 / \mu V \tag{A.21}$$

The transient current can then rewritten into a very familiar form

$$j = Q / t_0 \tag{A.22}$$

This is understandable since there is little interference between the injected charges and the electrical field, the injected charges can move freely inside the dielectric and hence the transient current is entirely determined by their mobility. Because of this, the current resulted from this small amount of charge injection is called space-charge-free transient current.

Theoretically, because the charge injection is instantaneous, the transient current can persist up to t_0. Thereafter, the current drops suddenly to zero once the injected charges reach the anode. Therefore, the current-time curve will be a horizontal straight line with a sudden drop at t_0, and the injected charges will move in the dielectric like a charge sheet. However, with

diffusion taken into account, the injected charges will spread out during migration in the dielectric. Nevertheless, the total amount of injected charges, however, is maintained at a constant when they are far away from the counter electrode, and thus the current is still a constant. However, once they approach the counter electrode, part of the injected charges will be transport to the external circuit due to the spreading out, resulting in a gradual decrease of transient current till all the injected charges are guided to the external circuit. When this occurs, the current becomes zero. The whole process is schematically shown in Figure A.3 (a).

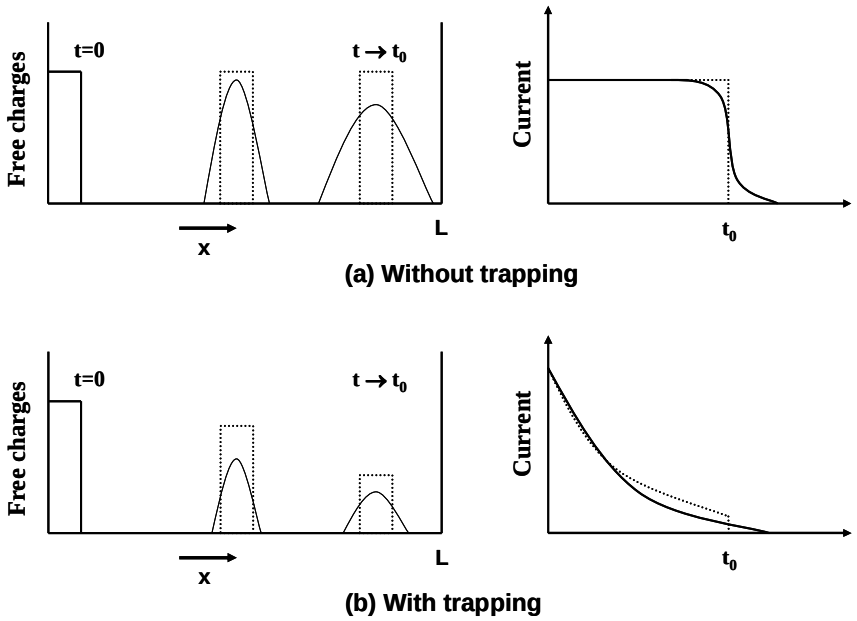


Figure A.3 Schematic plots showing the time-dependent evolution of injected charges and the resulting transient current in the space-charge-free transient case: (a) in the absence of trapping; and (b) with trapping and ohmic relaxation. The dashing lines correspond to the approximation of ignoring charge diffusion.

In practice, due to charge trapping and ohmic relaxation, there is an attenuation of Q during the transit. As a result, the current will naturally decrease over the time interval $0<t<t_0$. This process is also shown in Figure A.3.(b).

A.3.3.2 Space-charge-limited Transient

The second case is a large amount of charge injection. In this case, SCL transient current which is distinctively different from the behavior shown in Figure A.3 is obtained. With diffusion current ignored, the boundary condition at the injection electrode, i. e. the cathode, is

$$E_c(t) = 0 \tag{A.23}$$

because otherwise a current singularity will occur at the injecting cathode. The basic equation governing the current flow is still Eq. (A. 13) and thus Eq. (A.18) is valid. Substituting Eq. (A.23) into Eq. (A.18)

$$j(t) = \varepsilon\mu E_a^2(t)/2L \tag{A.24}$$

As mentioned earlier, over the transit time before the injection charges reach the anode, the conduction current is zero and therefore the total current is determined by the displacement current. Considering the current behavior over this time interval, $0<t<t_1$, where t_1 is the transit time for the injected charges travel through the dielectric from the injection electrode to the counter electrode. Also notice that between the moving front of injected charges and the counter electrode, the electrical field is uniform because there is no free charges in-between. With Eqs. (A.13) and (A.15), Eq. (A.24) becomes

$$dE_a / E_a^2 = \mu dt / 2L \tag{A.25}$$

with initial condition $E_a(t=0)=V/L$. This is because at t = 0, there is no injected charge in the dielectric. The solution to this equation is then

$$E_a(t) = \frac{V}{L}\frac{1}{1-t/2t_0}, \qquad t_0 = L^2/\mu V \tag{A.26}$$

and

$$Q(t) = \frac{Q_0}{1-t/2t_0}, \quad Q_0 = \varepsilon V/L; \qquad j(t) = \frac{j_0}{(1-t/2t_0)^2} \quad j_0 = j(0) = \varepsilon\mu V^2/2L^3 \tag{A.27}$$

The transit time t_1 is obtained by utilizing the following equation

$$L = \int_0^{t_1} E_a(t)dt$$

Substituting Eq. (A.26) into this equation

$$\tau = 2(1-e^{-0.5})t_0 \cong 0.786t_0 \qquad \text{(A.28)}$$

Now from these results, two important characteristics of the transient current can be obtained:

(1) the transit time for the injected charges traveling from the injecting electrode to the counter electrode is less than t_0, the time for space-charge-free transient, as seen from Eq. (A.28)

(2) at time t_1, the transient current reaches its maximal

$$j(t_1)/\, j(0) \cong 2.72; \qquad j(t_1)/\, j_\infty = 1.21$$

where j_∞ is the steady state current.

Figure A.4 schematically shows these characteristic features of the trap-free transient current Also displayed is the trapping effect on the transient current behavior, whose theoretical details can be found in Refs. [179] and [180].

Physically, the SCL transient current behavior can be understood as follows. With the application of a constant voltage at the electrode, a massive amount of electrons that is far beyond the thermal equilibrium electron density is allowed to enter the dielectric, giving rise to the initial current increase. As injection continually proceeds, the initially injected electrons move against the applied electrical field followed by an electronic cloud between the moving front and the cathode. Since there are no electrons between the leading front and the anode, the field between the leading front and the anode is uniform and equals to the field at the anode. As more electrons advance into the dielectric, the field at the anode that pulls the electron leading front keeps growing. This can be effectively imaged as a MIM capacitor whose dielectric space is continuously narrowing down yet the two electrodes are maintained at a constant voltage. Because of this growing electrical field, the current continuously increases. This current increase, however, can only persist up to time τ, at which the leading front reaches the anode,

leaving behind a uniformly distributed electronic cloud. Recalling that at the steady-state, the charge distribution monotonically decreases between the electrodes to maintain a constant steady-state current J=μn(x)E(x)=constant. The greater uniformity of charge distribution in the dielectric obviously means that there is a space charge overshoot occurring at the time the injected electron leading front arrives the cathode. In other words, the injected electrons in the dielectric at this time are more than allowed at the steady state. Therefore, once the leading front arrives at the anode, the dielectric contains the maximum amount of space charges and the current reaches its peak value. Thereafter, the current has to decay to its steady-state and the space charge distribution relaxes to it steady-state configuration.

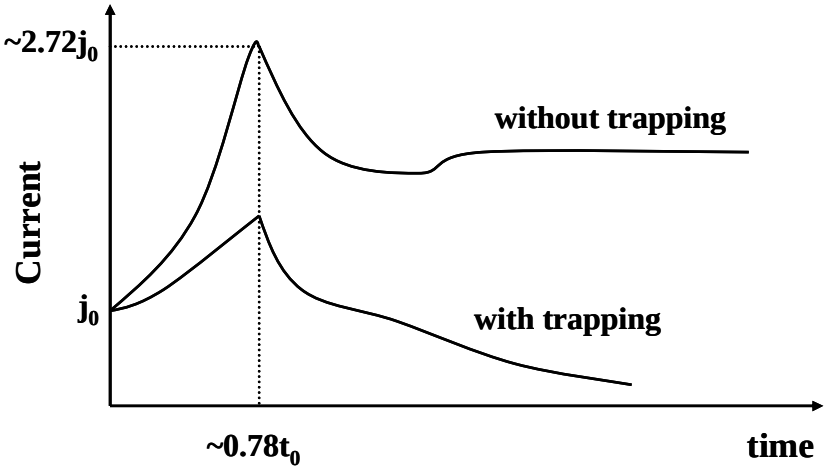


Figure A.4 A schematic plot showing the space-charge-limited transient current responses in the cases of without and with trapping. The trapping effect exemplified here corresponds to a moderate trapping, i. e, the trapping time is not significantly larger than the space-charge-free transit time t_0.

As the time for the leading front to reach the anode depends on the migration rate of the injected charge carriers, the time to the current peak is a reflection of the charge mobility in the dielectric. Thus, the SCL transient current mechanism essentially describes a migration-controlled current transport process. Rewriting Equation (A.28),

$$\tau = 0.78\frac{L^2}{\mu V} = 0.78\frac{L}{\mu E} \tag{A.29}$$

It is readily seen that based on experimental data the mobility of injected charge carriers can be extracted.

A.4 Frenkel-Poole Emission [197, 200]

Frenkel-Poole (FP) emission is a typical bulk-controlled mechanism that shares similar physical essence with SE in that both arise from the field-enhanced thermal excitation of electrons. However, the barrier lowering effect in FP emission occurs inside the dielectric bulk rather than at the interface, as in SE. In this respect, FP emission is also known as internal SE. In FP emission, the barrier to be overcome is the Coulombic potential well generated by the electron traps inside a dielectric. When an electrical field is applied, the lowering of potential well increases the excitation rate of electrons into the dielectric conduction band, resulting in an enhancement of current density. The physics of FP mechanism can be demonstrated in Figure A.5 and the FP emission current density is given by

$$J \sim E\exp\left(\frac{-q\phi_B + \sqrt{q^3 E/\pi\varepsilon_i}}{k_B T}\right) \tag{A.30}$$

This expression is virtually identical to that of SE. It however should be noticed that the barrier lowering quantity of FP emission is larger than that of Schottky emission by a factor of 2, as seen in Equation (A.1) and Equation (A.29). This is because in FP emission the trap center is assumed to be immobile. In contrast, the image charge in SE mechanism is mirror-symmetrical to the moving electron and hence “mobile”. Because of their similarity, it is extremely difficult to distinguish which process dominates the current conduction simply by J-E curve fitting if the dynamical permittivity is unknown. Experimentally, two methods are commonly combined to distinguish these two mechanisms. One is the thickness-dependent leakage current study and the other is polarity-dependent leakage current behaviors. While the electrode-controlled (SE)

mechanism is thickness-independent but polarity-dependent, the bulk-controlled (FP) mechanism shows thickness-dependent but polarity-independent behaviors.

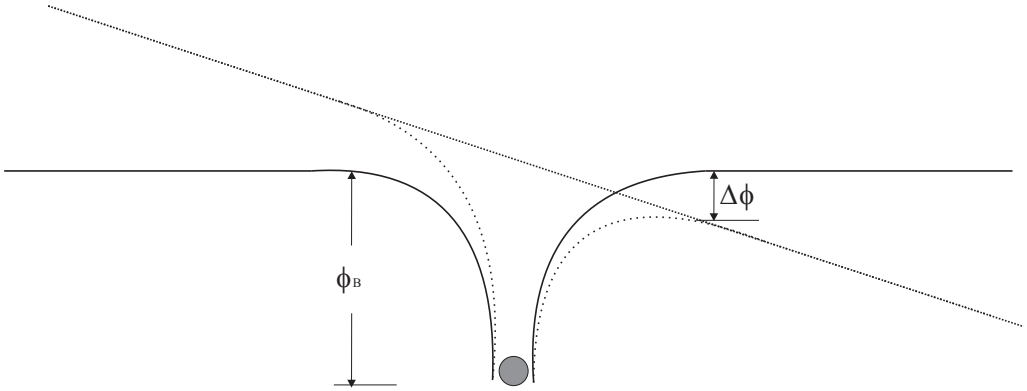


Figure A.5 The physical picture of FP mechanism. Solid lines denote the potential well Φ_B generated by a trap center with the absence of an electrical field. Dashed lines show the electrical field effect that lowers the potential barrier by $\Delta\Phi$.

A.5 Ionic Conduction [196, 201, 202]

In essence, ionic conduction is the diffusion process of mobile ions in a dielectric under the influence of external electrical field. According to ohm's law, the ionic conduction current density is given by

$$J = nq\mu E \tag{A.31}$$

where n, q, μ E are ionic concentration, unit charge, ionic mobility and applied electrical field, respectively. From Nernst-Einstein equation, the ionic mobility at temperature T is related to the ionic diffusivity by

$$\mu = Dq / k_B T \tag{A.32}$$

Here k_B is Boltzmann constant; D is the self-diffusivity of mobile ions and can be expressed in Arrhenius form

$$D = D_0 \exp(-E_a / k_B T) \tag{A.33}$$

where D_0 is the proportionality diffusion constant that has accounted for the probability of one ion successfully jumping from its original site to the next accessible site and E_a is the activation energy required for overcome diffusion energy barrier. The ionic current density is then given by

$$J = \frac{nq^2 D_0 E}{k_B T} \exp(-E_a / k_B T) \tag{A.34}$$

Since the ionic current is strongly dependent on the ionic diffusivity and activation energy in dielectric bulk, ionic conduction is one of the bulk-controlled mechanisms.

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