A HIGH FILL FACTOR CMOS IMAGE SENSOR FOR IR CAMERA APPLICATIONS

by

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ABSTRACT

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FOR IR CAMERA APPLICATIONS

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In this thesis, a unit cell for high-SNR applications is presented. The proposed circuit is significantly smaller than other circuits that perform dark current subtraction because less circuitry is used inside the unit cell. The proposed circuit uses only two transistors and one resistor inside each unit cell to suppress the dark current. The size of the circuit in the layout is 25 x 25 μm^2. With this new unit cell and routing approach, the size of the unit cell was reduced by 300% compared to other circuits which also suppress dark current.

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CHAPTER 1

INTRODUCTION

Infrared imaging systems have been developed for many applications including search and track, medical examination, astronomy, forward-looking infrared systems, missile guidance, and surveillance. The infrared focal plane array (IR FPA) can be divided into two main parts, the detector array and the readout electronics. Compared to discrete design, the IR FPA has the inherent advantages of high packing density, low cost, reduced signal leads through the dewar, high feasibility on-chip signal processing, and high flexibility for system integration. To achieve the optimal system performance, tradeoffs must be made among circuit performance, power dissipation, and chip size [1].

Various types of infrared detectors have been developed to convert incident infrared radiation into electrical signals. The two major classes are photon detectors and thermal detectors. In the photon detectors, incident photons create electron-hole pairs near the depletion region of the semiconductor, which produces a current, voltage, or resistance change in the detector. The sensitivity of photon detectors depends on the spectral absorption and photo excitation. The spectral response depends on the energy gap of the semiconductor and the optical radiation wavelength. In thermal detectors, incident radiation is absorbed by the crystal lattice of the material. This changes the temperature of the material, which changes the physical or electrical property of the detector. Most thermal detectors operate at room temperature and have a wide spectral response. Because the operation involves changes in temperature, they have a slow response time and relatively low sensitivity compared to photo detectors [1].

The readout integrated circuits (ROIC) integrate the photocurrent generated by the detectors and multiplex the outputs off chip. The ROIC consists of three main components: pixel-

level input circuits which integrate the photocurrent into a voltage, analog circuits that multiplex the sampled voltage to output stages, and output buffers which drive the voltages off-chip [2].

The ROIC should provide a stable and near zero detector bias voltage to reduce the dark current and detector noise. It should also have small input impedance to obtain high injection efficiency for integrating the maximum amount of photo current, increasing the detector's bandwidth, and decreasing the detector's input referred noise. It should also have large dynamic range to increase the charge storage capacity [3].

High dynamic range imaging has applications in the automotive, surveillance, tactical, industrial, and medical areas. The system must be able to capture scenes which have large variations in irradiance due to object temperatures. The system must also be able to deal with scene disturbances such as sun reflection. One demanding scenario that exemplifies the need for precision imaging is one that involves scenes that have small variations in temperatures around a much larger background temperature. For example, for imaging the human body, the target temperature range is only a few Kelvin around a nominal background of approximately 300K. So, sensitivity is critical, necessitating ROICs that have high signal to noise ratio (SNR) [4].

Methods that extend the dynamic range (DR) or SNR at the high end can do so by adapting the integration time to pixel photo current, which provides long integration times for pixels with small photo currents and short integration times for pixels with high photo currents. Multiple capture can achieve high DR and SNR by sampling the signal nondestructively multiple times during integration. Synchronous self-reset with residue readout improves the DR but does not improve the SNR [4]. Background suppression and adaptive gain control techniques can also be used to improve DR and SNR. Background suppression can be realized using charge-domain background suppression or current-memory based background suppression [5].

Background suppression can be realized using current-memory or a blind photo diode in each pixel. In [6-8], memory was used to suppression the dark current. The pixel size was increased because extra capacitors and transistors had to added to the unit cell in order to

memorize the dark current during the calibration cycle. In [9], a blind photo diode was used in each unit cell, and the blind photo diode increased the pixel size.

The proposed ROIC uses a blind photo diode that is placed outside the pixel, and the dark current is routed to each unit cell using current mirrors. Inside the unit cell, only two transistors and one resistor have to be added to in order to suppress the dark current. The size of the circuit in the layout is 25 x 25 μm^2. With this new unit cell and routing approach, the size of the unit cell was reduced by 300% compared to [6-9].

This thesis is organized as follows. Chapter 1 provides a brief introduction to IR systems. It discusses the operation of the IR detector and performance criteria. It also provides motivation for the work that is performed. Chapter 2 provides background material related to types of IR materials, readout circuits, dark current, and high-SNR architectures. Chapter 3 discusses the proposed circuit design. Chapter 4 discusses the results obtained from the simulations. Chapter 5 provides conclusions and future work.

CHAPTER 2

BACKGROUND

2.1 Performance Measures

There are many performance measures for ROICS. Tradeoffs must be made when designing a ROIC because many of the measures are contradictory. For example, the size of the unit cell should be minimized in order to improve the quality of the image, but reducing the size of the unit cell often requires using architectures which have higher noise or lower detector frequency response.

The injection efficiency is defined as the ratio of the current flowing into the readout circuit to the detector current. The detector bandwidth is defined as the maximum rate at which the detector can respond to changes in photon flux. High injection efficiency and wide input bandwidth improve the sensitivity of the readout circuit. To increase the injection efficiency and bandwidth, the input impedance of the interface circuit should be lower than the shunt resistance of the IR detector [1].

Charge storage capacity is determined by both the background and dark current levels of IR detectors and the value of the integration capacitor. The charge storage capacity should be increased in order to improve the SNR. High charge storage capacity can be achieved by reducing the magnitude of the background and dark currents and by using a large integration capacitor [1].

The dynamic range is defined as ratio of the maximum photo current to the total noise. The required dynamic range is determined by the ratio of the largest incident photon flux to the minimum photon flux. The dynamic range should be maximized, but its magnitude is limited by the storage capacity, linearity, and total noise [1].

The frame rate is chosen according to the specific IR system requirements. For example, frame rates of 30-60Hz are typical for consumer video cameras. Frame rates above 1kHz are

typical for military and space applications. Increasing the frame rate is also necessary in order to implement some signal processing functions such as color reconstruction and image compression [1].

When incident photons are absorbed by the IR material, the material's physical properties such as density of carriers in the conduction band, resistivity, or dielectric constant will change. Signal integration occurs when the readout electronics sample the change in the material's properties. Generally, the saturation frequency of the integration capacitor and the detector sensitivity determine the proper length of integration time [1].

The sizes of the array and unit cell are usually determined by the fabrication technology and the type of the IR detector material. Higher image resolution requires larger arrays and smaller pixels. However, increasing the size of the pixel also decreases the size of the integration capacitor. Because the size of the integration capacitor reduces, the integration time must be reduced, which will reduce the SNR [1].

The power dissipation is limited by the loading of the cooling system. As the power dissipation increasing, the cost of the cooling system increase. So, the power dissipation should be minimized [1].

The operating temperature is determined by the detected wavelength region and the type of IR material. Each type of IR material has its own operating temperature. For example, ternary alloys such as HgCdTe often operate below 100K so that the thermal dark current is reduced. Bolometer materials, however, often operate between -40C and 100C [1].

The dark current, injection efficiency, detector 1/f noise, and responsivity are affected by the detector bias. The operation ability and linearity of the spectral response are also affected by the bias. So, the detector bias should be reduced and its magnitude should be stable [1].

2.2 Types of Infrared Detectors

Infrared detectors fall into two broad categories, photon and thermal. In the classical photon detector, photons are absorbed by the detector material and generate free electrons, which are sensed by the ROIC. If the carriers are majority carriers, then the sensing is photoconductive in nature. For minority carriers, both photo conductive and photovoltaic modes of

detection can be utilized. The thermal detector is a power law detector. The incident photons are absorbed by a thermally isolated detector element, which increases the temperature of the element. This change is sensed by a parameter such as resistivity or dielectric constant [11].

2.2.1 Infrared Photon Detectors

There are four main types of photon detectors: direct band semiconductors, extrinsic semiconductors, Type I supperlattices, and Silicon Schottky barriers. Each type of material is either a majority or minority carrier device. A majority carrier is the electron, and the minority carrier is the hole [11].

The direct bandgap semiconductor is a minority device. Examples of this type of material include binary alloys, ternary alloys, Type II supperlattices, and Type III supperlattices. The ultimate limit on lifetime in a direct gap semiconductor is determined by band-to-band recombination, which can occur by either radiative or Auger processes [12].

The extrinsic semiconductor is a majority carrier device. Examples include Si:Ga and Ge:Hg. Because the intrinsic material has been doped with impurities, many of the device parameters depend on the dopant concentrations. For example, the carrier concentration, majority carrier lifetime, carrier thermal velocity, ionization energy, and absorption coefficient depend on the donor and acceptor concentrations [13].

The classic example of a Type I super lattice is the GaAs/AlGaAs Quantum Well Infrared Photodetector (QWIP). With this type of device, IR absorption is achieved by transitions between energy levels induced in the majority carrier conduction band by dimensional quantization. The AlGaAs layers are thick, and they serve the dual purpose of providing geometrical confinement and quantization. The IR signal is detected as a photoconductive current, and the QWIP is a majority carrier device [14].

Silicon Schottky barriers are primarily majority carrier devices. Examples include PtSi and IrSi. The IR absorption in the material causes electron transport across a metal-semiconductor barrier. When the incident radiation is absorbed by the material, the carriers must be transported

to the barrier with enough energy to cross the barrier. The carriers escape over the barrier and are detected in the external circuit [15].

Optimum performance of a photon detector occurs when the temperature dependence of the parameter is large enough that the limiting noise of the thermal detector is determined by thermal fluctuations with the surroundings. This is designated as Background Limited Performance (BLIP) [11].

The condition for BLIP is given by:

$$\frac{\eta_\alpha \Phi_B \tau}{t} > n_{th} \tag{2.1}$$

Φ_B is the background flux, η_α is the absorption coefficient, τ is the carrier lifetime, t is the thickness of the material, and n_{th} is the density of thermal carriers. For BLIP, the photon generation rate per unit area must be greater than $n_{th}t/\tau$, the thermal generation rate per unit area. For $\eta_a \sim \alpha t$, where α is the material absorption coefficient, the requirement for BLIP is $\Phi_B > n_{th}/\alpha\tau$. The normalized thermal generation rate is defined as [11]:

$$G_{th} = \frac{n_{th}}{\alpha\tau} \tag{2.2}$$

The normalized thermal generation rate can be utilized to predict the ultimate performance of different materials as a function of temperature [11].

The sensitivity of a detector can be expressed in many ways. However, the limiting factor is the fluctuation of the relevant carrier concentration because this determines the minimum observable signal of the detector. This fluctuation can be modeled by assuming that the detector current is integrated on a capacitive node, and the variance is given by [11]:

$$N^{1/2} = g\sqrt{(I_d + I_\Phi)\tau/q} \tag{2.3}$$

I_d is the dark current, I_Φ is the background flux current, g is the gain, q is the electron charge, and τ is the integration time. The minimum observable, or noise equivalent flux is given by [11]:

$$N^{1/2} = g\Delta\Phi\eta\tau A \tag{2.4}$$

A is the area of the detector and η is the overall quantum efficiency of the detector. The noise equivalent flux is given by [11]:

$$\Delta\Phi = g(1 + I_d/I_\Phi)\Phi_B/N^{1/2} \quad (2.5)$$

The sensitivity can be expressed as a temperature difference by considering that $\Delta\Phi = \Delta T(d\Phi_B/dT)$. Then the noise equivalent temperature difference is defined as [11]:

$$NE\Delta T = \frac{g(1+I_d/I_\Phi)\Phi_B}{(d\Phi_B/dT)\cdot N^{1/2}} \quad (2.6)$$

The above expressions contain specific system and detector quantities such as area and bandwidth. These quantities can be eliminated by normalization, resulting in the detector detectivity, D*, which is defined as:

$$D^* = \sqrt{\eta/2(G_{th} + \Phi_B)}/h\nu \quad (2.7)$$

The normalized thermal generation rate is a critical factor in determining the potential D* of the detector material [11].

2.2.2 Infrared Thermal Detectors

The resistance bolometer for detection of thermal radiation is a micro machined device with a resistance that changes corresponding to the amount of absorbed IR radiation. Incident IR radiation heats the detector and changes its resistance. The detector must be thermally isolated from chip, and this is usually accomplished by suspending the bolometer above the chip surface. The detector must be electrically biased in order to be able to readout the detector data in the form of a resistance change [16].

Figures of merit for thermal detectors include radiant responsivity, speed of response, noise equivalent temperature difference, thermal fluctuation noise, Johnson noise, and thermal conductance. The electrical resistance of the individual detector elements is determined by the value of the electrical resistivity of the heat sensitive material in the detector with its physical dimensions. In contemporary designs, infrared absorption is achieved either by incorporating into the design a single metal film that has a sheet resistance of 187Ω per square or a metal film of sheet resistance 377Ω per square [17].

The vanadium oxide thin films have temperature coefficient of resistance (TCR) in the range of 2%/K to 3%/K at room temperature. There are many phases in vanadium oxides, such as VO_2, V_20_5, and V_2O_3. They undergo transition from an insulator or semiconductor to a metal

phase at a specific temperature. Commonly used techniques such as evaporation and sputtering will create amorphous or polycrystalline films. Because high electrical resistance of the device results in a high level of noise, the use of the V_2O_3 phase showing low resistance is important to the fabrication of low-noise micro bolometers. The maximum TCR achieved so far was 5.12%/K using a reactive pulsed laser deposition method to fabricate the device [18].

Amorphous silicon bolometers are used in a variety of products, such as thin-film transistors, photovoltaic devices, and solar cells. The hydrogenated arrays take advantage of the high TCR, relatively high optical absorption coefficient, and the advantage that they can be manufactured using silicon fabrication processes. TCR values up to 3%/K at room temperature have been obtained. Bolometers made of amorphous silicon can consist of very thin membranes, which allows for a low thermal mass and consequently, for bolometers with a low thermal conductance while maintaining a fixed thermal time constant [18].

Theoretically, the temperature sensitivity of the material is large enough that all noise sources other than temperature fluctuations can be ignored. Then, the power fluctuation of the element is given by [11]:

$$\Delta W_n = \sqrt{4kT^2 G_{th} \Delta f} \tag{2.8}$$

So, the detectivity is given by:

$$D^* = \sqrt{\eta^2 A/(4kT^2 G_{th})} \tag{2.9}$$

This value of D* is impressive, but it only provides a limited insight into the suitability of the thermal detector for specific applications. Signal and spectral bandwidth requirements are also important, and NEΔT must also be considered. NEΔT is given by:

$$NE\Delta T = \sqrt{\frac{2kT^2}{C_{th}\cdot(1-exp(-\tau_{int}/R_{th}C_{th}))(R_{th}\cdot dp/dT)^2}} \tag{2.10}$$

Where dp/dT is the differential change in radiated power per scene temperature change in the spectral region of interest, and τ_{int} is the integration time. Image smearing considerations require $\tau_{int} \sim 2R_{th}C_{th}$, where the maximum value of R_{th} is given by the radiative coupling. For a required

system integration time, the only independent variable is the heart capacity, C_{th}. For most detectors, there is a finite limit on thickness and volumetric specific heat [11].

2.3 Readout Circuits

Readout electronics are designed to support a good interface between the IR detectors and the signal processing stages. Generally, the pixel pitch is reduced with the increasing array size. Also, the total power dissipation is limited by the image system. These two factors put constraints on the circuit design and complexity. So, the design of the readout electronics requires tradeoffs between circuit performance and complexity [1].

There are many criteria which must be considered when designing a readout circuit. These include the noise, location of the integration capacitor, power per unit cell, detector bias uniformity, and unit cell (UC) area. Tradeoffs must be made when the readout circuit is designed. For example, the unit cell size can be decreased by placing the integration capacitor outside the unit cell, but this would decrease the frame rate because only one column of pixels could be integrated at one time. Also, the power per unit cell can be lowered by decreasing the number of transistors inside each unit cell, but this increases the detector bias non-uniformity [1].

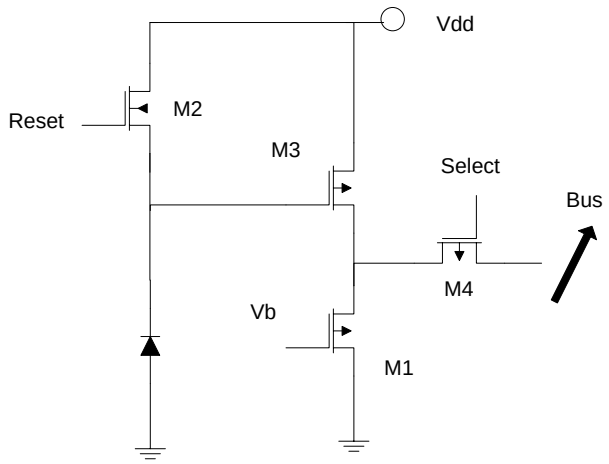

Figure 2.1 Source-follower per detector

The source-follower per detector (SFD) is a simple readout circuit. It consists of an NMOS source follower, a PMOS reset transistor, and a NMOS multiplexing transistor. The integration capacitance is the summation of the detector shunt capacitance and the input node capacitance of the SFD. The simple structure of the SFD makes it suitable for the applications of

high density, large format, and low power consumption. However, since the photon excited carrier charges are integrated on the input node capacitance of the detector directly, the detector bias voltage changes during integration. This causes variations in detector characteristics and nonlinearity of the readout circuit. Also, the SFD is susceptible to KTC noise induced by the integration-and-reset function and fixed pattern noise (FPN) caused by the process-dependent threshold voltage variations [19]. The circuit is shown in Figure 2.1.

The capacitor transimpedance amplifier (CTIA) circuit is shown in Figure 2.2. The integration capacitor is placed in the feedback loop of the amplifier with a reset device to discharge the integration capacitor and reset the amplifier output to the reference voltage. The detector bias is controlled by the virtual short feature of the amplifier. So, a good detector-bias control can be achieved with this circuit. Due to the Miller effect on the integration capacitor, its capacitance can be made extremely small to obtain low-noise and high-sensitivity. Unlike the direct injection and buffered direct injection, the input impedance of the CTIA is independent of the detector current. However, the feed-through effect of the reset clock can be coupled to the detector node and affect the stability of both the detector bias and amplifier operating point. Also, the circuit occupies more area and uses more power than the direct injection and buffered direct injection [21].

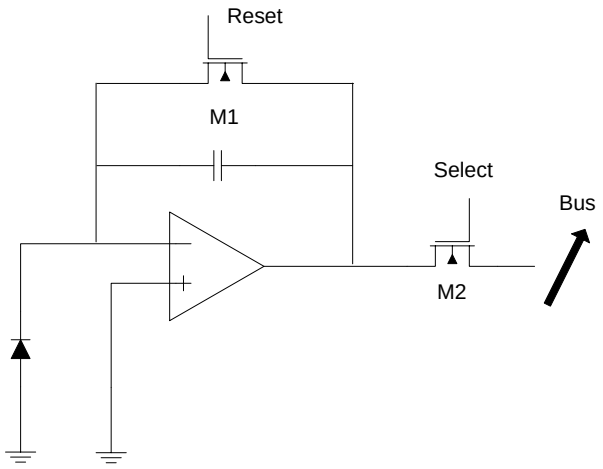

Figure 2.2 Capacitor transimpedance amplifier

The direct injection (DI) is another simple readout circuit. In the DI circuit, a common-gate PMOS device is used to bias and sense the current of the detector. The integrated voltage is readout through the PMOS source follower and the multiplexing device. In the DI circuit, the common gate device provides better bias control compared to the SFD. Like the SFD circuit, the DI circuit has a simple structure and low active power consumption. This makes it suitable for high-density applications. The injection efficiency of a readout circuit is defined as the ratio of the current flowing into the readout circuit to the detector photo current. The injection efficiency of the DI is determined by the ratio of the detector shunt resistance to the input resistance of the common-gate PMOS device. So, a lower input resistance means a higher injection efficiency and better detectivity since the input resistance of the PMOS device is proportional to its overall current including the background current level. So, the DI circuit is not suitable for applications involving low background flux levels. Both threshold voltage non-uniformity and KTC noise are problems of the DI circuit [23]. The circuit is shown in Figure 2.3.

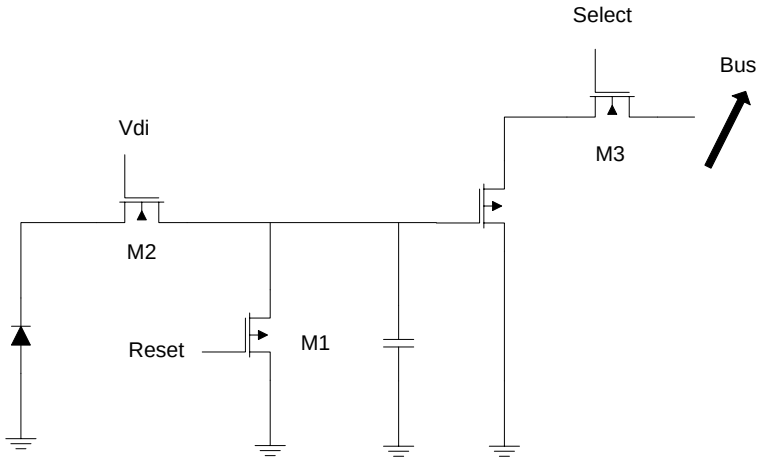

Figure 2.3 Direct injection

The buffered direct injection (BDI) circuit is shown in Figure 2.4. The structure of the circuit is similar to the DI, except that an additional inverted gain stage with the gain –A is connected between the gate node of the common-gate input device and the detector node. The input impedance can be decreased by a factor of A due to the negative feedback structure. So, the injection efficiency can be increased to near unity. The detector bias control of the BDI is

more stable than those of the SFD and DI due to the virtual-short property of the gain stage. Also, the equivalent input referred noise and operational bandwidth can be improved compared to the DI circuit. However, the additional gain stage consumes power during signal integration. Generally, the BDI is suitable for applications which require high readout performance and can afford additional circuit area and power consumption [25].

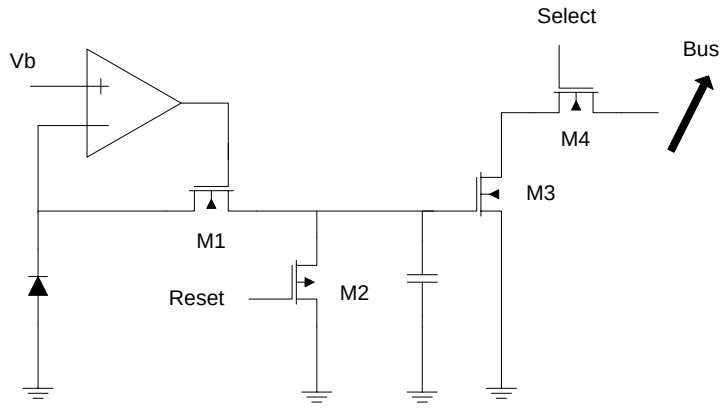

Figure 2.4 Buffered direct injection

In the shared-buffered direct injection (SBDI), the gain stage is implemented by the differential pair with the shared half circuit technique. The differential pair consists of the common left-half circuitry which is shared by all the unit cells in the same row. Under this arrangement, both chip area and power dissipation of the amplifier in the SBDI can be reduced to nearly 50% compared to those in the BDI or CTIA circuit. The SBDI also features high injection efficiency, good detector bias control, threshold voltage variation immunity, and low noise performance. A dynamic discharging output stage is also introduced to save the static power dissipation and improve readout speed by applying a dynamic discharging gate and clock. Generally, the SBDI can offer a better tradeoff between circuit area, power consumption, and circuit performance. This is makes it suitable for high density, large-array, and high performance applications [27]. The circuit is shown in Figure 2.5.

The current mirror readout circuit provides high performance without requiring an in-pixel op-amp or integration capacitor. In this circuit, the integration capacitor and source follower are place outside the pixel. Infrared radiation induces a current in the detector, and this current is

mirrored to circuitry which is located outside the pixel. The current mirror is designed so that the voltage on the detector is almost zero. The circuit features low input impedance, and most of the photo current is injected to the readout circuit even when the detector resistance is small [29]. The circuit is shown in Figure 2.6.

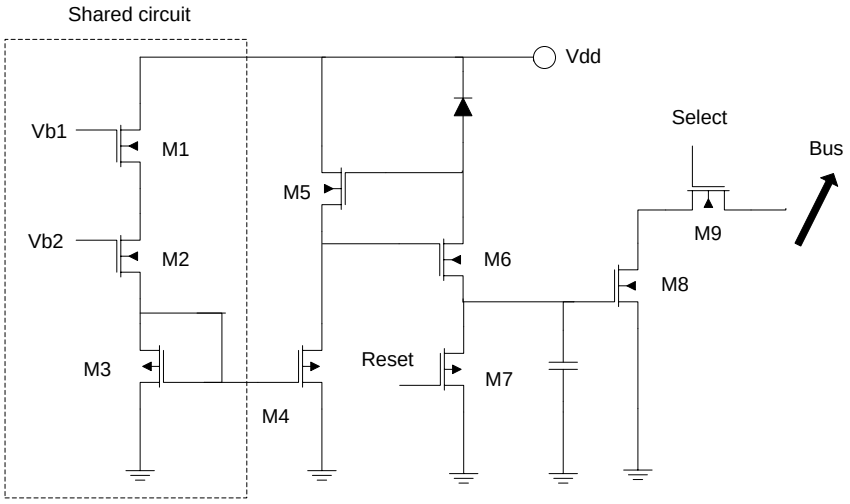

Figure 2.5 Shared buffered direct injection

The gate modulation input (GMI) circuit has a current-mirror configuration with the tunable source bias to control the current gain. The injection current flowing in the master device is mirrored and amplified by the slave device and integrated on the integration capacitor.

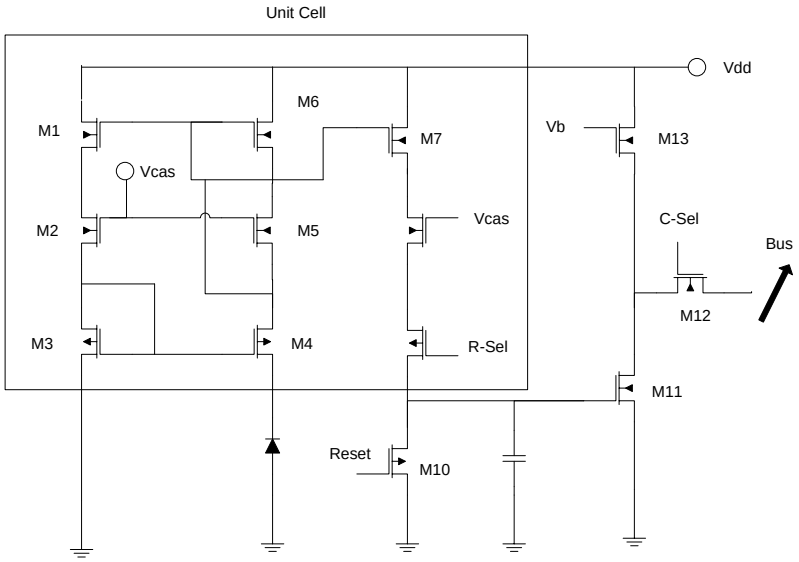

Figure 2.6 Current mirror

Similar to that in the DI circuit, the injection efficiency of the GMI circuit depends on the ratio of detector shunt resistance to the input resistance of the current mirror. However, the inherent current gain of the circuit leads to higher detection sensitivity and reduced input referred noise compared to the DI. To obtain a large total dynamic range, the current gain should be kept high and uniform [31]. The circuit is shown in Figure 2.7.

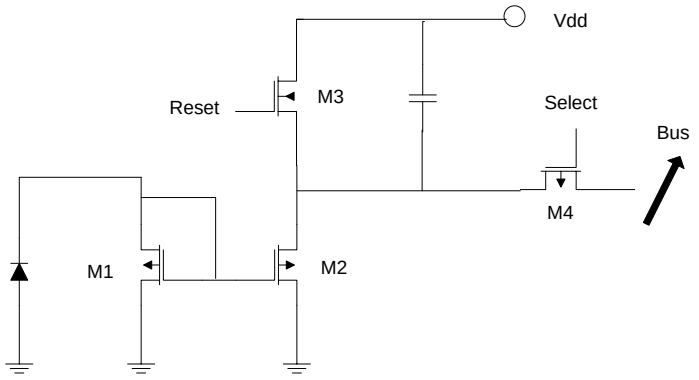

Figure 2.7 Gate modulation input

In the GMI, the amplified background current is integrated directly. So, a large integration capacitor is required to avoid saturation. However, it is challenging to increase the size of the integration capacitor without increasing the size of the pixel. To solve this problem, the buffered gate modulation input (BGMI) circuit uses current-mode background suppression to achieve higher dynamic range and better readout performance. The circuit consists of a shared buffer as the input stage, the unbalanced current mirror, and the row select switch. The shared-buffer technique provides a good bias control for the detector [33]. The circuit is shown in Figure 2.8.

When the resistance of the detector is small, the injection efficiency is low, and the bias across the detector can be non-uniform. The current mirroring direct injection (CMDI) circuit addresses these problems by using a current mirror to integrate the photo current. The current mirror can be designed so that the detector bias is almost zero, and the injection efficiency can be almost unity. The circuit occupies a small area and uses little power. The CMDI circuit has better injection efficiency detector bias uniformity compared to the DI and BDI. However, the CDMI uses more power than the DI and BDI [35]. The circuit is shown in Figure 2.9.

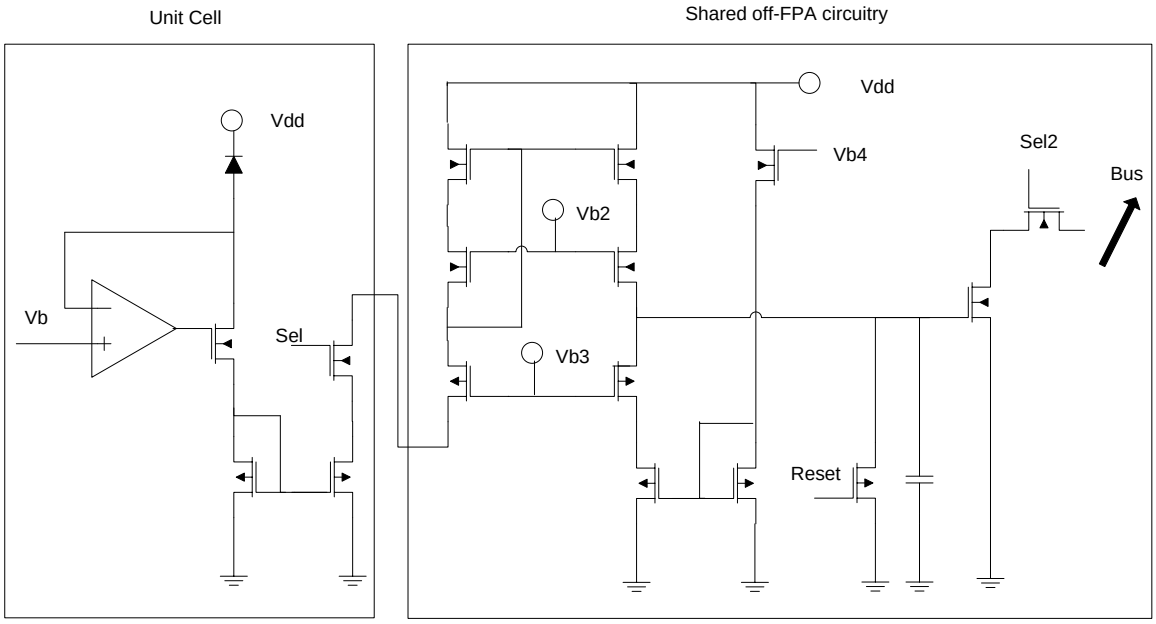

Figure 2.8 Buffered gate modulation input

The five most important criteria to compare the performance of the readout circuits are the noise electrons, location of the integration capacitor, power per unit cell, detector bias uniformity, and unit cell area. Table 2.1 compares the readout circuits.

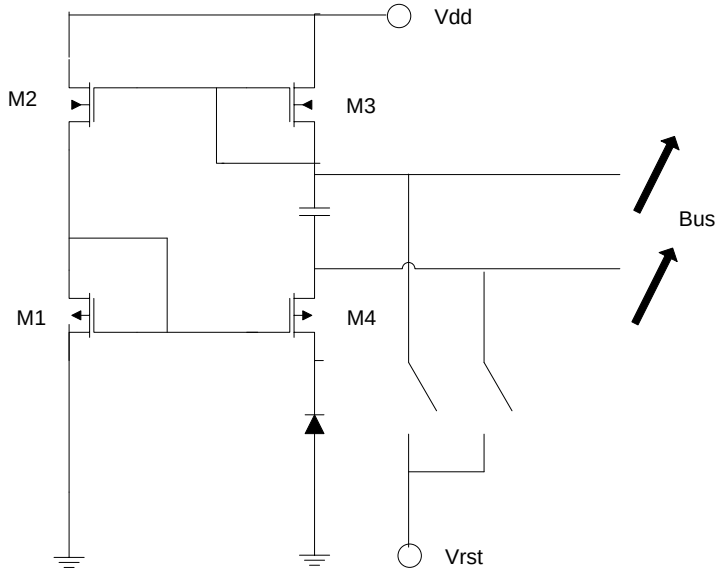

Figure 2.9 Current mirror direct injection

Table 2.1 Readout circuits and their performance criteria

Circuit	Typical noise electrons at frame rate	Location of integration capacitor	Power per UC (μW)	Detector bias uniformity	UC area (μm^2)	Ref.
Source Follower Per Detector	50-100 at 10Hz	Inside UC	0.5	1mV	20 x 20	[19], [20]
Capacitor TIA	40-150 at 10kHz	Inside UC	3-40	0.5-40mV	35 x 35	[21], [22]
Direct Injection	80 at 10kHz	Inside UC	0.5	10-40mV	20 x 20	[23], [24]
Buffered Direct Injection	80 at 10kHz	Inside UC	6-30	0.5-40mV	40 x 40	[25], [26]
Shared Buffered Direct Injection	80 at 10kHz	Inside UC	6-30	0.5-40mV	40 x 40	[27], [28]
Current Mirror	1k at 10kHz	Outside UC	0.5	10-40mV	30 x 30	[29], [30]
Gate Modulation Input	1k at 10kHz	Inside UC	0.5	10-40mV	30 x 30	[31], [32]
Buffered Gate Modulation Input	1k at 10kHz	Inside UC	0.5	10-40mV	30 x 30	[33], [34]
Current Mirroring Direct Injection	80 at 10kHz	Outside UC	6-30	0.5-40mV	40 x 40	[35], [36]

2.4 Dark Current in Focal Plane Arrays

Dark current is caused by thermal effects and intrinsic material properties. Dark current has a negative impact on the SNR and DR in an imaging system, and the magnitude of the dark current should be reduced in order to improve the performance of the system. Dark current has five primary sources: diffusion currents, thermal generation, surface generation, direct tunneling between the valence and conduction bands, and tunneling via band gap states [37].

Diffusion currents are affected primarily by generation-recombination kinetics through Shockley-Read centers. The electron and hole lifetimes also strongly affect the diffusion current. The number of Shockley-Read centers in the valence and conduction bands also affects the magnitude of the diffusion current. Short electron and hole lifetimes and large numbers of Shockley-Read centers cause large diffusion currents. The diffusion current is given by [37]:

$$J = qn_i^2 t \cdot [{}_{1/n\tau_n} + {}_{1/p\tau_p}] \cdot [exp(qV/kT) - 1] \tag{2.11}$$

Where n and p are the doping levels on either side of the junction, t is the thickness of the photodiode, and V is the bias across the diode. Equilibrium generation-recombination kinetics through a concentration of Shockley-Read centers N_r, located at an energy E_r above the valence band, give the following equations for the electron and hole life times [37]:

$$\tau_n = \frac{\tau_{p0}(n+n_1)+\tau_{n0}[p+p_1+N_r p_1/(p+p_1)]}{n+p+N_r p p_1/(p+p_1)^2} \tag{2.12}$$

$$\tau_p = \frac{\tau_{n0}(p+p_1)+\tau_{p0}[n+n_1+N_r p/(p+p_1)]}{n+p+N_r p p_1/(p+p_1)^2} \tag{2.13}$$

With

$$n_1 = N_c \cdot exp\left[-\left(E_g - E_r\right)q/kT\right] \tag{2.14}$$

$$p_1 = N_v \cdot exp(-E_r q/kT) \tag{2.15}$$

Where $\tau_{no} = 1/\gamma_n N_r$ and$\tau_{po} = 1/\gamma_p N_r$. γ_n and γ_p are the recombination coefficients for electrons and holes into the N_r centers, N_c and N_v are the densities of states in the conduction band and valence band respectively, and E_g is the band-gap voltage [37].

Thermal generation in the depletion region is caused primarily by Shockley-Read centers. The thermal generation current is given by [37]:

$$J = (qn_i^2 W)/(\tau_{no} p_r + \tau_{po} n_r) \quad (2.16)$$

Where $p_r = N_v \cdot exp\,[q(E_r - E_g)/kT], n_r = N_c \cdot exp\,(-qE_r/kT)$, $\tau_{no} = 1/\gamma_n N_r$, and $\tau_{po} = 1/\gamma_p N_r$. W is the width of the depletion region given by:

$$W \approx \sqrt{2\varepsilon\varepsilon_o(E_g - V)/qn} \quad (2.17)$$

ε is the dielectric coefficient. For the optimum levels at E_i, the intrinsic energy level, $n_r = p_r = n_i$, and $J = qn_i W/(\tau_{no} + \tau_{po})$ The bias dependence of the thermal generation current is contained in the depletion width, W, which varies as $\sim\sqrt{V}$ for an abrupt junction with an unlimited dimension to accommodate junction spread [37].

Surface generation currents are influenced by the intrinsic carrier concentration and the surface recombination velocity. The surface recombination velocity is a measure of the rate of recombination between electrons and holes at the surface of a semiconductor. The surface generation current is given by [37]:

$$J = qn_i s/2 \quad (2.18)$$

Where s is the recombination velocity. Surface generation currents have no explicit bias dependence [37].

Direct tunneling between the conduction and valence bands is influenced by the properties of the detector material and the detector bias. The current is given by [37]:

$$J = 4\varepsilon^{-\frac{3}{2}} V \left[\frac{m_e^*}{E_g m_o}\right] N_g \cdot exp\left[-\left(2 \cdot 10^{10} \cdot \sqrt{\varepsilon \cdot m_e^*} \cdot E_g^{\frac{3}{2}}\right)/N_g\right] \quad (2.19)$$

with:

$$N_g = \sqrt{n(E_g + V)} \quad (2.20)$$

Where n is the doping concentration.

The last source is tunneling via band-gap states. The current is given by:

$$J = \left[2 \cdot 10^{-12} \cdot N_t \cdot \frac{V}{\varepsilon \cdot E_g}\right] \cdot exp\left[-\left(3.35 \cdot 10^9 \cdot \pi\sqrt{\varepsilon \cdot m_e^*} \cdot E_g^{\frac{3}{2}}\right)/N_g\right] \quad (2.21)$$

2.5 Dark current suppression circuits

Several readout schemes have been developed to suppress dark current. Suppressing the dark current using memory was achieved in [6-8]. In [6], a PMOS transistor was added to the unit cell in order to suppress the dark current. A global voltage was routed to all of the unit cells in the array. The Vgs of the transistor was adjusted so that the current through the transistor was nearly identical to the dark current through the active photo diode. The unit cell is shown in Figure 2.10.

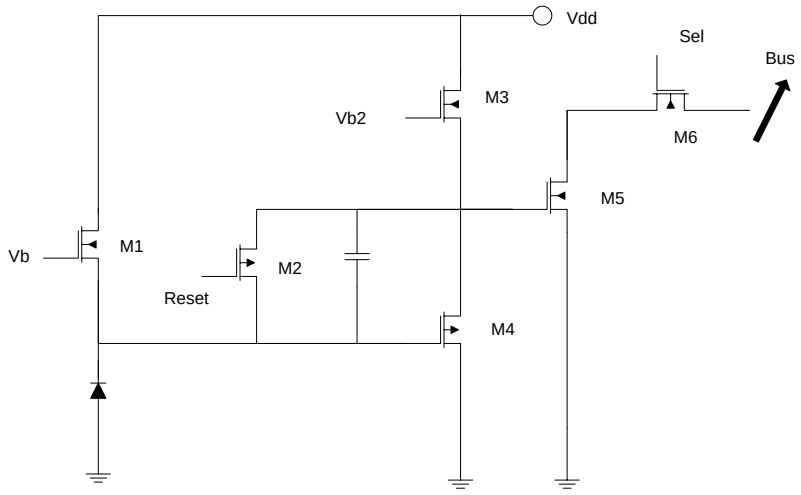

Figure 2.10 Unit cell from [6]

Transistor M0 is used to provide a suppression current, and the integration capacitor integrates the differential current between M0 and the infrared detector. This unit cell is 50 x 50 μm^2.

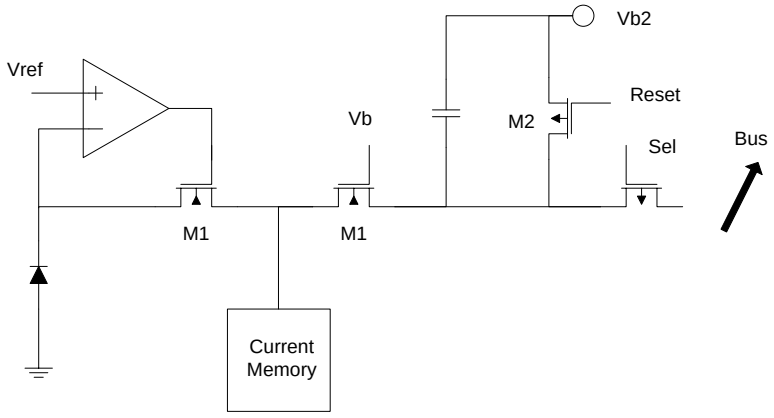

Figure 2.11 Unit cell from [7]

The unit cell in [7] used a current memorization circuit inside the unit cell. The schematic of the unit cell is shown in the figure below. This unit cell size is 50 x 400 μm^2. The unit cell is shown in Figure 2.11.

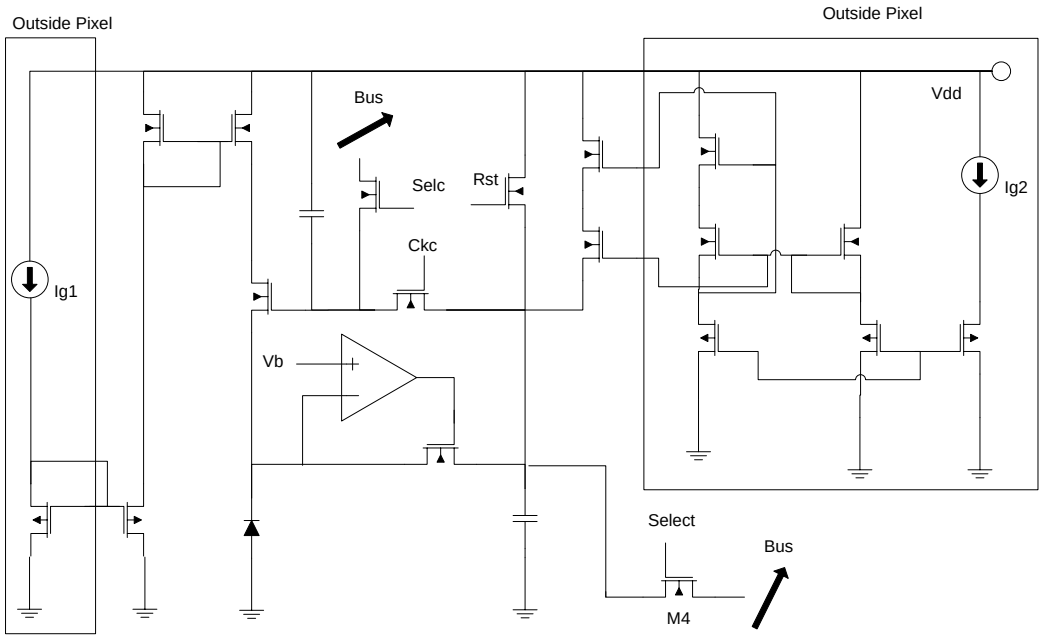

Figure 2.12 Unit cell from [8]

In [8], memory was used inside the unit cell. The size of this unit cell was increased because of the additional transistors and capacitors that had to be added. The unit cell size was 50 x 50 μm^2. The unit cell is shown in Figure 2.12.

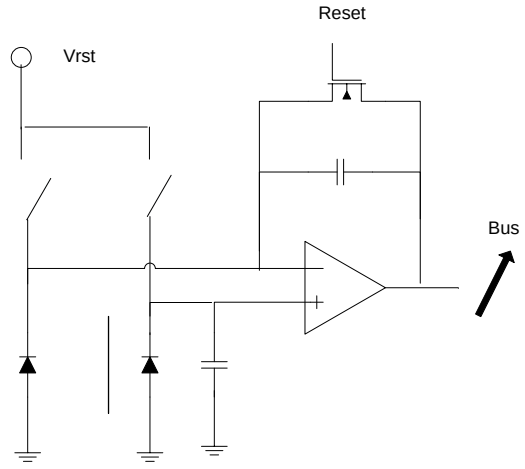

Figure 2.13 Unit cell from [9]

In [9], a blind photo diode was used in each unit cell in order to suppress the dark current. This increased the size of the unit cell to 150 x 150 μm^2. The schematic is shown in Figure 2.13.

2.6 High SNR Architectures

There are eight primary methods to improve the SNR in a readout circuit. The logarithmic photo detector has the advantage of providing a good dynamic range, about 120dB. This is a significant improvement compared to standard integration CMOS sensors and CCD sensors which have dynamic ranges of 70dB and 80dB, respectively. Continuous operating pixels transform the photocurrent into a corresponding voltage without using any integration process. A diode-connected MOS transistor operating in the sub-threshold region is used to create an output voltage that is a logarithmic function of the photo current. For imaging fast moving objects, a global shutter must be used. This method allows the simultaneous exposure of all the pixels [39]. The circuit is shown in Figure 2.14.

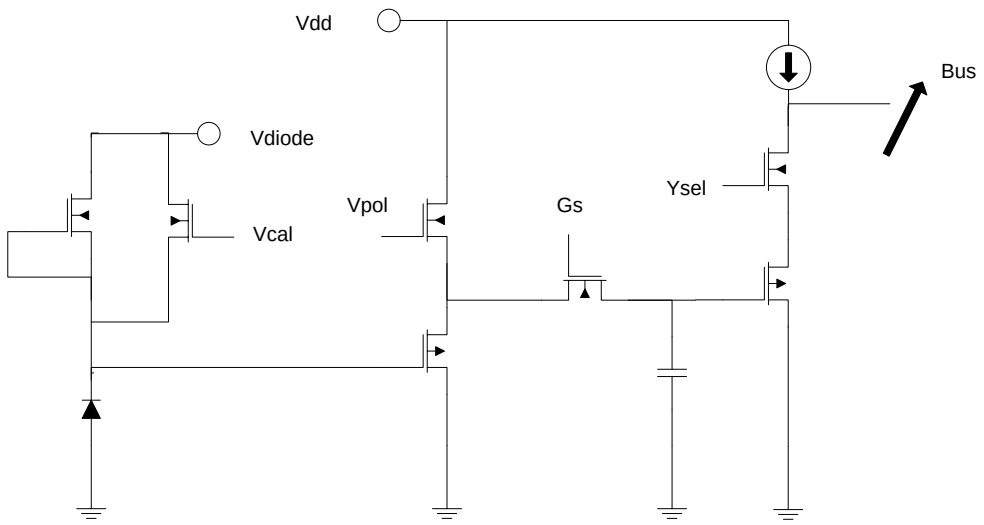

Figure 2.14 Companding sensor

Multimode sensors combine the features of several architectures. For example, in [42], a hybrid sensor uses a voltage-readout operation based on the lateral overflow integration capacitor in the pixel and a current-readout operation based on current amplification and logarithmic compression. The voltage readout extends the DR and SNR without losing the overflow charge from the photo diode. The current readout circuit achieves further extension of

the DR on the bright end of the range by reading out the logarithmic compression voltage of the photo current amplified in each pixel. The circuit is shown in Figure 2.15.

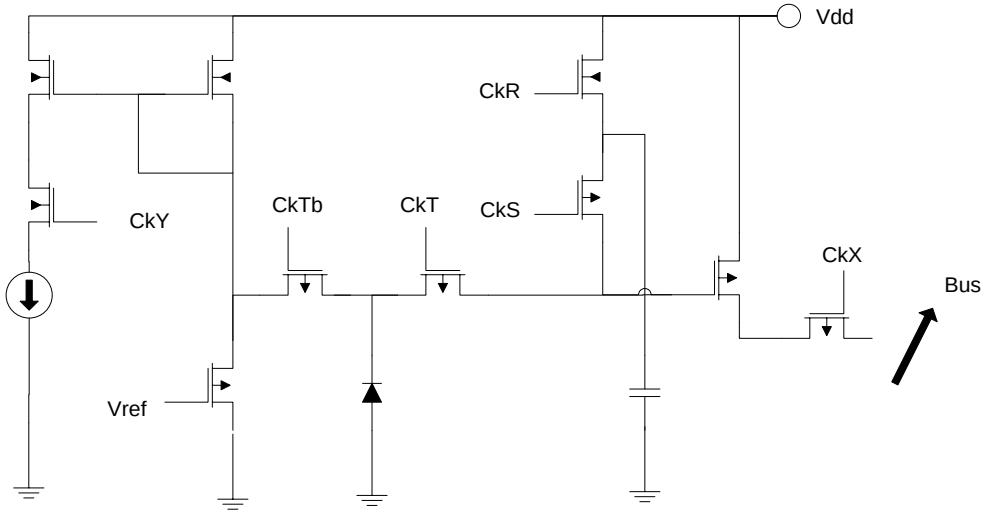

Figure 2.15 Multimode sensor

For clipping sensors, the signal is integrated until the photo diode saturates. Then, the overflow charges are integrated on the integration capacitors. This operation enables the overflow charges to be utilized for signal charges and achieves a high sensitivity and a high well capacity. Readout gains and input-referred noises of the image sensor are improved by actively using a pixel source follower feedback operation [45]. The circuit is shown in Figure 2.16.

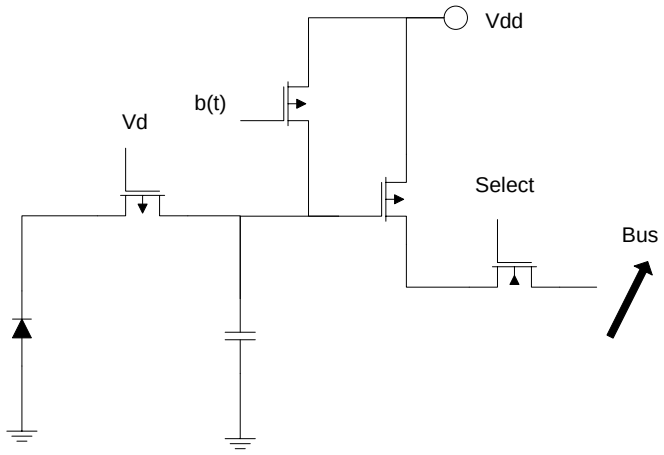

Figure 2.16 Clipping sensor

One solution to achieve high dynamic range is to use pulse-frequency modulation in digital-pixel sensors. The voltage at the photo detector nose is directly converted into a digital-

pulse signal through multiple-reset light-controlled oscillation. Photo current causes the voltage across the photo diode to drop at a slope that is proportional to the illumination level. When the voltage reaches the threshold of the oscillator, the oscillator's output flips and the photo diode is reset. Light to frequency encoding results because the frequency of the output pulse is linearly proportional to the light intensity [49].

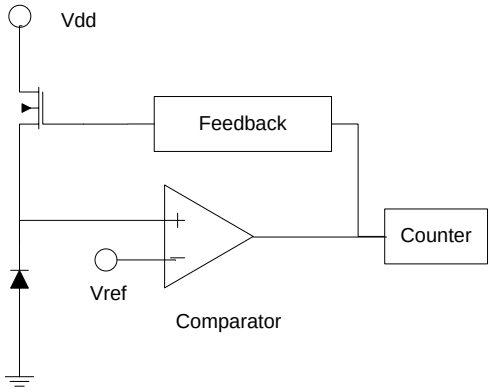

Figure 2.17 Frequency based sensor

The time to saturation architecture extends the dynamic range by allowing the integration time for each pixel to be adjusted based on the photon flux that each pixel receives. Pixels incorporate an on-pixel memory which allows the captured data to be randomly, and repeatedly, accessed. Also, a programmable dynamic range is obtained through simple modulation of the digital clock signal of the timing circuit. The pulse obtained from the start of integration corresponds to the discharge time of the photodiode and can be described as pulse width modulated signal [53]. The circuit is shown in Figure 2.18.

In the global control over integration time method, different exposure-time signals are used to increase the DR. The read image signals are synthesized in the external system. This approach provides many advantages for wide dynamic range imaging at the expense of system complexity and frame memory. First, the image capturing conditions such as the number of different exposure times and the length of each exposure time can be adjusted. Second, the different exposure times are sufficient for expanding the dynamic range to 120dB while maintaining a sufficient image quality. This method is compatible with many types of pixels [54].

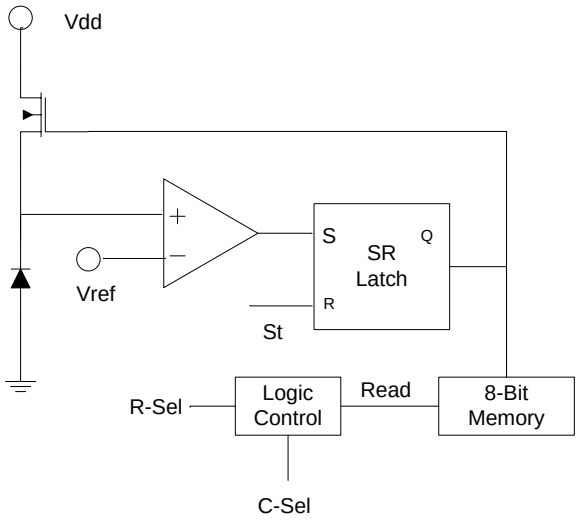

Figure 2.18 Time to saturation

For conventional CCD sensors with an electronic shutter, the integration time is the same for all pixels. The sensor does not take into account local changes of the image and cannot enhance dynamic range. With the autonomous control over integration time method, the pixel adapts to the intensity of the incident light and also the temporal changes of the pixel intensity. This reduces blur caused by moving objects in a scene and it improves the dynamic range. The sensor has circuitry for saturation detection and motion detection on the focal plane. Because of the variable integration time, the pixel intensity needs to be normalized afterwards [58]. The circuit is shown in Figure 2.19.

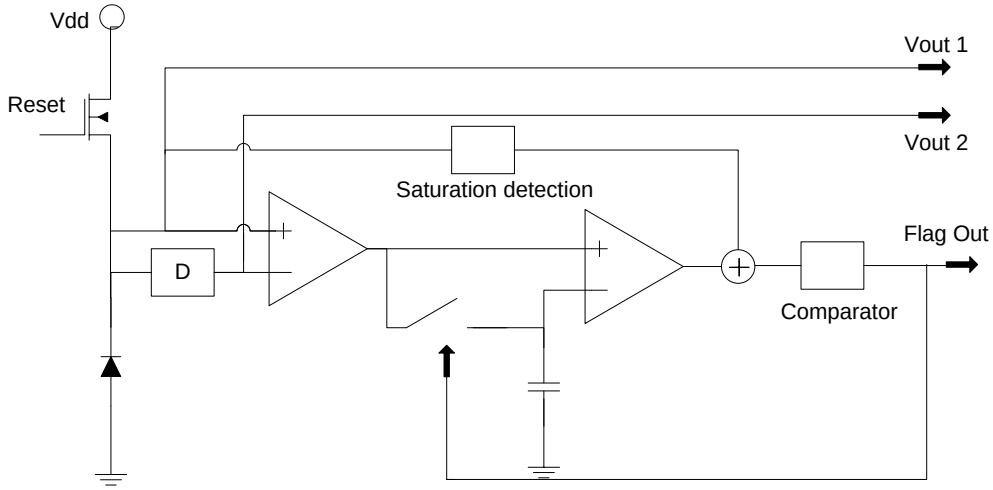

Figure 2.19 Autonomous control over integration time

CHAPTER 3

PROPOSED METHOD

Previous work in dark current subtraction has produced unit cells which are relatively large [6-9]. The purpose of the proposed readout circuit is to suppress the dark current without increasing the pixel size. However, the performance of the readout circuit should be comparable to the readout circuits in [6-9] in all performance criteria such as power dissipation, linearity, etc. The target specifications of the readout circuit are shown in Table 3.1.

Table 3.1 Target specifications

Criterion	Target
Pixel size (μm^2)	< 35 x 35
Fill factor	> 10%
Max. power per pixel	< 3µW
Pixel gain	> 40dB
Fixed pattern Noise	< 3mVrms
Random Noise	< 4mVrms
Linearity	> 90%
Background handling capacity	> 1 pA-300nA
Photo current range	> 1 pA-300nA
Current memory error	< 1%
Minimum detectable contrast	< -90 dB
Differential signal dynamic range	> 90 dB
Average SNR	> 80dB

The proposed ROIC was designed using the TSMC 0.18µm RF process. This process was chosen because it supports a deep N-well. The deep N-well structure is very useful because the deep N-well can be used to make a P-I-N photo diode. P-I-N photo diodes have a higher collection efficiency of incident photons because the intrinsic region between the p-type and n-type regions causes the depletion region to be larger than the depletion region in an ordinary P-N

photo diode. Because the depletion region is larger, more electron-hole pairs are generated [72].

The proposed P-I-N photo diode is shown in Figure 3.1.

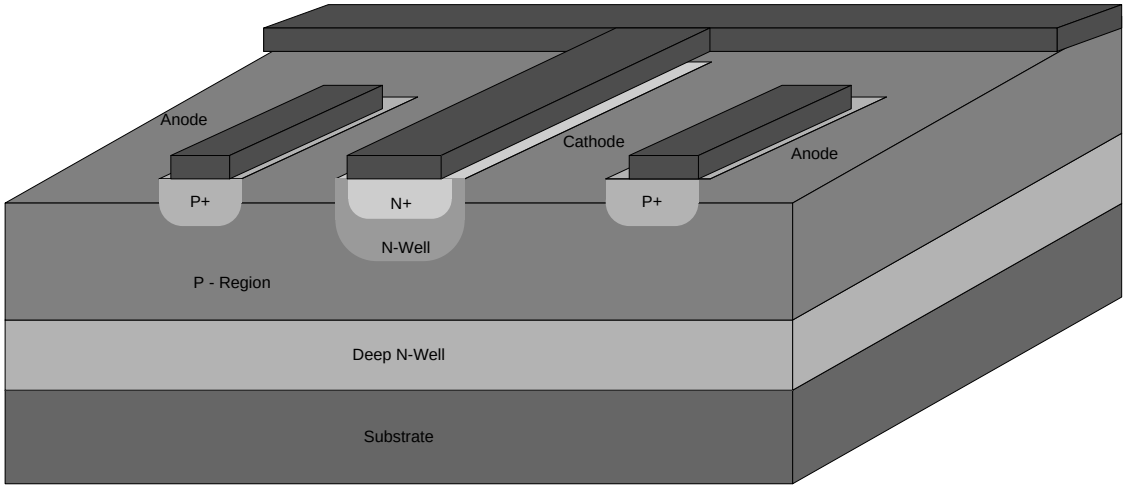

Figure 3.1 Proposed photo diode

The main components of the proposed ROIC are the horizontal column shift register, the vertical row shift register, the 1x768 array of shared ADCs, the 1024x1 array of blind photo diodes and current mirrors, and the 1024x768 unit cell array. A block diagram of the proposed ROIC is shown in Figure 3.2.

The operation of the ROIC is explained as follows. Each column of pixels contains a blind photo diode and a current mirror. The blind photo diodes are identical to photo diodes in the unit cells. The only difference is that several layers of metal are above the blind photo diodes so that photons cannot reach the junction of the photo diodes and create electron-hole pairs. Because the photo diodes are blind, the only current that flows across the P-N junction is the dark current. The current mirrors are used to route the dark current to each unit cell in the column.

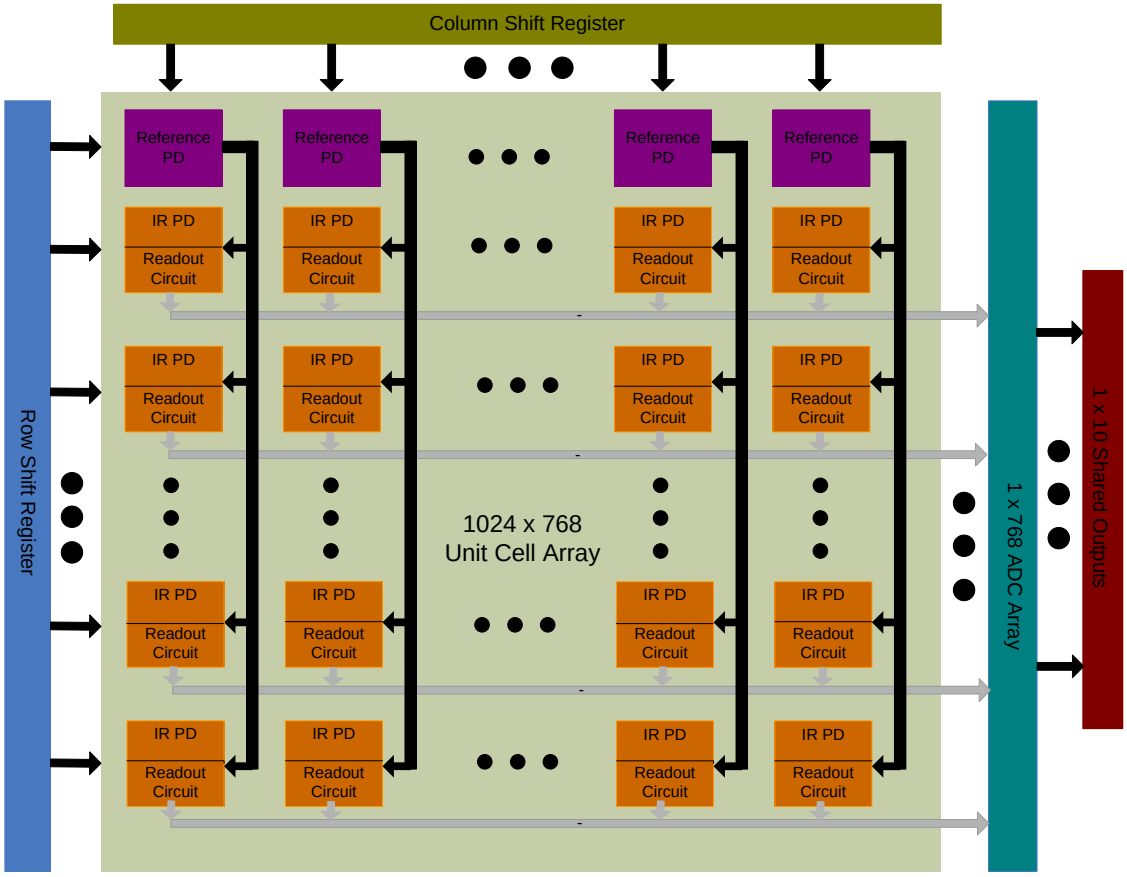

Figure 3.2 Proposed ROIC

At the beginning of each picture, the integration capacitors in all of the unit cells are reset to 0V. Then, photon-generated current in the photo diodes produces a voltage on the negative input of the amplifier in the unit cell. The dark current produces a voltage on the positive input of the amplifier. The output current of this amplifier is proportional to the difference between the dark current and the photo current. Using an integration capacitor, the output current is integrated.

After signal integration, the voltages on the integration capacitors are sampled, one column after the other by the horizontal shift register to the A/D converters. The A/D converters digitize the sampled voltages. After the voltages have been digitized, the row register samples the digital output voltages from each of the 768 ADCs and multiplexes the digital voltages off-chip.

After all of the bits from all of the rows in the column have been multiplexed off-chip, the horizontal shift register samples the next column of unit cells. This process continues until the all of the columns have been sampled.

3.1 Unit cell

The unit cell for the proposed circuit is in Figure 3.3. Transistors M13 and M14 form a current mirror which is used to bias the photo diode. Transistors M15 and M16 form a current mirror which is used to create voltage Vp. The current that is routed to transistor M13 is a bias current, and the current that is routed to M15 is a bias current and the dark current. The Operational Transconductance Amplifier (OTA) is used to compare voltages Vp and Vm and produce an output voltage.

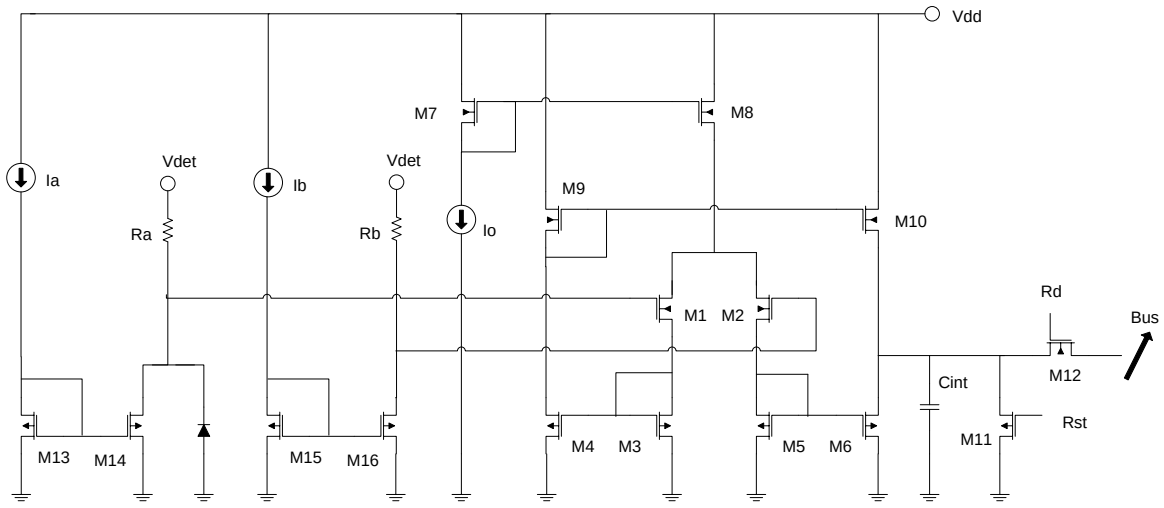

Figure 3.3 Proposed unit cell

Assuming transistors M13 and M14 operate in the saturation region, the voltage Vm is given by:

$$V_m = V_{det} - R_a \cdot \left(I_{ph} + I_{dk} + I_b\right) \tag{3.1}$$

Assuming transistors M15 and M16 operate in the saturation region, the voltage Vp is given by:

$$V_p = V_{det} - R_b \cdot (I_{dk} + I_c) \tag{3.2}$$

The output voltage of the OTA is given by:

$$V_{ota} = \left(V_p - V_m\right) \cdot g_m \cdot (R_{O10} || R_{O6}) + V_{DSAT,M6} \tag{3.3}$$

The integration capacitor integrates the differential current, which is given by:

$$I_{ota} = \left(V_p - V_m\right) \cdot g_m \tag{3.4}$$

To integrate the differential current, RST will go to logical '1', which turns on transistor M11, and the voltage on the integration capacitor resets to 0V. After the integration capacitor has reset to 0V, RST goes to logical '0', which turns off transistor M11, and the voltage on the integration capacitor integrates to V_{ota}.

The procedure for finding the device values in the circuit was obtained from [69]. For the OTA, the bias current is obtained from the slew rate:

$$I_O = C_{int} \cdot SR \tag{3.5}$$

Transistors M1 and M2 are sized to satisfy the gain-bandwidth:

$$g_{m1,2} = GB \cdot C_{int} \tag{3.6}$$

Transistors M3, M4, M5, and M6 are sized to satisfy the voltage drop across them:

$$\left(\frac{W}{L}\right)_{3,4,5,6} = \frac{I_o}{\mu_n C_{ox} V_{DSAT}^2} \tag{3.7}$$

Vdsat is usually set between 100mV to 200mV.

Transistors M7, M8, M9, and M10 are sized to satisfy the voltage drop across them:

$$\left(\frac{W}{L}\right)_{7,8,9,10} = \frac{I_o}{\mu_p C_{ox} V_{DSAT}^2} \tag{3.8}$$

Transistors M11 and M12 are sized to satisfy the rise and fall times. For M11:

$$T_r = \frac{C_{int} + W \cdot L \cdot C_{ox}}{\mu_n \cdot C_{ox} \cdot \left(\frac{W}{L}\right)_N \cdot (V_{gs} - V_{tn})} \tag{3.9}$$

For M12:

$$T_f = \frac{C_{int} + W \cdot L \cdot C_{ox}}{\mu_p \cdot C_{ox} \cdot \left(\frac{W}{L}\right)_P \cdot (V_{gs} - V_{tp})} \tag{3.10}$$

Transistors M13, M14, M15, and M16 are sized to satisfy the voltage drop across them:

$$\left(\frac{W}{L}\right)_{13,14,15,16} = \frac{I_o}{\mu_n C_{ox} V_{DSAT}^2} \tag{3.11}$$

The size of the integration capacitor is chosen to satisfy the electron well capacity:

$$WC = \frac{C_{int} \cdot V_{swing}}{q} \tag{3.12}$$

Vswing is the voltage swing on the integration capacitor, and q is the electron charge.

To test the unit cell, photo current and dark current were modeled as ideal DC current sources. The magnitudes of the DC currents were adjusted to simulate different magnitudes of

photo currents and dark currents. The magnitude of the DC current was 1pA to 1µA, and the magnitude of the dark current was 500pA to 1µA.

The active photo diode was replaced with a capacitor, a DC current source for the photo current, and a DC current source for the dark current in parallel. The blind photo diode was replaced with a capacitor and a DC current source for the dark current in parallel. The value of the capacitance of the blind and active photo diodes was calculated using the following expression from [71]:

$$C = \sqrt{q\varepsilon_S\varepsilon_0 N_a A^2/2(V_{bi} + V_{det})} \tag{3.13}$$

The calculated value was 1pF.

Figure 3.4 below shows a simulation of the unit cell. The reset time is 10µs. The photo current is 1pA, and the dark current is 500pA. The voltage on the integration capacitor is shown during reset and integration.

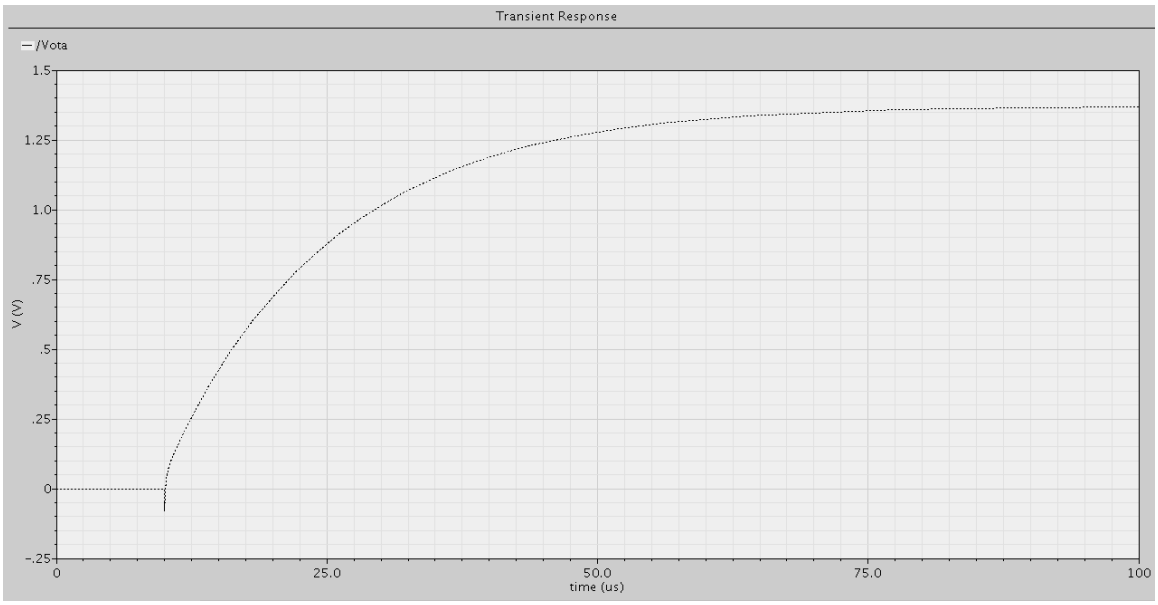

Figure 3.4 Output voltage with the DC current at 1pA

In Figure 3.5, the DC current is set to 1nA, and the output voltage integrates. The dark current is 500pA.

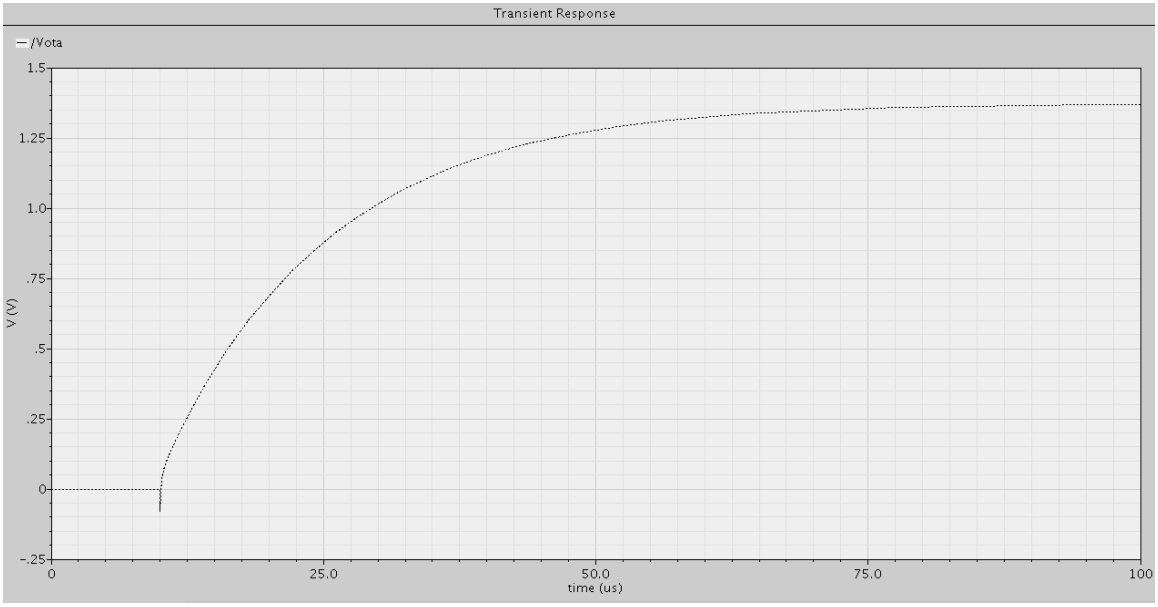

Figure 3.5 Output voltage with the DC current at 1nA

In Figure 3.6, the DC current is set to 1µA, and the output voltage integrates. The dark current is 500pA.

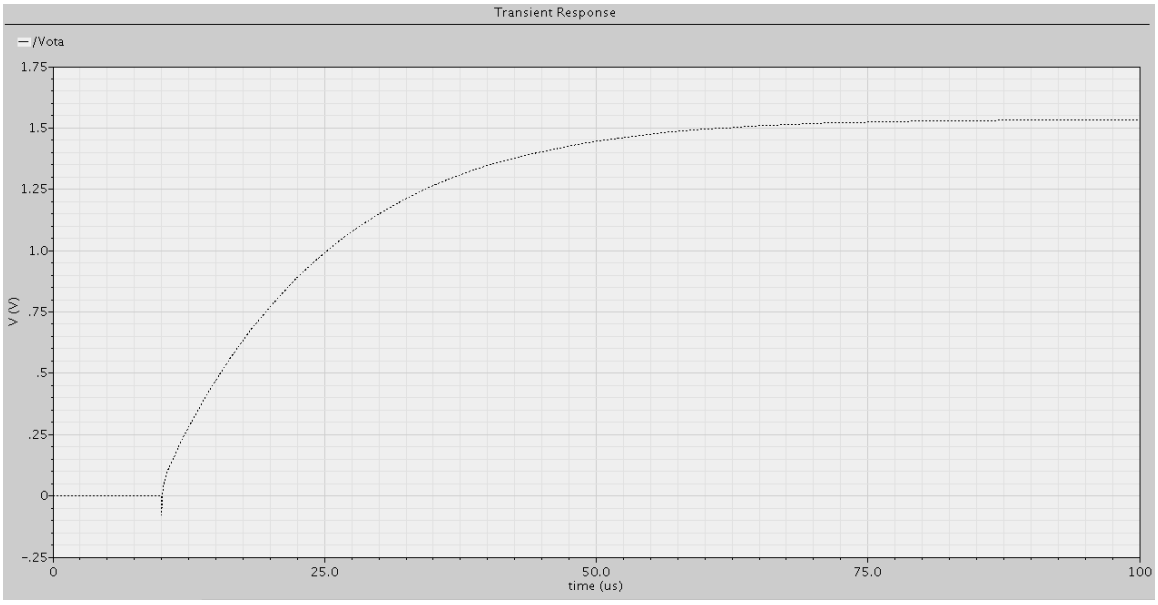

Figure 3.6 Output voltage with the DC current at 1µA.

Figure 3.7 shows the linearity of the OTA. To test the linearity, the Rst signal is held at logical ‘0,’ and the DC current sweeps from 1pA to 1µA over 500µs.

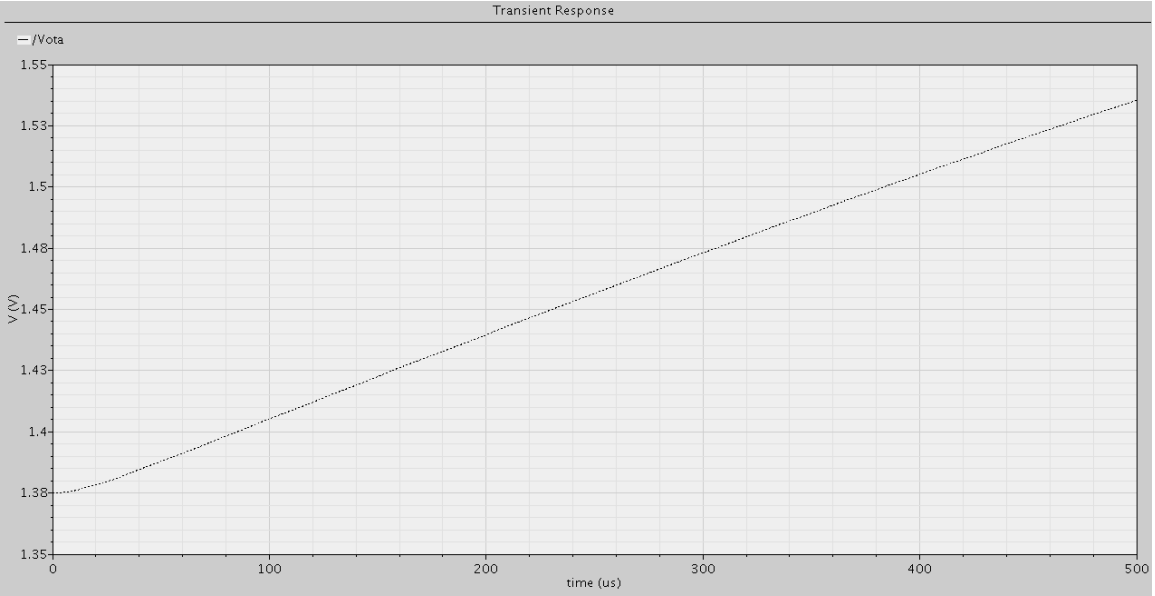

Figure 3.7 OTA linearity

The SNR for circuits that perform dark current suppression is given by:

$$SNR = 20 \cdot \log\left(\frac{I_{ph} \cdot V_{swing}}{(I_{ph} + I_{dk} \cdot E) \cdot N}\right) \tag{3.14}$$

where I_{ph} is the photo current, V_{swing} is the voltage swing on the integration capacitor, I_{dk} is the dark current, E is the current memory error, and *N* is the total noise. Research on dark current variability in silicon camera chips has shown deviations of 0.5% to 1% [70]. So, 1% was used in the calculations. The noise on the integration capacitor is approximately 1μV. In Figure 3.8, the photo current is 1pA, and the dark current ramps from 1pA to 1μA. The SNR is shown. In Figure 3.9, the photo current and dark current range from 1pA to 1μA. The x-axis, y-axis, and z-axis are the photo current, dark current, and SNR, respectively.

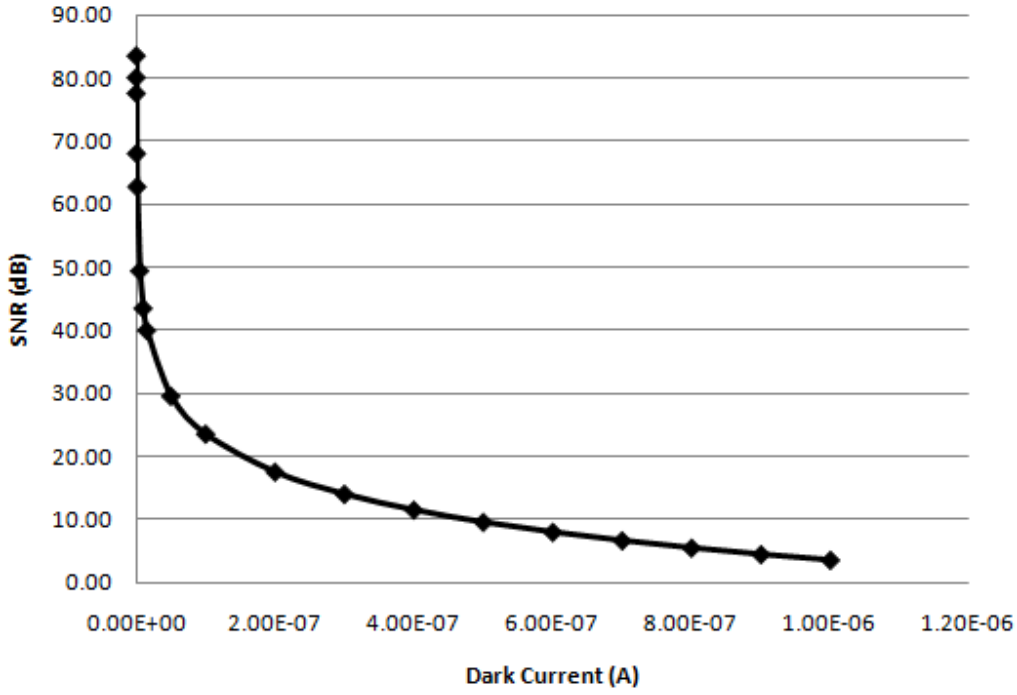

Figure 3.8 SNR versus dark current

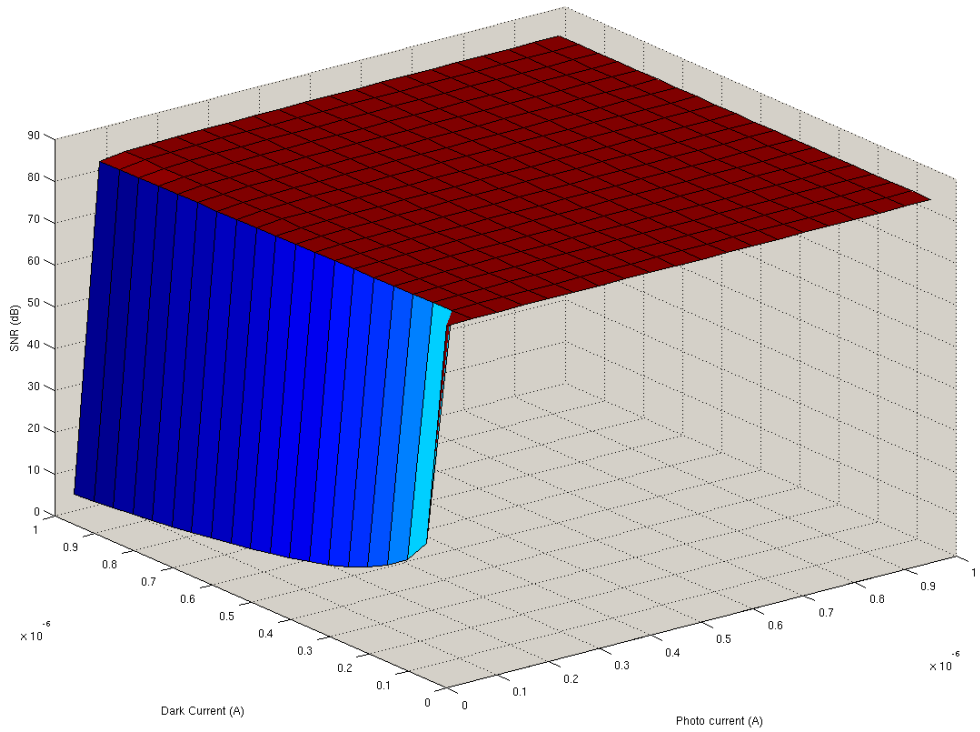

Figure 3.9 SNR versus dark current and photo current

The dynamic range is given by:

$$DR = 20 \cdot \log\left(\frac{V_{swing}}{N}\right) \tag{3.15}$$

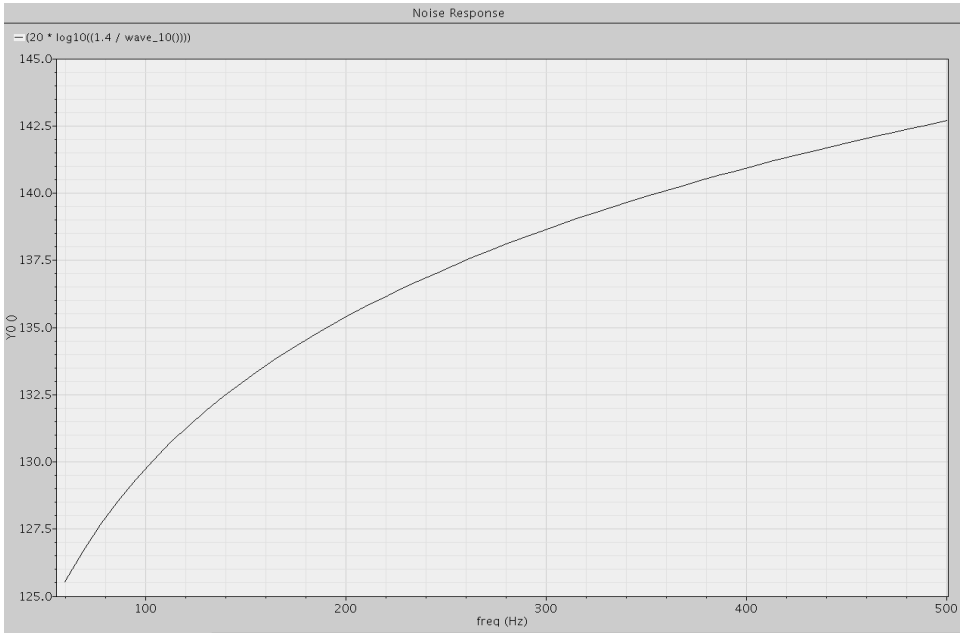

Figure 3.10 Dynamic Range

The dynamic range is shown in Figure 3.10. The frequency range is 60Hz to 500Hz.

3.2 Current Mirrors

The reference currents are generated outside the unit cell and routed to the unit cell using current mirrors. The routing circuit is shown in Figure 3.11.

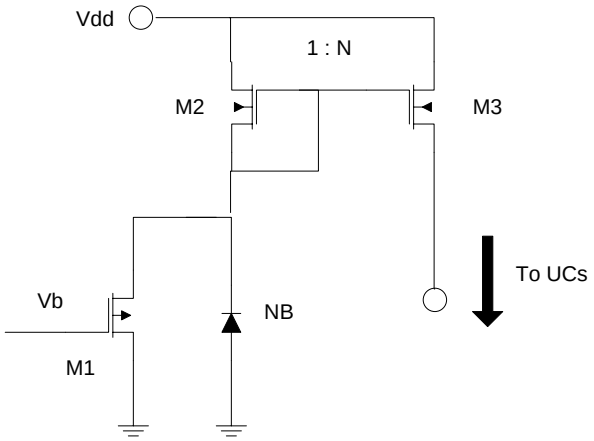

Figure 3.11 Routing circuit for the current from the blind photo diode

Transistors M1 and M2 are used to bias the blind photo diode. Transistors M2 and M3 form a current mirror which routes the current to each unit cell. The ratio of the transistor sizes between M2 and M3 is 1:N, where N is the number of unit cells in each column of the focal plane array.

3.3 Analog to Digital Converter

The most commonly used Analog to Digital Converters (ADC) are flash, pipeline, successive approximation, oversampling, and integrating. Each type has benefits that are unique to its architecture and span the spectrum of high speed and resolution.

Flash converters have the highest speed of any type of ADC. They use one comparator per quantization level (2^N-1) and 2^N resistors. The reference voltage is divided into 2^N values, and each value is fed into a comparator. The input voltage is compared with each reference value, and the result is a thermometer code at the output of the comparators. A thermometer code exhibits all zeros for each resistor level if the value of v_{IN} is less than the value on the resistor string, and ones if v_{IN} is greater than or equal to the voltage on the resistor string. The advantage of this converter is the speed because each clock pulse generates an output digital word. However, the disadvantages are the area and power requirements [60].

The pipeline converter is an N-step converter, with 1 bit being converted per stage. This type of converter is able to achieve a resolution of 10-13 bits at high speeds. Each stage of the converter performs three steps. After the input voltage has been sampled, it is compared to $V_{ref}/2$. The output of each comparator is the bit conversion for that stage. If $v_{IN} > V_{ref}/2, V_{ref}/2$ is subtracted from the held signal, and the result is passed to the amplifier. If $v_{IN} < V_{ref}/2$, then the original input signal is passed to the amplifier. Finally, the result of the summation is multiplied by 2 and the result is passed to the next sample-and-hold stage. The main advantage of this converter is its high throughput because one conversion is completed per clock cycle. The disadvantage with this converter is that the amplifiers have to be very precise because a slight error in the first stage propagates through the converter and results in a much larger error at the end of the conversion [61].

The successive approximation converter performs a binary search through all possible quantization levels before converging on the final digital value. An N-bit register controls the timing of the conversion, and N is the resolution of the converter. The input voltage is sampled and compared to the output of the DAC. The output of the comparator controls the direction of the binary search, and the output of the successive approximation register (SAR) is the actual digital conversion. The limit to the converter's accuracy depends on the accuracy of the DAC. If the DAC does not produce the correct analog voltage with which to compare to the input voltage, the entire converter output will contain an error. If a wrong decision is made early, a large error will result [62].

ADCs can be separated into two categories depending on the rate of sampling. The first category samples the output at the Nyquist rate. The second type samples the signal at a much higher rate. This type of converter is an oversampling converter. The oversampling ADC is able to achieve much higher resolution than Nyquist rate converters because digital signal processing techniques are used in place of complex and precise analog components. The accuracy of the converter does not depend on the component matching, precise sample-and-hold circuitry, or timing, and only a small amount of analog circuitry is required. However, because of the amount of time required to sample the input signal, the throughput is considerably less than the Nyquist rate ADCs [63].

The integrating ADC performs the conversion by integrating the input signal and correlating the integration time with a digital counter. These converters have high-resolution but slow conversions. A counter determines the number of clock pulses that are required before the integrated value of the reference voltage is equal to the sampled input signal. The number of clock pulses is proportional to the actual value of the input voltage, and the output of the counter is the actual digital representation of the input voltage. The time to increment the counter is 2^N clock cycles, and N is the number of bits [64].

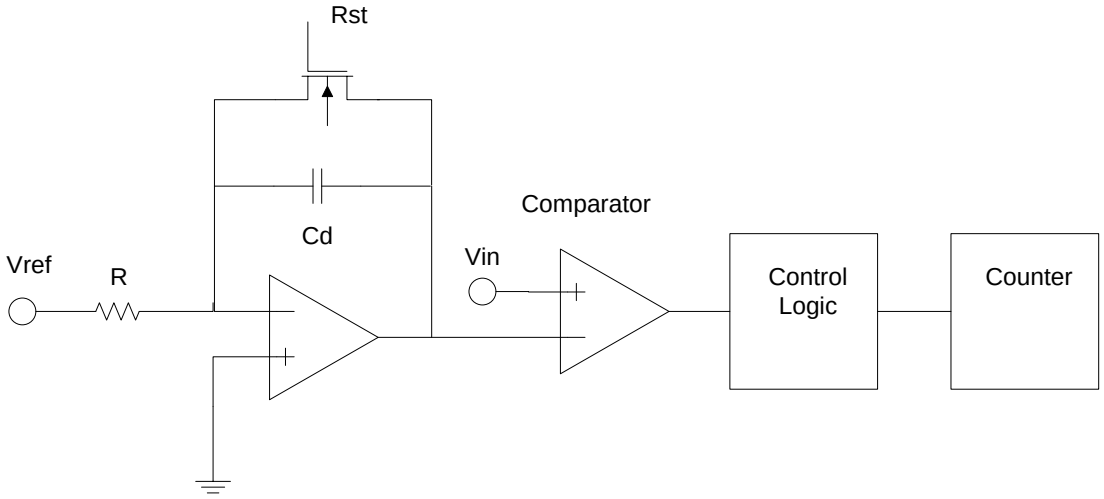

Figure 3.12 ADC schematic

The integrating ADC was selected for the proposed circuit because of its high accuracy. To improve the frame rate, one integrating ADC is used for each row of pixels. So, there are 768 integrating ADCs on the chip. The ADC is shown in Figure 3.12.

The op-amp consists of a differential amplifier with a source follower. The differential amplifier provides high gain, and the source follower provides high swing. The schematic of the op-amp is shown in Figure 3.13.

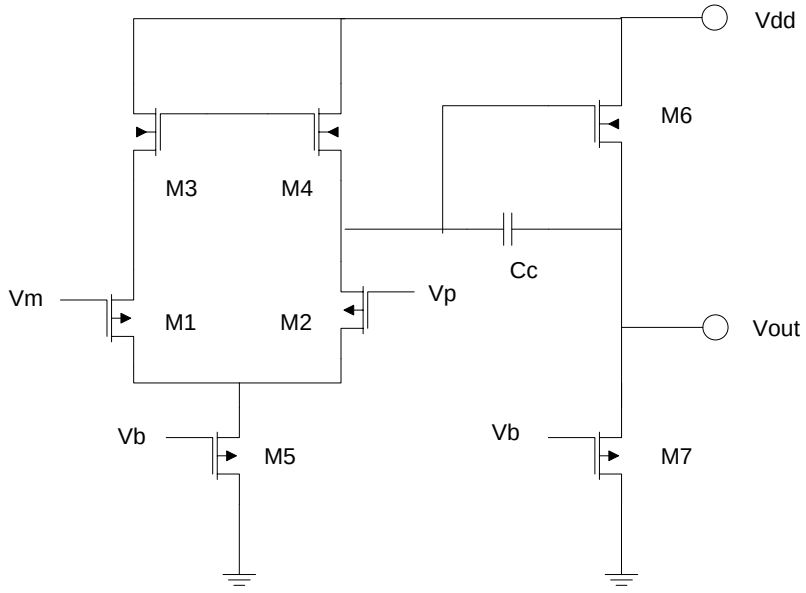

Figure 3.13 Op-amp

The bias current is calculated from (3.5). Transistors M1 and M2 are sized to satisfy the gain-bandwidth using equation (3.6). Transistors M3 and M4 are sized to satisfy the voltage drop across them using equation (3.8). Transistors M5, M6, and M7 are sized according to the following relationship:

$$\frac{(W/L)_3}{(W/L)_6} = \frac{(W/L)_4}{(W/L)_6} = \frac{(W/L)_5}{2(W/L)_7} \tag{3.16}$$

The feedback capacitor is given by:

$$C_c = \frac{C_d}{2} \tag{3.17}$$

The comparator must output a logical '1' when the voltages Vin and Vc are equal. The comparator consists of a preamplifier, decision circuit, and output buffer. The schematic is shown in Figure 3.14.

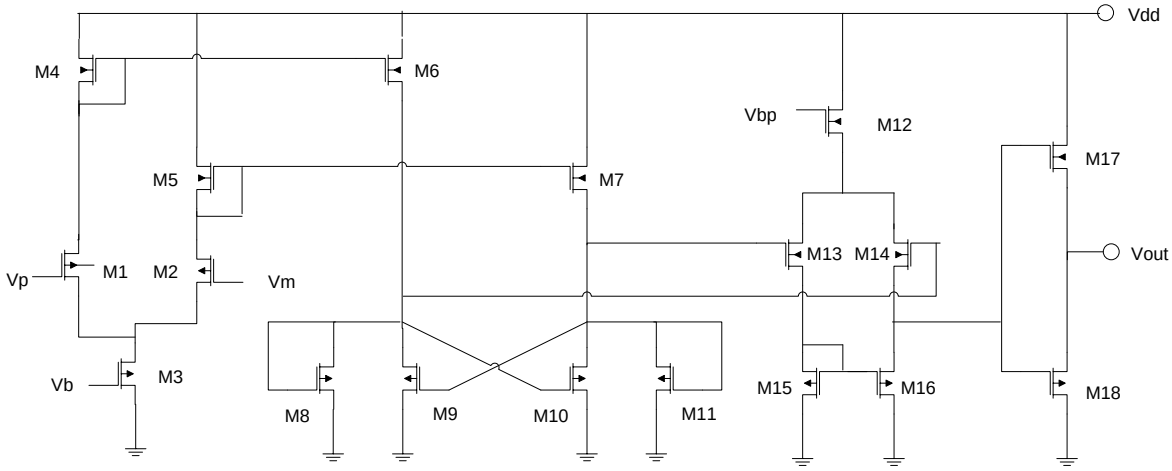

Figure 3.14 Comparator schematic

The bias currents in M3 and M13 are calculated from (3.5). Transistors M1, M2, M13, and M14 are sized to satisfy the gain-bandwidth using equation (3.6). Transistors M4, M5, M6, M7, and M12 are sized to satisfy the voltage drop across them using equation (3.8). Transistors M8, M9, M10, M11, M15, and M16 are sized to satisfy the voltage drop across them using equation (3.7). Transistors M17 and M18 are sized to satisfy rise and fall times using equations (3.9) and

(3.10), respectively, and the load capacitance is Cd. The schematic of the control logic is shown in Figure 3.15.

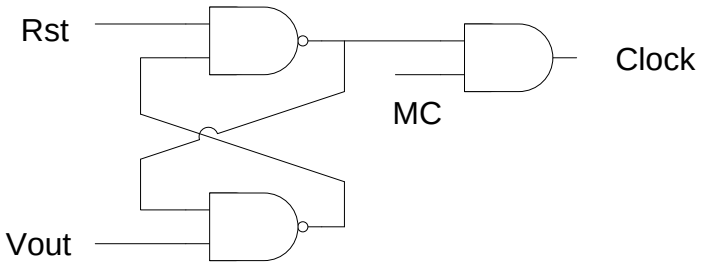

Figure 3.15 Control logic

The Rst signal sets the output of the S-R latch high. The Rst signal also resets the capacitor on the integrating op-amp. When the voltage Vc equals Vin, the output voltage of the comparator, Vout, will go high. This will cause the output of the S-R latch to go low, which will set the Clock signal low, and the counter will stop. The truth table for the S-R latch is shown in Table 3.2.

Table 3.2 Truth table of the S-R latch

S	R	Q_{n+1}	Qb_{n+1}	Operation
0	0	Q_n	Qb_n	hold
1	0	1	0	set
0	1	0	1	reset
1	1	0	0	not allowed

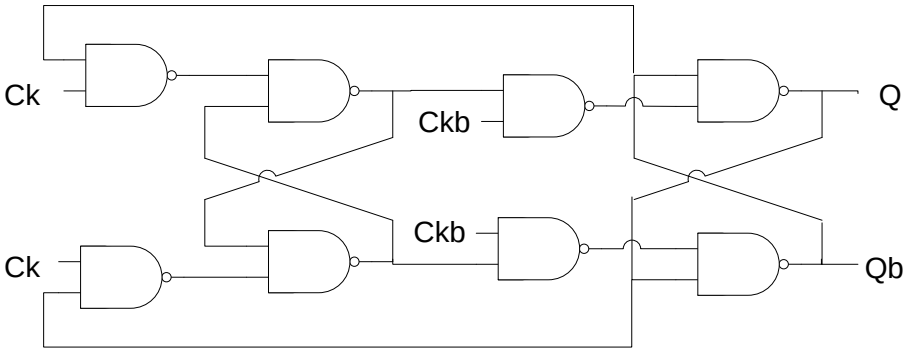

Figure 3.16 Master-slave T flip-flop

The counter was implemented using a cascade of ten master-slave T flip-flops. The schematic of a master-slave T flip-flop is shown in Figure 3.16.

The accuracy of the ADC depends on several factors, including the precision of the counter. Figure 3.17 shows the output of the counter. During normal operation of the ROIC, the ADC counters would operate at a frequency of 100MHz. However, the Master-slave T flip-flop structure has inherent feed through problems. If Ck and Ckb overlap, the counter will have glitches and intermittent codes which could cause the value of the counter to be incorrect. So, in order to demonstrate the correct operation of the ADC, the simulations were performed at an over-clocked frequency of 1GHz. If the ADC counter is susceptible to feed through, over clocking it by a factor of 10 should show the feed through.

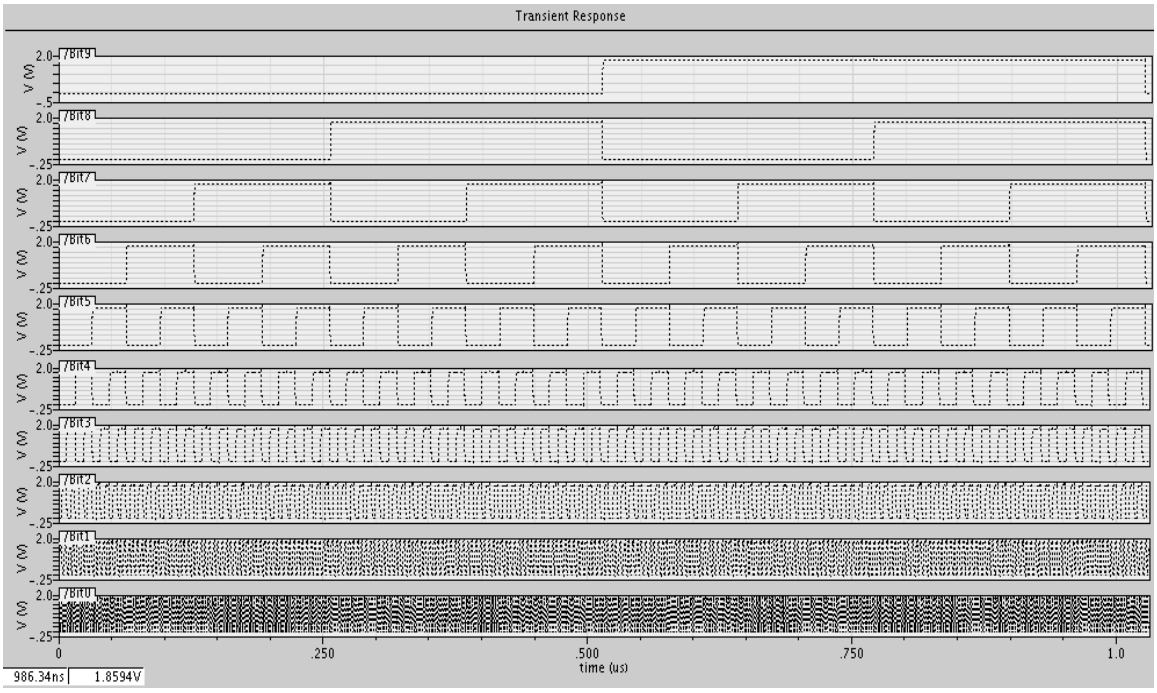

Figure 3.17 ADC Counter

The simulation in Figure 3.17 shows the ADC counter. The counter increments from 0 to 1023 over a period of 1.024µs. In the plot, the traces from top to bottom are Bit 9, Bit 8, Bit 7, Bit 6, Bit 5, Bit 4, Bit 3, Bit 2, Bit 1, and Bit 0. Bit 9 is the MSB, and Bit 0 is the LSB.

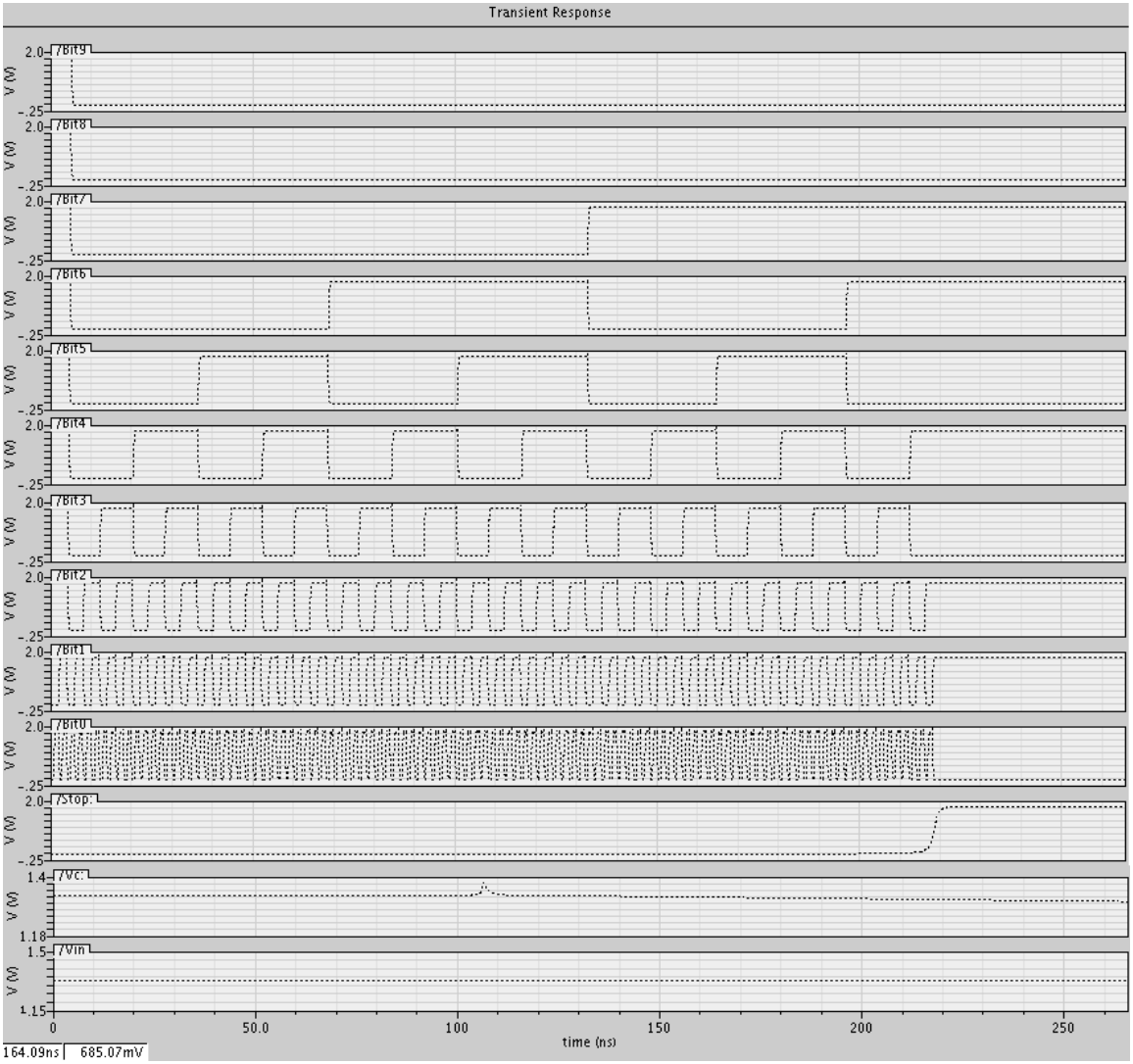

Figure 3.18 ADC simulation

The simulation shows that the counter functions properly at an over clocked frequency of 1GHz.Figure 3.18 shows the operation of the ADC. In the plot, Bits 9 through 0 are shown. The bottom three traces are Stop, Vc, and Vin, respectively. Stop is the digital signal which controls the S-R latch in Figure 3.15. Vc is the voltage on the output of the Op-amp in Figure 3.12. Vin is the input voltage. As the conversion continues, Vc decreases. When Vc equals the input voltage, Stop will go to logical '1,' and the counter will stop. In Figure 3.18, the input voltage is 1.3V, and Vref = 1.345V. Figure 3.18 shows that when Vin = Vc, Stop goes to logical '1,' and the counter stops.

3.4 Non-overlapping clocks

Non-overlapping clocks are used to generate shift registers for row and column addressing of the unit cells. The schematic is shown in Figure 3.19.

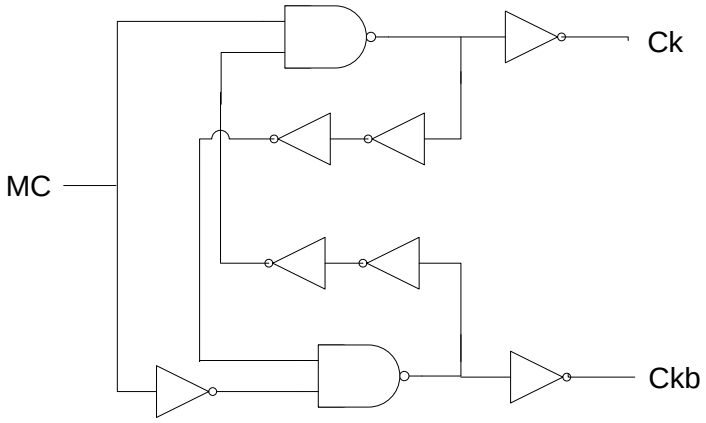

Figure 3.19 Non-overlapping clocks

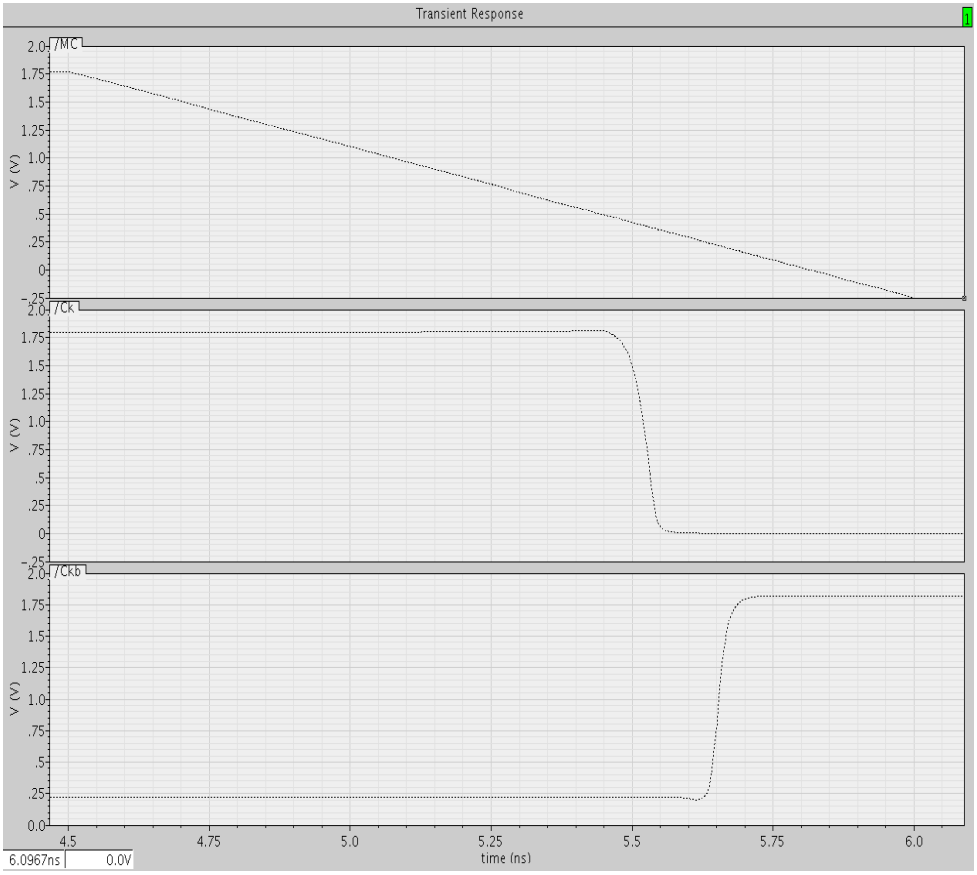

Figure 3.20 Falling edge of the input clock

This circuit generates non-overlapping clocks because the feed-back structure causes signals Ck and Ckb not to overlap. The non-overlapping clocks were simulated with an input clock frequency of 150MHz. The plots in Figure 3.20 and 3.21 show the rising and falling edges of the input clock. The simulations show that the output clocks do not overlap.

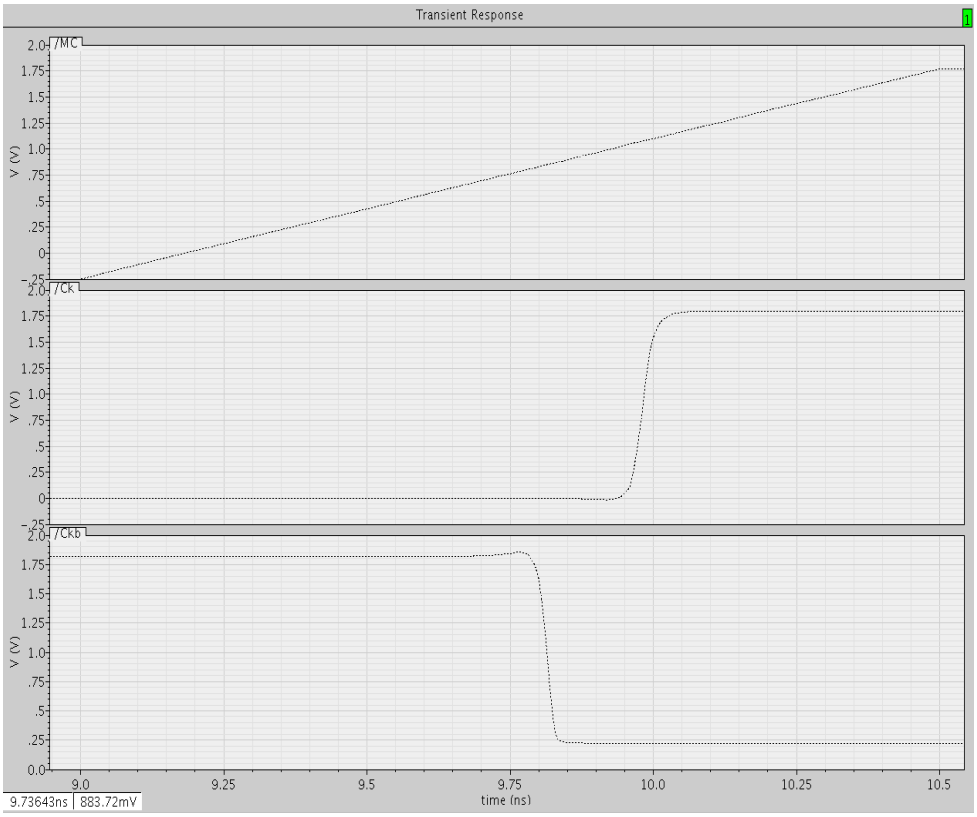

Figure 3.21 Rising edge of the input clock

3.5 Shift Registers

Shift registers are used in the column and row registers. The shift registers are created using non-overlapping clocks and S-R latches. The proposed design uses 3-bit and 10-bit shift registers. A 3-bit register is shown in Figure 3.22.

The Ck and Ckb signals are non-overlapping clocks. Syc is a synchronization signal. The first latch contains a cascaded S-R high followed by a S-R low. Its output will be logical ‘1’ when Syc is high.

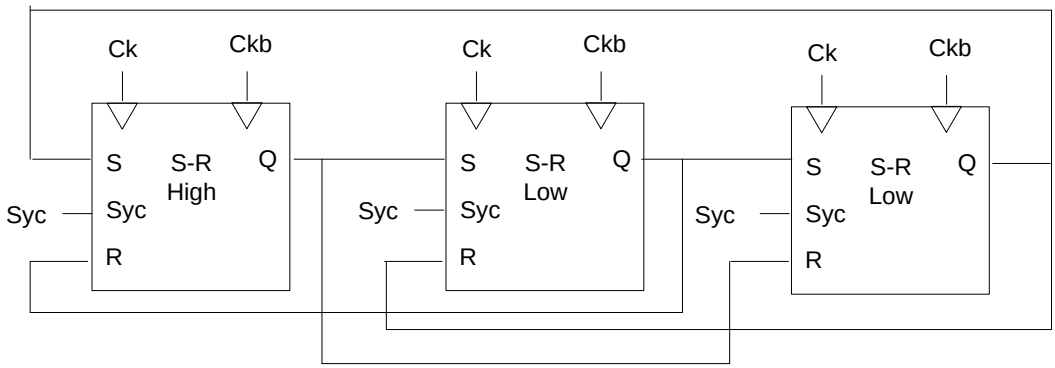

Figure 3.22 3-bit shift register

The second and third latches each contain two S-R low latches, which are cascaded, and their outputs will be logical '0' when Syc is high. The schematic of the S-R high is shown in Figure 3.23.

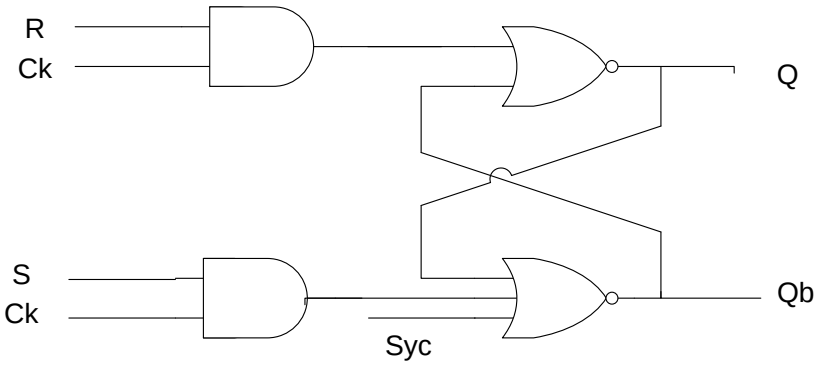

Figure 3.23 S-R high schematic

The truth table for the S-R high latch is shown in Table 3.3.

Table 3.3 Truth table of the S-R high latch

Syc	Ck	S	R	Q_{n+1}	Qb_{n+1}	Operation
1	X	X	X	1	0	synchronization
0	0	X	X	Q_n	Qb_n	hold
0	1	0	1	0	1	reset
0	1	1	0	1	0	set
0	1	1	1	0	0	not allowed

The schematic of the S-R low is shown in Figure 3.24.

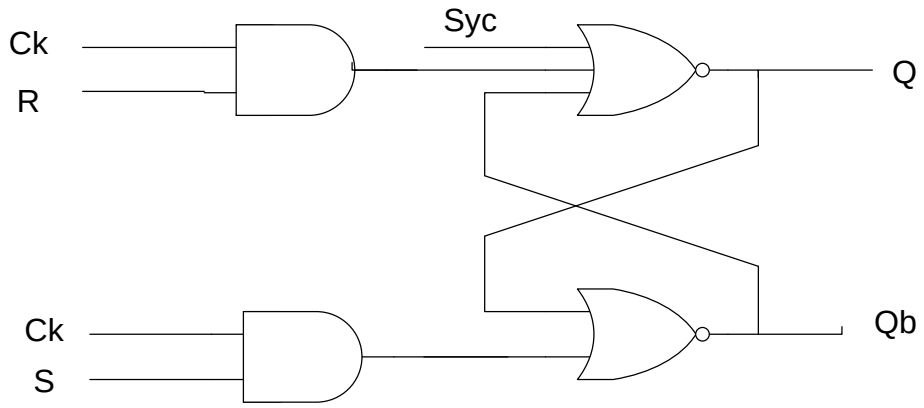

Figure 3.24 S-R low schematic

The truth table for the S-R low latch is shown in Table 3.4.

Table 3.4 Truth table of the S-R low latch

Syc	Ck	S	R	Q_{n+1}	Qb_{n+1}	Operation
1	X	X	X	0	1	synchronization
0	0	X	X	Q_n	Qb_n	hold
0	1	0	1	0	1	reset
0	1	1	0	1	0	set
0	1	1	1	0	0	not allowed

The shift registers were simulated with an input clock frequency of 150MHz. The plot below shows the operation of the 3-bit shift register. At the start of the simulation, the Syc is held high for 5ns. During this time, the output of the first register is logical ‘1,’ and the outputs of the other three are logical ‘0.’ After Syc goes low, the register begins shifting. Figure 3.25 shows the operation of the 3-bit shift register.

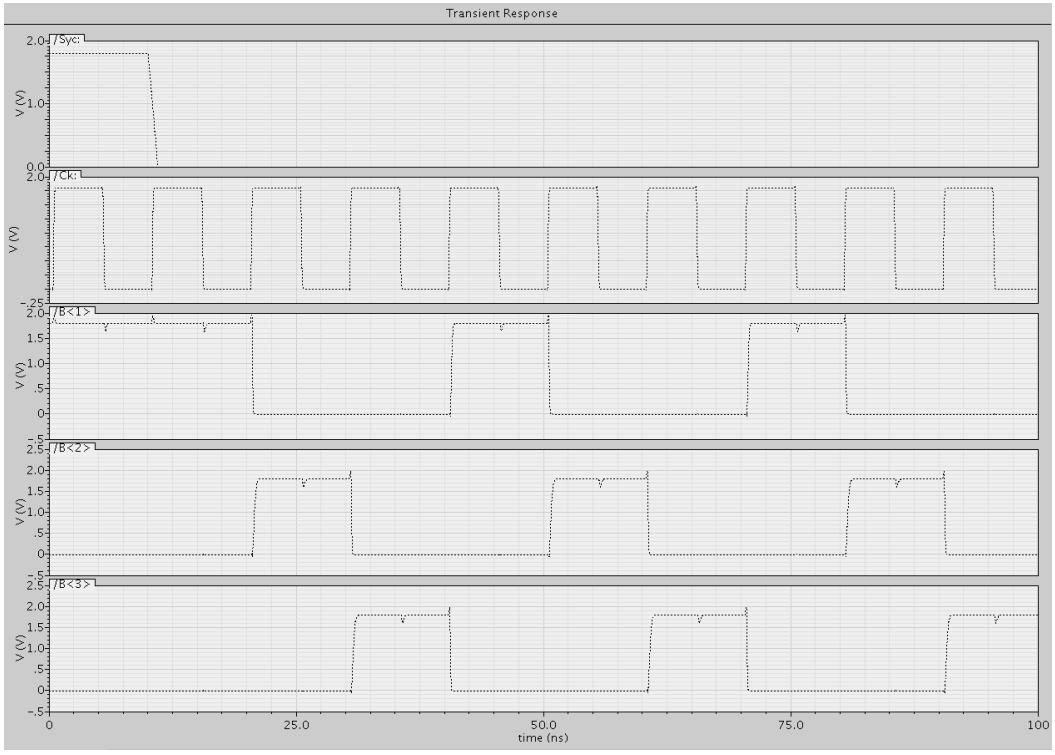

Figure 3.25 Simulation of the 3-bit shift register

Figure 3.26 shows the operation of the 10-bit shift register. At the start of the simulation, the Syc is held high for 5ns. During this time, the output of the first register is logical ‘1,’ and the output of the other nine is logical ‘0.’ After Syc goes low, the register begins shifting.

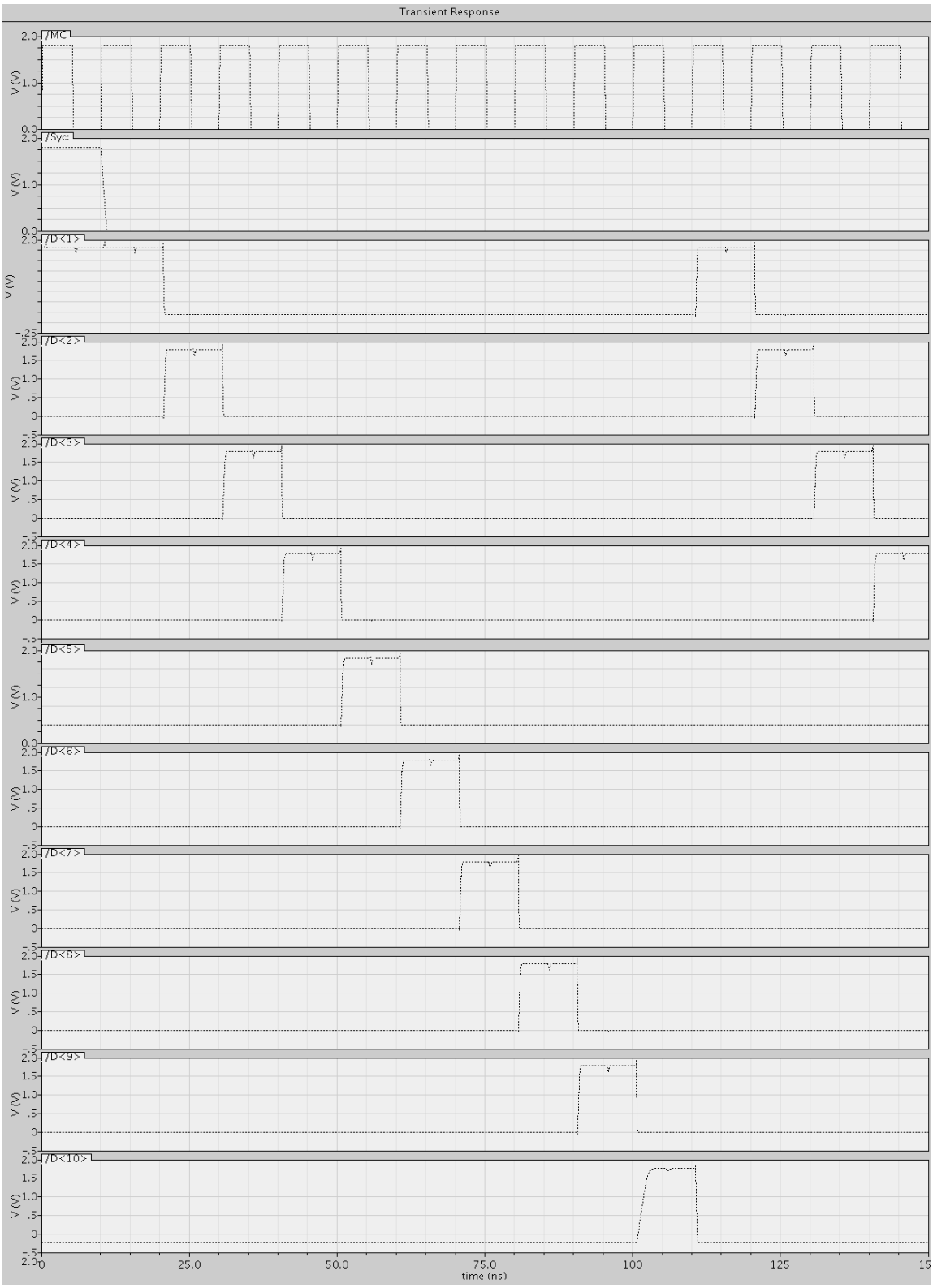

Figure 3.26 Simulation of the 10-bit shift register

3.6 Digital to Analog Converter

The most commonly used types of Digital to Analog converters (DACs) are binary-weighted current steering, R-2R ladder networks, charge scaling, and thermometer. Each type of converter has benefits that are unique to its architecture.

A binary-weight current steering DAC uses an array of N current sources, and N is the number of bits. The current sources are binary weighted, and the input code is a simple binary number. This type of converter does not require a buffer to drive a resistive load. One disadvantage with this architecture is the error due to switching. Because the current switches are in parallel, when one of the current sources is switched off and another is switched on concurrently, a glitch can occur in the output. At mid-code transitions, this is especially noticeable because the output will spike toward ground then back to the correct value. This type of converter is used in some types of high-speed applications which are not severely affected by glitches [65].

R-2R converters consist of a network of resistors that alternate in value between R and 2R. The digital input code determines whether each resistor is switched to ground or to the inverting input of the op-amp. Each node voltage is related to V_{REF} by a binary-weighted relationship which is caused by the voltage division of the ladder network. This type of converter requires device dimension matching to within the resolution of the converter. One particular cause of error is that the switch resistance must be negligible or a small voltage drop will occur across each switch, which will cause an error [66].

In charge-scaling converters, a parallel array of binary-weighted capacitors is used. The capacitors are connected to the input of an op-amp. After initially being discharged, the digital signals switch each capacitor to either V_{REF} or ground, and the output voltage is a function of the voltage division between the capacitors. A limitation of this converter is that there are parasitic capacitances on the capacitor array because of the input capacitance of the op-amp. Because of the parasitic capacitances, it does not have high-resolution [67].

Thermometer DACs use current-steering to convert the input digital code to an analog voltage. The thermometer has a decoder that converts each binary digit in the input code to a decimal value. For example, if the DAC contained six bits, there would be 63 current sources in

the converter. The main advantage of the thermometer DAC compared to the binary-weighted DAC is that the thermometer DAC is less prone to glitches. The disadvantages are that the thermometer DAC requires more circuitry and uses more power than the binary-weighted, R-2R, and charge scaling converters [68].

The reference voltage for the ADC is adjustable. Its value is controlled by a 10-bit binary-weighted current steering DAC. The DAC uses current sources and differential switches to route the current to a load resistor. Figure 3.27 shows the schematic.

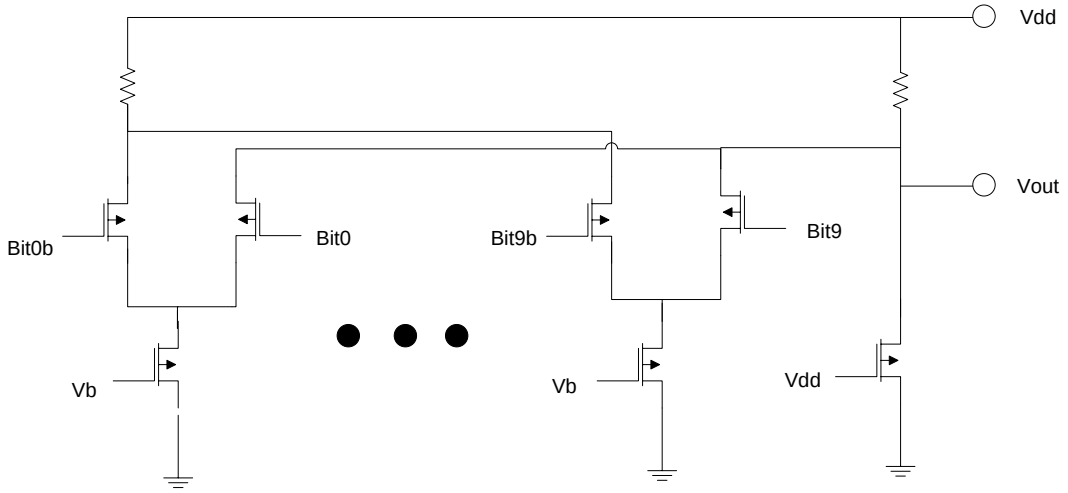

Figure 3.27 Digital to analog converter

To determine the currents, the differential voltage on the integration capacitor must be considered. The swing of Vota is 1.3V to 1.5V. The minimum current is given by:

$$I_{min} = \frac{V_{dd}-1.5V}{R} \tag{3.18}$$

When the current is maximum, the value of Vout should be 1.3V. So, the maximum current is given by:

$$I_{max} = \frac{V_{dd}-1.3V}{R} \tag{3.19}$$

The magnitude of the current for each current source is given by:

$$I_N = \frac{I_{max}-I_{min}}{2^N-1} \tag{3.20}$$

The sizes of the steering switches are found using equation (3.7).

Figure 3.28 shows the operation of the DAC. The input counts from 0 to 1023, and the output voltage sweeps from 1.3V to 1.5V.

The simulation shows that there are glitches at code transitions, especially at the mid-code transition. The output of the DAC would only have to be changed at the frame rate, which is 60Hz. So, the glitches would not affect the quality of the image because the output voltage would have approximately 16 ms to settle after the code was changed.

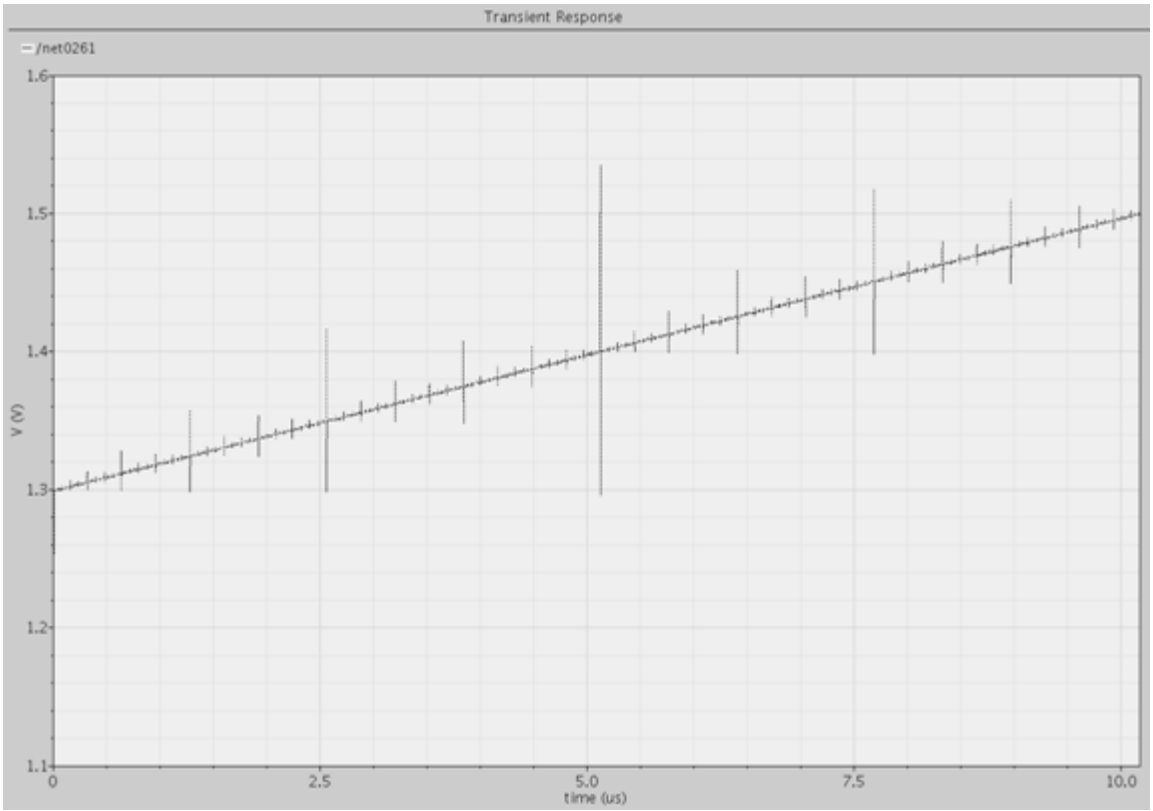

Figure 3.28 Simulation of the DAC

3.7 Output driver

After the integrated voltages from each unit cell have been digitized by the ADCs, complementary switches are used to multiplex the ten bits from each ADC in the column to ten bond-pads. The diagram of the multiplexer and inverter string is shown in Figure 3.29.

The W/L ratios of the complementary switches are found using the following expressions:

$$T_r = \left(\frac{1}{\mu_n \cdot C_{ox} \cdot \left(\frac{W}{L}\right)_N \cdot (V_{gs} - V_{tn})} \,||\, \frac{1}{\mu_p \cdot C_{ox} \cdot \left(\frac{W}{L}\right)_P (V_{gs} - V_{tp})} \right) \cdot C_{Load} \tag{3.21}$$

$$C_{Load} = (C_L + (W_N + W_P) \cdot L \cdot C_{ox}) \tag{3.22}$$

$$\left(\frac{W}{L}\right)_N \cdot \mu_n \cdot (V_{gs} - V_{tn}) = \left(\frac{W}{L}\right)_P \cdot \mu_p \cdot (V_{gs} - V_{tp}) \tag{3.23}$$

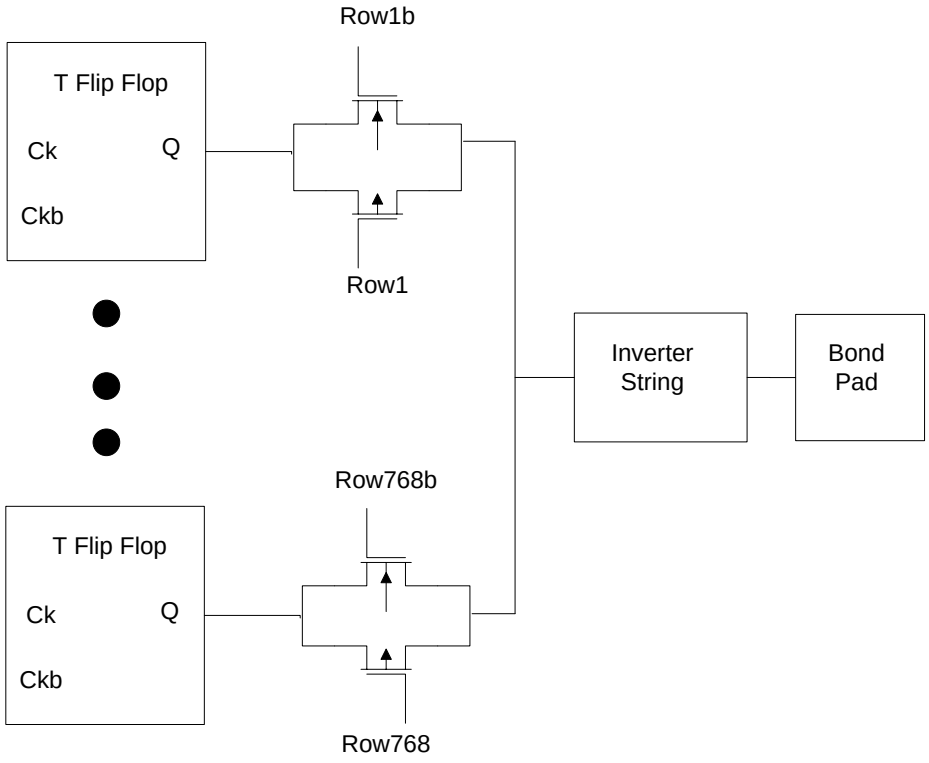

Figure 3.29 Multiplexer and output driver

The inverter string is used to drive the digital values off-chip. For laboratory testing, the output buffers must be able to drive a 50Ω load. To design the output driver, the number of inverters and sizes of the transistors in each inverter are calculated from the rise fall time equations. With the 50Ω load, the rise time of the inverter is given by:

$$T_r = \left(\frac{1}{\mu_n \cdot C_{ox} \cdot \left(\frac{W}{L}\right)_N \cdot (V_{gs} - V_{tn})} \,||\, 50\Omega \right) \cdot (C_L + W_N \cdot L \cdot C_{ox}) \tag{3.24}$$

The fall time of the inverter is given by:

$$T_f = \left(\frac{1}{\mu_p \cdot C_{ox} \cdot \left(\frac{W}{L}\right)_P \cdot (V_{gs} - V_{tp})} \,||\, 50\Omega \right) \cdot (C_L + W_P \cdot L \cdot C_{ox}) \tag{3.25}$$

C_L is the capacitance of the bond pad. The master clock frequency is 100MHz, and 1ns was selected as the required value for the rise and fall times. For the inverters, $\left(\frac{W}{L}\right)_P = 5{,}000$ and $\left(\frac{W}{L}\right)_N$ =1,250. Because these ratios are very large, a string of inverters must be used. To calculate the number of inverter in the string, the following expression is used:

$$\left(\frac{W}{L}\right)_{P,1} \cdot N \cdot e = \left(\frac{W}{L}\right)_P \tag{3.26}$$

N is an even number, and e is the natural logarithm. The W/L ratio of the first inverter in the string is usually chosen to be approximately 1 for the PMOS device. For this readout circuit, N is eight. Figure 3.30 shows a simulation of the output voltage on the bond pad with a load resistance of 50Ω. The input bits alternate between 0 and 1. The simulation shows that there is a skew of approximately 1.5ns on the output. Also, the output voltage only rises to approximately 1.7V. This happens because the 50Ω load resistances creates a large R-C time constant, and in order to drive the output voltage to nearly 1.8V, the W/L of the PMOS device must become larger than the current ratio.

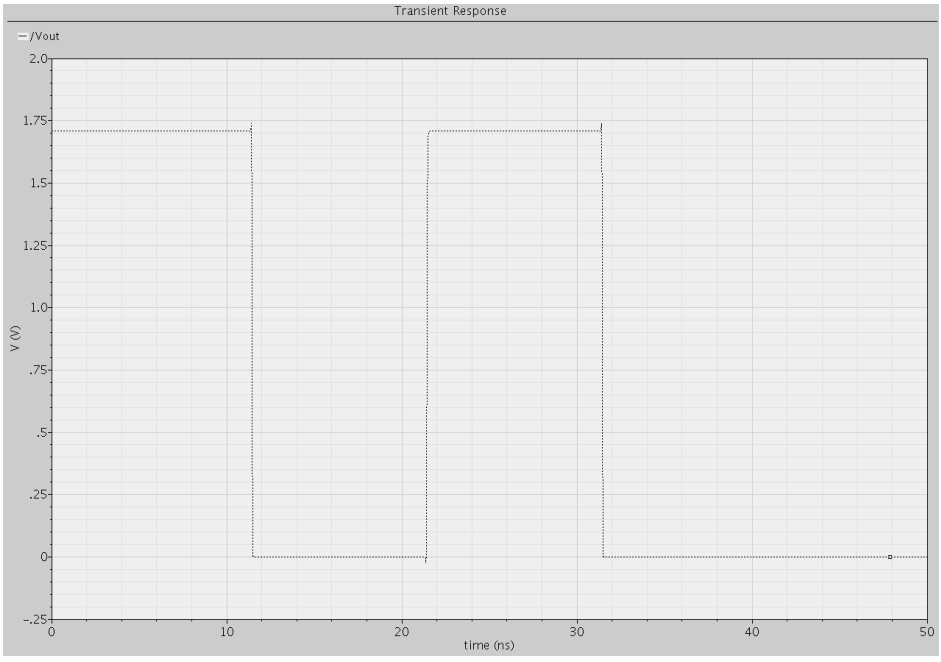

Figure 3.30 Simulation of the output driver

CHAPTER 4

RESULTS

In this chapter, simulation results are presented for one column of unit cells. Layouts of the components are also shown. For all of the simulations, parasitics from the layout were included in the simulations.

4.1 Column simulation

To simulate the column, the entire one column of unit cells was laid out, and parasitics were extracted. The simulation results in this chapter show the outputs for each circuit in the column. Figure 4.1 shows a zoomed-in view of the chip. The figure shows a portion of the unit cell array, column shift registers, current mirrors, row shift registers, ADCs, and output drivers.

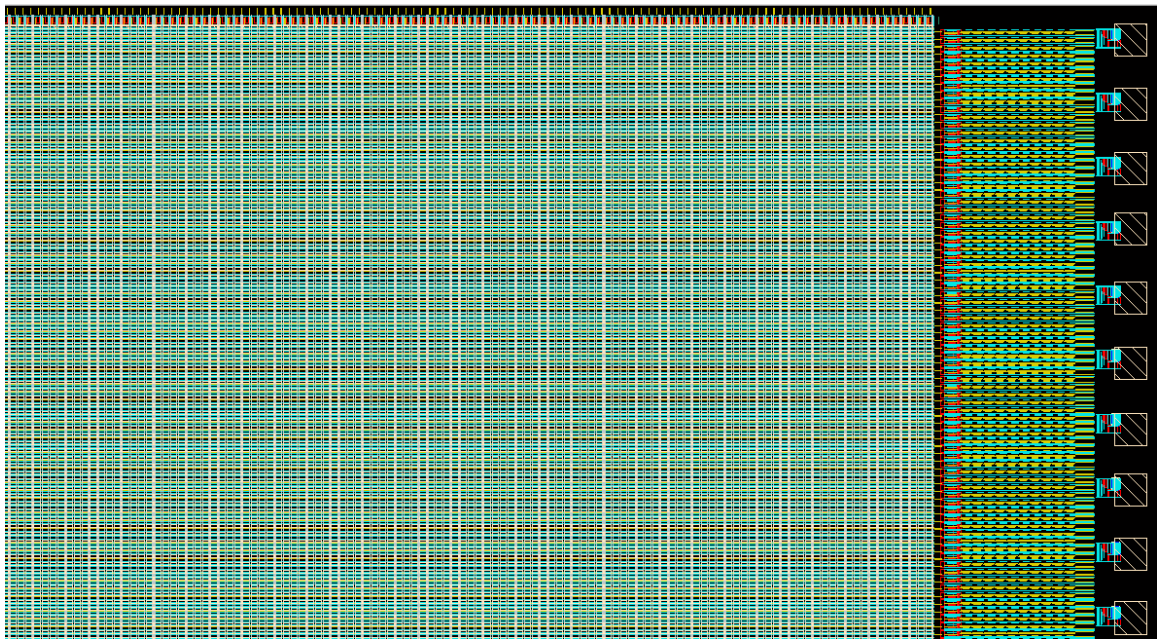

Figure 4.1 Layout of the chip

Figure 4.2 shows a zoomed-in view of the chip. The figure shows six S-R low latches in the column shift register, six blind photo diodes and current mirrors, and 24 unit cells.

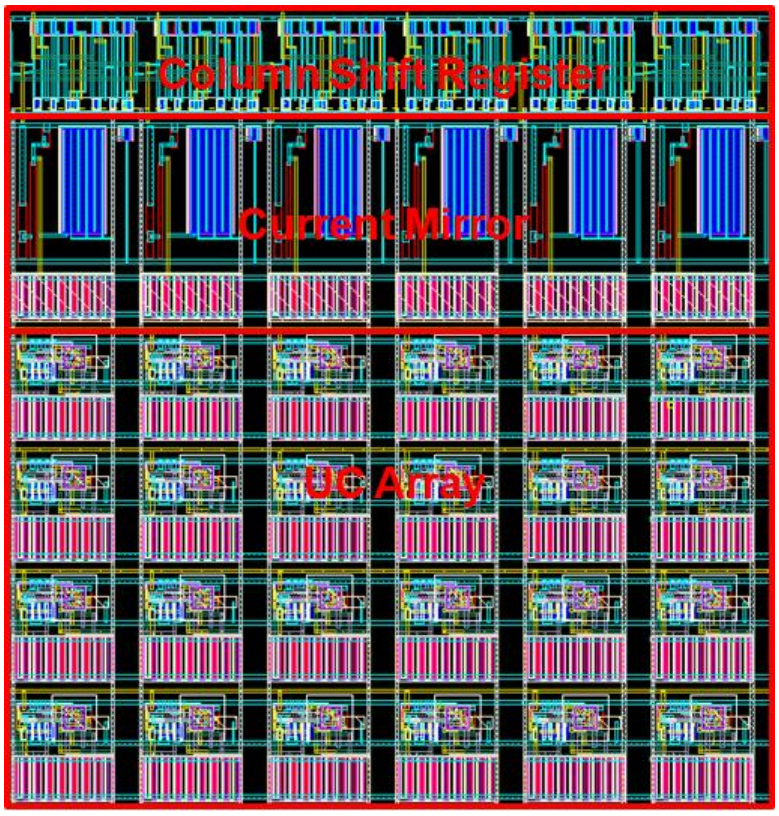

Figure 4.2 Layout of 24 unit cells

Figure 4.3 shows the column shift register, blind photo diodes, row shift register, ADCs, and eighty unit cells in the top-right corner of the chip.

The unit cells were simulated using the method from chapter 3, but the capacitances of the blind and active photodiodes were modeled as the parasitic capacitances from the layout. In the plots, the output voltage on the integration capacitor is shown for unit cells in rows #1, #384, and #768. It is important to test the output of several unit cells in each column because parasitics in the layout will create resistors which will cause voltage drops, and capacitors can cause clock glitches and slow rise times in the digital circuits. If the parasitics from the layout affected the device performance, there would be a difference among the response of the unit cells in rows #1, #384, and #786.

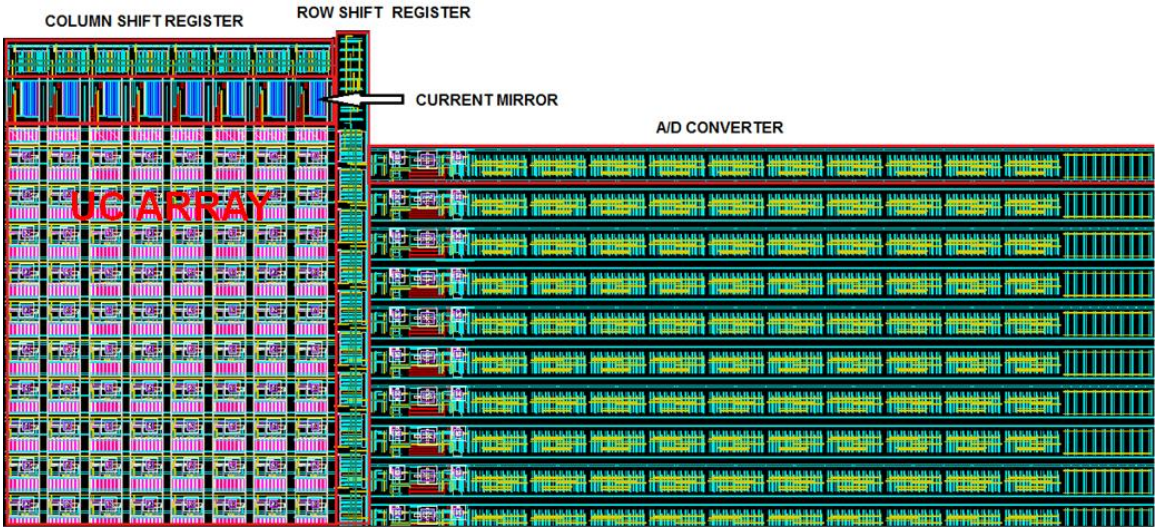

Figure 4.3 Layout of 80 unit cells

In Figure 4.4, the DC current is set to 1pA, and the output voltage integrates.

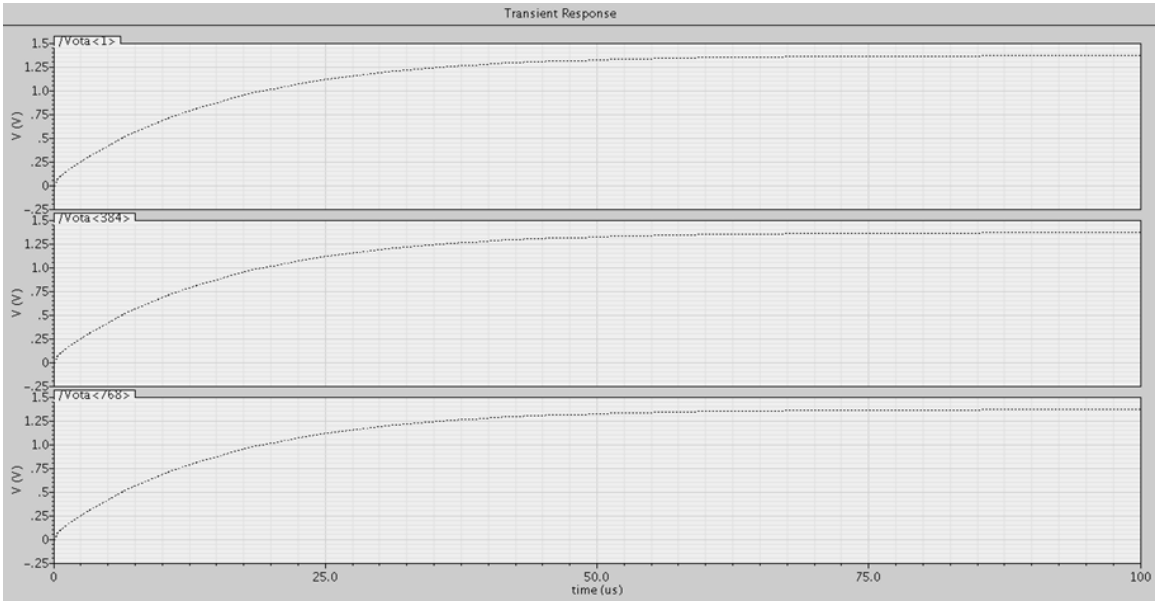

Figure 4.4 Output voltage with the DC current at 1pA

In Figure 4.5, the DC current is set to 1nA, and the output voltage integrates.

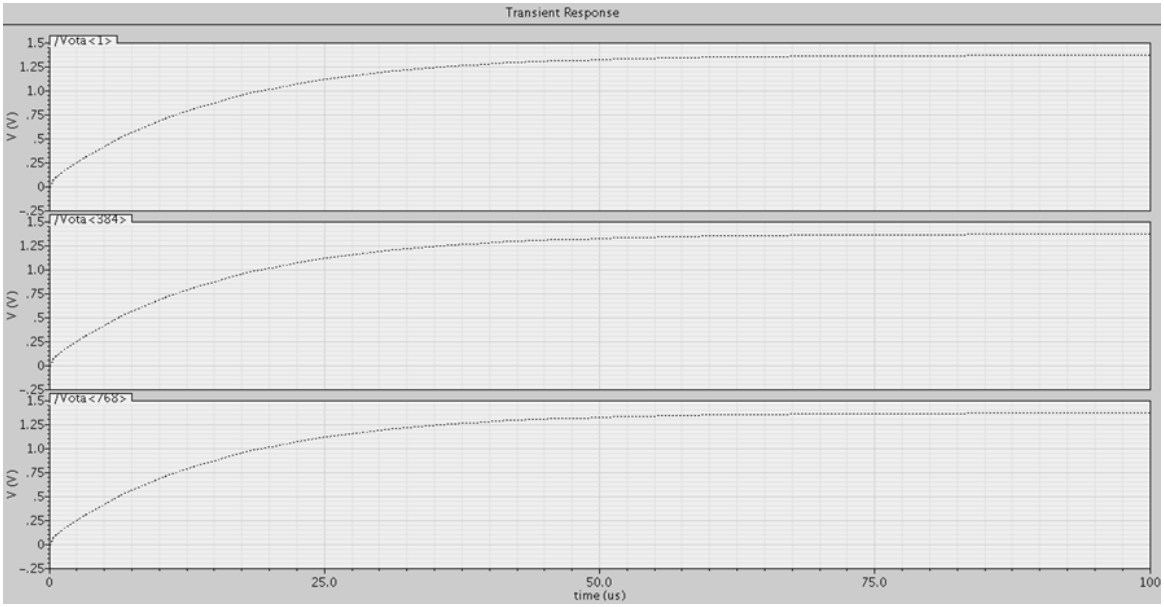

Figure 4.5 Output voltage with the DC current at 1nA

In Figure 4.6, the DC current is set to 1μA, and the output voltage integrates.

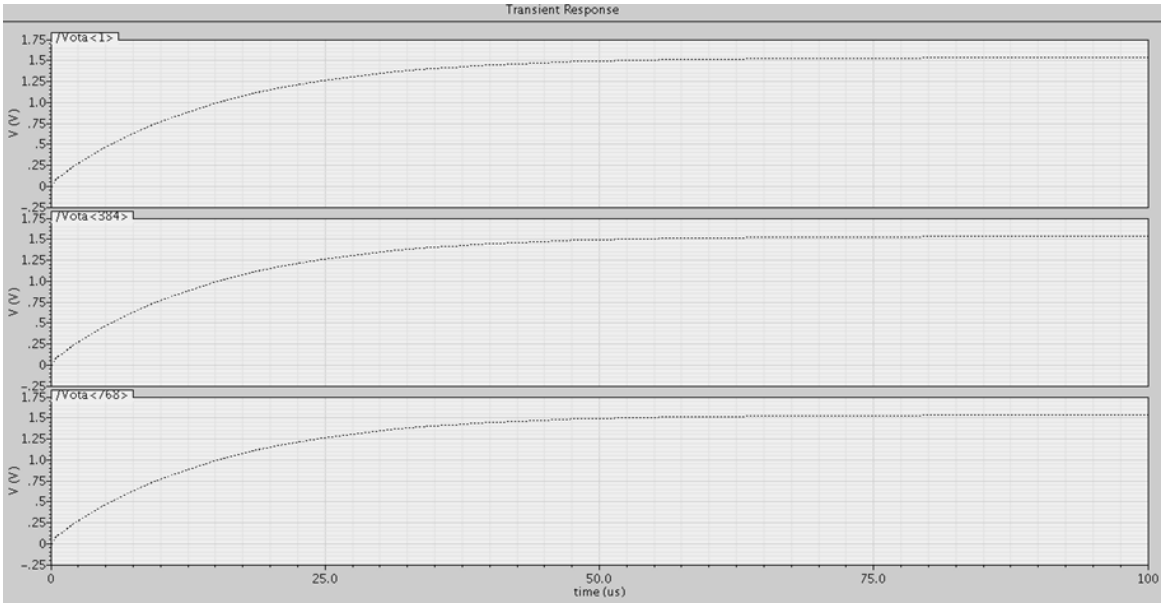

Figure 4.6 Output voltage with the DC current at 1μA

The three plots show that unit cells in rows #1, #384, and #768 have responses that are almost identical. Figure 4.7 shows the linearity of the OTA. To test the linearity, the Rst signal is held at logical ‘0,’ and the DC current sweeps from 1pA to 1μA over 50μs. The outputs of the unit

cells in rows #1, #384, and #768 are shown. The DC current magnitude is the bottom signal in the plot.

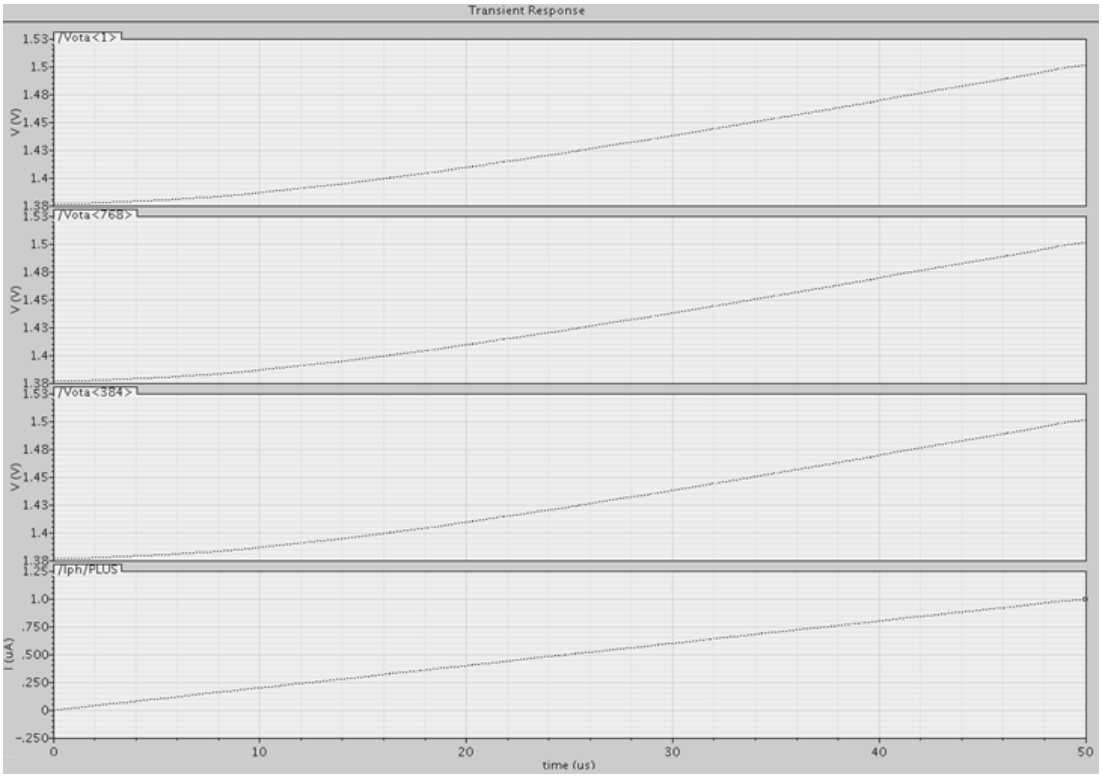

Figure 4.7 OTA linearity

In Figure 4.8, the photo current is 1pA, and the dark current ramps from 1pA to 1μA. The SNR is shown. Figure 4.9 shows the SNR for photo currents and dark currents in the range of 1pA to 1μA. The x-axis, y-axis, and z-axis are the photo current, dark current, and SNR, respectively.

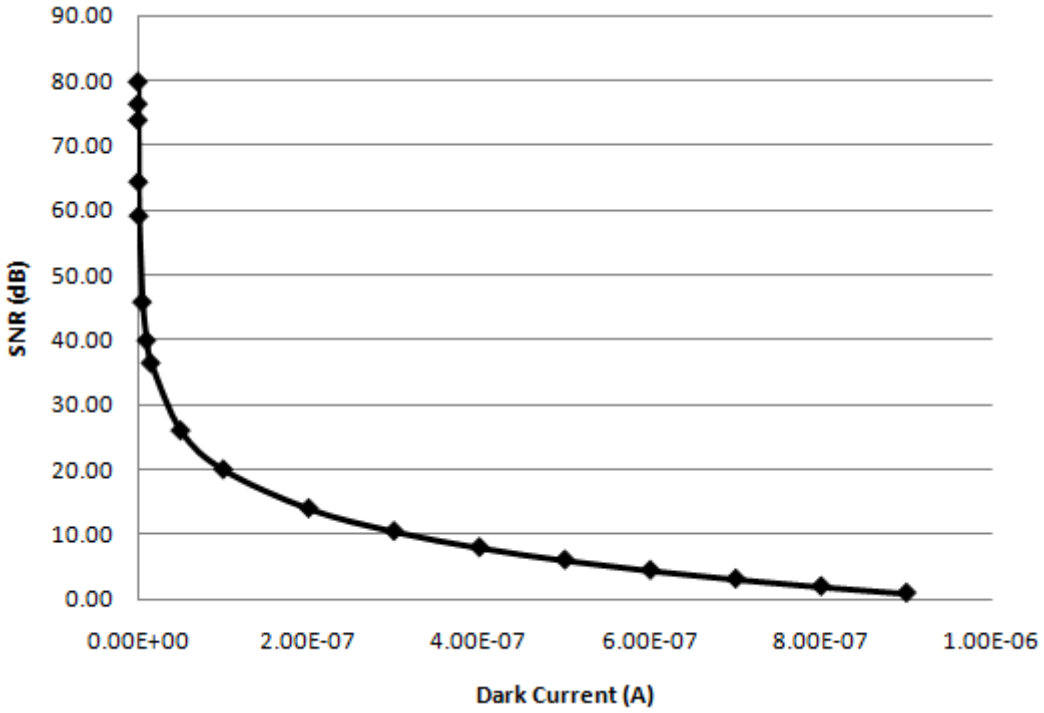

Figure 4.8 SNR with the photo current at 1pA

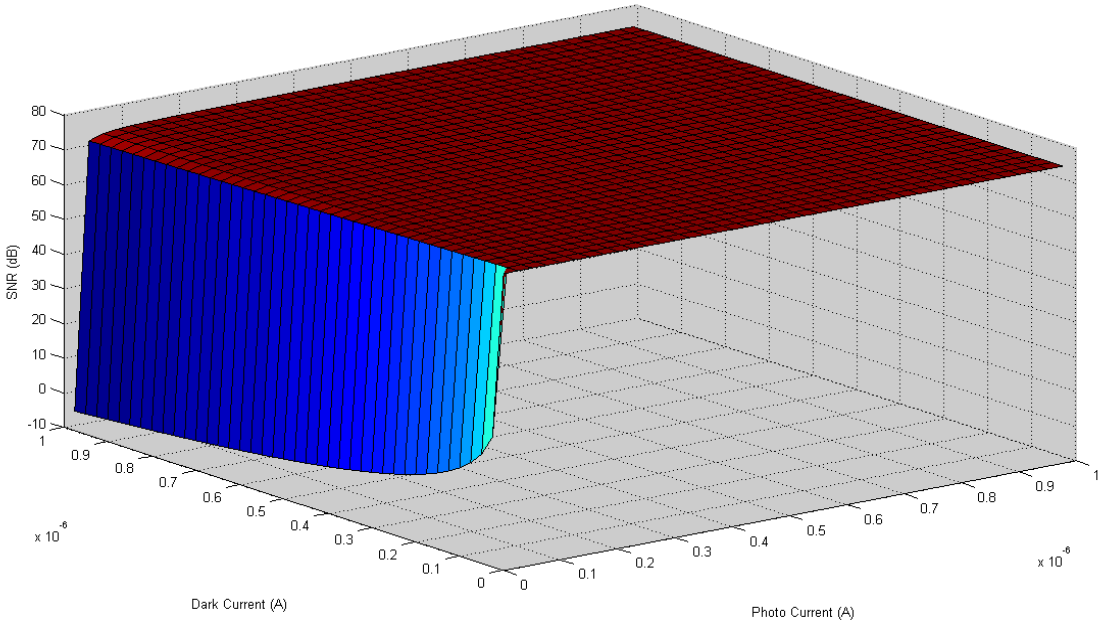

Figure 4.9 SNR versus dark current and photo current

The dynamic range is shown in Figure 4.10. The frequency range is 60Hz to 500Hz.

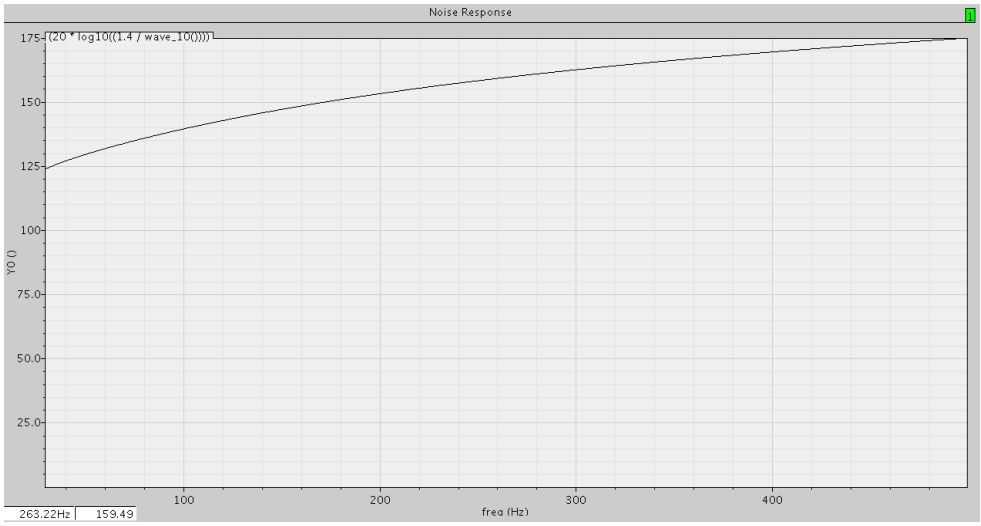

Figure 4.10 Dynamic range

The layout of the UC is shown in Figure 4.11. The circuit occupies 25x25 μm^2.

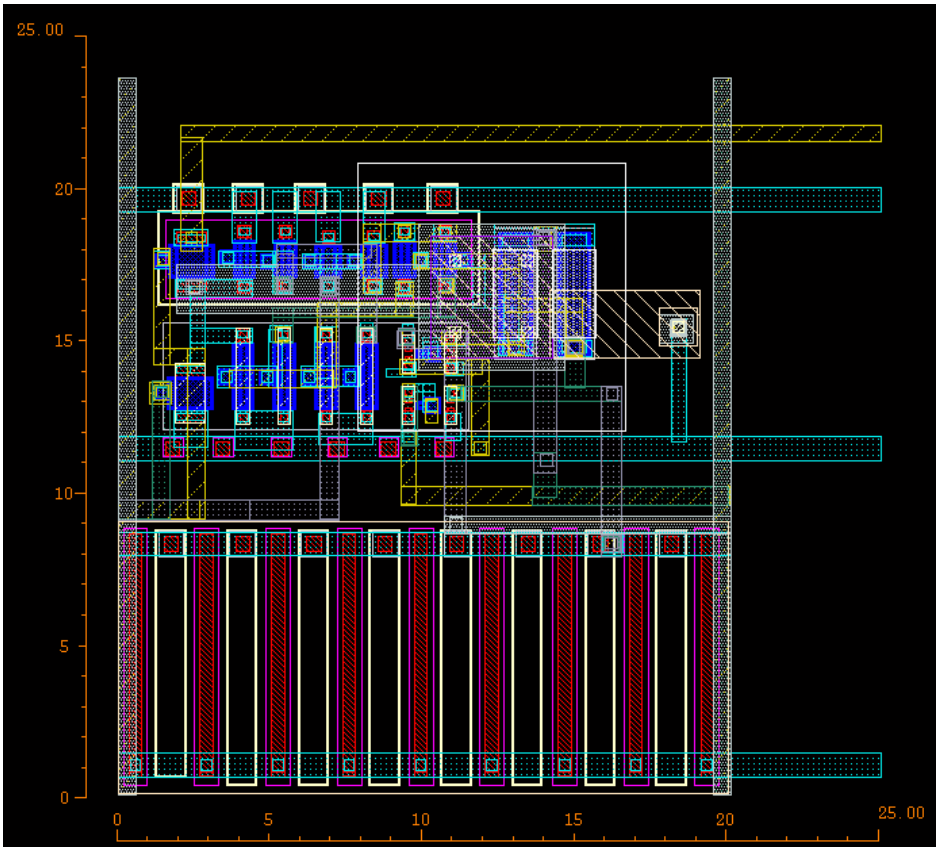

Figure 4.11 Layout of the unit cell

4.2 Analog to Digital Converter

The layout of the ADC is shown in Figure 4.1. The size of the ADC is approximately 25x1000 μm^2. The ADC was simulated at a frequency of 1GHz. Figure 4.12 shows the output of the ADC. The input voltage is ADC simulation with Vin=1.48V, and Vref=1.5V

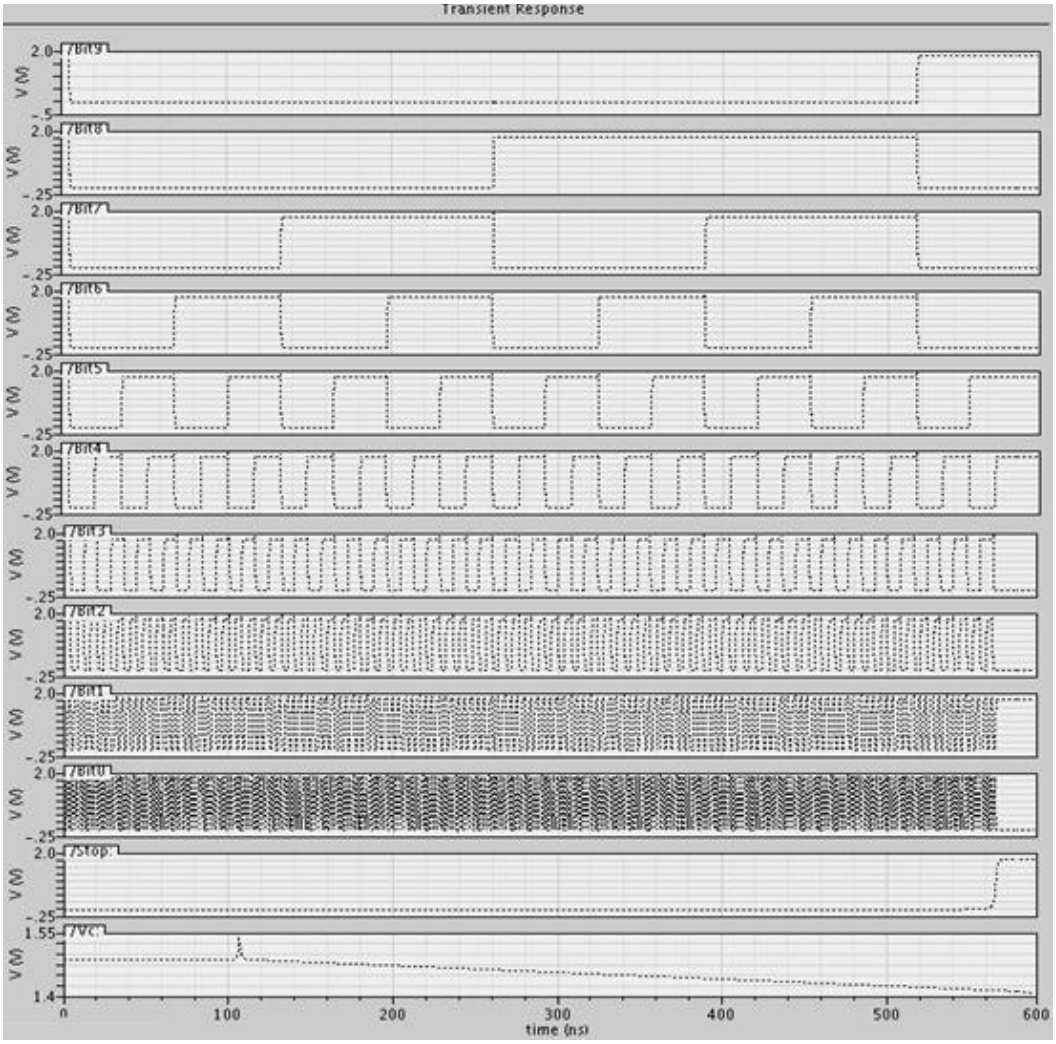

Figure 4.12 Simulation of the ADC

4.3 Non-overlapping clocks

The layout of the non-overlapping clocks is shown in Figure 4.13. The non-overlapping clocks were simulated with an input clock frequency of 100MHz. Figure 4.14 and Figure 4.15 show the rising and falling edges of the input clock. The simulations show that the output clocks do not overlap.

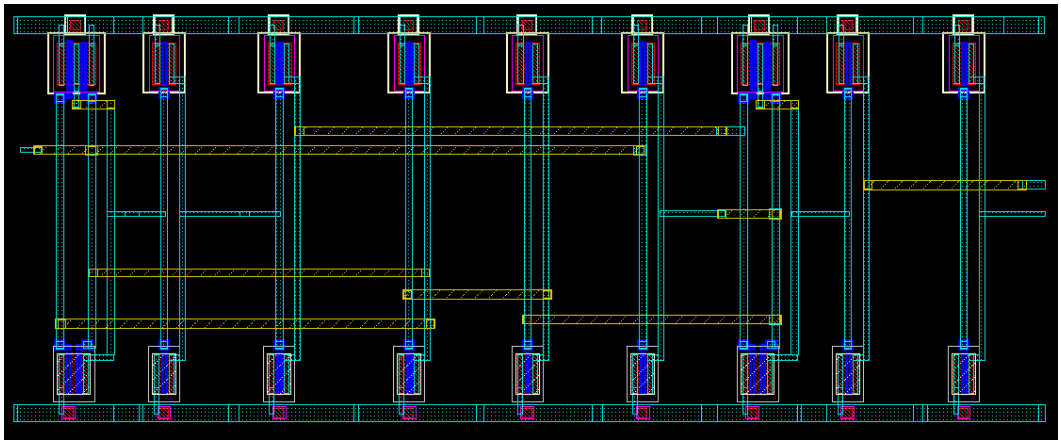

Figure 4.13 Layout of non-overlapping clocks

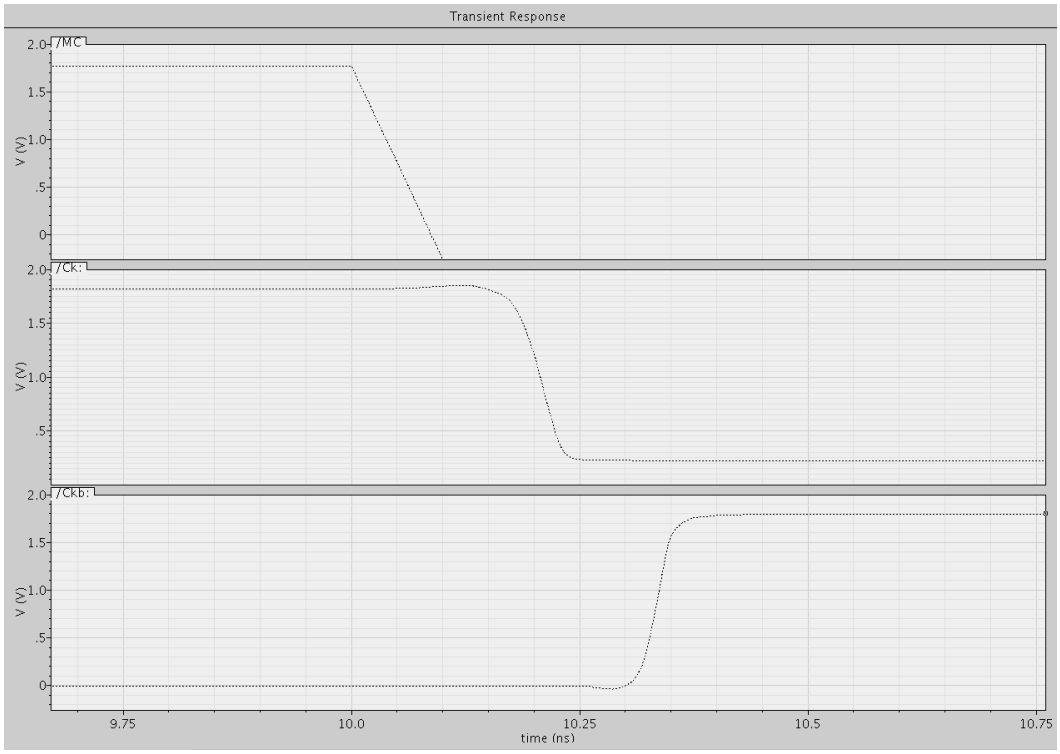

Figure 4.14 Falling edge of the input clock.

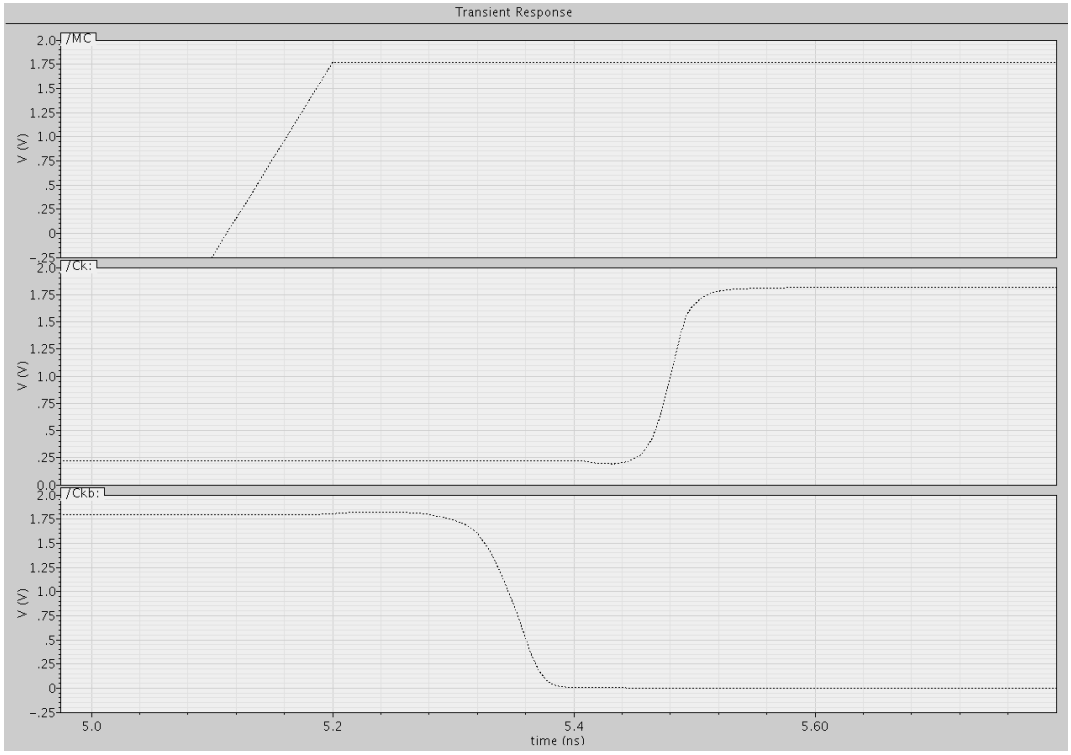

Figure 4.15 Rising edge of the input clock.

4.4 Shift registers

The layout of the 3-bit shift register is shown in Figure 4.16.

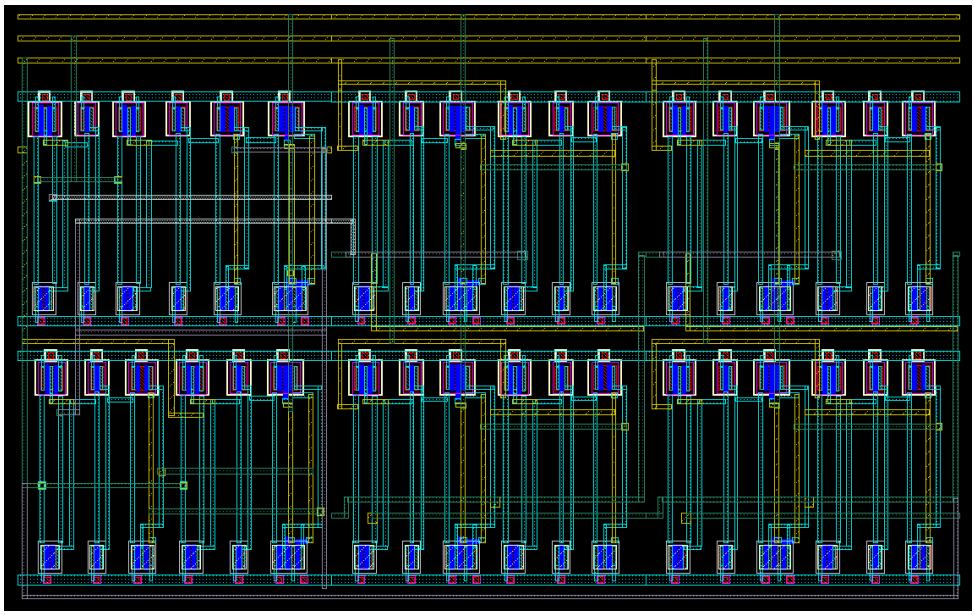

Figure 4.16 Layout of 3-bit shift register

Figure 4.17 shows the operation of the 3-bit shift register. At the start of the simulation, the Syc is held high for 10ns. During this time, the output of the first register is logical 1, and the output of the other three is logical 0. After Syc goes low, the register begins shifting.

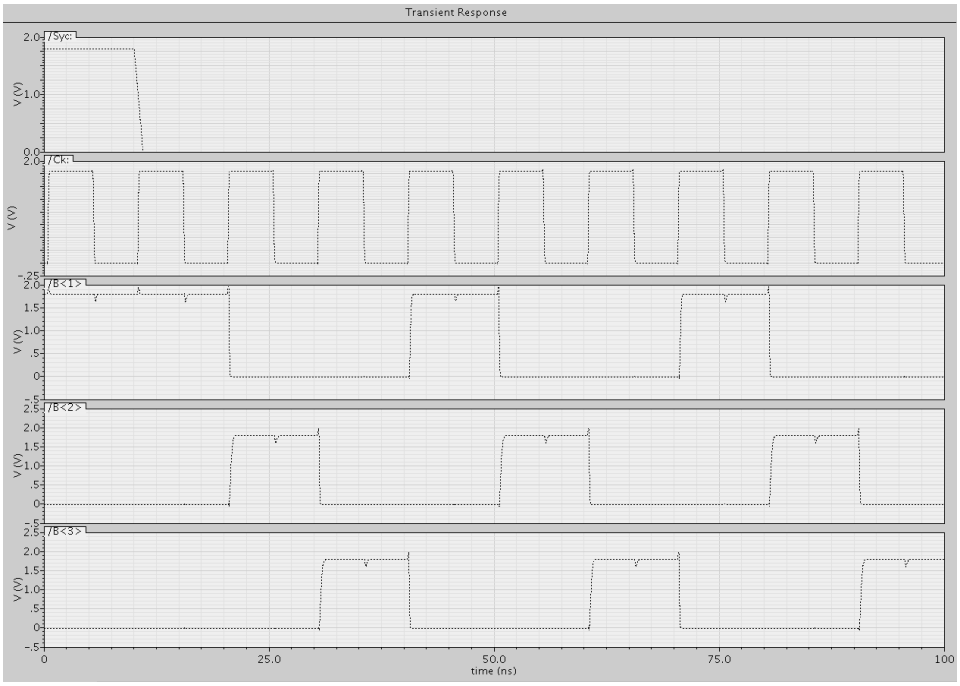

Figure 4.17 Simulation of 3-bit shift register

The layout of the 10-bit unit cell is shown in Figure 4.18.

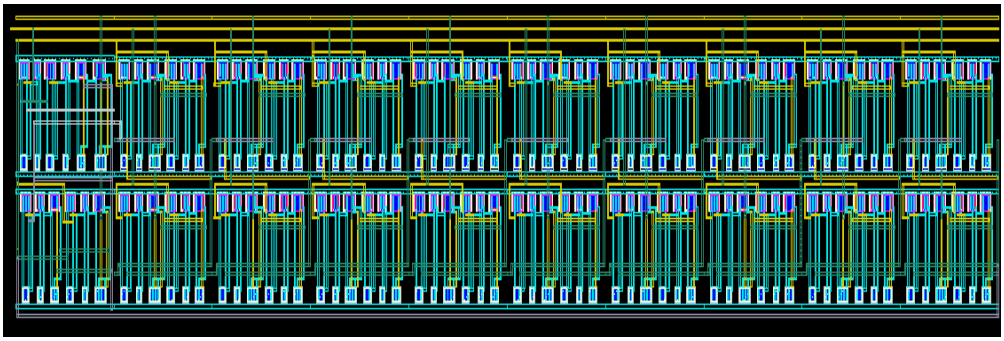

Figure 4.18 Layout of 10-bit shift register

Figure 4.19 shows the operation of the 10-bit shift register. At the start of the simulation, the Syc is held high for 10ns. During this time, the output of the first register is logical 1, and the output of the other nine is logical 0. After Syc goes low, the register begins shifting.

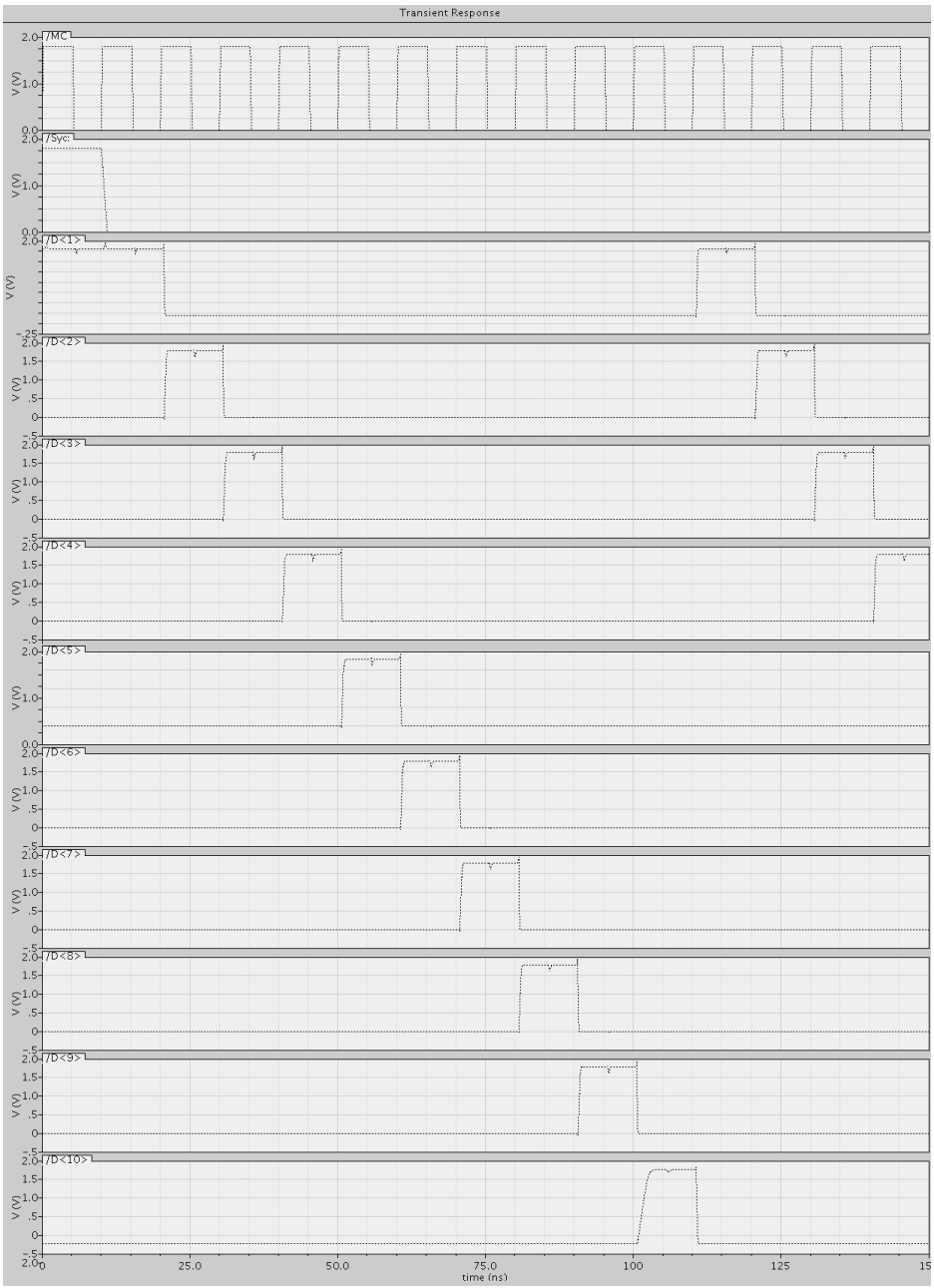

Figure 4.19 Simulation of 10-bit shift register.

4.5 Digital to Analog Converter

The layout of the DAC is shown in Figure 4.20.

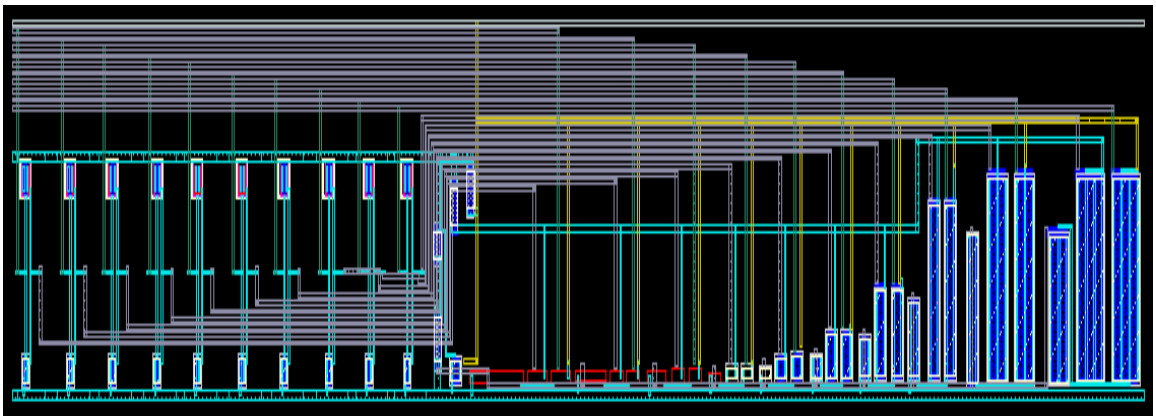

Figure 4.20 Layout of DAC

The DAC was simulated at a frequency of 100MHz. The output voltage versus input code is shown in Figure 4.21. The input code ramps from 0 to 1023.

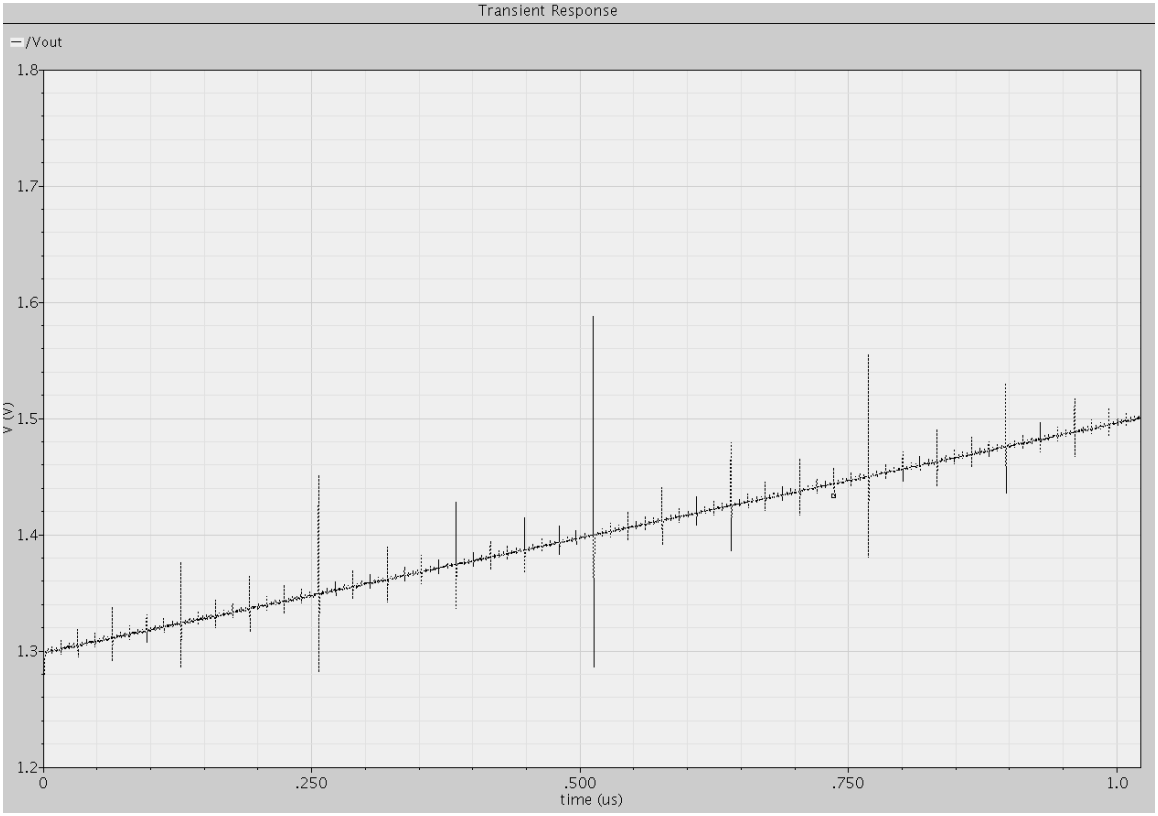

Figure 4.21 Simulation of DAC

4.6 Output driver

The layout of the output driver is shown in Figure 4.22.

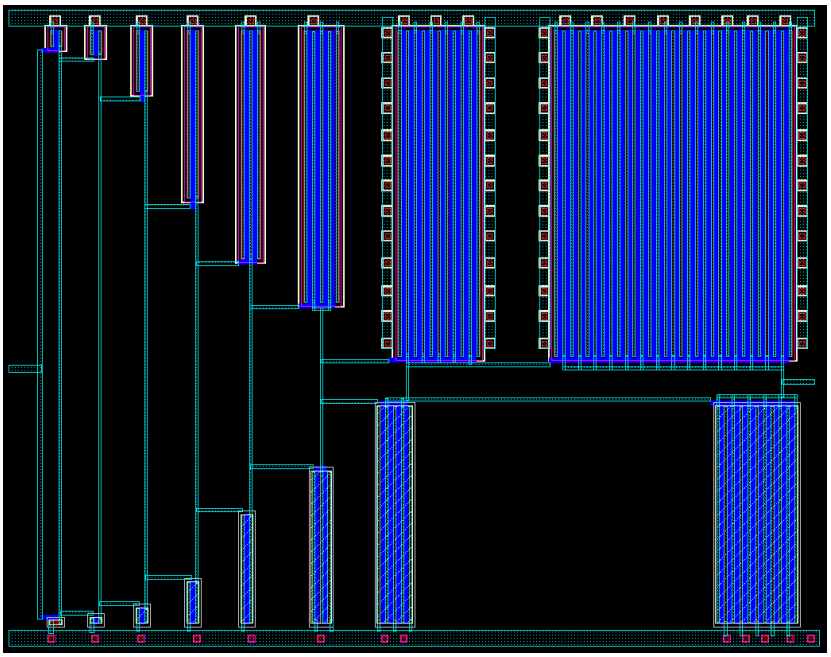

Figure 4.22 Layout of output driver

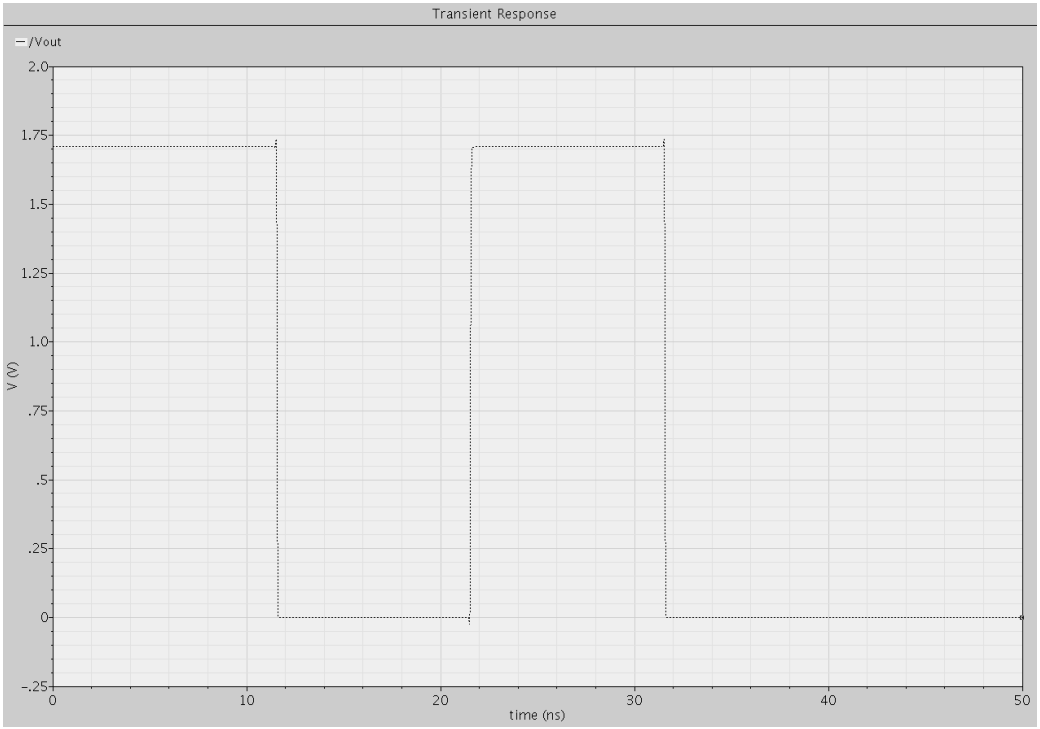

Figure 4.23 Simulation of output driver

The simulation of the output driver is shown in Figure 4.23. The simulation shows that there is a skew of approximately 2ns on the output. Also, the output voltage only rises to approximately 1.7V.

4.7 Comparison

Table 4.1 presents a comparison of the proposed circuit and other circuits. The other circuits in this table are the ones that also perform dark current suppression.

The pixel gain is calculated by:

$$Gain = \frac{V_{range}}{Noise_{Amp}} \tag{4.1}$$

V_{range} is the voltage swing on the amplifier that drives the load capacitance off the chip, and $Noise_{Amp}$ is the noise of this amplifier. This gain is not available because this amplifier would only be needed for tape-out. The fixed pattern and random noise would be measured on a fabricated chip.

The minimum detectable contrast is defined as:

$$Min.Contrast = 20 \cdot log\left(\frac{Min\ photo\ current}{Max\ dark\ current}\right) \tag{4.2}$$

The differential signal dynamic range is defined as:

$$Diff.\ sig.\ range = 20 \cdot log\left(\frac{Max\ photo\ current}{Min\ photo\ current}\right) \tag{4.3}$$

Table 4.1 Comparison with other methods for dark current suppression

Criterion	Ref. [6]	Ref. [7]	Ref. [8]	Ref. [9]	This work
Detector interface circuit	CTIA	Buffered direct injection	Buffered direct injection	CTIA	Op-Amp
Dark Current Suppression Method	Global suppression current created using memory	Current memory inside unit cell	Current memory inside unit cell	Blind photo diode in each unit cell	Global suppression current generated by blind photo diode
Pixel size ($\mu m^{2)}$	55 x 50	50 x 400	50 x 50	150 x 150	25 x 25
Fill factor	9%	N/A	N/A	N/A	28%
Max. power per pixel	32 µW	25 µW	3 µW	N/A	500 nW
Pixel gain	42 dB	72 dB	N/A	N/A	TBD
Fixed pattern Noise	2.6 mVrms	N/A	N/A	N/A	TBD
Random Noise	4.0 mVrms	N/A	N/A	N/A	TBD
Linearity	N/A	99%	> 90%	N/A	99%
Background handling capacity	1-40 nA	1-300 nA	1-100 nA	N/A	1 pA-1 µA
Photo current range	1 pA-40 nA	1 pA-300 nA	1 pA-100 nA	N/A	1 pA-1 µA
Current memory error	1%	0.25%	0.3%	N/A	1%
Minimum detectable contrast	-32 dB	-85.5 dB	-34 dB	N/A	-120 dB
Differential signal dynamic range	77 dB	94.6 dB	85 dB	N/A	120 dB
Average SNR	80dB	90dB	90dB	N/A	80dB

A comparison between this work and other high SNR architectures is shown in Table 4.2.

Table 4.2 Comparison with other high SNR Architectures.

Circuit	Average SNR	Pixel (μm^2)	Fill Factor	Power	Ref.
This work	80dB	25 x 25	28%	500nW	-
Companding sensors	35dB	10 x 10	20%	2µW	[38-41]
Multimode sensors	40dB	20 x 20	N/A	N/A	[42-44]
Clipping sensors	50dB	23 x 23	25%	250nW	[45-47]
Frequency based sensors	50dB	30 x 30	14%	10µW	[48-50]
Time to saturation	40dB	45 x 45	12%	N/A	[51-53]
Global control over integration time	40dB	10 x 10	40%	401nW	[54-56]
Autonomous control over integration time	50dB	85 x 85	15%	N/A	[57-59]
Dark current subtraction using global current	80dB	55 x 55	9%	32 µW	[6]
Dark current subtraction using memory	90dB	50 x 400	N/A	25 µW	[7]
Dark current subtraction using memory	90dB	50 x 50	N/A	3 µW	[8]
Dark current subtraction using blind photodiode	N/A	150 x 150	N/A	N/A	[9]

CHAPTER 5

CONCLUSION

In this thesis, a unit cell for high-SNR applications was designed and simulated using the TSMC 0.18µm CMOS technology. The proposed circuit was significantly smaller than other circuits that perform dark current subtraction because less circuitry was used inside the unit cell. The proposed circuit uses only two transistors and one resistor inside each unit cell to suppress the dark current. The size of the circuit in the layout was 25 x 25 μm^2. With this new unit cell and routing approach, the size of the unit cell was reduced by 300% compared to other circuits that also suppress dark current. The ROIC is also competitive with [6-9] in areas including linearity, photo current range, background handling capacity, and power dissipation.

For future work, a ROIC for frame rates above 10kHz is desirable. The proposed unit cell is compatible with high rates up to 100kHz, but the ROIC can only operate up to 500Hz. The factor that prevents the ROIC from reaching a frame rate of 10kHz is the number of outputs. The ROIC has ten outputs, and if the number of outputs were increased, the frame rate could be increased.

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BIOGRAPHICAL INFORMATION

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