PHASE LOCKED LOOP FOR RADIATION HARDENED ENVIRONMENT

by

JER-FU DENNIS WU

Presented to the Faculty of the Graduate School of

The University of Texas at Arlington in Partial Fulfillment

of the Requirements

for the Degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

THE UNIVERSITY OF TEXAS AT ARLINGTON

December 2006

ACKNOWLEDGEMENTS

Earning my master of science at University of Texas at Arlington has been a rewarding experience. As with any challenge, it began eagerly with an opportunity and ends successfully with perseverance and determination, learning and training, support from mentors, and a certain amount of luck.

With gratitude, I thank my advisor Dr. Enjun Xiao at UTA for offering me the opportunity to work in collaborative research group. I have benefited from his guidance, support, and technical expertise.

I also thank Dr. Alan Davis, Dr. Jung-Chih Chiao and Dr. Ping Peggy Gui for reviewing my thesis and being on my defense examination committee.

There are several companies and organizations that have supported this research project such as financial support from the U.S. R&D funds for the ATLAS upgrade at CERN. I appreciate Peregrine Semiconductor for the fabrication of experimental circuits. Appreciation also goes to Brookhaven National Laboratory (BNL) for radiation tests.

Partha Ghosh deserves a special acknowledgment from Integrated Circuit Design And Reliability Laboratory (ICDAR) at the Electrical Engineering Department at UTA. I would like to give a special appreciation to Partha for his mentor with Cadence, ring VCO design, PLL architecture, and discussions.

I thank Peiqing Zhu at SMU for collaborations on LC VCO and CML divider design, and discussions of the inductor, varactor, and self-bias PLL design. Thank SMU colleagues for their TSPC and D2S circuits.

I acknowledge the following colleagues for their technical discussion and friendship. Support from Wickham Chen and Junheng Zhang greatly assisted my use of SMU's simulator. Professor Jingbo Ye, Andy Liu, Annie Xiang, and John Yang tested and analyzed valuable device level data and performance during the pre-radiation and post-radiation design. Thank you to fellow ICDAR students Karthik Neelakantan, Tao Wang, Young-Sik Seo, and Harvijaysinh Raj for their support and encouragement.

I thank my parents for their support and encouragement to finish my master degree.

November 16, 2006

ABSTRACT

PHASE LOCKED LOOP FOR RADIATION HARDENED ENVIRONMENT

Publication No. _____

Jer-Fu Dennis Wu, M.S.

The University of Texas at Arlington, 2006

Supervising Professor: Dr. Enjun Xiao

This thesis describes a Phase Locked Loop (PLL) design for operation within a radiation environment. Specific design architecture and techniques were implemented to help mitigate radiation effects that degrade PLL performance. This thesis presents several elements of a rad-hard PLL that were developed to solve this challenge, such as a very wideband coupling coefficient LC VCO that has a much higher frequency tuning range than conventional varactor based LC VCOs.

The PLL consists a Phase and Frequency Detector (PFD), a rail to rail charge pump, a loop filter, the quadrature LC tank Voltage Controlled Oscillator (VCO), a

Current Mode Logic (CML) frequency divider, a True Single-Phase Clocked (TSPC) divider, and a Differential to Single-ended converter (D2S).

The main radiation effects on MOSFETs include changes of threshold voltage and mobility, which causes the drain current to decrease. As a result, the phase noise and tuning range of PLL are degraded.

The proposed radiation hard PLL uses the unique Peregrine Semiconductor Corp (PSC) 0.25um Silicon on Sapphire (SOS) CMOS process technology. The center frequency is 3.6 GHz, and the tuning range is from 2.3 GHz to 5.1 GHz. The minimum frequency tuning range is 70% under pre-radiation and post-radiation conditions. Simulated power consumption is 124.23 mW in pre-radiation and 145.73 mW in post-radiation. Simulated pre-radiation phase noise is -130 dBc/Hz at 1 MHz offset, and post-radiation phase noise is -127.9 dBc/Hz at 1MHz offset. The locking time is less than 450ns under post-radiation conditions. The overall focus is on a systematic design methodology for radiation-hardened PLL in a SOS CMOS process.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

CHAPTER 1

INTRODUCTION

1.1 Background

The University of Texas at Arlington (UTA) Integrated Circuit Design and Reliability Laboratory (ICDAR) is collaborating with the Southern Methodist University (SMU) Integrated Circuits and System Laboratory and the SMU Physical Electronics Laboratory to design a new generation Gigabit Optical Link (GOL) for the Inner Detector and Liquid Argon Calorimeter Upgrade to the ATLAS Particle Physics Experiment at the Large Hadron Collider (LHC) in Geneva, Switzerland.

CERN is the European Organization for Nuclear Research, the world's largest particle physics centre. It is located along the Franco-Swiss border near Geneva.

ATLAS is a particle physics experiment that explores the fundamental nature of matter and the basic forces that shape our universe. The ATLAS detector will search for new discoveries in the head-on collisions of protons of extraordinarily high energy. ATLAS is one of the largest collaborative efforts ever attempted in the physical sciences. There are 1800 physicists (Including 400 students) participating from more than 150 universities and laboratories in 35 countries.

For the ATLAS project, SMU physicists designed and built elements of readout electronics for the electromagnetic calorimeter system, including a 1600 channel optical link system with a total data rate of about 2.7 terabits per second.

The UTA/SMU team is tasked to design the PLL, serializer, and line driver for the GOL.

1.2 Motivation

The GOL serializer chip is a multi-protocol high-speed transmitter that must be able to withstand radiation doses compatible with the LHC detectors radiation environment. The IC supports two standard protocols, the G-Link and the Gbit-Ethernet, and sustains transmission of data at both 800 Mbit/s and 1.6 Gbit/s.

The GOL is basically a simple 20-bit serializer with an integrated PLL. This project designed and tested the high-speed critical parts (PLL, serializer) that will be incorporated into the GOL ASIC. The GOL will be made in deep submicron technology using design techniques that are resistant to radiation effects. The PLL is one of the main design challenges in the GOL transmitter IC.

Figure 1.1 shows the GOL serializer block diagram on the Gigabit Optical Link Transmitter manual [1].

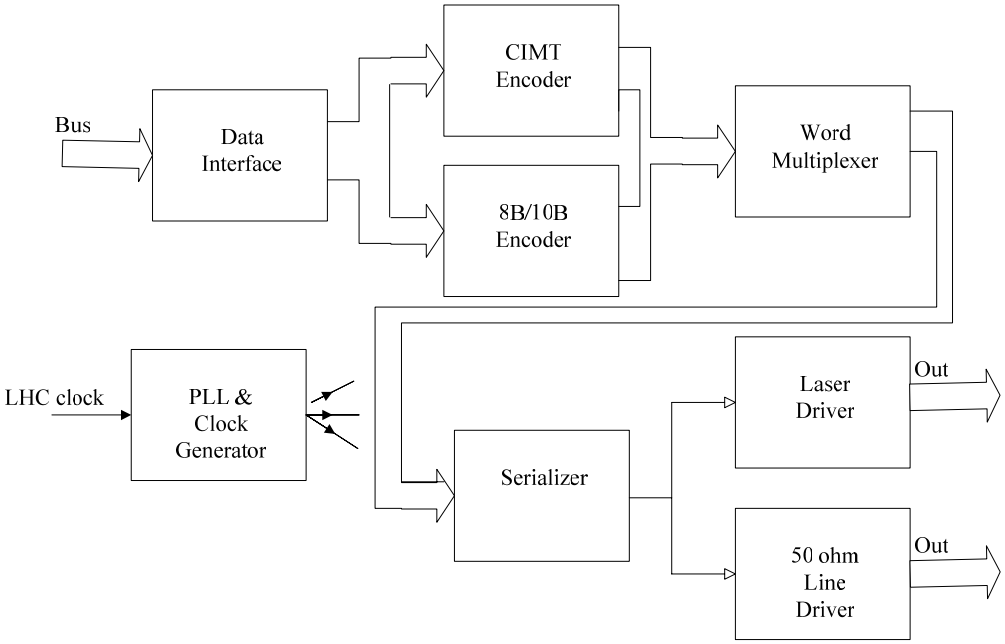


Figure 1.1 Block diagram of a GOL Serializer

The radiation effects are both instantaneous and long-term. The instantaneous effects of the collision of a single energetic particle on an active device are called single-event effects (SEE). The cumulative effects of several single energetic particles over a long period of time are called total ionization dose (TID) effects. The objective of this project is to develop a phase-locked loop that can tolerate both effects.

1.3 Organization

This thesis is organized as follows:

Chapter 2 discusses Radiation and SOS process. This chapter describes the effects of radiation on active devices (mainly in MOSFETs).

Chapter 3 discusses the PLL background.

Chapter 4 discusses the spiral inductor design on High Frequency Structure Simulator (HFSS) and varactor design.

Chapter 5 addresses the radiation hardened PLL design.

Chapter 6 is focused on simulation results and discussion.

Chapter 7 presents layout considerations.

Chapter 8 summarizes this research and proposes future PLL design work.

CHAPTER 2

RADIATION EFFECTS AND SOS PROCESS

2.1 Total Ionization Dose effects

Total ionization dose (TID) effects on active devices are a long term exposure of electronic components to radiation. The total amount of ionization dose depends on the intensity of radiation and the period of exposure time. SMU has preliminary TID results for Silicon-On-Sapphire technology based upon testing of the initial prototype chip. From the experimental results, TID resulted in a PMOS and NMOS threshold voltage shift, and an unexpected back-channel current leakage was observed.

2.1.1. Threshold voltage shift on PMOS

The TID test was carried out in July 2006 by the Brookhaven National Laboratory's Co-60 gamma source on 32 types of transistors. Their I-V curves were measured before and after the irradiation, and during the month long annealing period. The total dose is 615 krad at 30 krad/hr. The width and length ratio of PMOS transistor is 40μm/0.25um with 4 fingers on the layout. From the measurement and calculation, it is found out that the TID effects increased the threshold voltage of PMOS transistors by about 0.2 V.

2.1.2. Threshold voltage shift on NMOS

During the experiment, the total dose is 33 krad at 1.2 krad/hr. The width and length ratio of NMOS transistor is 40μm/0.25μm with 4 fingers on the layout. From the

measurement and calculation, it is found out that the TID effects increased the threshold voltage of NMOS transistors by about 0.2 V.

2.1.3. Gate leakage current on PMOS

The gate current leakage in MOS transistors is increased after irradiation. Gate leakage occurs when electrons tunnel through the thin gate oxide layer. The trapped charges in the oxide act as an intermediate state in the transfer of electrons through the oxide [3] [19]. The trap assisted tunneling is the reason for the increased gate current leakage after irradiation.

From the preliminary results, leakage current changed from below 100 nA before irradiation to 10 μA soon after irradiation but reduced back to below 800 nA after a 40 day annealing period.

2.1.4. Gate leakage current on NMOS

From preliminary results at SMU, leakage current increased from 30 nA to 3 μA after irradiation but after annealing it went back to 90 nA after 40 days.

According to the experimental results from SMU, the gate leakage current on PMOS is much greater than on NMOS after irradiation and a 40 day annealing period. In addition, the impact of back-channel radiation-induced leakage on PMOS transistors is more concerned. This may cause unpredictable behavior to the phase-locked loop.

2.1.5. Annealing

A radiated device can recover from the effects of radiation by annealing. A fast PMOS leakage current anneals in 10 days at room temperature. And slow anneals is on

going after 40 days. PMOS still has more of leakage current after a 40 day annealing cycle.

2.2 Single Event Effects

Single Event Effects (SEEs) are caused by a single, energetic particle, and can take on many forms, striking out a semiconductor device. The particle transfers the energy to the device material when it transverses through the device. The possibility of single-event upsets was first postulated by Wallmark and Marcus in 1962. Single Event Upsets (SEUs) are soft errors, and non-destructive. They normally appear as transient pulses in logic or support circuitry, or as bitflips in memory cells or registers. Several types of hard errors, potentially destructive, can appear. Single Event Latchup (SEL) results in a high operating current above device specifications, and must be cleared by a power reset. Other hard errors include Burnout of power MOSFETS, Gate Rupture, frozen bits, and noise in CCDs.

Single event phenomena can be classified into three effects (in order of permanency):

a) Single event upset (soft error)
b) Single event latchup (soft or hard error)
c) Single event burnout (hard failure)

SEE tests will be carried out this year. The SEE cross section has been measured with SOS 0.5 micron feature size. It has been found to be much less than the bulk CMOS SEE cross section.

2.3 Silicon on Sapphire

The first test chip from SMU is designed to evaluate the radiation hardness. It was fabricated by Peregrine Semiconductor with a 0.25 micron SOS process. This process has been commercially available since 2005. SMU decided to use this technology in the Link-On-Chip (LOC) ASIC design.

Silicon On Sapphire (SOS) is a hetero-epitaxial process for integrated circuit manufacturing that consists of a thin layer (typically thinner than 0.6 micrometres) of silicon grown on a sapphire (Al2O3) wafer. SOS is part of the Silicon on Insulator (SOI) family of CMOS technologies. Figure 2.1 shows the Silicon-On-Sapphire (SOS) structure in a CMOS technology. SOS is primarily used in aerospace and military applications because of its inherent resistance to radiation. The advantage of sapphire is that it is an excellent electrical insulator, preventing stray currents caused by radiation from spreading to nearby circuit elements. SOS has seen little commercial use to date because of difficulties in fabricating the very small transistors used in modern high-density applications.

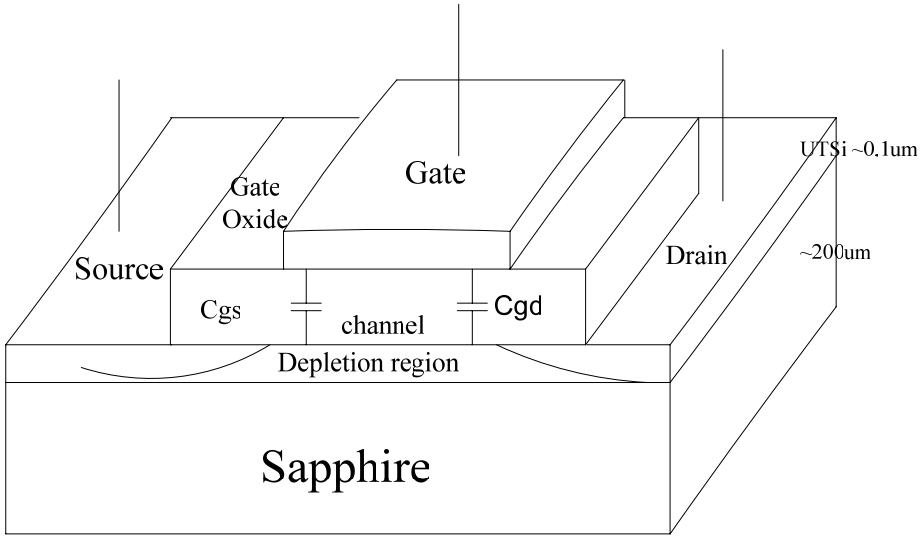


Figure 2.1 UTSi Silicon-on-Sapphire process technologies

Peregrine semiconductor has announced a 0.25 μm UltraCMOS Silicon-On-Sapphire (SOS) process in Aug 2004. The two new single poly, triple metal processes, designated as GA and GC, complement the existing 0.50 μm FA and FC processes and will push the transistor performance beyond the 100 GHz maximum clock frequency. While the GA is aimed at analog/digital circuits, the GC with low-loss high Q passives (L and C) capability is tailored for RF and mixed-signal designs. SMU selected GC process from Peregrine semiconductor in this Link-On-Chip (LOC) ASIC design because the low electron mobility at the Si-Sapphire interface causes the reduction of the back-channel leakage current in NMOS device. Additionally, the high Q capability on inductors and capacitors is a beneficial consequence for the LC-VCO design.

CHAPTER 3

PHASE LOCKED LOOP

3.1 Introduction

A Phase Locked Loop (PLL) is a closed-loop feedback control system that generates a signal in relation to the frequency and phase of an input ("reference") signal. The output of phase-locked loop circuit compares with both frequency and phase of the input reference signals, automatically raising or lowering the frequency in a controlled oscillator until the output signal is matched to the reference in both frequency and phase. Both analog and digital PLL circuits include three fundamental elements: A phase detector, a variable oscillator, and a feedback path. The feedback path is often a frequency divider. It divides the higher output frequency by a multiplication factor N to the reference frequency.

3.2 General Considerations

3.2.1. Phase Noise

In an oscillator, phase noise is random fluctuations in the phase of a wave caused by time domain instabilities. The noise source may be internal or external to the oscillator, and noise can influence the output signal frequency and amplitude. Phase noise is usually characterized in the frequency domain. Figure 3.1 shows the ideal oscillator with an ideal sinusoidal output at carrier frequency (ω_c). However in the real

world, oscillators exhibit random fluctuations with noise spreading around both sides of the carrier signal.

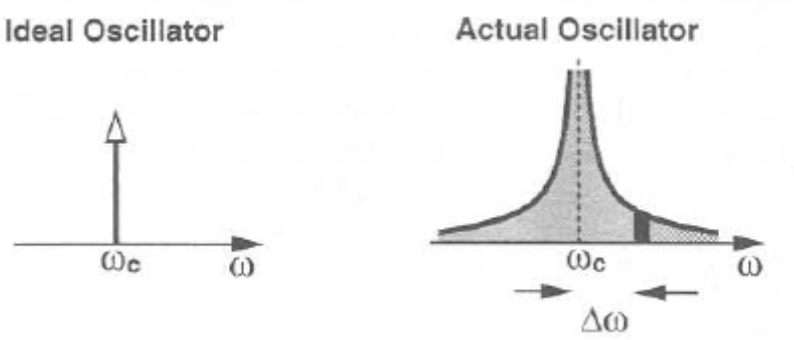


Figure 3.1 Output spectrum of ideal and actual oscillators. [15]

To calculate the quantity of the phase noise, it is needed to consider a unit bandwidth at an offset frequency ($\Delta\omega$) from the carrier frequency (ω_c), then within this bandwidth, noise power divided by carrier power is the phase noise.

Each of the elements in the PLL contributes noise to the overall phase noise on the output. The biggest noise contributor in the PLL is the oscillator. In the Cadence Spectre simulator, it can only simulate the oscillator phase noise. So we attempted to minimize overall PLL noise by reducing oscillator phase noise as much as possible.

3.2.2. Reference Spurs

The input reference frequency modulates the voltage control oscillator (VCO), and generates sidebands around the carrier frequency. In the ideal case, the UP and DOWN signals from the phase frequency detector to the charge pump would have identical and opposite outputs. However, in the real world, because of mismatch shapes on both pulses, these spurs will be increased by mismatched up and down currents from

the charge pump, charge-pump leakage, and inadequate decoupling of supplies. The spurious tones will get mixed down on top of the desired signal and reduce receiver sensitivity.

3.2.3. Locking Time

The lock time of a PLL is the period of time it takes to jump from one specified frequency to another specified frequency within a given frequency tolerance. The locking time is sometimes called the settling time. In the PLL, one can detect settling time by the oscillator's control voltage. When the control voltage settles to steady state, it means that the PLL is fully locked. A fast locking phase-locked loop is desired.

3.2.4. Chip Size

Smaller chip sizes are desired to reduce production cost. A 3 x 3 mm^2 die will be used in this chip to conserve space for other circuits.

3.3 PLL Architecture

3.3.1. Generic phase-locked loop

Typical PLLs consist of a voltage controlled oscillator (VCO), frequency divider, phase/frequency detector (PFD), charge pump (CP), and loop filter (LP). Figure 3.2 illustrates all building blocks in a PLL.

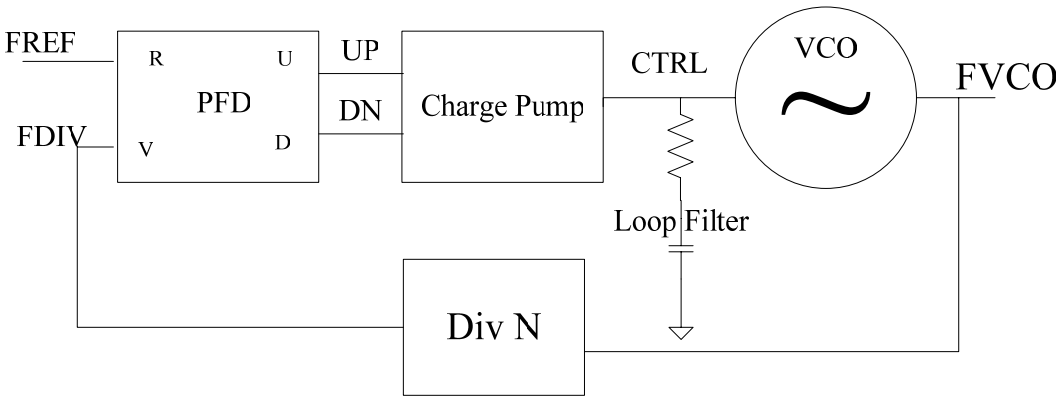


Figure 3.2 Typical Phase-Locked Loop Architecture

The PLL operates as follows. The PFD generates UP and DOWN pulses to the charge pump. If the phase from the feedback clocks, sometimes called divided clocks, falls behind that of the reference clock, the PFD causes the charge pump to change the control voltage so that the frequency of the oscillator speeds up. Alternatively, if the phase of the feedback clocks leads the reference, the phase detector causes the charge pump to change the control voltage to slow down the oscillator. The phase difference is converted to a current in the charge pump. The loop filter refines this current to a control voltage that controls the frequency of the VCO. The divider divides the VCO frequency down to the reference clocks with a constant ratio of frequency division, then the feedback loop around the PLL ensures the reference and divided clocks are in the same phase.

It is imperative to understand the behavior of each building block and the overall closed-loop behavior in the PLL. The following sections focus on Charge Pump PLL (CP-PLL). Because the CP-PLL is the most popular type of PLL technique in current use, it is adopted that technique in this research.

3.3.2. Phase/Frequency Detector

The PFD detects both phase and frequency difference of the divided feedback signal to that of the reference signal. Figure 3.3 illustrates the typical PFD operation. When the input frequency A is leading another input frequency B, the output signal Q_A generates the positive pulse, while Q_B remains at lower level. Otherwise, when the input frequency A is lagging another input frequency B, the output signal Q_B generates the positive pulse, while Q_A remains at lower level. When the frequencies of both input A and B are equal, the circuit generates pulses equal to the phase difference between the two inputs at both Q_A and Q_B. Hence, the outputs Q_A and Q_B are generally called the "UP" and "DOWN" signals. Figure 3.4 (a) shows the PFD state machine diagram.

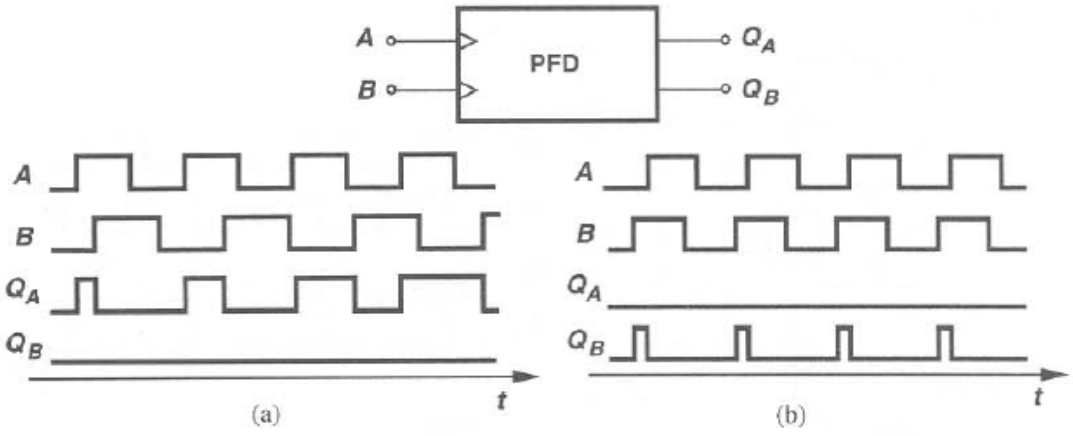
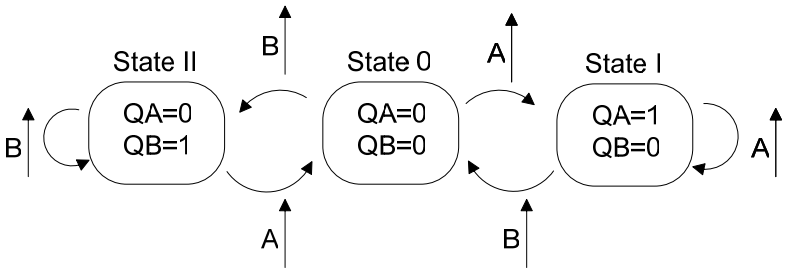
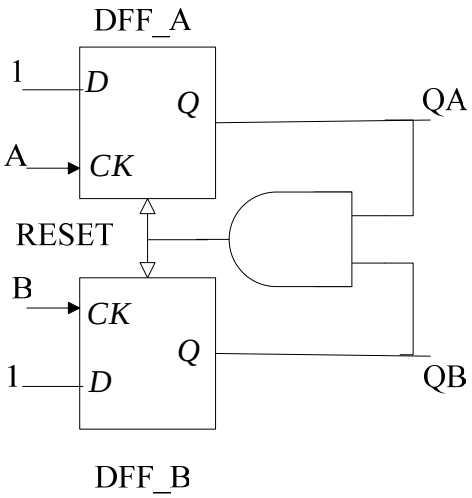


Figure 3.3 Phase/Frequency Detector (PFD) response (a) A leading B (b) A lagging B [15]

A PFD uses a simple state machine to determine which of the two signals has a zero-crossing earlier or more often. Figure 3.4(b) illustrates the generic Phase/Frequency Detector.



(a)



(b)

Figure 3.4 (a) Phase/Frequency Detector (PFD) state machine. (b) Phase/Frequency Detector (PFD) implementation

3.3.3. Charge Pump and Loop Filter

The charge pump output stage of the PFD is shown in Figure 3.5. The charge pump output supplies current to the loop filter that generates control voltage for the frequency operation of the VCO.

The UP signal is high when the input reference signal is operating at a higher frequency than the feedback signal. The charge pump forces current into the loop filter and causes the VCO control voltage to increase the VCO frequency and causes the feedback frequency to move towards the input reference signal.

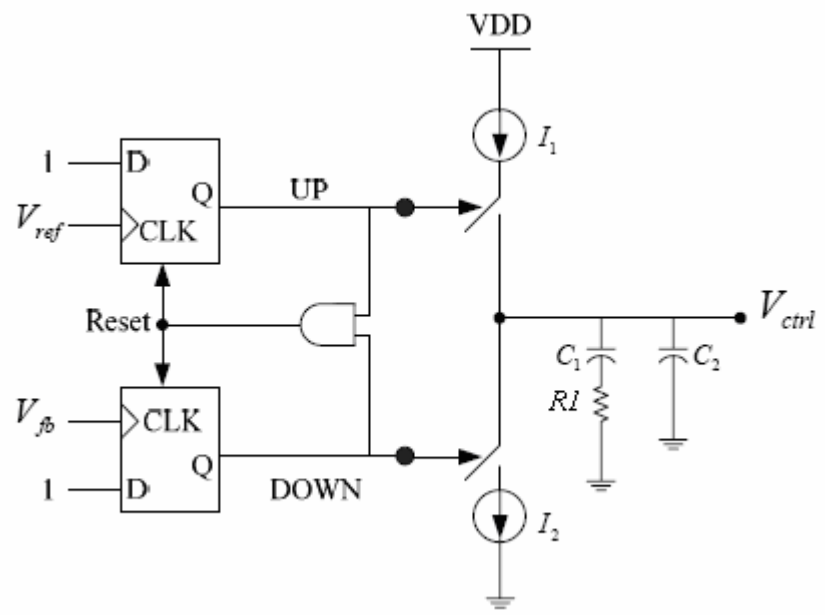


Figure 3.5 PFD with charge pump

Likewise, the DOWN signal is high when the input reference signal is operating at a lower frequency than the feedback signal. The charge pump sinks current out of the loop filter and causes the VCO control voltage to decrease. Then it decreases VCO frequency and brings the feedback frequency to match with the input reference signal.

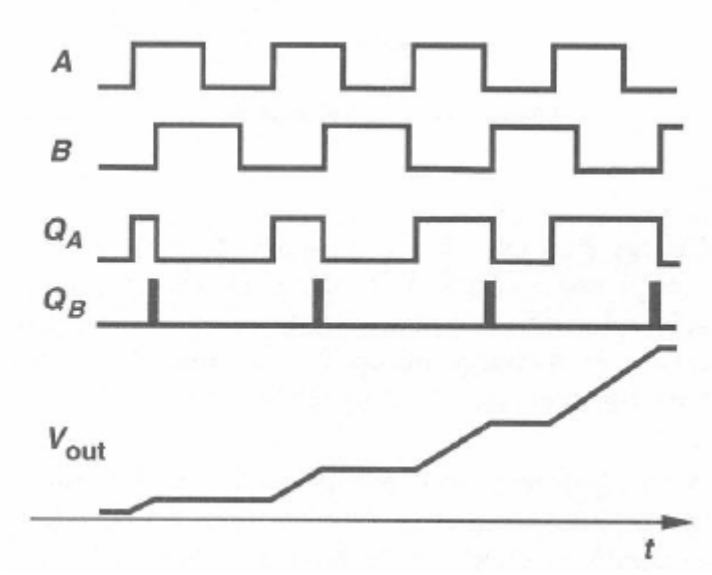


Figure 3.6 PFD with charge pump timing diagram [15]

The interaction between the PFD, charge pump, and loop filter is shown in Figure 3.6. Here the UP signal is high and forces the current into the loop filter. Hence, the VCO control voltage Vout is rising.

3.3.4. Voltage Controlled Oscillator (VCO)

The frequency of most PLLs must be adjustable. The VCO is a circuit which can tune the oscillator output frequency from the control voltage. The linear function of the frequency vs. voltage is shown below.

$$\omega_{out} = \omega_o + K_{VCO} V_{CTRL}$$

Where ω_o is the free running frequency and K_{VCO} is the gain of the VCO, expressed in rad/s-V. The ω_{out} in the linear function indicates that, for the practical

range of V_{CTRL} , ω_o may not approach zero. In other words, V_{CTRL} creates a change around ω_o . Figure 3.7 shows the VCO transfer characteristic.

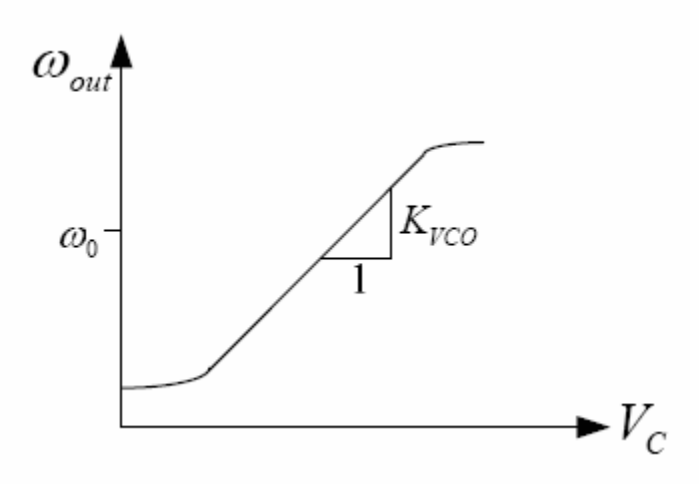


Figure 3.7 VCO transfer characteristic

There are two types of VCOs that one may choose to design.

1) waveform oscillators

2) resonant oscillators

Waveform oscillators have two topologies:

1) ring oscillator topology

2) relaxation oscillator (which has poor phase noise performance)

Resonant oscillators usually have two topologies:

1) LC tank oscillator topology

2) crystal oscillator (which is neither integrated nor tunable)

Ideally a VCO topology would be able to meet all of the specifications such as

a) low noise

b) low power

c) integrated

d) wide tuning range

e) small die area occupancy

f) high frequency (GHz)

g) low phase noise

The following table shows advantages and disadvantages of the ring oscillator VCO or LC tank VCO topologies.

Table 3.1 Ring Oscillator VCO vs. LC Tank VCO

	Ring Oscillator VCO	LC Tank VCO
Advantages	1) highly integrated in VLSI 2) low power 3) small die area occupancy 4) wide tuning range	Excellent phase noise and jitter performance at high frequency. Better radiation resistant.
Disadvantages	As frequency increases, performance degrades because phase noise or jitter increases.	1) Inductor and varactor (variable capacitor) have large area in the die. 2) high power consumption 3) small tuning range

The ring oscillator oscillation frequency is given by $f_{osc} = \frac{1}{2 \cdot n \cdot T_{delay}}$ and LC oscillator oscillation frequency is given by $f_{osc} = \frac{1}{2\pi\sqrt{LC}}$.

3.3.5. Frequency Divider

Most PLLs also include a divider between the oscillator and the feedback input to the PFD to produce a high frequency output signal. A programmable divider is particularly useful in radio transmitter applications. Frequency dividers are also called prescalers. The three most crucial performance factors for frequency dividers are speed, power dissipation, and phase noise.

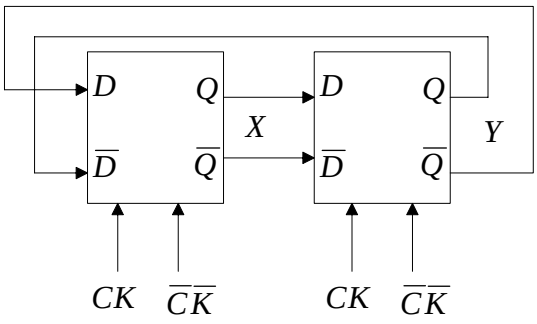


Figure 3.8 Frequency divider Divide-by-two circuit

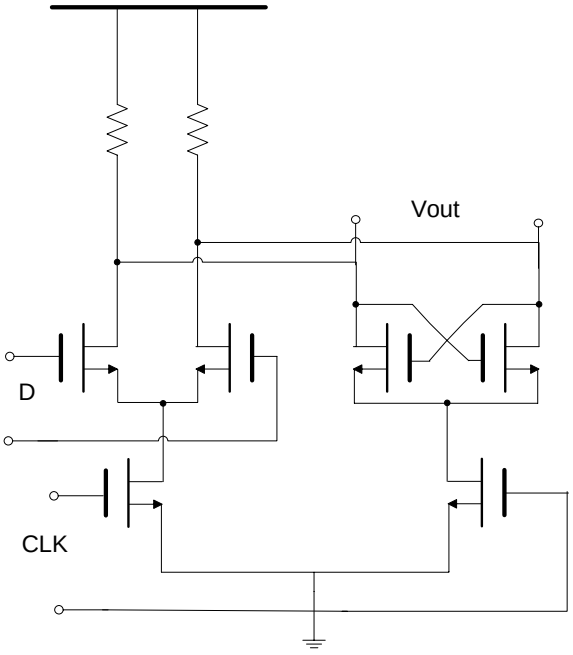


Figure 3.9 Frequency divider implementation for each latch

Figure 3.8 illustrates two latches in a negative feedback loop that can be realized as a divide-by-two divider. Figure 3.9 shows the differential circuit implementation for each latch.

There are two types of frequency dividers which have been studied in this project. One uses true single-phase clocked (TSPC) logic, and the other uses current mode logic (CML). The TSPC frequency divider operates at lower frequencies, typically below 4 GHz. The CML frequency divider can work up to 8 GHz, but these dividers have high power consumption and are complex to design.

3.4 PLL Close Loop Transfer Function

The charge pump PLL (CP-PLL) with frequency multiplication model [13] [14] is illustrated below in Figure 3.10.

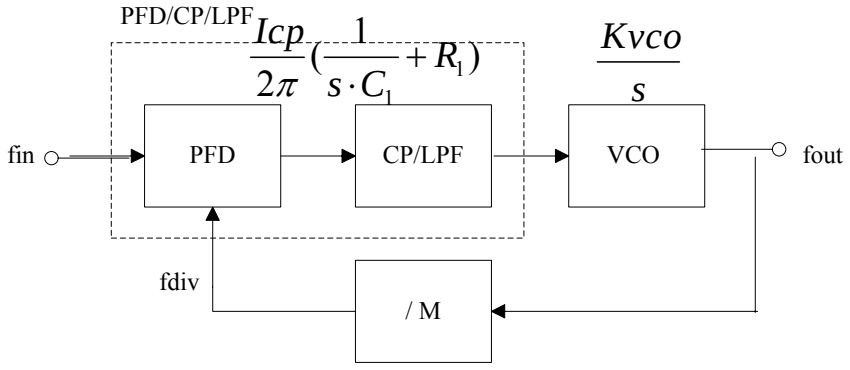


Figure 3.10 CP-PLL with frequency multiplication model

K_{PFD} is the gain of PFD/CP/LPF combination blocks. Icp is the charge pump current. R_1 and C_1 are in the loop filter. Its transfer function can be expressed as $\frac{Icp}{2\pi}(\frac{1}{s \cdot C_1} + R_1)$. The forward gain (open loop) transfer function is

$$G_1(s) = \frac{Icp}{2\pi}(\frac{1}{s \cdot C_1} + R_1)\frac{Kvco}{s} \tag{3.1}$$

The loop gain is

$$G_2(s) = \frac{Icp}{2\pi M}(\frac{1}{s \cdot C_1} + R_1)\frac{Kvco}{s} \tag{3.2}$$

The transfer function of the PLL can be written as

$$H(s) = \frac{G_1(s)}{1 + G_2(s)} \tag{3.3}$$

Now substitute the forward gain and the loop gain into the PLL transfer function

$$\begin{aligned} H(s) = \frac{G_1(s)}{1 + G_2(s)} &= \frac{\frac{Icp}{2\pi}(\frac{1}{s \cdot C_1} + R_1)\frac{Kvco}{s}}{1 + \frac{Icp}{2\pi M}(\frac{1}{s \cdot C_1} + R_1)\frac{Kvco}{s}} \\ &= \frac{\frac{Icp}{2\pi}\frac{Kvco}{s}(\frac{1 + s \cdot C_1 R_1}{s \cdot C_1})}{1 + \frac{Icp}{2\pi M}\frac{Kvco}{s}(\frac{1 + s \cdot C_1 R_1}{s \cdot C_1})} \\ &= \frac{\frac{Icp}{2\pi}\frac{Kvco}{s}(\frac{1 + s \cdot C_1 R_1}{s \cdot C_1})}{\frac{2\pi M \cdot s^2 \cdot C_1}{2\pi M \cdot s^2 \cdot C_1} + \frac{Icp}{2\pi M}\frac{Kvco}{s}(\frac{1 + s \cdot C_1 R_1}{s \cdot C_1})} \\ &= \frac{\frac{Icp}{2\pi}\frac{Kvco}{C_1}(s \cdot C_1 R_1 + 1)}{s^2 + s\frac{IcpKvcoR_1}{2\pi M} + \frac{IcpKvco}{2\pi M C_1}} \end{aligned} \tag{3.4}$$

The standard second-order transfer function can be rewritten as

$$H(s) = \frac{\omega_n^{\,2}}{s^2 + 2s\zeta\omega_n + \omega_n^{\,2}} \frac{M}{1} \tag{3.5}$$

Where the neutral frequency ω_n of the system is

$$\omega_n = \sqrt{\frac{K_{VCO} \cdot I_{CP}}{2\pi \cdot M \cdot C_1}} \text{ in Hz} \tag{3.6}$$

And the damping factor ζ is

$$\zeta = \frac{R_1}{2}\sqrt{\frac{K_{VCO} \cdot I_{CP} \cdot C_1}{2\pi \cdot M}} = \frac{R_1 C_1 \omega_n}{2} \tag{3.7}$$

The close-loop system contains a zero at $s_z = -1/(R_1 C_1)$. A PLL may be stable or unstable depending on the damping factor.

CHAPTER 4

SPIRAL INDUCTOR AND VARACTOR DESIGN

This chapter describes the design for the spiral inductor and varactor used in the LC-tank VCO. The success of a LC-tank Voltage Controlled Oscillator (VCO) design is dependent on the design of the inductor and the varactor, which are critical to not only the LC-VCO performance but overall PLL performance.

4.1 Introduction

Inductor design critically influences the phase noise performance of an LC-tank VCO. The most important inductor performance parameters are the quality factor (Q) and resonant frequency. Q is particularly low in CMOS therefore the inductor design is critical for this project. A large inductor consumes a large chip area. The area consumed influences these factors as well as material costs. The inductor value and quality factor vary at different frequencies, and the peak quality factor value will only occur at a specific frequency. Circuit layout and the IC technology influence the inductor value and qualify factor.

The quality factor (Q) is defined as:

$$Q = 2\pi \frac{\left|Peak\ Magnetic\ Energy - Peak\ Electric\ Energy\right|}{Energy\ Loss\ in\ One\ Oscillation\ Cycle}$$

$$= 2\pi \frac{\left|Peak\ Energy\ Stored\ \right|}{Energy\ Loss\ Per\ Cycle}$$

An inductor's Q most often given as the simple ratio:

$$Q = \frac{\mathrm{Im}(Z)}{\mathrm{Re}(Z)} \tag{4.1}$$

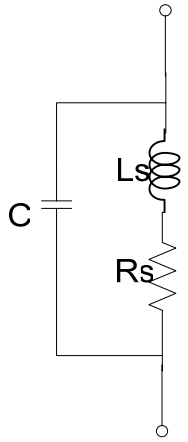


Figure 4.1 Inductor with loss modeled by a series resistor

Figure 4.1 shows a realistic LC tank model with loss modeled by a series resistor [17]. The inductor's Q is given by

$$Q = \frac{L_s \omega}{R_s} \tag{4.2}$$

4.2 Design Consideration

Many tools can simulate the quality factor, frequency, and the inductance value of the inductor such as ASITIC, High Frequency Structure Simulator (HFSS), ADS Momentum, Fast-Henry, and Spiral Inductor design in Cadence.

In this thesis, a simplified frequency independent four-element model [20] is used to simulate and calculate our quality factor and inductance value.

Peregrine also provided their design kit manual so our design could incorporate process parameters for their unique Silicon On Sapphire (SOS) technology which has a

different cross-section structure than other processes such as TSMC 0.25μm and IBM CMOS RF technology (CMOS 6RF).

4.3 Inductor Design Implementation

4.3.1 Process parameters from Peregrine Semiconductor

The design began with process parameters from Peregrine Semiconductor. There are three metal layers in this GC process: Metal 1, Metal 2, and Metal 3 which is usually called Metal Thick or Top Metal. Other fabrication processes may go up to 7 metal layers. The top metal layer usually has a better quality factor. Figure 4.2 illustrates a Preliminary GC process back-end stack cross section diagram from Peregrine Semiconductor.

Each layer includes the following key parameters that will influence inductor design.

- Thickness
- Eps : Relative Permittivity
- Bulk Conductivity
- Relative dielectric constant

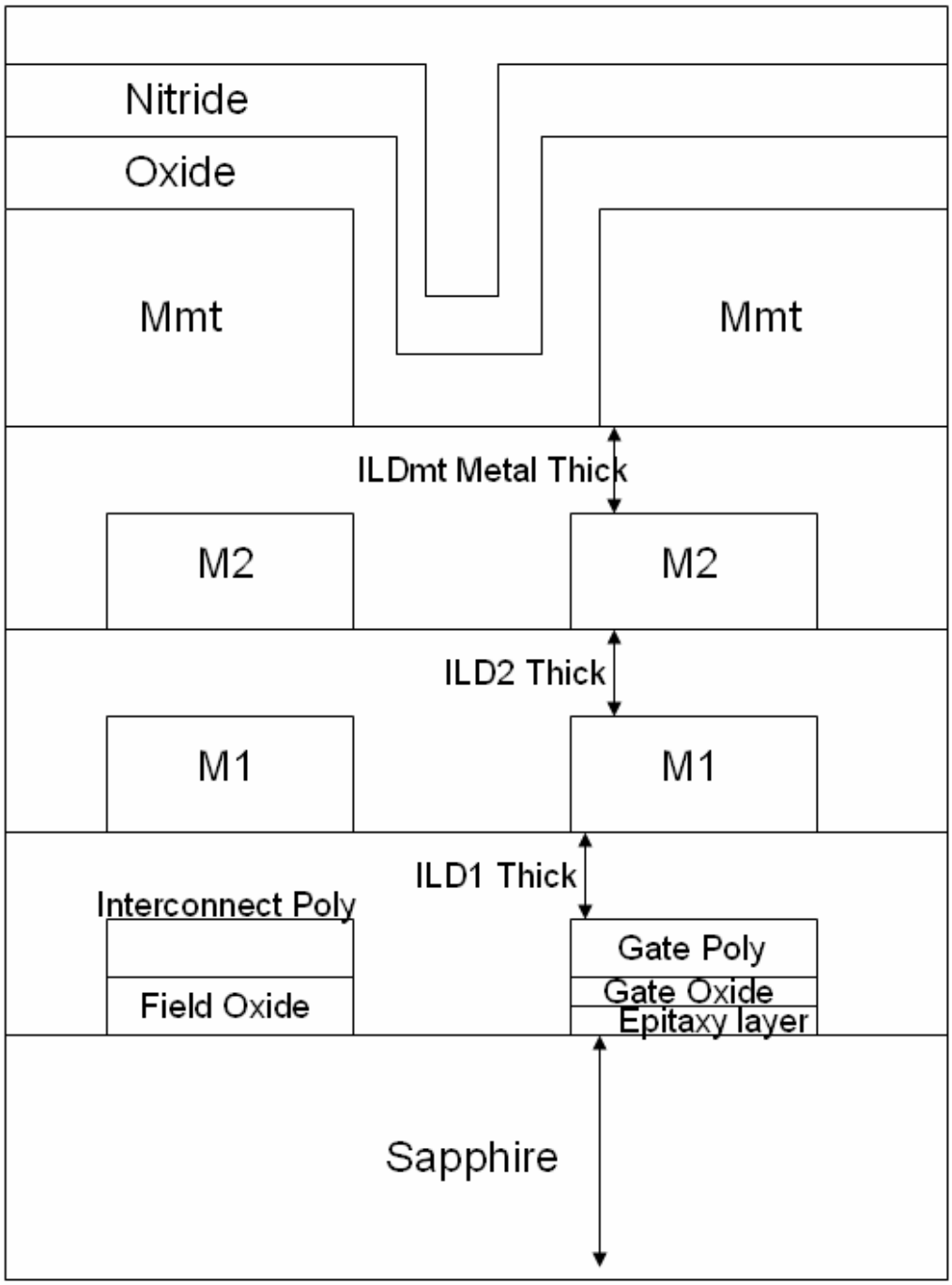


Figure 4.2 Peregrine GC Process Back-End Stack Cross Section

Table 4.1 is the description of each layer from top to bottom view.

Table 4.1 Peregrine GC process layer

Nitride Layer	A nitride (compound) is a compound that has nitrogen with more electropositive elements
Oxide Layer	An oxide is a chemical compound of oxygen with other chemical elements
Mmt (Metal Thick)	Metal 3, Top Metal, Metal Thick
ILDmt	Interlevel dielectric layer between M2 and Mmt
M2	Metal 2
ILD2	Interlevel dielectric layer between M1 and M2
M1	Metal 1
ILD1	Interlevel dielectric layer between Poly and M1
Interconnect Poly	Interconnect polysilicon
Field Oxide (FOX)	relatively thick oxide formed to passivate and protect semiconductor surface outside of active device area
Gate Poly	a gate contact in MOS/CMOS devices
Gate Oxide	very thin layer of oxide sandwiched between semiconductor and gate contact in MOS devices
Epitaxy	a kind of interface between a thin film and a substrate
Sapphire	single-crystal Al2O3

4.3.2 Spiral Inductor Model in SOS

To explain the method used to derive the proposed inductor, it might be helpful to first consider how this task would have been approached with the enhanced resources and intellectual property available to industry, resources which significantly exceeded that available to the academic environment. It was shown from "modeling spiral inductors in SOS processes"[20] that SOS has very high resistivity or insulating substrates. However, the model breaks down since inductor quality factor Q is then determined predominantly by series trace resistance.

There are many specifications from the Peregrine library, which usually lists large, medium, and small layouts. The inductor design started with a 5.1 nH design that had peak quality factors at 3.7 GHz, very close to the desired center frequency of 3.6 GHz. The library only provided a small layout for this device, which appealed to lower costs. So L_S, R_S, C_P, R_P, and k parameters were replicated into a Four Element Model [20], and performance was simulated over the scope of about 1-7 GHz, a bandwidth somewhat larger than our intended tuning range in hopes of compensating for the unknown degree that radiation may affect future VCO performance.

Figure 4.3 and 4.4 shows the standard small spiral inductor model and equivalent circuit model used for modeling SOS library inductors. This is known as a four element model in [16] [20].

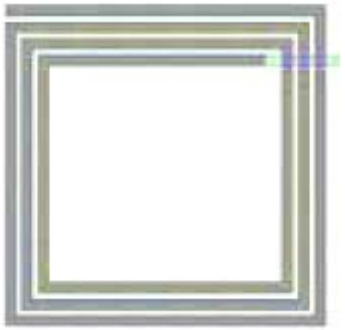


Figure 4.3 Standard small spiral inductor model

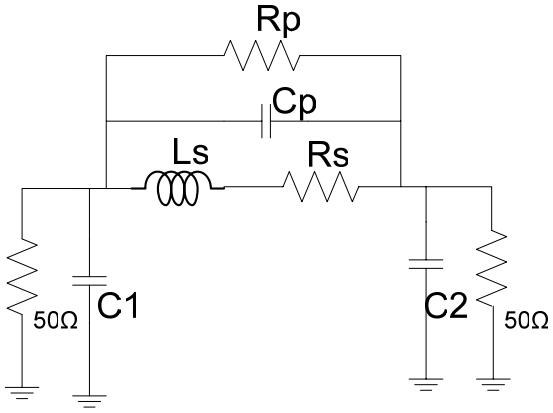


Figure 4.4 Equivalent circuit model used for modeling SOS library inductors

4.3.3 Spiral Inductor in SOS process

An improved equivalent circuit topology shown in Figure 4.4 is used for the GC inductor library. The intrinsic model parameters L_S, R_S, C_P, R_P, and k are listed in the design manual for all inductors. The parasitic shunt capacitors to ground, C1 and C2, are included in the model to represent the actual return path used in the measurements. They are for user reference only.

The four-element model is easier to work with in manual analysis of RF circuits. For this model, the impedance of the R_S, Ls components in parallel with R_P is

$$Z_{RsLsRp} = \frac{(Rs + j\omega Ls)Rp}{(Rs + j\omega Ls) + Rp} = \frac{RsRp(Rs + Rp) + (\omega Ls)^2 Rp}{(Rs + Rp)^2 + (\omega Ls)^2} + j\omega Ls \frac{Rp^2}{(Rs + Rp)^2 + (\omega Ls)^2} \quad (4.3)$$

This can be simplified by noting that for high Q inductors

$$Z_{RsLsRp} \approx Rs + \frac{(\omega Ls)^2}{Rp} + j\omega Ls \quad (4.4)$$

Z_{RsLsRp} is calculated from the intrinsic model parameters provided by Peregrine Semiconductor, and the quality factor (Q) is

$$Q_{11} = \frac{\mathrm{Im}(Z_{11})}{\mathrm{Re}(Z_{11})} \quad (4.5)$$

The inductance value can also be calculated from the inductor equation as

$$L_{11} = \frac{-1}{2\pi \cdot f \cdot \mathrm{Im}(Z_{11})} \quad (4.6)$$

From the above equations, the inductor Q and L are simulated over a range of frequencies. Resulting plots are given in the next section.

4.4 Simulation Result from Four Element Model

The simulation data given in Figure 4.5 shows that Q=18 at 3.6 GHz. The measured inductance value is 5.1 nH at the frequency of 3.6 GHz. Figure 4.6 shows the inductance value vs. working frequency in the spiral inductor simulation. This simulation shows a reasonably constant inductance value for the frequency from 3 GHz to 5 GHz and the quality factor is above 10 from 1 GHz to 6 GHz. Therefore this 5.1 nH inductor is suitable for this very wide tuning range LC VCO design.

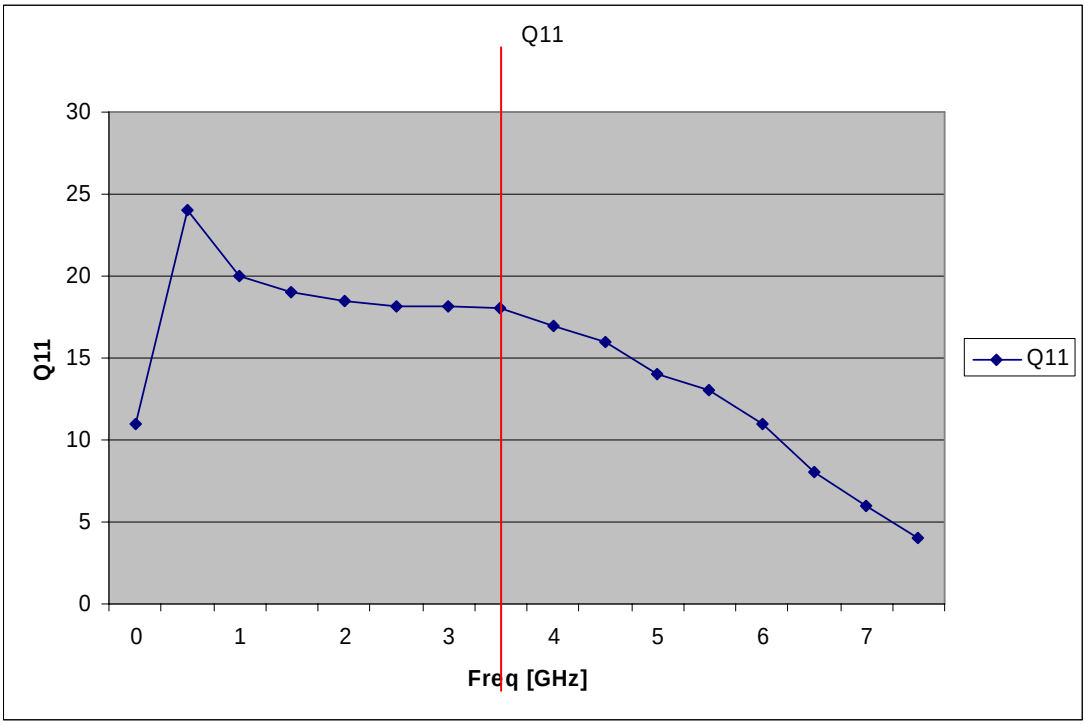


Figure 4.5 Quality factor (Q) value in Spiral Inductor

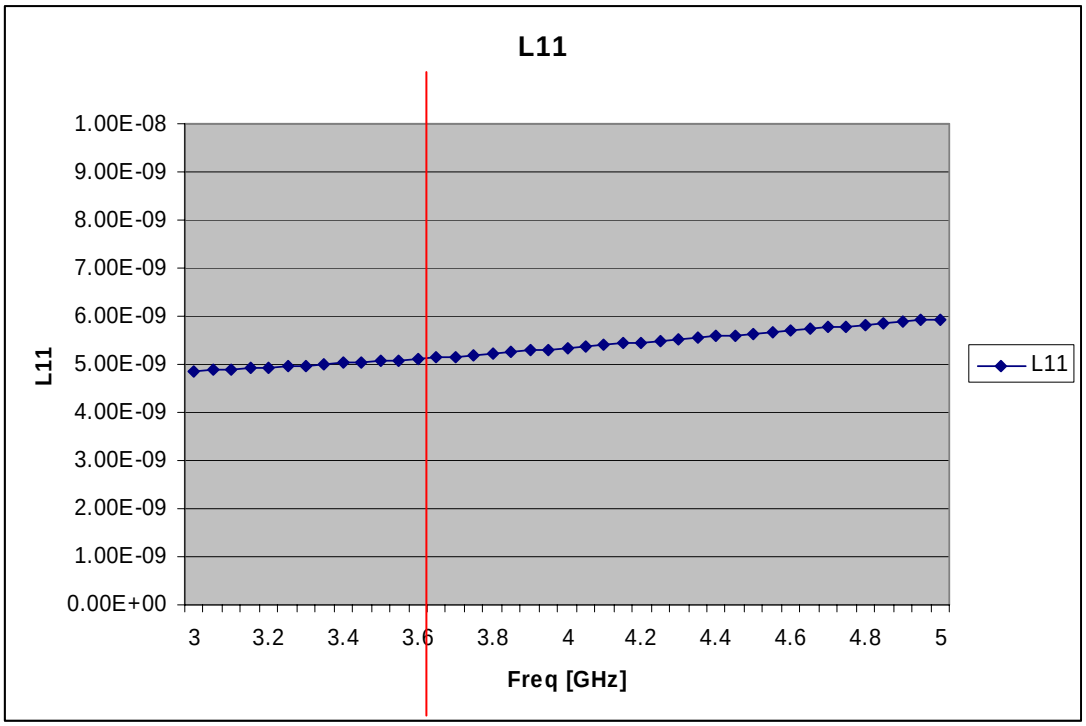


Figure 4.6 Inductance (L) value in Spiral Inductor

4.5 Layout on Virtuoso

Figure 4.7 shows the layout of the spiral inductor. The inductance value is 5.1 nH. The inductor layout dimension is 250µm by 250µm in Virtuoso. It is designed with 5.25 turns, width of 12 and space of 6 in the PSC inductor library.

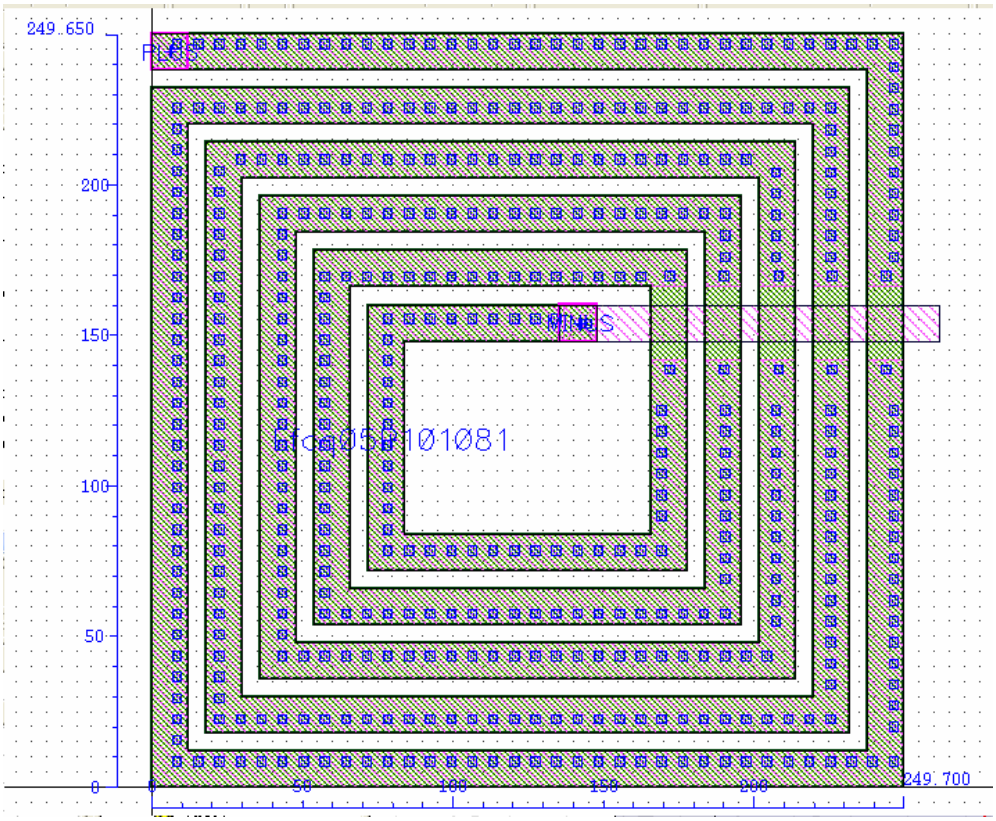


Figure 4.7 Spiral Inductor layout

4.6 Varactor Design Implementation

An accumulation mode or strong inversion mode varactor is designed to achieve a wide tuning range, because depletion/inversion varactors experience parasitic source-drain capacitance. The quality factor of an accumulation mode varactor is also better than a depletion mode varactor because the intrinsically higher electron mobility causes

a smaller resistance in series with the accumulation layer. Figure 4.8 shows the varactor simulation setup and Figure 4.9 shows the simulated C-V curve of the MOSFET varactor.

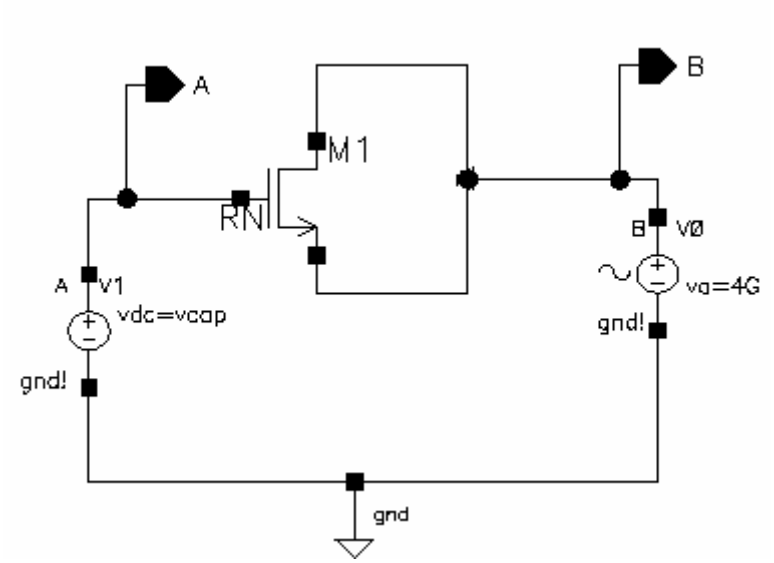


Figure 4.8 MOSFET varactor simulation setup

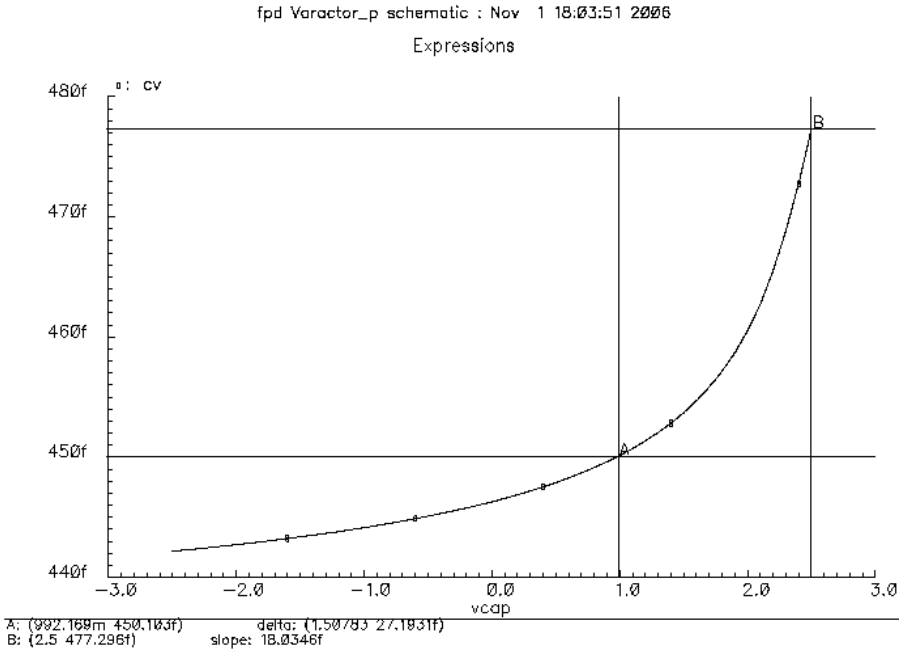


Figure 4.9 C-V curve of the MOSFET varactor

CHAPTER 5

RADIATION HARDENED PLL DESIGN

In this chapter, the circuit level implementation of individual blocks and phase locked loop are presented. The analysis, design, and radiation hardened considerations of LC voltage controlled oscillator, CML frequency divider, phase frequency detector, charge pump, and loop filter.

5.1 Proposed PLL architecture

The proposed phase locked loop (PLL) is similar to a generic PLL. The architecture of the PLL can be seen in Figure 5.1. The basic PLL building blocks are (a) LC voltage controlled oscillator (LC-VCO) (b) frequency divider (c) Phase/Frequency Detector (PFD) (d) Charge Pump (CP), and (e) Loop filter (LF). The design and implementation of the building blocks are explained in the following sections.

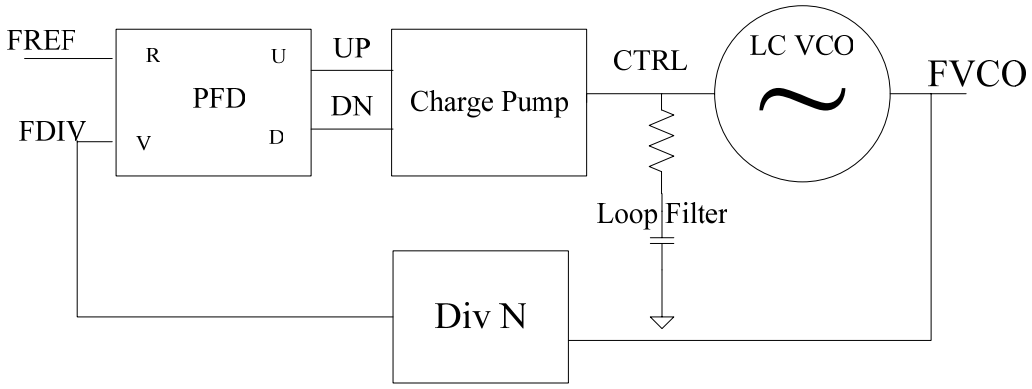


Figure 5.1 Proposed PLL architecture

5.2 Building Blocks of a PLL

5.2.1. LC Voltage Controlled Oscillator (LC-VCO)

Frequency tuning range and phase noise are the key performance parameters of a high frequency voltage controlled oscillator. Total dose radiation causes the tuning range of the VCOs to shift [2]. However, radiation causes LC VCOs to experience smaller tuning shifts than ring VCOs that have more transistors and parasitic capacitors [4] [12]. So far there is no LC PLL that can be locked after irradiation. There is a need to design a wide band and wide tuning range LC VCO in order to assure the PLL locks in a radiation environment.

There are many conventional LC VCOs available, but most of these designs fall short of requirements for the following reasons. Most of these LC VCOs use varactors to tune the output frequency. The maximum frequency tuning limit is narrow, around 1 GHz at f_o=6.25 GHz, which may degrade after irradiation. This may result in the PLL losing lock. Also, conventional LC VCOs use PMOS cross coupled techniques, but radiation cause PMOS to experience increased back channel leakage. Hence, varactors are not used and the use of PMOS is also minimized to reduce phase noise and increase the tuning range.

Figure 5.2 shows a cross-coupled VCO architecture with the loop gain for two identical LC VCO cores [5] [6], G1, G2 and coupling circuits m_1 and m_2. The output phasors are X and Y, and output frequency can be controlled by adjusting the coupling coefficient of m_1 and m_2. Outputs are coupled to inputs with the coupling coefficient m_1 and m_2.

In a steady state and VCOs synchronized to ω, VCO diagram has $(X+m_1Y)G_1(j\omega)=X$ and $(Y+m_2X)G_2(j\omega)=Y$. If VCOs are assumed to be identical ($G_1=G_2=G$, $m_1=-m_2=m$), then it gets $X=\pm jY$ and $(1 \pm jm)G(j\omega)=1$. The loop gain is $G(j\omega)=g_mZ(j\omega)$ and the impedance phase is $\phi[Z(j\omega)]= \pm \tan^{-1}(m)$. So the oscillation starts from $\phi[Z(j\omega_2)]= \tan^{-1}(m)$ to $\phi[Z(j\omega_1)]= -\tan^{-1}(m)$.

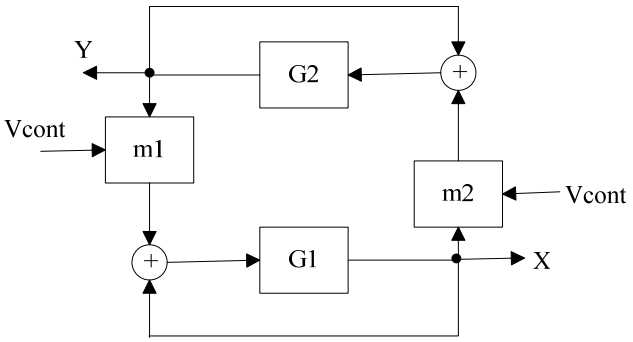


Figure 5.2 Block diagram of the cross-coupled VCO

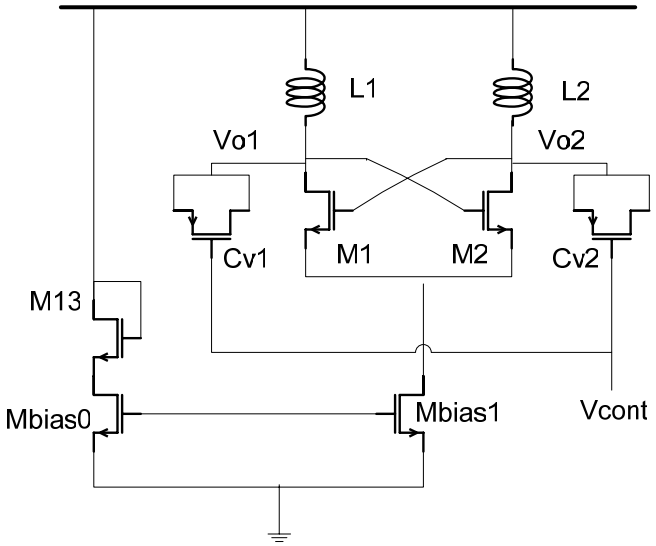


Figure 5.3 A conventional LC VCO tuned by varactors.

Both of the VCO cores G1 and G2 are designed as a conventional LC VCO in Figure 5.3. A pair of NMOS transistors perform negative g_m to replenish the loss in the

LC tank. Vcont controls the capacitance of the varactors Cv1 and Cv2 and thus the resonant frequency of the LC tank.

The proposed wideband CMOS cross-coupled LC voltage-controlled oscillator schematic is shown in Figure 5.4. The advantage of this LC VCO is the wide tuning range and use coupling coefficient technique instead of varactor design. Figure 5.2 shows the block diagram of this LC VCO schematic. The LC VCO is composed of two VCO cores, G1 and G2, and coupling circuits m_1 and m_2. G1 is made up of M0, M1, Cv0, Cv1, L0, L1, and M5. G2 is made up of M2, M3, Cv2, Cv3, L2, L3, and M6. m_1 contents M7, M8, and M11. m_2 contents M9, M10, and M12. The biasing circuit is M4, M17, and M18. Also a compensation circuit of M19, M20, R_{cap} is used.

Here is a brief description of the cross-coupled LC VCO operation. The coupling coefficient m is the ratio of two transconductances, $-g_{m7}/g_{m3}$. Figure 5.5 shows the magnitude and phase response of the LC resonator. The oscillation may start when $\phi[Z(jw)] = \pm\tan^{-1} m$ at ω_2 shown in Figure 5.5. However the |Z| is too small to maintain the oscillation when $\phi[Z(jw_2)] = \pm\tan^{-1} m$ (|G(jω)| > 1, Barkhausen Criteria). So the oscillation is sustainable only at ω_1 when $\phi[Z(jw_1)] = -\tan^{-1} m$. The precise resonant frequency of a parallel LC tank is $\omega_0 = \sqrt{\frac{1}{LC} - \frac{R^2}{L^2}}$. As a result, the oscillation frequency can be tuned from ω_0 to ω_1 by changing m with a control voltage ($\omega_0 < \omega < \omega_1$).

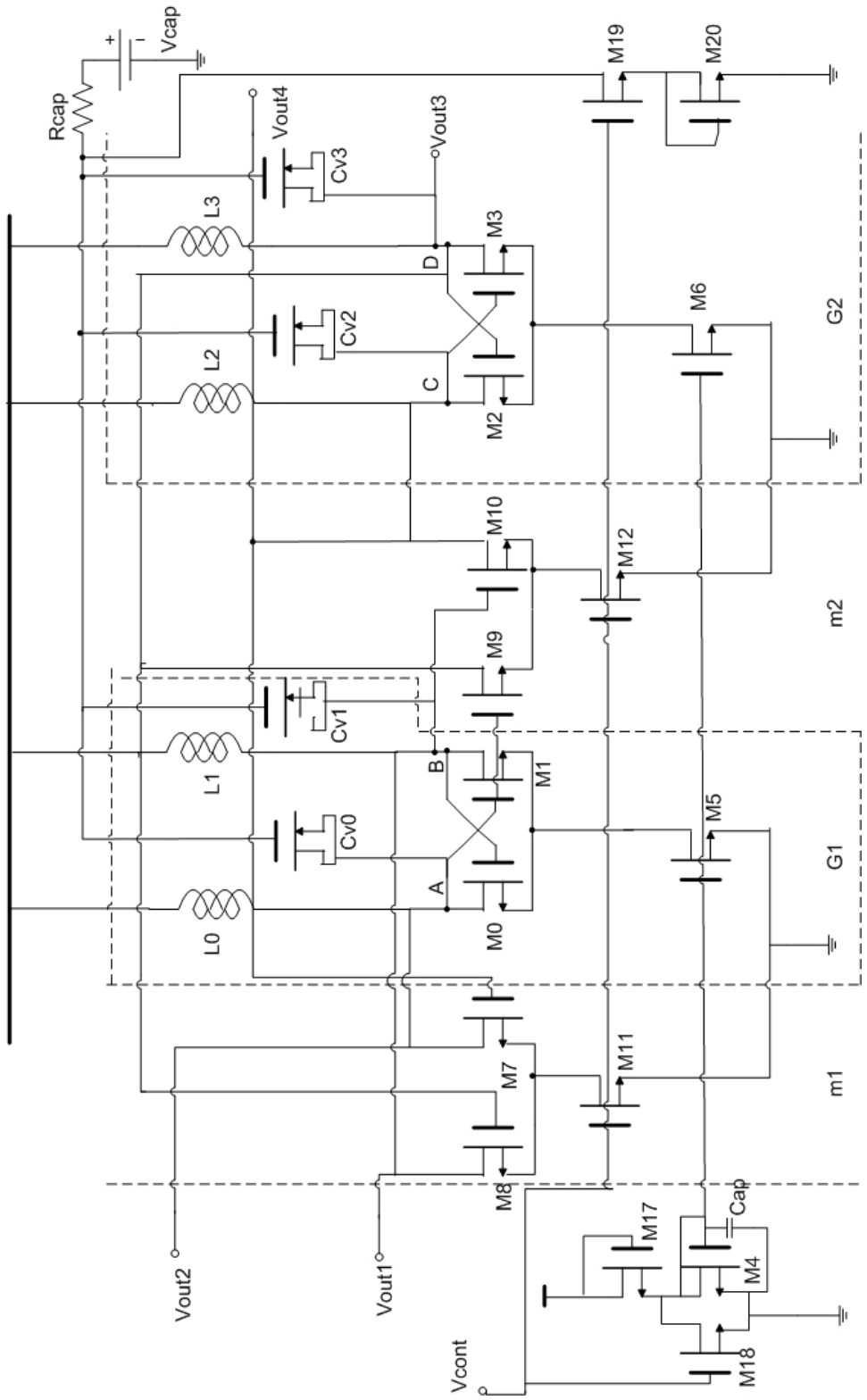


Figure 5.4 Schematic of coupling coefficient LC VCO with AC coupling [5]

If $\phi[Z(jw_2)]$ becomes high enough with higher impedance |Z|, it may start oscillation. So it will appear the multi-mode oscillation phenomenon on the output. $\phi[Z(jw_2)]$ is set by the tranconductance ratio *m* and will design to be much less than $\phi[Z(jw_1)]$ to generate the single tone oscillation. Additionally, |Z| is not a function of *m* and will not be controlled by the control voltage.

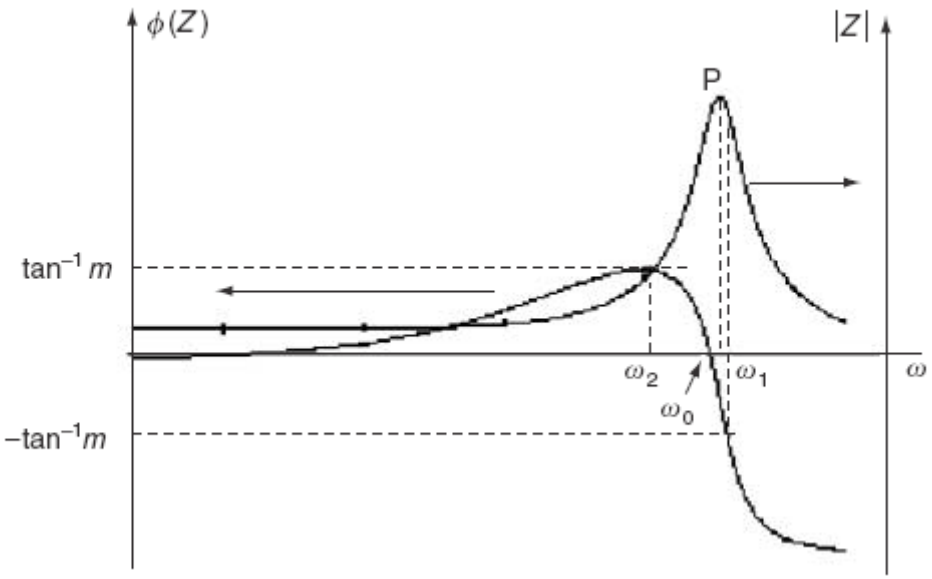


Figure 5.5 Magnitude and phase responses of the LC resonator. [5]

Now follows detailed an explanation and derivation of the coupling coefficient LC VCO.

Transistors M7-M12 form the coupling circuit and determine the coupling coefficient between the oscillator cores. v_A, v_B, v_C, and v_D are the AC output voltages on the VCO outputs A, B, C, and D. Also the "transconductance" g_m is expressed as:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu_n Cox \frac{W}{L}(V_{gs} - V_{th}) \tag{5.1}$$

or

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} = \frac{2I_D}{V_{gs} - V_{th}} \tag{5.2}$$

Thus, the drain-source current of M9 and M3 are given by

$$i_{ds9} = v_A g_{m9} \tag{5.3}$$

$$i_{ds3} = v_c g_{m3} \tag{5.4}$$

The drain-source current of M9 is injected into the VCO output D. The total current flow through the tank L3 and C3 at output D is given by

$$i_{\tan k3} = i_{ds3} + i_{ds9} = v_C g_{m3} + v_A g_{m9} \tag{5.5}$$

The total voltage at output D is

$$V_D = V_{dd} - I_{\tan k3} Z_3(j\omega) \tag{5.6}$$

where $Z_3(j\omega)$ is impedance of L_3 and C_{V3} tank. The AC signal at output D is

$$v_D = -I_{\tan k3} Z_3(j\omega) \tag{5.7}$$

Using $v_C = -v_D$, v_D, this can be expressed as

$$v_D = (v_D g_{m3} - v_A g_{m9}) Z_3(j\omega) \tag{5.8}$$

$$v_D = (v_D - g_{m9} / g_{m3} \cdot v_A) g_{m3} Z_3(j\omega) \tag{5.9}$$

or

$$v_D = (v_D + m2 \cdot v_A) G_2(j\omega) \tag{5.10}$$

where the coupling coefficient m2= $-g_{m9} / g_{m3}$ and $G_2(j\omega) = g_{m3} Z_3(j\omega)$

Using the same procedure, it is clear that $v_A = (v_A + g_{m7} / g_{m0} \cdot v_D) g_{m0} Z_0(j\omega)$ or $v_A = (v_A + m1 \cdot v_D) G_1(jw)$. The coupling coefficient m1 $= + g_{m7} / g_{m0}$.

If the circuit is symmetrical, both oscillators G1 and G2 are identical, $G_1(j\omega) = G_2(j\omega) = G(j\omega)$ and the coupling coefficients are the same (m_1=-m_2=m). Hence, $v_A{}^2 + v_D{}^2 = 0$ or $v_A = \pm j v_D$. Using the same process, $v_B = \pm j v_C$.

The new oscillation frequency ω can be found by substituting $v_A = \pm j v_D$ into $v_D = (v_D + m2 \cdot v_A) G_2(j\omega)$ as

$$1 = (1 + jm) G(j\omega) \tag{5.11}$$

where $G(jw) = g_m Z(j\omega)$ (5.12)

The oscillation may start when $\phi[Z(j\omega)] = \pm \tan^{-1} m$. (5.13)

This is satisfied with the result from the VCO diagram. And the impedance of the parallel LC tank is given by [5]

$$Z = \frac{L}{CR} \frac{1 - j\dfrac{R}{\omega L}}{1 + j\left(\dfrac{\omega L}{R} - \dfrac{1}{\omega CR}\right)} \tag{5.14}$$

At the resonant frequency, the phase of the impedance must be zero since

$$-\frac{R}{\omega_0 L} = \frac{\omega_0 L}{R} - \frac{1}{\omega_0 CR} \tag{5.15}$$

Thus,

$$\omega_0{}^2 L^2 C = L - CR^2 \tag{5.16}$$

$$\omega_0{}^2 = \frac{L - CR^2}{L^2 C} \tag{5.17}$$

The precise resonant frequency of the lossy parallel LC tank is

$$\omega_0 = \sqrt{\frac{L - CR^2}{L^2 C}} = \sqrt{\frac{1}{LC} - \frac{R^2}{L^2}} \tag{5.18}$$

A lossy LC resonator has a lower resonant frequency than the ideal resonator. The peak of its impedance magnitude is shifted away from the resonant frequency. The magnitude of the impedance in (5.14) is

$$\begin{aligned} |Z| &= \sqrt{\left(\frac{L}{CR} \frac{1 - j\frac{R}{\omega L}}{1 + j(\frac{\omega L}{R} - \frac{1}{\omega CR})} \right)^2} \\ &= \sqrt{\left(\left(\frac{L}{CR}\right)^2 \frac{\left(1 + \frac{R}{\omega L}\right)^2}{1 + (\frac{\omega L}{R} - \frac{1}{\omega CR})^2} \right)} \\ &= \sqrt{\frac{R^2 + \omega^2 L^2}{\left(1 - \omega^2 LC\right)^2 + (R\omega C)^2}} \end{aligned} \tag{5.19}$$

Hence, the maximum value of |Z| can be found at $\omega_0{}'$. It is higher than the resonant frequency of ω_0 as

$$\omega_0{}' = \frac{1}{LC} \sqrt{\sqrt{1 + \frac{2CR^2}{L}} - \frac{CR^2}{L}} \tag{5.20}$$

The coupling coefficient is $m = g_{m7}/g_{m0} = g_{m8}/g_{m1} = g_{m9}/g_{m3} = g_{m10}/g_{m2}$. In order to control the coupling coefficient value, one is to keep the transconductance of the amplifying transistors g_{m0}-g_{m3} constant, while varying the transconductance of the

coupling transistors g_{m7}-g_{m10}. When the transistor dimensions are determined, the oscillating frequency is a function of the drain-source current of M11, M12 divided by another drain-source current of M5, M6. [5]

The LC tank impedance increases with the resonant frequency. Accordingly, the oscillating magnitude increases with frequency even though the g_{m3} is unchanged. Figure 5.6 shows the output amplitude variation vs. frequency at the LC VCO output.

The power dissipation will increase only if g_{m7}-g_{m10} changes. The technique used to reduce power dissipation is to increase the control voltage, and as V_{gs18} increases, $I_{ds}18$ increases. The drain-source current of M17 will increase too. As I_{ds} is proportional to V_{gs}, the bigger I_{ds} the larger V_{gs} is. The gate-source voltage of M17 would increase then V_{gs4} will decrease. As of result, the drain-source current on M5 and M6 will decrease. Finally, the *m* will increase and result the higher tuning range with lower power dissipation.

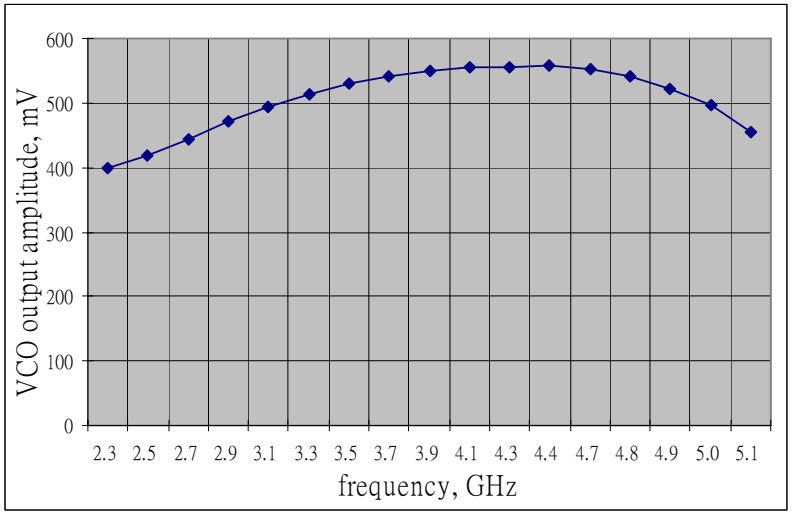


Figure 5.6 Output amplitude variation over a wideband, V_{dd}=2.5 V.

From the C-V curve of the MOSFET SOS varactor, the accumulation region is chosen for better quality factor in this thesis. Hence, there is only one band used in this LC-VCO. The ratio of W/L for transistors and values of components are shown in Table 5.1.

Table 5.1 Dimensions and values of components in LC-VCO

L0 – L3	5.1 nH
Cv0 – Cv3	600 µm / 1 µm
M0 – M3	25 µm / 0.25 µm
M4	1.2 µm / 1 µm
M5 – M6	40 µm / 0.25 µm
M7 – M10	500 µm / 0.25 µm
M11 – M12	120 µm / 0.25 µm
M17	3 µm / 1 µm
M18	1.2 µm / 1 µm
M19 – M20	140 µm / 0.25 µm
Rcap	20 ohm

A compensation circuit is used for the voltage-current inverter, M19, M20, and Rcap, to reduce harmonic noise [5]. It can significantly reduce the second harmonic content if the dimensions of the transistors M19 and M20 are optimized.

The LC VCO output amplitude is 2 – 3 V and common mode voltage (V_{CM}) is 2.5 V with the supply voltage = 2.5 V. The CML frequency divider requires the DC voltage of each input clock to be 1.25 V in order to achieve the highest input frequency

range. Hence, a level shifter or a buffer to connect the LC VCO and the CML divider together is needed. Unfortunately, the level shifter and buffer may require more than 2 stages which will introduce noise from each stage that might degrade the LC VCO performance too much. The original buffers, buffer 1 and buffer 2, can not precisely shift V_{CM} to 1.25 V. Therefore, an AC coupling technique replaces the buffers at the VCO outputs. This gives less noise and the passive components are more tolerant to radiation. The larger AC coupling capacitor maintains the LC VCO output swing but has impact on the area. Figure 5.7 shows the AC coupling techniques for the LC VCO output.

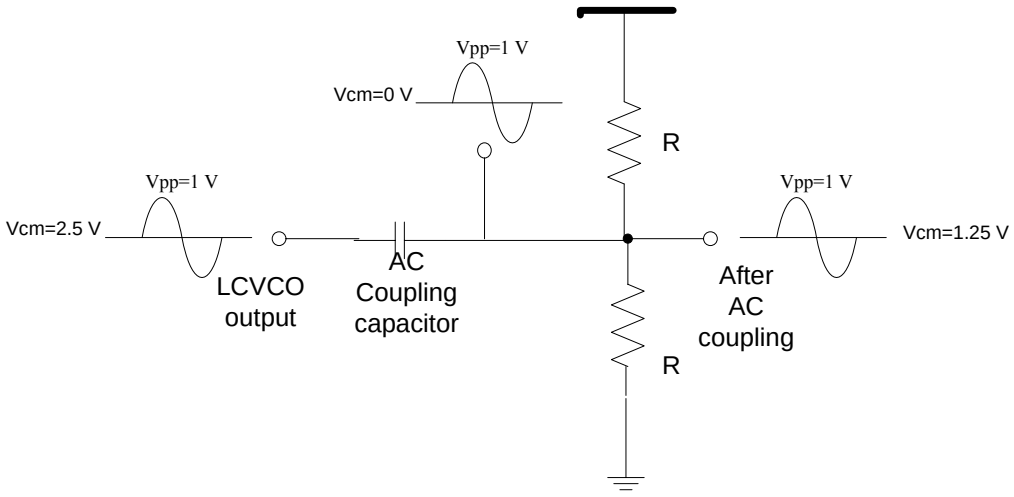


Figure 5.7 AC coupling techniques for LC VCO output.

Circuit optimization is done by the parametric analysis tool in Cadence to determine the best value for each component and to achieve the best performance on every PLL building block. For analysis purposes the initial voltage on LCVCO output net B is set to 2 V in order to start the LCVCO oscillation.

The LC VCO achieves a center frequency of 3.6 GHz and a frequency tuning range from 2.2 GHz to 5 GHz. This achieves a 77% tuning range with a phase noise of -130 dBc/Hz at 1 MHz offset.

At first, the LC VCO phase noise was not performing well compared with other conventional LC VCOs. The top noise contributors in Cadence were found out when M17 is operated in the saturation region, and it was observed that M17 contributed as much as 60% to the total phase noise. As published in the IEEE Journal of Solid State Circuits [7] [18], the phase noise can be reduced largely by placing the filtering capacitor on the current mirror. The filtering capacitor is a 20 pF capacitor to bring bottom node of the M17 to an AC ground and to reduce up-conversion of high frequency noise from the bias circuit. Therefore, this is also implemented in this circuit to reduce the phase noise.

5.2.2. Current Mode Logic Frequency Divider (CML Divider)

The CML divider was derived from a generic analog design. During the course of collaboration with SMU, both teams developed and simulated separate designs. SMU's design was selected for use because it achieved higher input frequency range.

The frequency divider is implemented as a broadband static current mode logic (CML) frequency divider. A circuit diagram of the static CML frequency divider is shown in Figure 5.8. The CML frequency divider can work at least 6 GHz frequency. In this CML frequency divider, the input frequency is from 1.5 GHz to 6.5 GHz at a typical corner.

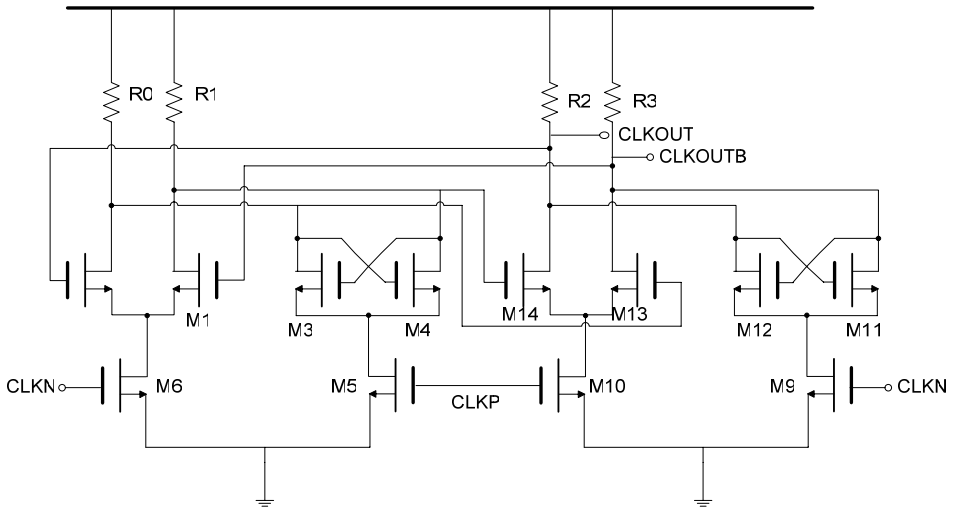


Figure 5.8 Schematic of CML divider circuit

The M3, M4, M11, M12 are called latch transistors. The M0, M1, M13, M14 are called driver transistors. The M5, M6, M9, M10 are called full-rate clock transistors. The cross-coupled latch transistors play an important role in determining whether the divider structure will self oscillate. To increase the high speed operation of the divider, it can usually reduce the size of the latch transistors [8]. Driver transistors size has less effect than the size of other transistors. It usually has the same or little bigger size than the latch transistors. The frequency will be reduced if larger driver transistors are used. The output swing will be reduced if smaller latch transistors are used.

There is a certain common mode size of full rate clock transistors that gives the highest self oscillating frequency. The higher the self oscillating frequency, the higher the speed of divider operation. From the Proceedings of ISCAS 2002 [8], as the size of full rate clock transistors is decreased, the locking range is increased and self oscillating frequency is decreased.

5.2.3. Phase/Frequency Detector

The basic inverter circuit is shown in Figure 5.9 (a) [9]. Figure 5.9 (b) is the transfer curve of the basic inverter after irradiation. The most important changes are the switch point, the decreased output rail voltage, and the increased leakage current. If radiation becomes strong enough, proper PFD operation may fail. Several solutions have been proposed by J. P. Colinge [10]. When VIN is low and NMOS cuts off, it may turn back on during irradiation. The inverter connects between VIN and the NMOS source terminal. When VIN is low, the NMOS source terminal becomes high and V_{gs} becomes negative. The main idea is to maintain the output voltage by making V_{gs} negative when the NMOS cuts off. Figure 5.10 (a) shows the radiation hardened inverter circuit. It is shown in Figure 5.10 (b) that the switch point improves from Figure 5.9 (b).

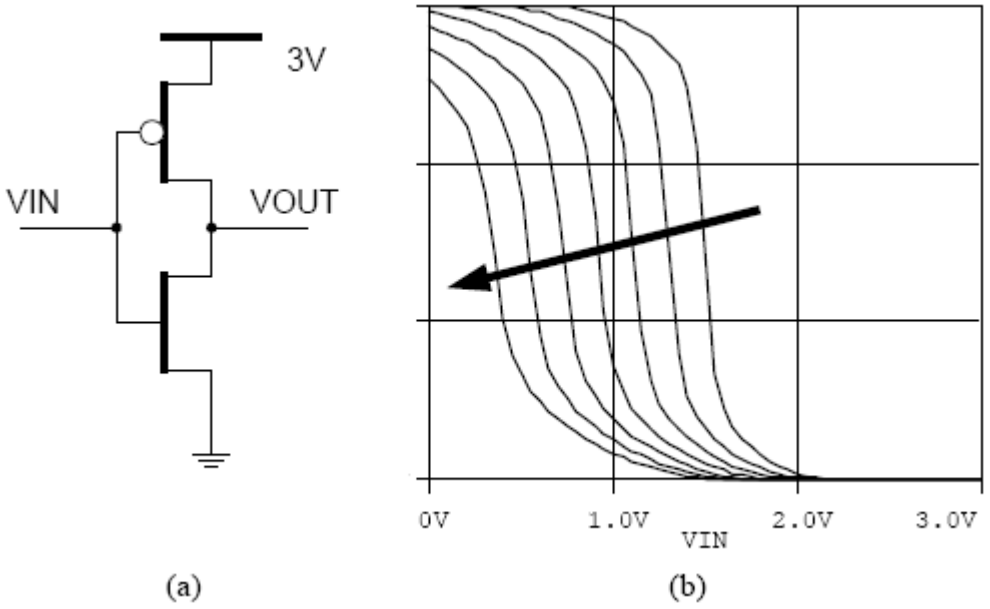


Figure 5.9 (a) Inverter Circuit and (b) input vs. output curve after irradiation [9]

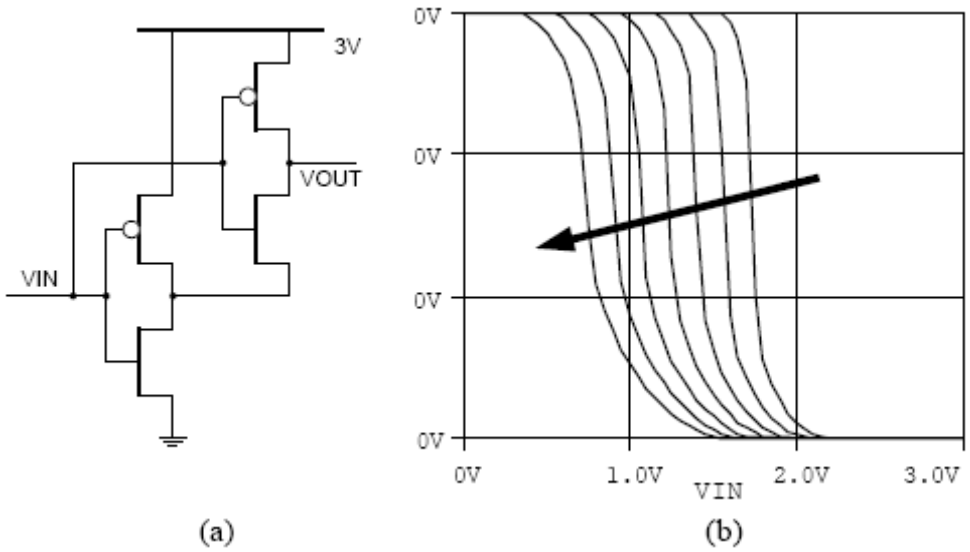


Figure 5.10 (a) Radiation Hardened Inverter Circuit and (b) input vs. output curve after irradiation [9]

The basic phase frequency detector circuit is shown in Figure 5.11 [9]. In order to redesign the circuit for radiation resistance, the above radiation hardened inverter circuit is implemented in each PFD gate. An additional inverter is also added for each NMOS to radiation harden the NAND gate and AND-NOR gate. Figure 5.12 shows the schematic of the radiation hardened phase frequency detector in this phase locked loop.

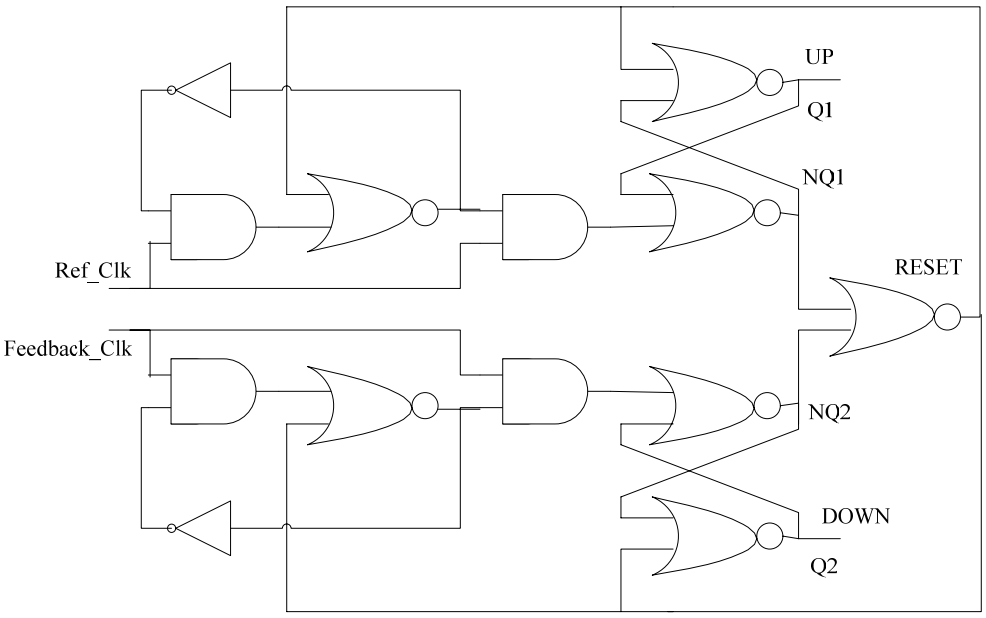


Figure 5.11 Phase/Frequency Detector circuit.

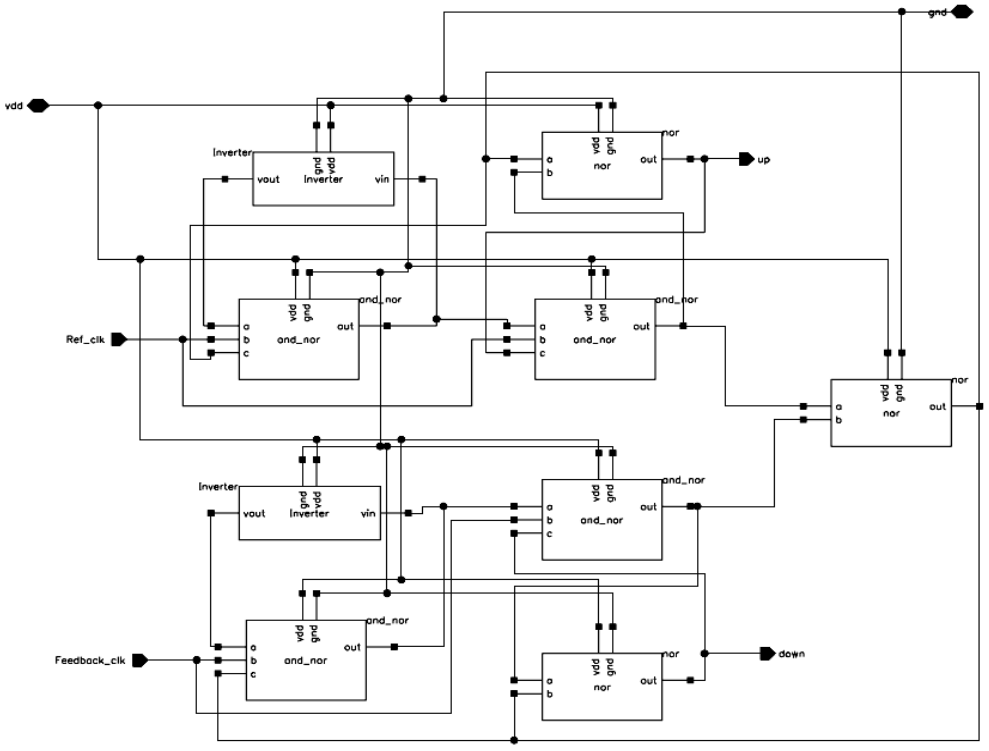


Figure 5.12 Schematic of Phase/Frequency Detector circuit

5.2.4. Charge Pump

Maneatis's self biased zero offset charge pump design was used which adds two inverters to the UP bar and DOWN bar at the charge pump inputs [11]. Figure 5.13 is the zero offset charge pump schematic. The UP and DOWN output signals from PFD have single ended outputs. Charge will be transferred from or to the loop filter connected to the output when the UP input or DOWN input is switched high respectively.

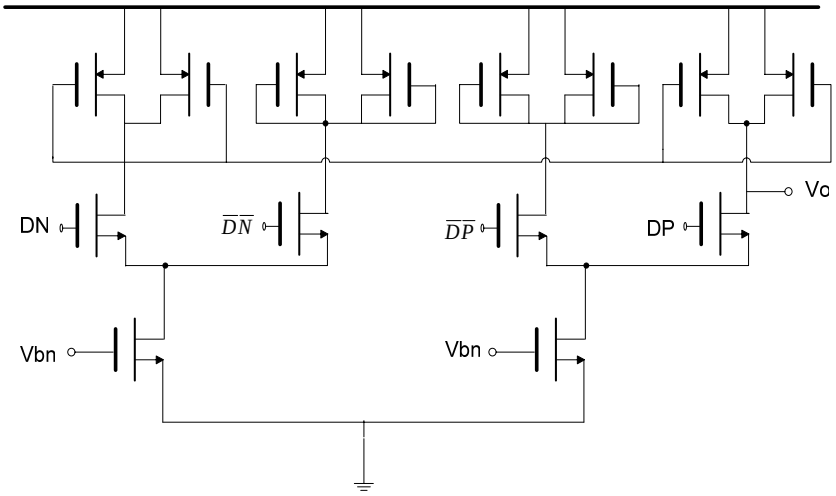


Figure 5.13 Schematic of Maneatis Charge Pump

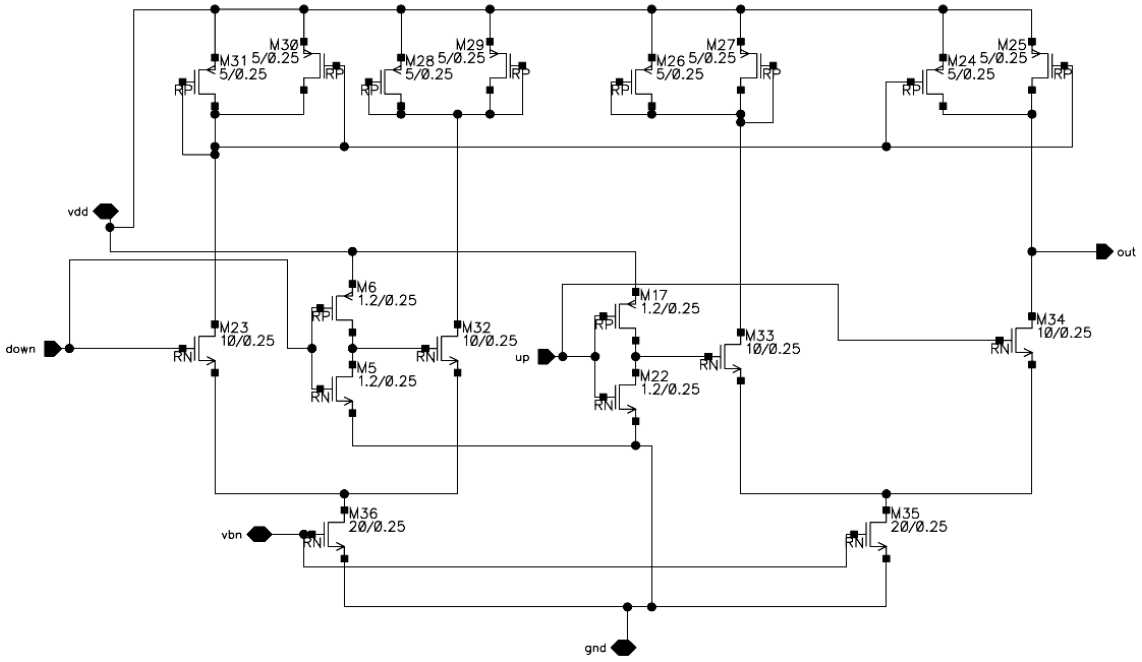


Figure 5.14 Schematic of Charge Pump

The schematic and transistor dimensions are shown in Figure 5.14 and Table 5.2. It has been simulated with the radiation hardened model file.

Table 5.2 Dimensions and values of components in Charge pump

M24 – M31	5 µm / 0.25 µm
M23, M32, M33, M34	10 µm / 0.25µm
M5, M6, M17, M22	1.2 µm / 0.25 µm
M35, M36	20 µm / 0.25µm

5.2.5. Loop Filter (LP)

A PLL may be stable or unstable depending on phase margin or damping factor. PLL bandwidth is the frequency at which the PLL begins to lose lock with the reference (-3dB). Both stability and bandwidth affect settling, phase error, or jitter. In order to determine the stability and bandwidth of the phase locked loop, the damping factor and neutral frequency must be determined. Figure 5.15 shows the second-order loop filter schematic.

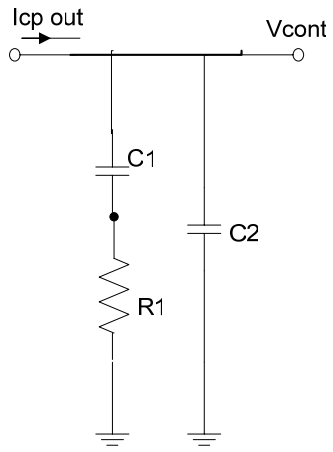


Figure 5.15 Schematic of loop filter

A charge pump PLL (CP-PLL) consists of two poles at the origin, one is from the VCO and the other is from the integrator in the second-order loop filter. A stabilizing zero is required to stabilize the loop. A second-order loop filter is commonly used in a CP-PLL. A resistor R1 is connected in series with a capacitor C1 to provide a stabilizing zero. C2 is connected in parallel to reduce the ripple at the control voltage on VCO and restrain spurious tones at the VCO output. Table 5.3 shows the dimensions and values of components in the loop filter.

Table 5.3 Dimensions and values of components in Loop Filter

C1	100 pf
R1	800 ohm
C2	10 pf

The un-damped neutral frequency is given by

$$\omega_n = \sqrt{\frac{K_{VCO} \cdot I_{CP}}{2\pi \cdot M \cdot C_1}} \text{ in Hz} \tag{5.21}$$

Where

Kvco = VCO gain in Hz/V

Icp = charge pump current in amps

M = feedback divider ratio

C1 = large LPF capacitor

In general, for good stability, ω_n is less than ~1/10 of the input reference frequency. A typical value of ω_n goes from 1 MHz to 10 MHz. The damping factor is given by

$$\zeta = \frac{R_1}{2}\sqrt{\frac{K_{VCO} \cdot I_{CP} \cdot C_1}{2\pi \cdot M}} \tag{5.22}$$

where

R_1 = LPF resistor

The damping factor is generally from 0.45 to 1.5. C2 is usually less than 1/10 of the large LPF capacitor C1 for stability and larger than 1/50 of C1 for low jitter. A larger C2/C1 will increase phase error slightly. With both equations, it is possible to

assume that R1=800 Ω and C1=100 pF and calculate the damping factor for 1.08 and un-damped neutral frequency for 4.3 MHz.

5.2.6. Differential to single ended converter and TSPC divider

LC VCO gives small amplitude outputs with high frequency. The TSPC divider can only operate below 5 GHz with CMOS logic input. Also the CML frequency divider input frequency range is from 1.5 GHz to 6.5 GHz. Hence, it cannot divide the VCO output down to the 90 MHz reference clock with a CML frequency divider.

In order to make the divider operate within the required frequency range, the CML frequency divider was used at the first stage (divided by 2). Then one differential to single ended converter is used on the second stage to amplify the signal level to CMOS logic output. Finally, the TSPC divider (divide by 20) is implemented on the last stage to divide down to the reference clock.

All D2S and TSPC circuits are provided by SMU. The total divider ratio M is 2 x 20 = 40.

5.3 PLL Block Diagram

Radiation hardened techniques are implemented on each block. Figure 5.16 shows the top level schematic of the radiation hardened phase locked loop.

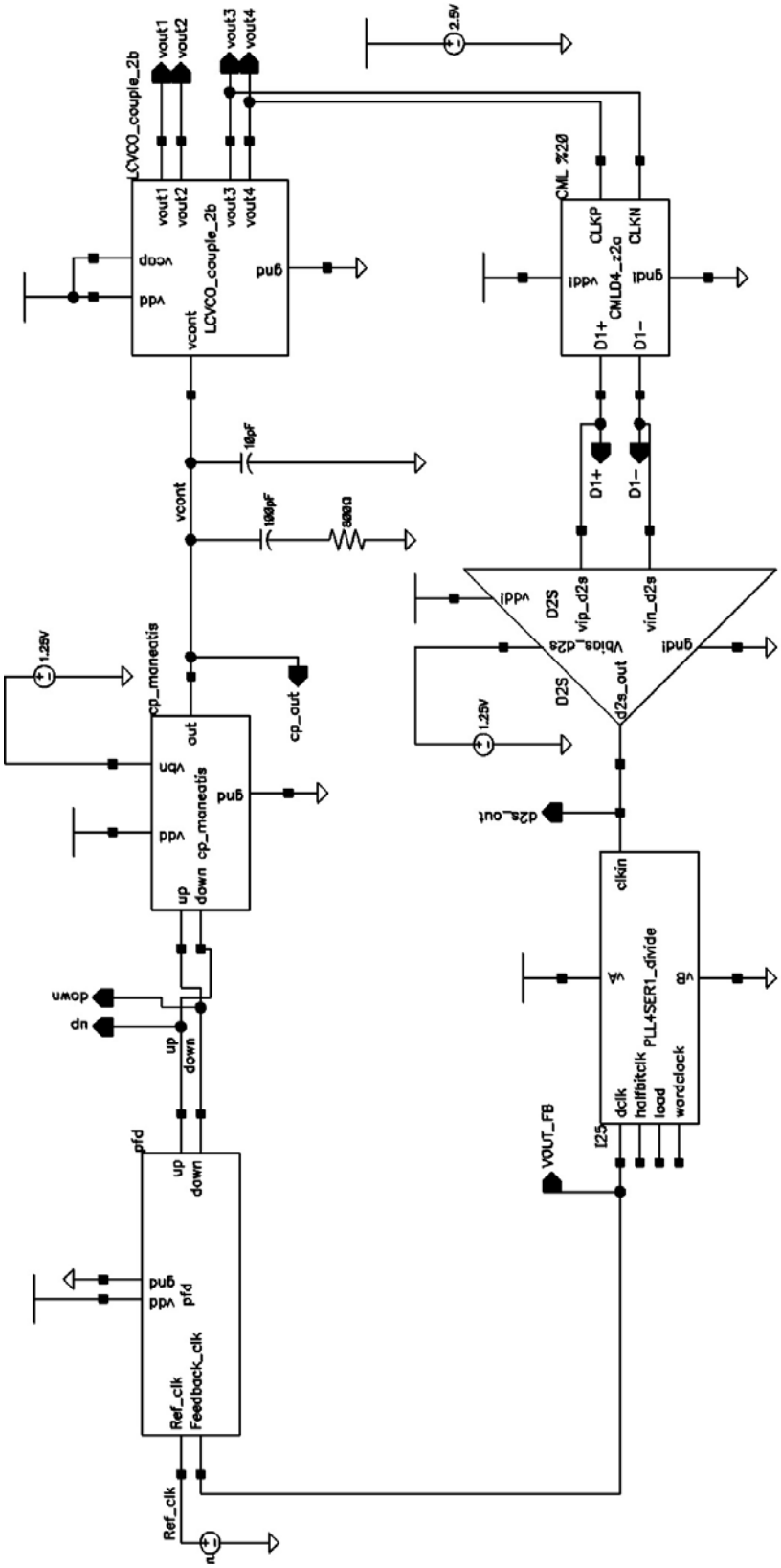


Figure 5.16 Schematic of radiation hardened phase locked loop.

CHAPTER 6

SIMULATION RESULTS AND DISCUSSION

This chapter focuses on the simulation results for the radiation hardened phase locked loop designed for this project. The first section shows the simulation results prior to radiation using a typical model file. The second section shows the post radiation simulation results using the radiation-hard model file. The last section shows the simulation results from the pre-radiation LCVCO corner simulation.

In Chapter 2, it was stated that the TID effects increased the threshold voltage of both NMOS and PMOS transistors by about 0.2 V. In simulations for the radiation effect, V_{th0} adjusts +0.2 V for NMOS and -0.2 V for PMOS (absolute value). The TID effects on PLL performance are evaluated by changing V_{th0} in the model files.

The other major radiation effect is the mobility degradation. The same estimate of mobility degradation in [9] was used, and the same Peregrine SOS technology was used except that a 0.5 μm process was used Also the lower dose volume of 1M rad/hr was supplied. This project tested for a much higher total dose, which is 4M rad/hr with a 0.25 μm process. The mobility changes -10% in [9] for 1M rad/hr total dose. In this post radiation simulation, the TID effect was simulated by reducing the mobility by -20% for both transistors in the model file.

Since other parameters have not yet been extracted, they cannot be adjusted in this radiation-hard model file. Because V_{th0} and mobility are main parameters of

MOSFETs, this post radiation simulation shows the basic degradations of the PLL performance due to the radiation effect. Accordingly, this simulation can help optimize our radiation hard PLL design.

6.1 Pre-radiation Simulation

6.1.1. LC Voltage controlled oscillator

The tuning range of the LC VCO is determined by using the control voltage vs. frequency curve shown in Figure 6.1. The simulated results are 2.32 GHz at 0.5 V and 5.1 GHz at 2.2 V. The total tuning range is 2.78 GHz. The Kvco is 1.718 GHz/V.

The phase noise response of LC VCO is shown in Figure 6.2. The measured value of phase noise is -130 dBc/Hz at 1 MHz offset.

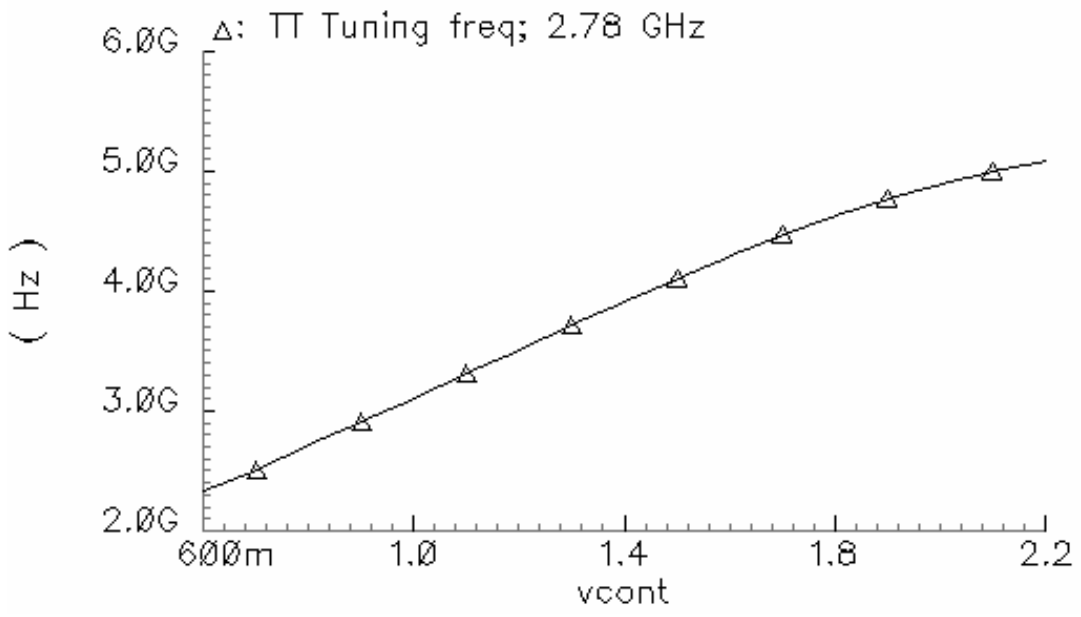


Figure 6.1 Frequency tuning range of VCO in pre-radiation simulation

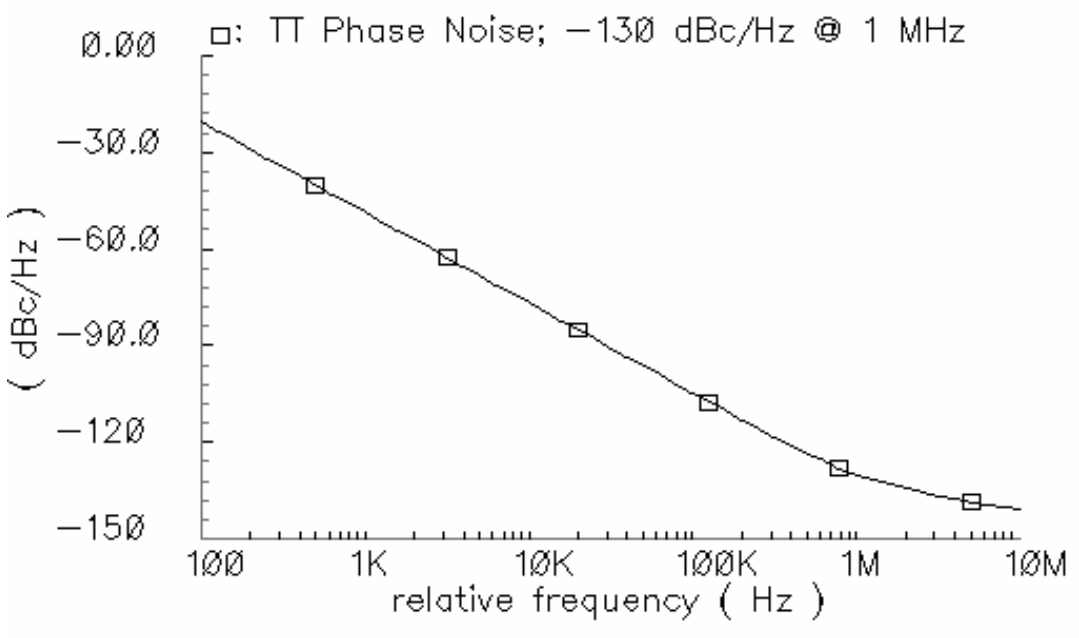


Figure 6.2 Phase Noise of VCO in pre-radiation simulation

6.1.2. CML divider

The CML frequency divider is a divide by two circuit. Figure 6.3 shows the output results of CML divider output and CML divider clock inputs. The CML divider clock input is 6 GHz sinusoidal wave and the measured CML divider output is 3 GHz.

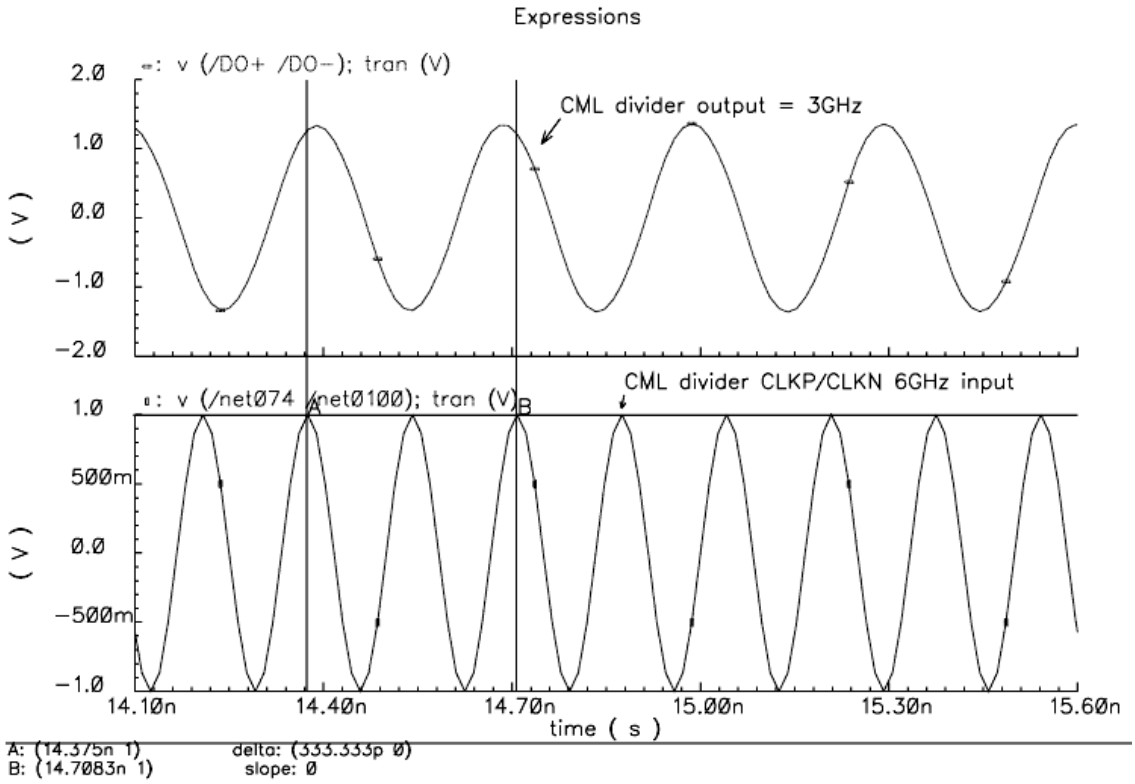


Figure 6.3 CML divider output in pre-radiation simulation

6.1.3. Phase/ Frequency detector

The response of phase frequency detector is shown in Figure 6.4, 6.5, and 6.6. The reference clock frequency is 90 MHz. Figure 6.4, 6.5, and 6.6 show the reference clock lags the feedback clock, the reference clock leads the feedback clock, and both clocks are in phase respectively in pre-radiation simulation.

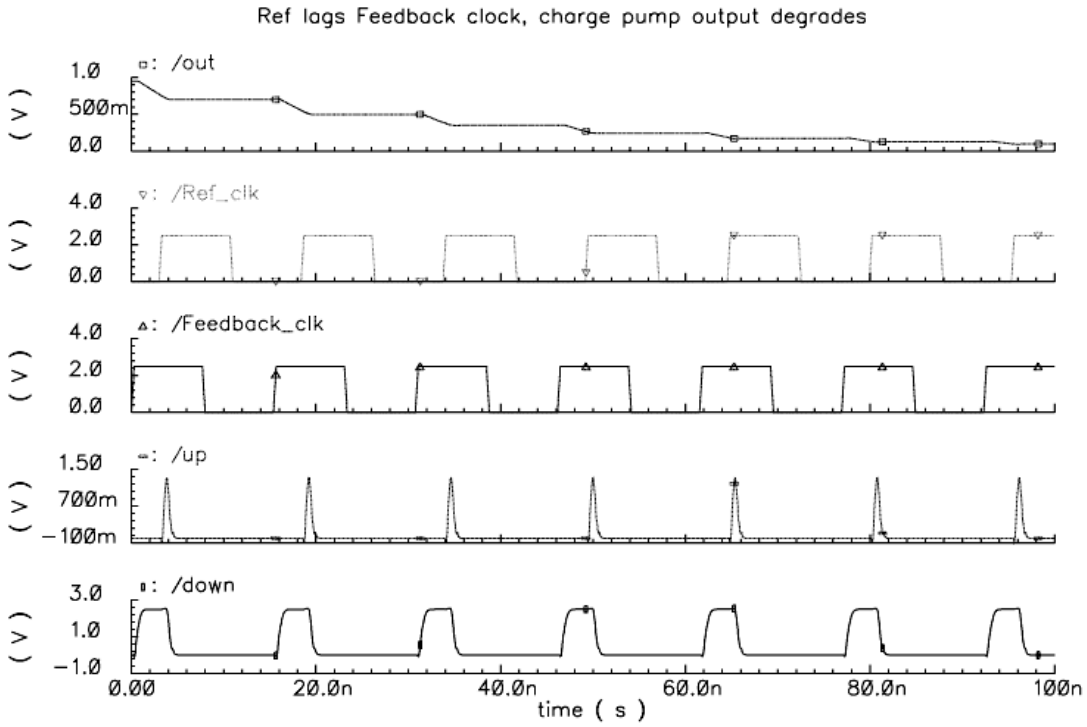


Figure 6.4 PFD and charge pump output when reference lags feedback clock in pre-radiation simulation

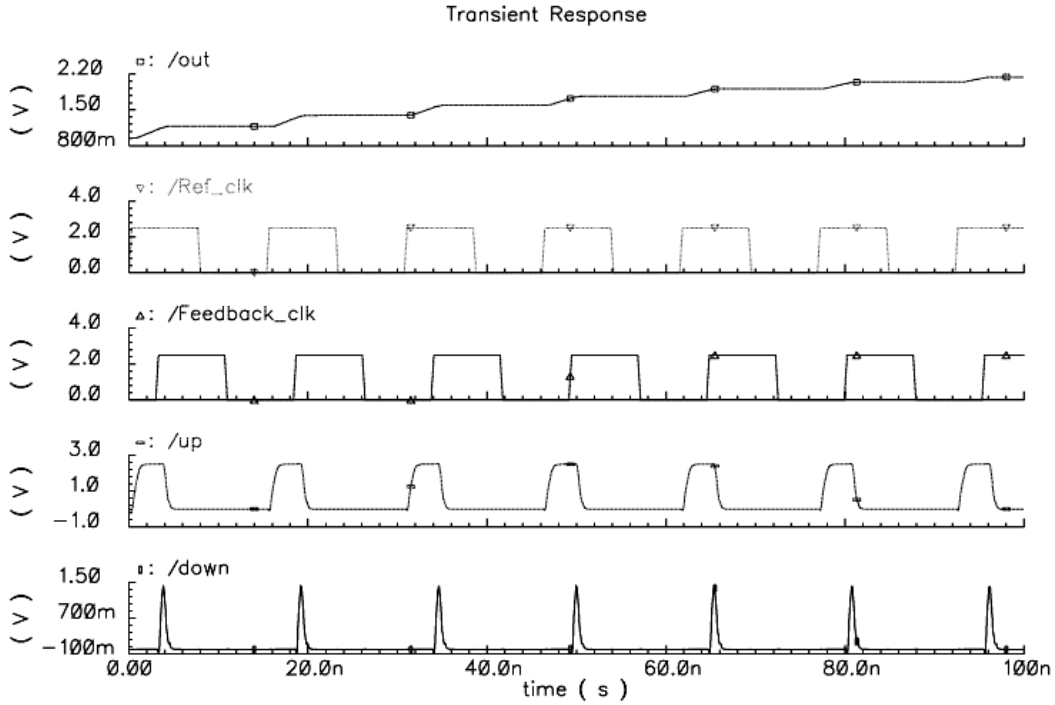


Figure 6.5 PFD and charge pump output when reference leads feedback clock in pre-radiation simulation

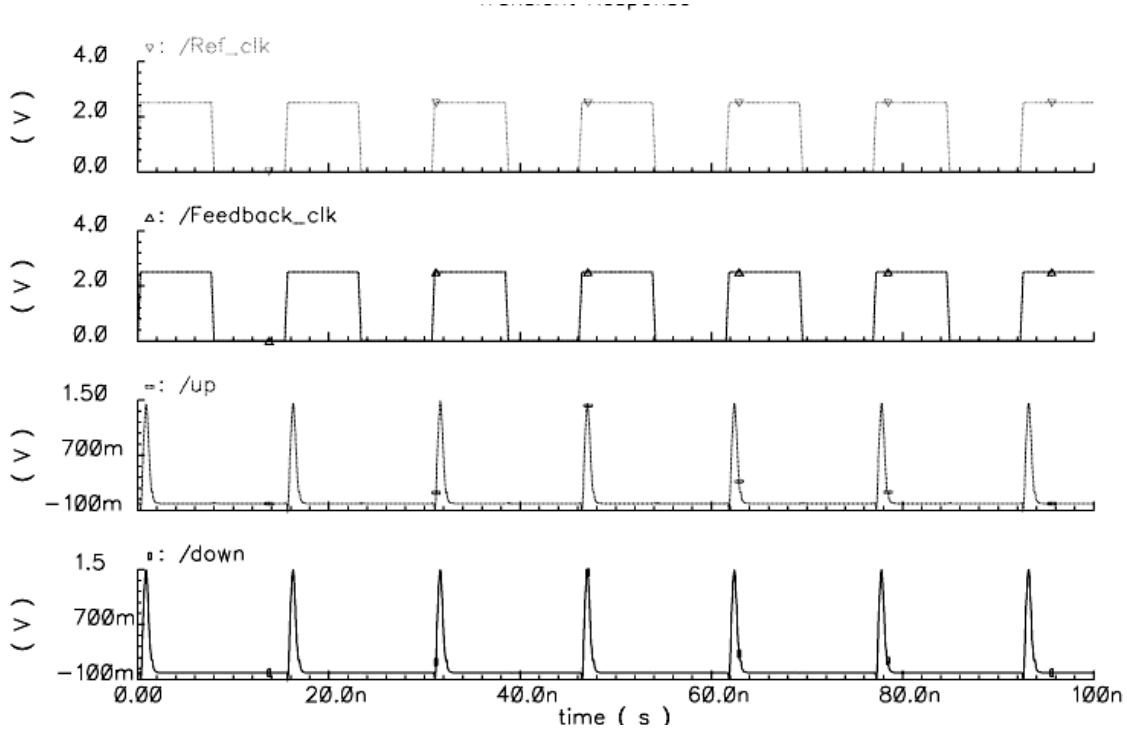


Figure 6.6 PFD and charge pump output when reference and feedback clock are in phase in pre-radiation simulation

6.1.4. LC Phase locked loop

The phase locked loop is locked at 350 ns in Figure 6.7 Figure 6.8 shows both reference/ feedback and up/ down clocks are locked in phase and frequency. The VCO output frequency is 3.6 GHz in Figure 6.9. From Figure 6.1 to Figure 6.9, shows the LC PLL operates very well in the pre-radiation simulation.

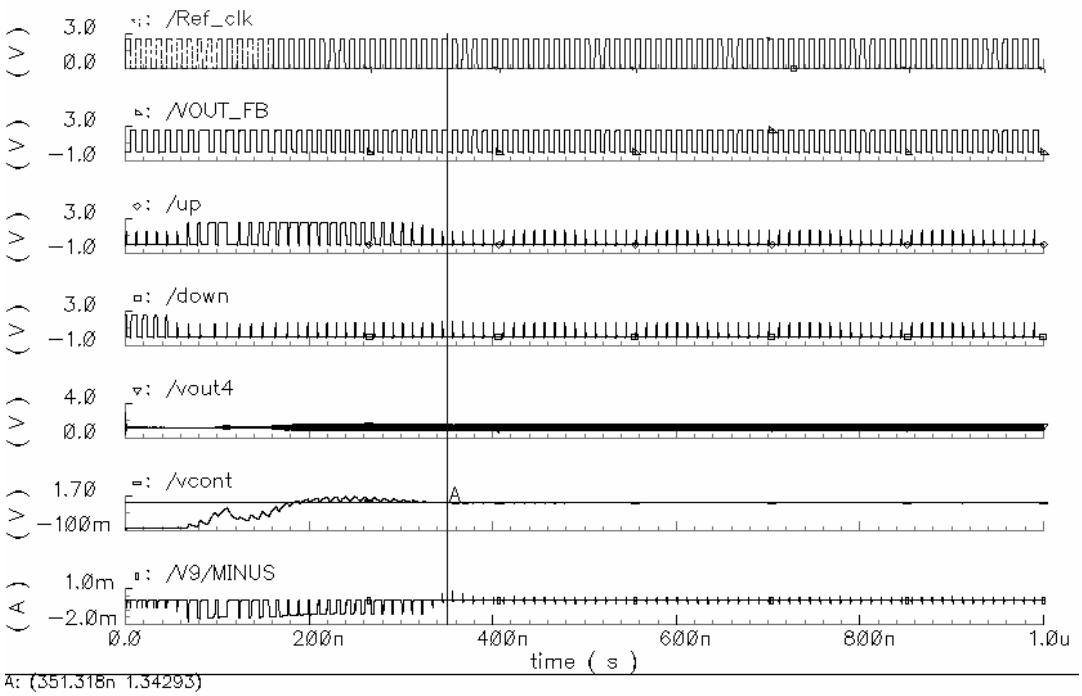


Figure 6.7 Locking time of Phase locked loop in pre-radiation simulation

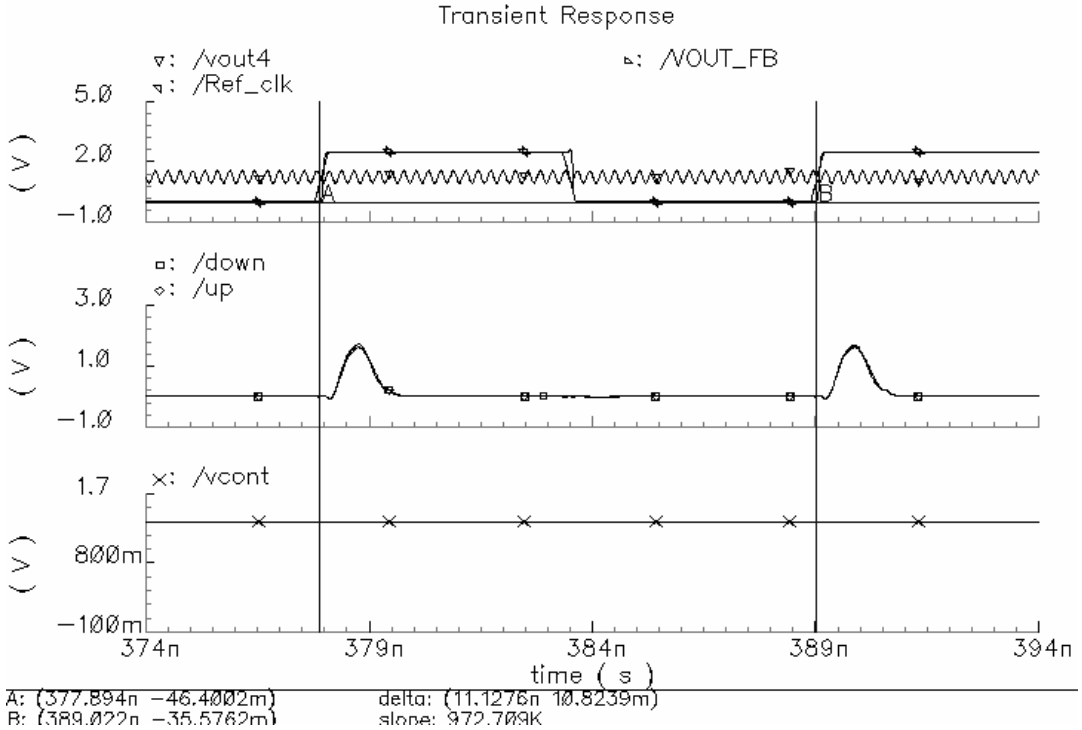


Figure 6.8 Reference clocks locked with feedback clock in phase and frequency in pre-radiation simulation (Zoom in)

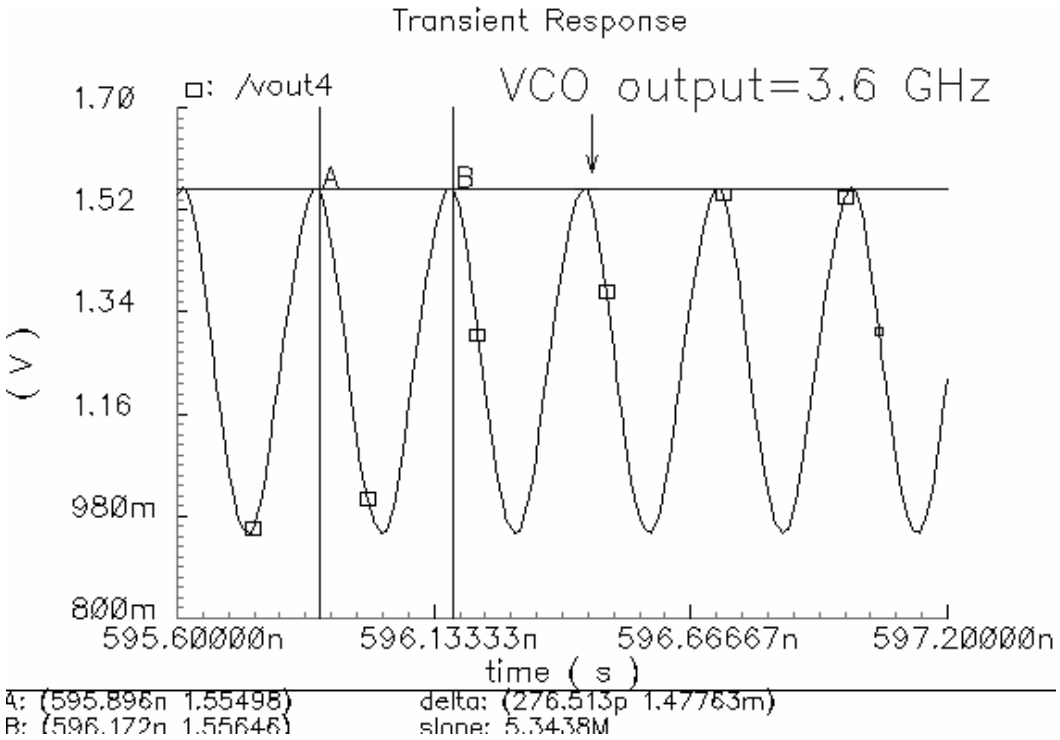


Figure 6.9 LC Voltage controlled oscillator output in pre-radiation simulation

6.2 Post-radiation Simulation

6.2.1. LC Voltage controlled oscillator

The tuning range of the LC VCO post radiation simulation is determined by using the control voltage vs. frequency as shown in Figure 6.10. The simulated results are 2.261 GHz at 0.7 V and 4.825 GHz at 2.1 V. The total tuning range is 2.564 GHz. The Kvco is 1.624 GHz/V.

The phase noise response of the LC VCO is shown in Figure 6.11. The measured value of phase noise is -127.9 dBc/ Hz at 1 MHz offset.

The total tuning range after post radiation is reduced from 2.78 GHz to 2.564 GHz and the phase noise after post radiation is increased from -130 to -127.9 dBc/Hz.

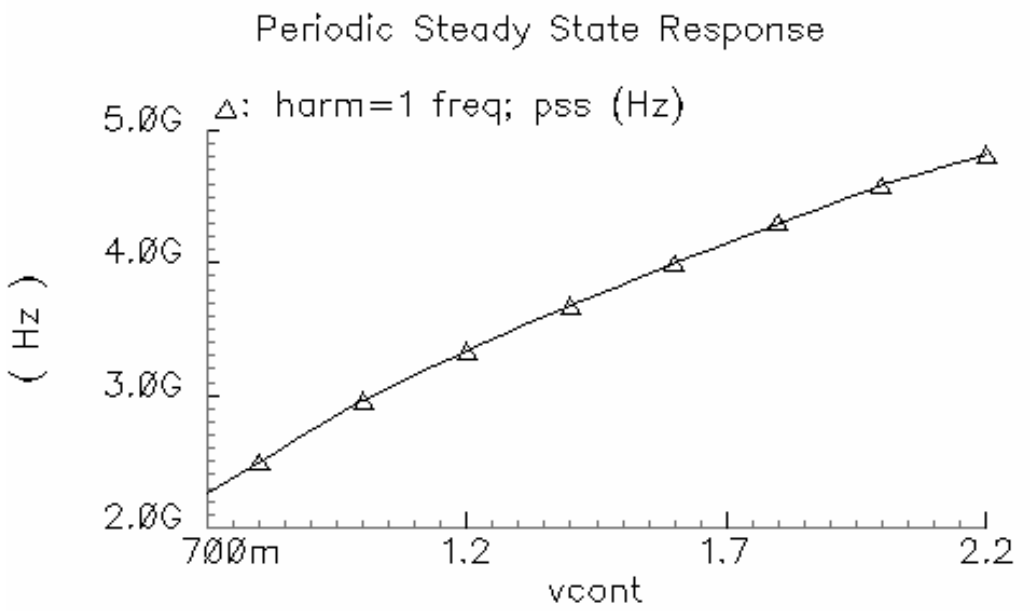


Figure 6.10 Frequency tuning range of VCO in post-radiation simulation

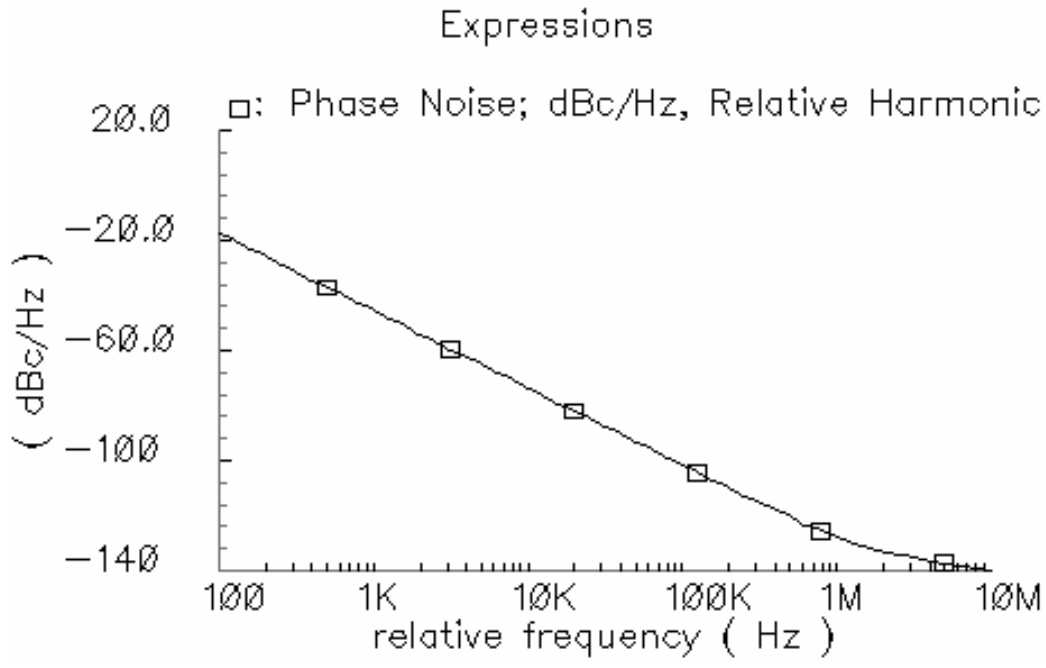


Figure 6.11 Phase Noise of VCO in post-radiation simulation

6.2.2. CML divider

Figure 6.12 shows the output results of the CML divider output and CML divider clock inputs. The CML divider clock input is 6 GHz sinusoidal wave and the measured CML divider output is 3 GHz. The CML divider operates very well after post radiation.

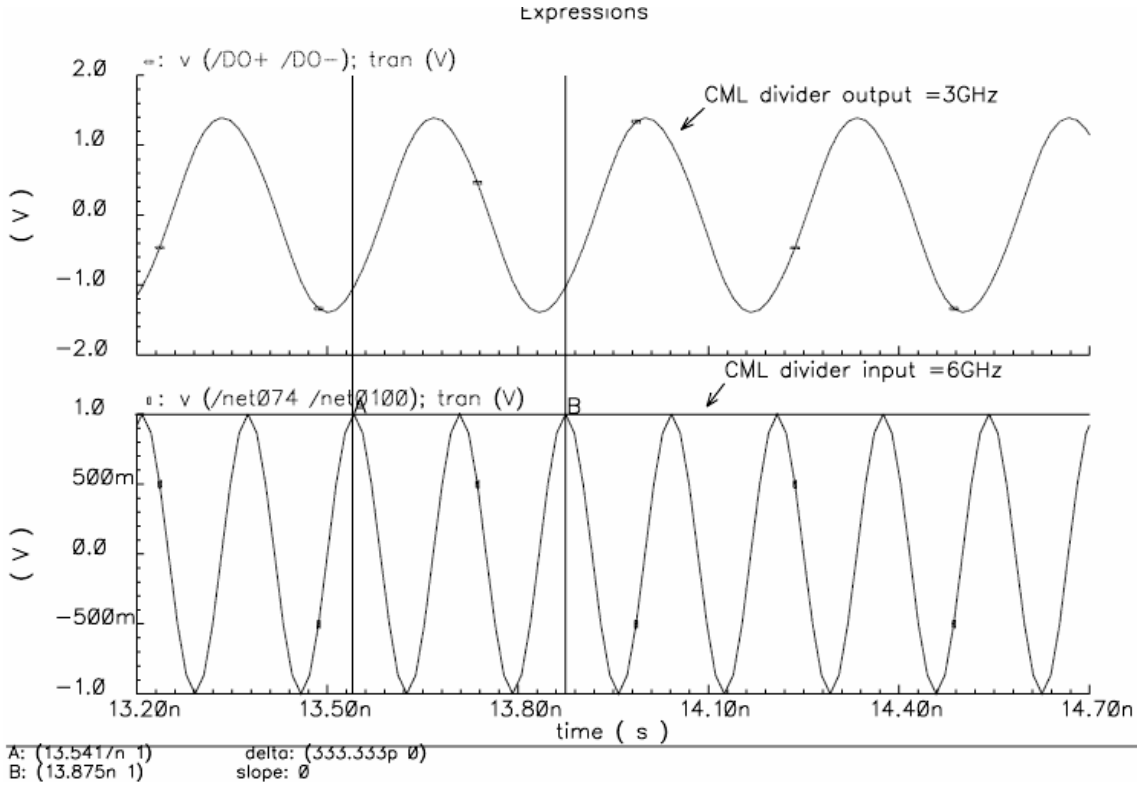


Figure 6.12 CML divider output in post-radiation simulation

6.2.3. Phase/ Frequency detector

The response of the phase frequency detector is shown in Figure 6.13 and 6.14. The reference clock frequency is 90 MHz. Figures 6.13 and 6.14 show the reference clock lags the feedback clock, the reference clock leads the feedback clock, and both

clocks are in phase respectively in post radiation simulation. PFD works correctly after post radiation simulation.

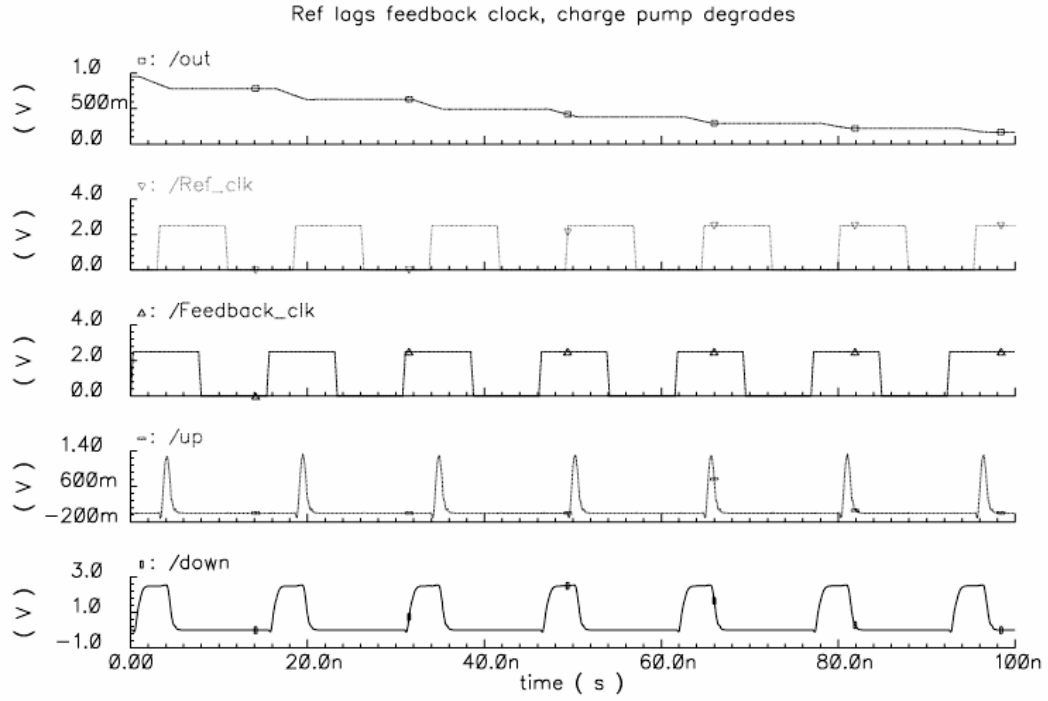


Figure 6.13 PFD and charge pump output when reference lags feedback clock in post-radiation simulation

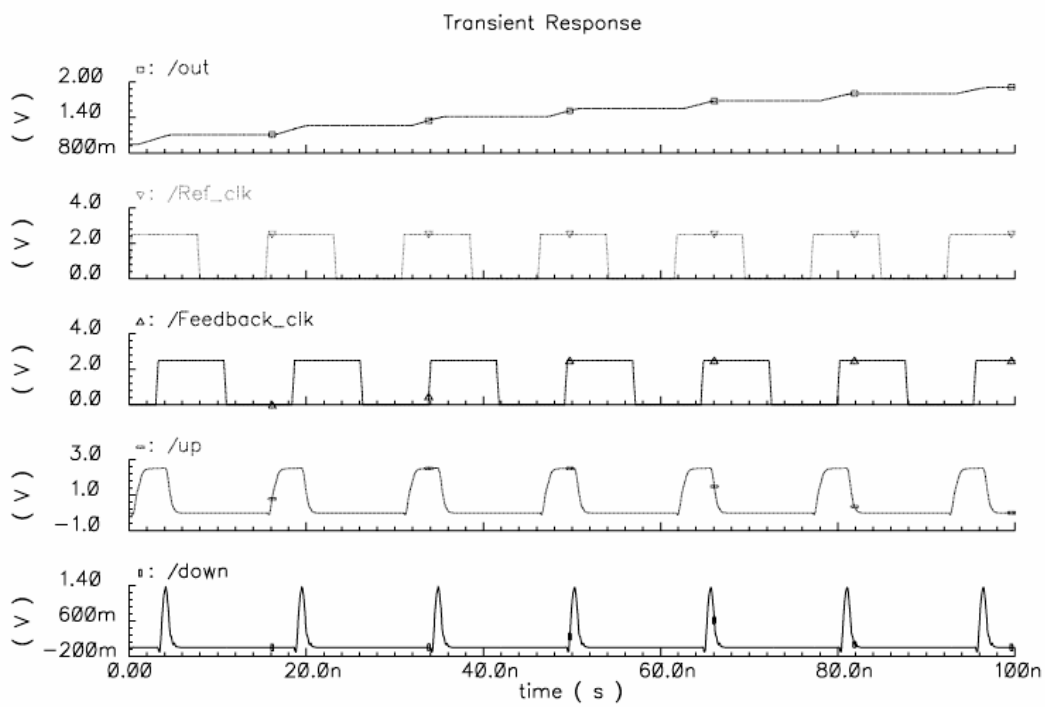


Figure 6.14 PFD and charge pump output when reference leads feedback clock in post-radiation simulation

6.2.4. LC Phase locked loop

The phase locked loop is locked at 450 ns in Figure 6.15. Figure 6.16 shows both reference/ feedback and up/ down clocks are locked in phase and frequency. The charge pump current is 1.2 mA in Figure 6.17. The VCO output frequency is 3.6 GHz in Figure 6.18. From Figure 6.10 to Figure 6.18, it is shown the LC PLL operates very well after post-radiation simulation.

The locking time is increased from 350 ns in pre-radiation to 450 ns in post radiation. The TID effects increased the locking time after radiation.

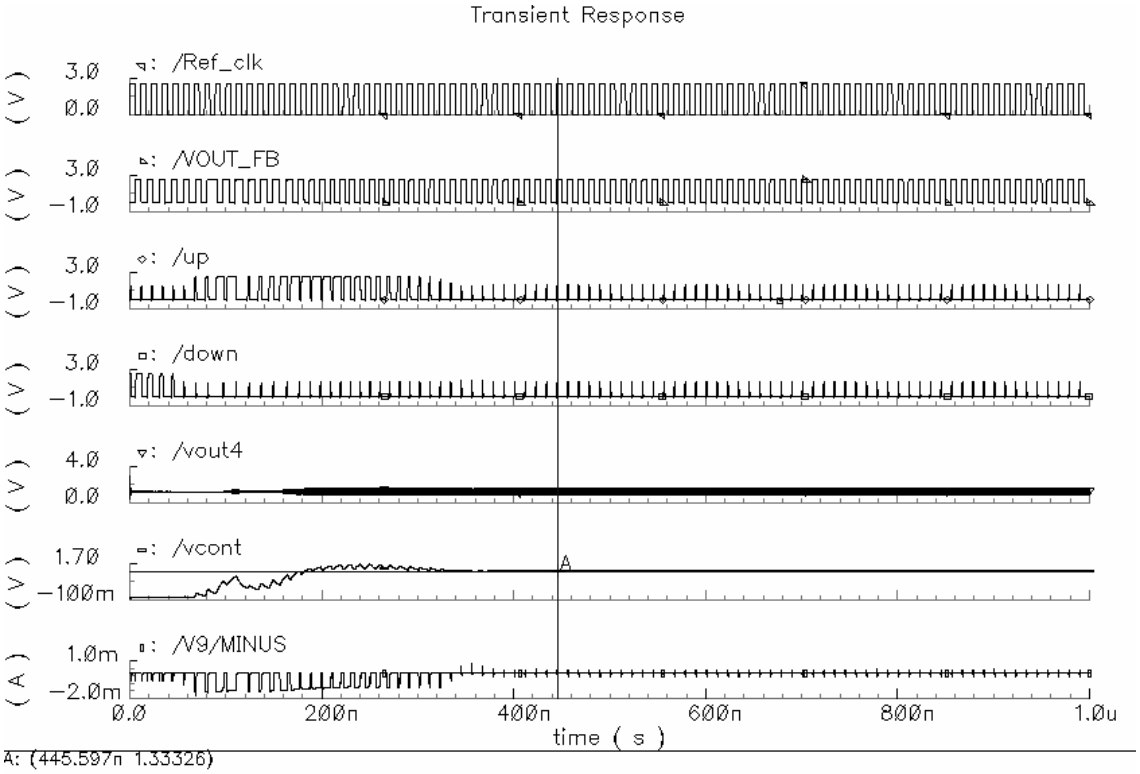


Figure 6.15 Locking time of Phase locked loop in post-radiation simulation

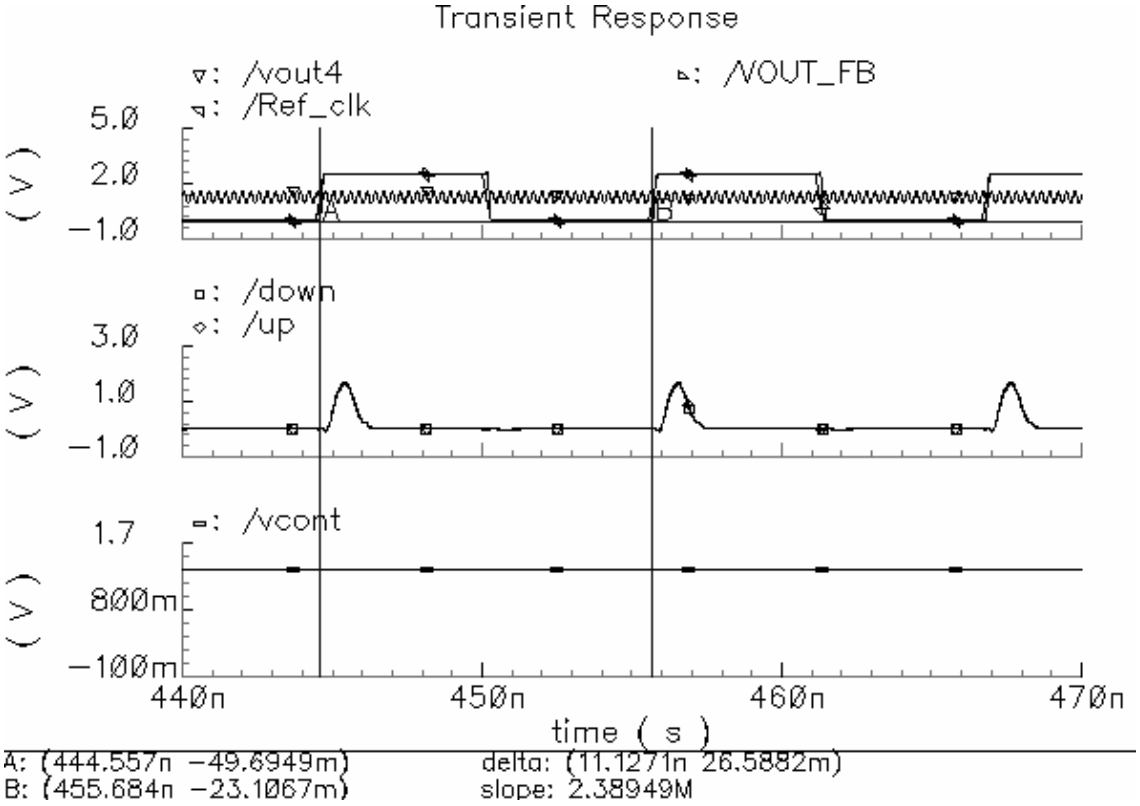


Figure 6.16 Reference clocks locked with feedback clock in phase and frequency in post-radiation simulation (Zoom in)

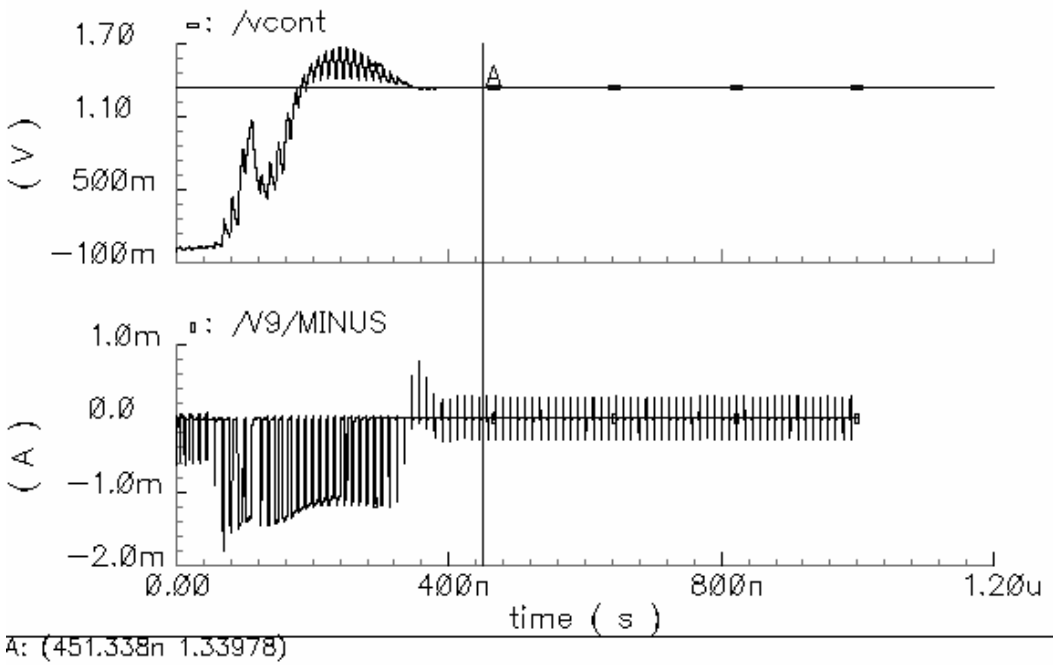


Figure 6.17 VCO output locking time and charge pump current in post-radiation simulation. (Zoom in)

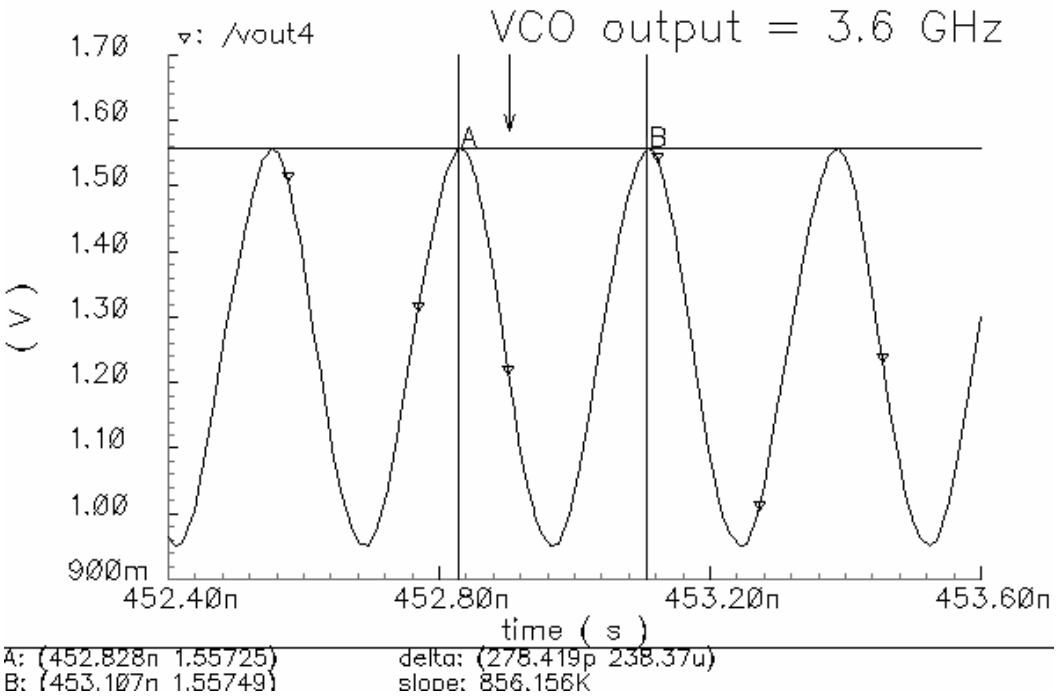


Figure 6.18 LC Voltage controlled oscillator output in post-radiation simulation

6.3 Pre-radiation LC VCO Corner Simulation

In order to ensure the chip can function well under different process, area on the wafer, voltage, and temperature, it is required to run all corners tests for more accurate simulations. Traditional simulation corners are defined as typical, strong (fast) and weak (slow). The strong corner uses a high voltage, and low temperature silicon process. The weak corner uses a low voltage, and high temperature silicon process. It is imperative to characterize designs across all corners and compare simulated design data against specifications.

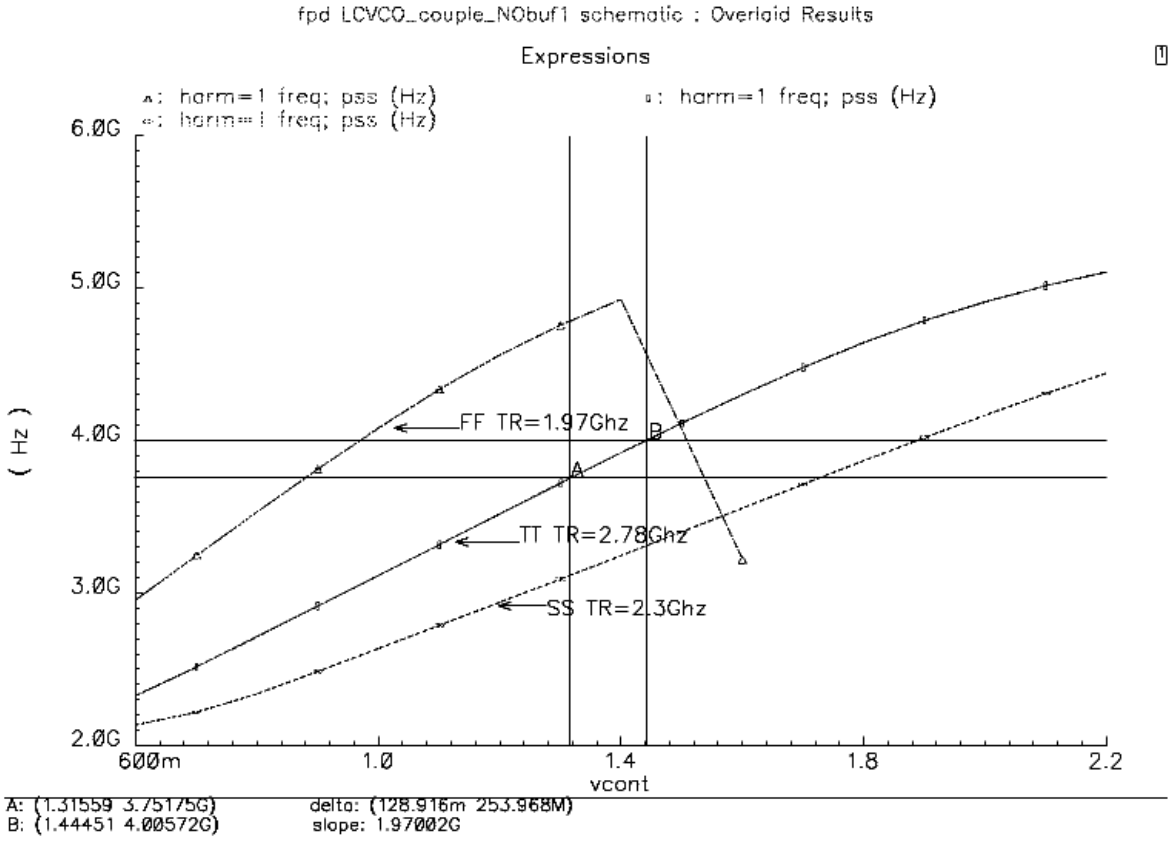


Figure 6.19 Frequency tuning range of VCO in pre-radiation corner simulation

Figure 6.19 shows LCVCO tuning range corner simulation. The tuning range on typical, slow, and fast corner is 2.78 GHz, 2.3 GHz, and 1.97 GHz respectively. The fast corner has a short tuning range from 600 mV to 1.4 V. This range is still in the VCO control voltage range. All tuning range is covered ± 1 GHz of 3.6 GHz at the VCO output frequency. From the corner simulation, the design of LC VCO is operated well in all margins.

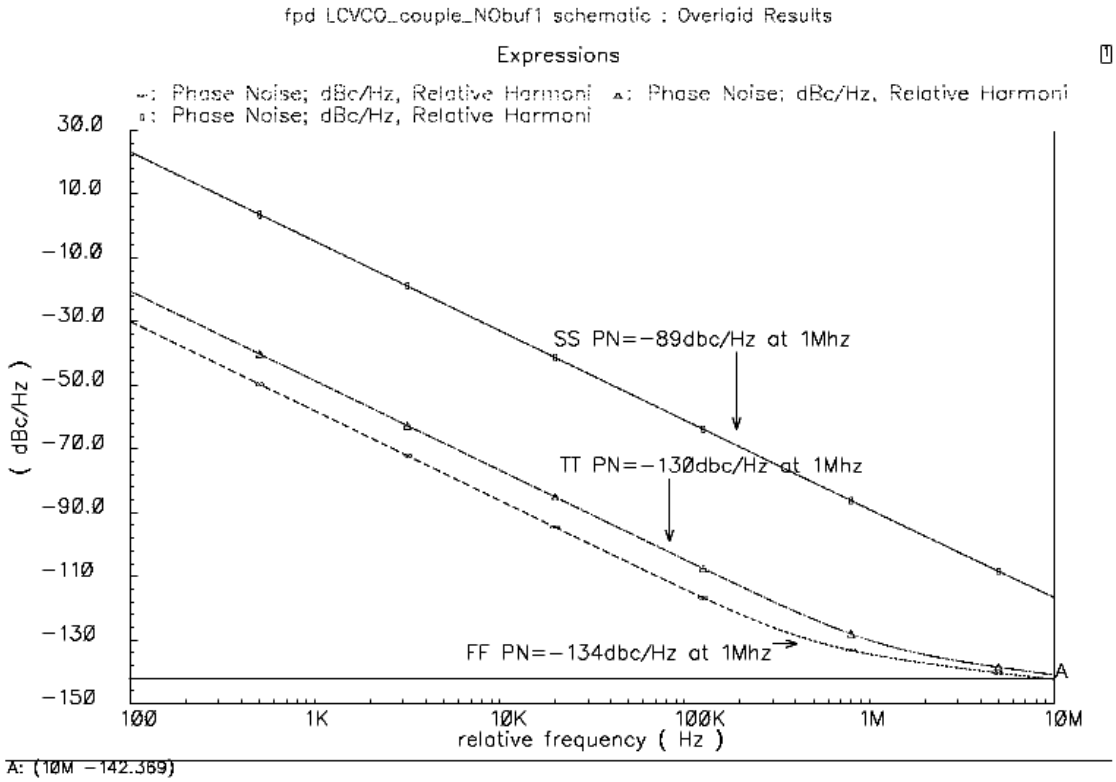


Figure 6.20 Phase Noise of VCO in pre-radiation corner simulation

Figure 6.20 shows LCVCO phase noise corner simulation. The phase noise on typical, slow, and fast corner is -130 dBc/Hz, -89 dBc/Hz, and -134 dBc/Hz at 1 MHz offset respectively. From the corner simulation, the design is resulted higher phase noise on the weak corner but performed well on typical and strong corners.

CHAPTER 7

LAYOUT

7.1 Introduction

Cadence can be used to design a layout for a 0.25 μm SOS CMOS process using either a standard technique or an Enclosed Layout Transistor (ELT) technique.

The advantage of a standard layout is less area is consumed (cost savings), and less design complexity. However, the drawback of a standard layout is the expectation of higher PMOS leakage current after radiation based on SMU research.

The advantage of ELT is that it reduces radiation-induced edge leakage currents and increases guard banding around the devices to mitigate field oxide leakage and circuit susceptibility to latch-up conditions. However, the drawbacks of an ELT layout are both the area penalty (cost) and layout complexities for the high W/L ratio transistors.

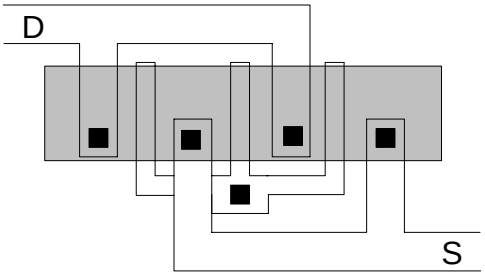


Figure 7.1 Standard multi fingers layout shape

The multi fingers layout is imperative for the high ratio W/L transistors. Figure 7.1 shows standard multi fingers layout. Additionally, The ELT layout shape is illustrated in Figure 7.2.

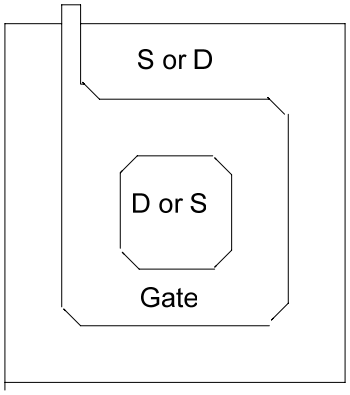


Figure 7.2 ELT layout shape

After considering the design tradeoffs, the time and material economies of a standard layout is chosen. Significant density advantage is achieved.

7.2 Layout Consideration

For the LC VCO and each building block in the PLL, careful consideration was taken to maintain as much symmetry as possible between the differential pairs of the circuit. Symmetry was emphasized to limit parasitic capacitance and resistance in the tank and circuit and thus limit destructive noise that could greatly degrade the frequency and the quality factor achieved. Additionally, the metal traces were designed to minimize resistance.

CHAPTER 8

CONCLUSION AND FUTURE WORK

The objective of this project is to develop a radiation hardened PLL. The radiation effects on transistors, PLL, and its various building blocks have been studied. The PLL was designed and will be fabricated in a 0.25 μm SOS CMOS process with 2.5 V power supply. The LC VCO tuning range and phase noise are 2.78 GHz and -130 dBc/Hz at 1 MHz offset before radiation. After radiation simulation, the LC VCO maintains a good tuning range of 2.56 GHz and phase noise of -127.9 dBc/Hz at 1 MHz offset. The PLL locking time of pre-radiation and post-radiation are 350 ns and 450 ns respectively. The post radiation results degradation of the performance of LCVCO tuning range, phase noise, and PLL locking time.

The VCO tuning characteristics and the charge pump bias currents in the PLL may shift after irradiation. This variation will result in a change in the loop bandwidth and the damping factors. This could lead to peaking in the jitter and change the locking time in the PLL.

SEE effects on the frequency divider, phase/frequency detector, and the loop filter can result in the loss of phase lock. Restoring the lock requires several hundred nanoseconds. The data stream could be corrupted after SEE effects.

This project will continue to do layout and the post layout simulations. The top level system validation will also be implemented. The VCO and PLL will be tested and

evaluated in the fabricated chip. The characterization work of radiation hardness and noise tolerance will be done. Table 8.1 shows the performance summary chart of the proposed radiation hardened PLL. The chip area value is tentative.

Table 8.1 Performance summary chart of the proposed radiation hardened PLL

	Typical (Pre-radiation)	Post-radiation
Technology	PSC 0.25 μm SOS CMOS	PSC 0.25 μm SOS CMOS
Supply Voltage	2.5 V	2.5 V
Threshold Voltage (NMOS/PMOS)	0.44 V / - 0.4 V	0.64 V/ -0.2 V
Mobility (NMOS/PMOS)	0.0236/ 0.015	0.01888/ 0.012
Output Frequency	3.6 GHz	3.6 GHz
Frequency Range	2.32 GHz ~ 5.1 GHz	2.261 GHz ~ 4.825 GHz
Tuning Range	77 %	71 %
Reference Frequency	90 MHz	90 MHz
Divider topology/ ratio	Integer N/ 40	Integer N/ 40
Neutral Frequency	4.3 MHz	3.21 MHz
Phase Noise on VCO	-130 dBc/Hz at 1 MHz offset	-127 dBc/Hz at 1 MHz offset
Locking time	<350 ns	<450 ns
Power dissipation	124.225 mW	145.73 mW
Chip area (estimate)	~900 by 1100 μm²	~900 by 1000 μm²
Off chip part	None	None

The future work includes developing new ideas such as

a) power dissipation reduction

b) leakage cancellation technique

c) self calibration architectures techniques

d) radiation-hard circuit techniques

e) fractional-N frequency synthesizer PLL

f) start-up circuits.

REFERENCES

[1] Gigabit Optical Link Transmitter manual. Available at http://proj-gol.web.cern.ch/proj-gol/manuals/gol_manual_0.1.pdf

[2] M. Vandepas, K. Ok, A.N. Nemmani, M. Brownlee, K. Mayaram, and U.-K. Moon, "Characterization of 1.2 GHz phase locked loops and voltage controlled oscillators in a total dose radiation environment," in Proceedings of 2005 MAPLD International Conference, Sept. 2005.

[3] A. N. Nemmani, "Design Techniques for Radiation Hardened Phase-Locked Loops," Master's thesis, Oregon State University, Aug. 2005.

[4] A. Nemmani, M. Vandepas, K. Ok. K. Mayaram, and U. Moon, "Radiation hard PLL design tolerant to noise and process variations," in CDADIC report, July 2004.

[5] M.A. Do, R. Y. Zhao, K.S. Yeo, and J.G. Ma, "New wideband/ dualband CMOS LC voltage-controlled oscillator," in Circuits, Devices and Systems, IEE Proceedings Volume 150, Issue 5, 6 Oct. 2003 Page(s): 453-9 –

[6] T.P. Liu, "A 6.5 GHz monolithic CMOS voltage controlled oscillator," ISSCC Digest of Technical Papers, San Francisco, USA, Feb. 1999, pp. 404-405

[7] E. Hegazi, H. Sjoland, and A. A. Abidi, "A filtering technique to lower LC oscillator phase noise," IEEE J. Solid State Circuits, vol. 36, no. 12, pp. 1921-1930, Dec, 2001.

[8] U. Singh, and M. Green, "Dynamics of high frequency CMOS dividers," Proc. ISCAS 2002, pp. 421-424.

[9] D. Pan, H. W. Li, B. Wilamowski, "A Radiation-hard phase-locked loop," ISIE Industrial Electronics, IEEE, vol.2, pp. 901-906, June 2003

[10] J. P. Colinge, “Hardening Integrated Circuits Against Radiation Effects,” Short Course.

[11] J. Maneatis, “Low-jitter process-independent DLL and PLL based on self-bias techniques,” IEEE J. Solid-State Circuits, vol.31, pp. 1723-1732, Dec. 1993.

[12] M. Vandepas, “Oscillators and Phase Locked Loops for Space Radiation Environments,” Master’s thesis, Oregon State University, Aug. 2005

[13] F. M. Gardner, “Charge pump phase locked loops,” IEEE Transactions on Communications, vol. CMO-28, pp. 1849-1858, Nov. 1980.

[14] F. M. Gardner, Phaselock Techniques, John Wiley and Sons, 2005

[15] B. Razavi, RF Microelectronics. Prentice Hall, 1998.

[16] T. H. Lee. The Design of CMOS Radio-Frequency Integrated Circuits. Cambridge University Press, Cambridge, 1998.

[17] B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill, 2001

[18] R. B. Staszewski, C. M. Hung, N. Barton, M. C. Lee, D. Leipold, “A Digitally Controlled Oscillator in a 90nm Digital CMOS Process for Mobile Phones,” IEEE J. Solid State Circuits, vol. 40, no. 11, pp. 2203-2211, Nov. 2005.

[19] Space Radiation Effects on Microelectronics. Available at http://parts.jpl.nasa.gov/docs/Radcrs_Final.pdf.

[20] W. B. Kuhn, X. He, M. Mojarradi, “Modeling Spiral Inductors in SOS Processes,” IEEE Transactions on Electron Devices, vol.51, no. 5, May. 2004.

BIOGRAPHICAL INFORMATION

Jer-Fu Dennis Wu received the degree in electronics engineering from National Taipei University of Technology, Taiwan, in 1998. He began his graduate studies in the School of Electrical Engineering at the University of Texas, Arlington in the Fall of 2004 and joined the Integrated Circuit Design And Reliability Lab (ICDAR) in Dec 2005. He became a Member of IEEE since 2001.

He joined TI Taiwan in 1999 as a MSP product engineer and focused on the yield improvement and the test time reduction. From 2000 to 2005, he was with the Mixed Signal Wireless Custom Product Group in Wireless Terminal Business Unit of Texas Instrument Inc., Dallas, TX, where he was a Make Member of Technical Staff (MMTS) working on the semiconductor multi-site testing and new product development. His current research interests include LC VCO, frequency synthesizers, mixed-signal integrated circuits, and radio-frequency integrated circuits for wireless and optical communications.