THERMO-MECHANICAL ANALYSIS OF A 3D PACKAGE IN MICROELECTRONICS AND COOLING TECHNOLOGIES FOR AN IGBT THERMAL TESTER IN POWER ELECTRONICS

by

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ABSTRACT

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In the past, compact components such as chip scale packages and flip chip packages were the work horses of miniaturization. However emerging applications are now demanding even higher packaging density which has led to the evolution of 3D packaging, some of the advantages being minimal conductor length, reduce speed limiting inter chip interconnects. This has resulted in the emergence of 3D packaging technologies like stacked package, through silicon vias (TSV), package on package (PoP) etc. In order to address the various challenging requirements, PoP is seen as the leading 3D packaging platform by the system designers and semiconductor suppliers. PoP is primarily stacking one package on top of the other. Depending on the power, due to the torturous heat flow path, it can result in high temperatures of the packaged die and the thermal specifications of the package can be easily exceeded. Due to its complex architecture, reliability related to thermo-mechanical issues is another challenge in the design of PoP. Hence Part-1 and Part-2 of the thesis lays the impetus on the thermal and thermo-mechanical analysis of a commercially available PoP.

Power semiconductor devices are the essential components determining the efficiency, size and cost of electronic systems for energy conditioning. As the power density continues to increase and the product form factors continues to shrink, thermal management technologies and their applications early in the product design process is extremely important. Alternative thermal cooling technologies such as thermoelectric cooling and thermal diodes are being explored that provide precision cooling and heating in complex operating conditions to modular platforms like air conditioning, liquid and direct contact designs. Part 3 of the thesis focuses on the development of an insulated gate bipolar transistor (IGBT) thermal tester where thermal cycling is performed on the IGBT module by coming up with an appropriate thermoelectric cooler and heat sink arrangement. IGBT's represent the most commercially advanced device of a new family of power semiconductors synergizing high input impedance MOS-gate control with low forward voltage drop bipolar conduction. They are 3 terminal power semiconductors noted for high efficiency and fast switching.

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CHAPTER 1

INTRODUCTION

1.1 Introduction to Electronics Packaging

A back-end process that results in the transformation of bare integrated circuits (IC) into functional products is conventionally known as electronic packaging [3]. For a particular electronic package, any architecture/system design chosen is a compromise between the electrical, mechanical and environmental requirements for the package as well as reliability and cost targets [4]. As the IC feature size decreases and the size of silicon wafer increases, the cost per IC is reduced and the performance is enhanced. The future IC chips will be larger in size, have more input/output terminals (I/Os) and require higher power. In addition to the advancements in IC technology, low cost, small size and multi-functional electronic products are important drivers for the electronic packaging market. In response to these requirements, packaging related areas such as design, packaging architectures, materials, processes and manufacturing equipment are all changing at a fast pace.

Some of the important functions of electronic packaging are protection, powering and cooling the chips and components which provide electrical and mechanical connections between these parts and the outside world [3]. The electronic components can be roughly characterized into active and passive components. Active components consume power in delivering functionality within a system whereas passive components provide connection, mechanical support, filtering, noise reduction and other functions which are critical to the performance of the active devices.

The electronic packaging technology has evolved from a simple metal can and soldered metal wiring to complex multilayer ceramic and organic structures depending on the applications (medical applications, automotive electronics, optoelectronics, military and

consumer) with provision of proper hermeticity and improved thermal and electrical performance [3].

1.2 Packaging Levels

In order to develop a thermo-mechanical design for a specified electronic product, it is important to know the different packaging levels. The packaging hierarchy is divided into three structural levels:

1. First / Device level package: Chip into single chip modules (SCM) or Multichip modules (MCM).
2. Second / Package level package: Components (SCMs, MCMs, Connectors, etc.) on a printed circuit board (PCB).
3. Third / System level package: PCB assemblies, cables, power supplies, cooling systems and peripherals into a frame or box.

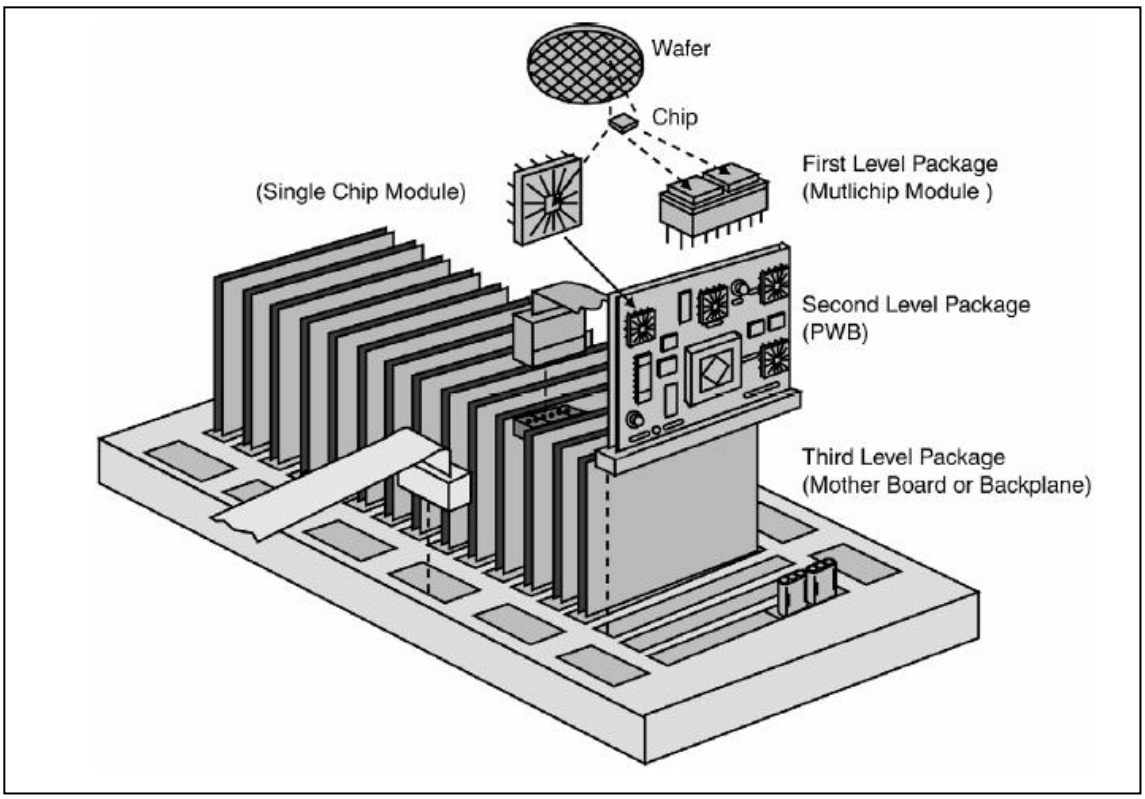


Figure 1.1 Packaging Hierarchies [1]

The chip or the IC is extracted from the wafer and is then placed on an individual container or carrier as a SCM or a MCM which houses and protects the chip. This is known as the first level package. The package is then assembled onto a larger PCB which is usually a card or a board. The board not only carries these components on top and below but also interconnects every component with conductor wiring to form an interconnected system. This is known as the second level package. In order to manage large amounts of data, sometimes connectors and cables typically connect several boards together to make the entire system. This is known as the third level package. For the optimal and reliable working of the electronic products different thermo-mechanical techniques could be implemented based on the level of the package [2]. Figure 1.1 shows the packaging hierarchies with the different structural levels.

1.3 Power Trends in Electronics

In 1965, Gordon E. Moore published a paper “Cramming more components onto integrated circuits” which stated that the number of transistors that can be placed inexpensively on an integrated circuit will increase exponentially doubling every 18 to 24 months, figure 1.2. The trend has continued for more than half a century and is expected to continue for at least another decade or so [5]**.** Figure 1.3 shows the power trend for high end chips. The chip power has increased and will keep on increasing in the coming years. As a result some of the challenges faced in the electronics packaging industry that limits its technological development would be the thermal management and its mechanical reliability.

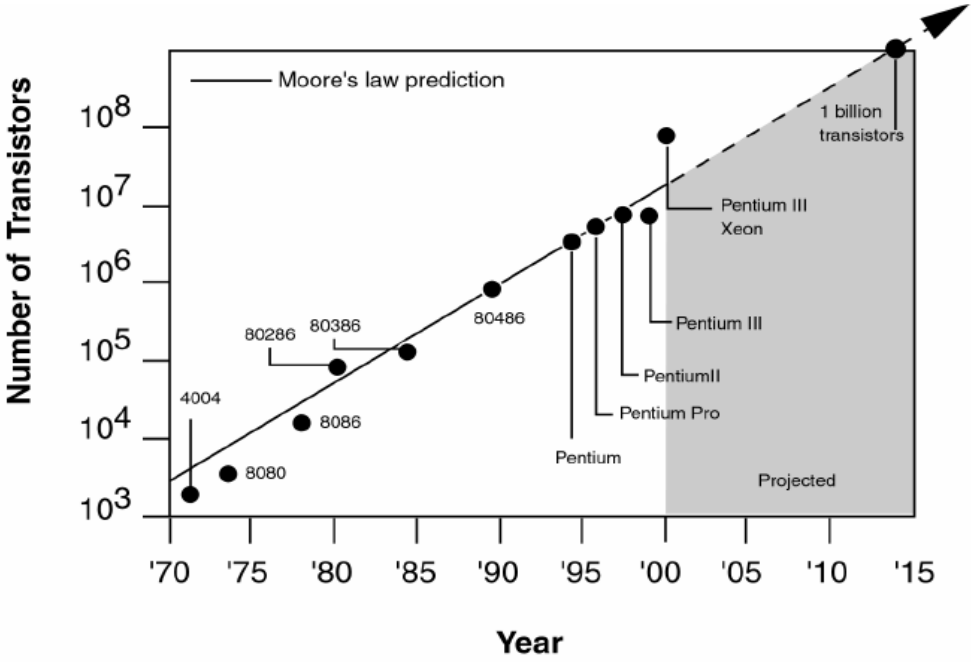


Figure 1.2 Moore's Law [1]

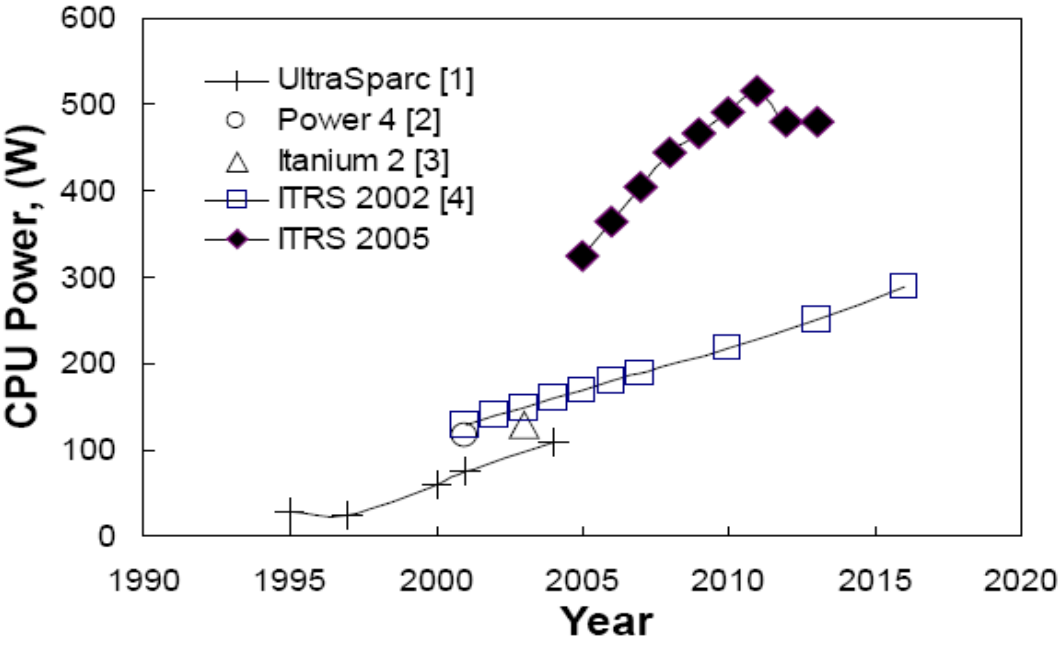


Figure 1.3 High End Chip Power Trends [6]

1.4 Thermal Management

In recent years, heat-sensitive electronics systems have been miniaturized far more than their heat-producing power supplies leading to major design and reliability challenges and making thermal management a critical design factor. There are three basic issues at the core of effective thermal management - how and where the heat is generated; how the temperature at a given point in the circuit is determined; and how the heat is removed [7]. Thermal management may employ different modes of heat transfer at different levels.

1.4.1 First / Device Level Cooling

The first / device level that forms the bottom of the packaging hierarchy comprises of the chip package that houses and protects the chip. Conduction of heat from the chip to the package surface and then into the printed wiring board is the primary concern for the thermal management at this level. In order to lower the chip temperature, reduction of thermal resistance between the die and the package surface would be the most effective way. This reduction in temperature can be brought about by using die attach adhesives with high conductivity, thermal greases. The cooling can be brought about by active cooling techniques such as by using heat sinks, jet impingement and dielectric liquids etc [1].

1.4.2 Second / Package Level Cooling

The second / package level comprises of the printed circuit board where the heat removal occurs by conduction in the printed circuit board and by convection to the ambient air. Printed circuit boards with high thermal conductivity with heat sinks or heat pipes attached to the back side are some of the ways to take away the heat from the printed circuit board. Some of the other ways by which heat can be removed from the printed circuit board would be by fans or blowers that create internal air flow loops [1].

1.4.3 Third / System Level Cooling

The third / system level comprises of the motherboard which interconnects the printed wiring. Active thermal control measures such as air handling systems, heat pumps, refrigeration

systems are some of the thermal management criteria's at this level. The cooling of the rack or module can be done by the natural circulation of air depending on the application [1]. So the thermal aspects of third / system level cooling are the thermodynamic considerations, overall system balance and the application [8].

1.5 Mechanical Reliability

In the context of this overview reliability is defined as the ability of a device to conform to its electrical/visual or mechanical specifications over a specified period of time under specified conditions at a specific confidence level. In an electronic package the reliability of solder joints are of utmost concern as they are one of the most fragile elements of a package (mainly due to the fact that they are small in size and used at high temperatures relative to the melting points). For the improvement of solder joint reliability of any electronic package there has to be a good understanding of solder joint failures [9].

Temperature fluctuations caused due to power transients or environmental changes along with the resulting thermal expansion mismatch between the various package materials results in time and temperature dependent creep deformation of solder. With repeated cycling the deformation accumulates thereby causing solder joint cracking and interconnect failure.

1.6 3D Packaging Technology

Packaging has been the "silent partner" in electronics and information advances in the last three decades. Yet the desire for increased speed, density and affordability has increased the importance of this silent partner so that in some applications the packaging of the IC is the critical enabler in meeting customer requirements [10].

An IC is complete only when it has a suitable package. A package has to provide power to the chip as well as heat dissipation path for it in addition to protecting the IC from mechanical damage from outside elements. There are different types of chip packaging technologies available of which 3-dimensional (3D) packaging is considered to be one of the most efficient.

1.6.1 3D Packaging Technology

Continuous demand for miniaturization, increased functionality, better performance and lower cost has forced the electronics industry to shift from traditional packaging techniques to advanced packaging technologies such as stacked packaging, Package on Package (PoP) etc. This has resulted in increased packaging density thereby satisfying the current requirements [11]. Vertical integration of chips in a single package multiplies the amount of silicon that can be squeezed in a given package footprint and more data functions per cubic centimeter (cc) of application space, conserving less board real estate. In stacked packages, two or more silicon dice are stacked within a single package. Different die arrangements such as rotated, staggered, pyramid etc. are commonly adopted [12, 13]. The increasing trend of die stacking is shown in figure 1.4.

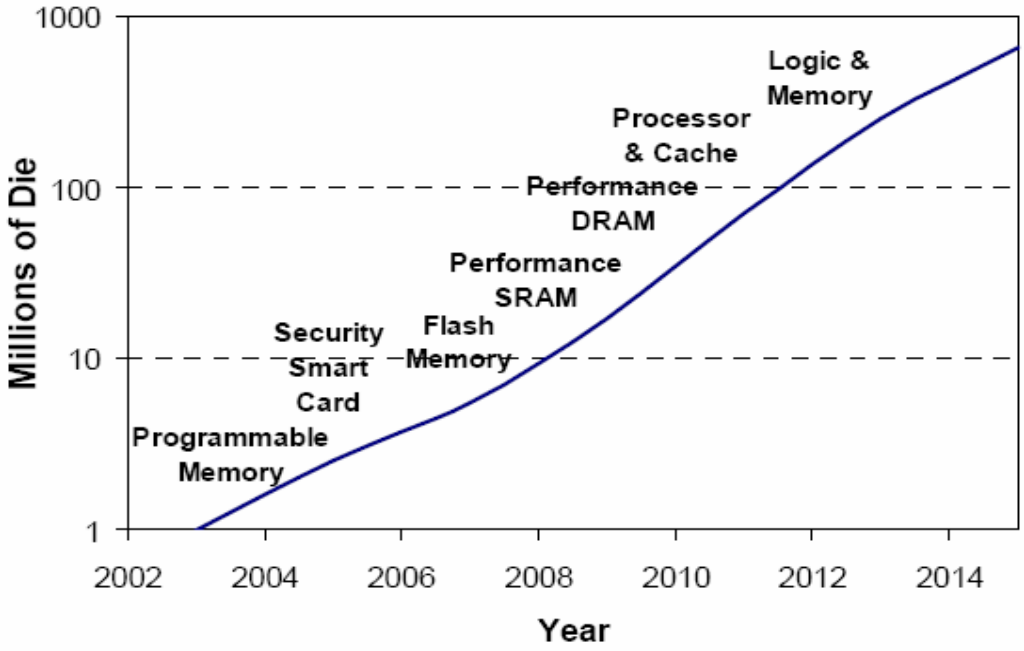


Figure 1.4 Die Stacking Trend [13]

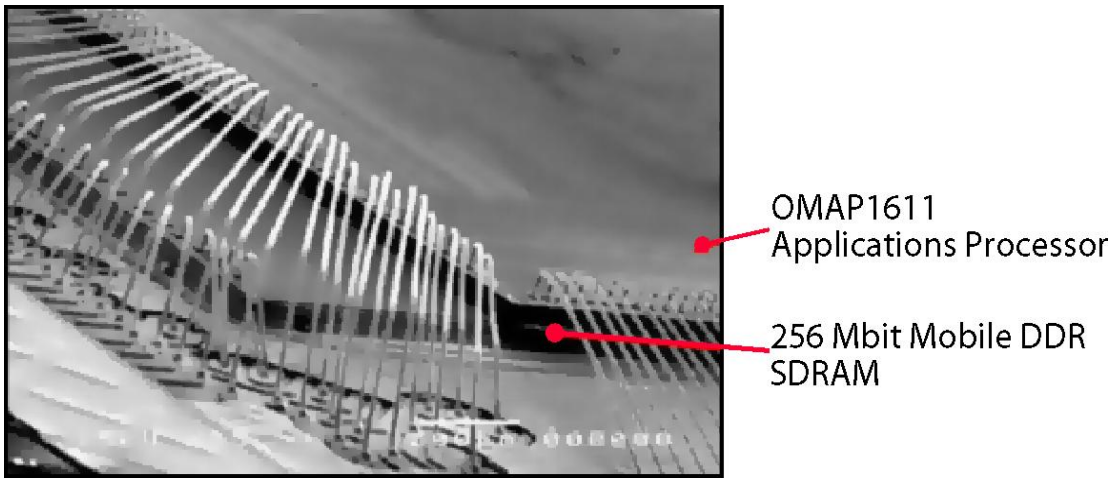
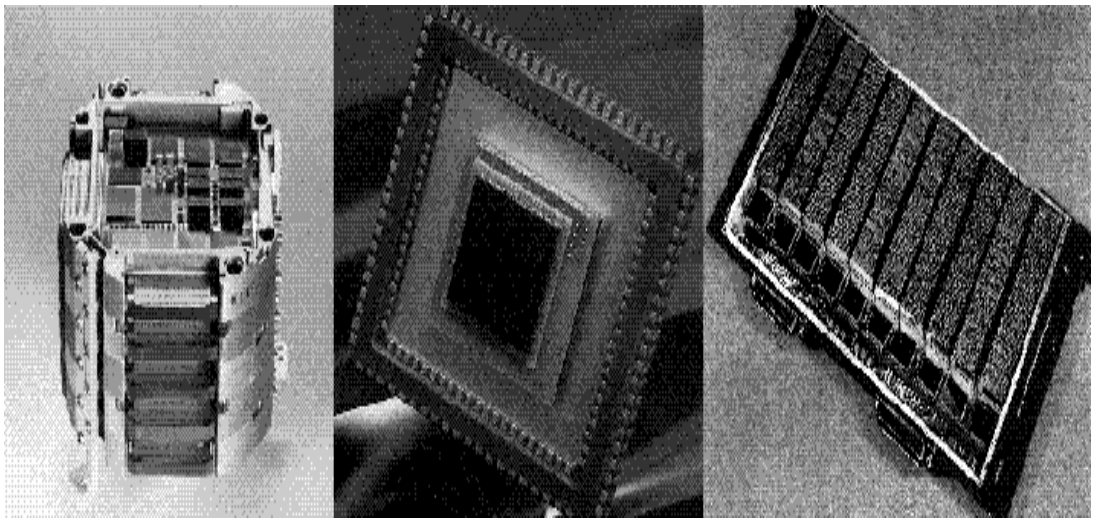


Figure 1.5 An example of 3D Architecture [14]



(a) (b) (c)

Figure 1.6 Example of 3D Packaging Technology: (a) The Aladdin parallel processor (b) Irvine's 3D smart sensor (c) TI 1.2 Gbit Solid State Recorder [15]

3D packaging technologies exploit the third or Z height dimension to provide a volumetric packaging solution for higher integration and performance. As a result 3D packaging has become critical in integrating the multi-media features and consumers demand in smaller and lighter products. This increasing functionality requires higher memory capacity in more

complex and efficient memory architectures. 3D packaging as a result is experiencing high growth and new applications by delivering the highest level of silicon integration and area efficiency at the lowest cost [16].

A microelectronic device might consist of a number of packages that are mounted near each other on a single PCB thereby consuming a lot of real estate. As a result the size of the device increases and this type of configuration is referred to as 2D packaging. Hence some of the drivers of 3D integration are a) Interconnection in the third dimension which results in reduced chip area producing better yields and shorter global interconnection which gives better performance. (b) Logic plus memory: 2D interconnect results in long interchip connections between logic and memory, SOC solutions results in large die and intrachip connections whereas 3D with through silicon vias provides the shortest interconnect between logic and memory functions [17].

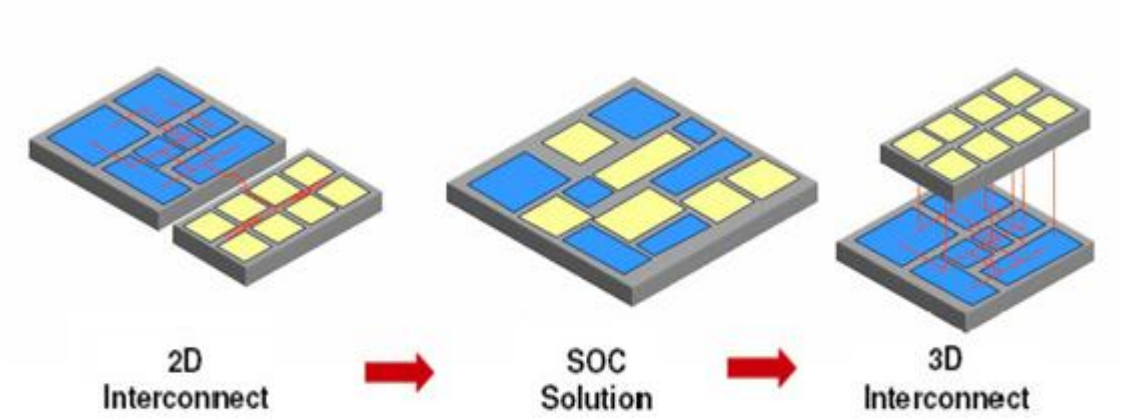


Figure 1.7 2D Packaging to 3D Packaging [17]

Based on the interconnects, the packages can be classified as wire bond package, flip chip (FC) package, ball grid array package (BGA) and chip scale package (CSP). These packages have their applications depending on the requirement. In wire bond packages, the wire bonds are the primary method of making interconnections between an IC and a PCB during semiconductor device fabrication. Although less common, wire bonding can be used to

connect an IC to other electronics or to connect from one PCB to another. It is generally considered the most cost-effective and flexible interconnect technology and is used to assemble the vast majority of semiconductor packages. Bond wires are usually of one of the following materials: aluminum, copper or gold. The wire diameters start at 15 µm and can be up to several hundred micrometers for high-powered applications [5].

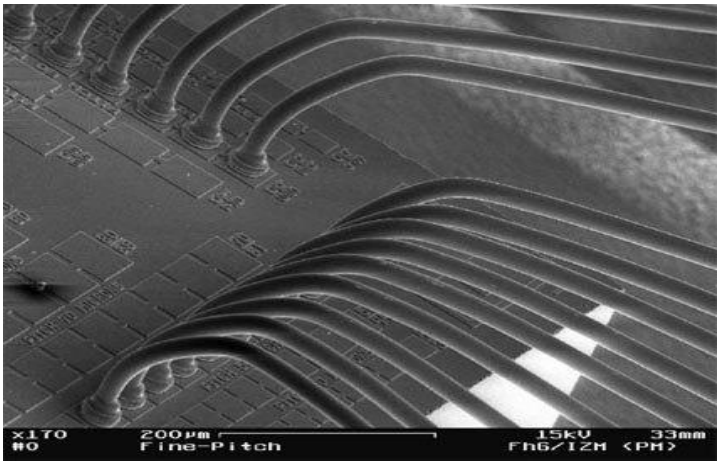


Figure 1.8 Wire Bonding [18]

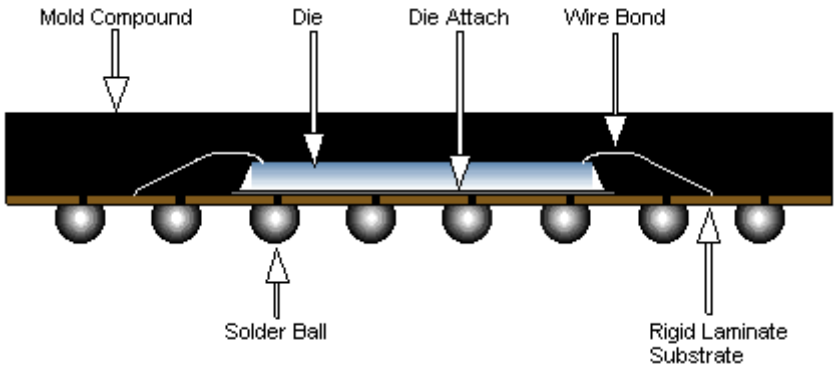


Figure 1.9 Wire Bond Package [16]

In flip chip packages, the interconnection between the die and the carrier is made through a conductive "bump" that is placed directly on the die surface. The bumped die is then

"flipped over" and placed face down with the bumps connecting to the carrier directly. Once the die is soldered, underfill is added between the die and the substrate. Underfill is a specially engineered epoxy that fills the area between the die and the carrier, surrounding the solder bumps that are designed to control the stress in the solder joints caused by the difference in thermal expansion between the silicon die and the carrier [16].

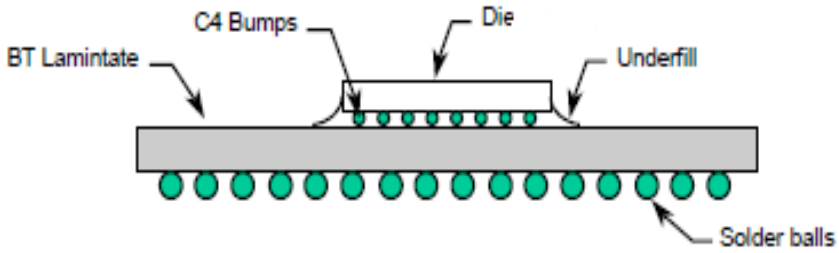


Figure 1.10 Flip Chip Package [19]

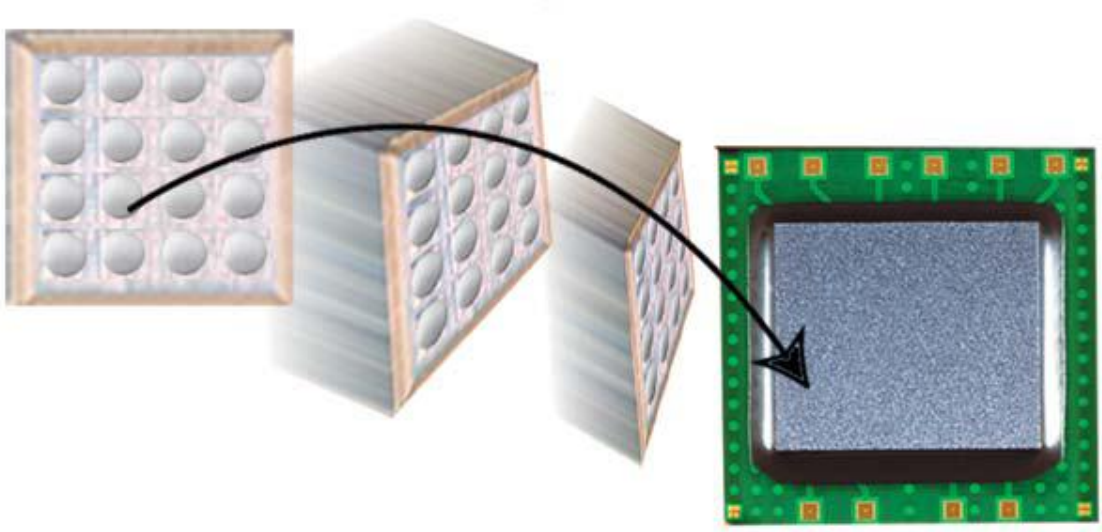


Figure 1.11 Flip Chip Package Arrangement [16]

Ball Grid Array or BGA is a surface-mount package that utilizes an array of metal spheres or balls as the means of providing external electrical interconnection. The balls are composed of solder and are attached to a laminated substrate at the bottom side of the package. The die of the BGA is connected to the substrate either by wire bonding or flip-chip connection. The substrate of a BGA has internal conductive traces that route and connect the die-to-substrate bonds to the substrate-to-ball array bonds. The main advantage of BGA as a packaging solution for integrated circuits is its high interconnection density, i.e., the number of pins (or balls, rather) that it offers per given package volume is high. A related advantage arising from this high I/O density is its small board space occupation [9].

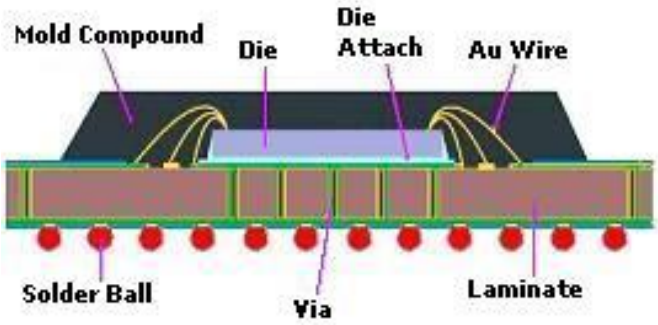
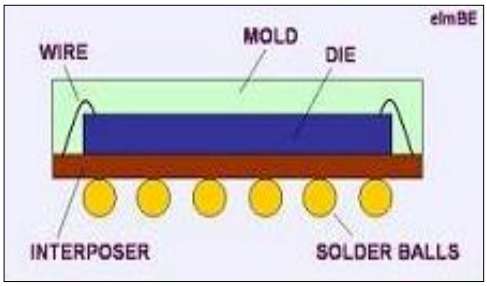


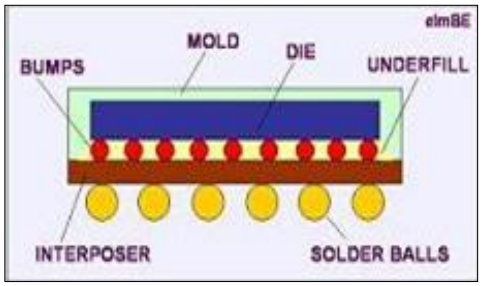
Figure 1.12 Cross Section of a BGA Package [9]

Figure 1.13 Examples of BGA Packages [9]

A chip scale package or CSP is a type of integrated circuit chip carrier where the package area is no greater than 1.2 times of the die and it must be a single die. To qualify a package as a CSP its ball pitch should me no more than 1 mm [5].



(a) Cross Section of Wire Bond CSP



(b) Cross Section of Flip Chip CSP

Figure 1.14 CSP Packages [9]

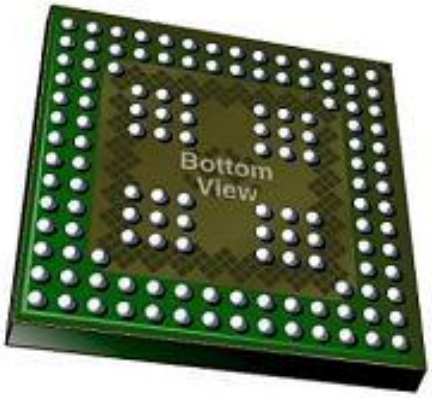


Figure 1.15 Bottom View of a CSP Package [20]

1.6.1.1 Benefits of 3D Packaging Technology

In the webcast, “Ultra Thin Wafer Processing Solutions” [21] and one of the white papers by Waytronx, Inc. [22], Steven Koester from CMOS technology at IBM, East Fishkill, N.Y. noted that “3D Integration will establish a new scaling path that will extend Moore’s Law beyond its expected limits”. Based on this, 3D packaging has the following benefits.

1. Shorter Interconnects:

The wiring does not scale down the way transistors do as the width of the wires is reducing but not its length. Hence stacking of dice is a feasible solution that can allow interconnects to go between the dice thereby reducing their lengths upto 1000 times.

2. Increased System Performance:

In order to keep the system performance close to on-chip performance, high speed interconnections are necessary. 3D packaging can shorten communication paths, increase bus speeds and open up performance through economic parallel, fabric communications.

3. Reduction of Size and Weight:

3D packaging allows 40-50% reduction in weight and size and 5-6 times reduction in volume compared to conventional packaging [23].

4. Reduction of Signal Time Delay:

Shorter interconnection length and closer proximity of electronic components helps to reduce the signal time delay [24].

5. Reduce Power Consumption:

Boosting signals and combating low signal to noise in high speed chip interconnections takes away a significant percentage of system power.

6. Faster Time to Market:

By stacking the chips together, known good functions from the previous generation IP can be quickly integrated to achieve faster time to market, thereby reducing the development and engineering costs. Also the system functionality can be proven prior to production.

7. Speed:

Power saving achieved using 3D technology allows the 3D device to run at a faster rate of transitions per second with no increase in power consumption [25].

1.6.1.2 Limitations of 3D Packaging Technology

In any technology there are some tradeoffs that need to be performed for efficient operations. Some of those in 3D packaging are as follows.

1. Design Complexity:

Although Moore's law when applied to IC design lasts for approximately 18 months, the size of wafers have been increasing at a faster rate than the present 3D technology allows for.

2. Thermal Management:

Thermal management is a very important factor in designing of 3D packages because of high power density.

3. Design Software:

This is one of the problem areas for 3D packaging as most of the design tool kits used are limited to manufacturers rather than having universal access. There is a need for the manufacturers to put their design rules in a format that is available in the popular design tools which would make it easily accessible to the designers [26].

4. Microwarming:

Microwarming starts at the transistor level and protracts to the integrated environment within and surrounding advanced devices. It is pervasive in every level of digital integration [22].

1.6.2 Different Types of 3D Packaging Technology

Increased functionality in a smaller area, high performance computing are some of the reasons for the development of 3D packages. They can be classified as stacked packages, Package on Package (PoP), Package in Package (PiP), Through Silicon Vias (TSVs).

Stacked die packaging is a packaging technology where two or more dice are stacked in a single package or multiple packages. Some of the benefits observed as a result are as follows:

- Smaller, thinner and lighter packages
- Reduced packaging costs and components
- Reduced system level cost for system in package (SiP) vs. System on Chip (SoC)
- Reduced system level size due to smaller footprints and decreased component count [27]

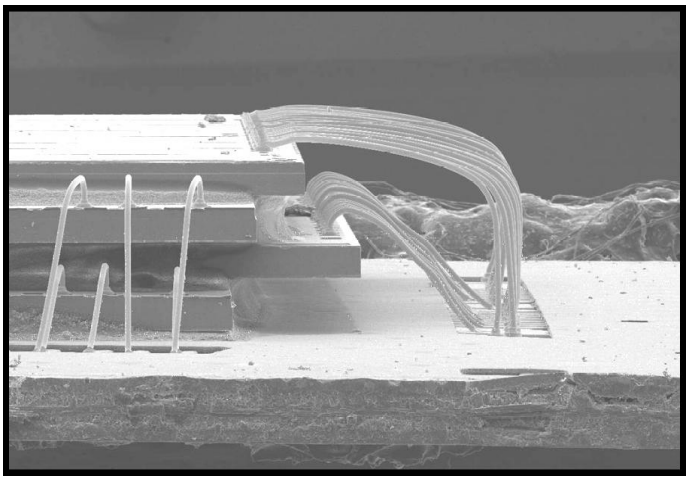


Figure 1.16 Stacked Package [17]

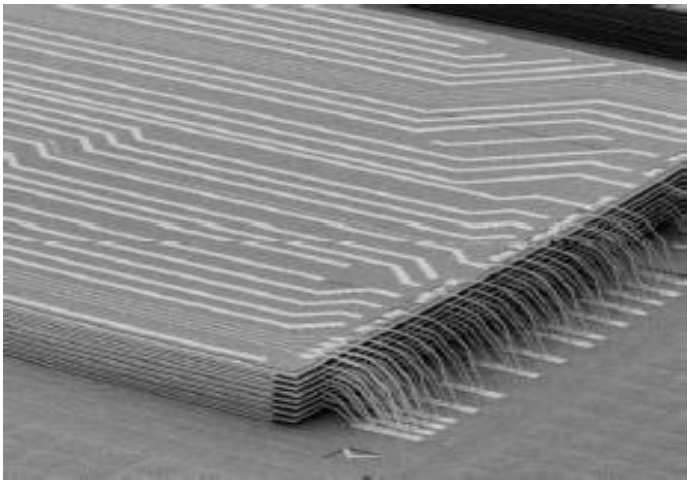


Figure 1.17 Stacked 16-Die Package [17]

Stacked package have four different type of architectures and they are divided as pyramid, rotated, spacer and staggered.

Package on Package (PoP) has emerged as the vertical stacking solution to stack logic processor with memory due to its testability, business flow and configuration flexibility issues. The PoP solution typically consists of the logic processor in the bottom package and the

memory device in the top package. PoP stacks discrete packages thus enabling greater flexibility of signal routing and resolve known good die (KGD) issue.

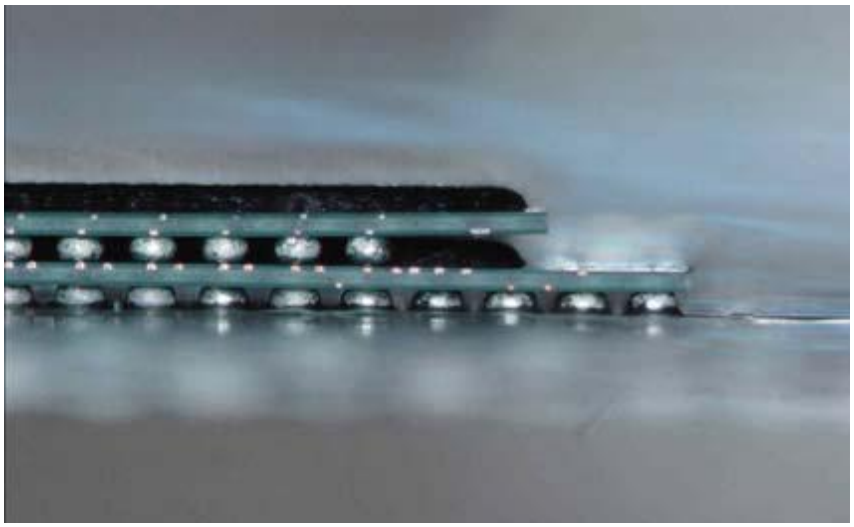


Figure 1.18 Amkor's PoP [16]

New PoP design include 2 to 4 stacked memory dice in the top package and 1 or 2 logic dice in the bottom package [28].

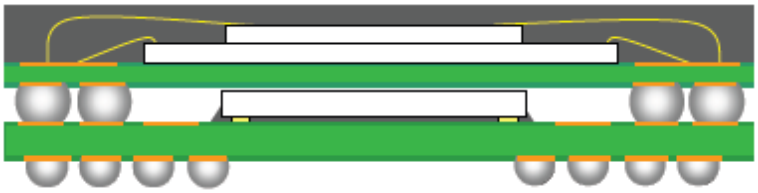


Figure 1.19 Flip Chip PoP [16]

The advantage in PoP is that since it has two different packages, if one of the packages goes bad, then there is no need to throw the PoP but only the bad package can be disposed. Some of the applications are digital cameras, mobile handsets, MP3 players.

Comparing stacked package and PoP we see some of the advantages and disadvantages.

Table 1.1 Stacked CSP vs. Package on Package – trade-offs [29]

	Stacked CSP	Package on Package
Advantages	• Low package profile. • SMT line infrastructure. • Low packaging cost.	• OEM ownership. • Flexible package selection- can stack packages from different suppliers and hence more application. • Testing is done at individual level hence the product yield is very high.
Disadvantages	• KGD required for high product yield. • New development needed to change stacked device. • If stacked package fails one loses two or more dies and subsequent components hence low yield.	• High package profile. • Infrastructure for package stacking.

Package in Package (PiP) has two or more packages assembled together and overmolded so that the end result is a single package that interconnects to the product board. It is also known as stacked module package and is typically more expensive than the stacked die package but is more flexible. It allows the memory to be fully tested before assembly [17].

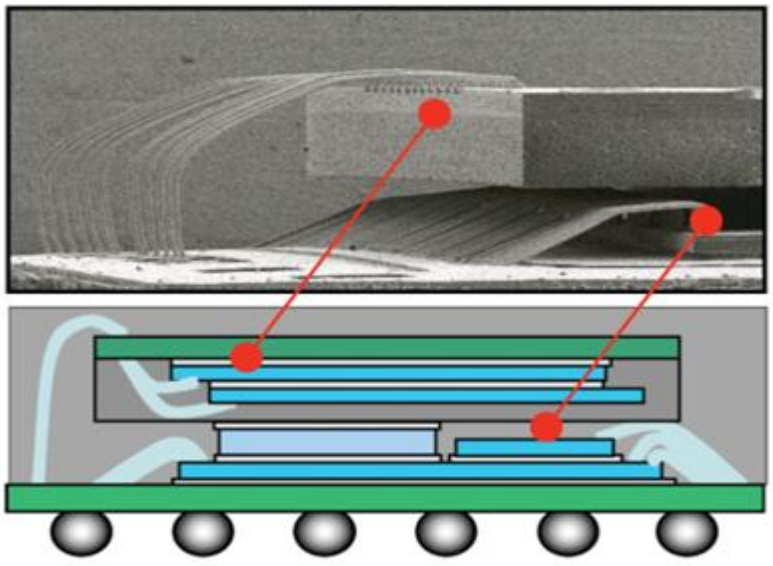


Figure 1.20 Qualcomm's PiP [17]

Through silicon vias (TSV) is the latest in a progression of technologies for stacking silicon devices in 3D. TSV refer to a 3D package that contains two or more chips (IC) stacked vertically so that they occupy less space on a PCB. In some 3D packages through silicon vias replace edge wiring by creating vertical interconnections through the body of the chips. The resulting package has no added length or width. Since no interposer is required a TSV package can be flatter than an edge wired 3D package [30].

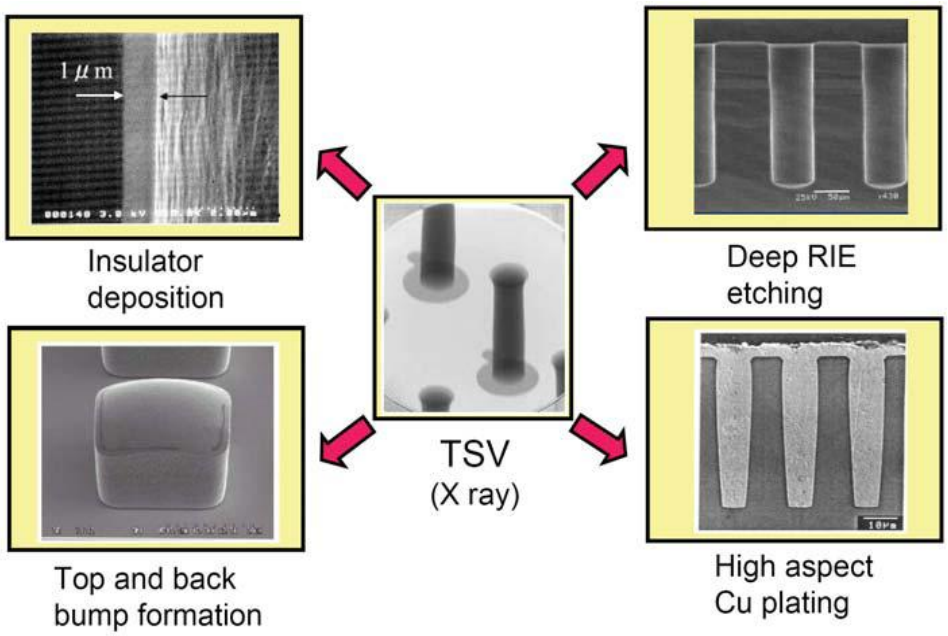


Figure 1.21 3D TSV Technologies [31]

Some of the basic technologies involved in through silicon vias are high aspect ratio, deep via formation in silicon, filling conducting material in the via. 3D chip stacking TSV technology offers the possibility of solving serious interconnection problems while offering integrated functions for higher performance.

CHAPTER 2

NUMERICAL MODELING OF A PACKAGE ON PACKAGE

2.1 Package Description

A schematic diagram of a molded ball grid array stacked Package on Package (PoP) model whereby thermal analysis and thermo-mechanical reliability of the package is carried out is shown in figure 2.1. The PoP consists of two packages, one package mounted on top of the other package.

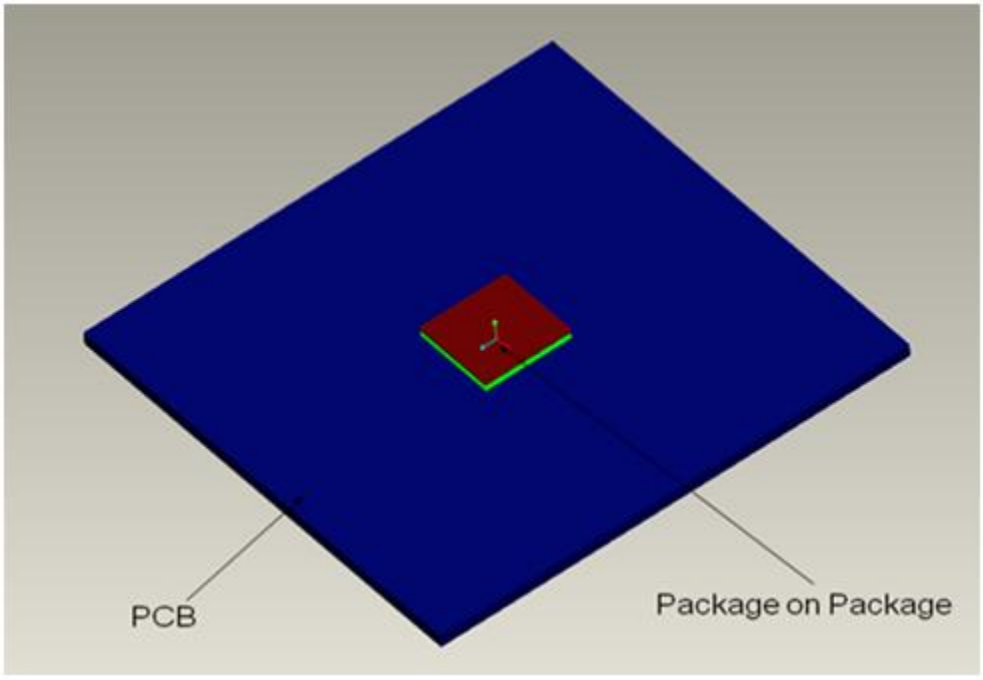


Figure 2.1 CAD Model – Package and PCB

The top package is a wire bonded package which consists of two memory dice stacked on each other having a pyramid formation. The two memory dice are separated by attaching two die attaches, the top die attach between the two memory dice and the bottom die attach

between the lower memory die and top substrate. Both the die attaches have a thickness of 0.0318 mm each. The electrical interconnections are achieved via wire bonds. A mold cap is considered for the top package in order to protect it from external contaminants, moisture or mechanical damage.

The bottom package which is a flip chip package has its die (logic) with its active side down mounted on the bottom substrate via a fully populated solder ball matrix with a ball count of 23 x 23. These solder balls are referred to as C4 interconnects as shown in figure 2.2. The ball pitch for C4 interconnects is 0.3 mm with a diameter of 0.14 mm and height of 0.1 mm.

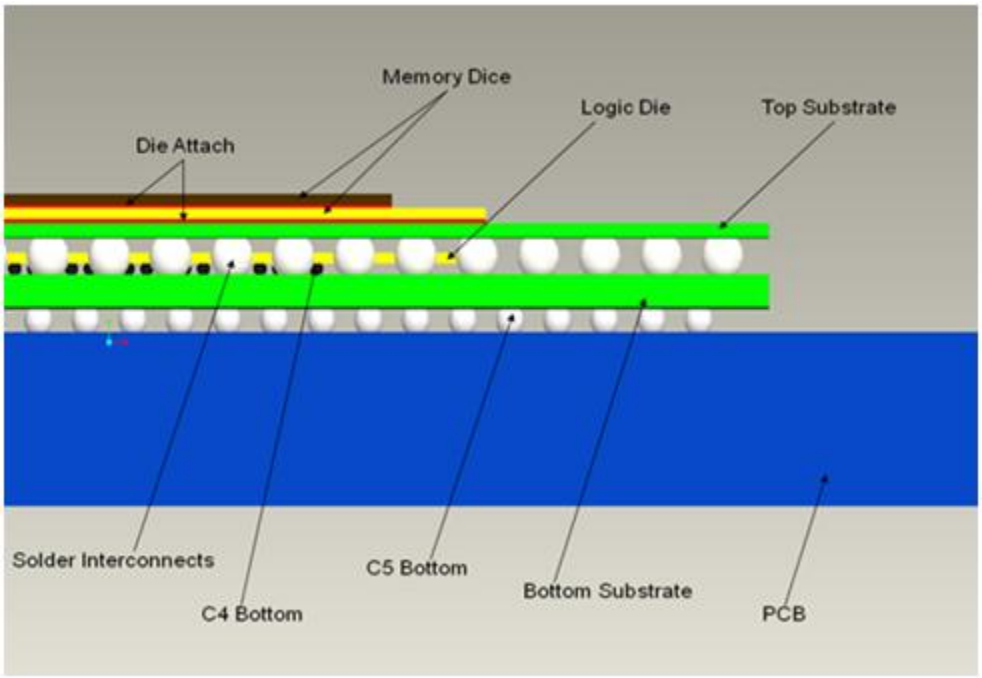


Figure 2.2 Schematic Representation of the PoP
(Note: The molding compound is hidden on purpose)

The wire bonded stacked BGA package (memory dice) is attached to the flip chip BGA package (logic die) via solder balls that have a height of 0.32 mm and a diameter of 0.45 mm. These solder interconnects are arranged at the periphery in an array of 21 x 21 and 19 x 19.The

standoff height for the solder interconnects depend on the height of the bottom package. This forms the PoP architecture.

This PoP is mounted on the PCB via the C5 interconnects that has a fully populated matrix of 23 x 23. The dimensions are: the standoff height is 0.21 mm, the diameter and the ball pitch are 0.3 mm and 0.5 mm respectively.

A single layer PCB of size 76 mm x 76 mm x 1.57 mm as per the JEDEC standards is modeled along with the package representing the test board. The 14 mm x 14 mm BGA package is positioned at the center of the PCB.

Other packaging attributes are summarized in table 2.1. Figure 2.2 shows the detailed view of the PoP. The details of the package were taken from Amkor's Package Stackable Very Thin Fine Pitch BGA (PSvfBGA) [16].

Table 2.1 shows the package dimensions considered for the modeling.

Table 2.1 Package Dimensions

Component	Memory Package [mm]	Bottom Package [mm]
Substrate	14 x 14	14 x 14
Substrate Thickness	0.13	0.3
Die	6 x 6 / 8 x 8	7.62 x 7.62
Die thickness	0.1 / 0.1	0.1
Die attach thickness	0.0318 / 0.0318	NA
Mask thickness	0.0175	0.0175
Solder ball diameter	0.457	0.14 (C4) / 0.3 (C5)
Solder ball height	0.32	0.1 (C4) / 0.21 (C5)
Solder Pitch	0.65	0.3 (C4) / 0.5 (C5)
Ball Count	152	529 (C4) / 676 (C5)

2.2 Modeling Methodology

The geometries are modeled as “Parts” using Pro/Engineer Wildfire 3.0 as a CAD tool. Then an “Assembly” is created using these parts. This ensures accurate material property assigning and material continuity of each component. This Pro/E assembly file is then imported to Ansys to carry out the thermal analysis of the PoP for the first part of the study and similarly imported to Ansys to carry out the stress analysis on the PoP for the second part of the study. Owing to the symmetric nature of the problem, an octant model is considered for both the thermal and thermo-mechanical analysis of the PoP. Once the octant model is generated, material properties are assigned to the respective components. Figure 2.3 shows the octant model considered for the study.

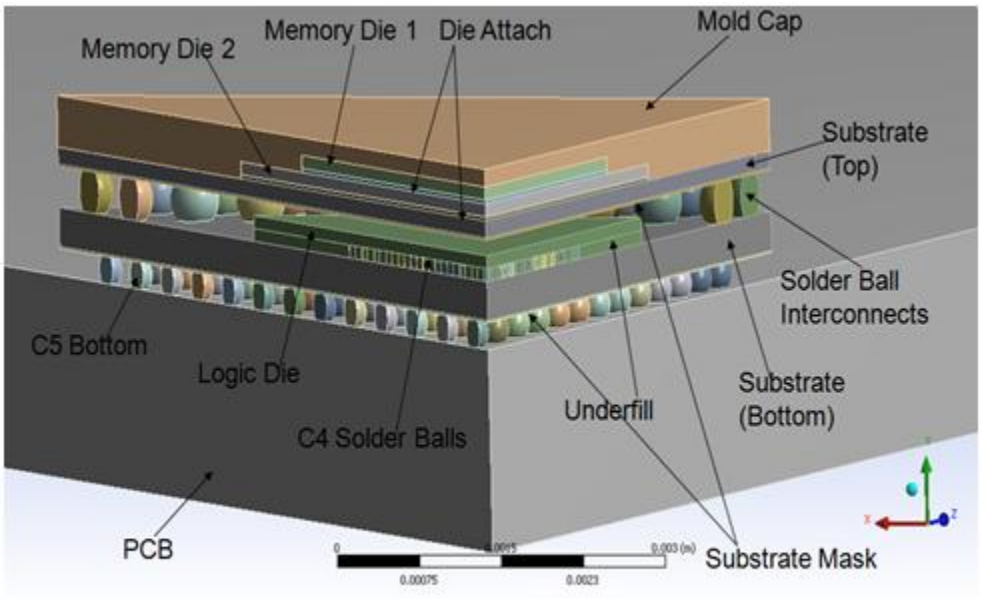


Figure 2.3 Octant model of PoP

PART-1

THERMAL ANALYSIS OF A PACKAGE ON PACKAGE

CHAPTER 3

INTRODUCTION

3.1 Background

In general three factors affect the thermal performance of a BGA: package and board material, package geometry and the environment conditions in which it is going to be used. More conductive the materials better the heat dissipation of the chip. A key challenge in 3D die stacking is the heat generation from the internal active layers because the power density per volume increases drastically in 3D. Thermal design is more complex in 3D IC's as compared to 2D IC's because the heat flux increases proportionally to the number of active layers [30]. Hence thermal management should be considered during package selection for high reliability.

Previously, researchers have performed modeling and thermal simulation of various stacked packages. These include package in package, die stacked package, different architectures in die stacked packages, multi chip modules (MCM), multi chip package (MCP) [13, 27, 32-38]. These involved mainly memory die or memory die and logic die packaged separately and stacked on top of one another. Hence a PoP was considered for this study where thermal analysis is performed. The PoP considered for the thermal analysis has a stacked package which is a wire bonded two dice package and the bottom package is a logic die flip chip package.

CHAPTER 4

THERMAL ANALYSIS

In this chapter the focus is on the design approach used for the thermal analysis, the material properties assigned to the components of the package, the boundary conditions applied and the design of experiments.

4.1 Design Approach

The thermal resistance model of the PoP is as shown in figure 4.1. There are mainly two paths for the heat to dissipate to the ambient. The first path is from the stacked dice through the mold cap to the ambient. The second path is from the memory package to the substrate, through the solder balls to the PCB and then to the ambient. There are additional paths through which the heat dissipates but then they are not significant when compared to the above paths as mentioned. The additional paths can be through the wire bonds or through the sides of the package.

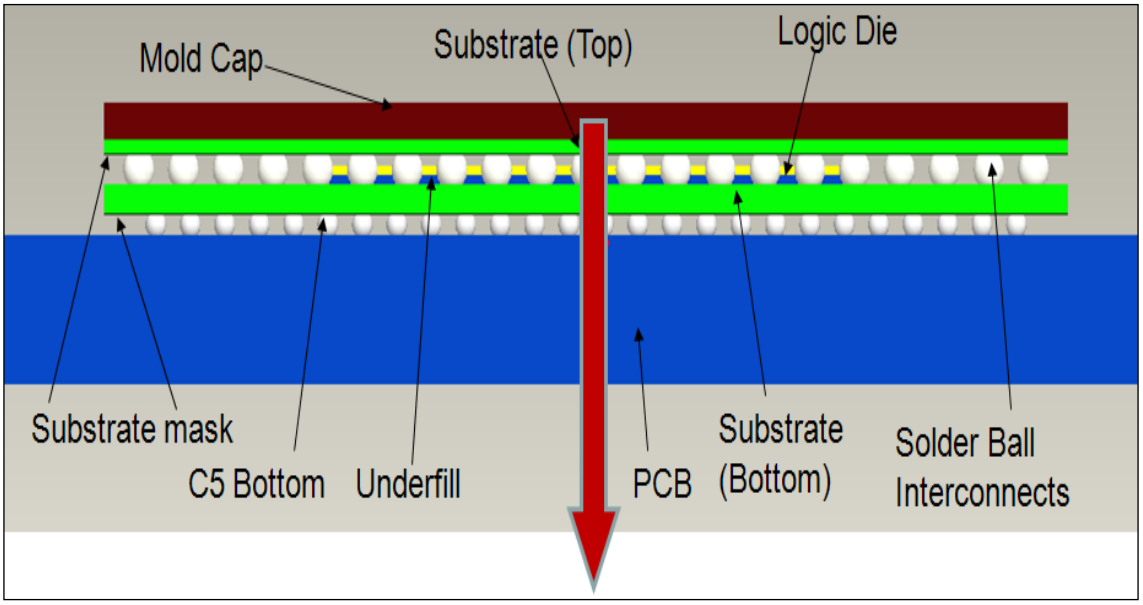


Figure 4.1 Heat Dissipation Path

About 80%-90% of the heat dissipation is through the second path i.e. through the bottom as shown in figure 4.1. This is due to the high thermal resistance of the interface between the die-mold cap and the mold-cap ambient.

The thermal resistance of the interface of the package – PCB (includes the thermal resistance of the interface for PCB – ambient) is important in determining the efficiency of the heat dissipation. This can be represented as:

$$T_j = P * (R_{pckg} + R_{PCB}) + T_a$$

$$R_{pckg} = \sum (R_{dice}, R_{datch}, R_{mold}, R_{subs})$$

The maximum power that can be dissipated through the package and the PCB to the ambient air is determined by,

$$P_{max} = ([T_j]_{max} - T_a) / (R_{pckg} + R_{PCB})$$

where $[T_j]_{max}$ is the maximum junction temperature.

So in order to reduce the junction temperature or to dissipate more power from the package, the thermal resistances of the interface between the package – PCB and PCB – ambient have to be minimized. The thermal resistance of the package depends on the size of the package and the material properties of the components that are used in the package [39].

4.2 Material Properties

For the thermal analysis of the PoP, natural convection is considered and the convection is coupled to the conduction in the package via a heat transfer co-efficient. As the conduction considered is steady, thermal conductivity is the only property that is relevant. Orthotropic property is considered for the PCB and the substrate. Heat transfer by conduction involves transfer of energy within a material without any motion of the material as a whole. The rate of heat transfer depends upon the temperature gradient and the thermal conductivity of the material.

For the last scenario, in-plane thermal conductivity of 80 W/m-K and out-of-plane thermal conductivity of 0.2 W/m-K is considered for the PCB and substrate respectively.

Table 4.1 Material Properties [13]

Component	Thermal Conductivity [W/m-K]
Die	120
Die Attach	0.3
Mold Cap	0.88
Substrate	0.418
Substrate Mask	200
Solder ball (SAC405)	57
PCB: In plane Out of plane	9 0.29
Underfill	0.8

The model is later on meshed in order to generate approximately 285,000 elements and it is ensured that the results obtained are meshing independent.

4.3 Boundary Conditions

Thermal transfer within a BGA package is primarily due to conduction which is governed by the Fourier equation. Also convection in a BGA package occurs during removal of heat away from outside of the module. It occurs between the surface of the package and a fluid or air moving over it at different velocities. Forced and natural convection are the different types of convection classified by how the fluid motion is created.

In this study a convective heat transfer coefficient of 10 W/m^2-K is applied. Ambient reference temperature of 20°C is considered.

Table 4.2 Boundary Condition

Ambient Temperature	20ºC
Heat Transfer Co-efficient	10 W/m^2-K

Heat transfer coefficient is defined on mold top, mold side, top substrate side, bottom substrate side and on top and bottom side of PCB as shown in figure 4.2.

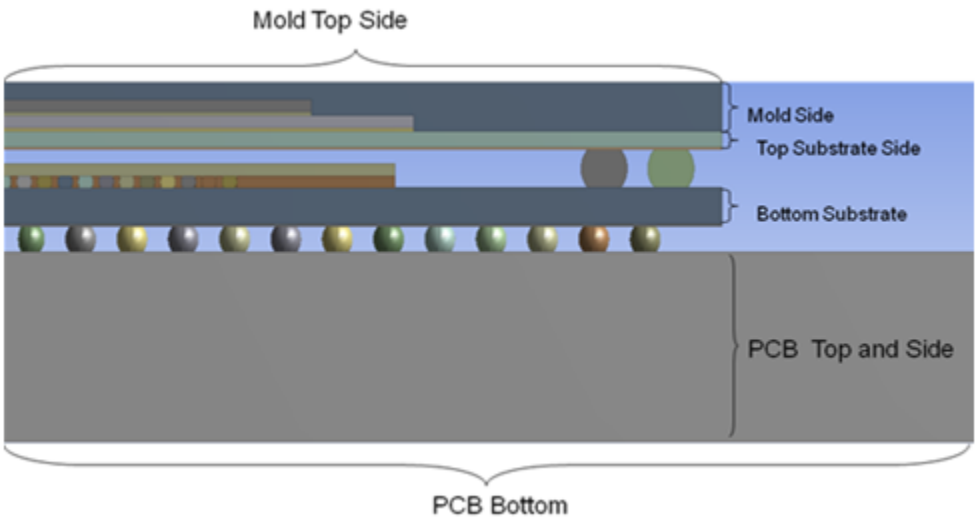


Figure 4.2 Boundary condition: locations where convective heat transfer coefficient is applied

4.4 Design of Experiments

An initial thermal analysis is conducted assuming that the bottom chip dissipates 1 W and the two memory chips dissipate 0.1 W each. Eleven different power configurations are analyzed for the thermal characterization of PoP. Table 4.3 shows the constant power levels assigned to each die.

Table 4.3 Power Levels of Each Die

Scenarios	Memory Die - Top [W]	Memory Die - Bottom [W]	Logic Die [W]
1	0.1	0.1	1
2	0.1	0.1	2
3	0.1	0.1	3
4	0.2	0.2	1
5	0.2	0.2	2
6	0.2	0.2	3
7	0.3	0.3	1
8	0.3	0.3	2
9	0.3	0.3	3
10	1	1	1
11	0.3	0.3	3

CHAPTER 5

RESULTS AND DISCUSSION

A steady state thermal analysis is performed using ANSYS. From table 4.3 it is seen that eleven different cases of power distribution is considered. The power ranges from 0.1 W to 0.3 W for the memory dice for the top package with an incremental step of 0.1 W and 1 W to 3 W for the logic die for the bottom package with an incremental step of 1 W. For each case, maximum and minimum temperatures are noted. Table 5.1 summarizes the results for all the scenarios.

Table 5.1 Temperature values of different power cases for the bottom and top package

Scenarios	**Power Cases [W]**	**T_{max} on Logic Die [°C]**	**T_{max} on Memory Dice [°C]**
1	0.1, 0.1, 1	68.6	52.9
2	0.1, 0.1, 2	112.9	73.8
3	0.1, 0.1, 3	157.3	94.7
4	0.2, 0.2, 1	72.2	64.9
5	0.2, 0.2, 2	117.1	85.8
6	0.2, 0.2, 3	161.5	106.7
7	0.3, 0.3, 1	76.9	76.8
8	0.3, 0.3, 2	121.8	97.8
9	0.3, 0.3, 3	165.6	118.7
10	1, 1, 1	106.3	160.6
11	0.3, 0.3, 3	100.8	89

From the first nine scenarios it is seen that a maximum temperature of 165.6°C is observed for the case 9 where the memory dice dissipates 0.3 W each and the logic die dissipates 3 W. The maximum temperature is noted on the logic die on the bottom package. Similarly, a minimum temperature of 52.9°C is observed for the case 1 where the memory dice dissipates 0.1 W each and logic die dissipates 1 W. The minimum temperature is noted on the memory dice on the top package.

For all the scenarios (except 10) maximum temperature is always noted on the logic die and minimum temperature is always noted on the PCB. Also, from the results it is seen that, with increase in logic die power, maximum temperature increases significantly. However, increase in memory die power, results in small increase of temperature. Figure 5.1 compares the temperature for the different scenarios. Thus, maximum PoP temperature is dominated by power on the logic die. However, when the power on memory die is compared to the logic die (case 10), the maximum PoP temperature is dominated by power on memory die. In this case, maximum temperature is noted on the memory die as seen in table 5.1. In the tenth case it is noted that when a power of 1 W each is applied on the memory dice and the logic die, a maximum temperature of 160.61°C is obtained and it occurs on the bottom memory die.

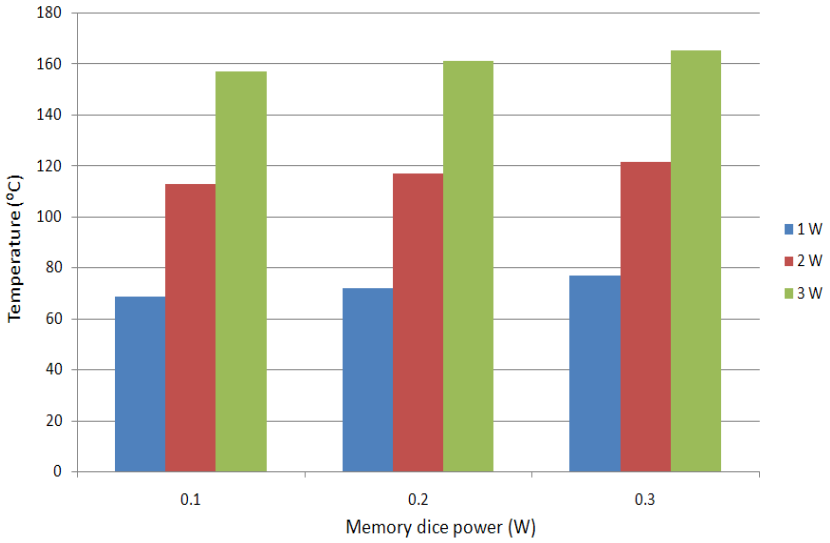


Figure 5.1 Temperature variation for various power combinations of logic and memory dice

Figures 5.2 to 5.10 shows the temperature contours for the first 9 cases and figure 5.11 show the temperature contour for case 10.

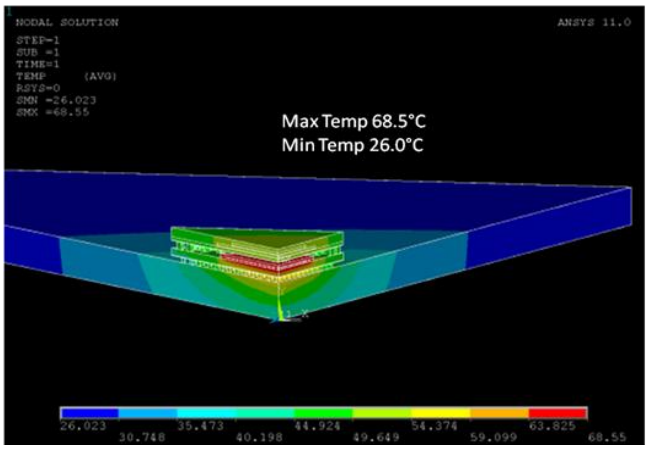


Figure 5.2 Power 0.1, 0.1 and 1W

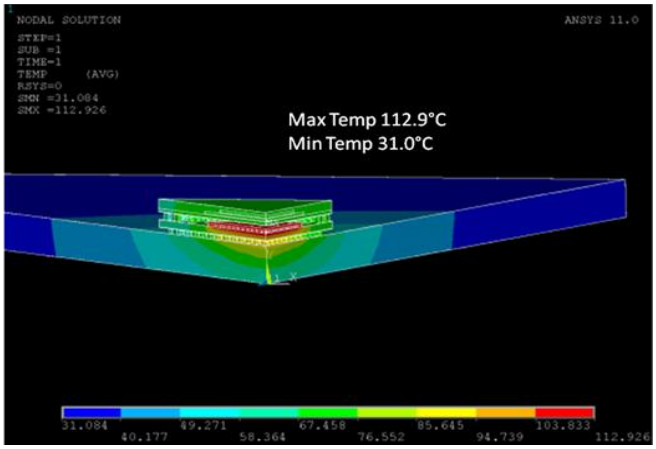


Figure 5.3 Power 0.1, 0.1 and 2W

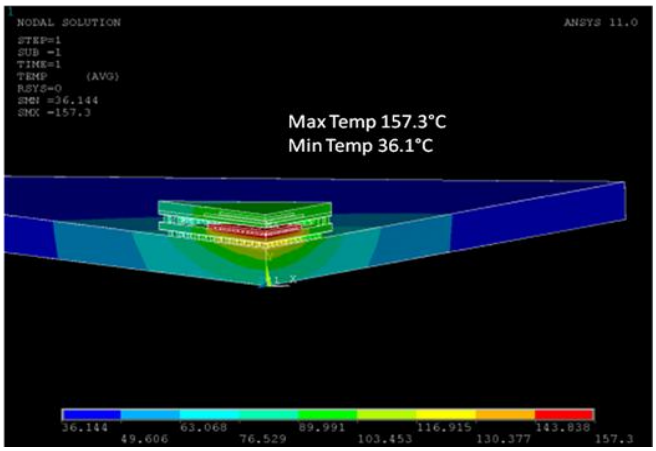


Figure 5.4 Power 0.1, 0.1 and 3W

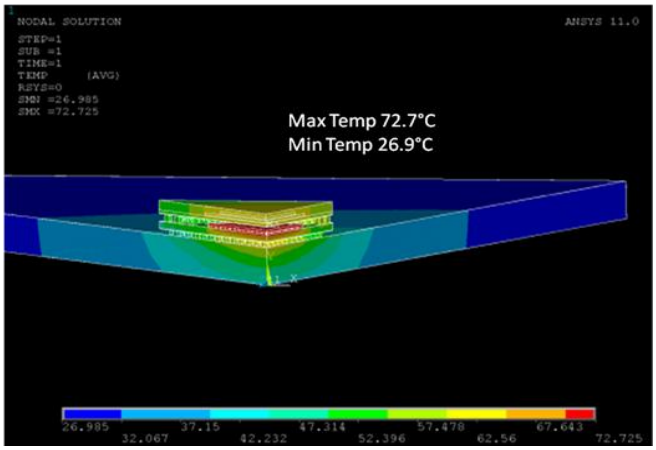


Figure 5.5 Power 0.2, 0.2 and 1W

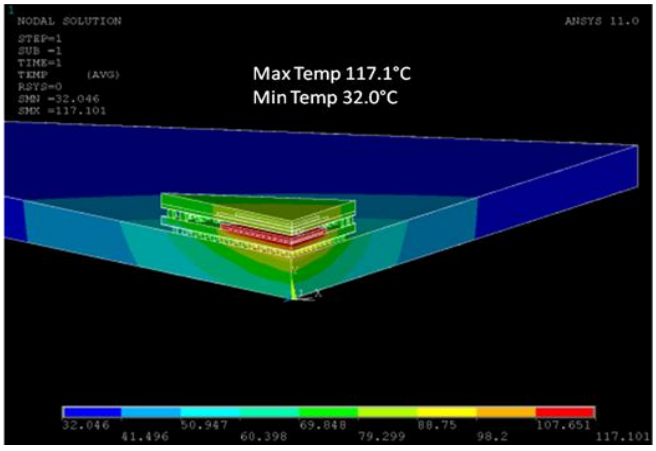


Figure 5.6 Power 0.2, 0.2 and 2W

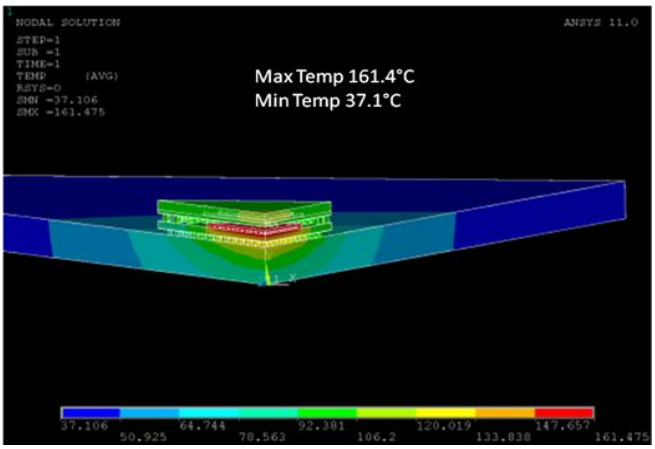


Figure 5.7 Power 0.2, 0.2 and 3W

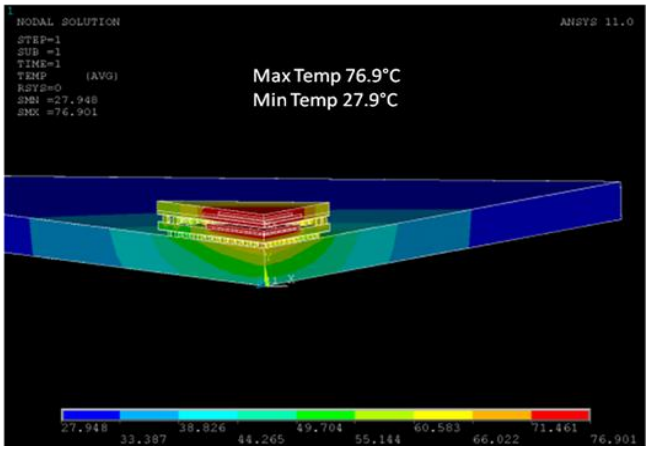


Figure 5.8 Power 0.3, 0.3 and 1W

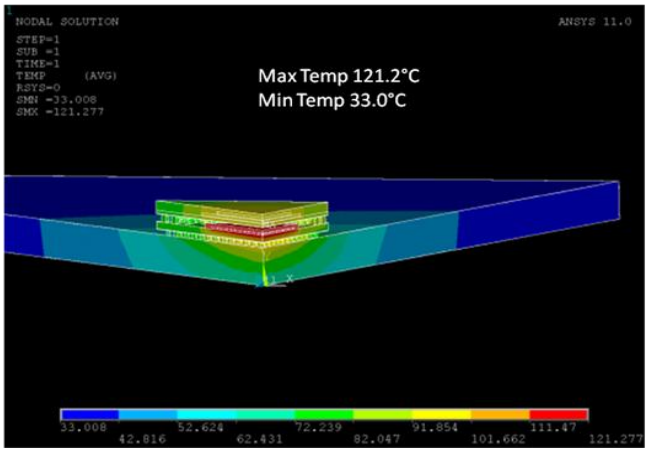


Figure 5.9 Power 0.3, 0.3 and 2 W

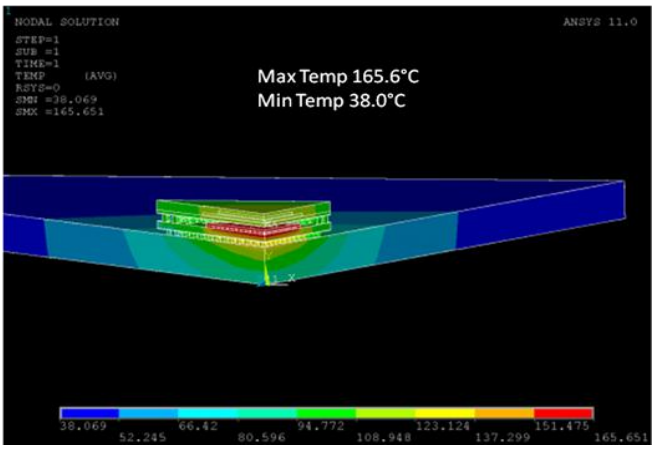


Figure 5.10 Power 0.3, 0.3 and 3W

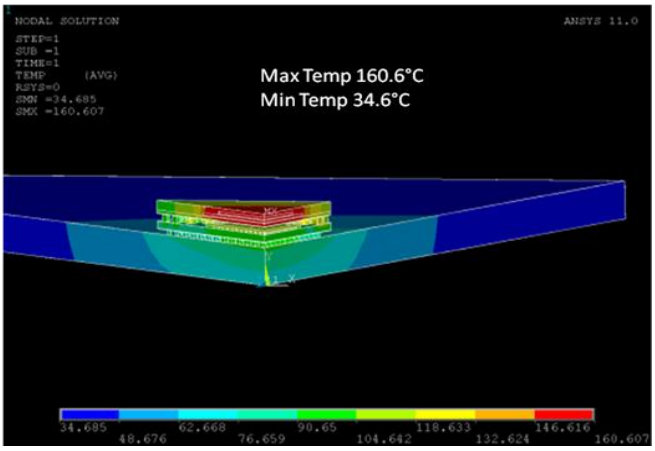


Figure 5.11 Temperature Contours for Case 10 (1 W each)

It is observed that for the low power memory dice, most of the heat dissipates through the mold and partly to the BGA interconnects. For the logic die, all the heat dissipates through the solder balls underneath and eventually to the PCB. BGA solder interconnects significantly conducts heat when the power on the memory dice is comparable to the logic die (case 10). In order to better understand the phenomenon, heat dissipation on individual surfaces are itemized. Table 5.2 shows the itemized heat distribution.

Table 5.2 Itemized Power Distribution

Power Cases	Mold Cap [W]		Mold Cap side [W]		Top Substrate Side [W]		Bottom Substrate Side [W]		PCB Top [W]		PCB Bottom [W]	
	Actual Power	% Total Power	Actual Power	% Total Power	Actual Power	% Total Power	Actual Power	% Total Power	Actual Power	% Total Power	Actual Power	% Total Power
0.1,0.1,1	0.065	5.435	0.009	0.82	0.014	1.168	0.008	0.725	0.732	61.000	0.37	31.230
0.1,0.1,2	0.108	4.916	0.016	0.744	0.025	1.156	0.027	1.253	1.4	63.636	0.622	28.273
0.1,0.1,3	0.114	3.583	0.023	0.715	0.029	0.911	0.046	1.449	2.05	64.063	0.93	29.063
0.2,0.2,1	0.087	6.249	0.013	0.941	0.017	1.187	0.001	0.1	0.84	60.000	0.44	31.429
0.2,0.2,2	0.13	5.435	0.019	0.824	0.028	1.167	0.017	0.727	1.5	62.500	0.71	29.583
0.2,0.2,3	0.173	5.099	0.026	0.772	0.039	1.16	0.026	0.778	2.152	63.294	0.982	28.882
0.3,0.3,1	0.109	6.86	0.016	1.03	0.019	1.2	0.012	0.72	0.94	58.750	0.503	31.438
0.3,0.3,2	0.153	5.873	0.023	0.885	0.031	1.177	0.007	0.281	1.6	61.538	0.786	30.231
0.3,0.3,3	0.196	5.435	0.029	0.821	0.042	1.167	0.026	0.727	2.25	62.500	1.057	29.361
1, 1, 1	0.264	8.8	0.03	1	0.021	0.7	0.1824	6.08	1.6	53.333	0.902	30.067
0.3,0.3,3	0.139	3.876	0.06	1.677	0.001	0.014	0.152	4.21	2.97	82.500	0.457	12.694

It is noted that for all the cases (except 11), approximately 92% of heat dissipates through the PCB whereas approximately 5% of heat dissipates through the mold cap. Remaining 2% of heat dissipates through the package side. It is also observed that for all scenarios, the minimum temperature is observed on the PCB because of its large area for heat transfer. Solder interconnects are considered to be the weak link in a BGA structure and they play an important role in the heat dissipation.

In order to reduce the temperature of the package there are some ways that can be employed. Instead of natural convection, forced convection can be considered that can help in reducing the temperature of the package. The other option would be to use a PCB with high thermal conductivity that has been considered as case 11 for the analysis. Case 9 and case 11 have similar power conditions. It is seen that the temperature drops by 64.8°C for the bottom package and by 29.7°C for the top package.

Figure 5.12 shows the temperature contour for case 11.

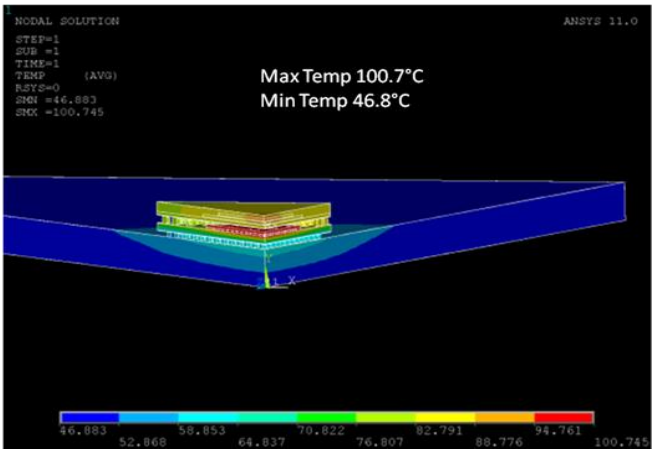


Figure 5.12 Temperature Contours for High Conducting PCB (Case 11)

CHAPTER 6

CONCLUSION

Thermal characterization of PoP is performed to study the effect of die power on the logic die and the memory dice. Also the effect of highly conductive PCB and substrate are studied. For the cases considered it is seen that the maximum temperature is always noted on the logic die (bottom package). Also for the highest power distribution case, the junction temperature far exceeded the design requirement. From the results it is seen that about 92% of the heat is dissipated through the PCB. Hence a viable solution would be to use a high conducting PCB. The effect of using a highly conductive PCB is seen in case 11 where the junction temperature is highly reduced. It is seen that the temperature drops by 64.8°C for the bottom package and by 29.7°C for the top package. Also when the power on the memory die is of the same order as that of the logic die as seen in case 10, the maximum temperature is seen on the memory dice (top package). Hence alternative cooling techniques like through silicon vias or microchannel cooling may have to be employed.

The solder interconnects, C4 and C5 solder balls are the only carriers for the heat to dissipate from the top package to the bottom package and through the PCB. They act as the thermal as well as the electrical interconnects. The solder balls are considered to be the weak link in a 3D package. Hence it is necessary to have a detailed simulation of the critical components in order to have maximum solder joint reliability and has been discussed in Part-2.

PART-2

THERMO-MECHANICAL ANALYSIS OF A PACKAGE ON PACKAGE

CHAPTER 7

INTRODUCTION

7.1 Background

Reliability is defined as the probability that a component or assembly will be operational for the expected period of use [1]. When microelectronic packages are subjected to actual field use, the failures are usually observed at the system level whereas the actual failure occurs at the component level due to thermal, mechanical, electrical or a combination of these failure modes and mechanisms. In order to assess the reliability and qualify the product within a reasonable amount of time in a well controlled environment, accelerated tests can be performed. A commonly accepted thermal cycling profile for microelectronics is when the packages are subjected between -40ºC to 125ºC, 15 min ramps / 15 min dwells.

Some of the previous work involves 3D packages like package in package, die stacked package, different architectures in stacked packages.

Mao *et al.* focuses on the analysis of a twin die stacked package under a cyclic thermal loading. Viscoplastic finite element analysis and Darveaux theory are applied to investigate the solder joint reliability of the stacked die package. The authors uses a 3D-slice model and concludes that solder joint under the die edge overhang area is always the critical especially for stacked die package [40].

Rodgers *et al.* uses sub structuring and sub modeling finite element techniques on a 9x9 ball grid array package. Darveaux's method is used to estimate the fatigue life of solder joints under various thermal loading. The innermost solder joint on the diagonal of the BGA is predicted to fail first in the accelerated thermal cycling (ATC) and accelerated thermal cycling plus constant power cases. The outermost solder joint is predicted to fail first in power cycling in comparison to ATC and ATC plus power cases [41].

Hossain *et al.* discusses about the viscoplastic finite element simulation to predict the solder joint fatigue life of different die stacking architectures for flash memory applications. Pyramid stack, rotated stack, stacking with spacers and staggered die stacking keeping the interconnection architecture (solder joint) constant are considered. Effects of different package reliability parameters like die size, die and die attach thickness are varied and their stress effects are studied. It is found that spacer-die architecture has better solder joint reliability performance than the other three die architectures [42].

Hence Part-2 of the thesis focuses on the thermo-mechanical analysis of a PoP.

CHAPTER 8

THERMO-MECHANICAL ANALYSIS

In this chapter the focus is on the design approach used for the thermo-mechanical analysis, the material properties assigned to the components of the package, the boundary conditions applied and the design of experiments.

8.1 Design Approach

An octant model of PoP is generated using ANSYS as a finite element solver. The models are simulated under accelerated temperature cycling conditions (-40ºC to 125ºC, 15 min ramps / 15 min dwells). Different package reliability parameters like die thickness, die attach thickness, top substrate thickness and bottom substrate thickness are varied and the effects of stresses are studied. Darveaux's approach is used to find out the fatigue life and plastic strain of the solder balls.

8.2 Material Properties

The assigning of accurate material properties and proper meshing determines the accuracy of FE model. As shown in table 8.1, the finite element model is integrated with linear and non-linear, elastic and plastic, time and temperature independent and dependent material properties. The thermo-mechanical properties used are Young's Modulus (E), co-efficient of thermal expansion (CTE) and Poisson's ration (v).

The solder material is modeled with modified Anand's rate dependent plasticity model. Viscoplasticity, a time dependent plasticity phenomenon is incorporated by Anand's constitutive model where the development of plastic strains is dependent on the rate of loading. Darveaux has presented solder constitutive relations based on Anand's model for rate dependent plasticity. Linear orthotropic material properties are used for the PCB.

Table 8.1 Material Properties [43]

Component	Young's Modulus, E [MPa]	Co-efficient of Thermal Expansion, CTE [1/K]	Poisson's Ratio, v
Ball	75842	24.5×10^{-6}	0.35
Die	162716	$-5.88 \times 10^{-6} + 6.261 - 8T\text{-}1.610\text{-}10T^{2} + 1.510\text{-}13T^{3}$	0.28
Die Attach	4700	60.0×10^{-6}	0.47
PCB	27294 - 37T (XY) 12204 - 16T (Z)	16.0×10^{-6} (XY) 84.0×10^{-6} (Z)	0.39 (XY & YZ) 0.11 (XY)
Substrate	4137	30.0×10^{-6}	0.4
Substrate Mask	3914	60.0×10^{-6}	0.47
Mold Cap	15513	15.8×10^{-6}	0.25
Underfill	14.5	20.0×10^{-6}	0.28

The detailed package is meshed using SOLID45 and VISCO 107 elements. The solder balls are meshed using VISCO 107 elements with unified Anand's constitutive equation and the rest of the model is meshed using SOLID45 elements. Structured mesh is used for the 3D model for the analysis. The solder balls are densely meshed whereas the mesh is made coarse on the far side of PCB to reduce the overall mesh count. The baseline case is meshed with 322,518 total number of elements. The total number of elements is divided into 268,950 SOLID45 elements and 53298 VISCO 107 elements.

SOLID45 elements are used as this element is defined by eight nodes having three degree of freedom at each node: translational in the nodal x, y and z directions. This element has plasticity, creep, swelling, large deflection and large strain capabilities [44].

VISCO 107 elements are used for solder balls as the element is defined by eight nodes having three degrees of freedom at each node: translational in the nodal x, y and z directions. The element is designed to solve both isochoric rate dependent and rate dependent large strain plasticity problems. VISCO 107 represents highly nonlinear behavior [44].

Table 8.2 shows the material constants for Anand's constitutive equation

Table 8.2 Material Constants for Anand's Constitutive Equation [45]

Constant	Definition	Parameter	Value
C1	Initial value of Deformation Resistance	S_o (MPa)	12.41
C2	Activation energy / Boltzmann's constant	Q/R (Kelvin)	9400
C3	Pre-exponential factor	A (1/sec)	4.08×10^{-6}
C4	Multiplier of stress	ς	1.5
C5	Strain rate sensitivity of stress	m	0.303
C6	Hardening Constant	h_o (Mpa)	1378.95
C7	Coefficient of deformation resistance saturation value	S (Mpa)	13.79
C8	Deformation resistance value	N	0.07
C9	Strain rate sensitivity of hardening	a	1.3

8.3 Boundary Conditions

Following are the four boundary conditions that are applied on the octant model. Symmetry boundary condition exists in the inner x and y directional plane. Throughout the analysis $U_z = 0$ for the lowest node in the inner section of the x and y direction intersection of the PCB. Figure 8.1 shows the application of the four boundary conditions.

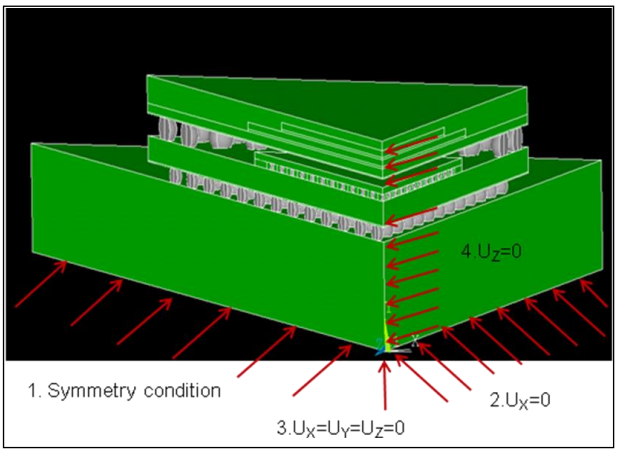


Figure 8.1 Location of boundary conditions applied on the model

8.4 Constitutive Models

For evaluating the reliability of the component, a 60 minute thermal cycle, ranging from -40ºC to 125ºC with 15 minutes high and low dwells and 15ºC/min low and high ramps are given as the input load for the simulation. Nonlinear, diagonal, octant, global models are used with the ANSYS finite element solver. Figure 8.2 shows the thermal cycles used for the simulations. The problem is solved for two cycles and hence there are 8 sub-steps. The plastic work of the solder balls are monitored at the end of 4^{th} and 8^{th} sub-step.

Based on the basic mechanism that is viewed as being responsible for inducing damage, the model proposed for predicting the fatigue life of solder joints can be divided into five major categories: (a) Stress based, (b) Plastic strain based, (c) Creep strain based, (d) Energy based and (e) Damage accumulation based [46].

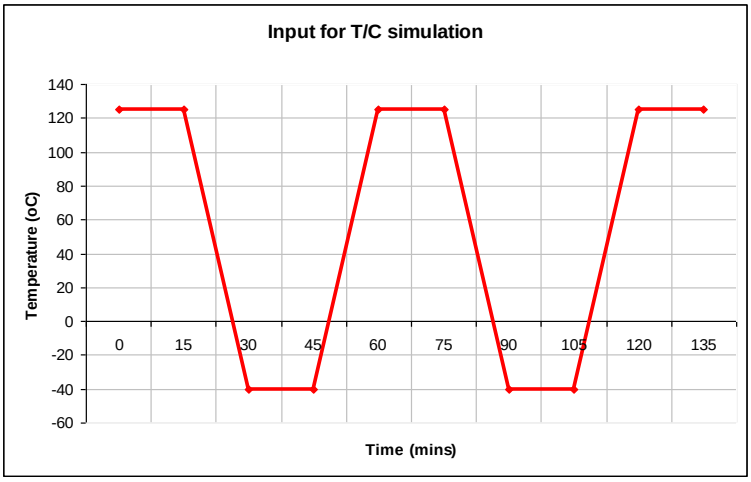


Figure 8.2 Input for Thermal Cycling Simulation

ANSYS APDL script is used for incorporating Darveaux's energy based fatigue life model to predict the solder joint fatigue life. The solder life prediction model based on the plastic work dissipated in crack initiation and crack growth to failure is reported by Darveaux [46]. The layer of elements having maximum plastic work density is included in the calculation of the

weighted average plastic density ΔW_{avg}. Then plastic work is averaged across the elements along the solder joint interface where the crack propagates.

$$\Delta W_{avg} = \frac{\sum_{i=1}^{Element} \Delta W_i * V_i}{\sum_{i=1}^{Element} V_i} \text{ ---------- (1)}$$

where ΔW_i denotes the plastic work density in the i^{th} element and V_i is the volume of that element.

Thermal cycles to crack initiation "N_o" is given by,

$$N_o = K_1 \Delta W_{avg}^{K2} \text{ ---------- (2)}$$

Crack propagation rate per thermal cycle "*da/dN*" is given by,

$$\frac{da}{dN} = K_3 \Delta W_{avg}^{K4} \text{ ---------- (3)}$$

where K_1, K_2, K_3 and K_4 are growth constants that depend on the geometry, loading and the finite element analysis method.

Table 8.3 shows the Darveaux's crack growth correlation constants.

Table 8.3 Darveaux's crack growth correlation constants [46]

No.	Constant	Value
1	K_1	22400 (cycle/psi)
2	K_2	-1.52
3	K_3	5.86 x10^{-7} in/cycle/psi
4	K_4	0.98

The characteristic solder joint fatigue life "" (number of cycles to 63.2% probability of failure) can be calculated by summing the cycles to crack initiation with the number of cycles it takes for the crack to propagate across the entire solder joint diameter "*a*". "" is given by,

$$\alpha = N_o + \frac{a}{\frac{da}{dN}} \text{ ---------- (4)}$$

Using the above equation to evaluate the 63.2% failure probability lifetime is strongly based on the assumption that the solder joint fatigue life follows an exponential distribution [46]. Figure 8.3 shows the flow chart used in modeling per Darveaux approach.

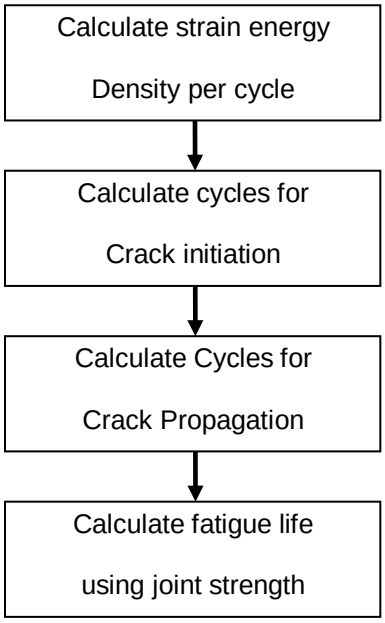


Figure 8.3 Flowchart of Darveaux's Approach [46]

8.5 Design of Experiments

By substituting the values of plastic work into Darveaux model, the fatigue life of all three solder interconnects are found out for the baseline case and a significant difference is observed in the fatigue life of all three solders. So to investigate the case further, the effect of die thickness, die attach thickness and substrate thickness on fatigue life of different solder interconnections are studied. The thicknesses are varied in the range of ± 20% as a result of which a DOE of 9 cases are generated.

For the package under study there are three different solder interconnects, three dice, two substrates and two die attaches. The objective of this study is to optimize the fatigue life of all interconnects in order to have high reliability in thermal cycling test.

The following table gives the different cases in which the die, die attach, top substrate and bottom substrate thicknesses are varied.

Table 8.4 Different cases of thickness variation

Bottom Substrate thickness: Baseline: 0.3 mm Increase: 0.36 mm Decrease: 0.24 mm	**Die Attach thickness:** Baseline: 0.0318 mm Increase: 0.03816 mm Decrease: 0.02544 mm
Top Substrate thickness: Baseline: 0.13 mm Increase: 0.156 mm Decrease: 0.104 mm	**Die thickness:** Baseline: 0.1 mm Increase: 0.12 mm Decrease: 0.08 mm

CHAPTER 9

RESULTS AND DISCUSSION

Accelerated thermal cycling is performed on the modeled PoP using finite element analysis. The temperature variation is from -40ºC to 125ºC with 15 minutes high and low dwells and 15ºC/min low and high ramps. ANSYS APDL code is used to obtain the stress strain relationship and post processing information. An octant symmetry model is used for the finite element simulation. The problem is solved for two cycles and hence 8 sub-steps. The plastic work of the solder balls is monitored at the end of the 4^{th} and 8^{th} sub-steps. After successful thermal load cycles, Von-mises stress, warpage induced and plastic work at the end of the thermal cycling are found out and documented. Figure 9.1 shows the Von-mises stress induced in the model.

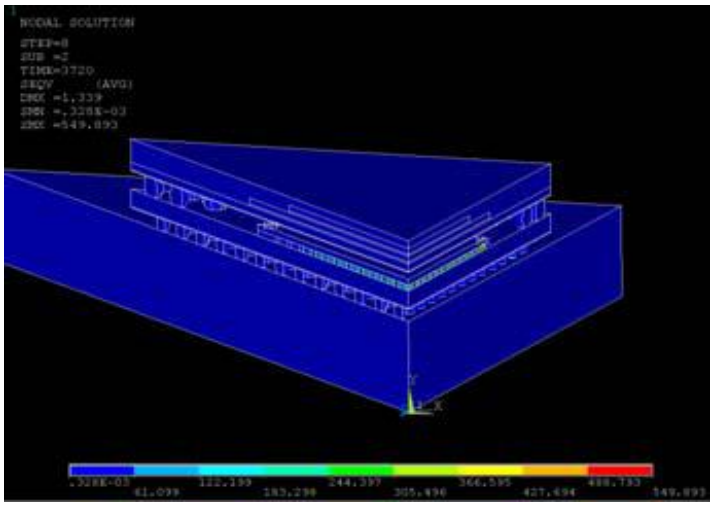


Figure 9.1 Von-mises Stress induced in the model

Figures 9.2 and 9.3 show the warpage induced and the Von-mises plastic strain induced in the model.

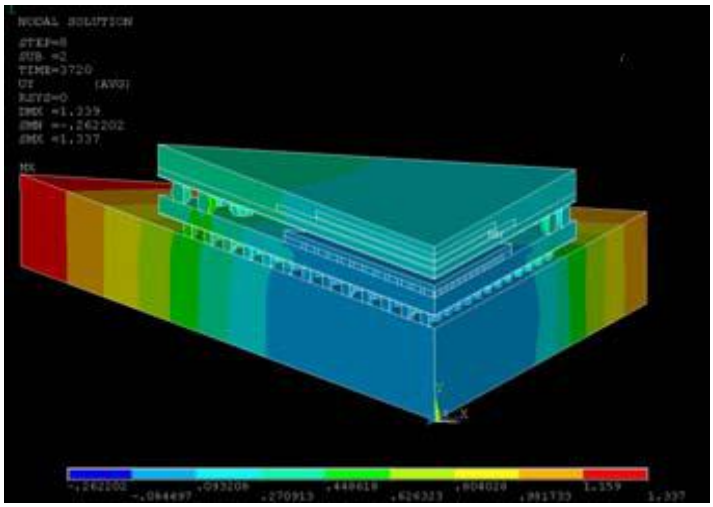


Figure 9.2 Warpage induced in the model

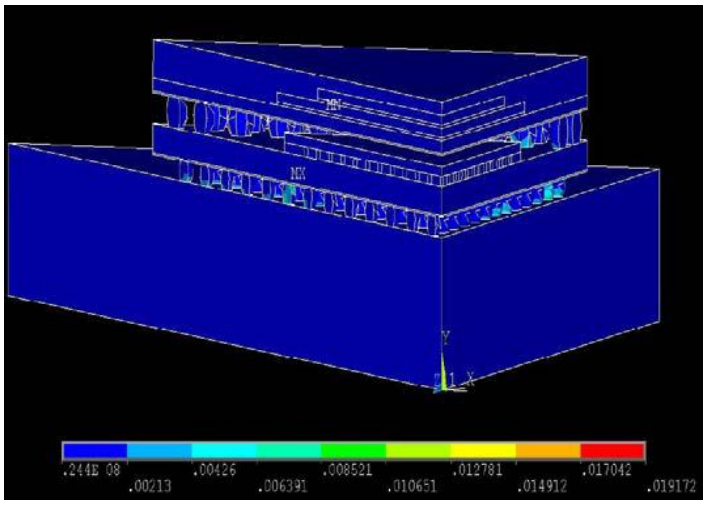


Figure 9.3 Von-mises plastic strain in the model

From figure 9.1 it is seen that the maximum stress occurs at the far end of C4 solder ball in the underfill which makes sense as it is at the far end that has been a traditional failure mode in accelerated thermal cycling simulations. One of the reasons the maximum stress does

not occur in the solder interconnect is because of its height. More the height of the solder ball more compliant it is for the fatigue loading. Figure 9.2 shows the warpage induced in the model. Warpage induced in the package is calculated by calculating the difference between minimum and maximum Y displacement of the model. As expected the maximum warpage is induced in the far end of PCB. This result confirms that the boundary conditions that are applied to the model are correct.

On substituting the values of plastic work into Darveaux model, the thermo-cycling life of the package under consideration came to 2324, 1525 and 3080 for C5, C4 and solder interconnect respectively. The reason for having such a high life for C4 is the presence of underfill. This statement is corroborated from figure 9.1 where the maximum Von-Mises stress occurs in the underfill. This result is strange as a significant difference is observed in the fatigue life of the three solders. To investigate this issue further, it is decided to study the effect of die thickness, die attach thickness and substrate thickness on fatigue life of different solder interconnections. These thicknesses are varied in the range of ± 20% and hence a DOE of 9 cases are generated.

DOE Results:

Tables 9.1, 9.2, 9.3 and 9.4 show the fatigue lives obtained (number of cycles) for the three different types of solder interconnects on varying the thicknesses of the bottom substrate, die attach, top substrate and the die.

Table 9.1 Fatigue lives obtained because of bottom substrate thickness variation (no. of cycles)

No.	Name	C5 (no. of cycles)	C4 (no. of cycles)	Solder Interconnect (no. of cycles)
1	Baseline	2324	1525	3080
2	Bottom Substrate Increase	3092	1682	1818
3	Bottom Substrate Decrease	402	970	1398

Table 9.2 Fatigue lives obtained because of die attach thickness variation (no. of cycles)

No.	Name	C5 (no. of cycles)	C4 (no. of cycles)	Solder Interconnect (no. of cycles)
1	Baseline	2324	1525	3080
2	Die Attach Increase	2539	1136	2944
3	Die Attach Decrease	3017	1810	1956

Table 9.3 Fatigue lives obtained because of top substrate thickness variation (no. of cycles)

No.	Name	C5 (no. of cycles)	C4 (no. of cycles)	Solder Interconnect (no. of cycles)
1	Baseline	2324	1525	3080
2	Top Substrate Increase	2931	1577	2645
3	Top Substrate Decrease	2783	1225	615

Table 9.4 Fatigue lives obtained because of die thickness variation (no. of cycles)

No.	Name	C5 (no. of cycles)	C4 (no. of cycles)	Solder Interconnect (no. of cycles)
1	Baseline	2324	1525	3080
2	Die Increase	2831	1370	3274
3	Die Decrease	2497	1842	2606

Figures 9.4, 9.5, 9.6 and 9.7 show the effect of variation of bottom substrate, die attach, top substrate and die thicknesses on the fatigue life of solder.

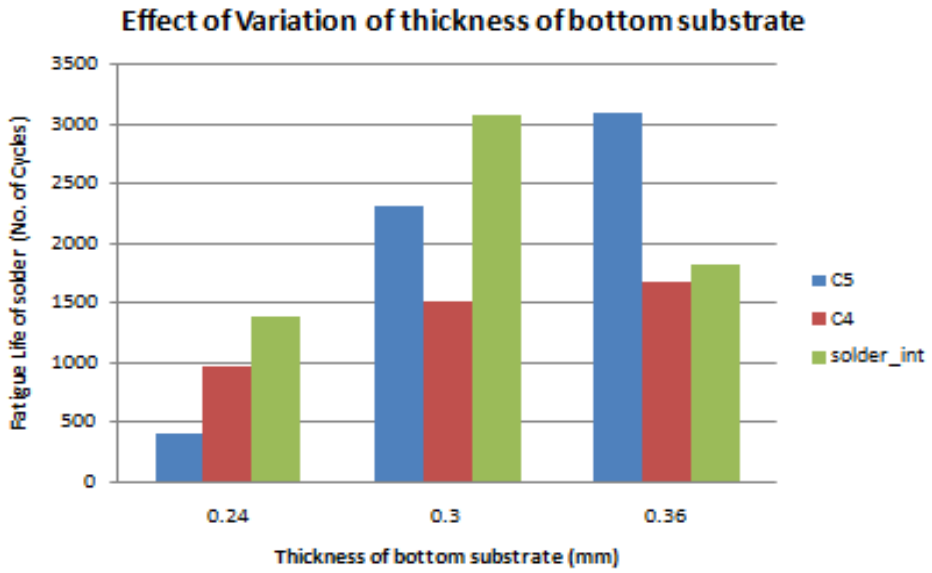


Figure 9.4 Effect of variation of bottom substrate thickness on fatigue life of solder

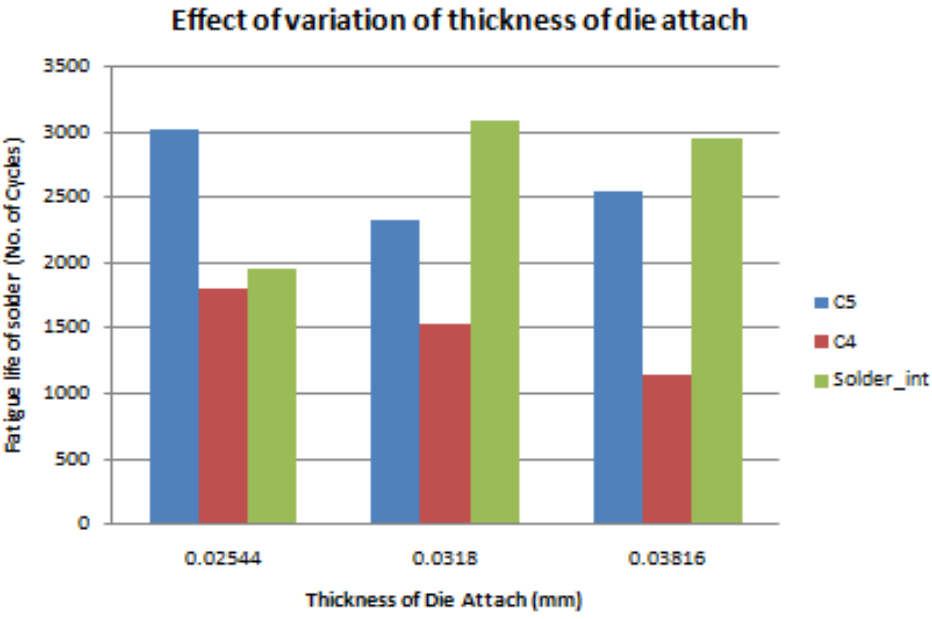


Figure 9.5 Effect of variation of die attach thickness on fatigue life of solder

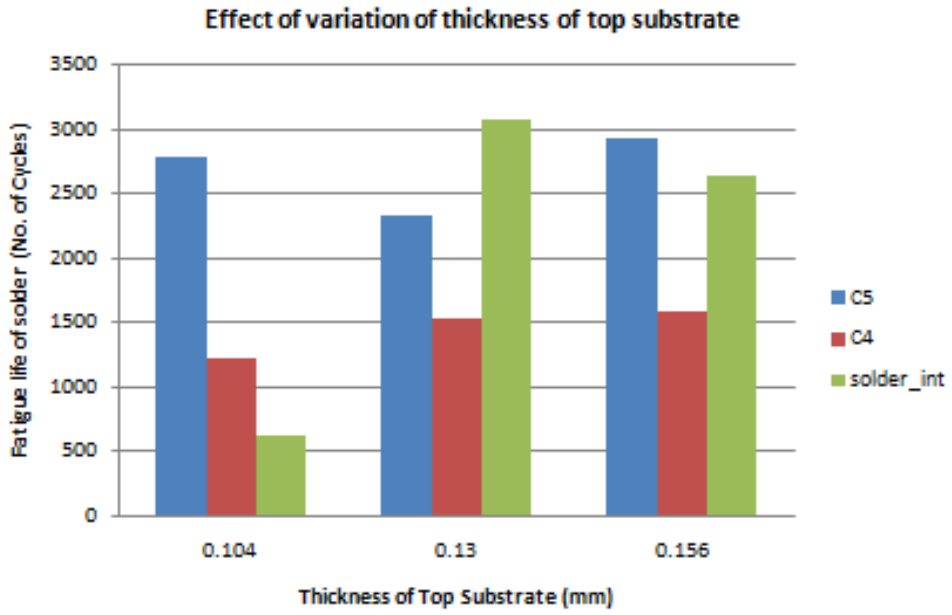


Figure 9.6 Effect of variation of top substrate thickness on fatigue life of solder

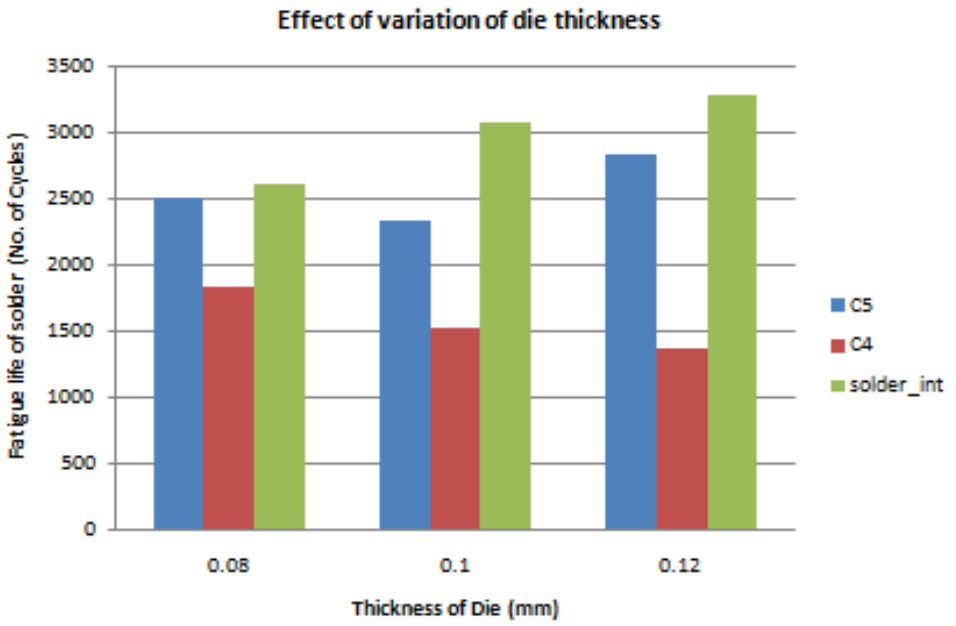


Figure 9.7 Effect of variation of die thickness on fatigue life of solder

From the above figures it is observed that having the existing configuration gives a very high life for the C4 solder ball as opposed to C5 solder and solder interconnects. Variation of thickness of bottom substrate significantly varies the fatigue lives of all three solder interconnects and is most beneficial to C5 solder. Having a thicker die and die attach are good as an increase in fatigue life is observed for all the three solder interconnects.

Figure 9.8 shows the warpage induced in the model.

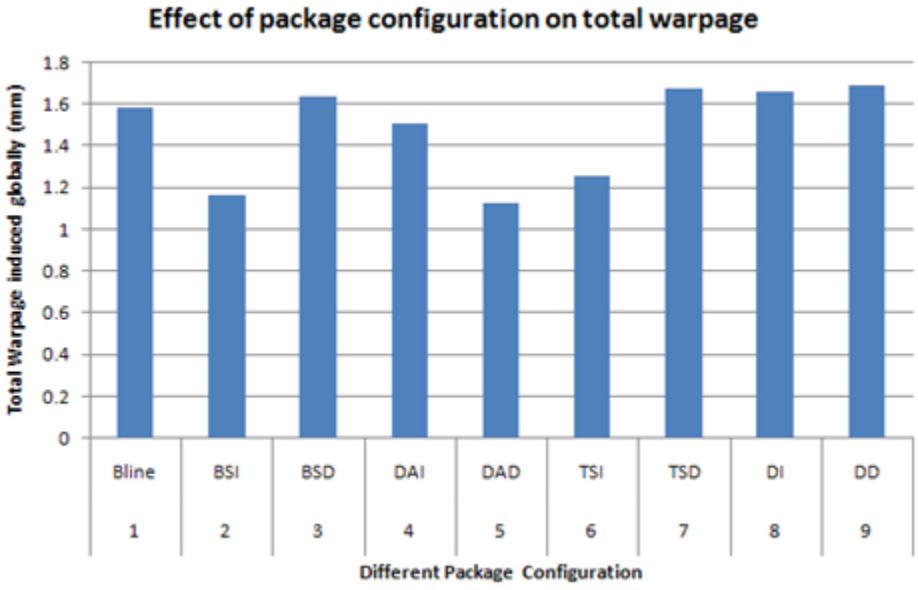


Figure 9.8 Total warpage induced in the model

Total warpage induced in the model is calculated by monitoring the displacement in Y direction. The warpage reported in figure 9.8 is the global warpage induced in the model and not the local warpage in package.

CHAPTER 10

CONCLUSION

A finite element analysis based study for estimating the accelerated temperature cycling solder joint fatigue life is applied to predict the reliability performance of a package on package. FEA tool ANSYS is used along with Anand's viscoplastic constitutive law. Darveaux's crack growth rate model is applied to calculate solder joint fatigue life. The thicknesses of the bottom substrate, die attach, top substrate and die are varied and their effect of the solder joint fatigue life is monitored. Solid45 and VISCO 107 elements are used to mesh the components and the solder balls respectively.

It is seen that on varying the thicknesses of bottom substrate, die attach, top substrate and die no fixed trend is observed. The variations of these thicknesses affect the C4, C5 and solder interconnects in different ways. The fatigue life of C5 increases in the range of 10-35% as compared to 8-20% for C4 and 8-15% for PoP interconnects. From the study it is noted that increase in bottom substrate thickness gives the best results for C5, decrease in die thickness gives the best results for C4 and increase in die thickness gives the best results for PoP solder interconnects. Based on the results, it is observed that C4 is the most crucial.

Hence to further study the effect on the fatigue life of the three types of solder balls, their attributes can be varied i.e. diameter, pitch and height by keeping the package height constant.

PART-3

COOLING TECHNOLOGIES FOR AN IGBT THERMAL TESTER IN POWER ELECTRONICS

CHAPTER 11

INTRODUCTION

11.1 Background

Thermal management of electronic components is becoming critically important and more challenging than ever before. The power densities continue to increase and the form factors continues to shrink resulting in early consideration of thermal management technologies and their applications in the product design process [47]. Hence solid state cooling such as thermoelectric or thermal diode is very important to future electronic thermal management because besides vapor compression and cryogenic, solid state cooling is the only well researched alternative technology that can provide sub-ambient cooling. In today's complex environment, thermoelectrics are required to provide cooling and heating in a variety of modular platforms including air-conditioning, liquid and direct contact designs. Unlike vapor compression cooling system which follows conventional thermodynamic and fluid principles, solid state cooling follows thermodynamic and electrical principles [48]. Some of the advantages of thermoelectric coolers (TEC) are [47, 49-51]:

1. Precision Temperature Control Capability
2. Quick and Economical Cooling Below Ambient Temperature
3. Reduced Space, Size and Weight
4. Heat Transport Controlled by Current Input
5. Able to Operate in Any Orientation
6. Virtually No Electrical Noise
7. Heating or Cooling by the Same Thermoelectric Module
8. No Moving Parts
9. Environmentally Friendly

10. High Reliability

Power semiconductor devices are the essential components determining the efficiency, size and cost of electronic systems for energy conditioning. Insulated gate bipolar transistors (IGBT) are 3 terminal power semiconductors noted for high efficiency and fast switching. They represent the most commercially advanced device of a new family of power semiconductors synergizing high input impedance MOS-gate control with low forward voltage drop bipolar conduction. It is designed to rapidly switch ON and OFF. Some of the applications are medium power and medium frequency range in uninterruptible power supplies, industrial motor drives and domestic and automotive electronics [52].

In these power electronics applications when the IGBTs are powered, they generate a lot of heat and they are usually mounted along with other components to make a complete set up. Hence cooling of these IGBTs is a major concern. The current industry standards are using conventional cooling methods like vapor-compression refrigeration and water-cooled systems such as air-conditioners and air to water heat exchangers. Owing to the advantages the TECs offer, an experimental study has been performed to design an IGBT thermal tester by making use of thermoelectric coolers instead of the conventional cooling systems.

11.2 Use of Thermoelectric Cooler in IGBT Thermal Tester

The IGBT Thermal Tester has to be developed for three different sizes of IGBT modules that have to be thermal cycled between 0ºC to 125ºC. Once the desired temperatures are obtained, the IGBT module with its mounting plate has to be regulated at that temperature with +/-1ºC for 30 minutes.

CHAPTER 12

DESIGN OF IGBT THERMAL TESTER

This chapter is based on the test set up for the IGBT thermal tester and the experimental procedure used for its design.

12.1 Test Set Up

The IGBT thermal tester assembly comprises of an IGBT module, IGBT mounting plate, TECs and a heat sink (air cooled). There are 3 different sizes of IGBT modules that have to be tested. The size of the IGBT modules are: 190 mm x 140 mm, 140 mm x 130 mm and 108 mm x 62 mm. Two different mounting plates are used, an aluminum plate and a copper plate. A single thermocouple is placed at the interface between the IGBT module and its mounting plate. Two more thermocouples are placed at the base of the heat sink. The thermoelectric coolers are insulated by fibre glass. The IGBT modules are non-insulated. The following figure shows the schematic of the IGBT thermal tester.

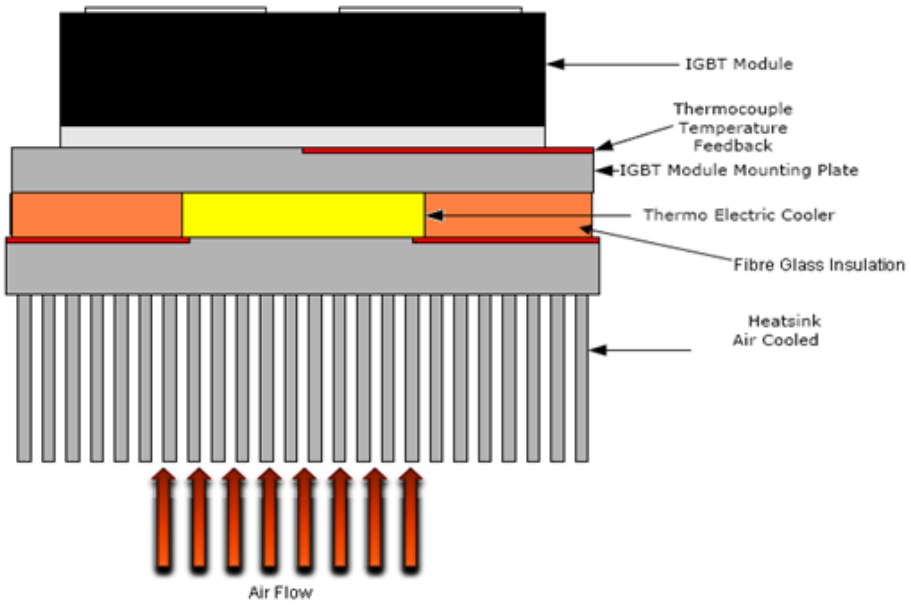


Figure 12.1 Schematic of IGBT Thermal Tester

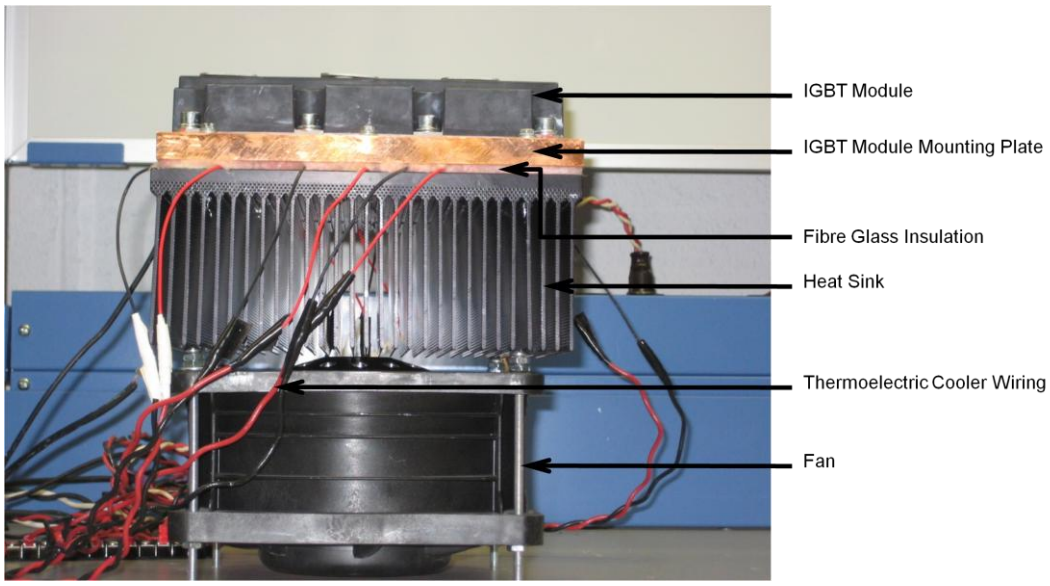


Figure 12.2 Actual IGBT Thermal Tester

12.2 Experimental Test Procedure

With the set up discussed, following is the procedure that is followed to carry out the experiment:

- The test is carried for the largest IGBT module of size 190 mm x 140 mm.
- The IGBT module is in a no load condition.
- The IGBT module and its mounting plate are non-insulated and exposed to an ambient temperature of 22ºC.
- The thermoelectric coolers are insulated by fibre glass so that the TEC does not pump the heat that is found in the environment around it.
- At the interface between the IGBT module and the mounting plate a thermocouple is placed to monitor the temperature during the thermal cycling.
- Two more thermocouples are placed at the bottom of the heat sink to monitor the temperature during the thermal cycling.
- The thermoelectric coolers are connected to a DC supply in order for it to be powered.

- A 3-way switch is used for changing the polarity of the thermoelectric coolers for cooling and heating.
- The current is applied to the thermoelectric cooler in such a way that it is able to attain the temperature of 0ºC and 125ºC and the time taken to achieve this temperature is noted.
- Once these temperatures are achieved, the current is controlled so as to maintain the desired temperature within +/- 1ºC.

CHAPTER 13

RESULTS AND DISCUSSION

As mentioned in the previous chapter TECs are used to cool and heat the IGBT module and the mounting plate. A number of different series, parallel and series-parallel combination of electrical connections with different specifications of TECs are carried out. Two different heat sinks and fans are also considered during the study.

The decision to use multiple thermoelectric modules goes beyond just thermal consideration. One of the concerns for using TEC is the heat generated from its cold side and the input power of the TEC that has to be dissipated using a heat sink. As the efficiency of such devices decreases with increasing thermal load there is a desire to use more modules to take advantage of higher efficiency. Hence to increase the amount of heat transferred, TECs modular design allows the use of multiple TECs mounted side by side and is known as thermoelectric array.

The amount of cooling a device can apply is dependent on the electric current supplied and this can be used to maintain a constant temperature of the device even if the ambient temperature varies. TECs perform better with heat sink having low thermal resistance. One of the most important things to note in a TEC is its maximum ratings, i.e V_{max}, I_{max}. It should always be taken care of that whenever a TEC is being operated, its maximum ratings should never be exceeded or else its performance would degrade or may even damage it.

Using a TEC in heating mode is very efficient because all the internal heating (Joulian heat) and the heat from the cold side is pumped to hot side. The temperature difference (DT) of a TEC can be increased while heating and it can exceed its maximum temperature difference (DT_{max}) since its material properties are temperature dependent.

13.1 Experimental Results

Initially the experiment is carried out with 2 TECs and in order to maintain the same current through them they are connected in series and placed adjacent to each other. The TECs are from TE Technology, Inc. For the experiment, an aluminum mounting plate and a heat sink-1 with a fan-1 having an open flow rate of 100 cfm is considered. Cooling is performed by applying a current of 2.56 A to the TECs. It is noted that the TECs can cool the IGBT module to a minimum of 3.1°C. Figure 13.1 shows the time taken during the cooling mode.

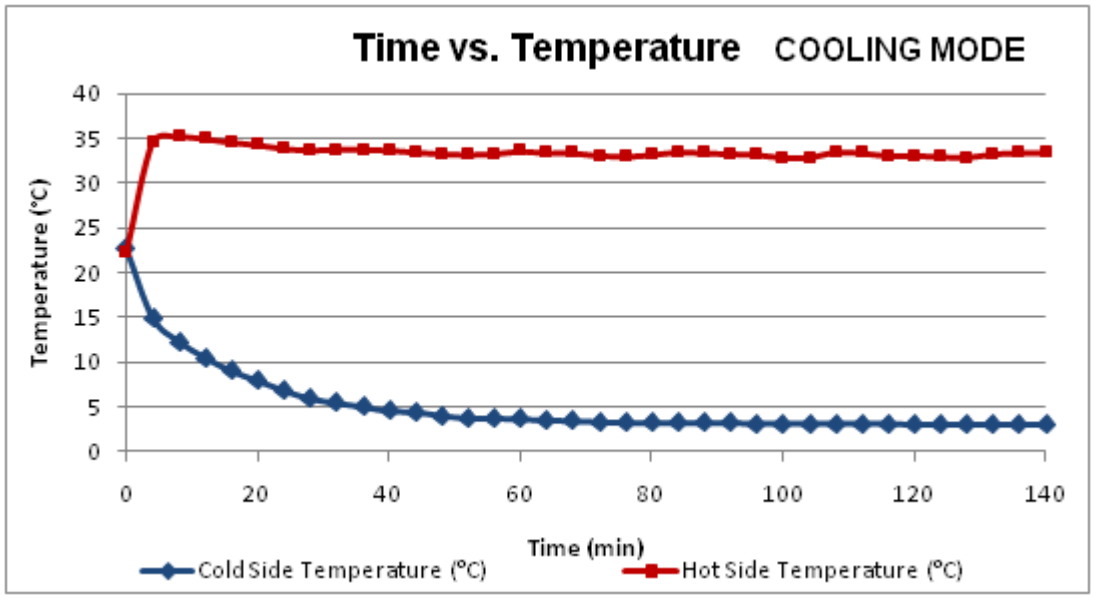


Figure 13.1 Two TECs - Series Connection (TEC-1)

During cooling the temperature at the interface between the IGBT module and the mounting plate is the cold side temperature and the thermocouple placed at the bottom of the heat sink is to note down the hot side temperature and during heating it is vice-versa. The reason TECs are unable to cool down the module to 0°C is because the total amount of heat that is generated from the cold side and the input power of the TEC is more than the amount of

heat the TEC can pump. Since the TECs are unable to satisfy the cooling requirement the heating mode study is not conducted.

Hence another study is performed where the same 4 TECs are connected in parallel. The same heat sink and fan are used. The test is performed again for the cooling mode. It is noted that in spite of connecting the 4 TECs in parallel the minimum temperature observed is 2.9°C. Figure 13.2 shows the time taken for the cooling mode. Again the cooling capacity is less than the required amount of heat to be dissipated.

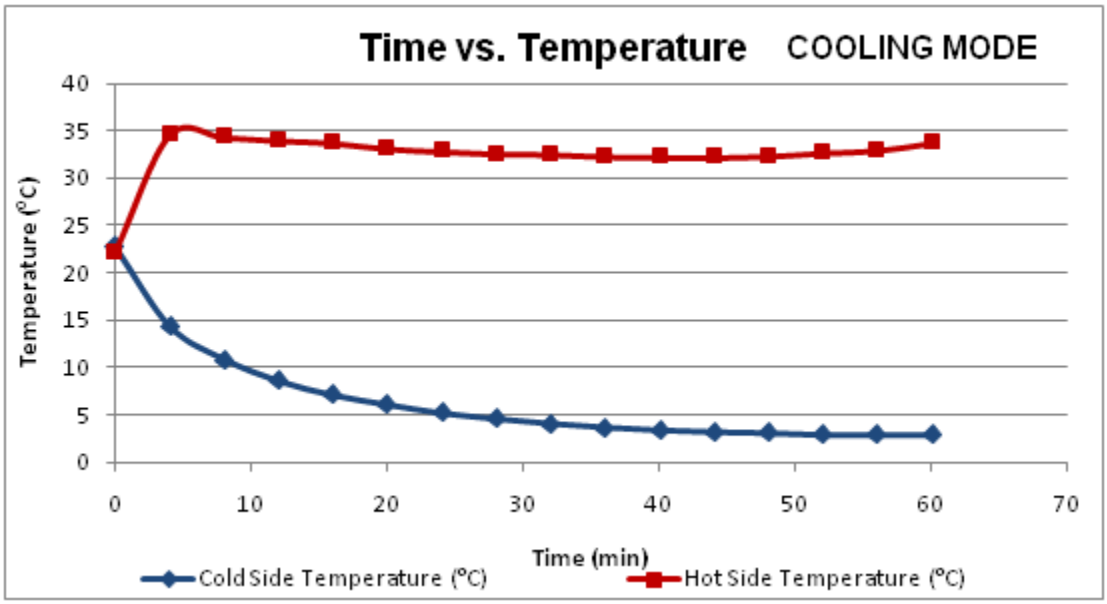


Figure 13.2 Four TECs - Parallel Connection (TEC-1)

The test is repeated with a new set of 4 TECs of higher specifications from TE Technology, Inc. They are again connected electrically in parallel with heat sink-2 and fan-1. The TECs are arranged in a 2 x 2 matrix array. A current of 3.93 A per module is applied during the cooling mode and it is observed that the IGBT module attains 0°C at the end of 18th minute. Similarly for the heating mode, a current of 3.97 A per module is applied and it is observed that the IGBT module reaches a temperature of 125°C at the end of 22nd minute. A high temperature

difference is observed during the cooling and heating mode and the COP is found to be less for the cooling mode. Figure 13.3 and figure 13.4 show the time vs. temperature chart for the cooling and heating mode respectively.

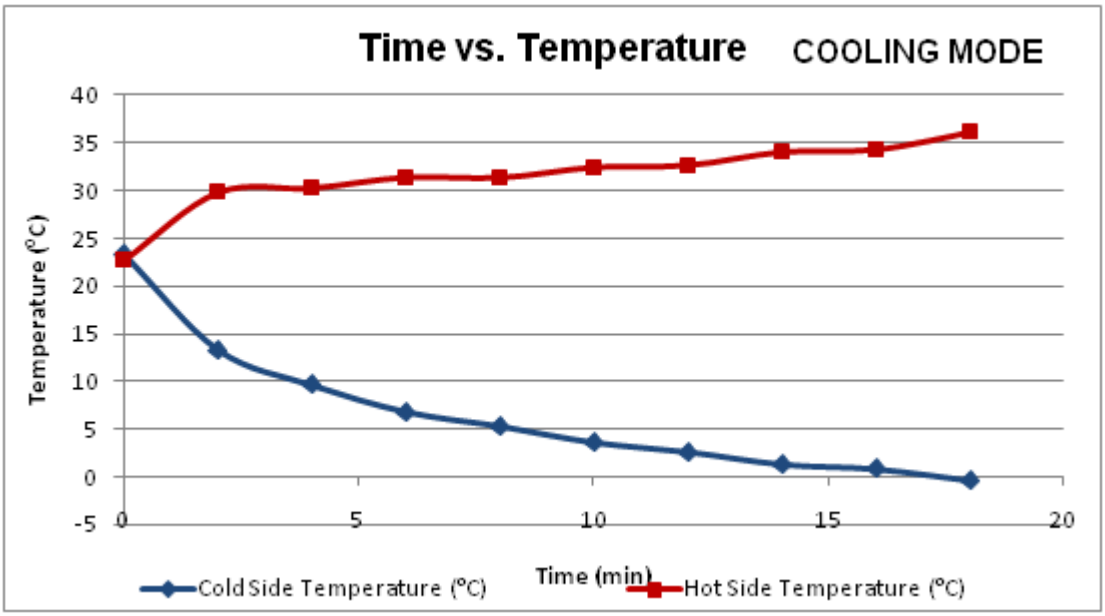


Figure 13.3 Four TECs - Parallel Connection (TEC-2)

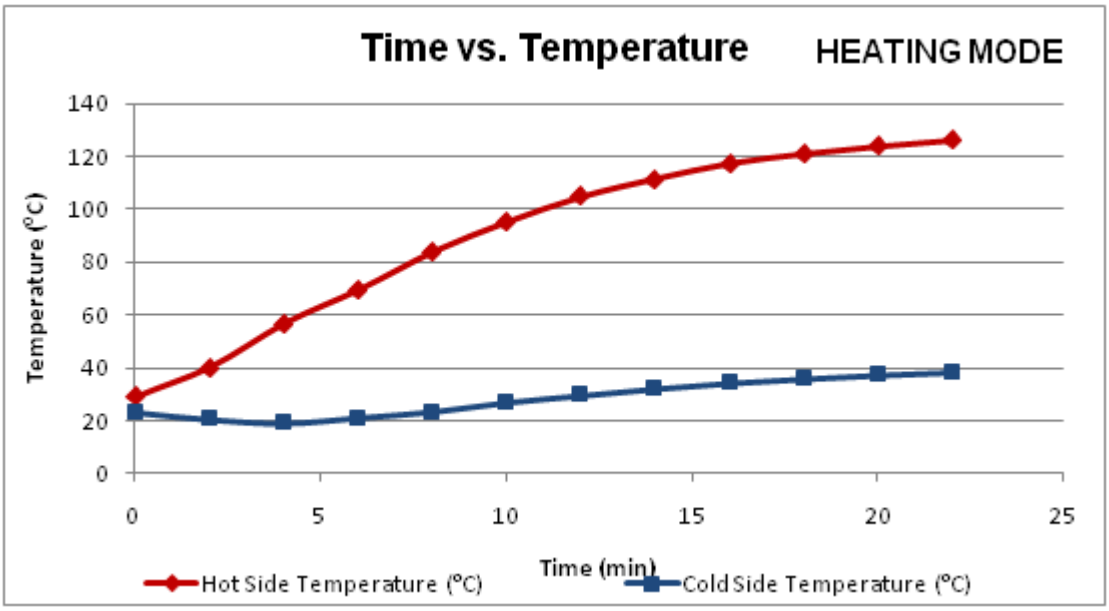


Figure 13.4 Four TECs - Parallel Connection (TEC-2)

As mentioned in the previous test since the COP is found to be less and the temperature observed at the base of heat sink is high, a third set of TECs from FerroTec are considered whose specifications lie between the previous two sets of TECs. This time 6 TECs are connected electrically in parallel with a 3 x 2 matrix arrangement. Heat sink-2 and fan-2 with an open flow rate of 330 cfm is considered. The TEC is a potted TEC unlike the previous two sets of TECs. The advantage of a potted TEC is that it prevents corrosion, it improves the mechanical strength of the thermoelectric module and the module becomes more durable. A current of 3.67 A per module is applied and a temperature of 0°C is attained within 6 minutes and is able to be cool down to -8.9°C. The figure shows the time vs. temperature plot for the cooling mode.

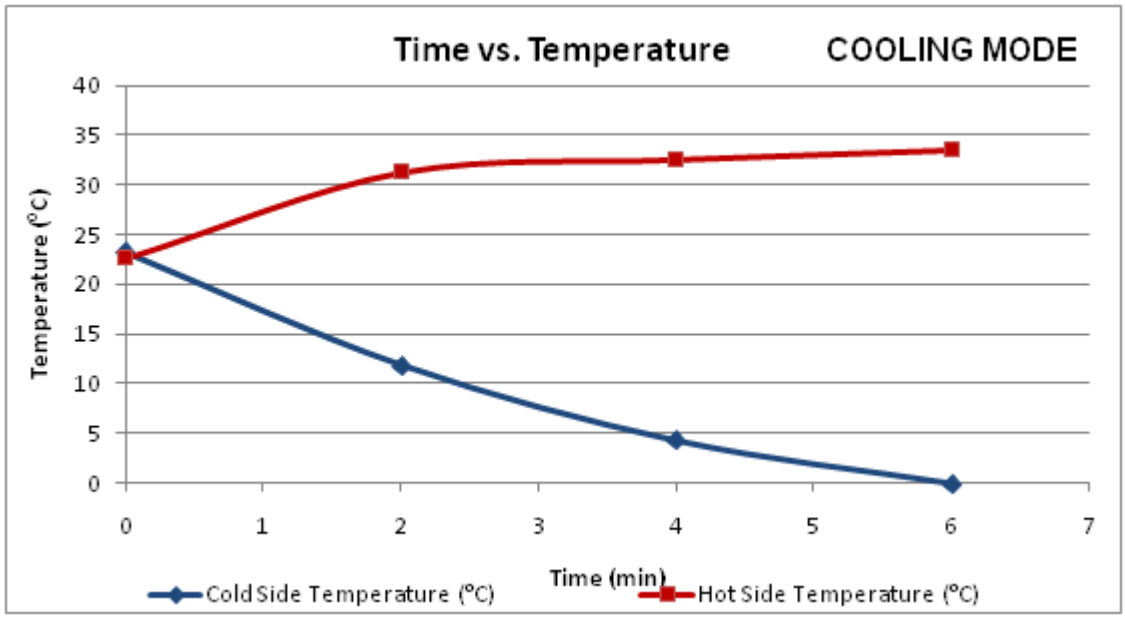


Figure 13.5 Four TECs - Parallel Connection (TEC-3)

But during the heating mode, the given set of TECs is not able to heat the IGBT module to 125°C. The rise in temperature is very gradual and the temperature at the base of the heat sink is seen to be very high. Although good results are obtained for the cooling, heating mode does not give the desired results. Hence two different electrical connection combinations are

thought of to proceed with, first being the series-parallel connection and the second being the series connection.

In a parallel combination, same voltage flows through all the TECs but the current gets added up. It drives up the current real high and normally limits the power supply. Hence the series connection is finalized as the best way to connect the TECs. In a series connection, the current remains the same whereas the voltage gets added up.

For the series combination, 6 TECs are considered. Heat sink-2 and fan-2 are considered with the exception of a copper mounting plate for the IGBT module. The TECs are connected in 3 x 2 matrix arrangement. On applying a current of 3.7 A, a temperature of 0°C is noted by 8.5 minutes during the cooling mode. Similarly when a current of 3.7 A is applied during the heating mode, the IGBT module reaches a temperature of 125°C by the end of 30^{th} minute. The COP is found out to be 0.58 during the cooling mode. During both the cooling and heating mode the temperatures are regulated within +/-1°C for an additional 30 minutes by controlling the input current. In order to maintain the temperature within +/-1°C, the input current is reduced such that the new current is 55% - 60% of the input current. Figure 13.6 and figure 13.7 show the temperatures for the cooling and heating mode respectively.

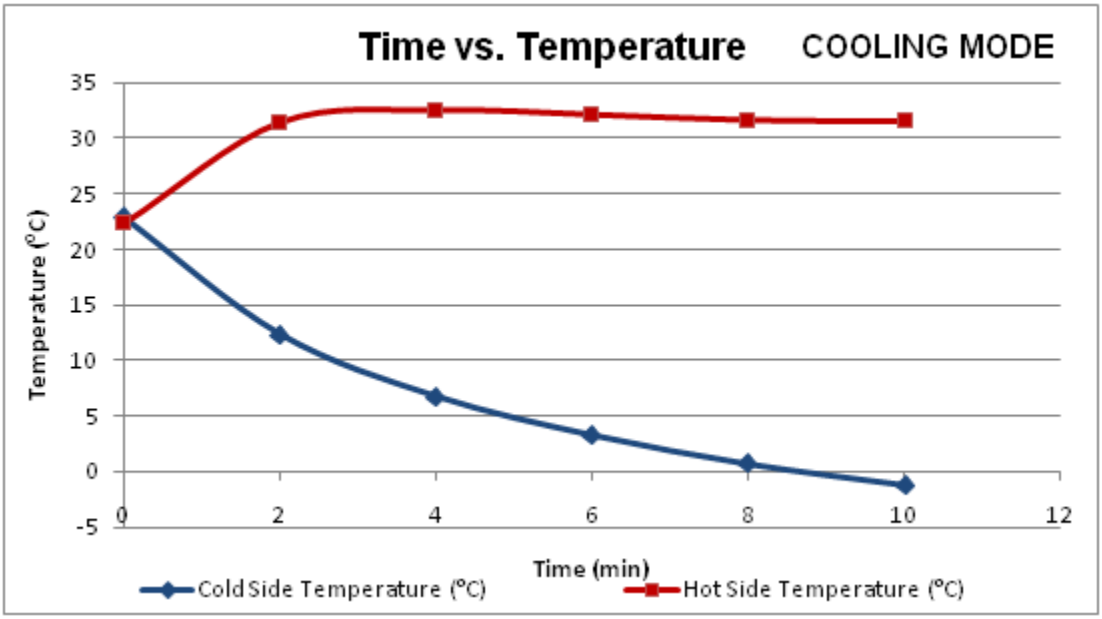


Figure 13.6 Six TECs - Series Connection (TEC-3)

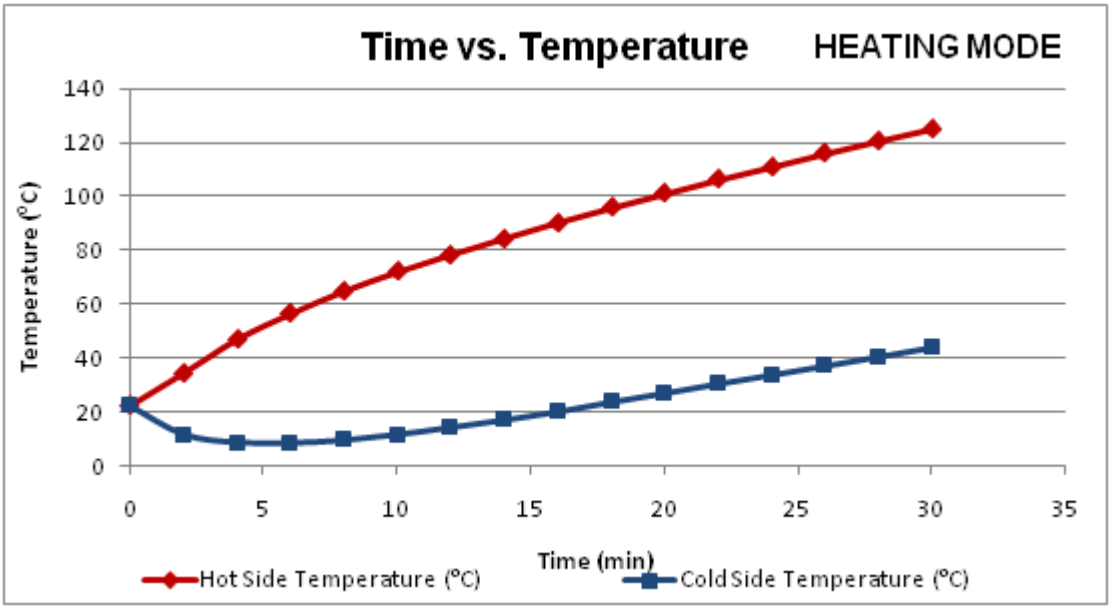


Figure 13.7 Six TECs - Series Connection (TEC-3)

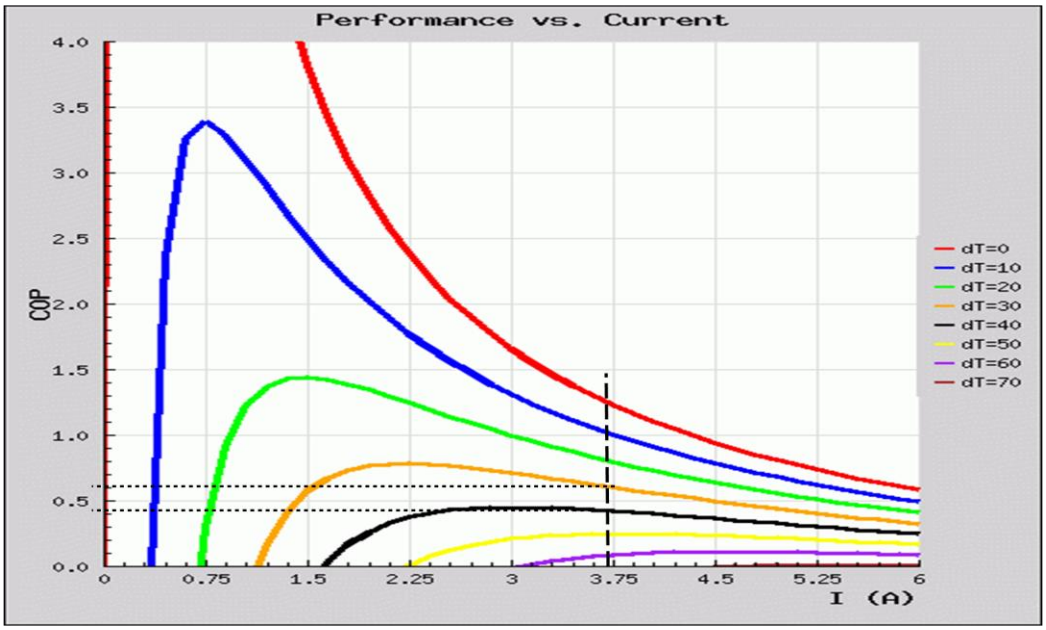


Figure 13.8 Co-efficient of Performance (COP) vs. Input Current (I)

Figure 13.8 is the performance chart of COP vs. I for the last mentioned case. It is noted that the TEC has a COP of 0.58 and the value is obtained by interpolating the temperature values against the input current of 3.7 A.

CHAPTER 14

CONCLUSION

The IGBT module of size 190 mm x 140 mm has been successfully thermal cycled between the temperature ranges from 0ºC to 125ºC. The set up included using 6 TEC's having them electrically connected in series and placed in a 3 x 2 matrix. In order for the tester to work efficiently the amount of waste heat i.e. the heat dissipated from the heat sink has to be less than the heat pumping capacity of the TEC. The series connection of the IGBT thermal tester helps it to be current controlled. Also it has to be made sure that the TECs are insulated to prevent condensation that can degrade the thermoelectric cooler's reliability. The best performance for the TECs is observed when the input current is about 60-65% of the maximum current rating.

The future work would include experimental testing for the remaining two sizes of IGBT modules and testing the largest sized IGBT module with the aluminum mounting plate. Once the tester is finalized a control system has to be developed so that the desired temperatures can be regulated by controlling the input parameters. Test the IGBT thermal tester for higher ambient conditions. Perform computational modeling of the IGBT thermal tester and compare with the experimental results. Similarly based on the heat load calculations the performance of the remaining two IGBT modules can be estimated.

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