SOLID-STATE TUNNELING SPECTROSCOPY OF INDIVIDUAL QUANTUM DOTS

by

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ABSTRACT

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Quantum dots are gaining importance for their potential applications in the fields of energy harvesting, bio-labeling and treatment, in opto-electronic devices and in photonic devices. For all these applications, it is imperative to know their electronic structure. Although currently several spectroscopic techniques exist to study the electronic structure of these quantum dots, they are accompanied by other effects and do not give purely the electronic structure of the individual quantum dot.

The main goals of this research are to:

- To study the energy level structure of '*single*' quantum dots.
- Develop a new spectroscopic technique that allows the measurement of the energy level structure of the single quantum dots.
- Demonstrate that the tunneling spectroscopy can be carried out without other effects such as electron-phonon coupling, non-resonant tunneling, dielectric response of the capping organic layer etc.

A major accomplishment from this research is the ability to study directly the energy level structure of individual quantum dots without peak broadening caused by other effects.

Spectroscopic measurements were carried out using the double barrier tunnel junction (DBTJ) approach. The DBTJ is formed when a quantum dot placed on the periphery of the vertically separated source-dielectric-drain electrode structure. The measurement units were fabricated using CMOS compatible parallel batch processing techniques.

Spectroscopic measurements were carried out using current-voltage and differential conductance measurements using the lock-in measurement technique. Using these measurements, the energy structure of individual quantum dots were mapped at room temperature as well as low temperatures. Conductance spectra showed that the peak-widths were linearly dependent only on the temperature and are not subject to any other broadening effects. The FWHM of the conductance peaks at 77, 150, 225 and 295K were measured to be 3, 7, 9 and 18meV respectively. The peak widths from this study are narrower when compared to ~60meV from STM spectroscopy conducted on 6.1nm CdSe quantum dots even at ~5K. Due to the dependence of the peak width only on the temperature, fine energy level separation measurements are possible using this spectroscopic technique. This narrow peak width allows the measurement of the electronic structure even at room temperature.

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CHAPTER 1

INTRODUCTION

1.1 Overview

Quantum dots are increasingly finding innovative applications in the fields of energy harvesting [1.1-1.2], biomedicine [1.3-1.1.7], nanoelectronics [1.8], and photonics [1.9]. For these applications, the knowledge of their electronic structure plays a critical role. The main focus of this work is to get an in-depth understanding on the fundamental transport properties in such nano-scaled objects. There are currently several techniques to study the transport properties through these quantum dots. The focus of this work is to study only the energy level structure of individual quantum dots without any other interference.

1.2 Quantum dots

Quantum dots are nanometer scaled objects with unique size-tunable optical and electronic properties. They are crystalline materials which are size-restricted in all three dimensions such that the electron wave functions are confined within its volume. Due to this confinement, their optical and electronic properties are also size-tunable. These 'quantized' states also lead them to be called as "*Artificial atoms*" [1.10]. They were first observed in 1926 with CdS colloids [1.11], but not until the early 1980s have these nanostructures been extensively studied. Early quantum dots were made using lithographic techniques or utilizing molecular beam epitaxial (MBE) growth [1.12-1.14], but with the advent of colloidal synthesis,

smaller and more varied quantum dots are being synthesized. These colloidal synthesized quantum dots can vary in size between few nanometers to tens of nanometers in diameter. Apart from these synthesis techniques, electrochemical deposition can also be accomplished directly onto substrates [1.15-1.17].

Quantum dots, due to their extremely small sizes and novel opto-electronic properties, are promising building blocks for the fabrication of optical and electronic devices. As these nanoparticles can be easily functionalized either chemically [1.18] or biologically [1.19], they may have varied applications in bio-labeling [1.20, 1.217], cancer treatment [1.22], hyperthermia treatment [1.23], and are very suitable candidates for sensor applications, both chemical and biological sensors. One of the prospective applications includes integrated circuits where these semiconducting particles could lead to smaller device sizes [1.24]. Using different materials, such as II-VI compound semiconducting quantum dots and by varying the sizes, the band gap for these quantum dots can be manipulated within a broad range including the entire visible spectrum. These properties and their tenability makes the quantum dots suitable candidates for light emitting diodes (LED) [1.25], coulomb islands for single electron transistors [1.26], chromophores or light absorbing material for solar energy harvesting [1.27, 1.28], or building blocks for photonic crystals [1.29].

For all of these potential applications, the most fundamental property that must be known is the electronic structure for these quantum dots. Various spectroscopic techniques have been employed to study the electronic properties of these quantum dots. The most commonly utilized technique for spectroscopy of colloidal synthesized quantum dots is optical spectroscopy. In optical spectroscopy, the electrons in the ground state inside the quantum dot absorb the energy from the photon and are thus excited. The energy or wavelength absorbed gives the difference in energy levels. This is called absorption spectroscopy. When these excited electrons relax, they do so while emitting photons and return to the ground state. This emitted energy spectroscopy is called photo-luminescence spectroscopy (PLE). One of the

disadvantages of this technique is that the optical transitions are subject to the selection rules, and not all the energy levels can be directly measured [1.30]. Due to the selection rules involved in this technique, energy level separations are obtained indirectly, hence it is called an indirect measurement technique.

For probing the energy levels of an individual quantum dot, scanning tunneling spectroscopy using tools such as Scanning Tunneling Microscope (STM) and Atomic Force Microscope (AFM) in the tunneling spectroscopy mode, can be performed. Using an ultra sharp tip and double barrier tunnel junctions, direct probing of the electronic structure of single quantum dots is accomplished. Electron-phonon coupling effects are observed using the STM spectroscopic technique [1.31, 1.32]. The broadening of conductance peaks due to this coupling effect may possibly be intrinsic with the STM as they are observed for both single molecules and quantum dots [1.33, 1.34]. Even in cryogenic temperatures (<10K), the peak broadening still remains in effect. This peak broadening may prohibit resolution of very small energy level separations as peaks may become convoluted.

Both of the above mentioned techniques, optical and scanning probe spectroscopy can probe the energy levels of quantum dots. The goal of this work is to study the energy level structure of individual quantum dots without any interference from the other interactions such as the electron-phonon coupling effect. In order to accomplish this, a new tunneling spectroscopic technique must be developed to directly probe the energy levels of an individual quantum dot without any external interference. A new spectroscopic measurement technique, where the above mentioned requirements are met will be presented in this thesis. As this thesis progresses, fundamental understanding of the quantized energy levels of quantum dots, tunneling spectroscopy concepts, measurement unit utilizing vertically separated electrodes design, fabrication and measurements will all be covered.

1.3 Organization of this thesis

The varied applications of quantum dots and other quantum structures were outlined above. The main goal of this work is to develop a spectroscopic technique to study the electronic transport behavior through individual quantum dots as outlined in the previous section.

In Chapter 2, the double barrier tunnel junction approach to perform solid-state resonant tunneling spectroscopic measurements will be introduced. This chapter identifies the basic components of solid-state resonant tunneling spectroscopic measurement unit, how these components are arranged forming the double barrier tunnel junction along with an equivalent circuit diagram of the measurement unit. To understand electron transport through these quantum dots, the governing equations will be derived. Energy diagrams will be used to qualitatively understand the electron transport mechanism through these quantum structures.

In Chapter 3, other widely utilized spectroscopic techniques will be presented along with their merits and demerits. The vertical electrode structure employed in this study for the spectroscopic measurements will be described along with its advantages over other spectroscopic techniques.

Fabrication of the single-electron spectroscopic measurement units will be completely detailed in Chapter 4. Parallel fabrication of a large number of measurement units on a 4” silicon wafer was made possible using CMOS compatible processing and wet chemistry. CMOS compatible processes such as e-beam evaporation, plasma enhanced chemical vapor deposition (PECVD), RF-magnetron sputtering along with self assembled monolayers were utilized for measurement unit fabrication.

Spectroscopic measurement set-up along with details of obtaining the differential conductance will be presented in Chapter 5. The analysis of the spectroscopic data obtained from several different individual quantum dot units will follow. Different current-voltage as well

as differential conductance spectra, either numerical or direct differential conductance measurements using lock-in amplifier for various spectroscopic measurement units will be presented.

In Chapter 6, the achievements of this study will be summarized and some additional experiments will be proposed that could enhance the potential of this study in the future.

CHAPTER 2

THEORY OF RESONANT TUNNELING SPECTROSCOPY

2.1 Introduction

In the previous chapter, the potential applications of nanoparticles and quantum dots were outlined. The advantages and disadvantages of current spectroscopic techniques were also presented briefly. In this chapter, we will discuss the quantization effect and the transport properties through these quantum dots. The outline of this chapter will be as follows:

a) We will start with a brief introduction into the electronic properties of quantum dots namely quantum confinement which is the fundamental property under study in this work.

b) Electron tunneling concepts including double barrier tunnel junctions and electron transport through nanoparticles/quantum dots through these tunneling junctions will be detailed.

c) Resonant tunneling spectroscopy will be explained with the aid of energy diagrams and measurement of energy level spacing detailed.

2.2 Quantum confinement

2.2.1 Discrete energy levels in three dimensional solids

While dealing with quantum dots, the electron wave function is larger than the actual size of the quantum dot. For the simplest case, a potential well of length '*L*' shall be considered in one dimension as seen in figure 2.1.

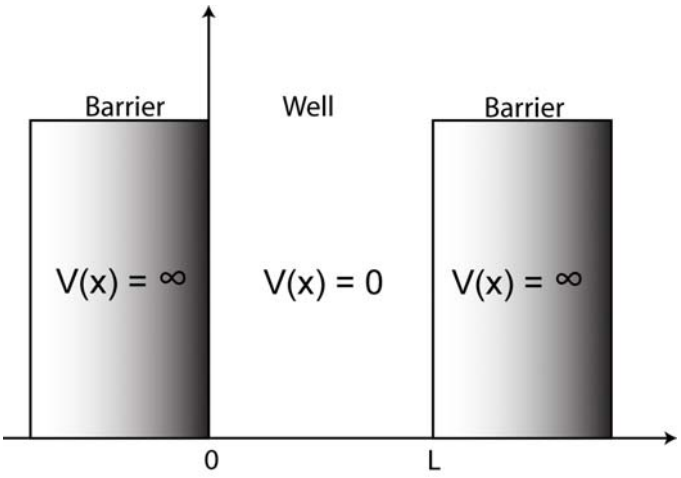


Figure 2.1: Schematic of an infinite potential well in one dimension.

The boundary conditions for this system are as follows:

$$V(x) = \begin{cases} 0 \; for 0 \le x \le L \\ \infty \end{cases} \tag{2.1}$$

The Schrödinger equation for this system can be written as:

$$\left(-\frac{\hbar^2}{2m}\frac{d^2}{dx^2} \right)\psi(x) = E\,\psi(x) \tag{2.2}$$

$$\frac{d^2}{dx^2}\psi(x) + k^2\psi(x) = 0 \tag{2.3}$$

where $k^2 = \dfrac{2mE}{\hbar^2}$

The solution for this equation (2.3) is as follows:

$$\psi(x) = A\sin(kx) \tag{2.4}$$

If the boundary conditions are applied, then,

$$\psi(L) = A\sin(kL) = 0$$
$$\Rightarrow kL = n\pi$$
$$\Rightarrow k = \frac{n\pi}{L}$$

where '*n*' is an integer. If normalized, then,

$$\int_0^L \psi(x)dx = 1$$

$$\Rightarrow A = \sqrt{\frac{2}{L}}$$

So the final solution and Eigen values can be written as:

$$\psi(x) = \sqrt{\frac{2}{L}}\sin(kx) = \sqrt{\frac{2}{L}}\sin\left(\frac{n\pi x}{L}\right) \tag{2.5}$$

$$E_n = \frac{\hbar^2 k^2}{2m} = \frac{n^2\hbar^2}{2m}\frac{\pi^2}{L^2} \tag{2.6}$$

This solution leads to the discrete energy levels based on different '*n*'. This solution is for a one-dimensional system. For a 3-dimensional system, the wave function can be written as a product of three independent wave functions, or,

$$\psi(x,y,z) = \psi_1(x)\cdot\psi_2(y)\cdot\psi_3(z)$$

The final solution for this 3-D cubic system can be written as follows:

$$\psi(x,y,z) = \sqrt{\frac{8}{L_x\cdot L_y\cdot L_z}}\sin\left(\frac{n\pi\cdot x}{L_x}\right)\cdot\sin\left(\frac{n\pi\cdot y}{L_y}\right)\cdot\sin\left(\frac{n\pi\cdot z}{L_z}\right) \tag{2.7}$$

$$E_n = E_{nx} + E_{ny} + E_{nz} = \frac{\hbar^2 k_{nx,ny,nz}{}^2}{2m} \tag{2.8}$$

where, $k_{nx,ny,nz}{}^2 = \frac{\pi^2}{L_x\cdot L_y\cdot L_z}\cdot(n_x{}^2 + n_y{}^2 + n_z{}^2)$

Equations 2.7 and 2.8 show the presence of discrete energy levels for a three dimensional cubic system.

2.2.2 Discrete energy levels in quantum dots

For real quantum dots, the shape is assumed to be spherical hence; the coordinate system must be changed to the spherical coordinate system (*r, θ, Φ*). The similarity between quantum dots and isolated atoms becomes particularly striking in the case of quantum dots when the confining potential has a spherical symmetry. The potential energy outside the quantum dot is infinite; thus the electron and hole are always found within the quantum dot (i.e., the surface of the quantum dot defines the walls of the "box"). Thus the boundary conditions for such and infinitely deep spherical potential well are as follows:

$V(r) = 0$, if $r < R$, and,

$V(r) = \infty$, $\psi(r) = 0$ if $r > R$

where *R* is the radius of the quantum dot. The time independent Schrödinger equation can be written as:

$$\left[-\frac{\hbar^2}{2m}\nabla^2 + V(r) \right] \psi(r,\theta,\phi) = E\,\psi(r,\theta,\phi) \tag{2.9}$$

In terms of spherical coordinates if ∇^2 is split into in to $\frac{\partial^2}{\partial r^2}$ and momentum operator '*L*' which works only on *θ* and *Φ* such that $L = \vec{r} \times \vec{p}$, where $\vec{p}$ is the momentum operator, then equation 2.9 can be written as follows:

$$\left[-\frac{\hbar^2}{2mr^2}\frac{\partial}{\partial r}\left(r^2 \frac{\partial}{\partial r} \right) + \frac{L^2}{2mr^2} + V(r) \right] \psi(r,\theta,\phi) = E\,\psi(r,\theta,\phi) \tag{2.10}$$

If $\psi(r,\theta,\phi)$ is split into independent variables such that $\psi(r,\theta,\phi) = R_l(r) \cdot \Theta_l(\theta) \cdot \Phi_l(\phi)$ using separation of variables. If a spherical harmonics $Y_l^m(\theta,\phi)$ is introduced such that $Y_l^m(\theta,\phi) = \Theta_l(\theta) \cdot \Phi_l(\phi)$, then,

$$\psi(r,\theta,\phi) = R_l(r) \cdot Y_l^m(\theta,\phi) \tag{2.11}$$

Equation 2.10 can then be simplified as:

$$\left[-\frac{\hbar^2}{2mr^2}\frac{\partial}{\partial r}\left(r^2\frac{\partial}{\partial r}\right)+\frac{L^2}{2mr^2}+V(r)\right]R_l(r)\cdot Y_l^m(\theta,\phi) = E\cdot R_l(r)\cdot Y_l^m(\theta,\phi) \tag{2.12}$$

Since *L* operator only acts on *θ* and *Φ*, equation 2.12 can be re-written as follows:

$$\left[-\frac{\hbar^2}{2mr^2}\frac{\partial}{\partial r}\left(r^2\frac{\partial}{\partial r}\right)+V(r)\right]R_l(r)\cdot Y_l^m(\theta,\phi)+\frac{L^2}{2mr^2}R_l(r)\cdot Y_l^m(\theta,\phi) = E\cdot R_l(r)\cdot Y_l^m(\theta,\phi)$$

(2.13)

$\frac{L^2}{2mr^2}R_l(r)\cdot Y_l^m(\theta,\phi) = \frac{l(l+1)\hbar^2}{2mr^2}R_l(r)\cdot Y_l^m(\theta,\phi)$, then equation 2.13 becomes the following:

$$\left[-\frac{\hbar^2}{2mr^2}\frac{\partial}{\partial r}\left(r^2\frac{\partial}{\partial r}\right)+\frac{l(l+1)\hbar^2}{2mr^2}+V(r)\right]R_l(r)\cdot Y_l^m(\theta,\phi) = E\cdot R_l(r)\cdot Y_l^m(\theta,\phi) \tag{2.14}$$

Now that $Y_l^m(\theta,\phi)$ is a constant on both sides of the equation 2.20, it can be cancelled out and equation 2.14 then becomes the following:

$$\left[-\frac{\hbar^2}{2mr^2}\frac{\partial}{\partial r}\left(r^2\frac{\partial}{\partial r}\right)+\frac{l(l+1)\hbar^2}{2mr^2}+V(r)\right]R_l(r) = E\cdot R_l(r) \tag{2.15}$$

Multiplying equation 2.15 on both sides by $\frac{2m}{\hbar^2}$,

$$\left[-\frac{1}{r^2}\frac{\partial}{\partial r}\left(r^2\frac{\partial}{\partial r}\right)+\frac{l(l+1)}{r^2}+\frac{2m}{\hbar^2}V(r)\right]R_l(r) = \frac{2mE}{\hbar^2}R_l(r) \tag{2.16}$$

Substituting $k^2 = -\frac{2mE}{\hbar^2}$ and re-writing equation 2.16, we get:

$$\left[-\frac{1}{r^2}\frac{\partial}{\partial r}\left(r^2\frac{\partial}{\partial r}\right)+\frac{l(l+1)}{r^2}+\frac{2m}{\hbar^2}V(r)+k^2\right]R_l(r) = 0 \tag{2.17}$$

The left hand side of equation 2.17 can be further simplified as follows:

$$\frac{1}{r^2}\frac{\partial}{\partial r}\left(r^2\frac{\partial}{\partial r}\right)=\frac{1}{r^2}\left[r^2\frac{\partial^2}{\partial r^2}+2r\frac{\partial}{\partial r}\right]=\left[\frac{\partial^2}{\partial r^2}+\frac{2}{r}\frac{\partial}{\partial r}\right]$$

By applying the boundary condition where $V(r)=0$ for $r < R$, equation 2.17 can be written as follows:

$$\left[-\left(\frac{\partial^2}{\partial r^2}+\frac{2}{r}\frac{\partial}{\partial r}\right)+\frac{l(l+1)}{r^2}+k^2\right]R_l(r)=0 \tag{2.18}$$

If an arbitrary function is defined such that $R_l(r)=\frac{1}{\sqrt{kr}}J(kr)=\frac{1}{\sqrt{\rho}}J(\rho)$, then equation 2.18 can be re-written as follows:

$$\rho^2\frac{\partial J(\rho)}{\partial \rho^2}+\rho\frac{\partial J(\rho)}{\partial \rho}-\frac{J(\rho)}{4}-l(l+1)J(\rho)-\rho^2J(\rho)=0$$

$$\rho^2\frac{\partial J(\rho)}{\partial \rho^2}+\rho\frac{\partial J(\rho)}{\partial \rho}-\left[\rho^2+(l+\frac{1}{2})^2\right]J(\rho)=0 \tag{2.19}$$

Equation 2.19 is a modified Bessel function which has two independent solutions $I_{l+\frac{1}{2}}(x)$ and $K_{l+\frac{1}{2}}(x)$. The solution $I_{l+\frac{1}{2}}(x)$ is neglected as it grows exponentially as $r\to\infty$. The other solution $K_{l+1/2}(x)$ can be written as following:

$$R_l(r)\approx\frac{1}{\sqrt{kr}}K_{l+\frac{1}{2}}(kr) \tag{2.20}$$

The solution of equation 2.17 can then be written as follows:

$$\psi(r,\theta,\phi)=N\cdot K_l(r)Y_l^m(\theta,\phi) \tag{2.21}$$

where, N is the normalization constant, $K_l(r)$ is the spherical Bessel function and $Y_l^m(\theta,\phi)$ is the spherical harmonics. The discrete energy levels can be written as following:

$$E_{nl} = \frac{\hbar^2 k_{\ln}^2}{2mr^2} \tag{2.22}$$

where '*l*' and '*n*' are integers and *l* is considered the orbital number similar to the atomic orbitals and are (*2l+1*) folds degenerate for each level, '*m*' is the mass of the charge and '*r*' is the radius of the sphere. The orbital levels *l* = 0, 1, 2, 3….. can also be written as *l* = ***s, p, d, f***…etc similar to atomic orbitals.

The main consequence of quantum confinement of charges in the quantum dots is that the electronic structure consists of series of discrete energy levels. For a quantum dot, the first unoccupied energy level has a two-fold degeneracy; the second has six-fold degeneracy and so on. This is very similar to atomic degenerate energy orbitals ***s*** and ***p***, and thus these quantum dots are also called "*artificial atoms*" [2.2]. By changing the size of these quantum dots, it is possible to engineer their electronic properties.

The above section detailed the size quantization in quantum dots. The next section will deal with transport of electrons through these discrete energy levels of the quantum dots by tunneling.

2.3 Resonant tunneling theory

2.3.1 Tunnel junctions

Tunnel junctions form one of the most essential elements in tunneling experiments. A tunnel junction is a circuit element consisting of two conductors which are separated by a thin dielectric layer. A tunnel junction can be represented by a capacitor and resistor connected in parallel. The main difference of this capacitor from a classical capacitor is that this capacitor allows electron flow when only energetically favorable. Also, the tunnel resistor is not completely ohmic, it allows electrons to flow but only one at a time, or discrete flow. Figure 2.2 shows schematically a tunnel junction with the equivalent circuit diagram.

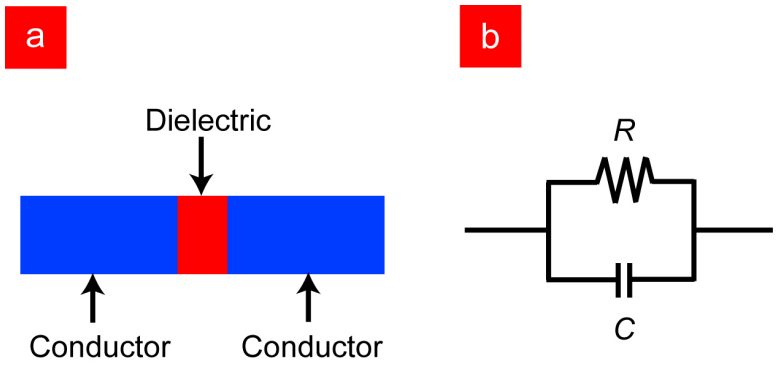


Figure 2.2: (a) Schematic of a tunnel junction. (b) Equivalent circuit diagram

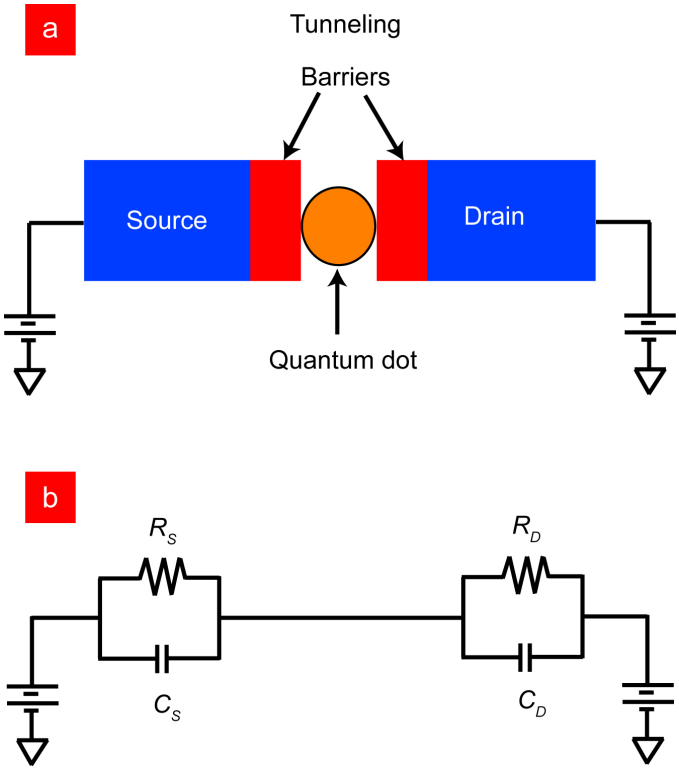


Figure 2.3: (a) Schematic of double barrier tunnel junction where quantum dot is placed between two metal electrodes separated by thin tunneling barriers. (b) Equivalent circuit diagram.

2.3.2 Double barrier tunnel junctions (DBTJ)

A double barrier tunnel junction is formed when a quantum dot is placed between two metal electrodes separated by thin tunneling barriers as shown schematically in figure 2.3 (a). The equivalent circuit diagram for the DBTJ is shown in figure 2.3 (b), it can be represented by two individual tunnel junctions in series. An electron can tunnel from the source electrode into the quantum dot and then from the quantum dot into the drain electrode.

Figure 2.4 shows the schematic of two metal electrodes with a quantum dot placed between these electrodes separated by tunneling barrier. The fermi levels of the two electrodes are ε_f^S and ε_f^D . When ε_f^S and ε_f^D are not equal due to an applied bias of eV_{DS}, the system is in a non-equilibrium state and there is a net current flow through the system.

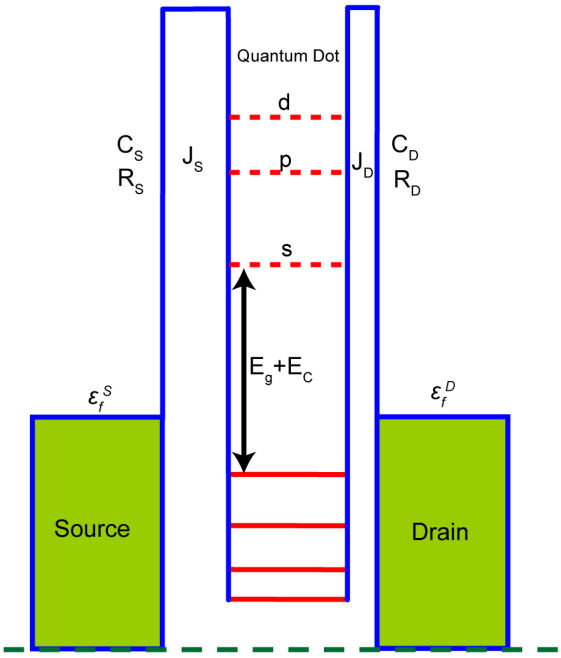


Figure 2.4: Schematic of a double barrier tunnel junction with two metal electrodes with fermi levels ε_f^S and ε_f^D , quantum dot placed in between these electrodes separated by thin dielectric tunneling barriers.

2.3.3 Resonant tunneling spectroscopy

This section will detail how resonant tunneling spectroscopy is performed using the double barrier tunnel junction and its two limiting cases. Tunneling spectroscopy using the DBTJ approach has been dealt in detail including derivations of expressions for tunneling rates, current etc., previously for STM spectroscopy [2.3-2.21]. In this work, energy diagrams will be used for ease of illustration of the tunneling process. Figure 2.4 shows the DBTJ formed when the quantum dot is placed between the source and the drain electrodes separated by thin tunneling barriers. The two tunneling junctions are characterized by their capacitances, C_S, C_D and their resistances, R_S, R_D corresponding to the source to quantum dot and the quantum dot to the drain junctions respectively. The tunneling rates Γ^S, Γ^D across these two junctions are the two main controlling factors for the spectroscopic measurements. Based on the junction capacitance and resistance, the tunneling rate through one junction, be it the source junction or the drain junction, the tunneling current is limited by one of these junctions. Two limiting cases shall be examined closely, namely:

1. Shell-tunneling case ($\Gamma^S << \Gamma^D$), and,
2. Shell-filling spectroscopy ($\Gamma^S >> \Gamma^D$)

1. Shell tunneling regime [2.22-2.24] ($C_S << C_D$ and $R_S >> R_D$): In this case, the tunneling rate from the source to the quantum dot Γ^S is the limiting factor for tunneling current. The tunneling rate in the junction between the drain electrode and the quantum dot (Γ^D) is much faster than the tunneling across the junction from the source electrode to the quantum dot (Γ^S). This case is shown schematically using an energy diagram as an aid in figure 2.5. The bias drop occurs across the source electrode to the

quantum dot junction (J_S), hence when a positive bias is applied on the drain electrode, the energy levels of the quantum dot move with the corresponding bias. If there exists some bias drop across the drain to the quantum dot junction (J_D), then the movement of the energy levels of the quantum dot will be a fraction of the applied bias. This fraction of the applied bias that drops across the source to QD junction is termed as the η factor and can be defined as follows:

$$\eta \equiv \frac{V_S}{V_S + V_D} = \frac{C_D}{C_S + C_D} \tag{2.23}$$

When the positive source-drain bias is applied (eV_{SD}), the fermi level of the electrode can align itself with the empty energy level of the quantum dot as shown in figure 2.5.

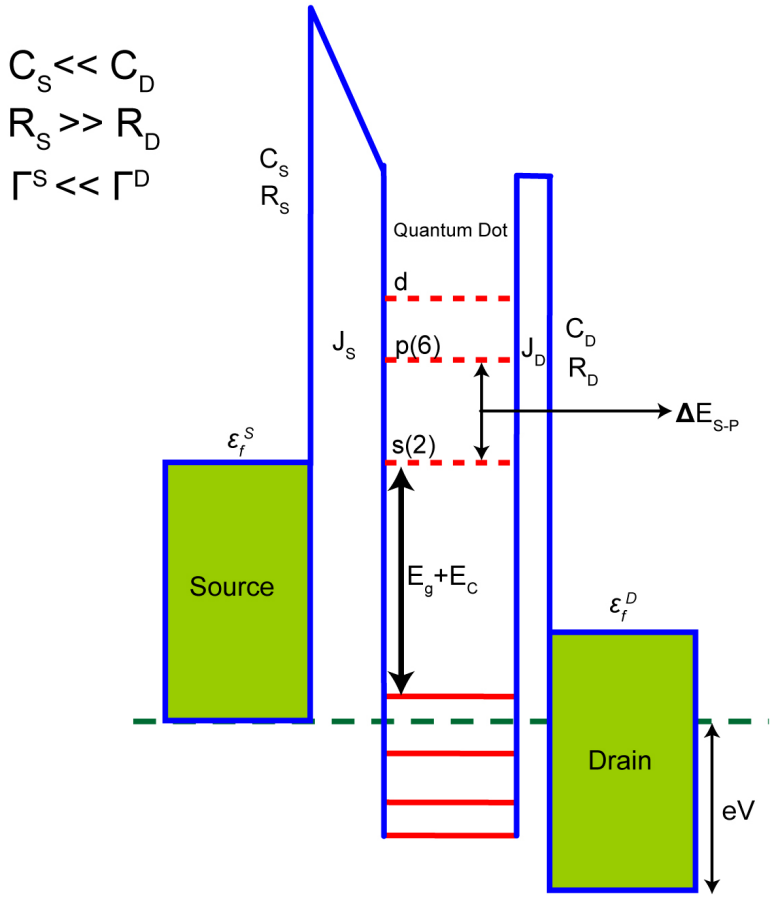


Figure 2.5: Shell-tunneling regime: Energy level (s) of quantum dot aligned with the source electrode. An electron can now tunnel from source electrode into any of the two available states in the '*s*' level.

Once the energy level of the quantum dot is aligned with the metal electrode, a tunneling channel opens and an electron from the source electrode tunnels into the quantum dot. This causes a step-wise increase in the tunneling current and corresponding peak in the conductance spectra. An electron of any spin can occupy any of the two available states in the 's' level. Addition of the one extra electron into the 's' level breaks the degeneracy of the energy level as shown in figure 2.6. Once an extra electron is added to the quantum dot, the electrostatic potential of the quantum dot rises up due to the extra electron inside the quantum dot. This prevents the addition of any more excess electrons. The energy difference between the occupied state and

the available state in the ‘s’ level is then given by the charging energy E_C. In the shell-tunneling regime, the extra electron in the quantum dot immediately tunnels out of the quantum dot into the drain electrode as the tunneling rate across the QD/drain junction is very fast. The transition of the electron from the source electrode into the quantum dot is shown using the energy diagram in figures 2.6.

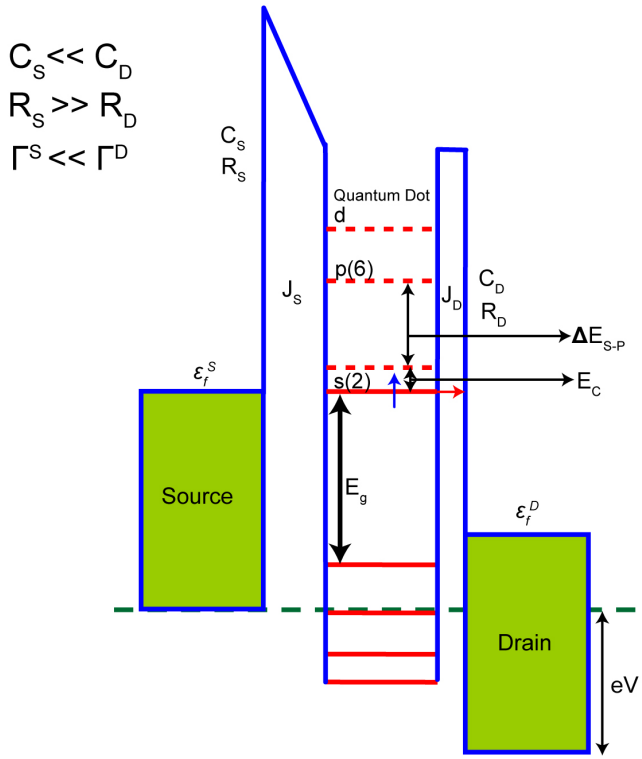


Figure 2.6: Shell-tunneling regime: One electron occupies one out of two available states in the ‘s’ level thereby raising the electrostatic potential of the quantum dot.

Once the electron tunnels out of the quantum dot into the drain electrode, it is restored back to the same configuration as shown in figure 2.5. As the tunneling rate out of the quantum dot is much faster than the rate tunneling into the QD, the probability of finding an excess electron in the quantum dot, given by the equation 2.24 below, is zero.

$$P(l) = \frac{2\Gamma_l^S}{\left(2\Gamma_l^S + \Gamma_l^D\right)} \tag{2.24}$$

The most probable configuration of this system in the positive bias would then be as shown in figure 2.5.

As the bias is increased further, the next energy level, i.e., the '*p*' level can now align with the source electrode as shown in figure 2.7. In this case, there are two available states in the 's' level and six additional states in the 'p' level for the electron to occupy in the quantum dot. This causes another step-wise increase in the tunneling current and corresponding peaks in the conductance spectra.

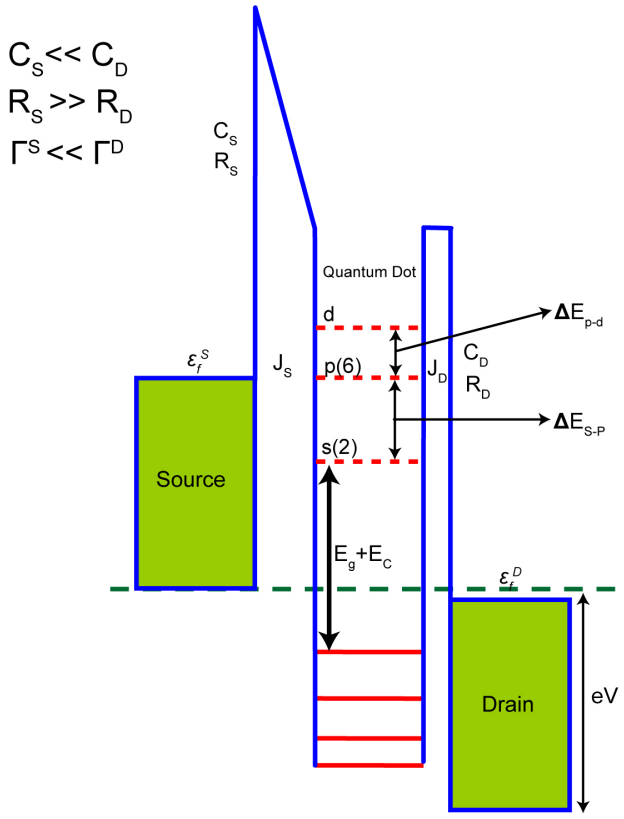


Figure 2.7: Shell-tunneling regime: Source electrode now aligned with the next energy level ('p' level) of the QD.

In the negative bias, the rate of electrons tunneling through the drain/QD junctions is faster; hence, the rate tunneling into the QD is much faster than the rate tunneling out. By applying the negative bias, the occupied energy levels or the valence levels of the QD can be aligned with the source electrode as shown in figure 2.8. Once an electron from the occupied level tunnels into the source electrode, the electrostatic potential of the QD drops by an amount equal to the charging energy as shown in figure 2.9. This allows another electron to immediately tunnels into the QD, thereby maintaining the most probable configuration as shown in figure 2.8.

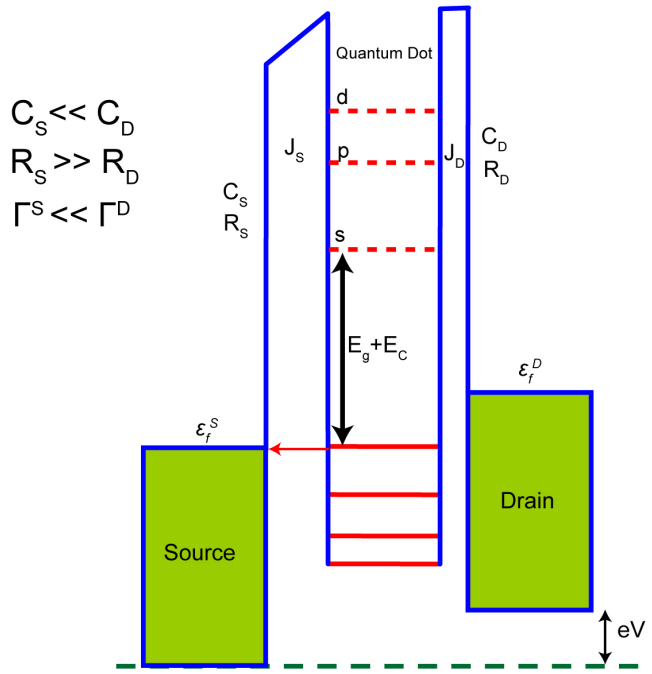


Figure 2.8: Shell-tunneling regime: By applying a negative bias, the valence energy levels of the QD can be aligned with the source electrode.

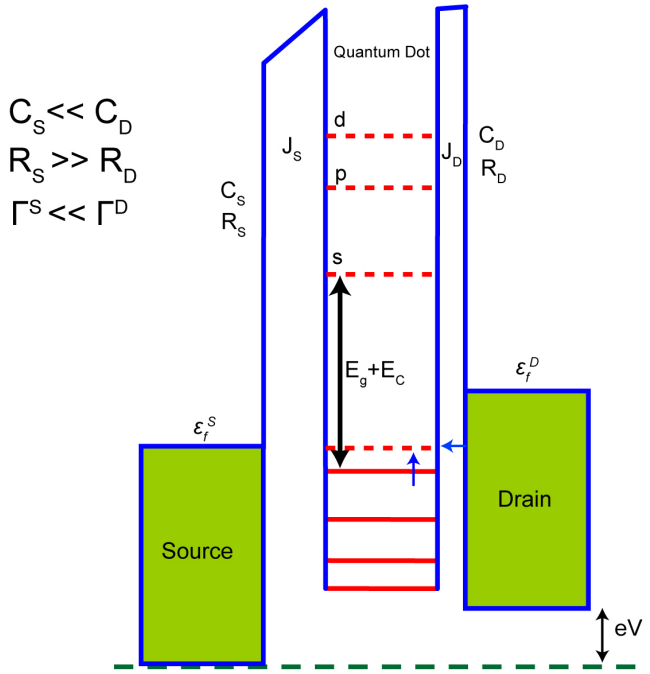


Figure 2.9: Shell-tunneling regime: The electrostatic potential of the QD drops by the charging energy when one electron tunnels into the drain electrode.

The most probable configuration maintained in this scenario is shown in figure 2.8 where the quantum dot occupied energy level is aligned with the source electrode. The tunneling current is limited by the rate of electrons tunneling out of the quantum dot Γ^S . The tunneling current will be dealt with in later section in this chapter.

2. Shell-filling regime [2.25-2.28] ($C_S << C_D$ and $R_S << R_D$): In this case, the tunneling rate from the drain to the quantum dot Γ^D is the limiting the tunneling current. The tunneling rate in the junction between the source electrode and the quantum dot (Γ^S) is much faster than the tunneling across the junction from the drain electrode to the quantum dot (Γ^D). This case is shown schematically using an energy diagram as an aid in figure 2.9.

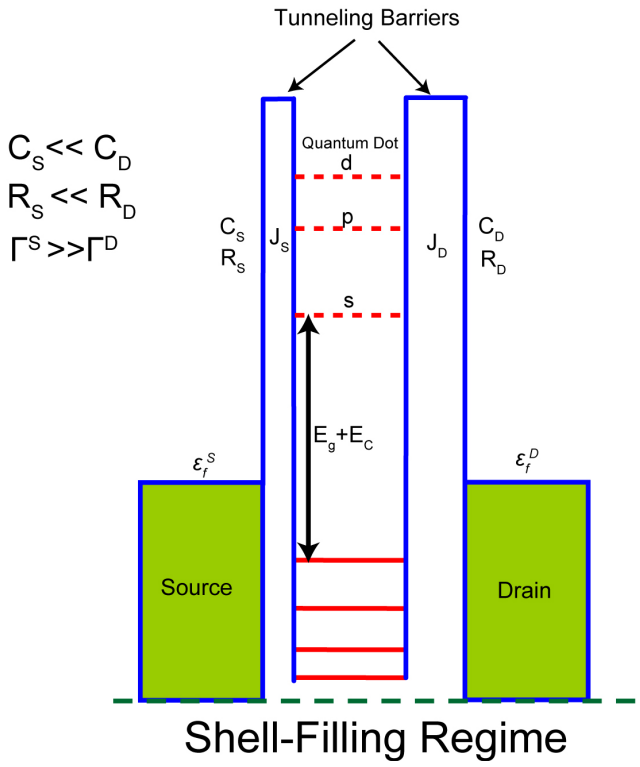


Figure 2.10: Shell-filling regime: $C_S << C_D$, $R_S << R_D$ and $\Gamma^S >> \Gamma^D$.

When a bias is applied, the energy level of the quantum dot can be aligned with the source electrode as shown in figure 2.11. Once an electron tunnels from the source electrode into the QD, the electrostatic potential is raised and it also breaks the degeneracy in the 's' level as shown in figure 2.12. The difference in the energy between the occupied state and the unoccupied state in the 's' level is the charging energy. Unlike the shell tunneling regime, in this case the rate of tunneling through the QD/drain junction is much slower. Hence, the probability to find an extra electron, given by equation 2.26, becomes close to unity. This additional electron in the QD causes a step-wise increase in the tunneling current and corresponding peaks in the conductance spectra. As the bias is further increased, as shown in figure 2.13, another electron can tunnel into the QD and occupy the other available state in the 's' level. This again causes another step-wise increase in the tunneling current and corresponding peak in the conductance spectra. Once the second additional electron is added to the

QD, the electrostatic potential raises up again and this prevents any additional electrons being added to the QD. This is shown in figure 2.14.

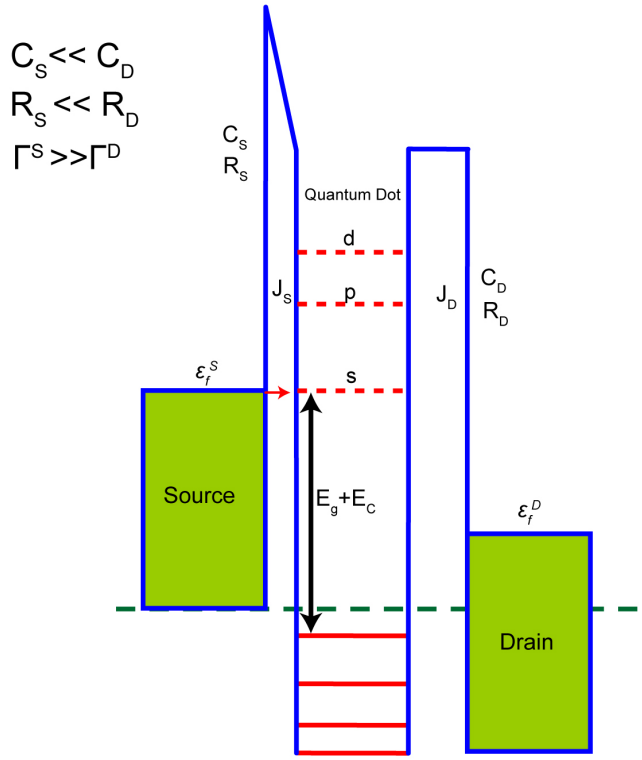


Figure 2.11: Shell-filling regime: Energy level (s) of quantum dot aligned with the source electrode. An electron can now tunnel from source electrode into any of the two available states in the '*s*' level.

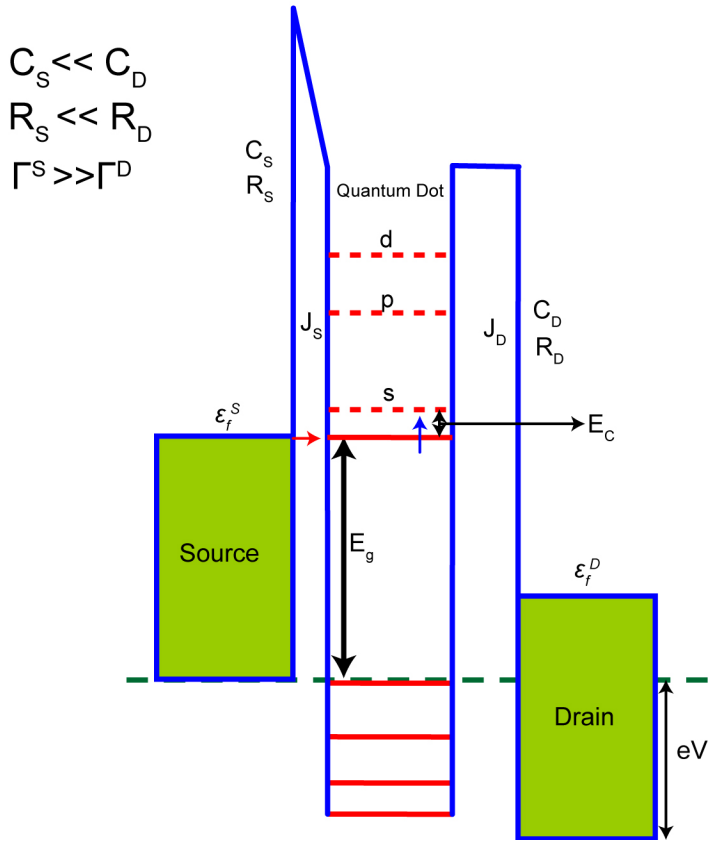


Figure 2.12: Shell-filling regime: One electron occupies one out of two available states in the '*s*' level thereby raising the electrostatic potential of the quantum dot. Addition of electron breaks the degeneracy of the 's' level and raises it by charging energy E_C.

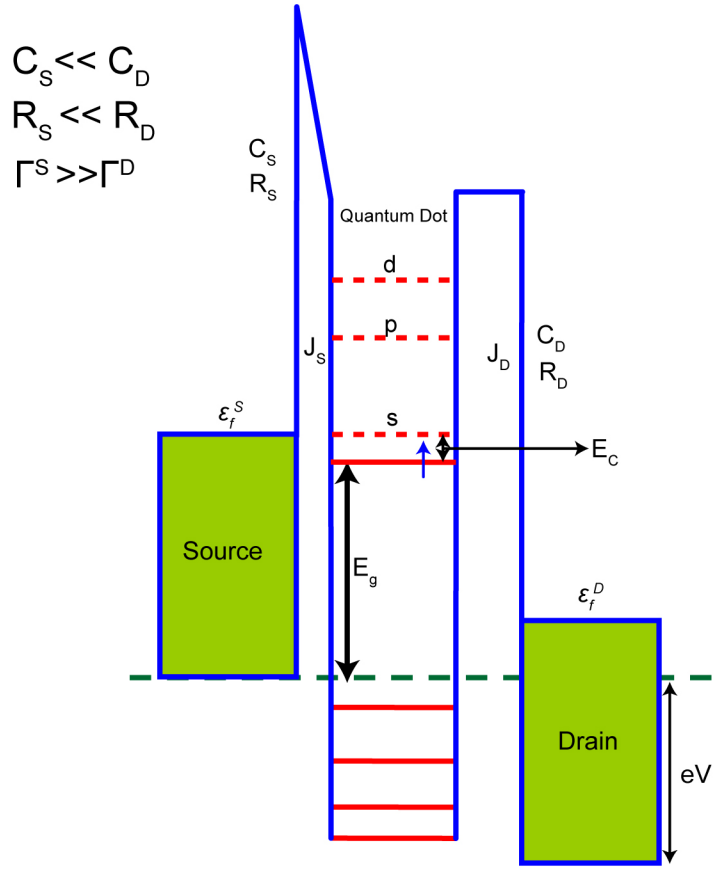


Figure 2.13: Shell-filling regime: When the bias is further increased by the charging energy E_C, another electron of opposite spin can occupy the second available state in the ‘s’ level.

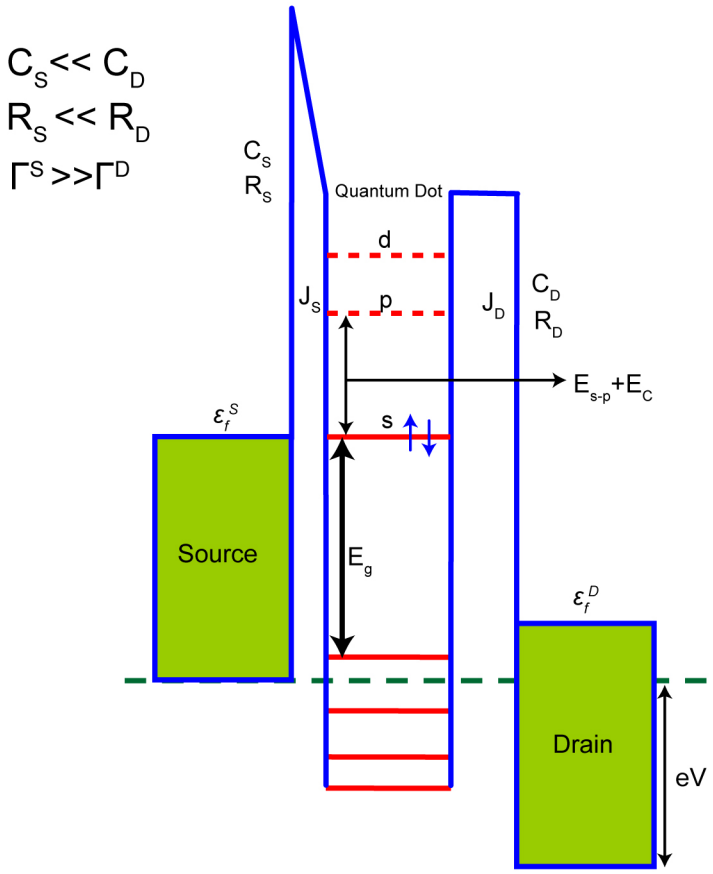


Figure 2.14: Shell-filling regime: After the addition of the second electron into the ‘s’ level, the electrostatic potential is raised up preventing addition of any more electrons into the QD.

When the bias is increased further, the second available energy level (‘p’ level) in the QD can be aligned with the source electrode as shown in figure 2.15. Once aligned, an electron of any spin tunnels into the QD, thus breaking the degeneracy of the level. This raises the electrostatic potential of the QD thus preventing addition of any more electrons in the QD. The difference in the energy between the occupied and unoccupied states in the ‘p’ level is the charging energy. If the bias is increased further by the charging energy, then another electron tunnels into one of the five remaining states of the ‘p’ level. This now leaves four unoccupied states in the ‘p’ level separated

from the occupied states by the charging energy as shown in figure 2.16. The same can be conducted in the negative bias as explained for the shell-tunneling regime.

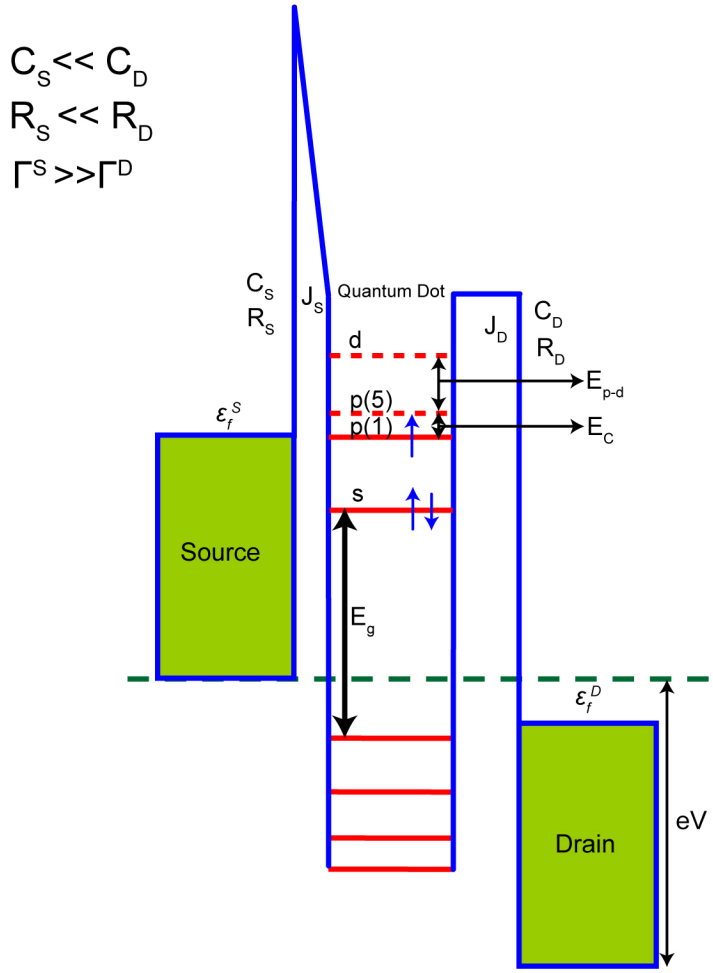


Figure 2.15: Shell-filling regime: Addition of one electron into the ‘p’ level breaks the degeneracy of the level and splits the level by the amount equal to the charging energy.

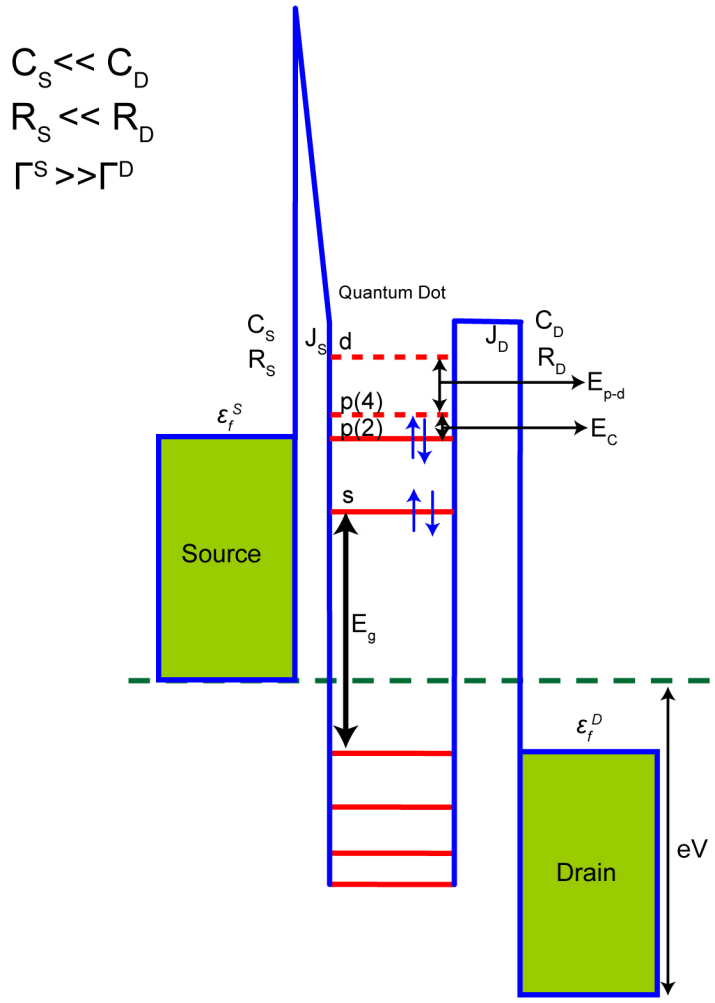


Figure 2.16: Shell-filling regime: Two occupied states in the 'p' level separated from the four unoccupied states by the charging energy.

From the current-voltage and conductance spectra, the energy level spacing of the QD can be directly deciphered as long as the voltage division factor η is known. Even if not known, the η factor can be calculated from the measured spectrum and the optical spectroscopy data. This calculation will be detailed in the next section. Figures 2.17 and 2.18 show the shell-filling and shell-tunneling current-voltage and conductance spectra for CdSe quantum dots (3.9nm) and InAs quantum dot (3.2nm) measured using the STM spectroscopy at 4.5K.

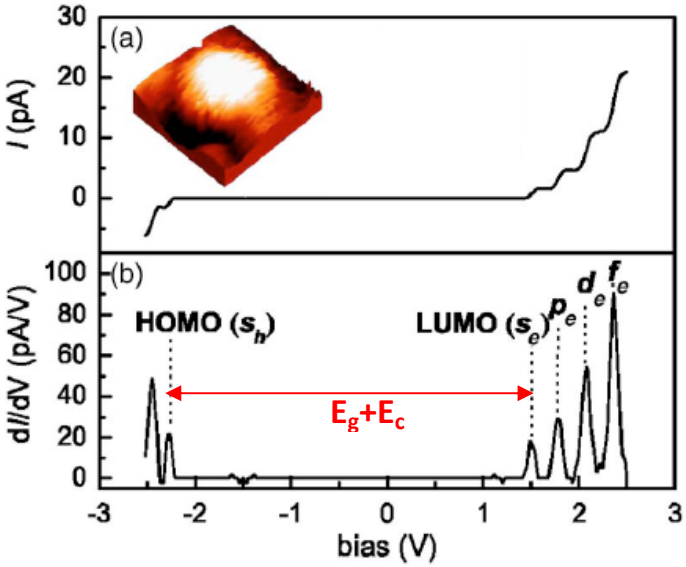


Figure 2.17: Shell-tunneling spectroscopy data for a 3.9nm CdSe using STM spectroscopy measured at 4.5K.

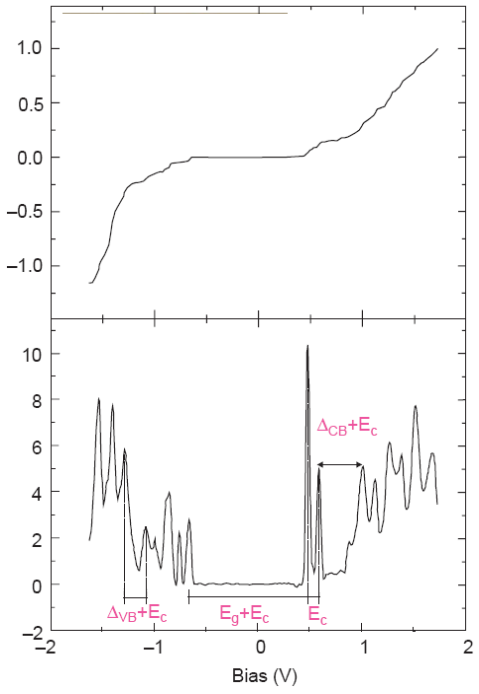


Figure 2.18: Shell filling spectroscopy data for InAs QD 3.2nm using STM spectroscopy at 4.2K. Doublet peaks for the ‘s’ level and six peaks for the ‘p’ level show the shell-filling spectra. Doublet peaks are separated only by charging energy, whereas peak to peak separation is energy level spacing plus the charging energy.

2.4 Mapping the energy level structure

The DBTJ approach to mapping the energy structure of the quantum dot was discussed in section 2.3. This section will detail how to measure the energy level separations from the measured current-voltage and differential conductance spectra. In order to exactly measure the energy level separations of the QD, the η factor has to be determined. The following steps will show how to determine the η factor from the measured conductance spectra.

The charging energy E_C can be calculated using the following expression:

$$E_C = \frac{e^2}{C_{self}} = \frac{e^2}{4\pi\varepsilon_0\varepsilon_{out}R} \tag{2.25}$$

where, e is the charge of an electron, ε_0 is the permittivity of free space, ε_{out} is the dielectric constant of the surrounding dielectric medium, C_{self} is the self-capacitance of the quantum dot defined by $C_{self} = 4\pi\varepsilon_0\varepsilon_{out}R$ and R is the radius of the quantum dot. This charging energy is the energy required to add an extra electron to the neutral quantum dot.

A common approximation of the electrostatic energy of a quantum dot occupied with *n* electrons and *p* holes with respect to the neutral states can be written in the form as follows [2.21]:

$$E\left(\{n_i\},\{p_i\},V\right) = \sum_i n_i\varepsilon_i^e - \sum_i p_i\varepsilon_i^p + \frac{e^2}{2C_{self}}q^2 + \eta eVq \tag{2.26}$$

$$E\left(\{n_i\},\{p_i\},V\right) = \sum_i n_i\varepsilon_i^e - \sum_i p_i\varepsilon_i^p + \frac{1}{2}E_c q^2 + \eta eVq \tag{2.27}$$

where ε_i^e and ε_i^p are the conduction and valence energy levels, n_i and p_i are the electron and hole occupation numbers $\left(n = \sum_i n_i,\ p = \sum_i p_i\right)$, $q = p - n$, E_C is the charging energy

defined by $E_C = \frac{e^2}{C_{self}} = \frac{e^2}{4\pi\varepsilon_0\varepsilon_{out}R}$ and $\eta = \frac{C_D}{C_S + C_D}$ is the ratio of bias drop across the junction between the source electrode and the quantum dot. The tunneling of an electron between the electrodes and the energy level ε_i is determined by the position of the Fermi levels with respect to the transition level in the quantum dot which is given by:

$$\varepsilon_i^e(q \mid q-1,V) = E(n_i = 1,\{p_i\},V) - E(n_i = 0,\{p_j\},V)$$

$$\varepsilon_i^e(q \mid q-1,V) = \varepsilon_i^e + \eta eV + E_C\left(\frac{1}{2} - q\right) \tag{2.28}$$

Similarly, the tunneling of holes through the transition levels in the quantum dot and can be given by:

$$\varepsilon_i^p(q \mid q+1,V) = \varepsilon_i^p - \eta eV - E_C\left(\frac{1}{2} + q\right) \tag{2.29}$$

The transition levels $\varepsilon_1^p(+1 \mid 0,V), \varepsilon_i^e(0 \mid -1,V)$ correspond to the injection of an electron and hole into the lowest unoccupied energy level and the highest occupied energy level respectively. When the applied bias is zero (V = 0, q = 0):

$$\varepsilon_i^e(0 \mid -1) = \varepsilon_i^e + \frac{E_C}{2} \tag{2.30}$$

$$\varepsilon_i^p(+1 \mid 0) = \varepsilon_i^p - \frac{E_C}{2} \tag{2.31}$$

The energy gap (E_g), combining with equations 2.30 and 2.31 now becomes the following:

$$E_g^{meas} = \varepsilon_1^e - \varepsilon_1^p + E_C \tag{2.32}$$

where E_C is the charging energy of the quantum dot.

The measured energy gap E_g^{meas} from the conductance spectra is defined as the energy separation between the first peak in the conduction level and the first peak in the valence level

which contains the charging energy. To get the absolute band gap E_g of the quantum dot, the charging energy must be removed from the measured energy gap. Hence, the real band gap from the tunneling spectroscopy is obtained as follows:

$$E_g = E_g^{meas} - E_C \tag{2.33}$$

The optical gap can be determined from the first peak in the optical absorption spectroscopy. The optical band gap is related to the measured band gap in the resonant tunneling spectroscopy by the following relation [2.19]:

$$\eta E_g = E_g^{opt} + J_{e-h} \tag{2.34}$$

where J_{e-h} is the electron-hole coulomb interaction energy, E_g^{meas} is the measured energy band gap in the resonant tunneling measurements. This interaction energy J_{e-h} can be approximately calculated by the following [2.19]:

$$J_{e-h}(R) = \left(\frac{1}{\varepsilon_{out}} + \frac{0.79}{\varepsilon_{in}} \right) \cdot \frac{e^2}{4\pi\varepsilon_0 R} \tag{2.35}$$

where J_{e-h} is the electron-hole coulomb interaction energy, ε_{in} is the dielectric constant of the bulk material of the QD, ε_{out} is the dielectric constant of the surrounding dielectric (organic capping layer of the QD).

The η factor can then be determined from the literature data for the optical band gap for the QD under study, calculating the electron-hole interaction energy, and the measured energy gap E_g^{meas} from the tunneling spectroscopic measurement as follows:

$$\eta = \frac{E_g^{opt} + J_{e-h}}{E_g} \tag{2.36}$$

Depending on the junction capacitances ratio η or the voltage division factor, the differential conductance peaks are offset in actual measurements. Using the analogy of the

STM for simple illustration, the variation of the peak separations based on different η factors can be shown in figure 2.19. If the tip is retracted from the QD, figure 2.19 (a), most of the bias drops in the QD/tip (source) junction, leading to a high η factor close to unity. Hence, the peak separations are closer to the applied bias. In the case when the tip is closer to the QD, figure 2.19 (b), the bias drop occurs symmetrically across both the junctions around the quantum dot $\eta = 0.5$. In this case, for a bias drop across the tip/QD junction of 1V, actual applied bias needs to be 2V. As a result of this symmetric barrier, the peak to peak energy separations will also appear higher unless corrected for the η factor. The η factor thus also affects the conductance peak widths as a result. For η factors close to unity, the peaks will appear sharper compared to lower η factor values.

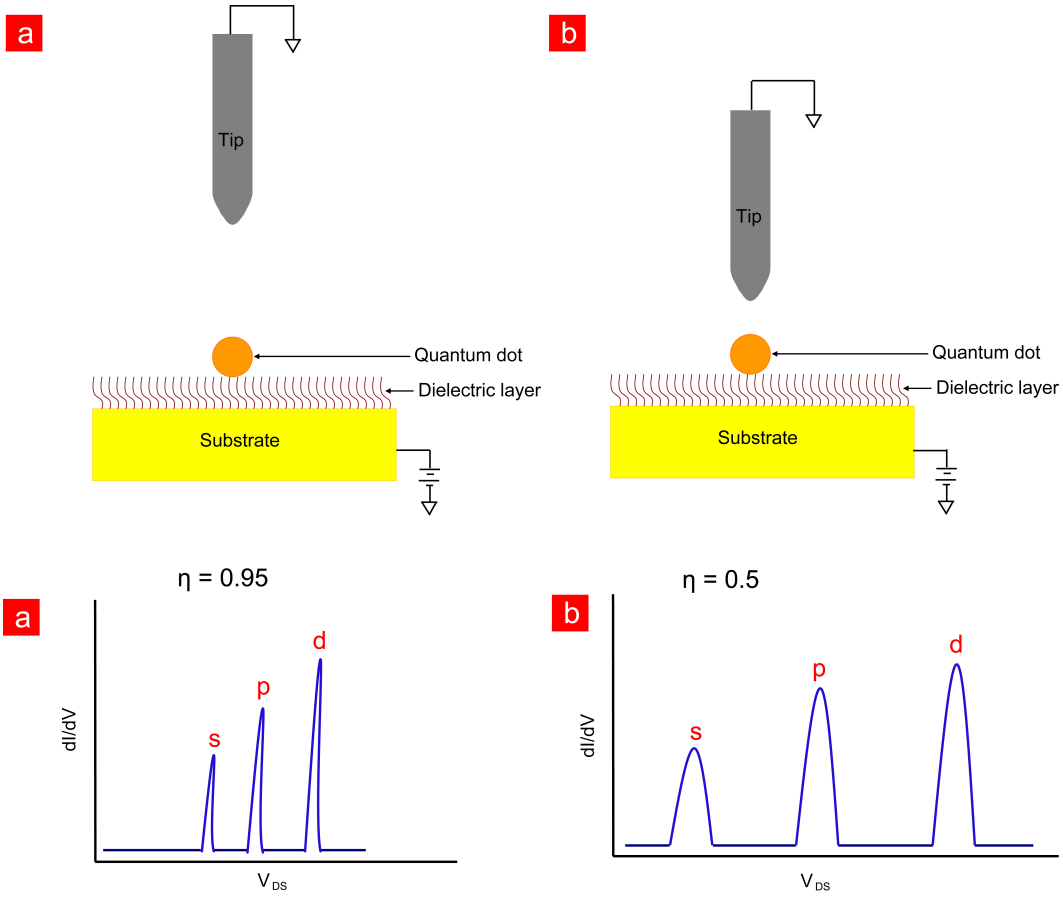


Figure 2.19: η factor analogy using STM tip to quantum dot separation. (a) The tip is retracted further away from the QD, thus, most of the bias drops across this junction leading to a η factor close to unity. (b) Tip is closer to the QD leads to equal bias drop across both the junction leading to smaller η factor, thereby increasing the peak to peak spacings.

Ideally, for spectroscopic measurements, η factor close to unity would make measurements simpler. For smaller η factor, more actual bias would have to be applied which could cause complications, such as instability in tunneling currents, leakage currents etc., depending on the structure of the DBTJ measurement unit.

The energy level separations can then be directly obtained by multiplying the η factor with the measured values from the peak to peak separation values in the conductance plots.

For example, if the measured ‘s’ to ‘p’ level separation was 100 meV, the η factor was 0.95, then the actual energy level spacing is 95 meV.

In conclusion for this chapter, the theory of quantum confinement, discrete energy levels of quantum dots, tunneling concepts including tunneling through double barrier tunnel junctions were presented. Using simple energy diagrams, the way to interpret the tunneling and conductance spectra was also detailed. Tunneling and conductance spectra is very complicated and affected by various factors such as junction capacitances, tunneling rates etc, so it is important to completely understand the underlying fundamentals to correctly interpret the tunneling and conductance spectra. The next chapter will discuss about the other predominantly used spectroscopic techniques for mapping the energy level structure of quantum dots.

CHAPTER 3

SPECTROSCOPY FOR QUANTUM DOTS

3.1 Introduction

In this chapter we look at the brief overview of quantum dot spectroscopy and most recent and widely employed spectroscopic techniques. This will be followed by the introduction of the proposed spectroscopic technique which is aimed at incorporating the advantages of other techniques to study directly the energy levels of individual quantum dots.

3.2 Overview of spectroscopic techniques

3.2.1 Optical spectroscopy

The most widely employed spectroscopic technique is optical spectroscopy. Spectroscopic measurements can be done either in absorption mode or photoluminescence mode. Figure 3.1 shows the optical spectra for both absorption and emission spectra for CdSe quantum dots of different sizes. The quantum dot samples are irradiated with white light. Due to the presence of quantized energy states in the quantum dots, the electrons in the ground state (occupied energy levels) in the quantum dot absorb the energy from photons and move into the distinct excited states (unoccupied energy levels). The wavelength of light absorbed is recorded and the absorption spectroscopy accomplished. These excited electrons eventually relax to their ground state and in the process, release the energy in the form of photons. By observing the energy of these emitted photons, photoluminescence spectroscopy is accomplished. The lowest energy absorbed is given by the energy difference between the lowest unoccupied

energy level (LUMO) and the highest occupied energy levels (HOMO). This energy gap is also called the band gap of the quantum dot. Optical spectroscopy can now also be performed on individual quantum dots [3.1-3.3]. These measurements are conducted at cryogenic temperatures and the resolution of the spectra can be up to a few μeV. Figure 3.2 shows the optical photoluminescence spectra accomplished for a single 4.5nm CdSe quantum dot [3.2].

The main disadvantage of this technique is it utilizes complex selection rules to obtain the energy structure based on the absorption or emission spectra. Using complex models and certain selection rules for allowable energy transitions, the complete electronic structure of the quantum dots can be obtained from the absorption spectroscopic technique. It is, however, difficult to separately investigate the electron and hole energy levels of the quantum dot by optical spectroscopy as it inherently involves transition between two levels and involves selection rules to get the energy level separations, so this technique is an indirect measurement technique.

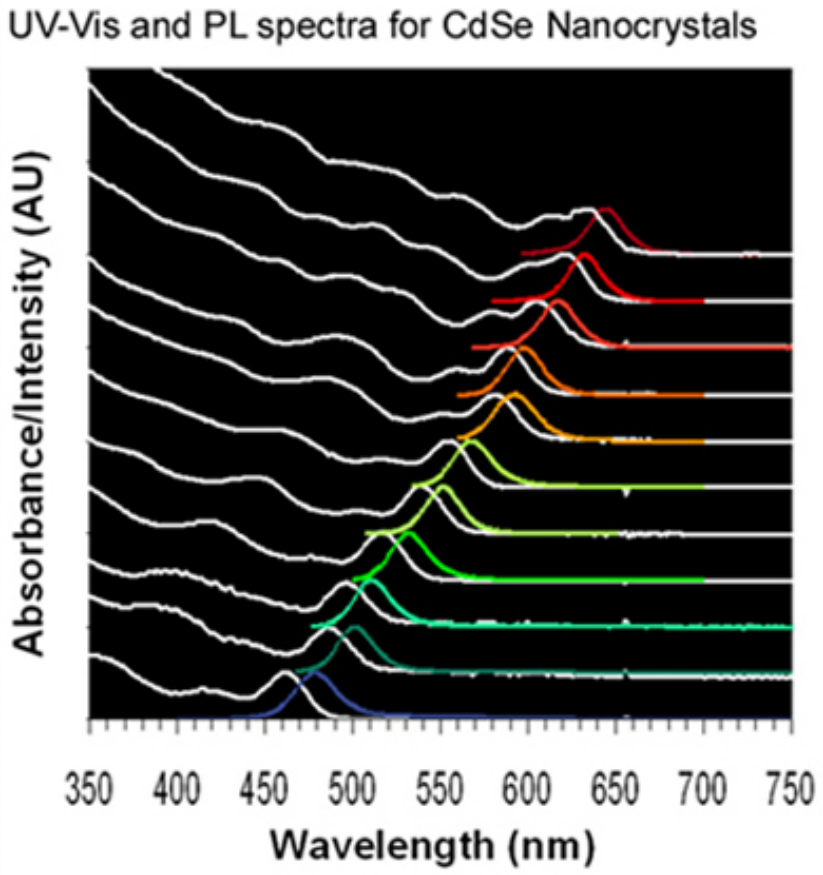


Figure 3.1: Absorption and photoluminescence (PL) spectra for CdSe quantum dots 2nm – 8nm in size [3.4], with the emission spectra shown in color for each individual sized quantum dots. The higher energy or smaller diameter quantum dots proceed from the bottom up to the top where the larger diameters/ lower energy quantum dots are shown.

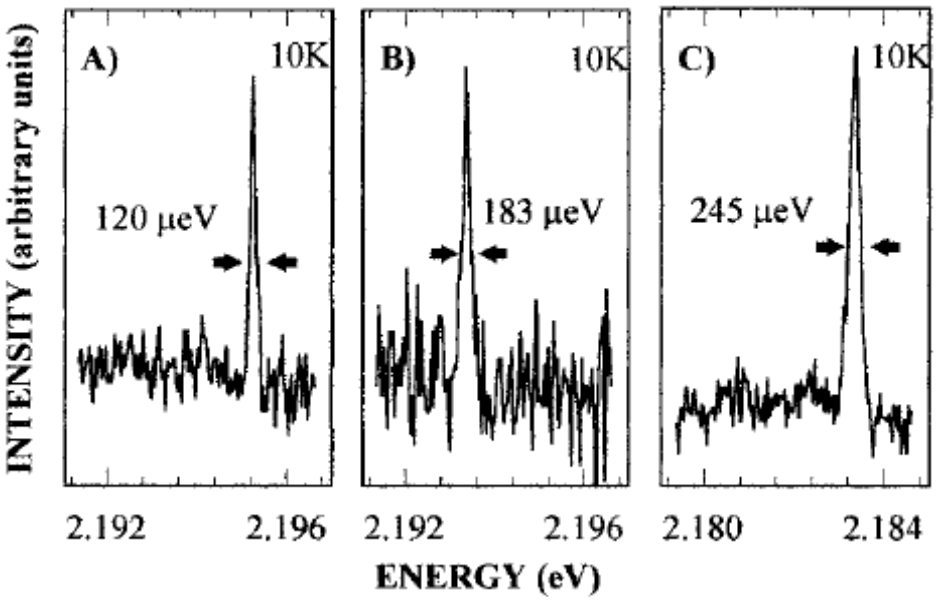


Figure 3.2: Photoluminescence spectra for single 4.5nm CdSe quantum dot at different intensity of incident light which shows resolution of a few μeV (A –C) Spectra obtained with 1 min integration time and at 314, 150, and 65 W/cm^2 excitation intensity respectively, [3.2].

3.2.2 Tunneling electron spectroscopic techniques

To directly probe the electronic structure of individual quantum dots, scanning probe spectroscopic techniques are employed [3.5-3.18]. Double barrier tunnel junctions (DBTJ) are formed when the quantum dot is placed between two electrodes separated by thin tunneling barriers. This forms the basis for tunneling spectroscopic measurements. The easiest method of forming the DBTJ is by using scanning probe techniques such as Scanning tunneling microscope (STM). Figure 3.3 shows the DBTJ approach using the STM or this can be simply called as scanning tunneling spectroscopy (STS). An energy diagram for this DBTJ spectroscopy method is shown schematically in figure 3.4.

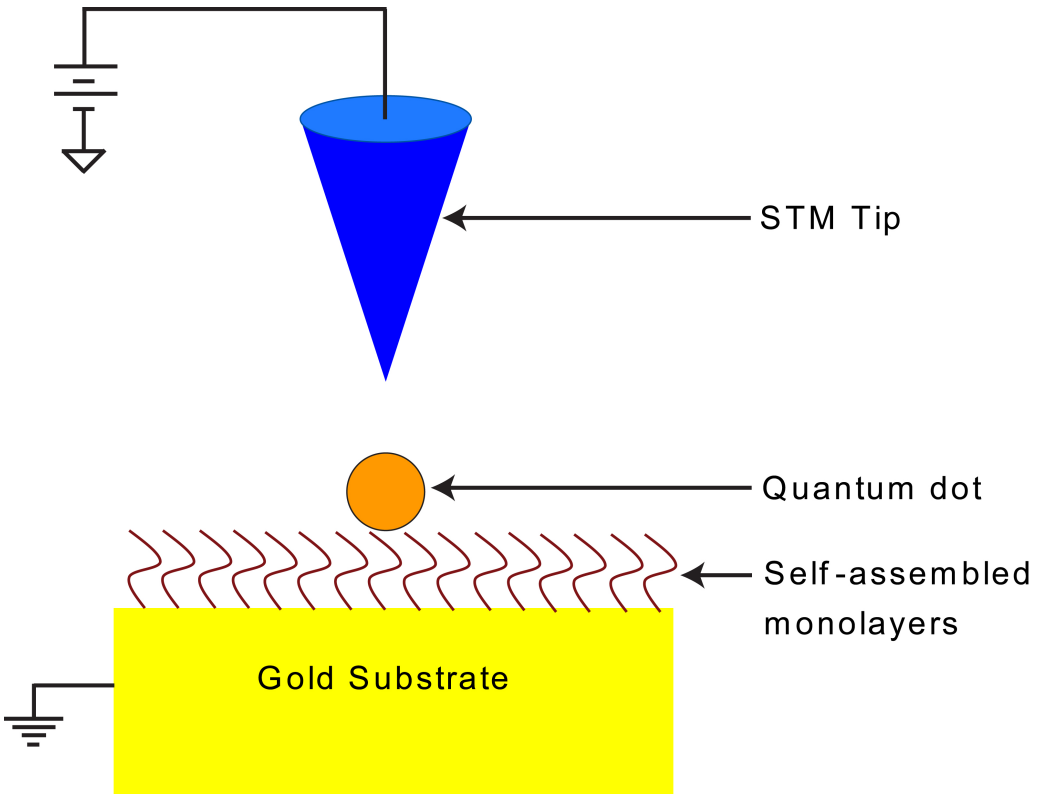


Figure 3.3: Scanning Tunneling Spectroscopy using the DBTJ approach with the electrodes being the conductive substrate and STM tip. Quantum dot/nanoparticle is tethered to the conducting substrate by thin self-assembled monolayer.

A conductive substrate and the STM tip act as the two electrodes. A quantum dot is placed or anchored on the conducting substrate by either electrodepositing the quantum dot directly onto the substrate or by the attaching the colloidal quantum dots using self-assembled monolayers. This organic monolayer acts as the dielectric tunneling barrier between the substrate and the quantum dot. Individual quantum dots are first located by a simple scan of the surface. Once the tip is positioned on top of the quantum dot of interest, the feedback loop is turned off. The tip to dot separation can be varied by altering the tunneling current set-point. This also changes the junction parameters for the DBTJ. Now, by sweeping the source to drain bias, tunneling current is monitored. When one of the electrodes aligns itself with an available energy level in the quantum dot, a tunneling path is opened resulting in a step-wise tunneling

current increase. Each subsequent step corresponds to the next available energy level. These steps are also observed as peaks in the conductance spectra. Each peak corresponds to the subsequent energy level.

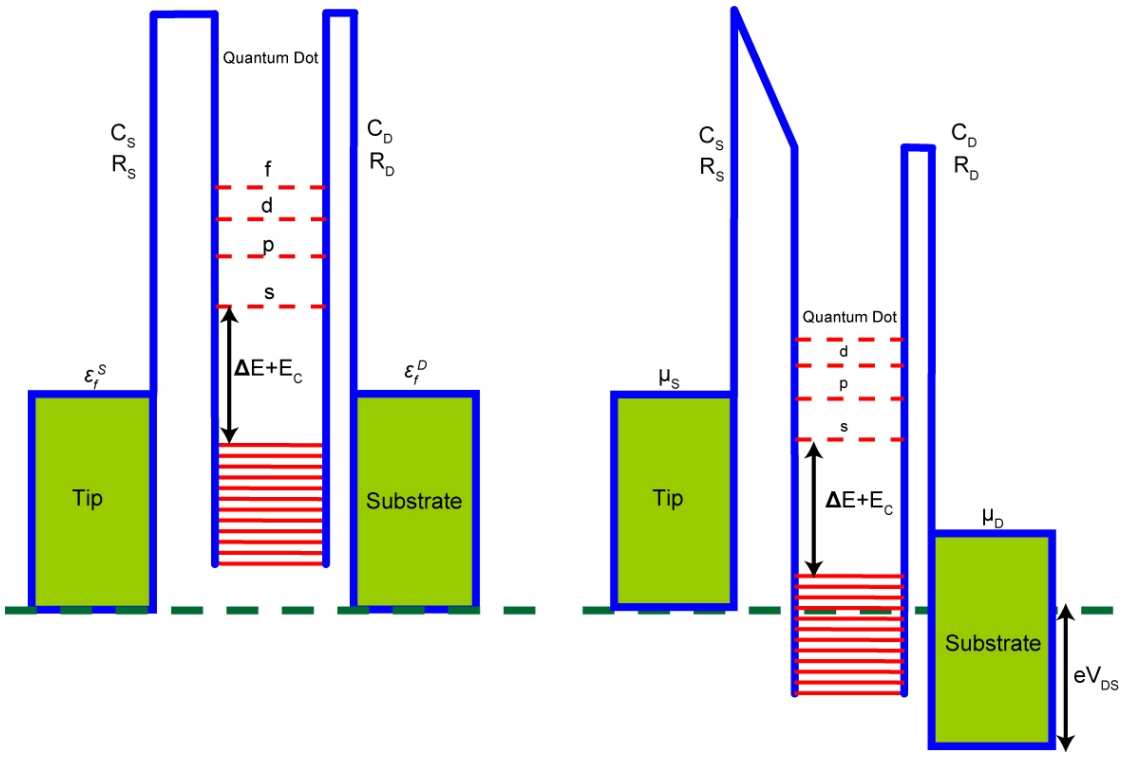


Figure 3.4: Energy diagram for scanning tunneling spectroscopy. A quantum dot placed between metal electrodes separated by thin dielectric tunneling barriers.

From the tunneling spectra and differential conductance spectra, the energy level spacing can be directly deciphered as described in Chapter 2. Figure 3.5(a) is the current-voltage and differential conductance spectra obtained at 4K for Cadmium Selenide (CdSe) quantum dot 3.9 nm in diameter in the shell-tunneling regime [3.19] and figure 3.5(b) shows the STS spectra for an individual Indium Arsenide (InAs) quantum dot 3.2 nm in diameter at 4K in the shell-filling regime [3.20]. As the energy level spacings are much larger than room temperature energy (~26 meV), these tunneling effects can be easily observed even at room

temperature, however, the STS measurements were done at temperatures of 4K or lower to reduce thermal drift of the STM tip from above the quantum dot as the feedback is turned off.

The main disadvantage of the STS technique is the peak broadening effect of the conductance spectra which has been observed in spectroscopic measurements ranging from single molecules to quantum dots [3.21, 3.22]. Figure 3.6 [3.22] shows one such example of the peak broadening effect on the STS spectra obtained on a 6.1nm CdSe quantum dot. This peak broadening effect is attributed to the electron-phonon coupling effects. Other causes such as temperature, (heat dissipation leading to increased quantum dot temperature) non-resonant tunneling, dielectric response of the capping organic layer etc were found not to affect the peak broadening significantly [3.22]. This peak broadening, which has been attributed to electron-phonon coupling, interferes with the spectroscopic measurements. The electron-phonon coupling leads to broadening of the conductance peaks many times over the thermal energy even up to few hundred millivolts [3.21-3.23]. The thermal energy at 4K is in the order of millivolts, but the observed peak broadening is in the order of few tens of millivolts and varies with the size of the quantum dots. This peak broadening effect exists in all temperature ranges from cryogenic temperatures (4K) to room temperature. These coupling effects are however undesirable for simple spectroscopic measurements as any fine energy level separations may not be distinguishable due to peak broadening.

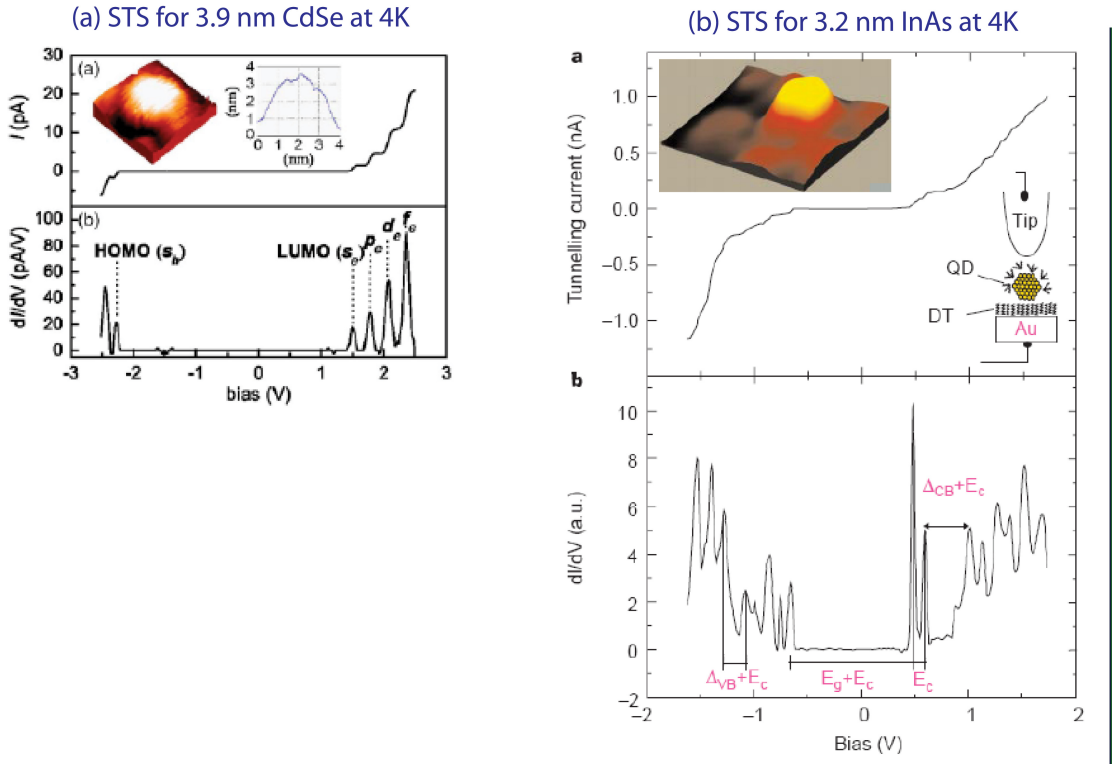


Figure 3.5: Scanning tunneling spectroscopy for different quantum dots. (a) STS shell-tunneling spectra for a 3.9nm CdSe quantum dot [3.21]. (b) STS shell-filling spectra for 3.2nm InAs quantum dot acquired at 4K [3.22].

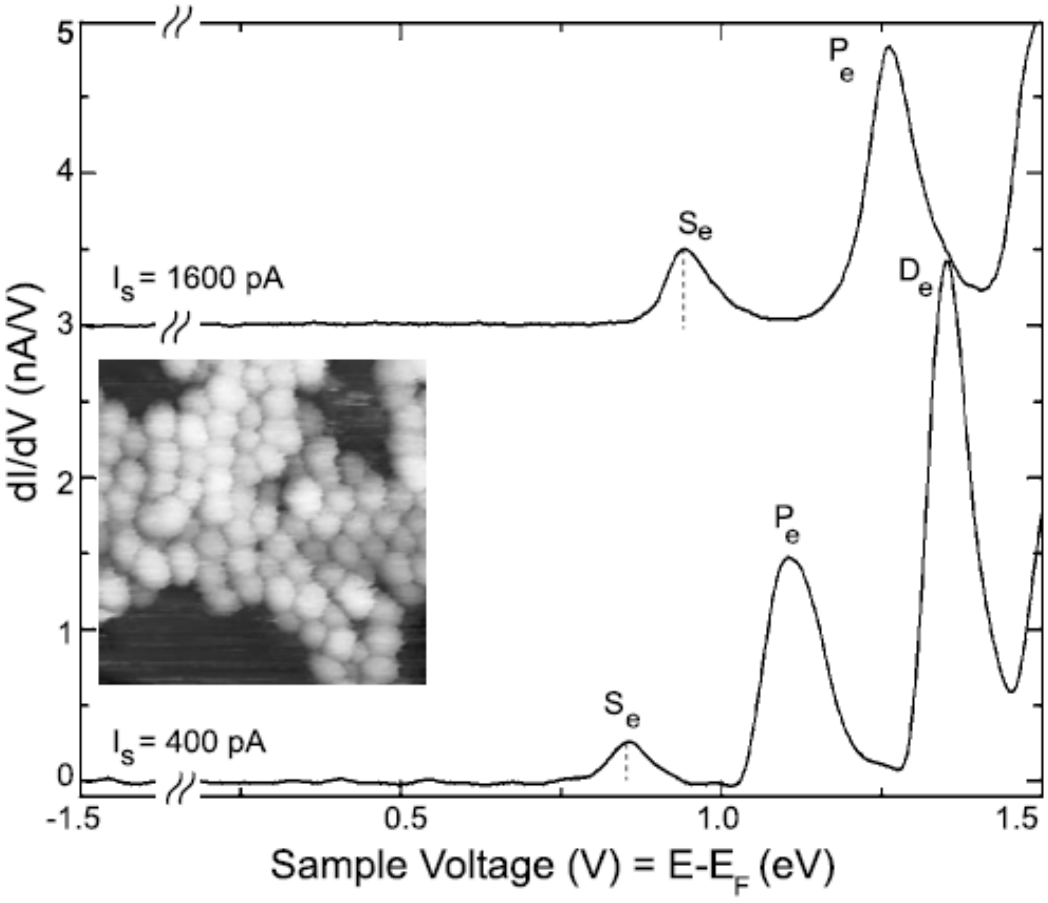


Figure 3.6: Peak broadening effect due to electron-phonon coupling effect as observed in Scanning Tunneling Spectroscopy [3.22] for a CdSe nanoparticle of core sizes 6.1 nm. The peaks shown are for the LUMO peaks at different current set points.

The focus of this work is the combine the advantages of both these methods, namely, (a) accomplish spectroscopy on individual quantum dots, and (b) to study the energy level structure of individual quantum dots without any interferences. The next section will outline how this will be achieved.

3.3 Vertical electrode tunneling spectroscopy

The most critical criterion in performing single-electron spectroscopic measurements on quantum dots using the DBTJ approach is to define the source to drain electrode separation. Other approaches to defining source-drain gap effectively have successfully demonstrated single-electron transport using fabrication techniques such as electromigration [3.24], a combination of e-beam lithography and shadow mask evaporation [3.25]. However, using these techniques, a large number of measurement units with the same exact source-drain gap cannot be fabricated simultaneously.

The focus of this work is on utilizing CMOS-compatible processing and vertically separating electrodes to achieving this requirement. In this new spectroscopic electrode architecture, the source and the drain electrodes are separated by sandwiching a thin dielectric spacer. The thickness of the spacer determines the separation between the electrodes and thus can be controlled using thin film deposition techniques such as PECVD, ALD which are CMOS-compatible. Using these deposition techniques, this thin film can be deposited uniformly over a large area. As seen from figure 3.7, quantum dot placed on the periphery between the source and the drain electrodes forms a double barrier tunnel junction, allowing for resonant tunneling spectroscopy measurements as explained in Chapter 2. When the fermi level of the metal electrode aligns with one of the available energy levels of the quantum dot, a tunneling channel opens resulting in a stepwise increase in the measured current and corresponding peaks in the differential conductance dI/dV_{DS}. Spectroscopy is performed by sweeping the applied bias and measuring the tunneling conductance.

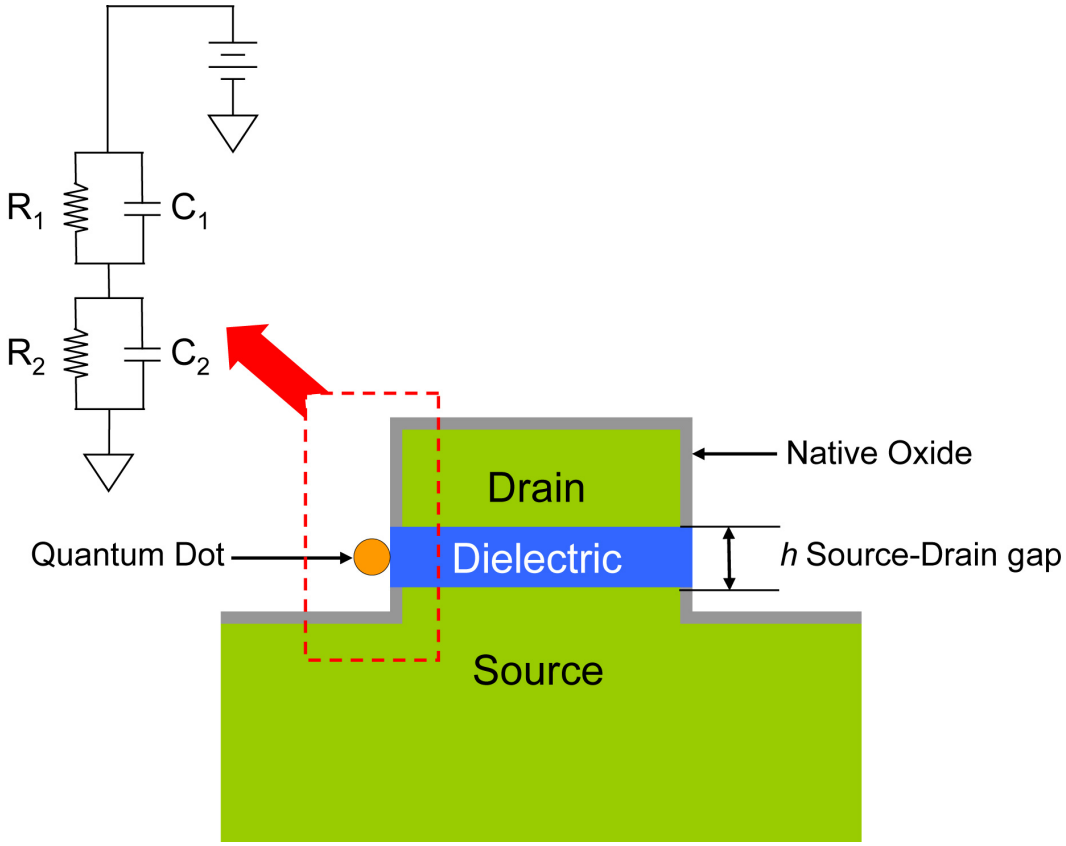


Figure 3.7: Vertical electrode configuration for single-electron tunneling spectroscopy of quantum structures where the source and drain electrodes are separated by a thin dielectric spacer of thickness '*h*'. Inset shows schematically the equivalent circuit diagram showing the double barrier tunnel junction which forms the basis for tunneling spectroscopic measurements.

Figure 3.7 schematically shows the vertical electrode architecture, where the source and drain electrodes are separated by a thin dielectric layer defined by height *'h'*. This allows for defining very precisely the source/drain gap using modern deposition techniques that can control thicknesses to sub-nanometer scale precision. Vertically sandwiching the dielectric between the source and drain electrodes ensures an equal separation throughout the periphery of the measurement unit. Furthermore, these films can be deposited over entire wafers such that numerous units can be fabricated concurrently. Due to the vertical stacking of electrodes, the lateral dimensions and the shape of the electrodes are inconsequential as only the exposed

sidewall with the quantum dots attached are considered as the active region taking part in the tunneling events.

The other advantage of this structure lies in the materials chosen for the electrode and tunneling barriers. Chromium was chosen as the metal electrode. Chromium forms a thin native oxide when exposed to air ~2nm thick. The tunneling barrier height for Cr/Cr_2O_3 is very low (~0.06 eV) [3.27]. A low tunneling barrier allows for a larger separation between the electrode and the quantum dot while still having reasonable tunneling currents. By locating the quantum dot further from the electrode, the junction capacitance is reduced. A smaller junction capacitance is favorable for room temperature measurements. Hence, the choice of Cr/Cr_2O_3 was one of the best options for the electrode/tunneling barrier materials, instead of higher barrier height materials such as Al/Al_2O_3 etc.

The inset on the top left of figure 3.7 shows an equivalent circuit for the DBTJ single-electron tunneling spectroscopy measurement unit. This vertical electrode structure has already been successfully incorporated into single-electron transistors (SET) operable at room-temperatures by Ray et al [3.26]. Details of the fabrication and spectroscopic measurements will be detailed in later chapters.

CHAPTER 4

FABRICATION OF RESONANT TUNNELING SPECTROSCOPIC UNITS

4.1 Introduction

The fabrication process of the solid-state spectroscopic measurement units will be described in detail in this chapter starting from a 4 inch silicon wafer to a finished measurement unit ready for tunneling spectroscopic measurements. Silicon wafer is used as substrate for making the spectroscopic measurement units which are fabricated using a combination of optical lithography, e-beam evaporation, plasma enhanced chemical vapor deposition (PECVD), RF magnetron sputtering, and reactive ion etching (RIE), self-assembled monolayers, colloidal nanoparticles. The equipments used to fabricate these devices are described in detail in the University of Texas at Arlington's Nanofabrication Facility home page [4.1].

4.2 Thermal oxidation

Silicon (100) wafer was used as substrate for all measurement unit fabrication. A 1.5 μm thick silicon dioxide film was grown using wet thermal oxidation. 4" silicon wafers were first cleaned in an ultrasonic bath containing acetone to remove any organic impurities. They were then immersed in a 10:1 Hydrofluoric acid bath for 2 minutes to remove the native oxide layer on them and then rinsed with DI water and blown dry with nitrogen. This step also terminated the surface with a layer of hydrogen preventing the formation of any native oxide layer. These cleaned wafers were then introduced slowly into the thermal oxidation furnace where the center zone maintained at 1000^{O}C. The wafers were introduced into the chamber at the rate of 1

inch/minute, to reduce the risk of any thermal shock. During wafer introduction into the furnace, the furnace tube is purged with nitrogen gas at 3 liters/minute. Once the wafer is placed in the middle zone of the furnace, 10 minutes of hold time is allowed for thermal equilibrium. Water vapor is then flowed into the furnace using a bubbler system with nitrogen being the carrier gas. The bubbler containing ultra pure DI water (18.2MΩ.cm) is maintained at 90^{O}C. Process time for 1.5 μm thickness oxide films was approximately 3 hours. Once the process time is completed, the nitrogen flow through the bubbler is cut-off and pure nitrogen is flowed through the furnace tube. The heater elements to the furnace are also turned off at this time. Once the furnace cools to below 200^{O}C, the wafer is slowly extracted from the furnace at the rate of 5 inches/minute. After removal of the wafers, the thickness of the oxide film is checked with the Gaertner ellipsometer and Ocean optics NC-UV-VIS reflectometer.

4.3 Definition of source electrodes

The next step in the fabrication process is the deposition of the (bottom) source electrode. The silicon wafer with the thermally grown oxide layer was first cleaned with acetone, blown dry with nitrogen and then cleaned in the UV-Ozone cleaner (Novascan Inc.) for 30 min to remove any contaminants from the surface. The negative photoresist NR9-1000PY (Futurrex Inc.) was then spun coat on the wafer at 2000rpm for 30 seconds giving a film thickness of 1.3 μm. Pre-exposure bake was done at 150^{O}C for 90 seconds. The 4” wafer was then cleaved into four equal sized quadrants. The quadrant was then placed on the sample holder in the OAI-Backside aligner for UV exposure. 365 nm primary wavelength UV light generated by a mercury vapor lamp was used for exposure. The samples were exposed through the photo-mask for 17 seconds. The post exposure bake was done immediately after exposure at 100^{O}C for 60 seconds. After baking the samples were developed in the resist developer (RD6, Futurrex Inc.) by immersing them in the developer solution for 16 seconds. After development, the samples

were rinsed with copious DI water till the pH of the rinsed water was 7.0. The quadrants were then placed inside the e-beam evaporator (AJA Inc.) chamber. After reaching vacuum levels of $4*10^{-8}$ Torr, the chromium metal was evaporated on to the patterned silicon wafer at a rate of 4 Å/s for a total thickness of 250 nm, with an acceleration voltage of 9 kV. After completion of evaporation to the desired thickness, the samples were unloaded from the chamber and immersed into an acetone bath in the ultrasonic agitator to facilitate the lift-off process. After 10 minutes, the acetone was replaced with fresh acetone. Once completed with the lift-off process, the samples were again rinsed with acetone and DI water and blown dry with nitrogen. To remove any remnants of the photoresist, the samples were then ashed inside the UV-Ozone cleaner for 30 minutes. Figures 4.1 (a) to 4.1(f) schematically illustrate the entire process flow for this step. Figure 4.1 (g) shows a 3-dimensional schematic of the completed source electrode.

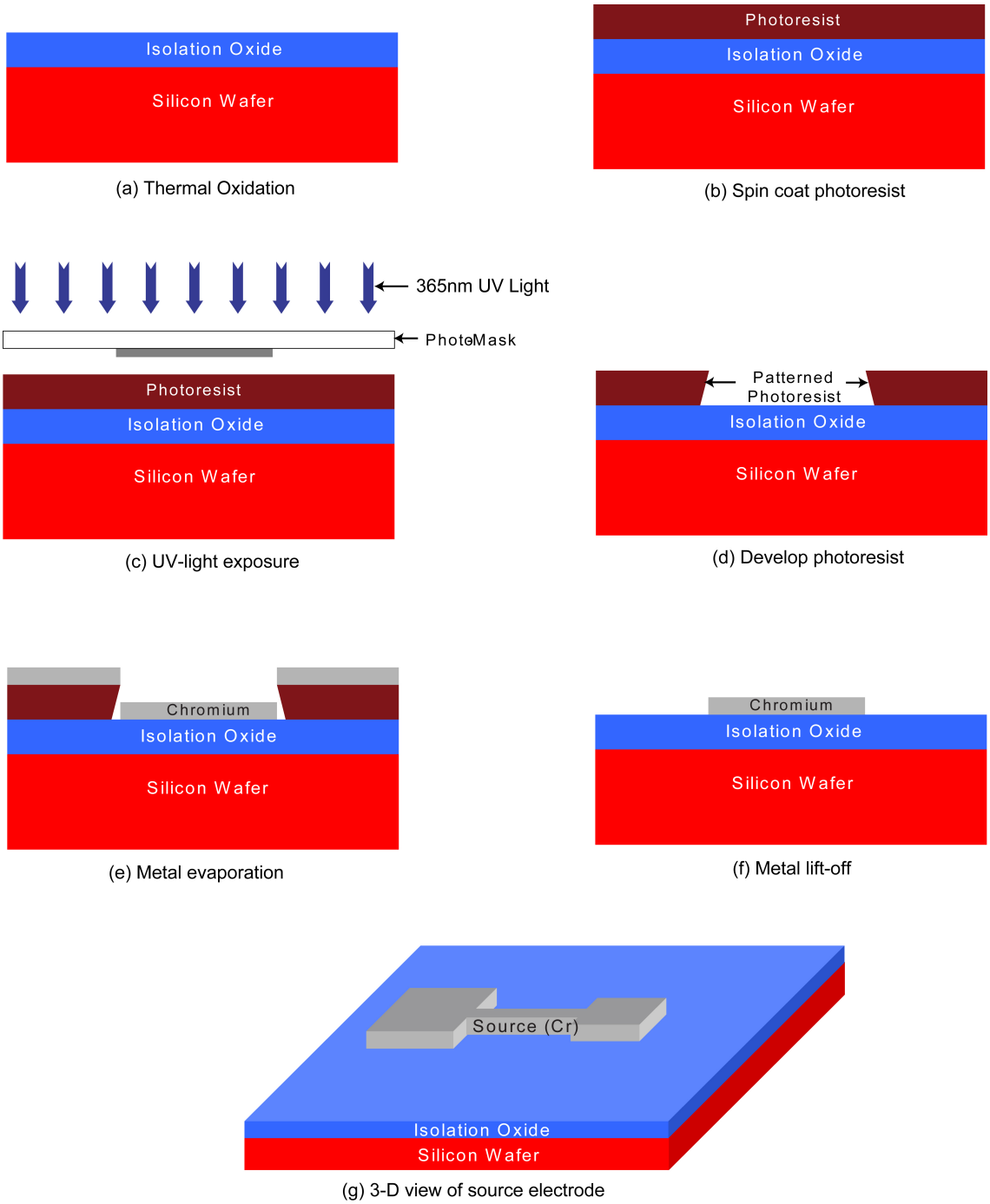


Figure 4.1: Definition of bottom source electrode using photolithography, metal evaporation and lift-off technique.

4.4 Development and deposition of PECVD silicon dioxide film

In the vertical electrode configuration, the source and the drain electrodes are separated by a thin dielectric film. This dielectric film (silicon dioxide) is deposited using plasma enhanced chemical vapor deposition (PECVD). This film is the most critical factor during experiments as the quality of this film affects the spectroscopic measurements. For good spectroscopic measurements, very low leakage between the source and the drain electrodes and a high breakdown voltage for this thin film is required. Surface roughness also plays an important role. By controlling the deposition parameters, a good quality film can be deposited [4.2, 4.3].

Chemical vapor deposition is a surface mediated growth technique where the precursors are decomposed into their elements and the reactive gases combine at the surface of the substrate maintained at high temperature. Decomposition of the process gases occurs due to the high temperatures (~1000^0C) in the process chamber. The process for silicon dioxide deposition which requires decomposition of its precursor gases (silane SiH_4 and nitrous oxide N_2O) can be represented as follows:

$$SiH_4 \rightarrow Si + 2H_2$$
$$2N_2O \rightarrow 2N_2 + O_2$$
$$Si + O_2 \rightarrow SiO_2$$

The various factors affecting the quality of this silicon dioxide film are listed below:

a) Dilution of Silane precursor

b) Pressure

c) Temperature

d) Radio frequency power

e) Substrate material

For film deposition on metals though, such high temperatures are not desirable. Radio frequency power helps to decompose the process gases in the plasma phase due to acceleration of charges between the charged plates. The reactive ion species then meet at the hot surface, react and form the film. RF power gives sufficient energy for decomposition of the gases as well as prevents any gas phase reactions. Figure 4.2(a) schematically shows the operation of a PECVD chamber. Figure 4.2(b) is the actual photographic image showing the top and bottom electrodes, wafer placed on the bottom electrode during actual deposition process with plasma in between the electrodes.

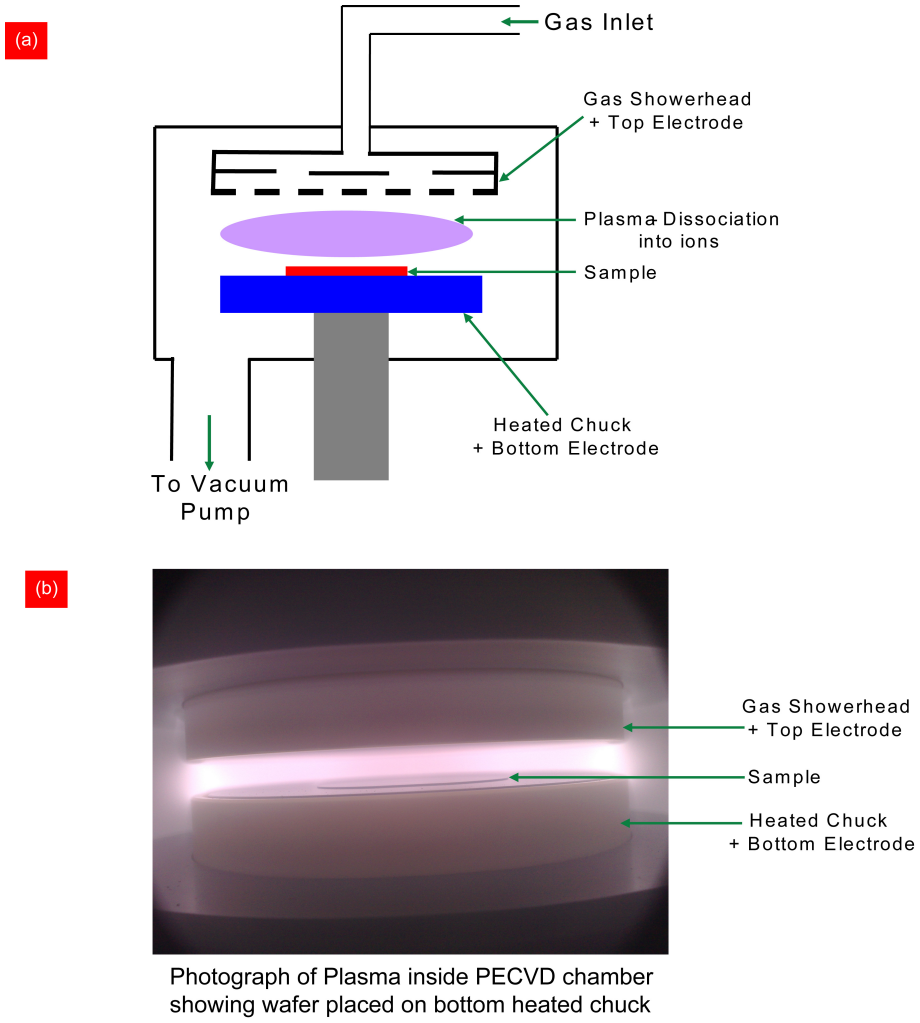


Figure 4.2: (a) Illustration of the PECVD deposition process. (b) Photograph of PECVD deposition of SiO_2 in the Trion Orion PECVD system showing top and bottom electrodes, sample placed on the bottom electrode/heated chuck.

An experiment was designed to find the significance of each of these factors. To characterize the films, the following tests were done: deposition rate measurement, atomic force microscope (AFM) scanning for roughness measurements, wet etch rates compared with dry thermal oxide etch rate etched with 10:1 HF solution, refractive index measurement using ellipsometer, breakdown voltage measurement using parameter analyzer and scanning electron micrographs to check for presence of pin holes.

Effect of silane dilution: The process time was fixed at 300 seconds, pressure at 0.9 Torr, and all experiments were conducted on a clean silicon substrate.

Table 4.1: Study effect of dilution of silane on the properties of the deposited film.

Sx #	SiH_4 (sccm)	N_2O (sccm)	N_2 (sccm)	Temp (^{0}C)	R.F.Power (W)	Thickness (Å)	Refractive Index
1	5	100	250	300	100	1275	n/a
2	4	20	250	300	100	1075	n/a
3	4	75	250	300	25	1200	1.44
4	4	250	250	300	50	1224	1.446
5	4	250	250	300	100	1200	1.456
6	4	250	250	300	400	968	1.446

For samples 1 through 4, due to high silane/total flow ratios and low RF power, the films were found to be grainy as seen in sample # 3 in figure 4.3. The presence of grains arises from gas phase reactions where the reactants already react in the gas phase and are then deposited on the substrate as tiny particles which results in grains. The film quality for these films is not good as the silane does not completely dissociate and there is still a lot of hydrogen incorporated into the film. Films formed in samples 5 and 6 showed a very smooth surface with roughness less than 1 nm for film thickness close to 100 nm thick. This implied that a low silane to total flow ratio was necessary to obtain good quality silicon dioxide films. Higher power also yielded a smoother surface. The etch rates for sample 5 and 6 were about 4 times (~870 Å/min) faster than thermal oxide (~220 Å/min). The closer the etch rates are to thermal oxide etch rates, the better the film quality representing the compactness/density of the film.

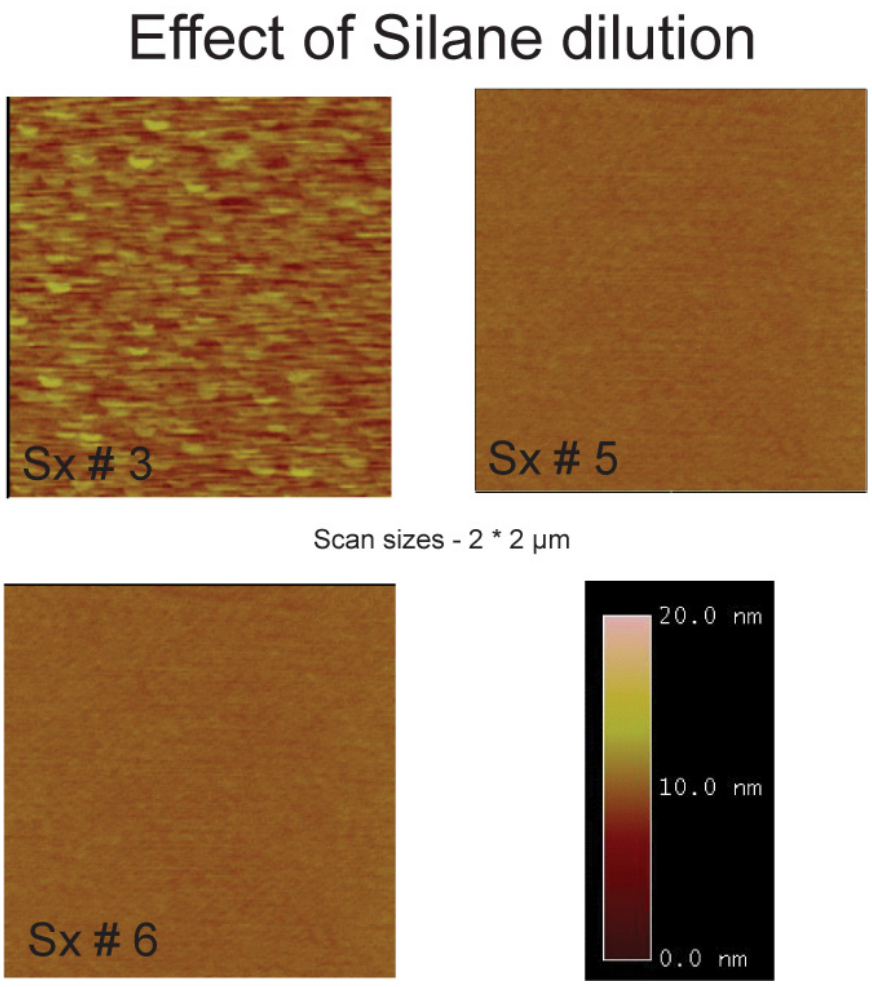


Figure 4.3: Experiment showing low silane to total flow ratio gives better films where sample 5 and 6 show very smooth surface with no grains. Sample 4 shows grains and is rough.

Effect of power and temperature: Process time was again fixed at 300 seconds, silane flow at 4 sccm, N_2O flow at 250 sccm and N_2 flow at 250 sccm.

Table 4.2: Study on the effect of R.F power and Temperature on the deposited film properties.

	Power (W)	Temperature (C)
+	400	350
-	200	250
mid	300	300

Table 4.3: Experimental conditions and observations for the second set of experiments:

	SiH_4 (sccm)	N_2O (sccm)	N_2 (sccm)	Temp (^0C)	R.F.Power (W)	Thickness (Å)	Ref.Index	Etch Time (s)
1	1	250	250	250	200	990	1.455	60
2	1	250	250	250	400	930	1.448	57
3	1	250	250	300	300	920	1.446	62
4	1	250	250	350	200	905	1.445	60
5	1	250	250	350	400	915	1.447	60

From this experiment, it was observed that increasing the temperature and power decreased the deposition rate. This implies that there is more hydrogen in the form of undissociated silane present in the film at lower power and lower temperature. By increasing the power and temperature, complete dissociation of silane can be insured for better quality films. The roughness for these films was below 1nm as the silane to total flow was set to the minimum value possible with this equipment.

Effect of pressure: From the previous set of experiments, time, temperature and flow rate of gases were set to constant. Only pressure and RF power were varied in this experiment.

Table 4.4: Effect of pressure on the properties of the deposited films

	Power (W)	Pressure (Torr)
+	550	4
-	400	0.9
mid	475	2.5

Table 4.5: Experimental conditions and film properties recorded from experiments conducted using table 4.4:

	SiH_4 (sccm)	N_2O (sccm)	N_2 (sccm)	Pressure (Torr)	R.F.Power (W)	Thickness (Å)	Etch Rate (Å/s)
6	1	250	250	0.9	550	450	8
7	1	250	250	4	400	168	6
8	1	250	250	4	550	156	5.57
9	1	250	250	2.5	475	206	5.75

As pressure was increased, the deposition rate dropped. Above a certain threshold pressure, there was no appreciable change in the film properties. Higher pressure gives a shorter mean free path for the ions in the plasma. Shorter mean free path leads to more collisions in the plasma phase. This ensures that the silane is completely dissociated and thus giving lower deposition rate and a slower etch rate (~350Å/min).

These experiments were also repeated for metal substrate (Cr) and the process parameters optimized after measuring the breakdown voltage. Best film qualities with roughness lower than 1 nm for films 20 nm and thicker had breakdown voltage in the order of 6 MV/cm. The main objective for the development of the PECVD silicon dioxide layer was to achieve a recipe for an isolation layer that will insulate the source and drain electrodes.

After further changing the system configuration of the Trion Orion PECVD system by changing the silane MFC flow ranges from 0-25 sccm, the deposition process for SiO_2 was further tuned to obtain the following final recipe with a deposition rate of ~200 Å/minute on Chromium substrate:

(1) SiH_4 : 21 sccm

(2) N_2O : 179 sccm

(3) N_2 : 250 sccm

(4) Pressure: 1.0 Torr

(5) Temperature: $360^{O}C$

(6) R.F Power: 500 W

4.5 Deposition of drain electrode/etching of oxide layer

The vertical electrode structure enables the use of photolithography for electrode definition. The drain electrode was deposited using photolithography, e-beam evaporation of chromium metal and lift-off process. After deposition of the PECVD silicon dioxide film, the samples were cleaned again in the UV-Ozone cleaner for 30 minutes. After cleaning, NR9-1000PY was spun coat at 2000 rpm for 30 seconds. The pre-exposure bake was done at $150^{O}C$ for 60 seconds and the sample subsequently placed on the OAI aligner substrate holder. As this was the second layer on our mask, using the alignment marks on the photomask as well as the sample surface, the features on the photomask were aligned with the corresponding features on the substrate. Once aligned, the sample was brought into contact with the photomask and subsequently exposed to the 365 nm UV light for 17 seconds. Post exposure bake was done at $100^{O}C$ for 60 seconds followed by developing the exposed photoresist in RD6 developer solution for 16 seconds. The samples were once again rinsed with copious DI water and blown dry with nitrogen. These patterned samples were then loaded into the AJA e-beam evaporator

and chromium metal of 250 nm thickness was evaporated on the sample. After unloading the samples from the evaporation chamber, final metal lift-off was completed by sonicating the samples in an acetone bath for 15 minutes. This was repeated once again using clean acetone and finally the samples were rinsed with DI water and blown dry with nitrogen. The drain and source electrode are now separated by the thickness of the deposited PECVD oxide layer.

The samples after cleaning with the UV-Ozone cleaner for 30 minutes, were placed inside the RIE chamber (Trion DRIE). Using the drain electrode as the hard mask, the PECVD oxide layer was vertically etched using fluorine chemistry. The process parameters for this vertical etching process are as follows:

(1) CF_4 flow rate – 50 sccm

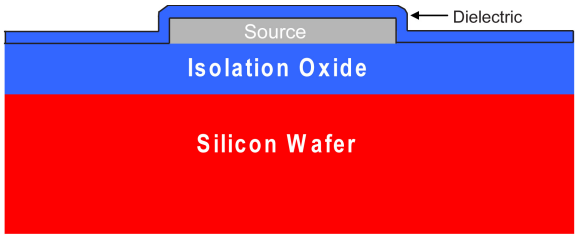
(2) Process pressure – 50 mTorr

(3) Top electrode power – 3000 W

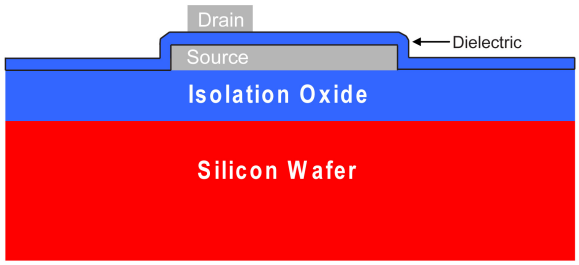
(4) Bottom electrode power – 100 W

(5) Process time – 150 seconds

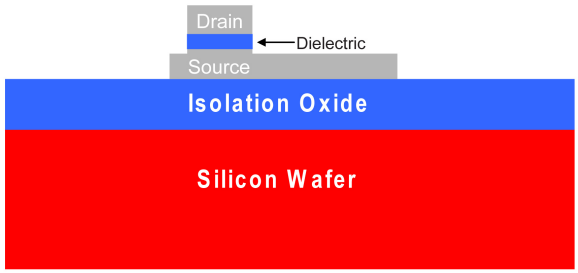
Over etching of the PECVD oxide layer is ensured by a longer etching time. This forms a small step of approximately 15-25 nm in the bottom chromium source layer as seen in the schematic shown in figure 4.4(c). After completing the etching step, the source and the drain electrodes are separated by a sub-nanometer scale gap controlled by the thickness of the PECVD oxide layer. This gap is maintained along the periphery of all the drain electrodes.



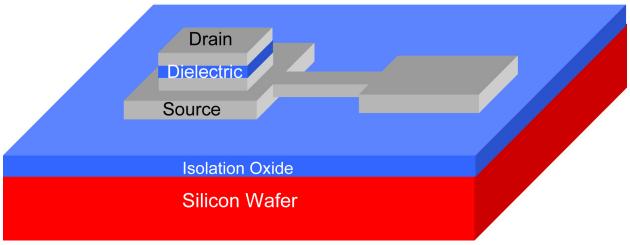
(a) PECVD Silicon dioxide deposition



(b) Drain electrode lift-off deposition



(c) Vertical RIE etching



(d) 3-D schematic

Figure 4.4: Fabrication of vertical electrode structure. (a) Deposition of PECVD SiO2 film of desired thickness. (b) Pattered deposition of drain electrode. (c) RIE etching of the deposited PECVD SiO2 film to expose the sidewall and form the vertically self-aligned source-dielectric-drain structure. (d) 3-D View of the vertical electrode structure.

4.6 Attachment of quantum dots

Cadmium Selenide (CdSe) quantum dots ~ 7nm in diameter (NN Labs Inc.) were chosen as a model system to demonstrate this new spectroscopic technique. These quantum dots were available in colloidal form with a surface ligand coating preventing them from agglomerating. Initially, these surface ligands (TriOctylPhosphine Oxide - TOPO) provided a net negative charge on these quantum dots. Using positively charged surface modified using self-assembled monolayers (SAMs), these quantum dots were attracted and attached onto the surface of the substrate. By November 2009, the manufacturer (NN-labs Inc.) switched the surface ligand to Octadecyl Amine (ODA) which has a net positive charge on the nanoparticle. SAMs terminating with thiol group (-SH group) were used to immobilize the nanoparticles on the exposed sidewalls.

The samples once removed from the etching chamber were once again rinsed with acetone and blown dry and subsequently cleaned in the UV-Ozone chamber for 30 minutes. For the TOPO stabilized nanoparticles, SAMs of 3-AminopropylTriethoxysilane (APTES – Sigma Aldrich) was formed on the chromium and silicon dioxide surface by immersing the substrate in a 1mM solution of the APTES in chloroform for 30 minutes. This was followed by rinsing in chloroform (Sigma Aldrich) and 2-Propanol (J T Baker Inc) solutions and blown dry with nitrogen. The samples were immediately immersed in the toluene solution containing the quantum dot colloid. The diluted quantum dot solution was prepared by taking 1ml of the concentrated quantum dot solution (as is from manufacturer) and dissolving it in 25 ml of pure toluene (Sigma Aldrich). The APTES functionalized substrates were immersed in this diluted colloidal quantum dot solution for 16-24 hours depending on the thickness of the oxide layer. Once the immersion was completed, the samples were rinsed with pure toluene and methanol (J T Baker Inc) and blown dry with nitrogen. By this attachment process, the quantum dots are randomly attached all over the substrate surface including the exposed sidewall of the

source/oxide/drain layers. A schematic after the quantum dot attachment is shown in figure 4.5. Once the quantum dots are attached, the organic monolayers on the substrate and the surface ligands on the quantum dots are removed by ashing the sample in the UV-Ozone cleaner for 30 minutes.

For the ODA stabilized nanoparticles, SAMs of (3-Mercaptopropyl)trimethoxysilane (MPTMS – Sigma Aldrich) was formed on the chromium native oxide and SiO_2 surfaces. The cleaned samples were immersed into a solution of 5mM MPTMS in 2-Propanol (JT Baker Inc) along with 3 drops of ultra pure DI water at $40^{O}C$ for 1 hour. After immersion, the samples were thoroughly rinsed with 2-Propanol and dried with a stream of nitrogen. The SAMs treated samples were then immersed into the diluted nanoparticle colloid in Toluene for 20 hours for good attachment of nanoparticles.

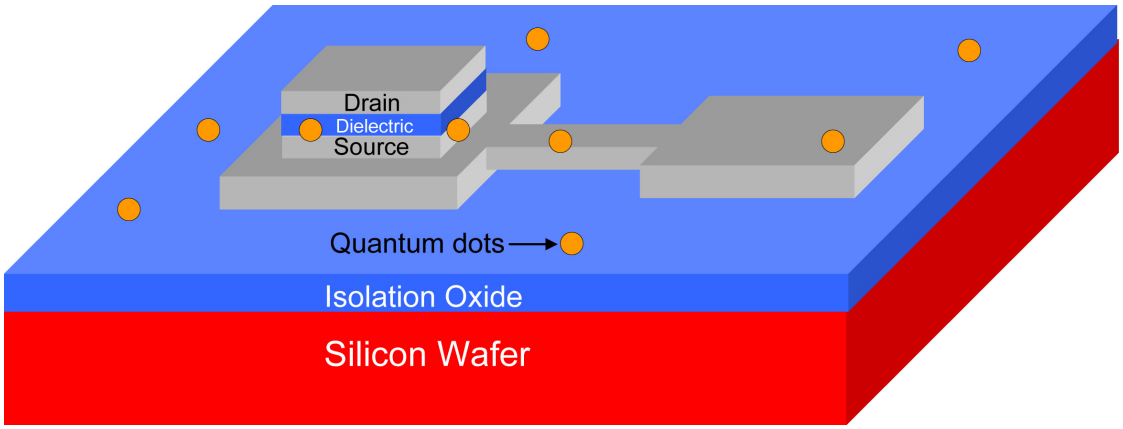


Figure 4.5: Quantum dots attached on the sidewall structure using self-assembled monolayers.

4.7 Final passivation of measurement units/ etching of via holes

The measurements units, now complete with the source/quantum dot/drain double barrier tunnel junction, were passivated using a combination of RF magnetron sputtered and e-beam

evaporated silicon dioxide. Initial passivation was done using RF magnetron sputtering once the chamber pressure was lower than $2*10^{-5}$ Torr. (Home built sputter system) using SiO_2 target at the following conditions:

(1) RF Power: 80 W

(2) Pressure: 10 mTorr

(3) Argon flow rate: 37.5 sccm

(4) Deposition rate: 30 Å/minute

A thickness of ~250 nm was reached after sputtering for 90 minutes. The sputter process was done in two 45 minute periods with 1 hour interval in between so as not to heat up the substrate too much. Once the sputtered SiO_2 was completed, the samples were again loaded into the e-beam evaporator (AJA Inc.). Approximately a 0.6 µm thick silicon dioxide was evaporated onto the substrate after a base vacuum of $2*10^{-8}$ Torr was reached in the evaporation chamber at a rate of 4-5 Å/second. Figure 4.6 schematically shows the final passivated samples.

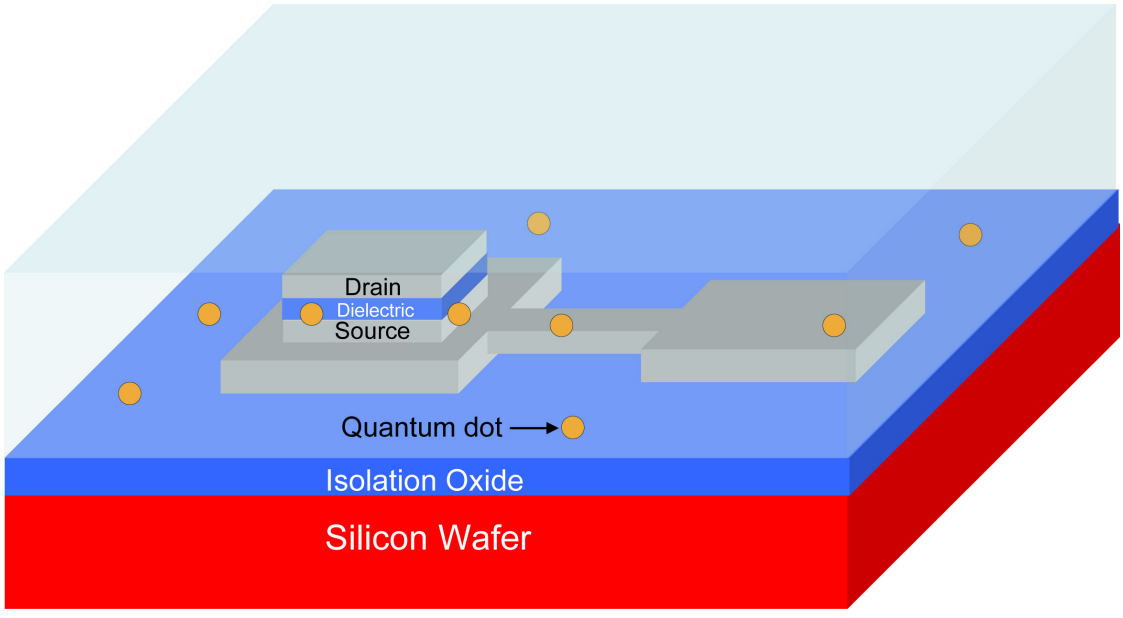


Figure 4.6: Final sample passivation using sputtered and e-beam evaporated SiO_2.

Via holes were etched in the passivation oxide layer to expose the source and drain electrode contact holes. This was done by using photoresist as mask and vertical etching using fluorine chemistry in the RIE chamber. The passivated samples were spun coated with the NR9-1000PY resist at 2000 rpm for 30 seconds and pre-exposure bake completed at 150^{O}C for 60 seconds. These samples were then loaded onto the substrate holder on the OAI aligner. The alignment of the photomask and the substrate was completed using the optical microscope and the x, y and tilt movements to the substrate using the alignment marks on the photomask and substrate as guides. After aligning the substrate with the photomask, it was exposed to the UV light for 17 seconds. Post exposure bake was done at 100^{O}C for 60 seconds followed immediately by developing the photoresist for 16 seconds in RD6 developer solution. The substrate was then rinsed with copious DI water till the pH of the wash was 7. The substrate was then blown dry with nitrogen. Pre-etching bake of the photoresist was done at 125^{O}C for 2 minutes.

The photoresist was used as the mask for the etching of the via holes. Fluorine chemistry was utilized to etch the SiO_2 passivation layer. The etching process parameters are listed below:

(1) CF4 flow rate – 50 sccm

(2) Process pressure – 25 mTorr

(3) Top electrode power – 3000 W

(4) Bottom electrode power – 50 W

(5) Process time – 300 seconds

During this etching process, photoresist was also consumed along with the etched SiO2 layer. Hence, this alignment/ lithography/ etch steps had to be repeated to etch via holes till the bottom source and drain electrodes were completely exposed. After completing the etching steps, the samples were cleaned by first sonicating in a bath of acetone for 30 minutes and then

ashing them to remove any residual contaminants in the UV-Ozone cleaner for another 60 minutes.

4.8 Final bond pad deposition for spectroscopic measurement units

The fourth layer in the photomask is used to define the final bond pads/contacts with the underlying source and drain electrodes. A layer of NR9-1000PY negative photoresist is again spun coated on the substrates at 2000 rpm for 30 seconds. Pre-exposure bake is done at 150^{O}C for 60 seconds. Using the alignment marks on the photomask and the substrate, the substrate is aligned to the corresponding feature on the photomask using the OAI mask aligner. Once aligned, the substrate is brought into contact with the photomask and exposed to the UV light for 17 seconds. Post exposure bake is done at 100^{O}C for 60 seconds followed by developing the exposed photoresist in the resist developer RD6 for 16 seconds. The samples are then rinsed with copious DI water till the pH of the wash is 7 and then blown dry with nitrogen. The wafers are then loaded in the e-beam evaporator (CHA Inc.) and the chamber is evacuated till the pressure reaches 1×10^{-7} Torr. 400 Å of chrome and 4500 Å of gold are evaporated at the rate of 3-4 Å/sec. Lift-off of is done by first immersing the wafers in an acetone bath for 1 hour followed by ultrasonic agitation in an clean acetone bath for 15 minutes. The samples are then rinsed with DI water and blown dry and subsequently cleaned in the UV-Ozone cleaner for 30 minutes. The final sample structure is shown schematically in figure 4.7.

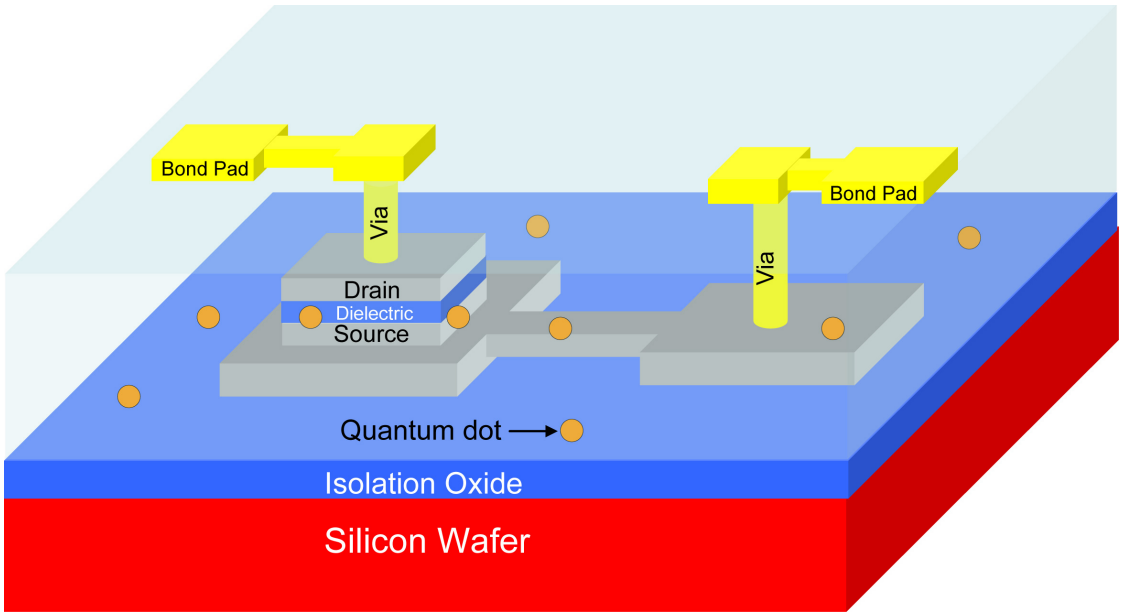


Figure 4.7: Final sample structure after bond pad deposition and lift-off.

4.9 Mounting single dies on chip carrier

For electrical characterization in the ST-500 (Janis) probe station, individual dies had to be mounted on chip carriers to allow easy mounting/dismounting of samples in the chamber. After the final bond pad fabrication step, individual dies (~1cm * 1cm in size) were diced from the wafer pieces by scribing on the wafer using a diamond tip scriber pen. By pushing with Teflon tweezers on either side of the scribed mark, individual dies were diced. Once diced, these dies were thoroughly rinsed with acetone and dried with a stream of nitrogen. The diced pieces were cleaned once again in the UV-ozone chamber for 30 minutes to ensure clean surfaces. Ceramic chip carriers (CCF06404; Kyocera) were used for mounting the dies containing the spectroscopic measurement units. The ceramic chip carriers offered excellent thermal conductivity along with electrical isolation. A drop of conducting silver paint (SPI supplies) was placed on the chip carrier and the diced die placed on top of it. By gently pressing on the top of the die using Teflon tweezers taking care not to press on any spectroscopic unit,

the die was securely positioned onto the chip carrier. The silver paint was allowed to dry for 2-3 hours to securely hold the dies. Once dry, the chip carrier along with the spectroscopic measurement units, were ready for electrical characterization.

CHAPTER 5

RESONANT TUNNELING SPECTROSCOPY OF INDIVIDUAL QUANTUM DOTS

5.1 Introduction

The focus of this chapter is extensively on the experimental setup and spectroscopic measurements using simple current-voltage and direct differential conductance measurements. Room temperature measurements were conducted either using the Agilent 4155C semiconductor parameter analyzer or the Agilent 4157B semiconductor parameter analyzer systems. Direct differential conductance measurements were conducted using a combination of Agilent 4157B semiconductor parameter analyzer, Stanford Research 830 dual phase lock-in amplifier (SR-830), Stanford Research 570 Current preamplifier (SR-570), Stanford Research SIM 980 Summing amplifier (SIM-980), and Stanford Research SIM 983 Scaling amplifier (SIM-983). The Agilent 4157B provided the direct current (dc) source for the measurements while the internal sine generator from the SR-830 was utilized for providing the sinusoidal (ac) input. Low temperature measurements were conducted in the Janis ST-500 probe station with liquid nitrogen as the coolant, Lake Shore model 331 temperature controller and either the I-V setup or the direct differential conductance measurement setup.

Kelvin connections (4-wire) were employed to conduct the spectroscopic measurements as shown in Figure 5.1 (a). The Kelvin connection practically eliminates any residual resistances from test leads and contacts. In this connection configuration, voltage is forced through the spectroscopic unit using the Force leads and the voltage drop across the electrodes measured through the Sense leads. To cancel the effects of the residual resistance, the test leads are connected as close to the DUT as possible.

For current-voltage (I-V) measurements done using either the Agilent 4155C or 4157B, sweep measurement mode, as shown by schematic in Figure 5.1 (b), was used. Current through the spectroscopic unit was measured as a function of varying source-drain voltage bias. Table 5.1 shows the various settings/parameters used for either of the parameter analyzer system tests.

Table 5.1: Settings for I-V measurements using either Agilent 4155C or 4157B:

Parameters	Agilent 4155C	Agilent 4157B
Initial hold time (s)	30	600
Delay time (s)	10	30
Step Delay time (s)	5	5
Integration time	High	1023

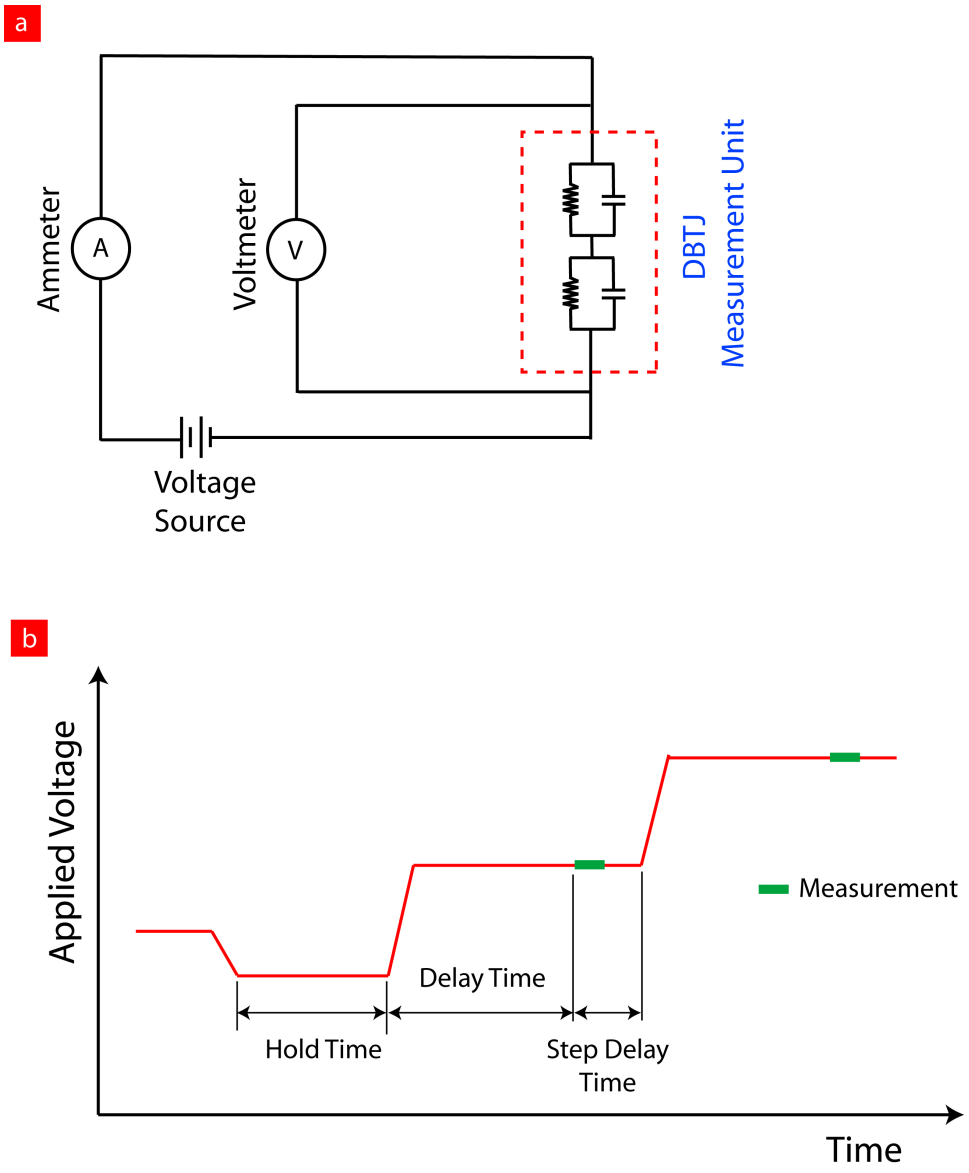


Figure 5.1: (a) Kelvin connection measurement setup. (b) Sweep measurement mode used in I-V plots using Agilent 4155C and Agilent 4157B parameter analyzer systems.

5.1.1 Current-Voltage measurements

Figure 5.2 schematically shows the electrical measurement setup for current-voltage measurements conducted using the Agilent 4157B system. Similar connections were used also for the Agilent 4155C measurement setup with a different probe station. The setup for the

Agilent 4155C measurements are explained in full detail by Ray in his thesis [5.1]. For optimum measurements, the parameter analyzers were tuned on for at least 30 minutes for warm up time. The SMU (source measure units) on the parameter analyzer are connected to the probe tips only using low noise triaxial cables. The outer shields of the cables are connected to the probe station to act as noise shield. The chuck/sample stage on the ST-500 probe station and the shield of the ST-500 probe station itself were all connected to the ground on the parameter analyzer. To facilitate sample mounting and dismounting, the diced dies were mounted on the chip carrier as explained in section 4.6.

Measurements were done in the Janis ST-500 variable temperature probe station. The chamber was vented with extra dry nitrogen. During sample loading or unloading the user always wore a hair net and a face mask so as not to contaminate the interior of the probe station. First, the optical microscope boom was moved such that the top of the probe station was easily accessible. The top port was opened by unscrewing the four restraining screws. While doing so care was taken so as not to open too quickly so the pressure built up during venting was slowly released. The top cover of the radiation shield was then removed by unscrewing the four restraining screws. Extreme care was taken so as not to drop the screws or washers inside the chamber. It would be impossible to remove any screws dropped into the chamber in house and the entire probe station system would have to be shipped back to the manufacturer. After loosening up the screws for the sample mount, the chip carrier was placed on the chuck of the probe station. The chip carrier was clipped in place and the clip screws tightened. The clip screws are electrically isolated from the chuck using alumina washers which offer excellent thermal conductivity and electrical isolation. The radiation cover was then positioned on top and the screws tightened. The radiation cover was greased with a low temperature grease to allow good thermal contact. This low temperature grease does not outgas in vacuum environment. Finally, after re-inspecting the o-ring around the top cover of the probe station, it was secured onto place by tightening the four screws.

Once the sample loading was completed, the chamber was purged with extra dry nitrogen for a minimum of 15 minutes. After the purge cycle, the dry mechanical vacuum pump (BOC Edwards, XD-5 dry scroll pump) was turned on. The lowest vacuum level attainable in this configuration with just the mechanical pump was ~ 3 * 10^{-3} Torr. For room temperature operation, the turbo molecular pump was not required. With the vacuum levels ready within a couple of hours, the sample was ready for electrical measurements.

After the Agilent 4157B was warmed up for the initial 30 minutes, the output of the HRSMU (Channel 1) was turned on and forced to 0V output manually by toggling the output ON/OFF button. The low noise triaxial cable (SC-22;Keithley Instruments Inc.) with male triaxial connectors (CS-631; Keithley Instruments Inc.) was first connected to the force lead on the HRSMU with the output still on at 0 V. The sense lead was then connected to the other triaxial cable. The other end of the force triaxial cable was then connected to the corresponding force input at the probe station, and then the sense input was connected to the sense triaxial cable coming from the HRSMU. This ensured that the triaxial cable as well as the probe tip inside the probe station was all held at 0V so as not the cause any electrostatic shock to the spectroscopic measurement unit. The ground terminal at the Agilent 4157B is always forced held at 0 V potential, so the ground terminal was first connected to the low noise triaxial cable. On the other end of the triaxial cable inside the triaxial connector, the force and sense (center conductor and guard wires) were shorted. Ideally, two separate triaxial wires are required for the ground terminal also just as in the HRSMU force and sense and they be connected inside the probe station to reduce noise as much as possible, but with the ground terminal, the force and sense would need to be separated from one triaxial connector (center conductor and guard) to two triaxial connectors with force on the center conductor of one and sense on the center conductor of another. The only such ‘splitter’ available was from Agilent was expensive, hence, a simpler approach was used where the force and sense were shorted right inside the connector (CS-631) to the probe station as seen in figure 5.2.

Now the probe tips are ready to be contacted to the spectroscopic measurement unit bond pads. All connections are double checked for integrity and correctness. The drain probe is positioned over the measurement unit and gently brought into contact with the drain electrode. As the probe touches the electrode, it skids gently on the surface leaving a small scratch on the surface. This indicates that the probe has good contact with the measurement unit. Similarly, the source probe is also positioned and lowered on to the source electrode. Figure 5.3 shows an actual photograph taken of the Janis ST-500 probe station with the inset showing the chip carrier mounted on the sample chuck held down using clips.

Ground loops are a prominent source of noise in any measurement set-up and are caused by the presence of two grounds in the circuit. The best way to check for them is by looking over the circuit and ensuring that the outer shield of the triaxial cables connecting the device to the parameter analyzer is separate from the vacuum pump and other ground connections and support structure. After all the connections were made and the probes touched on the source and drain electrodes, whilst still applying 0V, the microscope, light source for the microscope and the LCD monitor cables were unplugged from these devices and their power adapters removed from the power strip. This was done to ensure no ground loops existed. Only the Agilent 4157B should act as the ground. The noise of this entire setup without any spectroscopic measurement unit (open circuit) was measured to be in the order of a few tenths of femto amps at voltages in the range of 0 V - 0.5 V.

The Agilent 4157B is controlled by a computer and GPIB protocol used for communication between the computer and the parameter analyzer system. The source-drain bias is controlled using the LabVIEW 7.0 program developed in house. The sweep parameters such as voltage range, current compliance, power compliance, integration time, hold and delay times are all controlled by the program. Upon completion, the data is sent back to the computer from the internal buffer on the Agilent 4157B and saved as text file.

Low temperature (77K – 225K) measurements were also accomplished in the Janis ST-500 variable temperature probe station. All the wiring connections were the same as the room temperature measurements. After pumping down the ST-500 chamber with the dry mechanical pump, the turbo molecular pump (EXT75DX, BOC Edwards Inc.) was turned on. Pressures in the order of 5 $*10^{-6}$ Torr attained using this turbo molecular pump was a requirement to start cooling the sample stage, radiation shield and the probe tips with liquid nitrogen. The Lake Shore 331 temperature controller was connected to the ST-500 chamber using the supplied 10 pin connector and turned on to monitor temperature. The LS-331 reads the temperature of the chuck inside the chamber using a silicon diode placed on the bottom of the chuck. The chuck also came with a heater element with three modes of heating (low, medium and high modes). This heater was used to control the temperature of the chuck while flowing liquid nitrogen.

For the first time the dewar was filled, it was purged with dry nitrogen gas for about 30 minutes to remove any moisture inside the dewar and prevent any ice formation. About 80 lbs of liquid nitrogen was transferred into the storage dewar from the holding tank while placing the dewar on a scale to measure weight of added liquid nitrogen. The vent valve on the dewar was left open during the fill process to prevent any pressure build up. Once the dewar was full (~80 lbs), the top flange on the dewar was closed. The vent valve was closed at this point to start building nitrogen pressure inside the dewar. Pressure of ~ 4.0 psi was reached within a couple hours. A pressure relief valve (rate at 5 psi) was located at the outlet flange.

A liquid nitrogen transfer line was used to transfer the liquid nitrogen to the ST-500 chamber cold head. The outer jacket of this transfer line was pumped down with the dry mechanical pump for about 1 hour to reduce any heat transfer to the ambient through this jacket. The transfer line was then inserted very slowly into the dewar while the flow regulator valve at the transfer line was kept open at around 3 turns. As the transfer line entered into the dewar, due to heat from the transfer line, some nitrogen gas escaped from the line. The nitrogen gas was allowed to vent for approximately 5 minutes to ensure no blockage in the

transfer line. After this, the other end of the transfer line was slowly pushed into the inlet of the ST-500 cold head. Extreme care was taken so as not to bump the inlet port on the chamber and the transfer line pushed in all the way and sealed with the chamber using a o-ring locking nut. Nitrogen gas, pushed due to the pressure build up in the storage dewar, flowed out of the outlet on the ST-500 chamber. Once no blockage of nitrogen was confirmed, the flow regulator valve on the transfer line was closed slowly till it was open only to 1½ turns. During this initial cool down, to prevent any ice formation on the sample surface, the heater was turned on at medium power settings and the temperature maintained at 295K for approximately 30 minutes. The temperature set point on the LS-331 was dropped by 5 degrees every 20 minutes till the set point of 270K was reached.

The flow regulator valve was adjusted in such a way that the cooling rate was only 2K/minute. This ensured that the sample did not undergo any thermal shock during cool down. Final temperature of ~77K was reached within a few hours. The wiring connections were connections were identical to the room temperature connections and equal prudence was given while connecting the wires to prevent and electrostatic discharge on the sample.

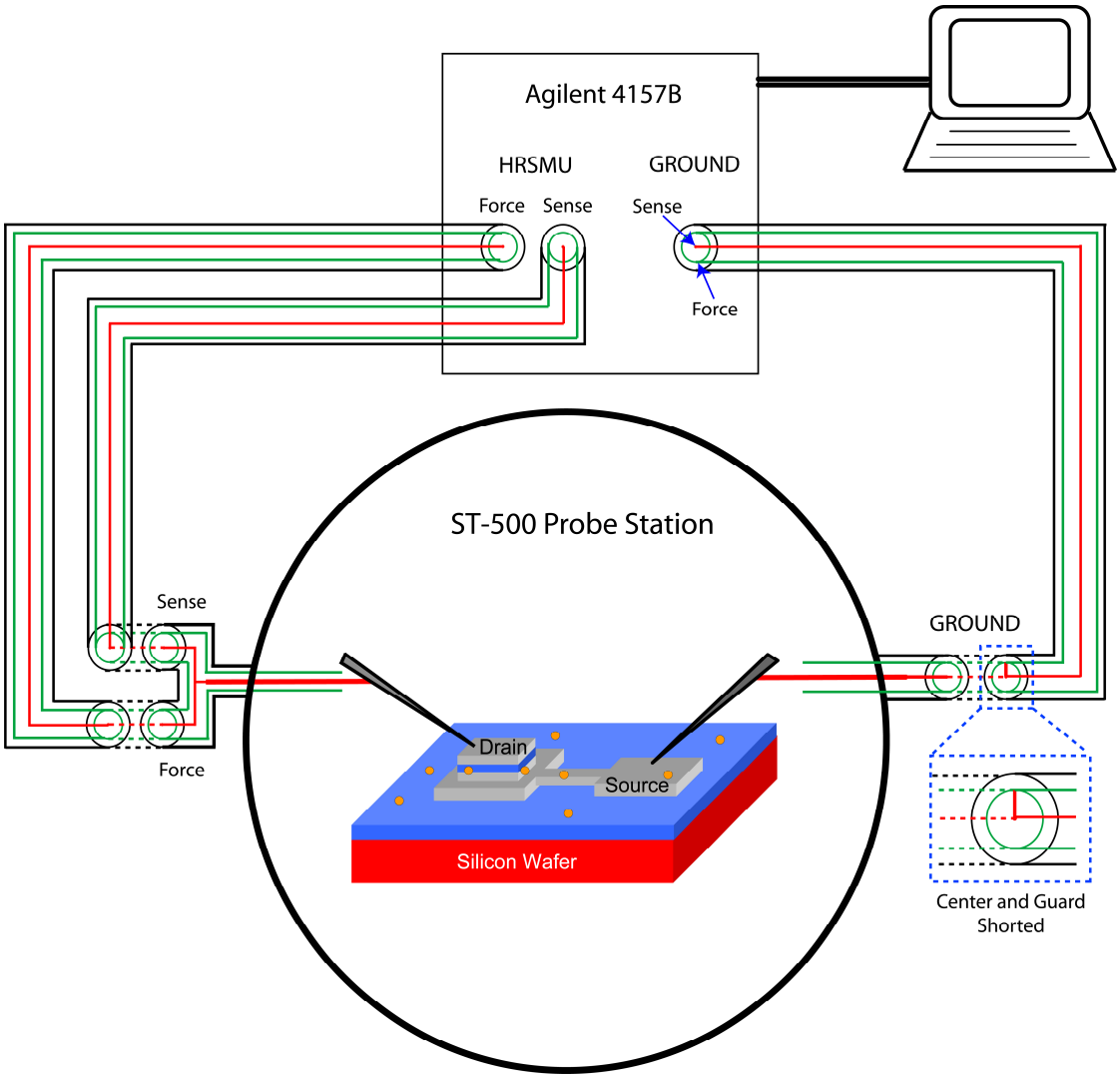


Figure 5.2: Janis ST-500/Agilent 4157B measurement setup for room and cryogenic temperature spectroscopic measurements. Solid lines are triaxial wires and dashed lines are connectors.

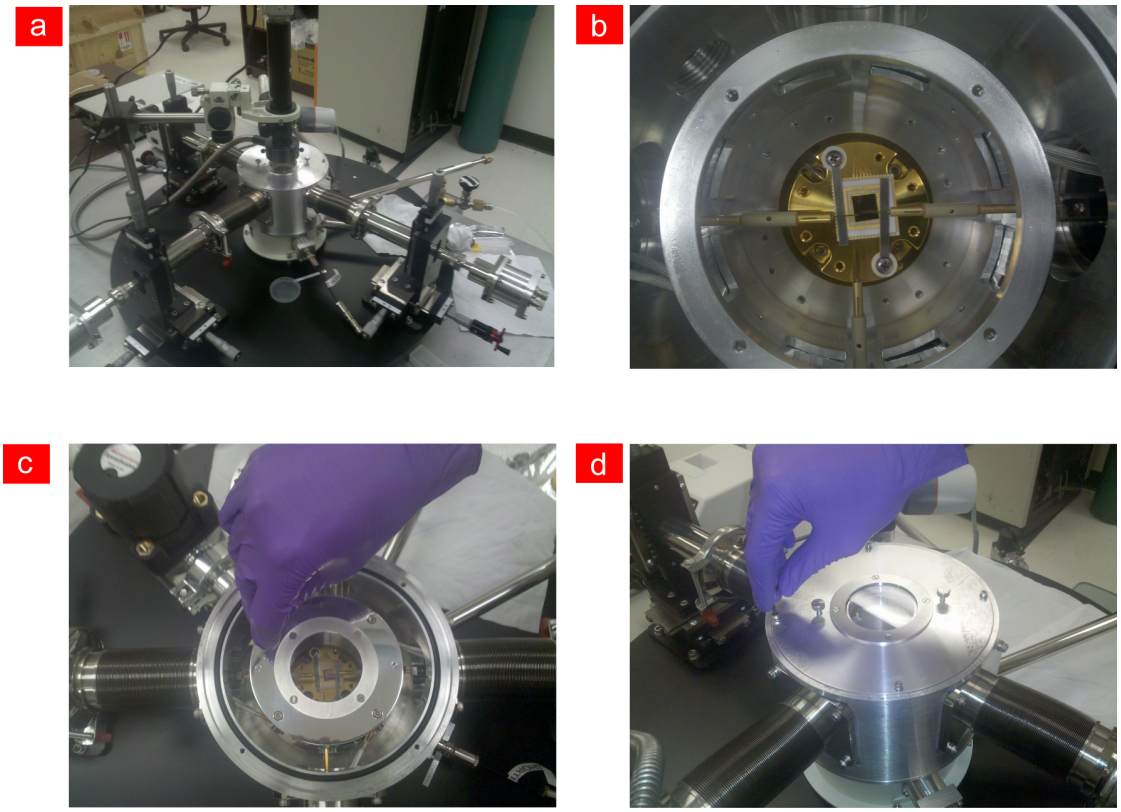


Figure 5.3: (a) Photograph of Janis ST-500 variable temperature probe station showing the micromanipulators and optical microscope with boom. (b) The chip carrier mounted on the chuck held down by the sample clips (c) Radiation shield of the ST-500 and, (d) Top/vacuum cover of the ST-500 probe station.

5.1.1.1 Numerical differentiation of the current-voltage plot

The basic technique of numerical differentiation of the current-voltage plot is outlined in figure 5.4. This technique is prone to more noise as any noise in the current-voltage plot leads to magnify that in the differential conductance plot. From a current-voltage staircase sweep measurement, the differential conductance can be calculated numerically. For a known small increase in current (ΔI), the differential voltage (ΔV) is given by the difference between voltages in points A and B. The differential conductance is then just the ratio of $\Delta I/\Delta V$.

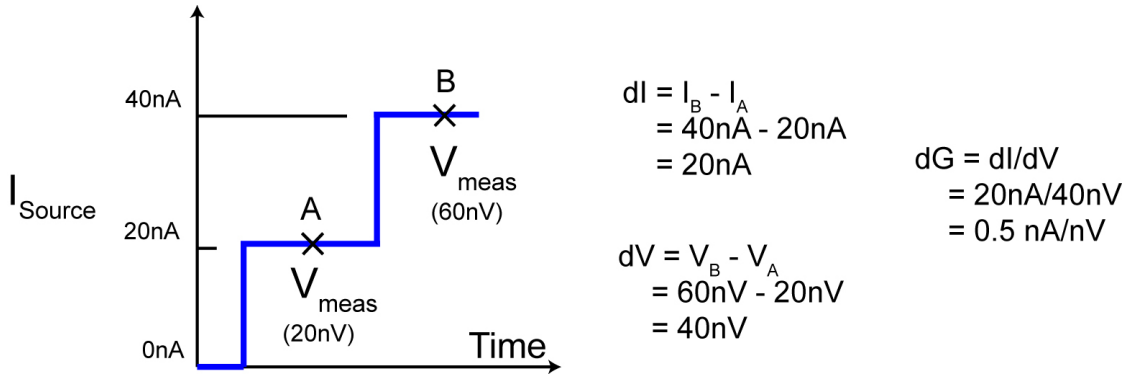


Figure 5.4: Basic method of calculating the differential conductance from current-voltage by numerical differentiation.

The method to numerically obtain clear differential conductance (*dI/dV*) from current-voltage (*I-V*) was taken from Keithely Inc which was originally developed to directly measure the differential conductance using Keithley 6221/2182A [5.2]. In the Keithley method, current is sourced in small increments (*dI*) and the differential voltage (*dV*) is measured for these small increments. A step-wise current impulse is sourced as shown in figure 5.5 and the resultant voltage measured at each increment of current. To reduce noise that may be part of the current-voltage measurements, a 3-point averaging technique is used. The basic measurement scheme is shown in figure 5.5.

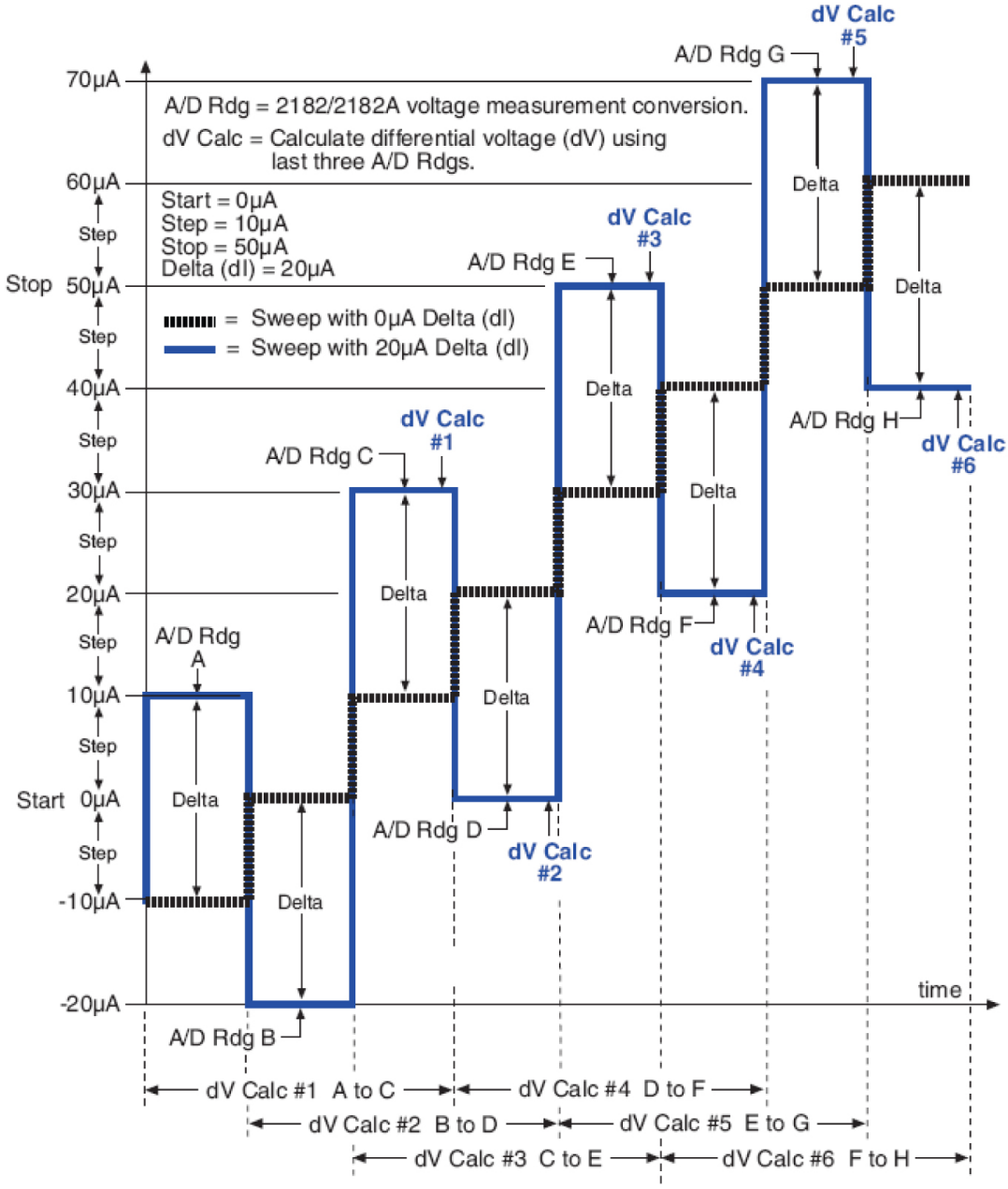


Figure 5.5: Keithley method of measurement of differential conductance.

Points marked A, B, C …H in figure 5.5 are the points where voltage is measured. The calculations for *dV* from the measured values of *V* are detailed below:

$$dV\#1 = \frac{\left[(A+B)/2 + (C-B)/2\right]}{2} \cdot (-1)^0$$

$$dV\#2 = \frac{\left[(B-C)/2 + (D-C)/2\right]}{2} \cdot (-1)^1$$

$$dV\#3 = \frac{\left[(C-D)/2 + (E-D)/2\right]}{2} \cdot (-1)^2$$

$$dV\#4 = \frac{\left[(D-E)/2 + (F-E)/2\right]}{2} \cdot (-1)^3$$

$$dV\#5 = \frac{\left[(E-F)/2 + (G-F)/2\right]}{2} \cdot (-1)^4$$

$$dV\#6 = \frac{\left[(F-G)/2 + (H-G)/2\right]}{2} \cdot (-1)^5$$

Using the known (sourced) *dI* value and the measured *dV* values, the differential conductance can be calculated easily. In this study, instead of sourcing current, voltage was sourced and the resultant current through the measurement unit measured. A simple staircase sweep of voltage was performed and the resultant current was measured. The current voltage plot was re-arranged to appear like the pulse input in figure 5.5. Thus from the sourced *dV* and the measured *dI* (from similar calculations as outlined above for current instead of voltage), the differential conductance *dI/dV* was numerically calculated. This system of numerically calculating the differential conductance proved to produce less noise than the conventional system of numerical differentiation.

5.1.2 Direct differential conductance measurements

Direct measurement of the tunneling conductance of individual nanoparticles was done using the setup shown in figure 5.6. Both room temperature and low temperature direct differential conductance measurements were done with the samples loaded in the Janis ST-500 variable temperature probe station. Similar to the I-V measurements, all wiring (coaxial and triaxial) was done using low noise cables (Keithley Inc.). All the wiring was made in house to custom lengths to avoid any extra capacitance or resistances using connectors from Keithley Inc.

To remove any ground loops, the only ground in the circuit was the Agilent 4157B ground. All other instruments were floating with no grounds. As with the I-V measurements, extreme care was taken to prevent any electrostatic shock to the samples. All the electronics were turned on for at least 30 minutes to an hour for warm up before any measurements were conducted. The wiring sequence was as follows:

The Agilent 4157B HRSMU was forced to 0V. The force triaxial connector was connected to the input A of the summing amplifier (SIM-980) while the output was forced to 0V. The guard wire at the connection at the SIM-980 was disconnected from any other connection using a guard disconnected/ Triaxial to Coaxial connector. In this connector, the center conductor from the triaxial wire was connected to the center pin of the male coaxial connector, and, the shield from the triaxial wire was connected to the shield of the coaxial connector, thereby disconnecting the guard wire completely as seen in figure 5.6. Hence, the guard wire extended all the way from the HRSMU output to right at the triaxial to coaxial connector thereby reducing any noise.

The internal sine wave generator of the SR-830 lock-in amplifier was connected to the input of the scaling amplifier SIM-983 using coaxial cables and connector. The scaling amplifier was used to scale down the 4mV amplitude of the sine generator to 1mV by setting a scaling

factor of 0.25. The scaled output from the SIM-983 was connected to the input B of the SIM-980 using coaxial wire and connectors. The summed/mixed output (ac and dc components) from the SIM-980 was connected to the source triaxial connector on the ST-500 using triaxial wire and male connector. Inside this triaxial connector, the guard and shield of the triaxial cable was shorted as seen in figure 5.4 to reduce/eliminate any noise.

The drain electrode on the ST-500 was connected to the input of a resistor box with a 10 kΩ connected inside the noise shielding box (low noise metal-film resistor, 0.5W, Allied Electronics Inc.) to protect the electronics in case of device failure (shorting – causing high currents) using triaxial wire and triaxial connector (shield and guard shorted) at the drain end of the ST-500 and coaxial connector at the resistor box housing. The shield from the triaxial wire was connected to the resistor box shield and center conductor connected internally to the low noise resistor. The output of the resistor box was connected to the current pre-amplifier SR-570 directly with male connectors at the end of the resistor box housing. Once again the guard and shield was shorted near the coaxial end to reduce noise. The operational settings for the SR-570 and SR-830 will be explained in further detail in section 5.1.2.2. After these connections were made, the source probe tip was lowered onto the source electrode and then the drain probe tip lowered onto the drain electrode of the spectroscopic measurement unit. This procedure avoided any electrostatic shock to the measurement unit.

After lowering the probe tips, the output of the SR-570 was connected to the input A of the SR-830 lock-in amplifier using coaxial wires and connectors. The digital microscope, light source and LCD monitor were all unplugged and the power chords removed from the power strip. All this was done while holding the HRSMU force at 0 V. After all these steps were completed, the output of the HRSMU was turned off and the system was ready for measurement.

As the case with the I-V measurements, the Agilent 4157B and the SR-830 lock-in amplifier were computer controlled using GPIB protocol. A home-developed LabVIEW 7.0

program was used to conduct measurements and to set the parameters for the measurements. The SIM-980 and SIM-983 did not need any computer control as they were used with fixed factors such as scaling factor of 0.25 in the SIM-983 and addition settings for input A and B in the SIM-980.

For low temperature measurements, the cool down procedure was identical to the low temperature I-V measurements. The connections were also identical to the room temperature connections outlined above. The measurements can be run with or without the temperature controller connected as there was no difference in measurements or any noise from the instrument being switched on.

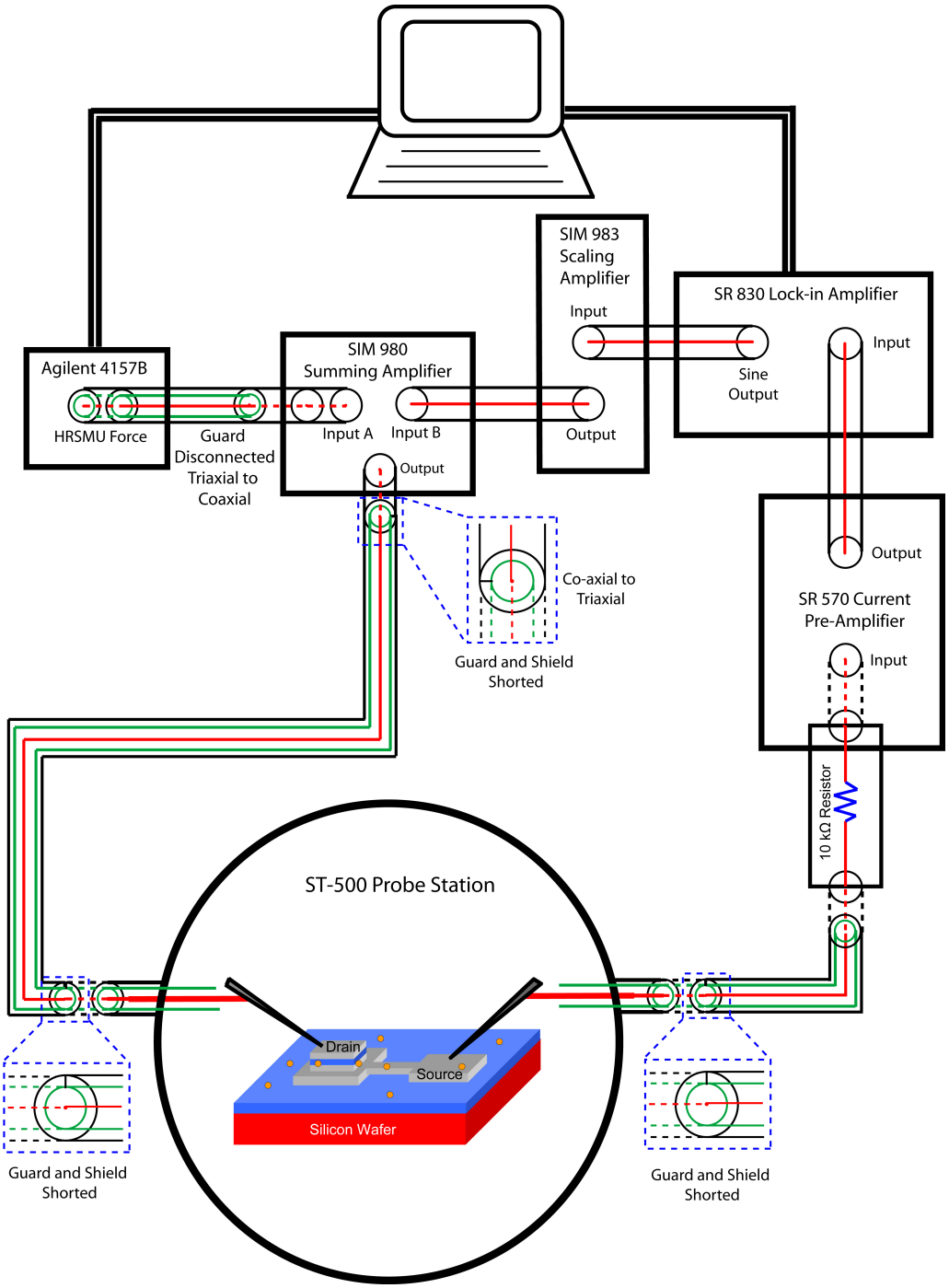


Figure 5.6: SR830/SR570/SR893/Agilent 4157B – Direct differential conductance measurement setup for room and low temperature spectroscopic measurements. Solid lines are hard connections through low noise coaxial or triaxial wires, and dashed lines are through connectors.

5.1.2.1 How to directly measure differential conductance

It is important to know how the SR-830 lock-in amplifier directly measures the differential conductance of the spectroscopic measurement unit. This section introduces the mathematical equations for measuring the differential conductance (*dI/dV*) directly by using the lock-in amplifier.

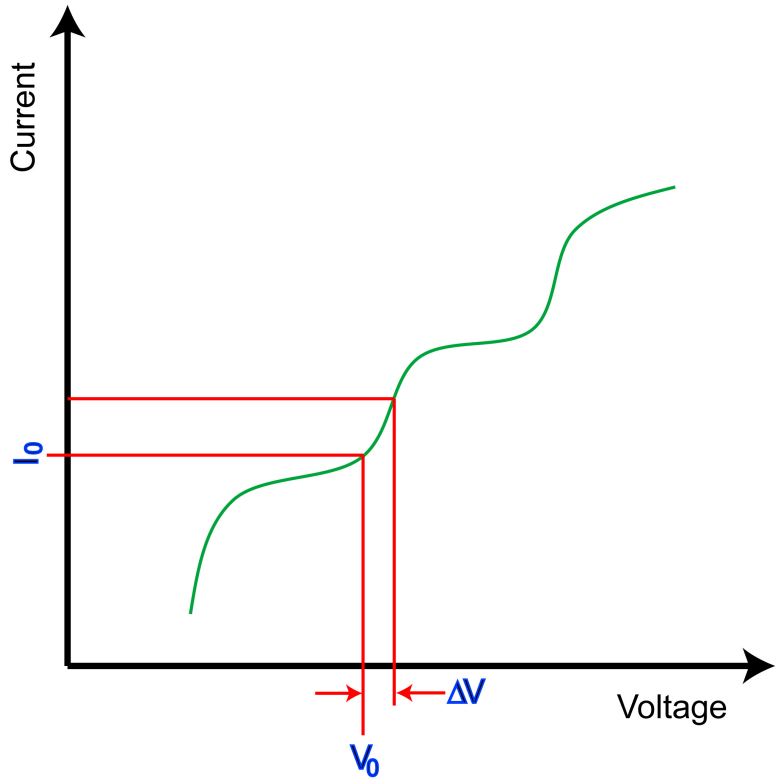


Figure 5.7: Schematic of a Current-Voltage plot where at voltage V_0, current is I_0.

As shown in figure 5.7, lets assume a current-voltage plot with current *I* varying as a function of the applied bias voltage *V*. We can write this as follows:

$$I = I(V)$$

If infinitesimal small voltage of ΔV is added, then the current *I* at $V_0 + \Delta V$ can be written as, (assuming ΔV is infinitesimally small):

$$I(V_0 + \Delta V) = I(V_0) + \left(\frac{dI}{dV}\right)_{V_0} .\Delta V$$

ΔV can be written as a sine function as:

$$\Delta V = V_{input} \sin \omega_l t$$

This yields the current *I* as a function of time *t* as follows, assuming no phase difference:

$$\Rightarrow I(t) = I(V_0) + \left(\frac{dI}{dV}\right)_{V_0} .V_{input} \sin \omega_l t \,,$$

If there is a phase shift/difference, then,

$$I(t) = I(V_0) + \left(\frac{dI}{dV}\right)_{V_0} .V_{input} \sin\left(\omega_l t + \theta_{sig}\right),$$

Where, θ_{sig} , is the phase difference.

The lock-in amplifier SR-830 amplifies the input signal and multiplies it with a reference signal (in this case it is an internally generated sine wave) using a phase sensitive detector or multiplier. The phase sensitive detector output is simply the product of two sine waves.

$$V_{PSD} \propto I(t) \cdot V_L \sin\left(\omega_l t + \theta_{ref}\right)$$

Where, $V_L \sin\left(\omega_l t + \theta_{ref}\right)$, is the reference signal from the internal oscillator in the SR-830.

$$V_{PSD} \propto \left[I(V_0) + \left(\frac{dI}{dV}\right)_{V_0} .V_{input} \sin\left(\omega_l t + \theta_{sig}\right) \right] \cdot V_L \sin\left(\omega_l t + \theta_{ref}\right)$$

$$V_{PSD} \propto \left\{ I(V_0) \cdot V_L \sin\left(\omega_l t + \vartheta_{ref}\right) \right\} + \left\{ \left[\left(\frac{dI}{dV}\right)_{V_0} .V_{input} \sin\left(\omega_l t + \theta_{sig}\right) \right] \cdot V_L \sin\left(\omega_l t + \theta_{ref}\right) \right\}$$

$$V_{PSD} \propto \left\{ I(V_0) \cdot V_L \sin\left(\omega_l t + \vartheta_{ref}\right) \right\} +$$

$$\frac{1}{2}\left(\frac{dI}{dV}\right)_{V_0} V_{input} V_L \left\{ \cos\left[(\omega_l - \omega_l)t + \theta_{sig} - \theta_{ref}\right] - \cos\left[(\omega_l + \omega_l)t + \theta_{sig} + \theta_{ref}\right] \right\}$$

$$V_{PSD} \propto \left\{ I(V_0) \cdot V_L \sin\left(\omega_l t + \vartheta_{ref}\right)\right\} +$$
$$\frac{1}{2}\left(\frac{dI}{dV}\right)_{V_0} V_{input} V_L \left\{\cos\left[\theta_{sig} - \theta_{ref}\right] - \cos\left[2\omega_l t + \theta_{sig} + \theta_{ref}\right]\right\}$$

When the phase sensitive detector output is passed through a low pass filter, all ac components are filtered/removed including the *2ωt* terms. This leaves the following:

$$V_{PSD} \propto \frac{1}{2}\left(\frac{dI}{dV}\right)_{V_0} V_{input} V_L \left\{\cos\left(\theta_{sig} - \theta_{ref}\right)\right\}$$

If the signal is made up of signal plus noise, only the noise frequencies close to the reference frequency will be detected by the phase sensitive detector and low pass filter. All other noise frequencies are removed by the low pass filter. Noise frequencies very close to the reference frequency will result in very low frequency ac output along with the phase sensitive detector output. The bandwidth and roll off of the low pass filter determine the attenuation of these ac components. Only the signal at the reference frequency yields true dc output, hence, a smaller bandwidth of low pass filter is better for this purpose.

Typically, the external reference sine wave is phase locked with the internal oscillator in the lock-in amplifier. Since we use the internal oscillator as the reference signal, it is automatically phase locked. When the θ_{sig} is the same as θ_{ref} then, cos (θ_{sig} - θ_{ref}) = cos (0) = 1, other wise the output of the PSD contains the cosine term. To remove any dependency of the PSD output on the cosine term, another PSD is added and the signal multiplied by reference phase shifted by 90^0. The reference signal of the PSD2 is thus:

$$V_{PSD-2} \propto I(t) \cdot V_L \sin\left(\omega_l t + \theta_{ref} + 90^0\right)$$

$$V_{PSD-2} \propto \frac{1}{2}\left(\frac{dI}{dV}\right)_{V_0} V_{input} V_L \left\{\cos\left(\theta_{sig} - \theta_{ref} - 90^0\right)\right\}$$

$$V_{PSD-2} \propto \frac{1}{2}\left(\frac{dI}{dV}\right)_{V_0} V_{input} V_L \left\{\sin\left(\theta_{sig} - \theta_{ref}\right)\right\}$$

To remove the proportionality sign from these equations, the constant term 'gain' *G* is added. This gain value is a combination of gain from both the lock-in amplifier SR-830 (if operating in current input mode) and the current pre-amplifier (SR-570) gain values. Hence the output of both the PSD will be as follows:

$$X = V_{PSD} = G \cdot \frac{1}{2}\left(\frac{dI}{dV}\right)_{V_0} V_{input} V_L \left\{\cos\left(\theta_{sig} - \theta_{ref}\right)\right\}$$

$$Y = V_{PSD-2} = G \cdot \frac{1}{2}\left(\frac{dI}{dV}\right)_{V_0} V_{input} V_L \left\{\sin\left(\theta_{sig} - \theta_{ref}\right)\right\}$$

The *X* and *Y* represent the signal as a vector relative to the lock-in reference signal, where *X* is the 'in-phase' term and *Y* is the quadrature term. When phase difference (θ_{sig} - θ_{ref}) = 0, the PSD measures only *X* or the signal and *Y* = 0.

To remove any phase dependency, the magnitude of this vector can be calculated as follows:

$$R = \sqrt{X^2 + Y^2}$$

$$R = \sqrt{\left[G \cdot \frac{1}{2}\left(\frac{dI}{dV}\right)_{V_0} V_{input} V_L \left\{\cos\left(\theta_{sig} - \theta_{ref}\right)\right\}\right]^2 + \left[G \cdot \frac{1}{2}\left(\frac{dI}{dV}\right)_{V_0} V_{input} V_L \left\{\sin\left(\theta_{sig} - \theta_{ref}\right)\right\}\right]^2}$$

$$R = \frac{1}{2} G \cdot \left(\frac{dI}{dV}\right)_{V_0} \cdot \left(\sqrt{2} \cdot V_{input,RMS}\right) \cdot \left(\sqrt{2} \cdot V_{L,RMS}\right)$$

$$R \propto G \cdot \left(\frac{dI}{dV}\right)_{V_0} \cdot \left(V_{input,RMS}\right) \cdot \left(V_{L,RMS}\right)$$

In the SR-830, the internal sine wave generator is used as the reference signals; hence, the *R* is automatically compensated with $V_{input,RMS}$. The output of the lock-in amplifier *R* then becomes as follows:

$$R \propto G \cdot \left(\frac{dI}{dV}\right)_{V_0}$$

In summary, by the addition of a small ac component to the dc biasing, the differential conductance of the spectroscopic measurement unit can be directly measured using the lock-in amplifier.

5.1.2.2 Selection of settings to measure differential conductance

5.1.2.2.1 Current pre-amplifier SR-570 settings

This section will deal with selecting the various settings available to be used in both the lock-in amplifier SR-830 and the current pre-amplifier SR-570. Before selecting any settings for a particular spectroscopic measurement unit, the I-V plot was conducted using the procedure detailed in section 5.1.1. From the I-V plot, the resistance of the specific unit was noted at +1V (since it is not linear resistance for these units, the resistance at +1V applied was chosen). Using this resistance and the cables capacitance values, the *RC* delay time was calculated. Based on this RC delay time, the frequency of operation ω was chosen. The current pre-amplifier SR-570 converts the current from the drain of the spectroscopic measurement unit and converts it into voltage scale. It offers extremely good sensitivity/gain and also offers excellent filters to remove any noise directly from the source before feeding the signal into the lock-in amplifier. The front panel for SR-570 is shown in figure 5.8.

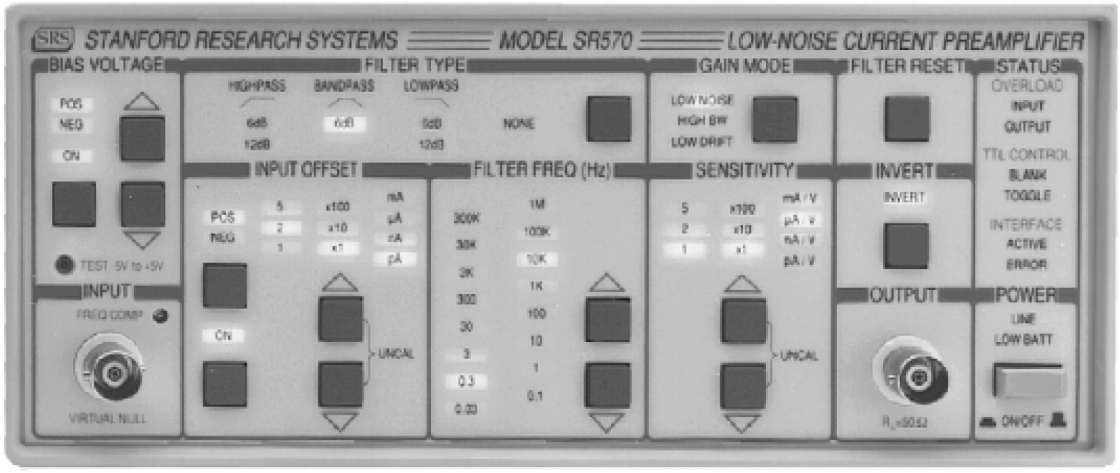


Figure 5.8: Front panel of the current pre-amplifier SR-570

The various settings options for the SR-570 current pre-amplifier and lock-in amplifier SR-830 are listed in the table below:

1. Bias voltage
2. Input offset
3. Filter type and frequency
4. Gain mode
5. Sensitivity

1. Bias voltage: This option was disabled as there was no need to add any more bias voltage to the output from the drain.
2. Input offset: This option was disabled as there was no need to offset any of the signal.
3. Filter type and frequency: The options included high pass filter, low pass filter and band pass filter. The roll off for the low pass and high pass filter could be set to either 6 dB/oct or 12 dB/oct. The 12 dB/oct was just two such filters in series. The operating range of our measurements was 7 Hz-15 Hz, so a band pass filter of 3 Hz – 30 Hz with 6 dB/oct roll off was chosen. Figure 5.9 shows a plot of the filter characteristics for

these settings. As seen from figure 5.9, most of the signal (gain ~ -0.831 > 90%) of the signal is intact with very little loss in the operating region from 7-15 Hz.

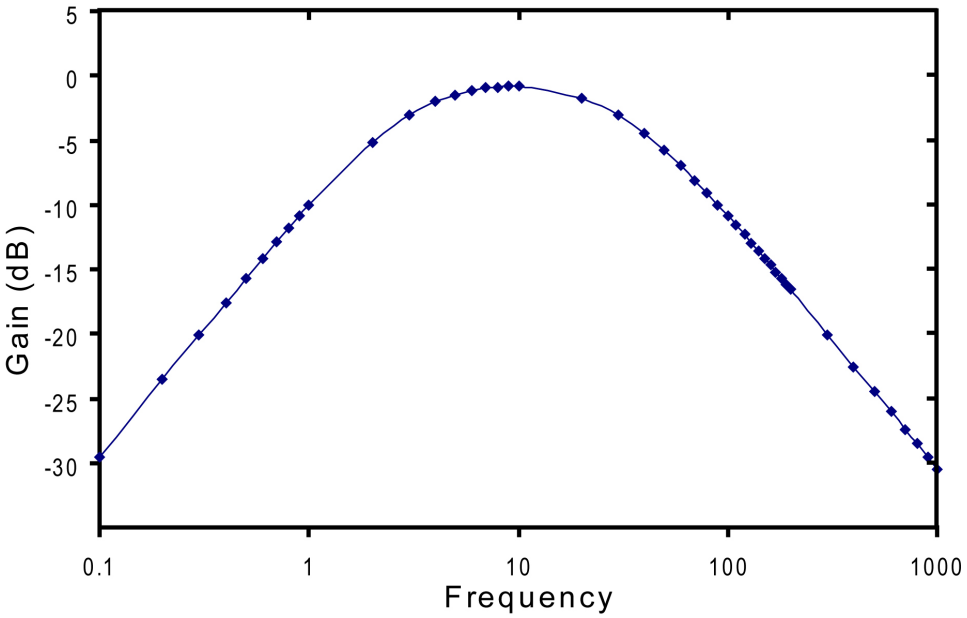
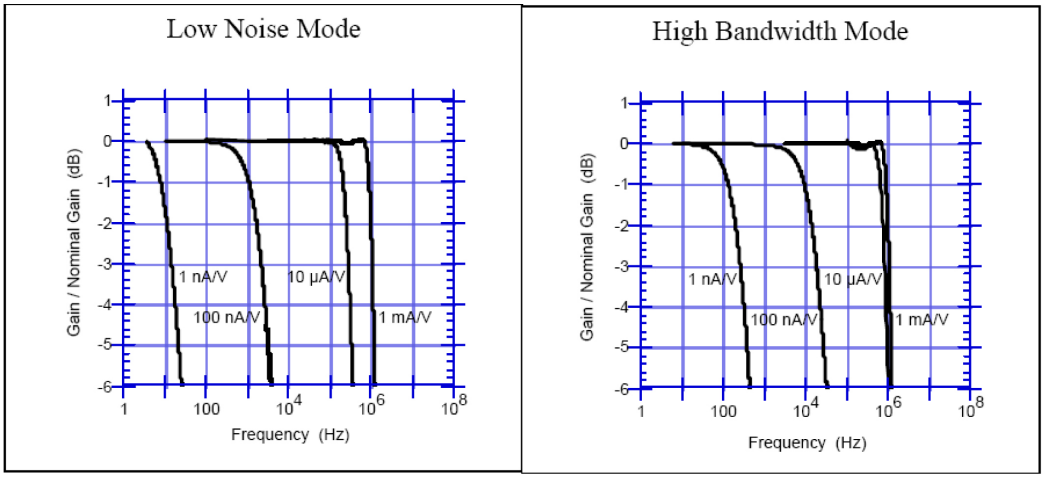


Figure 5.9: Band pass filter 3-30 Hz with 6 dB/oct roll off.

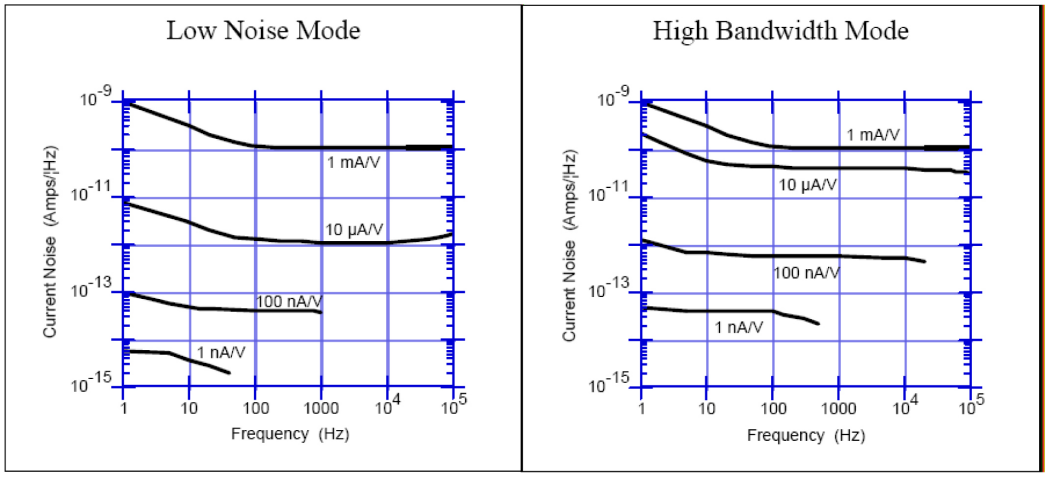
4. Gain mode: The options for gain mode were low noise, high bandwidth and low drift. These settings are of paramount importance as any wrong settings will cancel out the actual signal instead of any noise. Figure 5.10(a) is plot of amplifier gain in different modes (low noise and high bandwidth) for different sensitivity ranges. As our measurement units have very low currents (in the order of <5 nA) and the frequency setting of 7-15 Hz, only high bandwidth mode can be used as there is no drop off in any signal at the operating frequency range. If the low noise mode is used, for 10Hz, there is a loss of ~50% (gain = -3dB) of actual signal. To avoid any such losses, only the high bandwidth mode was used. The trade off comes with the current noise where at 10 Hz, the current noise for the low noise mode is < 0.01 pA, where as in the high bandwidth mode the current noise is < 0.1 pA with the same sensitivity scale of 1nA/V.

a



Amplifier Bandwidth for different sensitivity

b



Current noise for different sensitivity

Figure 5.10: (a) Amplifier bandwidth and (b) current noise for different sensitivity settings on the current pre-amplifier SR-570.

5. Sensitivity: Depending on the current range of the specific spectroscopic measurement unit, the sensitivity was chosen. For example, for a current range of 1 nA at +1V, the sensitivity was chosen as 5n A/V.

Table 5.2: Operational bandwidth and current noise for various gain modes and sensitivity settings.

Sensitivity (A/V)	Bandwidth (3dB)		Noise/$\sqrt{Hz}^2$		DC Input Impedance
	High BW	Low noise	High BW	Low noise	
1mA/V	1 MHz	1 MHz	150 pA	150 pA	1 Ω
1μA/V	200 kHz	20 kHz	600 fA	100 fA	100 Ω
10nA/V	2 kHz	200 Hz	100 fA	60 fA	10 kΩ
1nA/V	200 Hz	15 Hz	60 fA	10 fA	1 MΩ
100pA/V	100 Hz	10 Hz	10 fA	5 fA	1 MΩ
1pA/V	10 Hz	10 Hz	5 fA	5 fA	1 MΩ

5.1.2.2.2 Lock-in amplifier SR-830 settings

The current pre-amplifier SR-570 amplifies and converts the current input into voltage output and that is fed into the lock-in amplifier SR-830. The block diagram of the SR-830 is shown in figure 5.11. The various parameters to be set at the SR-830 are as follows:

1. Frequency and amplitude of sine output
2. Input type
3. Notch filters
4. Time constant (cut-off frequency and slope), and,
5. Sensitivity

1. Frequency and amplitude: Selection of frequency range has already been discussed in section 5.1.2.1. The amplitude of the sine wave that is added to the dc input has to be smaller than the width of expected conductance peaks to resolve it, hence amplitude of 4 mV (the lowest output available from the SR-830) was chosen. To reduce the

amplitude further, a scaling amplifier SR-983 was used with a scaling factor of 0.25 to reduce the amplitude to 1 mV.

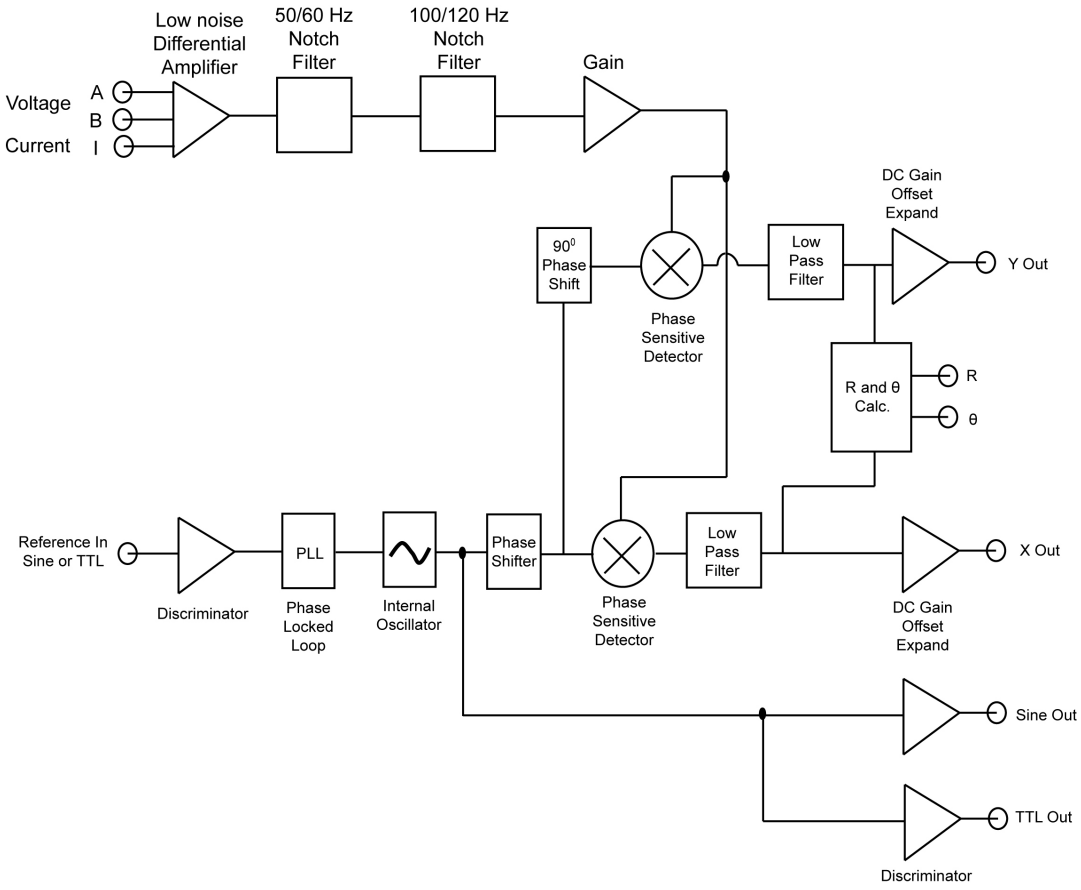


Figure 5.11: Block diagram of SR-830 lock-in amplifier

2. Input type: The options for input type are either A (single input), B (differential input) or current (I). In this particular set shown in figure 5.6, the input mode is A. Figure 5.12 is a block diagram for input A. The SR-830 ‘quasi-floats’ the system in this mode by separating the ground of the SR-830 from the shield of the input by a resistor (10 kΩ). If the ground were to be used, then it would cause a ground loop with the ground from the Agilent 4157B.

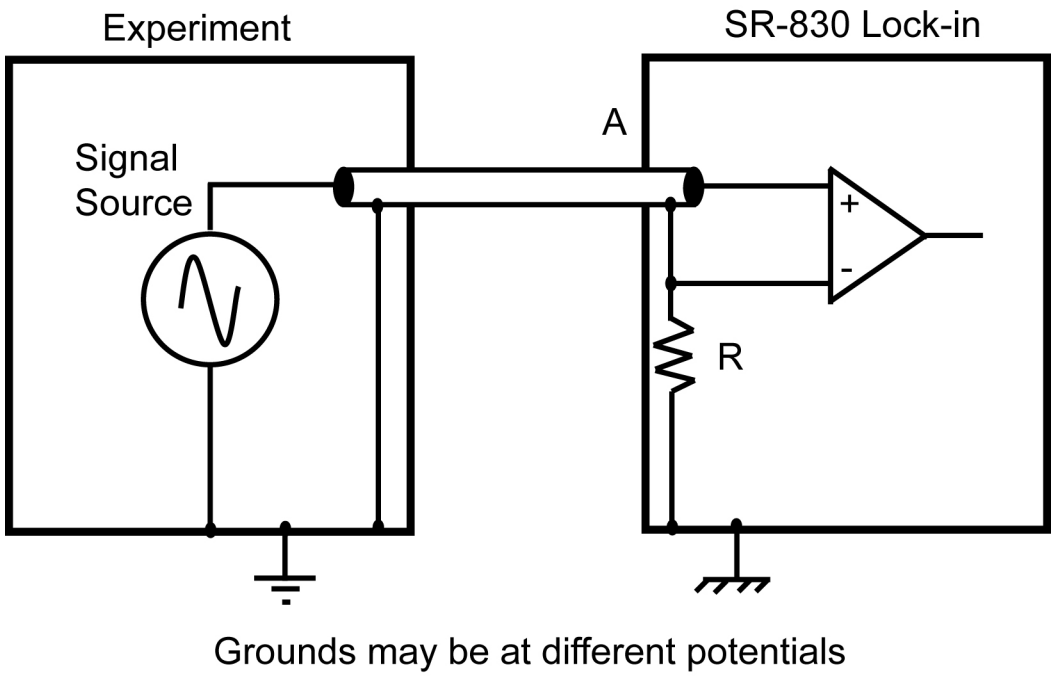


Figure 5.12: SR-830 input connections with input configured to Input A

3. Notch filters: The line notch filters are pre-tuned to the line frequency (50 or 60 Hz) and twice the line frequency (100 or 120Hz). Both the notch filters with an attenuation depth of 30 dB are used to reduce any line noise.
4. Time constant: The output of the phase sensitive detector in ideal case should be dc. Any noise to the input of the PSD is reflected by some ac noise in the output. The time constant is a simple low pass filter with tunable cutoff frequency (time constant) and tunable attenuation slope. The low pass filter characteristics for cutoff frequency of 10Hz and various attenuation slopes is shown in figure 5.13. Smaller time constants (larger cutoff frequency) give more noise compared to larger time constants. The trade-off being the settling time for the low pass filter. A settling time 5X of the time constant is required for reliable measurements. For example, with a time constant of 3 s, per point hold time would need to be 15 s at the minimum. For measurements, it is not practical to have a time constant of over 10 s as this would result in impractical delay

times for the measurement. Hence, a time constant of 10s was chosen. Time constant of 10 s yields cutoff frequency of 0.0159 Hz. The maximum filter slope of 24 dB/oct was chosen to reduce any ac noise in the output.

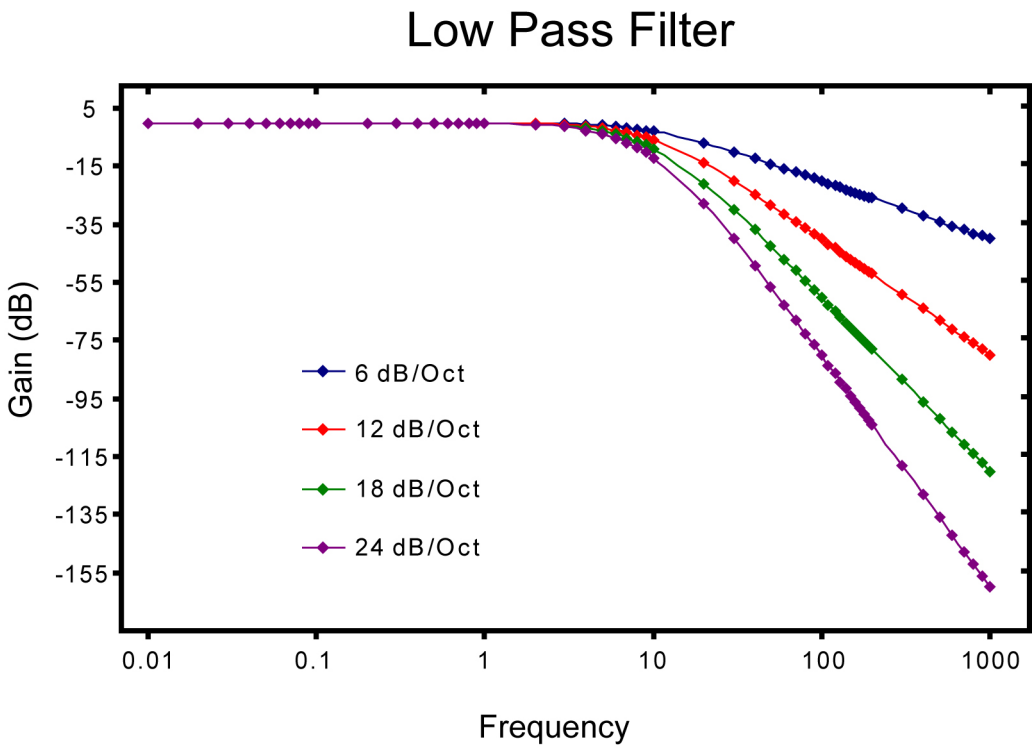


Figure 5.13: Low pass filter characteristics with cut-off frequency at 10 Hz and with roll off 8, 12, 18 and 24 dB/oct.

5. Sensitivity: The sensitivity is the scale of the measured output and can be varied from 2nV to 1V scale in the voltage scale and from 2fA to 1μA (RMS) in the current scale. The auto gain mode automatically adjusts the sensitivity to the required scale.

5.2 Solid-state tunneling spectroscopy resonant tunneling spectra

The double barrier tunnel junction spectroscopic unit with ~7nm CdSe nanoparticles was used as a model system to study this spectroscopic technique. The room temperature and

low temperature resonant tunneling spectra were measured using either current-voltage or direct differential conductance measurements using the procedures outlined in sections 5.1.1 and 5.1.2. The voltage was swept between -1.3 to +1.3 V for current-voltage measurements with either the Agilent 4155C or 4157B. Any voltage over ±1.3V could cause the dielectric between the source and the drain electrodes to breakdown. A typical current-voltage plot and the corresponding differential conductance calculated using the Keithley method outlined in section 5.1.1.1 is shown below in figure 5.14 for measurement unit # 12. The current-voltage measurements were all repeatable except that the plot would be offset in the voltage scale. This offset most likely comes from trapping of charges in the surrounding dielectric which then acts as a local gate and leads to energetic shift in the quantum dots. To circumvent this issue, after each measurement, 0V was applied for a minimum period of 4 hours. This was found to reproduce the current-voltage plots every time with very little offset. We believe that this application of 0V across the spectroscopic unit allows for the rearrangement of charges both in the dielectric and the quantum dot itself as its left in a charged state when the previous measurement ends at 1.3V. All the current-voltage plots and differential conductance plots shown in this study are the raw data and not corrected with the η (bias distribution) factor.

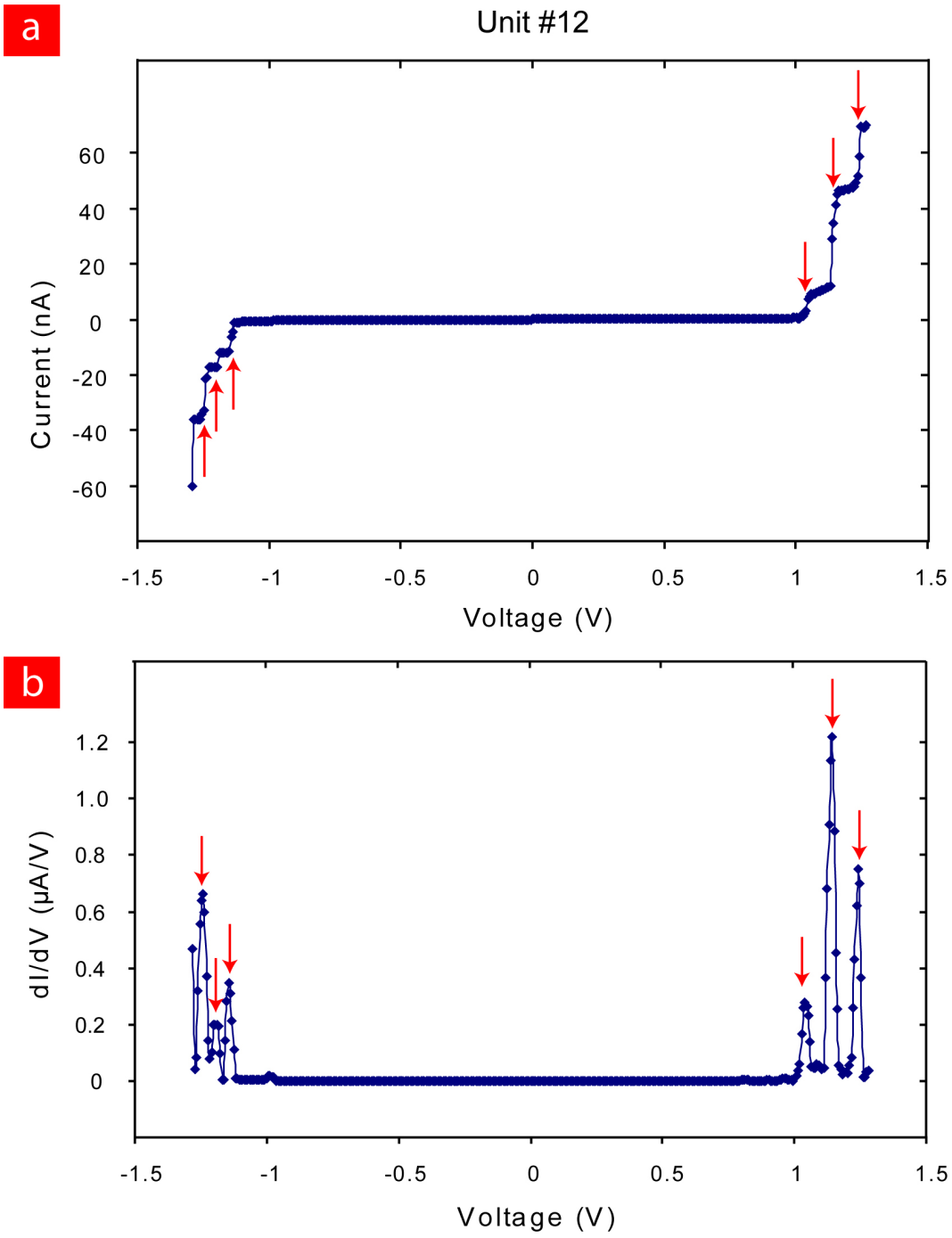


Figure 5.14: (a) Current-voltage plot for unit #12 showing clear step-wise increase in current with bias voltage. (b) Differential conductance obtained by numerically differentiating the current-voltage plot using Keithley method showing peaks for transport through the valence and conduction energy levels in the quantum dot.

A very distinct step-wise increase in current with voltage increase is observed as also observed from STM measurements on such nanocrystals [5.3-5.16]. The *dI /dV* curves show a very high signal-to-noise ratio, indicating the high quality of the current-voltage spectra and the numerically obtained differential conductance spectra. This step-wise current increase corresponds to the peaks observed in the differential conductance plot. The step-wise increase in current is direct evidence of transport through a single quantum dot, and resonant tunneling through the energy levels of the quantum dot. Transport through multiple particles is very complex depending on if the tunneling occurs in-phase or out of phase. In the shell-tunneling regime, the probability to find an electron inside the nanoparticle is always zero, hence there is no charging energy E_c term. The absence of any peaks separated by just the charging energy E_c shows that this case is only shell-tunneling spectroscopy. Also, the increase in the peak heights with increasing bias also indicates the shell tunneling regime. In the shell-filling regime, the first two peaks (s_1 and s_2) will be of equal heights and the next six peaks ($p_1 – p_6$) will be of equal heights.

Several peaks in the negative bias region correspond to the transport through the valence level orbitals and the peaks in the positive bias region correspond to conduction through the conduction band orbitals. The first peak in the negative bias is the occupation of the HOMO level and the first peak in the positive bias is the occupation of the LUMO level. Although all measurement units show similar structure to figure 5.14 (unit # 12), the peaks are all spaced different with different zero-conduction gaps. This is due to the difference in the η factors for all units. The attachment of the quantum dots is very random and hence the η factor will be different for different measurement units. The calculations to decipher the η factor will be detailed later in this section.

It was found during measurements that some units showed the peaks in the positive bias and some in the negative bias all of which had peak similar spacings. The cause for this was that the particle maybe closer to one electrode compared to the other. Hence, the source

and drain electrodes were interchanged instead of just reversing the polarity. The idea behind this was to maintain most of the bias drop across the source and the quantum dot. This meant that depending on initial current-voltage measurements, the source and drain electrodes were interchanged. The reversing of the electrodes was done for nearly 50% of the measurement units. This holds good as the attachment of the quantum dots was completely random and hence the attachment was expected to occur in such fashion.

The most important factor to note from figure 5.14 is the sharp rise in current with change in bias. The rise in current occurs within a window ~30meV. In ideal case at 0K, the current rise is very sharp and the voltage range is minimal (~0meV), but in this case, at room temperature, the noted current increase occurs within only 30meV. This is because of the room temperature thermal energy which broadens the window of current increase. This small window has also been observed for other spectroscopic measurement units in this study and will be shown later in this section.

The main assumption for calculating the η factor is that the mean diameter of the quantum dot is the same as the average size of the quantum dot population ~7nm. The calculation for the η factor for the spectroscopic measurement unit #12 shown in figure 5.14 can then be accomplished as follows:

The measured zero-conductivity gap ΔE_g^{STS} from figure 5.14 was 2.184 eV.

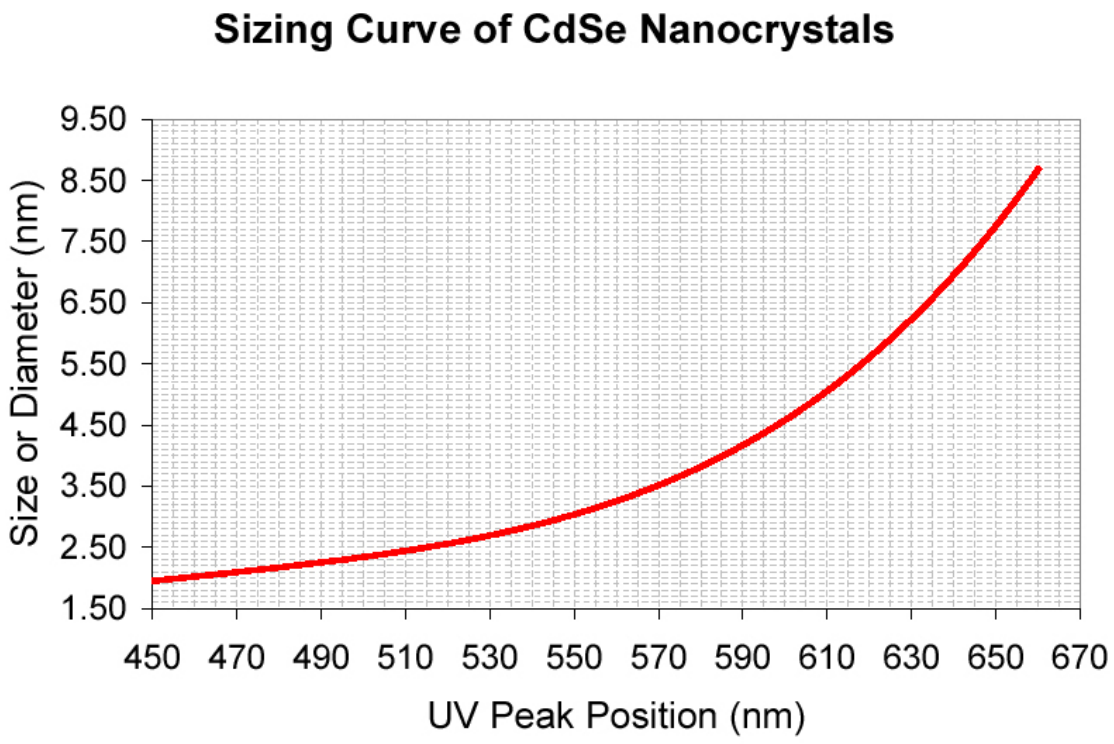


Figure 5.15: Optical absorption peak to size relationship for CdSe nanoparticles suspended in toluene as taken from NN Labs Inc [5.17].

The optical band gap E_g^{opt} was calculated from the size-absorption peak diagram as shown in figure 5.15 [5.17] and calculated to be 1.93 eV. The relation between the optical band gap and the STS band gap is given by the equation as discussed in chapter 2:

$$\eta E_g^{STS} = E_g^{opt} + J_{e-h}$$

where J_{e-h} is the electron-hole coulomb interaction energy, E_g^{STS} is the measured band gap in the resonant tunneling measurements. This interaction energy J_{e-h} can be approximately calculated by the following [5.18]:

$$J_{e-h}(R) = \left(\frac{1}{\varepsilon_{out}} + \frac{0.79}{\varepsilon_{in}} \right) \cdot \frac{e^2}{4\pi\varepsilon_0 R}$$

The value for J_{e-h} was calculated for the 7nm CdSe quantum dots suspended in toluene as received from NN Labs Inc. Substituting the constants: ε_0 = 1.418 E-39 $C^2.eV^{-1}.nm^{-1}$, e = 1.602E-19 C, ε_{in} = 8.0, ε_{out} = 4.5, R = 3.5 nm, the calculated value for the J_{e-h} was found to be 0.132 eV. Substituting this value to find the actual optical band gap:

$$\eta \cdot (2.184 - 0.091) = 1.93 + 0.132 = 2.062eV$$

$$\Rightarrow \eta = \frac{2.062}{2.093} = 0.985$$

Thus the η factor was calculated using the reasonable assumption that the quantum dot size was 7nm. The energy level separations were then multiplied with this η factor to give the correct separations and were measured to be: $\Delta E_{s\text{-}p}$ = 99.63 meV; $\Delta E_{p\text{-}d}$ = 93.40 meV. The absence of the fourth peak negated the possibility of calculating the $\Delta E_{d\text{-}f}$ separation energy. The energy level separations in the negative bias or the valence energy levels corrected for the η factor were measured to be: ΔE_{VB1} = 37.36 meV; ΔE_{VB2} = 56.04 meV.

Figure 5.16 shows the current voltage plot for another spectroscopic measurement unit # 15 showing clear step-wise increase in current with increasing bias. In the zero-conductivity gap, the only current observed is from the leakage through the intervening dielectric between the source and the drain electrode. Depending on the batch of samples, the leakage current was measured to be between 60 pA to 180 pA at 1.3 V for open circuit measurement units. The insets show (a) the step-wise increase in current with bias in the negative bias region and (b) the step-wise increase in current in the positive bias region.

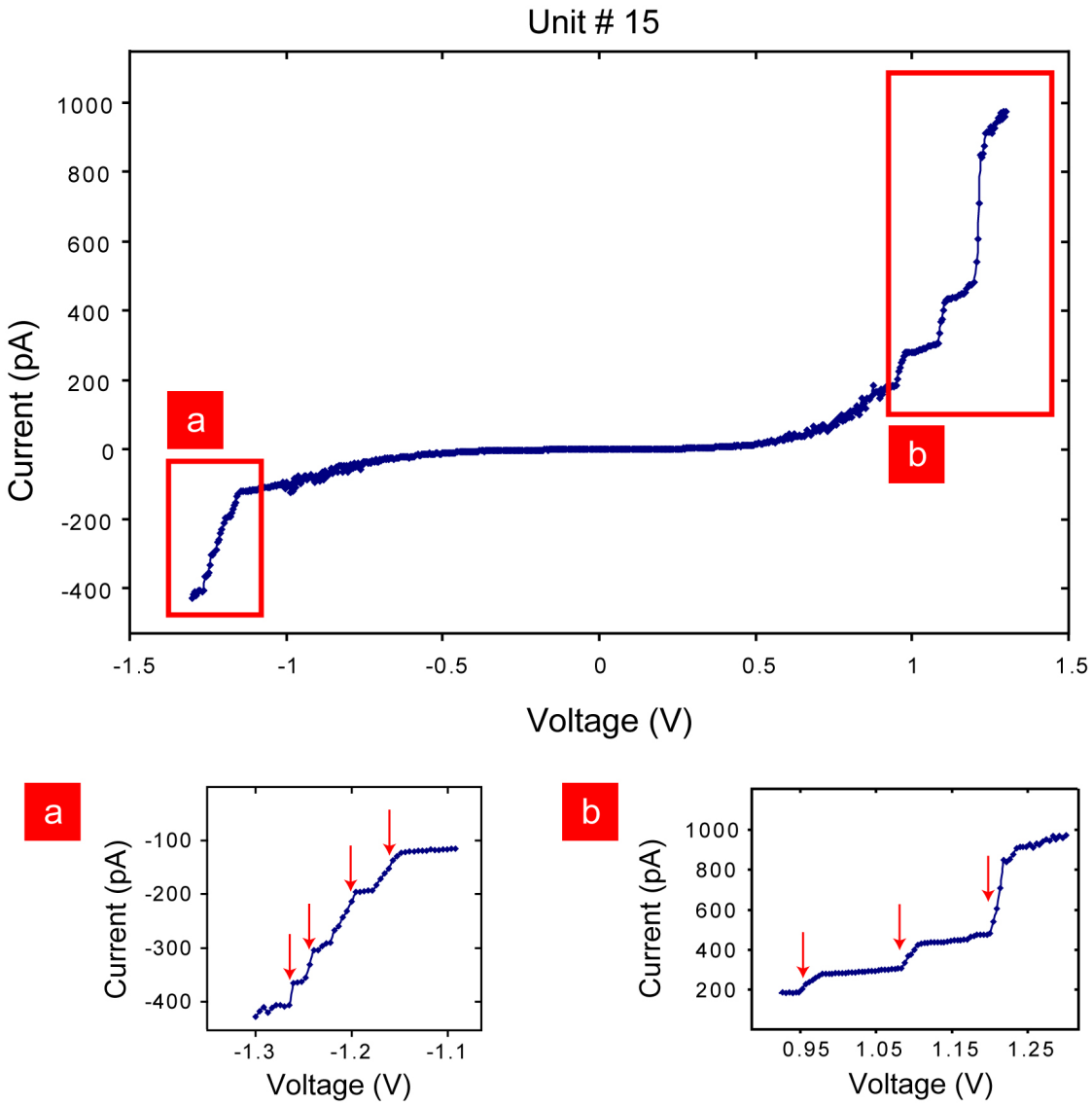


Figure 5.16: Current-voltage plot for unit # 14. Expanded view of the (a) negative bias and (b) positive bias region are shown here. Clear step-wise increase in current with increasing bias voltage is observed. Arrow positions indicate the start of step-wise increase in current.

For all direct differential conductance measurements, the settings for the are the same except that the gain values in the current pre-amplifier SR-570 to convert the current into voltage scale are based on the measurement unit resistance. In certain cases, the frequency and the band pass filter settings were changed according to the frequency in use. The settings

for all the lock-in measurements are given below and no settings are changed unless explicitly mentioned:

Table 5.3: Universal settings for differential conductance measurements using lock-in amplifier SR-830, current pre-amplifier SR-570 and scaling amplifier SIM-983 are given below in the table. Settings are same for all measurements unless explicitly noted of changes.

SR-570 Settings	SR-830 Settings	SIM-983
3-30 Hz Band Pass filter 6dB/Oct roll off	Frequency - 13 Hz	Scaling factor - 0.25
High Band width mode	Sine Amplitude - 4mV	
Sensitivity - 2nA/V	Time constant - 10s 24dB/oct roll off	
	Sensitivity - 20mV	
	Wait time/point - 70s	
	Both notch filters in line	

Figure 5.17 shows the direct measurement of the conductance peaks using the lock-in amplifier measurement technique discussed in section 5.1.2. The conductance peaks in both the positive and negative bias are clear even at room temperature. Figure 5.17 shows two such measurements done on the same measurement unit (unit # 15) and shows the reproducibility of the measurements. Before and after each measurement, 0 V was applied to the unit using the Agilent 4157B to both the source and drain electrodes to bring the quantum dot and the surrounding dielectric to the neutral state. This ensured the reproducibility of the measurements without very little offsets (<10 meV) in the voltage scale. The direct differential conductance spectra shown in this work are not normalized to the η factor as mentioned previously.

The zero conductivity gap and the energy level separations were then measured from this direct differential conductance plot. The zero conductivity energy gap or the band gap for

this unit was measured to be 2.0741 eV. The calculation of the actual band gap is done in a similar manner to the calculations described using the numerical differential conductance spectra. Using the same calculated value for the J_{e-h} as 0.132 eV, the calculations were as follows:

$$\eta \cdot 2.0741 = 1.93 + 0.132 = 2.062eV$$

$$\Rightarrow \eta = \frac{2.062}{2.0741} = 0.994$$

Thus the η factor was calculated using the same assumption that the quantum dot size was 7nm. The energy level separations were then multiplied with this η factor to give the correct separations and were measured to be: $\Delta E_{s\text{-}p}$ = 128.83 meV; $\Delta E_{p\text{-}d}$ = 120.90 meV. The absence of the fourth peak negated the possibility of calculating the $\Delta E_{d\text{-}f}$ separation energy. The energy level separations in the negative bias or the valence energy levels corrected for the η factor were measured to be: ΔE_{VB1} = 44.22 meV; ΔE_{VB2} = 57.23 meV. It should be noted again that these measurements were conducted at room temperature (295 K).

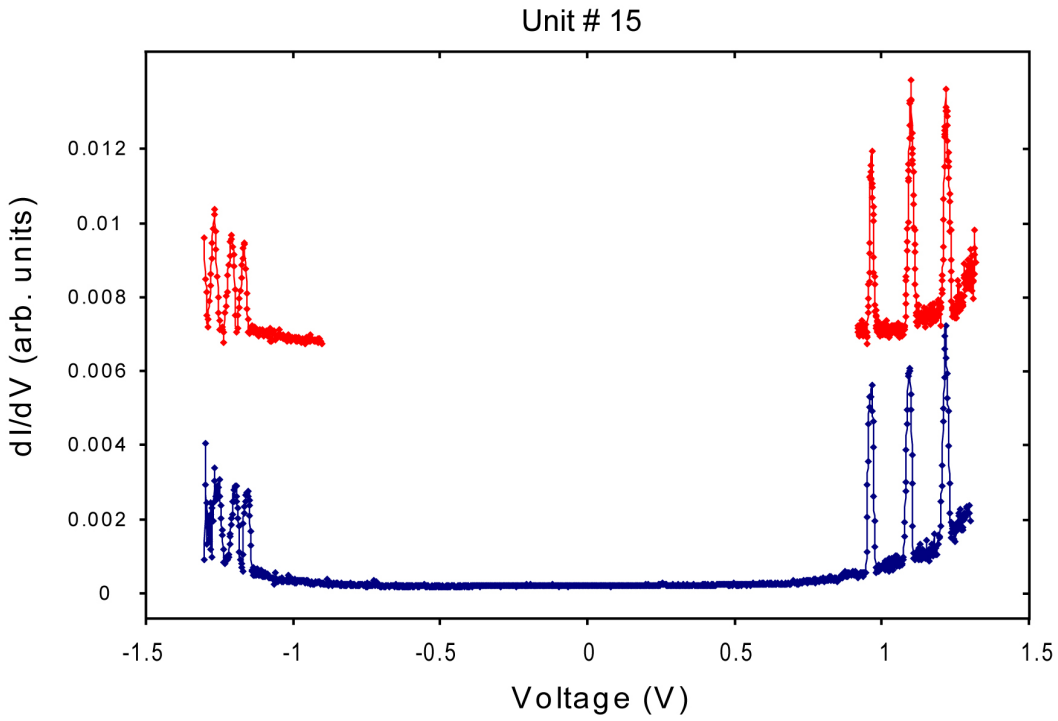


Figure 5.17: Direct differential conductance measurements for spectroscopic unit # 15 using the lock-in amplifier. The red curve is with higher number of data points than the blue curve. Both curves show peaks in positive and negative bias regions and show the repeatability of these measurements. Between any measurements, 0 V was applied for a minimum of 4 hours.

Figure 5.18 shows the direct differential conductance spectra for measurement unit #16. The sensitivity (gain) of the current pre-amplifier SR-570 was set to 5nA/V. All the remaining settings were the same as listed in table 5.3. The arrows indicate the positions of the peaks corresponding to the s, p and d orbitals positions. Due to the nature of the junctions in this unit, the peaks in the negative bias or the valence orbitals were missing or convoluted due to smaller energy level separations. To resolve the energy level spacings in the negative bias, measurements were conducted at lower temperature up to 77 K using liquid nitrogen open cycle system in the ST-500 variable temperature probe station. By measuring at the low temperatures, only the background due to leakage currents was also found to be diminished as a the temperature was lowered to 77 K, but the peak heights were the same in all temperature ranges for the same settings.

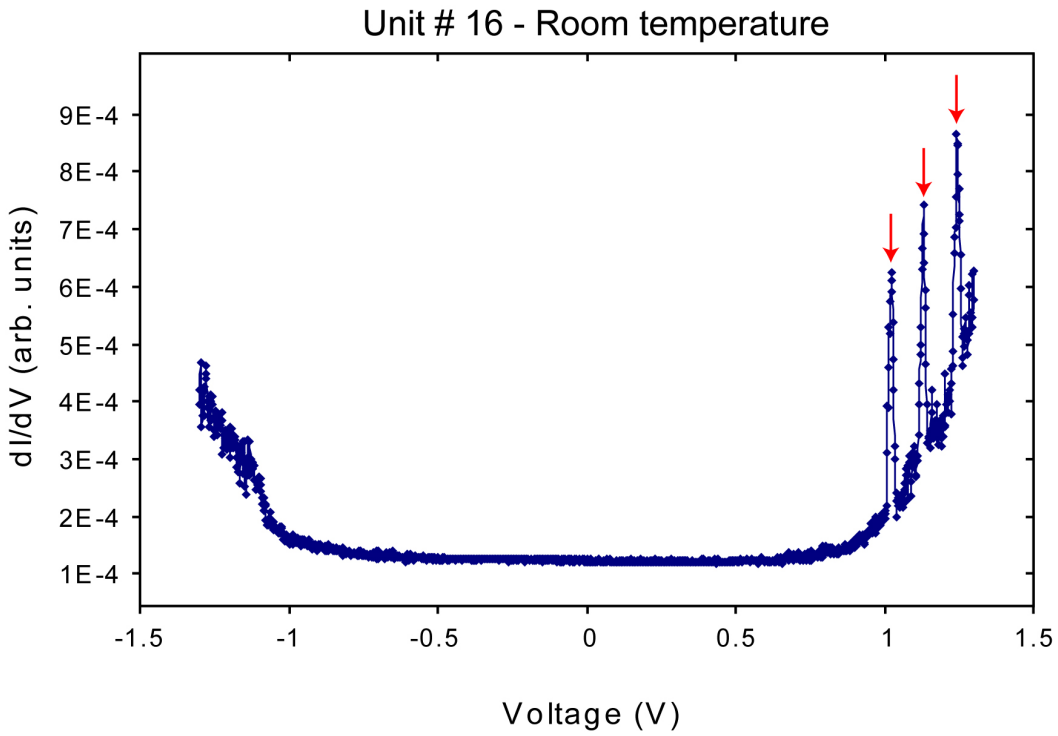


Figure 5.18: Room temperature differential conductance spectra for spectroscopic measurement unit # 16. Arrows indicate peaks in the positive bias corresponding to shell-tunneling through the conduction orbitals.

Figure 5.19 shows the direct differential conductance spectra for unit # 16 taken at 77 K. To reduce the noise levels and increase the peak heights, the settings for the measurements were optimized to obtain the plot shown in figure 5.19. The settings for this measurement in the negative bias are given in table 5.4. Although these settings were not the completely optimized settings, clear conductance peaks are still visible in the negative bias region indicating resonant transport through the valence energy levels. In the positive bias region, three peaks were again clearly visible as in the case of the room temperature measurements indicating the resonant tunneling through the s, p and d energy levels in the conduction orbitals. Successive measurements after holding the measurement units at 0 V were repeatable with only a few meV offset in the voltage scale as observed in other measurement units. The tunneling currents were found to be unstable after ±1.3 V, as well as, there was a risk of the measurement unit shorting

due to the breakdown of the intervening dielectric between the source and the drain electrodes. Hence, measurements were always stopped at or below ±1.3 V. Using these measurements, the band gap and the energy level separations were then calculated as detailed above. The zero-conductivity gap was measured to be 2.0714 eV, after correcting for the electron-hole interaction energy and the optical band gap, the η factor was calculated to be η = 0.995. Based on this η factor, the energy level separations were corrected and measured to be: $\Delta E_{s\text{-}p}$ = 102.44 meV; $\Delta E_{p\text{-}d}$ = 108.75 meV. The corrected valence orbitals energy level separations were measured to be: ΔE_{VB1} = 24.76 meV; ΔE_{VB2} = 34.95 meV. The absence of good peaks in the room temperature measurements in the valence orbitals can be due to these small energy level separations in the order of k_BT (26 meV @ 295 K) which can be convoluted in the conductance spectra. In the current-voltage measurements for other spectroscopic measurement units, energy level separations of up to a minimum of 50 meV were resolvable even at room temperature (~2 times k_BT) which will be detailed later in this section.

Table 5.4: Settings for direct differential conductance measurements in the negative bias region for spectroscopic measurement unit # 16.

SR-570 Settings	SR-830 Settings	SIM-983
0.3 - 30 Hz Band Pass filter 6dB/Oct roll off	Frequency - 7 Hz	Scaling factor - 0.25
High Band width mode	Sine Amplitude - 4mV	
Sensitivity - 2nA/V	Time constant - 10s 24dB/oct roll off	
	Sensitivity - 10mV	
	Wait time/point - 70s	
	Both notch filters in line	

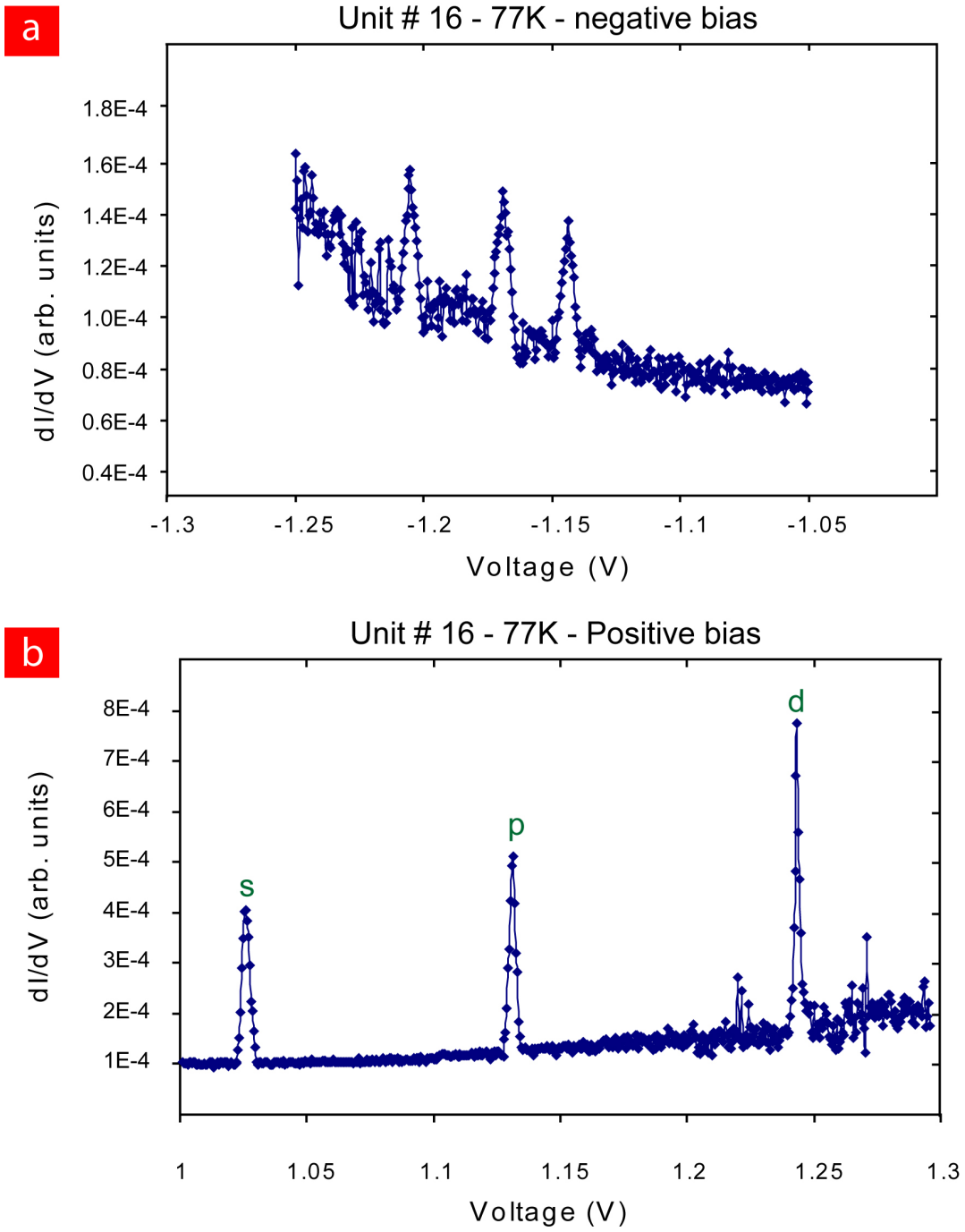


Figure 5.19: Direct differential conductance measurements for unit # 16 at 77K measured in the ST-500 variable temperature probe station. (a) Peaks in the valence orbitals that were not observed at room temperature measurements. (b) Peaks in the conduction orbitals labeled as s, p and d energy levels.

After the low temperature measurements at 77K revealed the energy structure in the negative bias region, the dependence of the peak width on temperature was studied. In order to accomplish this, measurements were done at various temperatures (77 K, 150 K, 225 K, and 295 K) and the peak widths determined. Figure 5.20 shows measurements done at the temperatures listed before for unit # 16 only in the positive bias region. Similar to other measurements, before and after each measurement, 0 V was applied for a minimum of 4 hours using the Agilent 4157B parameter analyzer to bring the quantum dot back to the neutral state. Clear dependence on temperature is visible from the measured conductance spectra as seen in figure 5.20. As the temperature is lowered, the peak width also decreases.

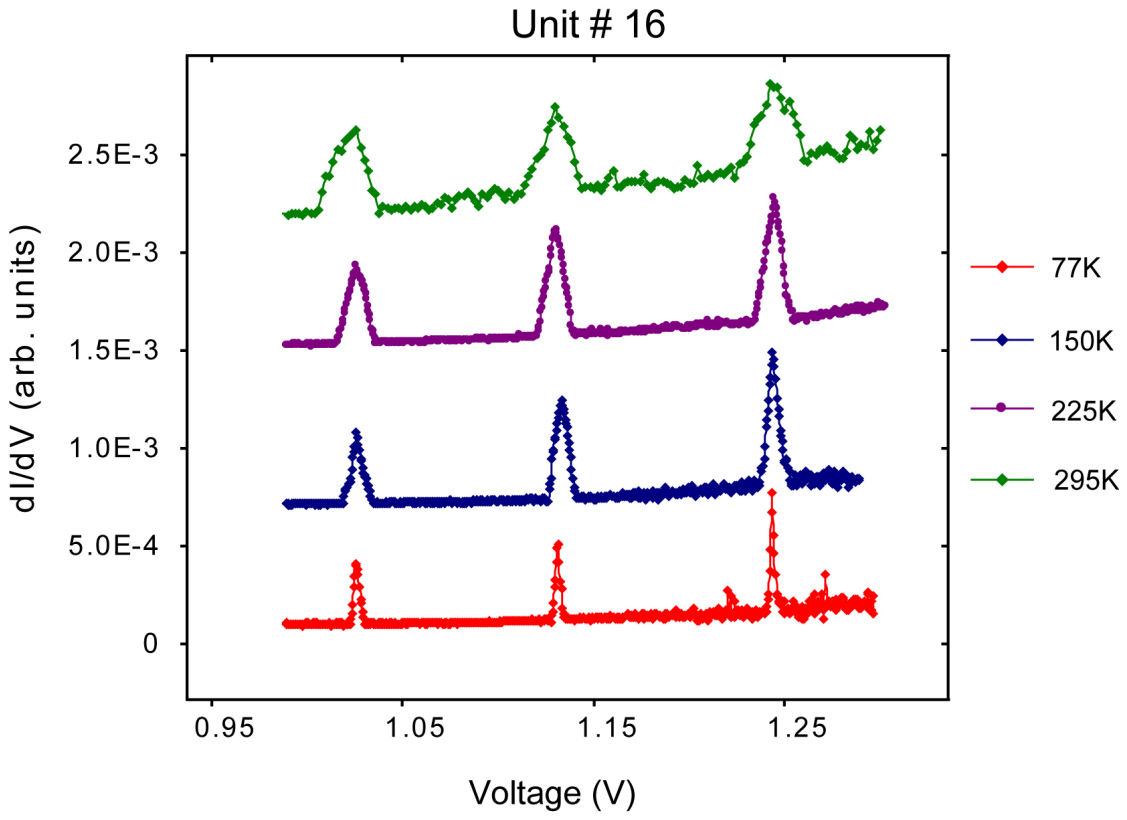


Figure 5.20: Temperature dependence on the direct differential conductance peak widths for measurement unit # 16. Measurements were completed at 77 K, 150 K, 225 K, and 295 K. Each different measurement at specific temperature starting from 225 K to 77 K is offset in the y-axis for clarity.

Jdira et al [5.19] have shown for CdSe quantum dots of diameter 2.6nm, 3nm, 5nm and 6.1nm that the peak width is dependant on temperatures. Apart from temperature dependence, the peak widths from the STM spectroscopy were also found to be much larger than some factor of thermal energies at the measurement temperatures. They show that the peak widths also enlarged due to electron-phonon coupling which then broadens the conductance peaks. This electron-phonon coupling maybe intrinsic to the STM spectroscopic technique as it has also been observed for other nanocrystals [5.19 – 5.23] and even in single-molecule spectroscopy [5.24] using STM spectroscopy. The peaks were fit to a Gaussian curve and the full width half maximum (FWHM) measured from the fit. The peak width (FWHM) at room temperature from their study for quantum dot size of 6.1nm was measured to be up to ~180 meV and at cryogenic temperatures of 4.8 K to be ~65 meV. The broadening of the peaks is shown in figure 5.21. The temperature dependence is given by the slope of the FWHM of the peaks at various temperatures and determined to be 0.37meV/K. The FWHM was determined to be independent of the current set points (which determine the η factor) in the STM spectroscopy after the substituting the η factor corrections. The temperature effect of peak broadening for CdSe quantum dots of mean diameter 6.1nm for the first peak (S_e) in the positive bias is shown in figure 5.22.

The peak width was determined to depend on the size of the quantum dot [5.25]. Slight asymmetry of the first peak for larger quantum dot sizes was also found [5.25]. The FWHM of the first peak for quantum dot sizes of 3nm and 5nm was determined to be 151 meV and 96 meV at 4.5K. Figure 5.21 (taken from Jdira et al [5.25]) shows the peak broadening effect observed in STM spectroscopy for 6.1nm CdSe quantum dots. The red dotted lines are the peaks for ~7nm CdSe from this study at (a) 77K and (b) at room temperature. The peak widths even at room temperature from this study are narrower than the STM data even at 4.5K. The peaks at 77K in this study resemble a delta function. The peaks were offset in the x-axis to match with the peaks from the STM study.

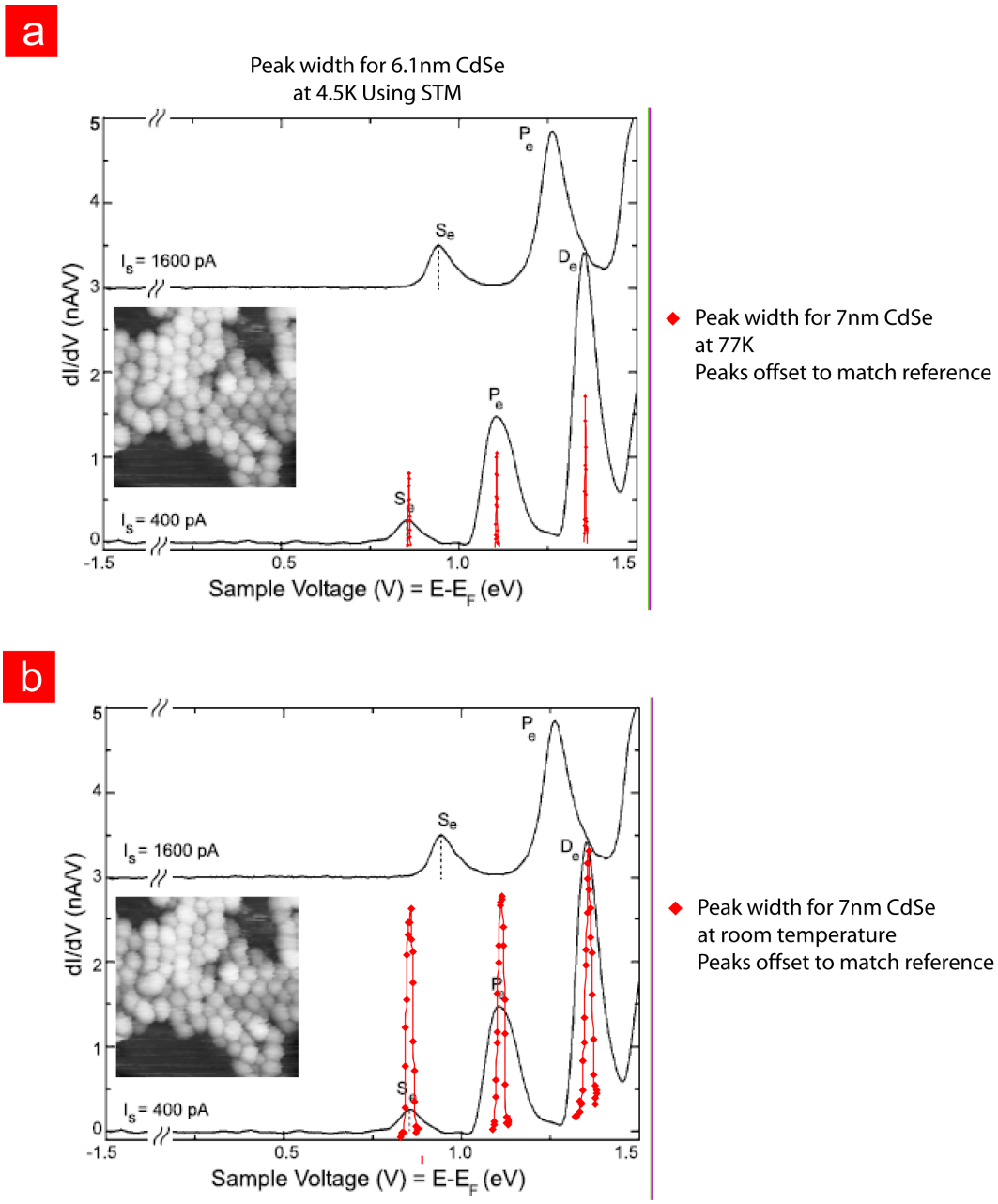


Figure 5.21: Figure taken from Jdira et al [5.25]. Differential conductance spectra for isolated CdSe QDs in the shell-tunneling regime for 6.1 nm at 4.5K. The red dotted lines in (a) at 77K, and (b) at room temperature, from this study. The peaks from this study are overlapped on the STM data by adding an offset to coincide the peaks. Even the peak width at room temperature from this study is much smaller than the STM data at 4.5K. At 77K, the peaks become almost a delta function.

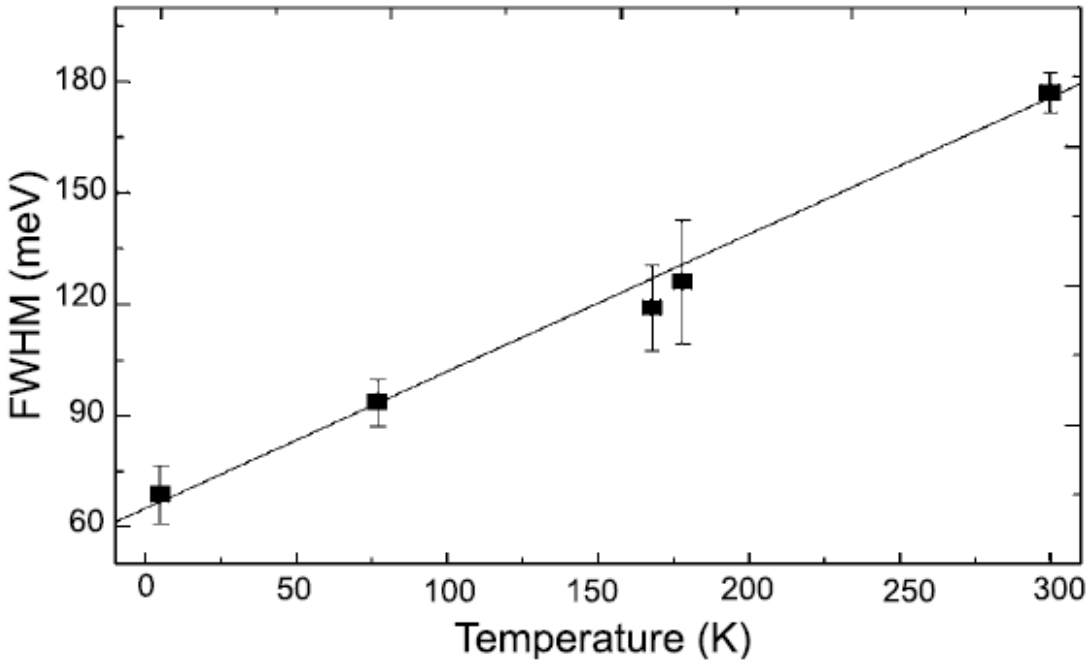


Figure 5.22: Taken from [5.25]. FWHM of the S_e peak, which is measured on CdSe dots, with a TEM determined core size of 6.1 nm, as a function of temperature. The dots belong to array assembled on the gold and HOPG surfaces. The FWHM is normalized by the ratio between the theoretical (from [5.26]) and measured S_e-P_e peak separation. Line: fit showing that the FWHM linearly varies with a slope of 0.37meV/K.

To compare the peak broadening effect from Jdira et al [5.25] to the one from this study, all the peaks from figure 5.20 were fit to a Gaussian distribution and the FWHM analyzed. The fitting of the curve was done using the Gaussian distribution function:

$$f(x) = B + A \cdot \exp\left(\frac{-(x-\mu)^2}{2\sigma^2}\right)$$

The fit parameters included the background (B), position of the peak (μ), height of the peak (A) and the standard deviation (σ). The error factor (ε_{err}) was given by the square root of the actual differential conductance values. The residual (ε_{res}) was then computed as the difference between the Gaussian fit and the actual data points. A function ζ was defined such that $\zeta^2 = \frac{\varepsilon_{res}^2}{\varepsilon_{err}^2}$. To optimize the fit of this Gaussian curve, the sum of all ζ^2, $\sum \zeta^2$ had to be

minimized. This was done manually to best fit the Gaussian curve to the measured data points by adjusting the standard deviation (σ) to better fit the expanse of the curve, adjusting peak height (A) and peak position (μ). Figures 5.23 to 5.25 show the Gaussian fits for the s_e, p_e and d_e peaks for 77K, 150K, 225K and 295K respectively.

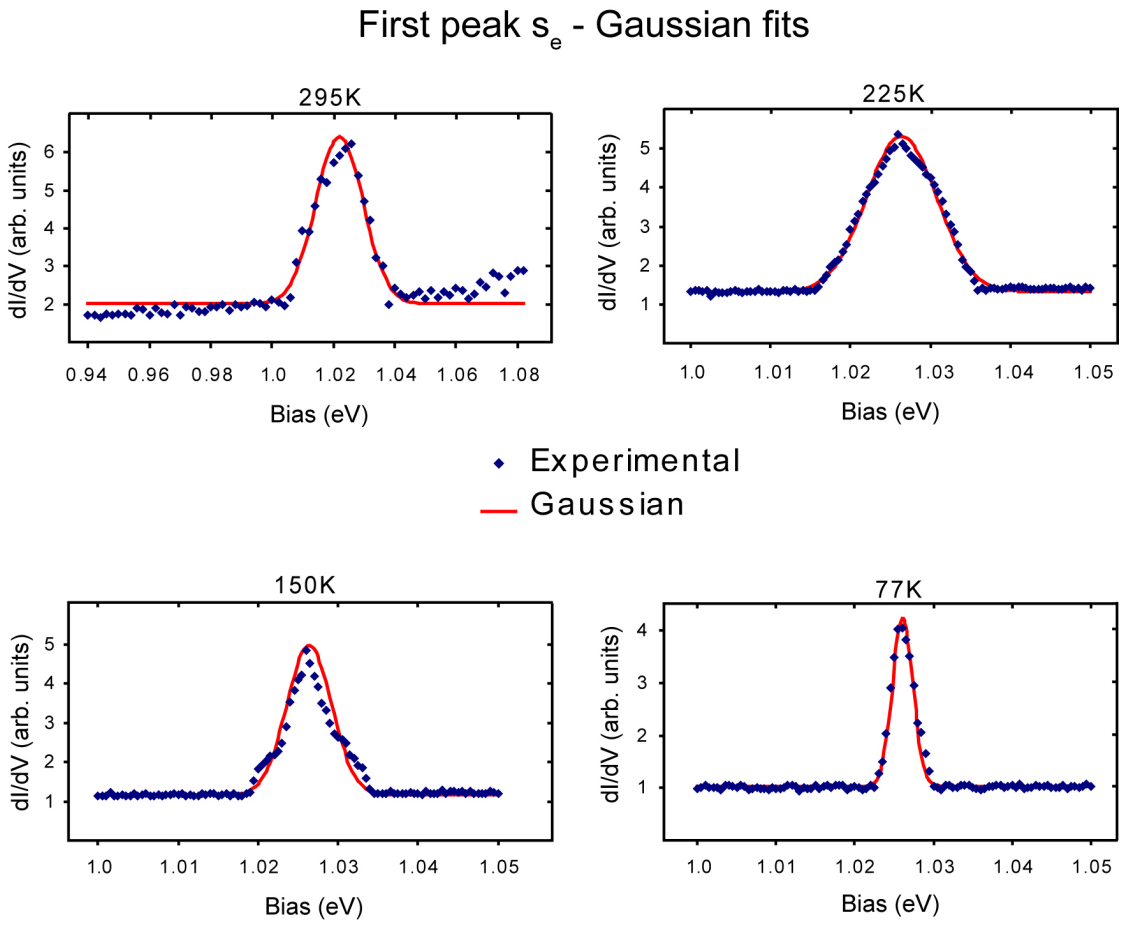


Figure 5.23: First peak in the conduction orbital s_e fit to Gaussian curves for measurements conducted at 77K, 150K, 225K and 295K.

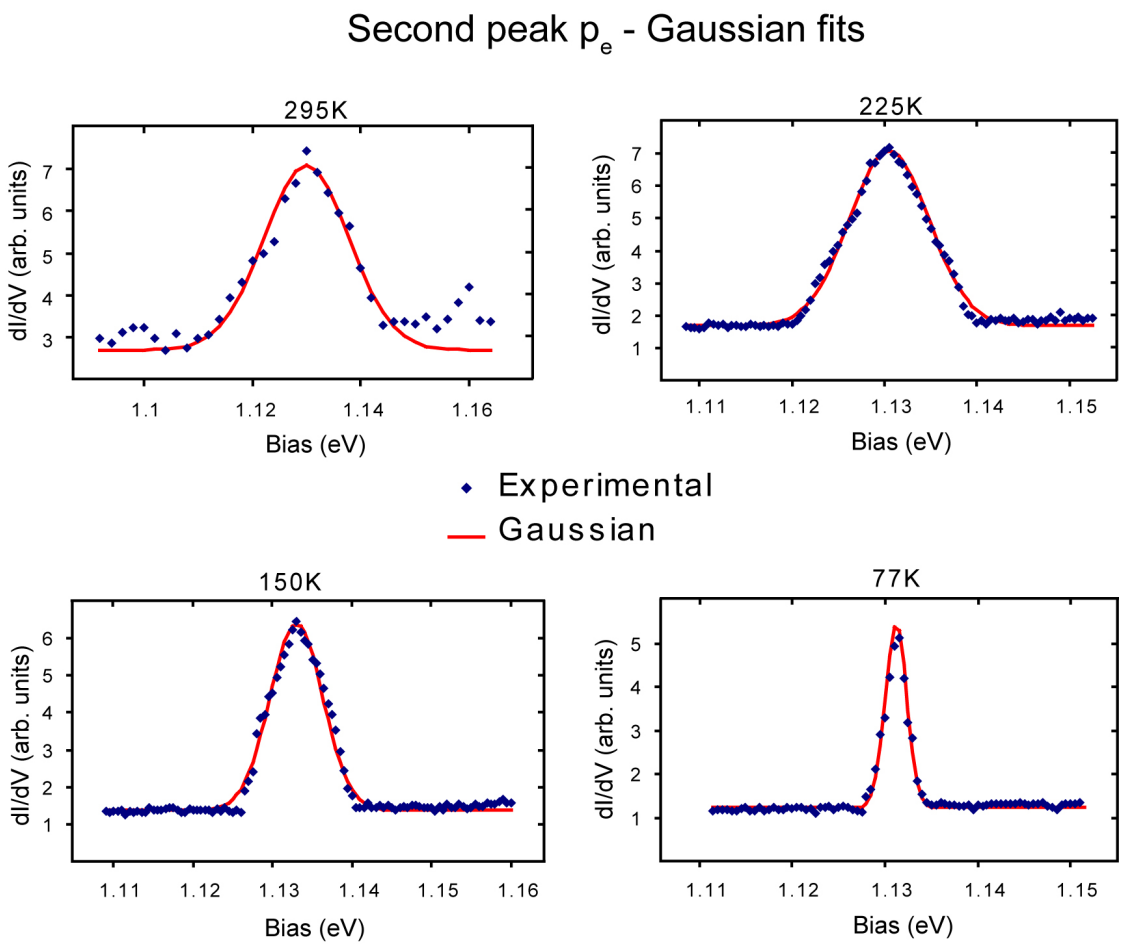


Figure 5.24: Second peak in the conduction orbital p_e fit to Gaussian curves for measurements conducted at 77K, 150K, 225K and 295K.

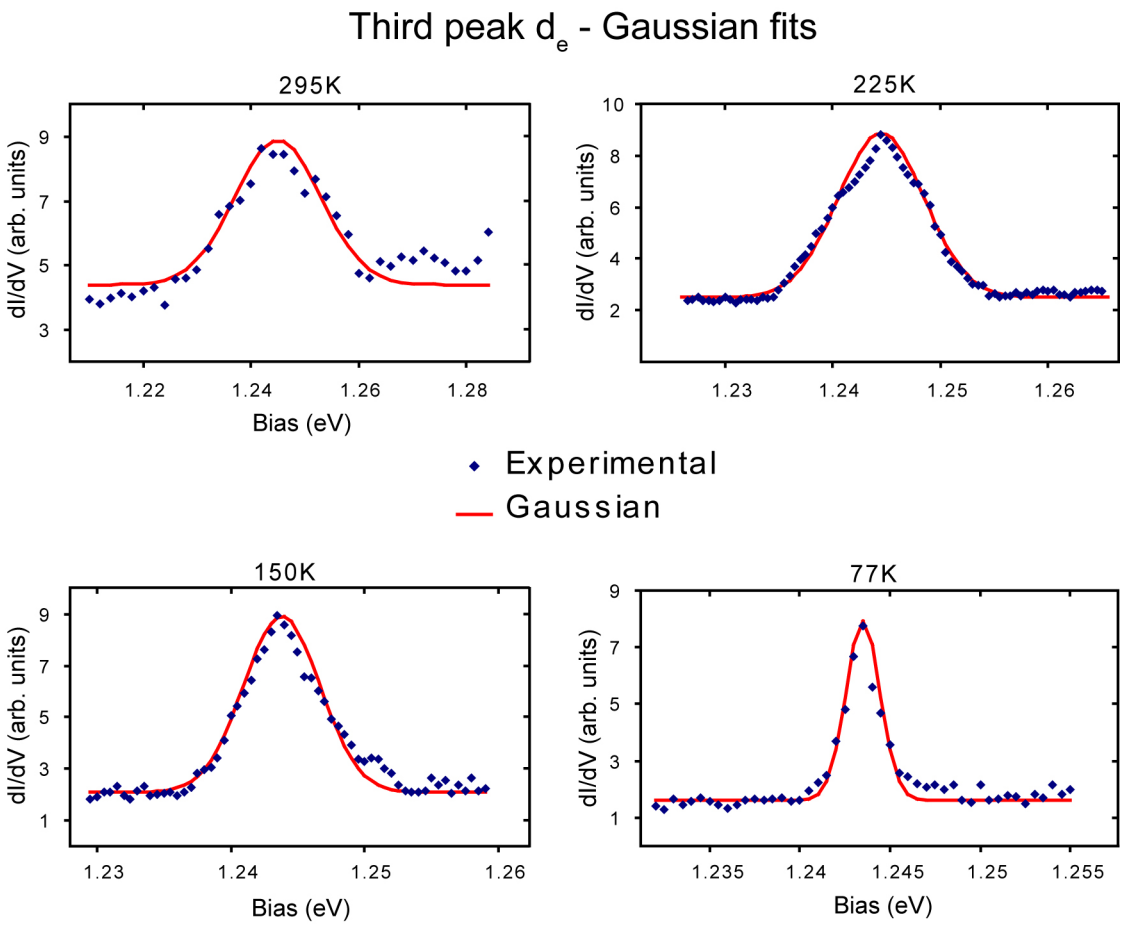


Figure 5.25: Third peak in the conduction orbital d_e fit to Gaussian curves for measurements conducted at 77K, 150K, 225K and 295K.

The leakage at room temperature was measured to be the maximum leakage current in the figures 5.23 to 5.25, hence the slope of the measured differential conductance background at room temperature. As the temperature was lowered, the leakage was found to be minimum and no slope observed in the lower temperature differential conductance measurements. The peaks were able to be fitted with the Gaussian distribution and the parameters were optimized for an excellent fit. The FWHM was calculated from this plot using the formula $FWHM \approx 2.3548 \cdot \sigma$. The average peak separations were then calculated and then corrected for the η factor, η = 0.995. Table 5.5 shows the FWHM for all three peaks in the conduction orbitals as a function of temperature and the average values at 295K, 225K, 150K

and 77K, and the η factor corrected values for these averages. Table 5.6 shows peaks width at the base of the peak. Table 5.7 shows the comparison between the thermal energy $k_B T; k_B = 8.617 * 10^{-5} eV / K$, and the corrected FWHM and peak width at base of the each peak at 295K, 225K, 150K and 77K.

Table 5.5: The FWHM for all three peaks in the conduction orbitals as a function of temperature and the average values at specific temperature and the η factor corrected values.

FWHM Data	295 K	225 K	150 K	77 K
s peak (meV)	18.13	10.36	6.59	3.08
p peak (meV)	18.13	10.13	7.91	2.73
d peak (meV)	18.84	9.42	6.73	2.24
Average (meV)	18.37	9.97	7.08	2.68
Average * η (meV)	18.28	9.92	7.04	2.67

Table 5.6: Peak width at the base of the peak various temperatures and η factor corrected values.

Width at peak base (meV)	295 K	225 K	150 K	77 K
s peak (meV)	34	20.5	15.5	8
p peak (meV)	32	20	14.5	7
d peak (meV)	32	20	15.5	6.5
Average (meV)	32.67	20.17	15.17	7.17
Average * η (meV)	32.50	20.07	15.09	7.13

Table 5.7: Comparison of FWHM, peak width at base of peak and thermal energy at 295K, 225K, 150K and 77K all corrected for η factor.

Temperature (K)	Thermal Energy (meV)	FWHM (meV)	Width at peak base (meV)
77	6.64	2.53	6.75
150	12.93	6.67	14.29
225	19.39	9.39	19.00
295	25.42	17.30	30.77

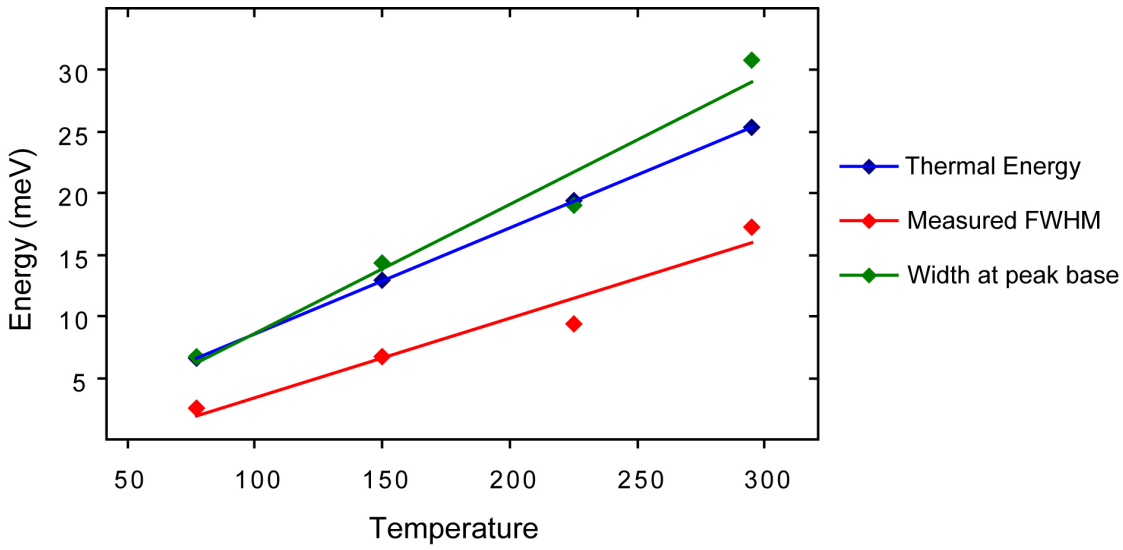


Figure 5.26: Temperature dependence on FWHM of each peak and peak width at the base compared to thermal energy at 295K, 225K, 150K and 77K all corrected for η factor. Dots are actual data points and the lines are linear fits to these measured data points.

From tables 5.5-5.7 and figure 5.26, it is very clear that in this study, the peak widths, be it based on the FWHM or at the base of the peaks, it is linearly dependant on temperature as was observed by Jdira et al [5.25]. The absence of peak broadening due to electron-phonon coupling is also observed in this study. The structure of the spectroscopic measurement unit as well as the electrode material (Chromium) may have the most deciding factor in observing only

the temperature dependence of the peak widths and not the electron-phonon coupling. Similar findings of room-temperature operable single-electron transistors were demonstrated by Vishva et al [5.27] with the same vertical electrode structure using 10nm gold nanoparticles. The electronic density of states of the Chromium electrodes may be a reason for this observation of Coulomb staircase at room temperature.

Figure 5.27 shows the current-voltage and numerically acquired differential conductance spectra for measurement unit # 13. As with other measured spectroscopic units, clear staircase like current increase with increase in voltage was observed in this unit as well indicating transport only through single quantum dot. The measured band gap is 1.89 eV, and hence, it is clear that the quantum dot size is larger than 7nm. Not knowing exactly what the size of quantum dot under study, it is not possible to calculate the η factor for this particular case. From spectroscopic measurement units 12, 15 and 16, the η factor was very close to $\eta \approx 0.99$ in each of those cases. Assuming the same η factor, then the η corrected band gap would then be 1.87eV. The energy level separations can then be calculated similar to the other quantum dot measurement units. The calculated energy level separation values for unit # 13 after the η factor corrections were as follows: $\Delta E_{s\text{-}p}$ = 111.74 meV; $\Delta E_{p\text{-}d}$ = 100.88 meV, $\Delta E_{d\text{-}f}$ = 100.88 meV. The corrected valence orbitals energy level separations were measured to be: ΔE_{VB1} = 60.53 meV, ΔE_{VB2} = 60.53 meV.

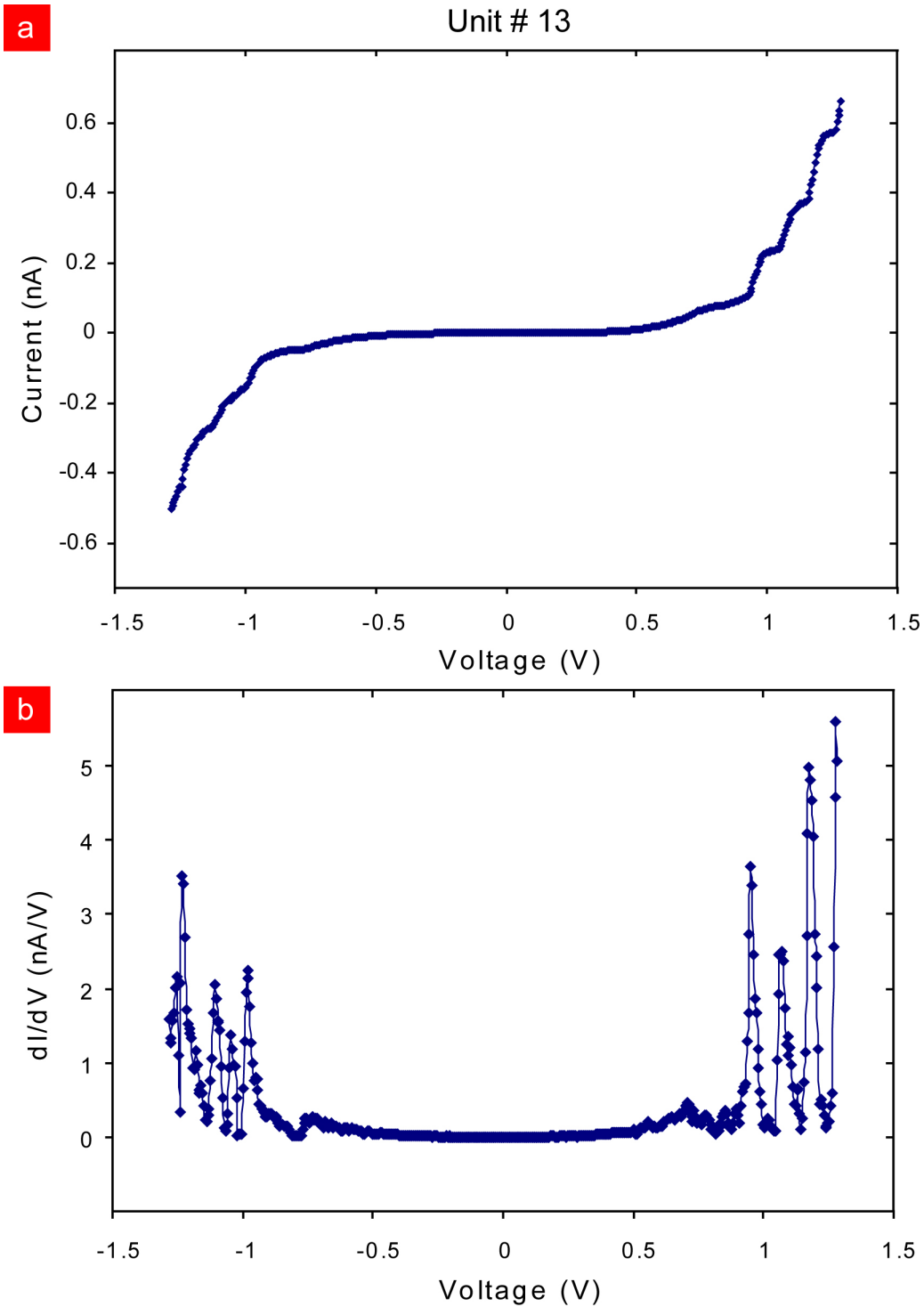


Figure 5.27: (a) Current-voltage and (b) differential conductance plots for spectroscopic measurement unit # 13.

The spectroscopic measurement units numbers 12, 13, 15 and 16 shown above were all fabricated with different sidewall etching recipe compared to the other measurement units that will be shown henceforth. The recipe was changed due to changing etching chamber conditions resulting from other materials being etched in the etching chamber. The vertical sidewall etching recipe (recipe-B) for the above mentioned units (12, 13, 15 and 16) was as follows:

(1) CF_4 flow rate – 50 sccm

(2) Process pressure – 50 mTorr

(3) Top electrode power – 3000 W

(4) Bottom electrode power – 100 W

(5) Process time – 150 seconds

The vertical sidewall etching recipe (recipe-A) for the measurement units shown from this point onwards is as follows:

(1) CF_4 flow rate – 50 sccm

(2) Process pressure – 25 mTorr

(3) Top electrode power – 3000 W

(4) Bottom electrode power – 50 W

(5) Process time – 120 seconds

The changed recipe (recipe-B) yielded a deeper sidewall with more bottom Chromium etching due to higher bottom electrode power and also longer etching times. This changed the dynamics of the tunneling junctions when the quantum dots were placed. Figure 5.28 shows the differences in sidewall profile due to the different etching recipes employed. As seen from this figure, the junction capacitance for recipe-A at the source-quantum dot junction will be much different than the junction capacitance at the source-quantum dot junction using recipe-B. As will be shown below, recipe-B yielded much clearer peaks both the positive and negative bias

regions where as recipe-A yielded only clear peaks in the positive bias region. No discernable peaks were seen in the negative bias region using recipe-A.

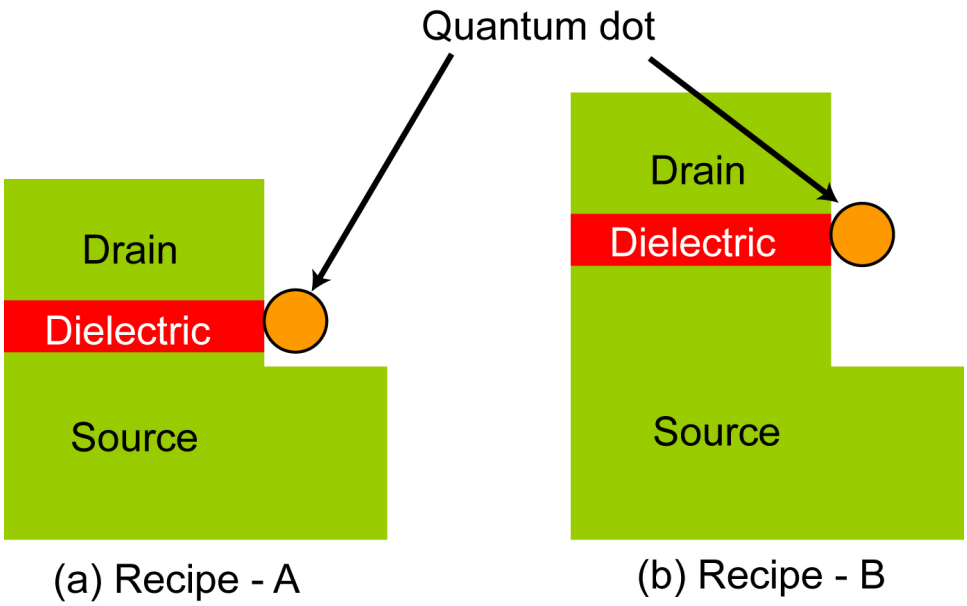


Figure 5.28: Vertical sidewall structures due to different etching recipes.
(a) Recipe-A with shallower sidewall depth, and (b) Recipe-B with deeper sidewall depth.

Figures 5.29 to 5.34 show the current-voltage and numerically calculated differential conductance plots for spectroscopic measurement units 1, 3, 4, 5, 6, and 11. These measurements were completed before the equipment for the direct measurement of differential conductance using the lock-in amplifier SR-830 was setup. Even though these units show clear step-like increase in the current with increasing voltage in the positive bias, due to noise in the measurements and also due to the nature of the tunneling junctions (sidewall etching recipe-A), clear peaks in the negative bias region could not be observed. Hence, these units were not utilized in any calculations. This also shows that the lock-in measurements can eliminate any noise either intrinsic to the measurement unit or extrinsic and yield good measurements. Unless measurements like unit 12 were obtained using simple current-voltage measurements, analysis

is easiest with data obtained using the lock-in direct measurement of differential conductance as the band gap and peak to peak separations are clearest using the lock-in method.

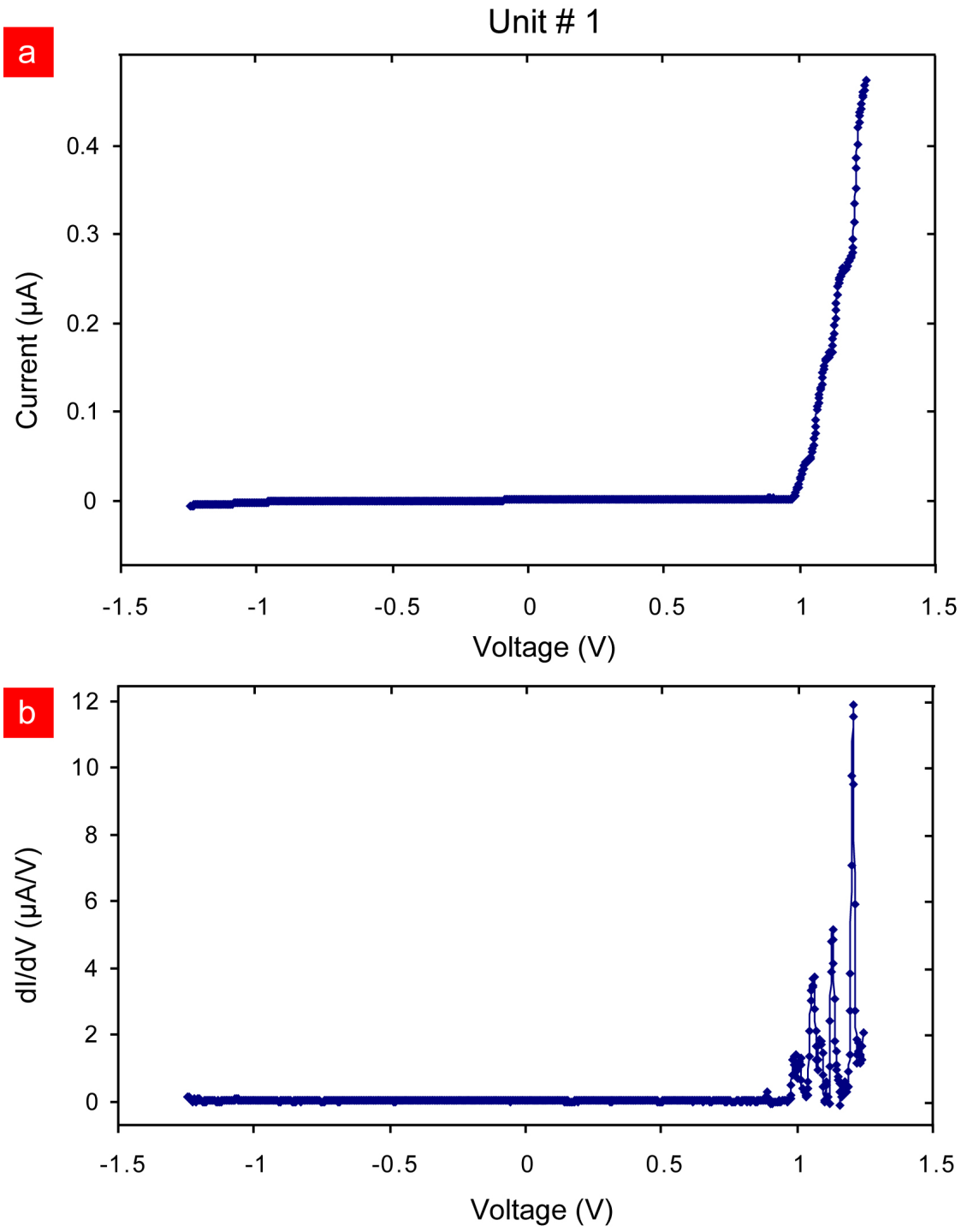


Figure 5.29: (a) Current-voltage and (b) differential conductance plots for spectroscopic measurement unit # 1.

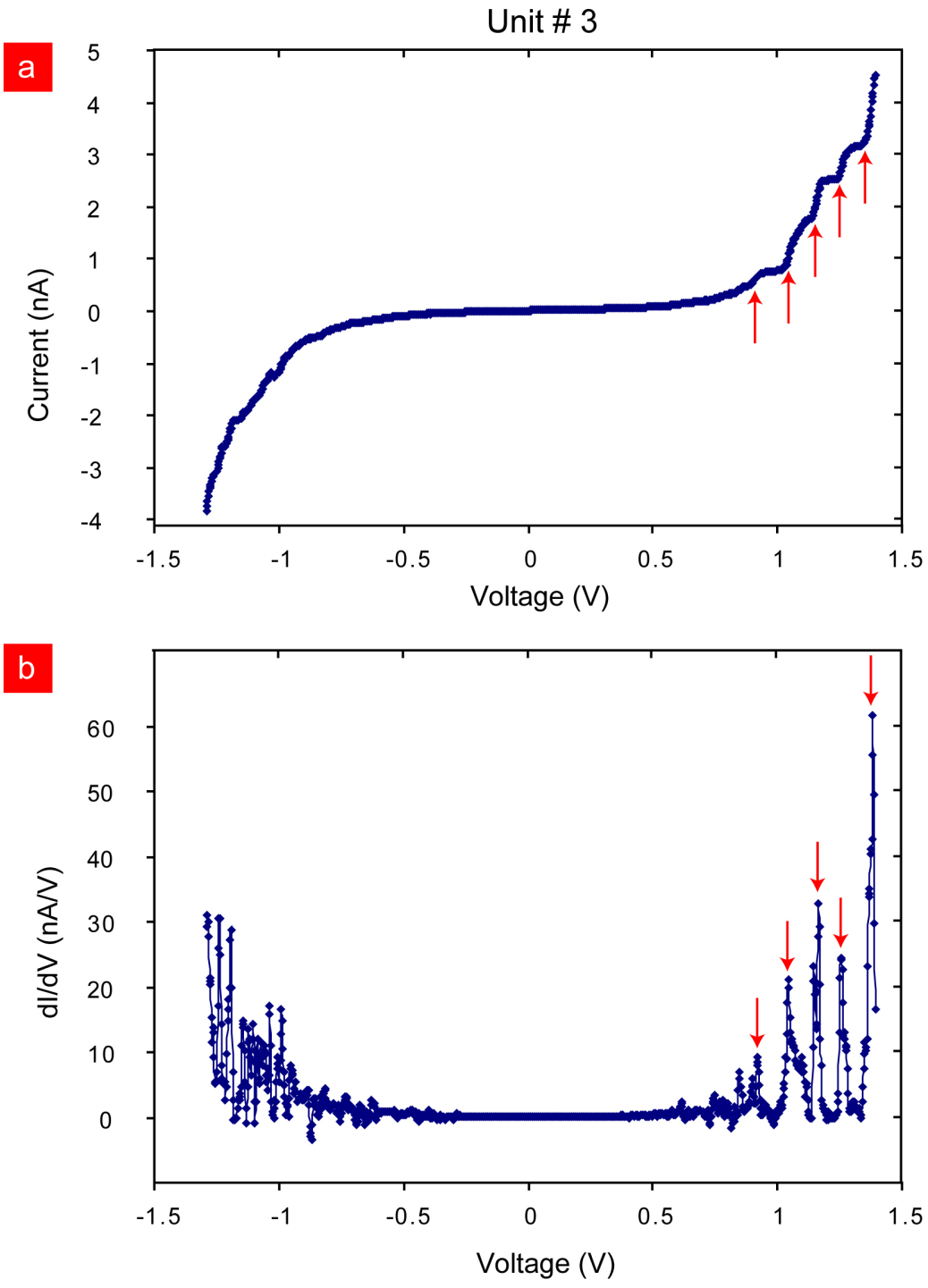


Figure 5.30: (a) Current-voltage and (b) differential conductance plots for spectroscopic measurement unit # 3.

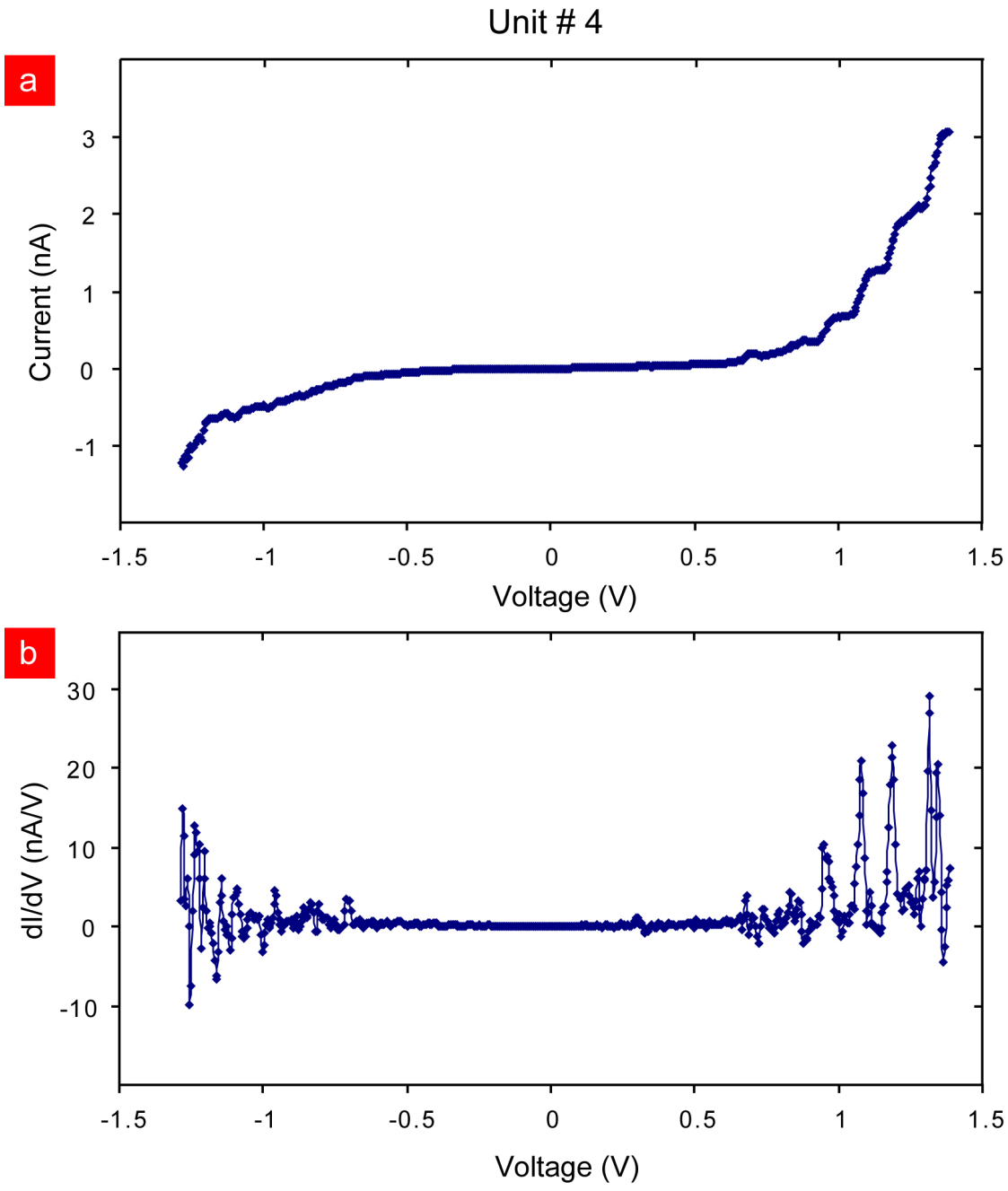


Figure 5.31: (a) Current-voltage and (b) differential conductance plots for spectroscopic measurement unit # 4.

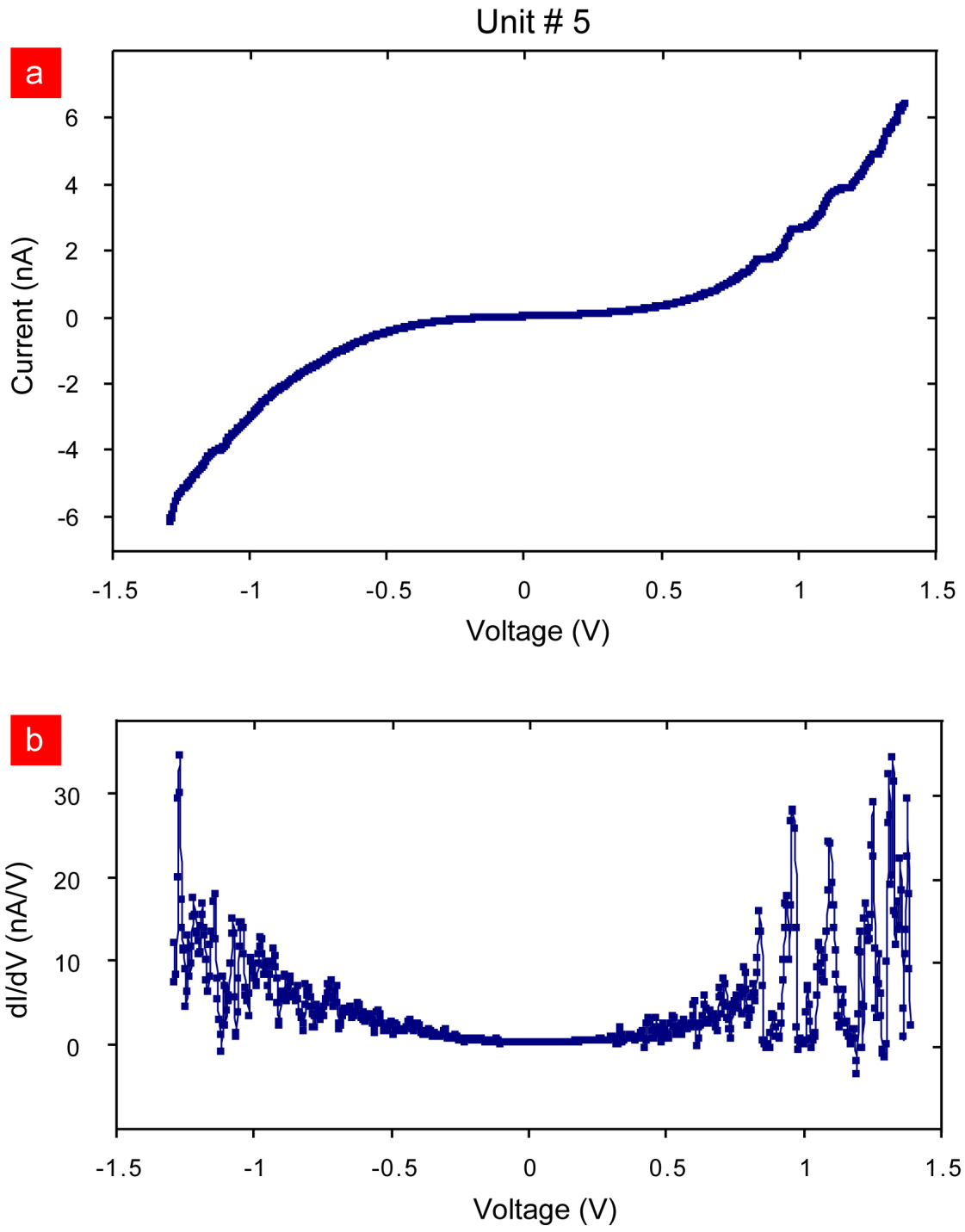


Figure 5.32: (a) Current-voltage and (b) differential conductance plots for spectroscopic measurement unit # 5.

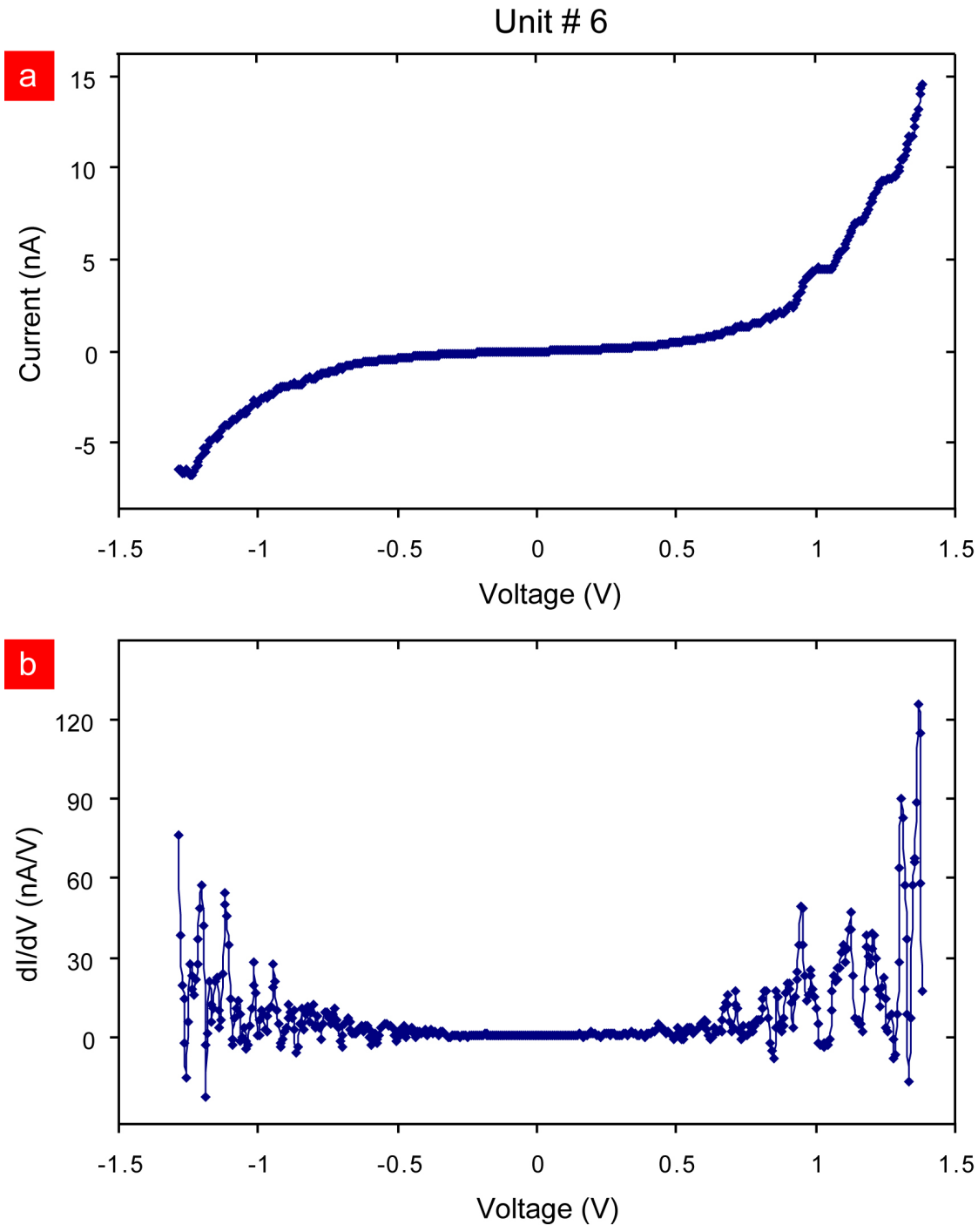


Figure 5.33: (a) Current-voltage and (b) differential conductance plots for spectroscopic measurement unit # 6.

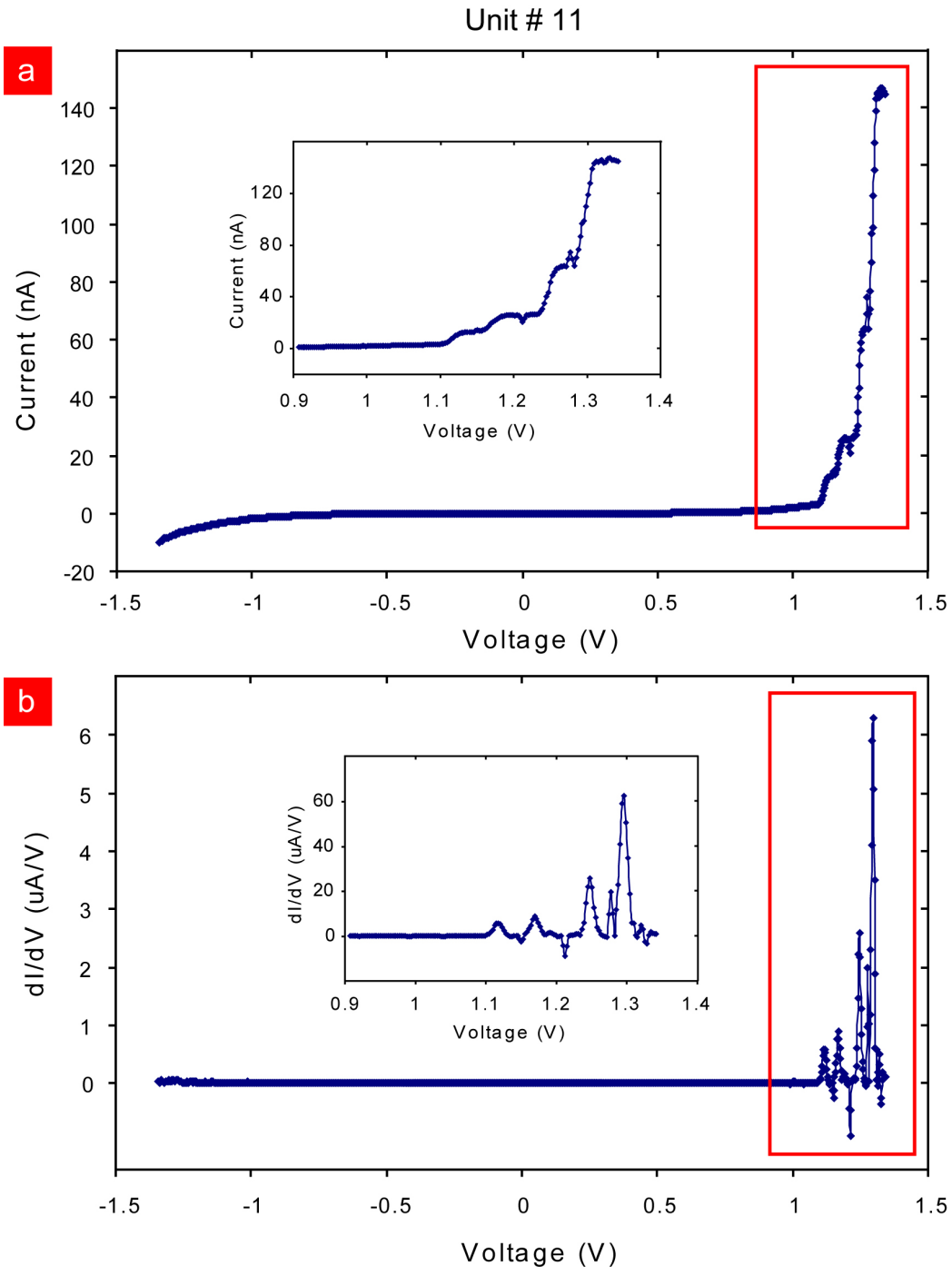


Figure 5.34: (a) Current-voltage and (b) differential conductance plots for spectroscopic measurement unit # 11. Insets show the exploded view of the staircase-like current increase and corresponding peaks in the conductance spectra.

5.3 Yield of the spectroscopic measurement units

Out of 120 spectroscopic measurement units fabricated, only about 4 showed current, others were all open circuit with only some leakage current as shown in figure 5.35. Out of the 4 units that showed some tunneling current, only one had the correct junction parameters to show clear staircase like increase in current with increasing voltage. The other three units may possibly have more than one quantum dot taking part in the tunneling process or the junction parameters were not suitable to show resonant tunneling through the single quantum dot. The final yield was close to one good measurement unit per every 120 measurement units fabricated ~0.83.

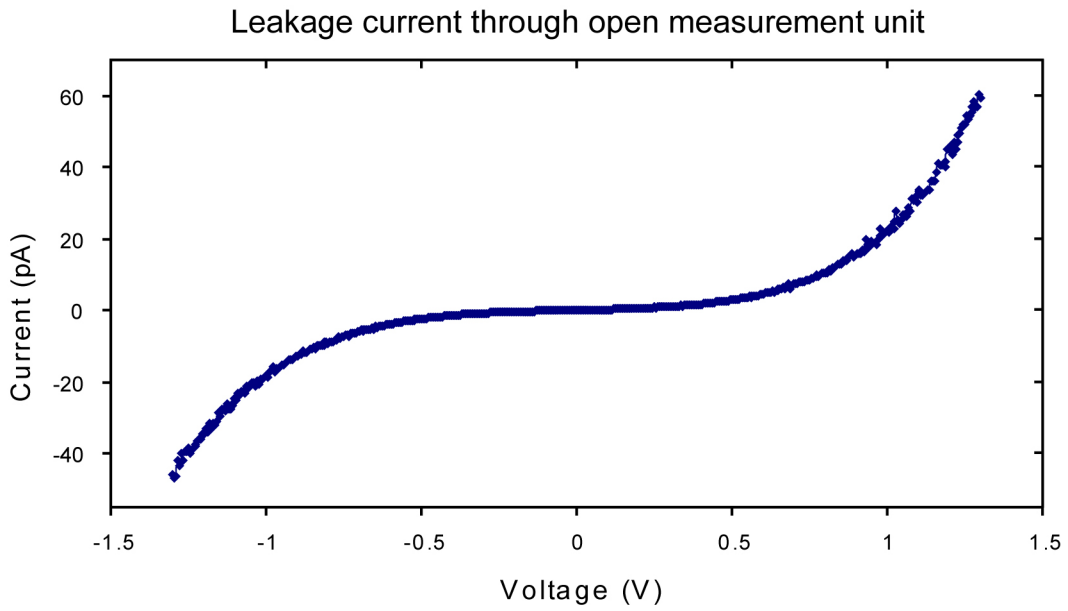


Figure 5.35: Leakage current through open-circuit spectroscopic measurement unit. Maximum leakage current of 150pA/1.3V has been measured in some batches. Average leakage current is ~60pA/1.3V.

The yield through the current fabrication process was determined to be very low (~0.08%). However, a technique to possibly increase the yield of these measurement units has

been developed. The main criteria for such a technique to be employed into the existing fabrication process are detailed below:

1. Large-scale assembly process: This process should be able to assemble individual nanoparticles/quantum dots onto exact substrate locations preferably up to wafer scale. This will enable the fabrication of a large number of these '*working*' spectroscopic measurement units using the same parallel processing techniques.
2. CMOS compatibility: As all the existing fabrication processes are CMOS compatible, it is highly desirable to have the particle placement technique also CMOS compatible. This will ensure the parallel fabrication of a large number of these spectroscopic measurement units in one single parallel batch process.
3. Precision of placement: The quantum dots need to be placed exactly on to the intervening dielectric layer between the source and the drain electrodes. The thickness of this dielectric layer is only a few nanometers (~7nm). Hence, the placement technique should be able to effectively guide the quantum dots exactly onto this location throughout the wafer.

The following particle placement technique that will be detailed is a re-arrangement of the work published by L-C.Ma, R.Subramanian, H-W.Huang, V.Ray, C-U.Kim, and S.J.Koh, in Nano Lett., 7, 439, 2007 [5.28].

This technique is termed as '*electrostatic funneling*' [5.28]. In this technique, a charged nanoparticle is guided to target locations on a substrate using electrostatic guiding structures. A schematic for the electrostatic funneling technique is shown in figure 5.36. Alternating lines of different materials are stacked on a plane next to each other on a substrate. The different materials are functionalized differently such that they form alternating patterns of positively and negatively charged regions in an aqueous solution. When this substrate is immersed into a negatively charged nanoparticle colloid, the nanoparticles are attracted towards the centers of

the positively charged regions on the substrate surface and repelled by the negatively charged regions via double layer interactions [5.28]. Across the plane of the substrate surface, the interaction energy between the particle and the charged substrate surfaces will have maxima and minima. The attractive force from the positively charged regions attract the particle towards the surface whereas the negatively charged regions on the substrate surface provide the lateral forces to push the nanoparticle towards the center of the positively charged surface. Once a nanoparticle attaches on the surface, it will repel other nanoparticles from occupying the same location on the substrate as they are of similar negative charges.

The attractive and repulsive forces are directly a function of the distance between the nanoparticle and the substrate surface. A particle closer to the surface (h_1 as shown in figure 5.36 (c)) will experience a higher guiding force than the nanoparticle further away from the surface (h_2 as shown in figure 5.36 (c)).The interaction energies at these two distances from the substrate surface is shown schematically in figure 5.36 (b). Thus the particles are '*funneled*' to the centers of the positively charged substrate locations.

The main advantage of this electrostatic funneling technique is that this can be accomplished over an entire wafer by simply functionalizing the entire substrate with these charged terminal groups and immersing the substrate into the nanoparticle colloid.

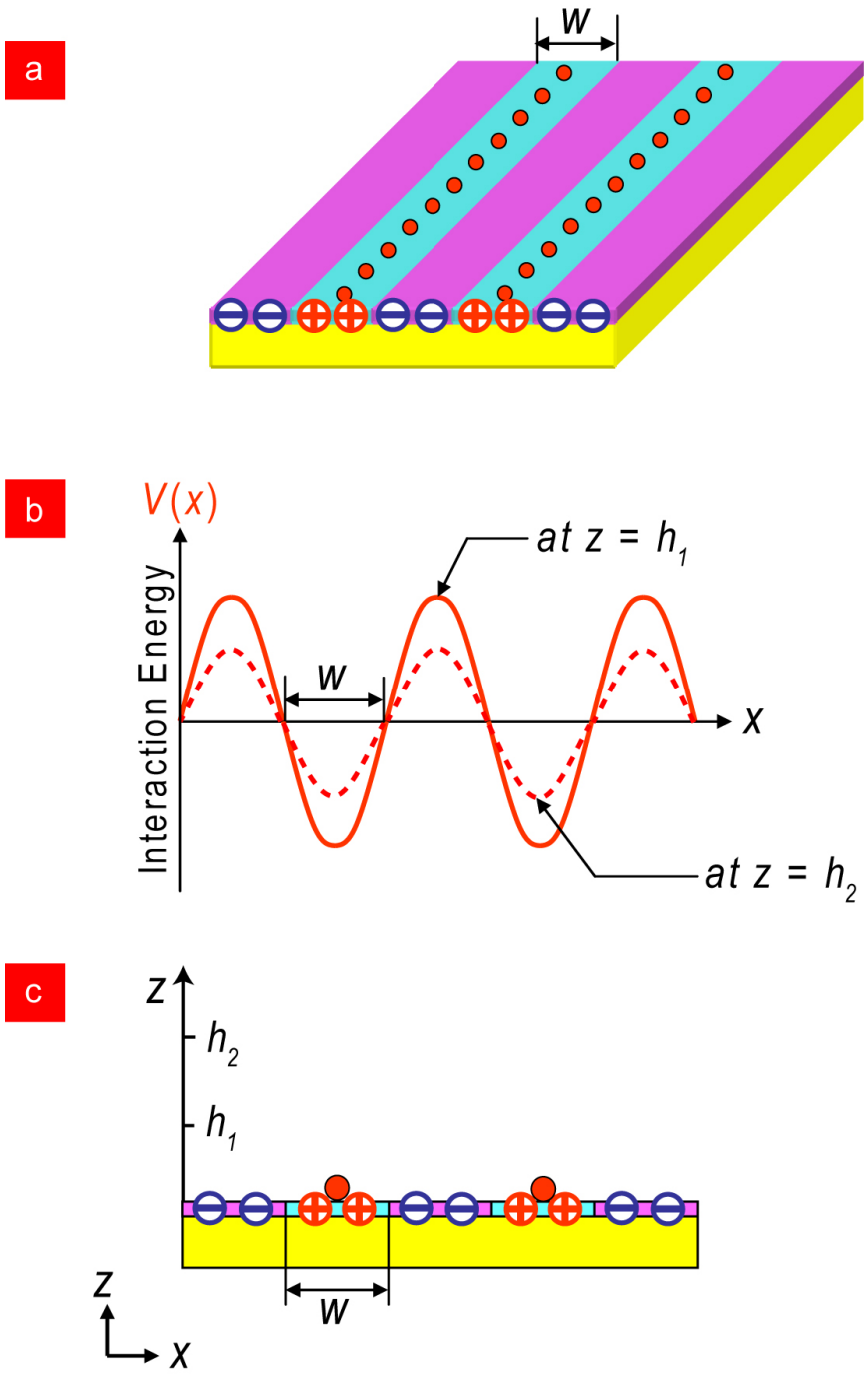


Figure 5.36: [5.28] Schematic of the electrostatic funneling technique. (a) Alternatively charged structures with negatively charged nanoparticles attached on the center of the positively charged centers. (b) Interaction energy as a function of the negatively charged nanoparticle distance '*x*' from the surface of the charged substrate. (c) Cross-sectional view of (a).

5.3.1 Experimental procedure for '*electrostatic funneling*'

A wafer with alternating lines of copper and silicon oxide which is similar to the interconnect lines used in standard CMOS technology made using the Damascene process [5.29] was used as the substrate. The width of the silicon oxide and copper lines were 80nm and 120nm respectively. Functionalization of copper surface posed a problem as copper gets oxidized easily. Gold surface functionalization is very easy compared to copper surface functionalization. Any organic molecule with a thiol head group can be attached to the gold surface using simple wet chemistry, hence gold was electroless plated onto the copper surface. The fabrication process is shown as a schematic in figure 5.37. In order to accomplish this, the wafers were diced into smaller pieces up to 2 * 2 cm in size. They were cleaned with acetone and treated in the UV –ozone chamber for 30 minutes. The samples were then immersed into a 1% citric acid solution to remove any residual copper oxide. After thoroughly rinsing with DI water and drying with a stream of nitrogen, the wafers were immersed into the electroless gold plating solution ((Alfa Aesar; major components of the plating solution are $KAu(CN)_2$, NH_4OH, and water) at 65^0C for 45 seconds. Once completed, the samples were thoroughly rinsed with DI water and dried with a stream of nitrogen. The height of the gold plated lines was ~10nm higher than the silicon oxide lines due to the deposition of gold on top of the copper lines.

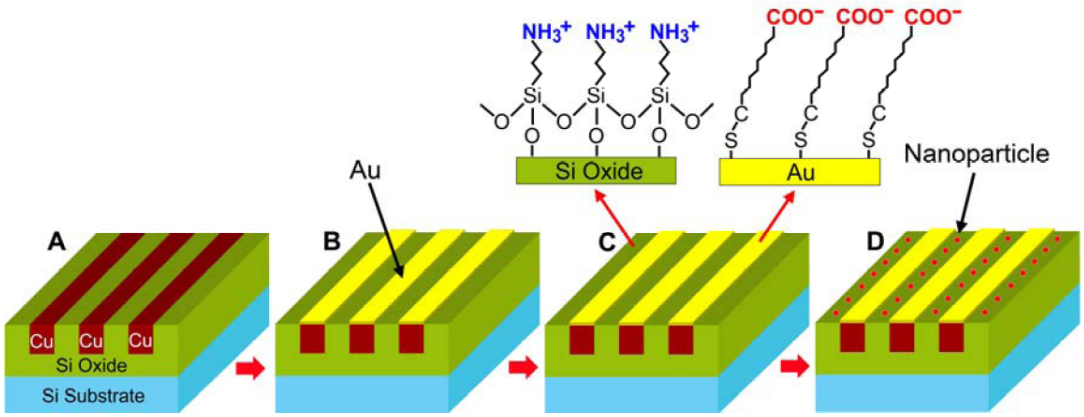


Figure 5.37: [5.28] Experimental procedures followed to demonstrate electrostatic funneling. (a) Starting structure in which copper lines (brown) are embedded in silicon oxide dielectric (green). (b) Electroless plating of the exposed copper lines with gold (c) Selective formation of self-assembled monolayers (SAMs) of APTES (NH_2; NH^{3+}) on silicon oxide surfaces and 16-MHA (COOH;$–COO^-$) on gold surfaces, respectively. These SAMs provide the silicon oxide surfaces with a positive charge and the gold surfaces with a negative charge, respectively, in an aqueous solution. (d) Immersion of the wafer into a colloidal solution containing negatively charged Au nanoparticles.

Using wet chemistry, self assembled monolayers (SAMs) of 3-Aminopropyltriethoxysilane (APTES; $[(C_2H_5)_3\text{-}Si\text{-}(CH_2)_3\text{-}NH_2]$) and 16-Mercaptohexadecanoic acid (16-MHA; $(CH_3\text{-}(CH_2)_{14}\text{-}COOH$) were formed on the silicon oxide and copper lines by immersing the substrate into first a 1mM solution of APTES in chloroform for 30 minutes and then immersing them into a 5mM solution of 16-MHA in ethanol for 3 hours, both done at room temperature. This functionalized the silicon oxide surface with an amine termination (provides positive charge in aqueous solution) and the gold surface with a carboxyl termination (provides negative charge in aqueous solution). After the immersion in 16-MHA is completed, the samples are rinsed with a 1%HCl solution in ethanol and then dried with a stream of nitrogen.

The samples are then immersed into the negatively charged gold nanoparticle colloid of mean diameter ~20nm (Ted Pella Inc.) for 30 minutes at 4^0C. The samples were then rinsed with methanol and dried with stream of nitrogen. The samples were then imaged in field emission scanning electron microscope (Zeiss Supra 55 VP).

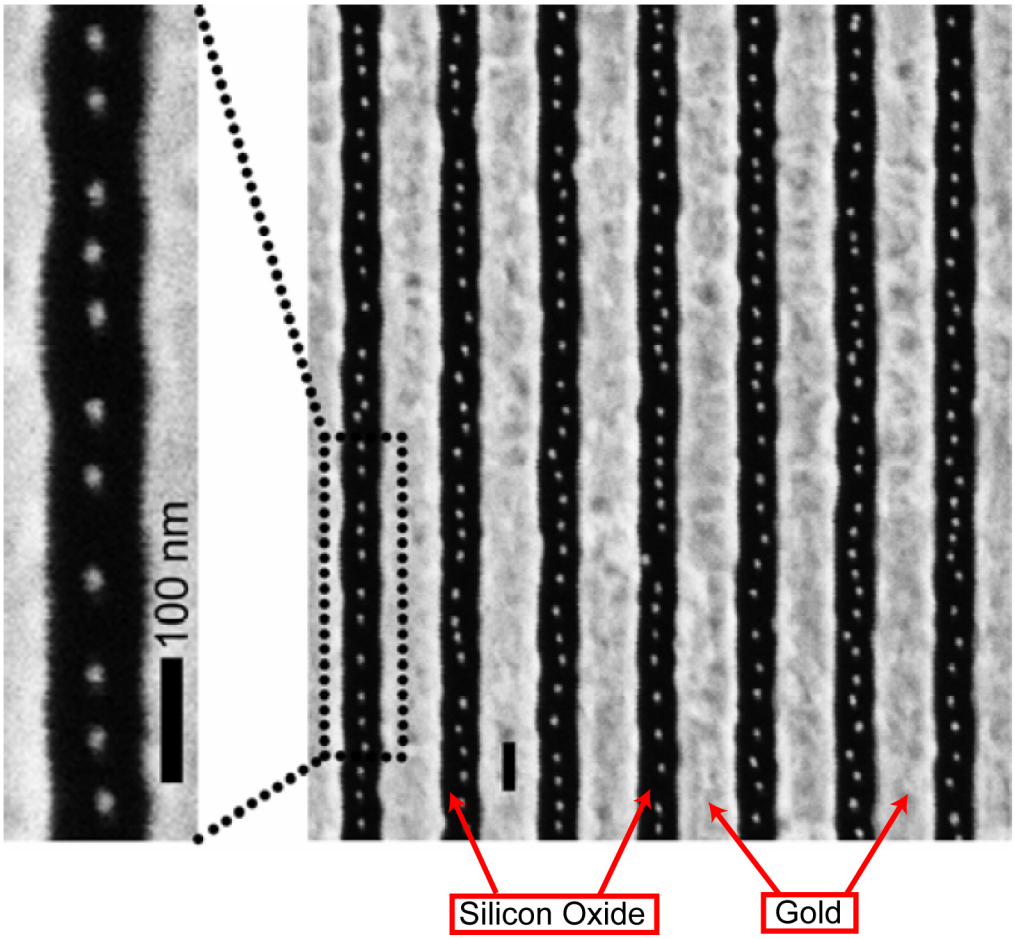


Figure 5.38: [5.28] FE-SEM image of nanoparticle precise placement using the electrostatic funneling process. 20nm Gold nanoparticles are positioned exactly on the center of the (dark) silicon oxide lines after using the negatively charged gold lines to guide them to the centers of the positively charged silicon oxide lines. Scale bar -100nm.

5.3.2 Effectiveness of the '*electrostatic funneling*' process

Figure 5.39 is an FE-SEM image of the 20nm gold nanoparticles electrostatically funneled to the centers of the silicon oxide surface using the process described in the section 5.31. The image shows a large number of gold nanoparticles placed onto the targeted substrate locations all in one single batch process. To get the estimate of the effectiveness of this process, the average deviation of the nanoparticles from center of the silicon oxide surface was measured. After measuring about 217 nanoparticles that appear in the image, the deviation of the center of the nanoparticles from the center of the silicon oxide surfaces was measured to be 6.2nm. The deviation of 6.2nm is for guiding structures of size ~100nm and nanoparticle size of 20nm which is about 3 times the size of the deviation. The inter-nanoparticle distance is also very periodic due to the particle-particle repulsion in the colloid. These deviations and particle-particle separation agree very well with theoretical calculations done by Ma et al [5.28]. Theoretical calculations were done using the DLVO (Derjaguin, Landau, Verwey, and Overbeek) theory [5.30, 5.31]. More information about the theoretical calculations can be found in the reference [5.28].

This technique of self-assembly of nanoparticles is not just limited to the planar structure shown in figure 5.39, but various other geometries were also investigated. Effective guiding structures can also be created using simple photolithography and lift-off techniques. 3-Dimensional guiding structures were fabricated using these simple CMOS compatible processes. The surfaces were again functionalized using the same SAMs layers are described in the previous section. By engineering the 3-dimensional guiding structures, it was made possible to guide different sized nanoparticles onto the targeted substrate locations. Figure 5.39 shows FE-SEM images of such experiments where a thin layer of silicon oxide was sandwiched between two layers of gold. The thickness of this dielectric layer was varied according to the size of nanoparticles to be attached.

Nanoparticles of size ~200nm, 80nm and 50nm were precisely placed on the middle of the intervening silicon oxide layer by immersing the functionalized substrates into the gold colloids for 30, 20 and 10 minutes respectively.

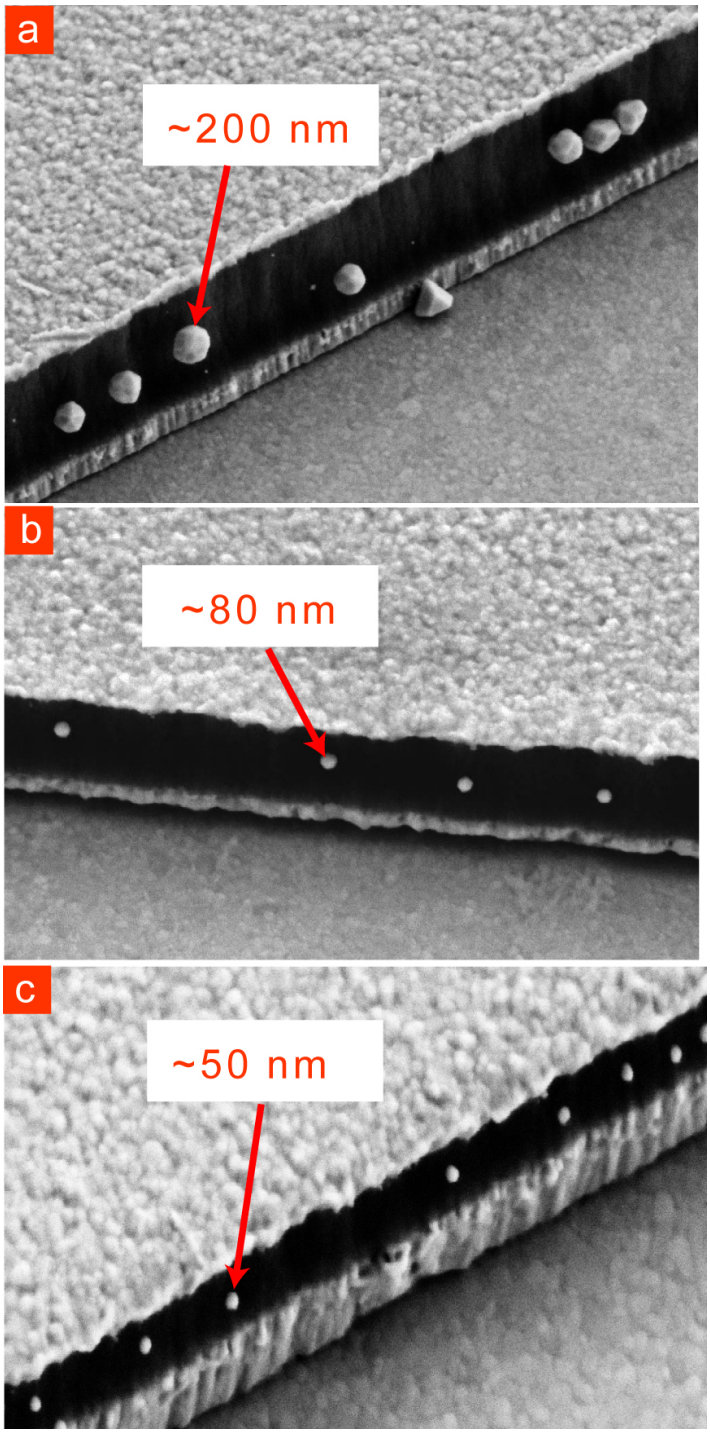


Figure 5.39: [5.28] FE-SEM of nanoparticles attached to the sidewall of the electrostatic guiding structure in 3-dimensional form. (a) Precise positioning of ~200nm gold nanoparticles. (b) Positioning of ~80nm Au nanoparticles. (c) Alignment of ~50nm Au nanoparticles.

The 3-dimensional guiding structures shown above in figure 5.39 are almost identical to the spectroscopic measurement unit architecture. This technique of electrostatic funneling can be introduced into the fabrication process to possibly increase the yield. Care must be taken to properly design the guiding structures as well as the quantum dots need to be functionalized to carry a negative charge in an aqueous solution. Functionalization of quantum dots can be accomplished using simple chemistry [5.32-5.34]. In order to attach the <10nm quantum dots onto the middle of the dielectric layer, the repelling force from the negatively charged gold regions must be reduced. This can be accomplished by using a non-charged terminal group such as $–CH_3$ (methyl) terminal group SAMs layer. The methyl end group does provides neither a repulsive force nor any attractive force, hence the nanoparticles selectively attaches only to the silicon oxide region with the positively terminated $–NH^{3+}$ (amine) group. Figure 5.40 shows the difference in repulsive forces from carboxyl and methyl terminated surfaces. By changing the terminal groups in the SAMs layers, we can engineer the interaction energies between the charged nanoparticles and the functionalized substrate surfaces to precisely position the nanoparticle onto the targeted substrate locations.

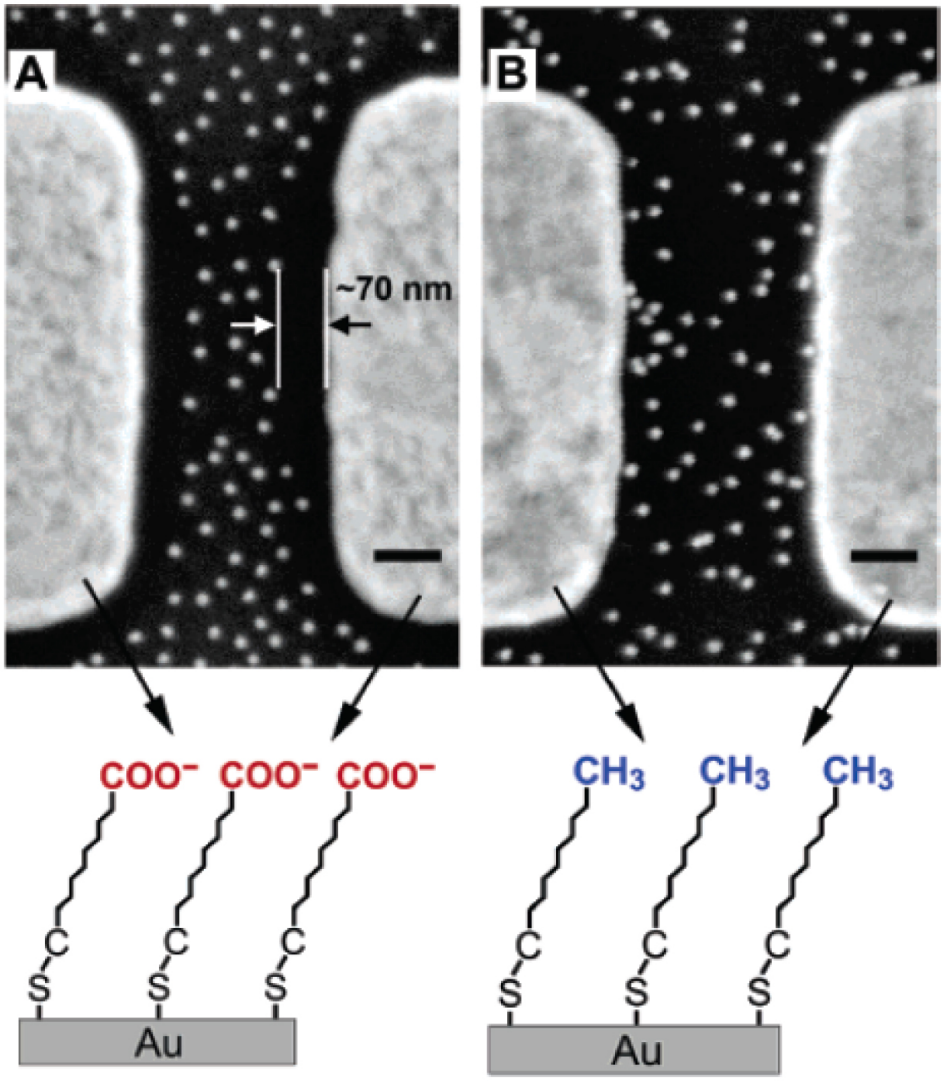


Figure 5.40: [5.28] Control of particle placement using different combinations of SAMs. Using a combination of different SAMs, the interaction energy between the charged nanoparticle and the charged surfaces on the substrate can be utilized to precisely place the nanoparticles.

Figure 5.41(a) shows how this electrostatic funneling technique can be applied to the spectroscopic measurement unit architecture. Two different SAMs layer have to be used on the silicon oxide surface and the electrode metal surfaces. The metal electrode surfaces are functionalized with SAMs-A with methyl termination and the silicon oxide surface is functionalized with SAMs-B with amine termination. Using this configuration, the negatively charged quantum dots can be selectively placed on the positively charged silicon oxide surface.

Figure 5.41(b) shows an FE-SEM image of ~80nm Au nanoparticles attached only on the silicon oxide surface. In this sample, the silicon oxide surface was functionalized with SAMs of APTES and the gold electrodes were functionalized with methyl terminated groups (1-Octadecane thiol –ODT; $HS-(CH_2)_{17}-CH_3$). The ODT SAMs is formed by immersing the patterned substrate in a 5mM solution of ODT in n-Hexadecane at 40^0C for 42 hours and then rinsing the samples with warm acetone at 40^0C and drying with a stream of nitrogen. From the FE-SEM image it clearly evident that the nanoparticles are placed exactly on the center of the silicon oxide surface, not only that, there are no nanoparticles attached on either of the electrode surfaces. The ODT layer does not offer any if at all, repelling force thus enabling the nanoparticles to selectively attach to the silicon oxide surface. Figure 5.42 shows a $Cr/SiO_2/Cr$ sidewall image with 100nm Au nanoparticles selectively placed on only the SiO_2 surface functionalized with the APTES. The Cr surface was functionalized with Hexadecanoic acid. If the thickness of the silicon oxide layer is reduced to ~7nm, this technique could possibly be utilized to selectively attach functionalized quantum dots on to the PECVD silicon oxide surface on the exposed sidewall, thereby possibly increasing the yield of the spectroscopic measurement units.

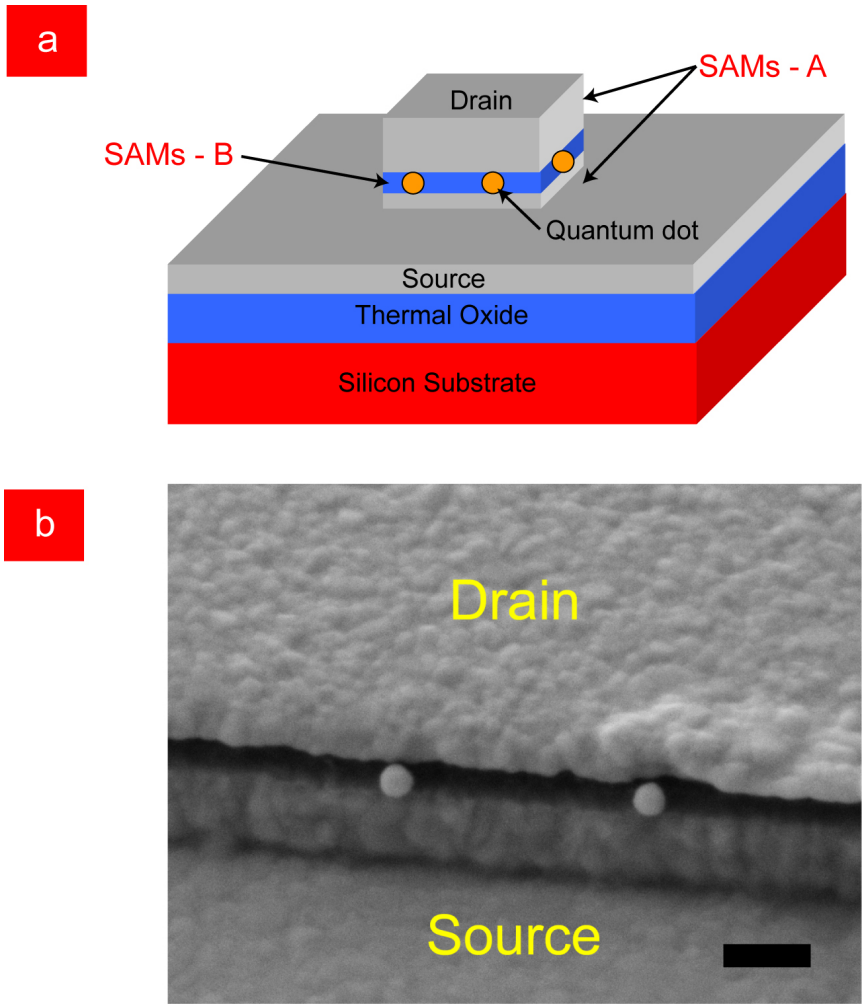


Figure 5.41: (a) Selective placement of negatively charged quantum dots on positively charged silicon oxide surface as the methyl termination. (b) FE-SEM image of silicon oxide layer (dark) sandwiched between gold electrodes and ~80nm Au nanoparticles are selectively placed only on the silicon oxide surface using SAMs of APTES on silicon oxide surface and SAMs of ODT on gold electrode surfaces. Scale bar = 200nm.

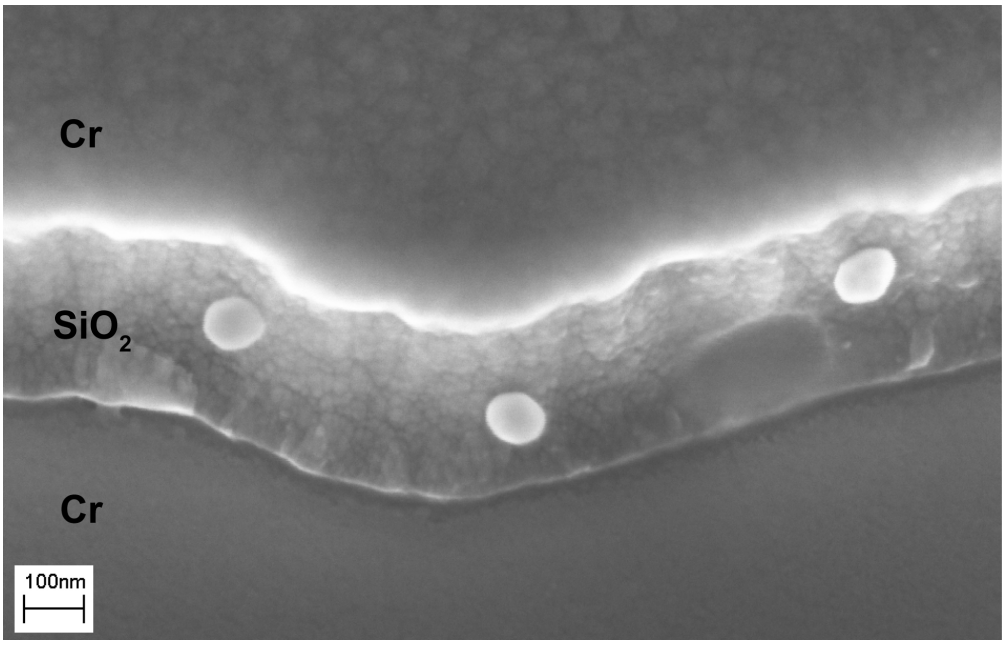


Figure 5.42: Cr/SiO_2/Cr sidewall structure with 100nm Au nanoparticles selectively placed only on the SiO_2 surfaces. Cr and SiO_2 surfaces were functionalized with Hexadecanoic acid and APTES respectively.

The spectroscopic measurement technique shown in this work only shows measurements for individual quantum dots. This technique can be employed to study other quantum dots such as Indium Phophide (InP), Lead Selenide (PbSe), Lead Sulfide (PbS) etc which have a smaller band gap. By engineering the source-drain separation, it may be possible to extend this spectroscopic measurement technique to other types of nanostructures such as core-shell nanoparticles and quantum rods etc. The simplicity of this measurement technique by using simple current-voltage and direct differential conductance measurements combined with the fabrication processes that are CMOS compatible make it possible to conduct resonant tunneling spectroscopy of individual quantum dots even at room temperature. This only allows the measurements of smaller sized nanoparticles easier as they have larger energy level separations and can thus be easily accomplished at room temperature.

CHAPTER 6

CONCLUSIONS

The fundamental knowledge of the electronic structure of the nano-objects such as quantum dots, quantum rods etc, is imperative for them to be employed as active devices or sensor materials.

In Chapter 3, a new technique to conduct tunneling spectroscopy on individual quantum dots using the double barrier tunnel junction approach was proposed. The key merit to this structure is to provide a spectroscopic measurement structure that allows for the direct measurement of the energy level structure of individual quantum dots without any conductance peak broadening effects. A vertical electrode structure was employed where the source and the drain electrodes are separated by a thin dielectric layer. The thickness of this layer determines the separation between the source and the drain electrodes. The gap between the electrodes was controlled in the sub-nanometer regime using deposition processes such as PECVD as detailed in Chapter 4. The spectroscopic measurement unit was fabricated by tethering the quantum dots to the exposed sidewall of the source/dielectric/drain structure using self-assembled monolayers (SAMs) and finally passivating the entire measurement unit. Each measurement unit was individually addressable and all such units were fabricated using CMOS compatible parallel batch processing.

The setup of measurements and measurement data was discussed in Chapter 5. Measurements accomplished at both room temperature and low temperatures were detailed. Clear step-wise current increases demonstrating resonant tunneling through an *individual* quantum dot was detailed. Differential conductance plots obtained by either direct measurements or through numerical methods were used to map the electronic structure of

these '*single*' quantum dots. Using systematic analysis the exact energy levels separations were deciphered from the differential conductance measurements. Detailed analyses demonstrated absence of any electron-phonon coupling occurrences using this spectroscopic measurement technique, which is always observed with STM tunneling spectroscopy. Data demonstrated a clear linear dependence of the peak width on temperature only without other peak broadening effects.

The major accomplishment of this work was enabling the probing purely the energy levels of *'single'* quantum dots. Due to this nature of measurement, room temperature measurement of the electronic structure was made possible as there was no additional peak broadening other than the thermal peak broadening. The FWHM of the conductance peaks at 77, 150, 225 and 295K were measured to be 3, 7, 9 and 18 meV respectively, which shows the linear dependence of peak widths on temperature. Due to the dependence of the peak width only on the temperature, very fine energy level separation measurement (fine resolution) is possible using this spectroscopic technique. Room temperature measurement of the energy level separation is possible using this new spectroscopic technique as the peak widths were only ~20meV at room temperature. Energy structure mapping was demonstrated for both electron and hole energy levels at room temperature as well as low temperatures.

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BIOGRAPHICAL INFORMATION

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