EFFECT OF STRUCTURAL DESIGN PARAMETERS ON WAFER LEVEL CSP BALL SHEAR STRENGTH AND THEIR INFLUENCE ON ACCELERATED THERMAL CYCLING RELIABILITY

By

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ABSTRACT

EFFECT OF STRUCTURAL DESIGN PARAMETERS ON WAFER LEVEL CSP BALL SHEAR STRENGTH AND THEIR INFLUENCE ON ACCELERATED THERMAL CYCLING RELIABILITY

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Wafer level chip scale package (WLCSP) is one of the most popular packages due to its size and cost advantages. It is expected that the usage of WLCSP in microelectronics and MEMS industry combined is going to cross 16000 Million Units by 2013. One of the main advantages of implementing WLCSP is its time to market because most of the package is done at the wafer level. Once the wafer processing is completed the package is just diced and mounted on board and the board is ready to go. However, just like any other package WLCSP too is not ideal and do have weaknesses from reliability point of view. The advantage of having a WLCSP is that the reliability program can be divided into two parts namely Wafer level reliability and Board level reliability. Ball shear test, Ball pull test etc. are some of the popular wafer level reliability tests that are very commonly employed in wafer fabs. Popular Board level accelerated tests are Drop tests and accelerated thermal cycling. Typically, the time taken by the board level reliability tests is much more as compared to wafer level reliability tests.

Various researchers have attempted to correlate board level and wafer level reliabilities using experimental and statistical correlations. Such correlations exist for High speed shear and high

speed ball pull and board level drop testing. However, such correlations don't exist for accelerated thermal cycling and wafer level reliability tests. In this dissertation, three different solder compositions, three solder sizes are mounted on two structures that are very commonly used in wafer level chip scale packages. The structures are fabricated on wafer and sheared off using a commercially available ball shear tester and two important results were noted (a) ball shear strength and (b) % ductile failure mode incidence. The structures were sheared off at two different heights namely 25μm and 125μm heights. The results in terms of gram force from both heights were combined in a statistical term called as Signal to Noise ratio which is Negative logarithm to the base 10. Results obtained using experimental ball shear were validated computationally using commercially available finite element codes.

Similar WLCSP packages were assembled on standard accelerated thermal cycling boards and were cycled between temperature extremes of -40ºC and 125ºC at the frequency of 2 cycles/hr. Weibull plots were obtained for all board assemblies for different scenarios considered in the study. Results from accelerated thermal cycling and ball shear testing were matched using two ways (a) the stress and inelastic strain from both the tests were matched on a log-log plot and (b) % ductile failure mode from ball shear testing was matched with Number of cycles and Weibull parameter from accelerated thermal cycling using CORREL function and correlation coefficients were determined. The correlation coefficients were determined from taking into consideration the variation in structure and corresponding changes in the Number of cycles in accelerated thermal cycling. Effect of individual structural parameters on the fatigue life was analyzed and corresponding recommendations were made.

It was concluded that matching stress- strain from accelerated thermal cycling and ball shear strength didn't result into any correlations. % ductile failure mode is a better parameter in establishing correlations between the two tests.

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CHAPTER 1

INTRODUCTION

1.1 Miniaturization of Electronic Components

Electronic devices now permeate virtually in every aspect of our life. Among most ubiquitous of these are the portable consumer electronics such as Laptop, PDA, cell phones, smart phones etc. The applications of electronic systems vary from entertainment to highly complex systems supporting vital health, economic, scientific and military. Developments in the semiconductor industry, along with consumer demand for cheaper, lighter, high density information processing tools have revolutionized the entire electronic packaging infrastructure. The result of this demand has resulted in development of high function, high density interconnect semiconductor devices with ever increasing functionality into smaller and smaller devices. Figure 1.1 shows the trend of packages decreasing size from a Quad Flat Pack to a Flip Chip Package and more.

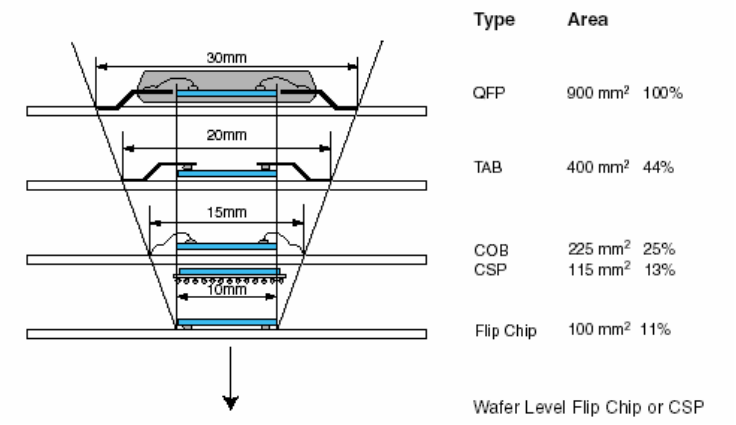


Figure 1.1 Reduction of the footprint of Electronic Package [1]

Chip scale packages were the workhorses of miniaturization post 1995. But Wafer level package reduces the size of the package and increases the packaging efficiency even more than a chip scale package. Next section talks about chip scale package and Wafer level Chip scale package.

1.2 Packaging Efficiency

Packaging Efficiency is defined as the ratio of area of die to the area of IC package. This is a very important parameter and plays a key role in miniaturizing electronic systems. Portable consumer electronic systems such as cell phones, PDAs, smart phones, digital cameras, camcorders and laptops have packages with high Packaging Efficiency where size is the most important concern. Bare chip packaging, as per the above definition is 100% efficiency, Dual Inline Package has less than 2% efficiency, BGA has about 30%-80% efficiency. Chip Scale Package (CSP) is defined as any IC package which occupies a footprint area of no more than 50% greater than area of the chip it packages and which has a perimeter no more than 20% greater than that of the chip it packages [1]. CSP is one of the most important packages types in recent years due to the unprecedented demand for portable and hand held devices. The advantage of CSP, compared to direct chip attach of flip chip to a board, is that the CSP is designed to take up the mismatch if coefficient of thermal expansion (CTE) between the chip and the board. Hence, in general it is not necessary to underfill the chip scale package after it is soldered to the board, which is very important component in flip chip assembly. This is one of the main reasons why CSP packages were the driving force of miniaturization especially in portable electronics in last decade. Another important reason for popularity of Chip scale package is it can normally be implemented into a standard surface mount process without any major modifications. Wafer level package however offers even better packaging efficiency, when chip scale package technology is implemented on the wafer scale that's when we get the Wafer Level Chip Scale Package (WLCSP).

1.2.1 Wafer level Chip Scale Package

The Wafer level package (WLP) is a type of chip scale package (CSP), which enables the IC to be attached face down to a printed circuit board (PCB) using conventional Surface Mount Assembly methods. WLP technology differs from Ball Grid Array, leaded and laminates based CSPs because no bond wires or interposers are required to connect die to the substrate. WLP can have good reliability without using an underfill because typically for WLP to be used in portable electronic devices the size of interconnect is big hence it has more compliance with the CTE mismatch. The main advantages of WLP are as follows

1. Space savings from attainment of the smallest package possible for a device i.e. a true chip size package.
2. Lowest cost per I/O since the traditional package assembly processes that are independent of wafer fab have been replaced by wafer level interconnection processes.
3. Lowest cost of electrical testing since this is done more efficiently at wafer level.
4. Lowest cost of burn-in since this is done more efficiently at wafer level.
5. Enhancement of device performance because of its minimum length interconnections.
6. Eliminating the need for underfilling of solder joints with organic materials hence possibility to rework the package and,
7. Easier inventory management since fab, assembly, test and burn-in can essentially be housed under one production floor. [2]

Typical wafer level package is shown in figure 1.2.

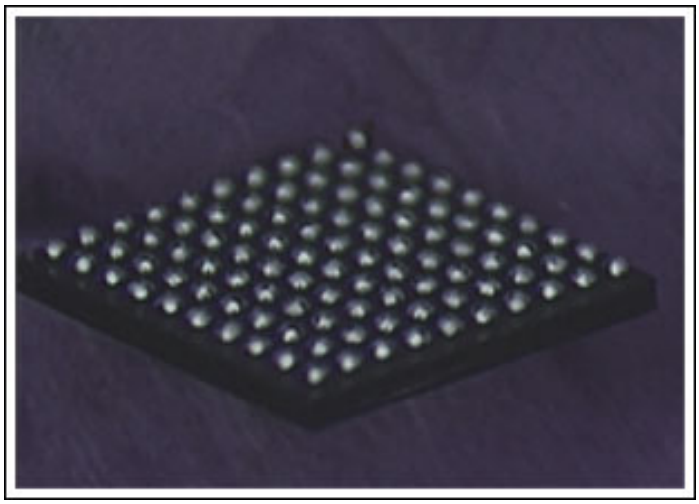


Figure1.2: Typical Wafer Level Chip Scale Package [3]

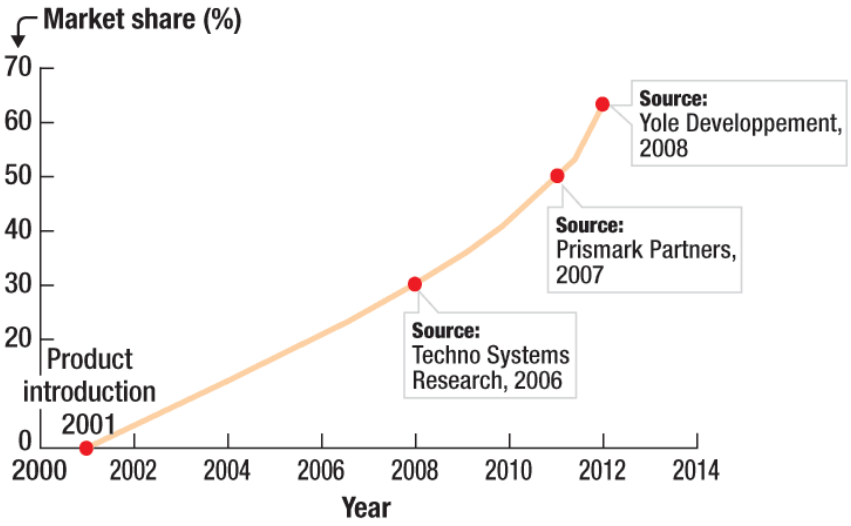


Figure 1.3: Market share of Wafer level packages in camera modules [91]

Yole.com reports that “Wafer level packaging is a confirmed high growth trend in the semiconductor packaging industry. Wafer level chip scale packaging (WLCSP), or the direct bonding on printed circuit boards (PCB’s) of bumped integrated circuits (IC’s) as one of the most visible expressions of WLP and is the fastest growing package type in the whole industry. Yole’s research study forecasts that it will exceed 10 billion units per year by 2012, at a

compound annual growth rate of more than 20% over the next 5 years as seen in figure 1.4. Primarily driven by footprint and thickness reduction of packaged integrated circuits in mobile phones, in a wide range of circuits for handsets, EMI/ESD interface protection, power supply, converters, LED drivers, MOSFET's and other features like FM,GPS, TV and on camera."

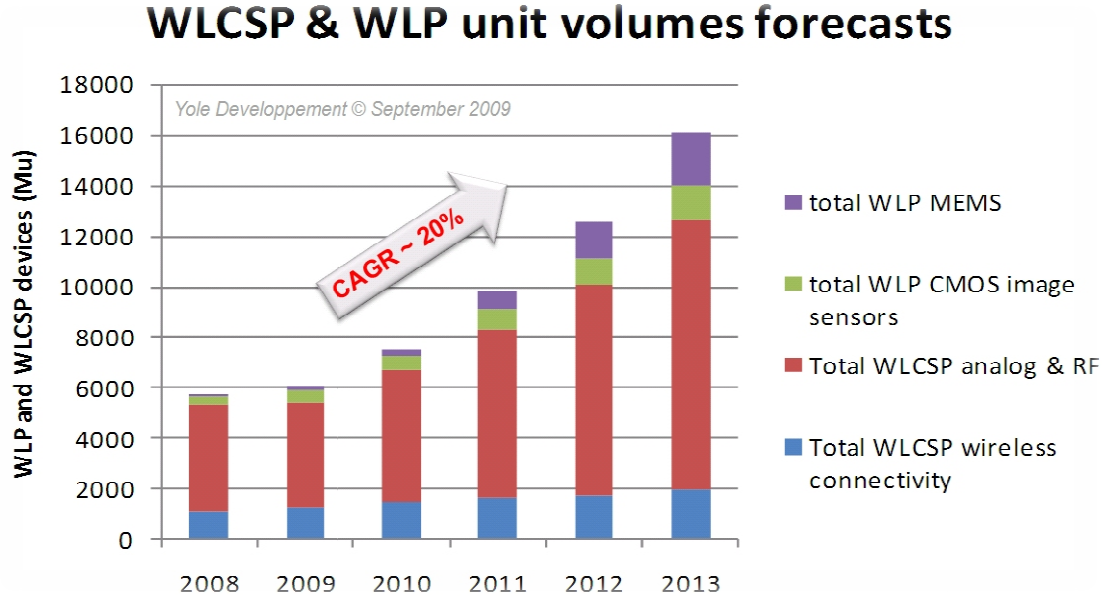


Figure 1.4: WLCSP and WLP unit volumes forecasts [92]

Besides offering unequaled benefits of small footprint and thickness geometries, WLCSP has become cost competitive with QFN, its main package platform competitor in handsets. This cost benefit now paves the way for the adoption of WLCSP by more consumer end user applications like netbooks, notebooks, gaming consoles, MP3 players and digital still cameras. Some WLCSP devices can also be found in automotive applications, which may well represent a future growth sector for WLP. Figure 1.5 shows the comparison of value offered by a wafer level chip scale package as opposite to other small packages.

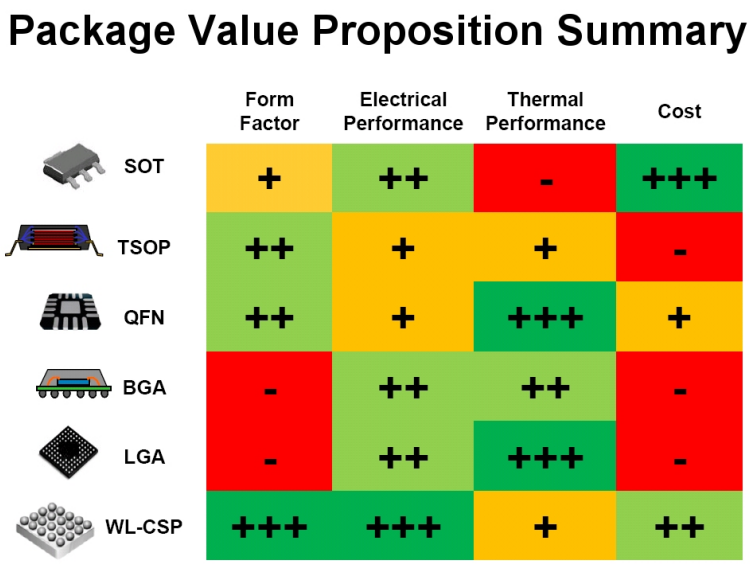


Figure 1.5: Comparison of WLCSP with other small packages [92]

Besides offering unequaled benefits of small footprint and thickness geometries, WLCSP has become cost competitive with QFN, its main package platform competitor in handsets. This cost benefit now paves the way for the adoption of WLCSP by more consumer end user applications like netbooks, notebooks, gaming consoles, MP3 players and digital still cameras. Some WLCSP devices can also be found in automotive applications, which may well represent a future growth sector for WLP.

Although Wafer level Chip scale package is great from all aspects of reducing size, increasing packaging efficiency, saving cost etc. it is not entirely free from failures. Wafer level chip scale packages present unique reliability challenges because as the size of the package reduces, number of packages put together on a wafer increases dramatically. Hence there are issues related to processing that typically can get percolated down the line as the package goes through different levels of packaging. In order to understand the reliability challenges that are offered by wafer level chip scale packages it is important to understand the process in which a package is fabricated from silicon crystal.

1.3 Fabrication of structures on wafer level

Wafer level fabrication of a chip scale package is an extremely complicated process and it typically involves a lot of processes and each of that process is dependent on controlling factors. Typical steps involved in wafer level fabrication of an IC package are discussed in this section. Processing of wafers can essentially be divided into two sections namely, front end processing and back end processing. Semiconductor manufacturing consists of the following steps

1. Production of silicon wafers from very pure silicon ingots
2. Fabrication of integrated circuits into these wafers
3. Assembly of every integrated circuit on the wafer into a finished product and
4. Testing and back-end processing of finished products.

1.3.1 Wafer level fabrication process

Wafer fabrication generally refers to the process of building integrated circuits on to silicon wafers. Prior to wafer fabrication, the raw silicon wafers to be used for this purpose are produced as a single crystal using Czochralski (CZ) method. The single crystal is then cut into very thin plate's perpendicular to its axis. The thin plates (also called as ingots) are then shaped into wafers using a process called as wafering. At the end of this process, a wafer has number of transistors that are connected to the second level interconnect which will eventually be connected to a board. A generalized process of forming devices is as follows

1. A p-type or n-type epitaxial layer on the silicon substrate is grown through chemical vapor deposition.
2. A Nitride layer is then deposited over the epi-layer, the nitride layer is masked and is then etched out using physical or chemical etch leaving behind exposed areas on the epi-layer i.e. areas no longer covered by the nitride layer.

3. The exposed areas are masked again and then bombarded with ions of the doping material in specific patterns using diffusion or ion implantation. Typical dopants used are phosphorous forming n-wells.
4. Silicon dioxide is then grown thermally to form oxides that isolate the n-wells from other parts of the circuit. This may be followed by several other steps of masking/oxidation cycle to grow gate oxide layers over the n-wells intended for p-channel MOS transistors. The gate oxide layer serves as the insulation between the p-type and n-type.
5. Deposition of polysilicon layer over the wafer may then be done, to be followed by a masking/etching cycle to remove unwanted polysilicon areas defining the polysilicon gates over the gate oxide of the p-channel transistors. At the same time, openings for source and drain drive-ins are made on the n-wells by etching away oxide at the right locations.
6. Another round of mask/implant cycle may then follow, this time driving the p-type dopant (typically boron) into new openings forming the p-type sources and drains. In such a way there are several mask/implant cycles that are repeated depending on the structure of the package.
7. The wafer is covered with phosphor-silica glass, which is then subjected to reactive ion etching in specific patterns to expose contact areas for metallization. Aluminum is then sputtered on the wafer, after which it is subjected to reaction ion etching, also in specific patterns, forming connections between various components of the circuit.
8. The wafer may then be covered with glassivation as its top protective layer, after which a mask/etch process removes the glass over the bond pads. Such is the process of wafer fabrication, consisting of a long series of mask/etch and mask/deposition steps until the circuit is completed.

9. The interconnection typically in case of a wafer level chip scale package is a solder bump. Thus once, the wafer with complete integrated circuit comes at the bumping process, pre-formed bumps are placed over the wafer and are pressed against the bond pads to form a temporary joints.
10. After the bumping process the wafer goes through a reflow oven where under the action of a reflow profile a firm bond between the solder and the bond pad due to formation of intermetallics and hence the wafer fabrication of the chip scale or for that matter any package is completed. [4]

Figure 1.6 shows the fabrication process of fabricating the device structure.

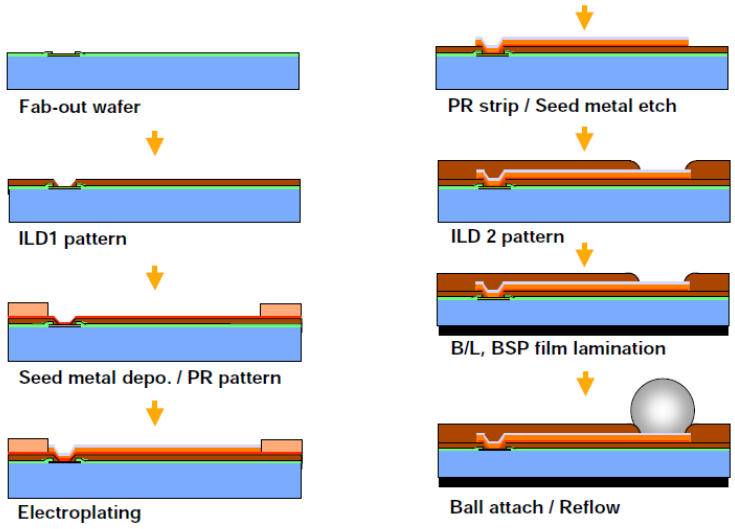


Figure 1.6 Process of fabrication of structures on a wafer [5]

The procedure mentioned in the above section is followed for practically every wafer level device fabricated in the industry with variation of the actual process parameters. Most important thing about fabrication of devices on wafer is that they have to be designed for reliability considerations of portable devices, high end devices, military standard devices etc. A wafer level package faces reliability challenges that are unique to each of these environments. In this dissertation however, we are going to focus only on the portable electronics section.

1.4 Reliability Considerations in Portable Electronic Devices

Portable electronic devices are exposed to a wider variety and severity of environmental stresses than their desktop counterparts. The failure of packaging and semiconductor components is often accelerated by higher than normal stresses such as temperature, relative humidity, excess voltage and current, vibration, shock and high acceleration. Ionic Contaminants, air borne particulates (dust and dirt), and environmental pollutants are added to hasten the onset of certain failure modes. [6] Long-term degradation cannot always be demonstrated at normal operating conditions. The sample size and the test are subjected to larger than usual environmental stresses to obtain failure data in a short amount of time. These tests are called accelerated environmental stress tests. The objective of accelerated tests is to estimate the lifetime distributions of the components at normal stress levels using failures data from such tests. These are designed to evaluate the robustness and reliability of the board level packages. Many of the tests with accelerated stress conditions are designed to enable the packaging engineer to extrapolate the test results to the field environments. Some of these tests are conducted with specially designed test vehicles, prior to the product manufacturing. The test vehicles are designed to exercise the design, fabrication and process limits of a given technology. Most products utilizing that technology are expected to have the intended reliability.

With the growing availability of low cost, portable devices, reliability engineers need to develop test programs that can be administered and can quickly to provide accurate information about the performance of the entire system. A well thought out and aggressive test program is one of the most significant techniques to validate the design's integrity and ability to meet established usability requirements. In this discussion general test planning plus considerations spanning the categories of mechanical, and thermo-mechanical reliability have been discussed.

One of the most important advantages of having wafer level chip scale packages was their faster time to market time and cost. Acceleration tests to determine the failure mechanism

and hence failure are different at every packaging level. Figure 1.7 shows different failure mechanisms and acceleration factors involved at all different levels of packaging.

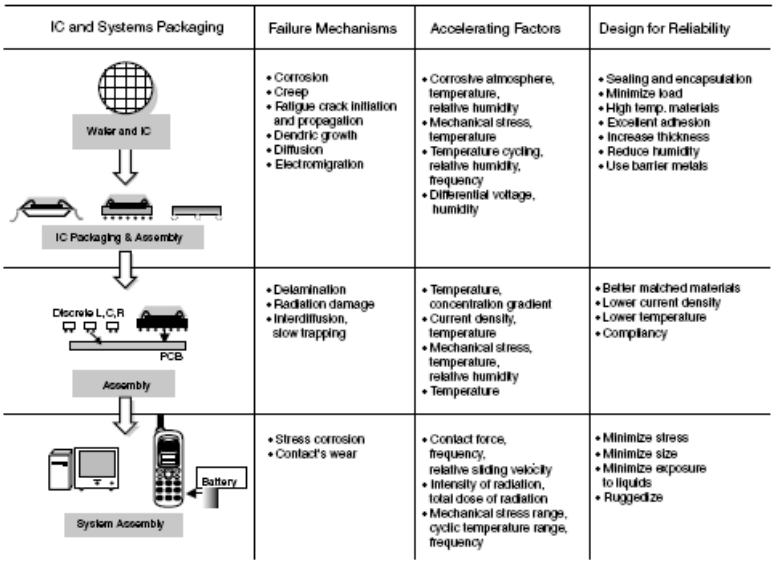


Figure 1.7: Failure mechanisms and acceleration factors at different levels of packaging [1]

It can be inferred from figure 1.7 that different levels of packaging have different failure mechanisms, different acceleration factors and different designs for reliability. Hence different at different levels of packaging there are different reliability tests that have been designed by Joint Electronic Device Engineering council (JEDEC) to capture the failures and eventually create design for them. An important challenge in designing a reliability program and a test vehicle is how to reduce its duration without sacrificing the accuracy of results.

1.4.1 Interconnect Reliability at Wafer level

Due to miniaturization, the number of iterations involved with the mask/etch process typically forming layers of interconnect increase. These different layers are then metalized using various processes and are programmed to perform specific tasks. Each of the processes namely spinning, etching, lithography, UV exposure, bumping and reflow are extremely sensitive to their controlling factors and temperature. Any variations in these knobs directly affect attachment of these layers considerably and hence it is important to have a test that can

check structure mechanically. The interconnect in case of a wafer level chip scale package is a solder bump made of a lead free solder that is attached on the bond pad and then reflowed to form a joint. The desired test should satisfy the following requirements.

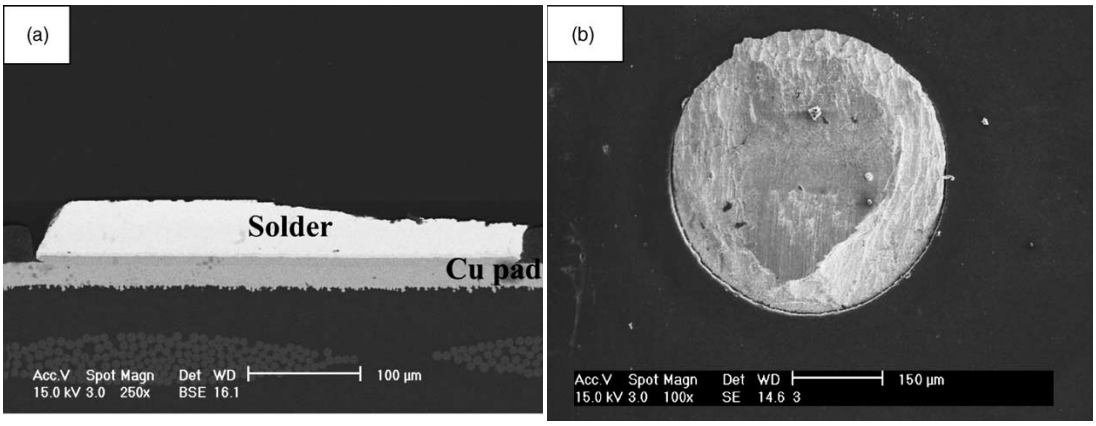
1. The reliability test should let the designer know what knobs are important and what the possible failures over a wide range of strain rates.
2. The reliability test should be easily employed in the wafer fabrication routine.
3. The test should be inexpensive and
4. The turnaround time of the test should be as little as possible.

Table 1.1 gives a summary of commonly employed failure reliability tests that are used for checking quality of a wafer level structure.

Table 1.1: Summary of Failure Reliability Tests that are used to check quality of wafer level structure

No.	Mechanical Testing Method	Cost of Test	Prep and Test time
1	Solder Ball shear	Low	Short
2	High speed ball shear	Low	Long
3	Cold Ball Pull	Low	Short
4	High speed ball pull	Low	Long

Ball pull test and ball shear test are very commonly employed in a wafer fabrication facility to check the process reliability. In case of high speed shear and high speed pull typically sample preparation is required. The sample consists of a particular part of wafer that is separated out by breaking the wafer and then is glued to a mounting plate using LocTITE and hence the time taken by the test is long. Figure 1.6 shows the typical failure mode that is observed in a ball shear test.



(a) (b)

Figure 1.8: Typical failures observed in a Ball shear Test (a) side view and (b) top view [7]

Several researchers have attempted to compare ball shear and ball pull and have tried to find out which mechanical testing method is better in identifying brittle failure mode. In ball pull test the primary failure mechanism is tensile force whereas in ball shear test the primary failure mechanism is shear force. Figures 1.8a and 1.8b show the typical failure modes that are observed in a ball shear test respectively. Typically the failures observed in these tests are divided into three modes namely ductile failure, semi-ductile failure and brittle failure. Different researchers have used different nomenclatures for describing the above mentioned failures. In this dissertation they are described as mode 1 failure, mode 2 failure and mode 3 failures. More about ball shear test and its failure is explained in chapter 3 of this dissertation. Every failure mechanism has its own signature and that can be found through its failure modes. For a ball shear test it is tension on one side and compression on other side of the bond pad. That particular failure signature matches with accelerated thermal cycling test which is a standard test done for the assessing reliability of interconnects at second level of packaging. In case of accelerated thermal cycling the failure mechanism is compression and on one side and tension on other side of bond pad. In case of accelerated test the direction of shear forces and hence signature alternates as temperature is ramped up and down in the given thermal cycle.

1.4.2 Interconnect Reliability at board level

As the package climbs up the ladder from first level packaging test to second level packaging the reliability tests change considerably. Second level reliability tests are followed after the reflow cycle. Thermal cycling tests are used to study the effect of thermo-mechanical stresses generated during operation of electronics. Shear strains and hence stresses are generated because of the mismatch between coefficient of thermal expansion between package and board. Thermal cycling tests are typically carried out in air-to-air or fluid-to-fluid test chambers depending on the required ramp rate of the cycling. Figure 1.9 shows the typical arrangement of boards and the acceleration cycle that is given to the chamber.

(a) (b)

Figure 1.9: Typical thermal cycling test setup (a) Chamber (b) Arrangement of boards in the chamber [8]

Important factors affecting the fatigue life of solders in accelerated thermal cycling are the temperature extremes and hence the mean temperature, the ramp rates, dwell times and frequency of cycle. Typically the maximum temperature in a thermal cycle is 125ºC which corresponds to a homologous temperature of 0.57-0.6 thus it allows the creep strain is also a major contributor to the total strain which cannot be ignored totally as it is done in a plasticity dominated failures. Different organizations have different standardized tests for accelerated

thermal cycling; JEDEC has published its own standardized test standard JESD22-A104C [9] for standard handheld portable electronic product. So for every test an organization spends thousands of dollars on equipment operating cost and maintaining cost. On top of it every product line will be going through a series of board level reliability tests. Researchers have actually started getting a crack at establishing acceleration factors between board level reliability and wafer level reliability. This dissertation is an attempt to establish similar acceleration factors between ball shear test and accelerated thermal cycling reliability.

In this dissertation, an attempt has been made to establish acceleration factors between wafer level ball shear testing and board level accelerated thermal cycling. Figure 1.10 compares the turnaround time of ball shear test and accelerated thermal cycling. Establishing acceleration factors between wafer level reliability testing and board level reliability testing is tedious. At wafer level the solder typically is as cast or virgin solder. An as cast lead free solder will have very less number of grains. In case of board level reliability tests the solder goes through another reflow process for joining of solder to board. This process adds another set of intermetallics formed on the board pad side. As the package goes through the accelerated thermal cycling the solder structure is modified into many grains primary due to the grain boundary binding phenomena that is very common in fatigue loadings. Thus, development of an analytical model is not possible between the two. Hence any correlation that is derived between wafer level reliability tests and board level reliability tests are empirical. To understand various aspect of structure, solder material and solder size a huge DOE has to be planned. In this study a DOE comprised of three solder materials SAC 305, SAC 405 and SAC 125Ni, three solder bump sizes 250μm, 300 μm and 350 μm, two different structures namely ball on pad structure and ball on RDL structure, three different dielectric thicknesses 3 μm, 7 μm and 12 μm are discussed. In this study ball shear test and accelerated thermal cycling were done separately and hence are discussed separately. Figure shows the difference in testing times between the ball shear test and the accelerated thermal cycling.

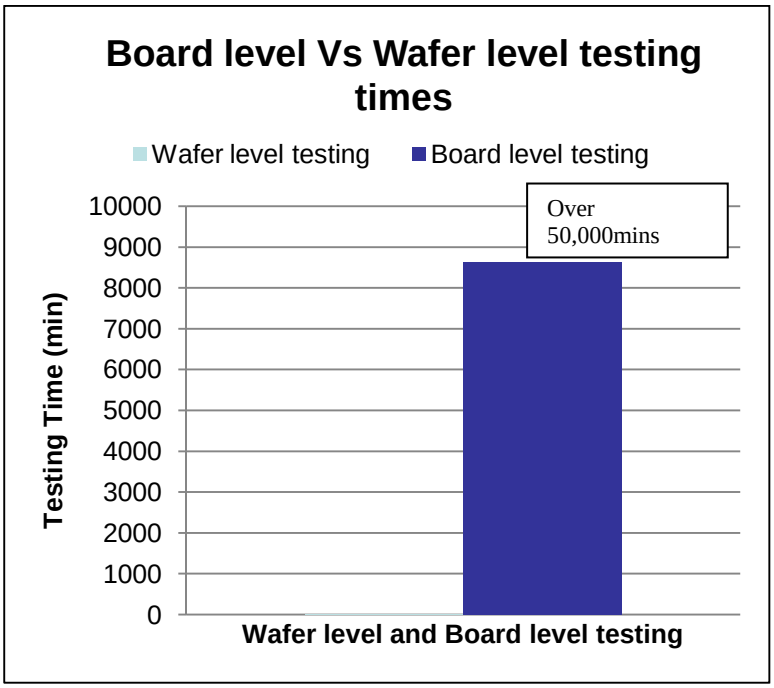


Figure1.10: Comparison of Wafer level testing and Board level test times

1.5 Dissertation outline

In order to understand and correlate the failure mechanisms at the two levels it is essential to understand the structure and also the constitutive models that a solder follows. In Chapter 2 lead free solders have been reviewed, also in chapter 2 a short review of various constitutive and fatigue life predicting models are made. Chapter 3 talks about the literature review of ball shear test. Detailed literature review that talks on the different aspects of ball shear test. In chapter 4 the details of experimental setup is discussed along with the finite element model generation in commercially available software. Chapter 4 also includes the results and discussion of experimental and computational testing of ball shear test. In chapter 5 accelerated thermal cycling performed on wafer level chip scale package is reviewed. Chapter 5 also reviews the publications where some publications were wafer level testing and ball shear testing is compared. In chapter 6 the experimental and computational setup for accelerated thermal cycling are discussed along with the results and discussion. In chapter 7 correlation

coefficients between accelerated thermal cycling and ball shear test are discussed along with empirical correlations that are derived based on the structural parameters at wafer level. Chapter 8 finally concludes the dissertation and suggests ideas for future work.

1.6 Problem Definition

From the above discussion, it is clear that one of the challenges today for electronic packaging industry is to reduce the testing time of board level packages. A methodology that can predict the fatigue reliability of board level packages based on the wafer level ball shear tests, can impact the entire electronic manufacturing industry, from component supplier to equipment manufacturer. The industry is moving forward to wafer level chip scale package which has only one interconnect between the substrate and board and hence this study is possible only on a wafer level package. Figure 1.11 shows the process that was followed in developing this dissertation. In this dissertation three different solder bumps of three different sizes on two different structures is tested and compared with the similar packages mounted on board level. Correlation factors are derived by comparing the shear forces and strains generated during the test. Work done in completing the dissertation is described as follows.

- Wafers are processed using the dedicated processing parameters so that the ball on pad and ball on RDL structures are generated.
- The structures are tested mechanically on a dedicated ball shear testing machine. The ball shears are carried out in zone. The zones are located in center and one of the corners of the wafer to make sure a mechanical integrity of structure is maintained throughout the wafer.

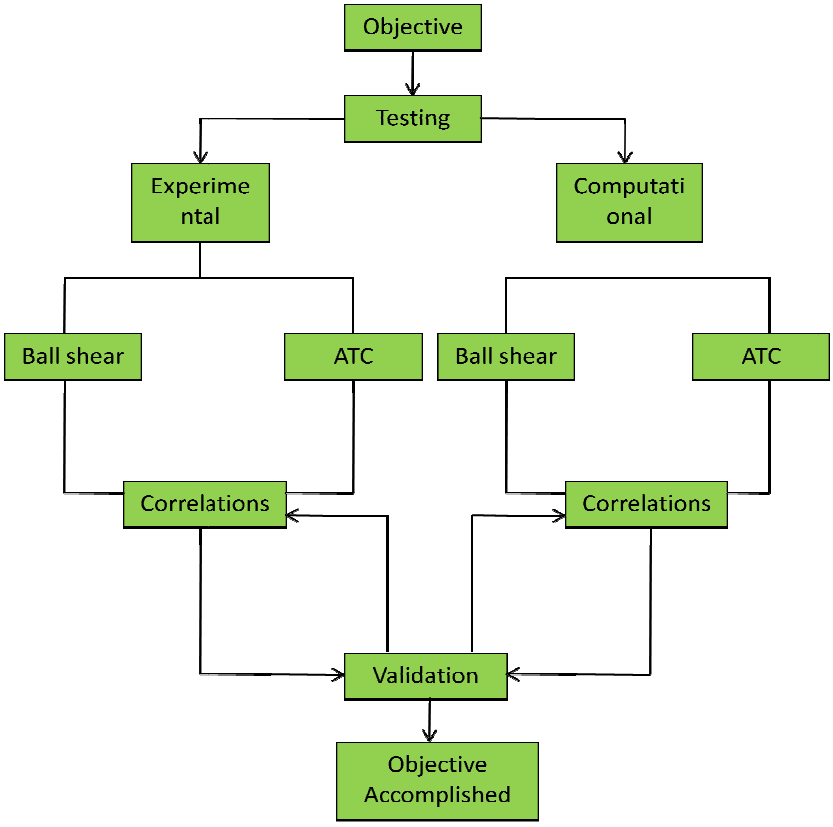


Figure 1.11: Process flow followed in developing this dissertation

- A DOE comprised of two different structures, three different solders and three different sizes is designed and implemented. Ball shear tests are carried out at two heights 25μm and 125μm to make sure that the design is tested in shear as well as a combination of shear and torsion loading. Best leg of the DOE was determined by using Signal/Noise ratio from larger the better option in Taguchi Analysis.
- All the ball shear cases were validated computationally and using the force Vs distance diagram the strain rates for different cases were obtained. shear stress was obtained using the time-history viewer in ANSYS® and compared with experimentally measured forces. Ball shear tests were also carried out at different temperatures using the

temperature dependent material properties that were fed into the multi-linear kinematic hardening model.

- Packages similar to the packages tested in ball shear test are mounted on a standard four layer accelerated thermal cycling boards. The boards are subjected to accelerated thermal cycling based on JEDEC standard JESD22-A104C [9] and weibull plot, along with other failure analysis data was obtained.
- All the accelerated thermal cycling cases are duplicated computationally using a mapped structured mesh. Anand's model was used to model the Viscoplasticity of solder joint considered; anand's model parameters of different solders were obtained through literature. All material properties given as inputs are modeled as temperature dependent properties. The post-processing of all the models was carried out using Darveaux's approach to calculate the crack initiation and crack propagation.
- The shear stress obtained from monotonic loading (ball shear test) and cyclic loading (accelerated thermal cycling) are fed into the Basquin's equation and basquin's coefficients were calculated for different temperatures and for different solder bumps with different solder sizes.
- Number of cycles required to failure occurred in accelerated thermal cycling is calculated based on Basquin's coefficients.
- Best configuration is determined based the studies performed computationally and experimentally.
- Correlation coefficients were drawn using statistical function "CORREL" between different arrays. These correlations are derived based completely on experimental data. The mode of failure obtained in Ball shear test was considered as a metric from monotonic loading. Failure mode is compared with weibull parameter, Number of cycles; solder ball diameter, dielectric thickness and correlation coefficients were derived.

- Trends were established in dimensions, types of solder of wafer level chip scale package structure on wafer level between Number of cycles and Weibull parameter from accelerated thermal cycling which is essentially a board level test.

CHAPTER 2

LITERATURE REVIEW OF LEAD FREE SOLDERS

2.1 Transition from Eutectic Tin Lead to Lead free Solders

The use of solders for establishing interconnection between package and board goes back at least five decades. Consistent reduction in size of electronic packages has resulted in reduction in size of interconnects. Number of interconnect went on increasing with different types of package evolution starting from DIP, QFP and finally to area array packaging following the rent's rule. Demand for decreasing dimensions of packages also prompted development of new technologies such as CSP, FlipChip, WLP etc. The change in interconnect technologies demanded changes in processes and in the dispensing technologies required for their application. For these packages, solder is both the electrical and mechanical interconnect and thus its reliability is one of the most researched studies in electronic packaging industry. In the past, the Sn-Pb system was used almost exclusively in interconnect industry. Sn-Pb system was well understood, well characterized and very forgiving from process engineering point of view. However, in recent years the Sn-Pb system has been under scrutiny due to concerns over lead contamination, pollution in ground water. It is now recognized that use of lead based alloys is an environmental and health problem. As a result of environmental concerns and anxiety over the use of lead based alloys, lead free soldering got introduced as a main stream interconnect technology in the present decade. In Europe, the Waste Electronic and Electrical Equipment (WEEE) and the restriction of hazardous substances (RoHS) directives set resitrictions that consumer electronic equipment must be free by July 1, 2006 [10]. In Asia, the Japanese Ministry of Industry and Trade Institute (MITI) passed a new environmental legislation calling for

a complete elimination of the use of lead by December 31, 2005. These laws kick started the implementation and characterization of different lead free alloy systems in consumer electronic industry. Another equally important issue in lead free development is the trend toward continuous increase in density of interconnects in electronic packages. This, in turn requires finer line circuitry solders with mechanical properties capable of withstanding the increasingly severe demands of miniaturization compared to the eutectic Pb-Sn solder.[11]

2.1.1 Selection of a Lead free Solder

Hossain [8] has a great chapter in his dissertation that reviews the selection process of Lead free solder. The development and selection of any viable lead-free solder is based on different properties such as metallurgical bonding capability, wetting ability during reflow process and metallurgical interactions with bond pad material. Practical factors cover the availability of natural resources, manufacturability, toxicity and cost. Table 2.1 summarizes important properties that are necessary in solder alloy. Over the past decade there has been an increasing number of consensus for using one family of alloys , based on tin, silver and copper, at least for many surface mount and wafer level package applications. The large telecommunication industry is the one that has targeted this alloy. But the choice will still be largely product or applications dependant, when factors such as temperature, compatibility and/or cost may sway the choice towards other alloys. The following alloys are considered representative of viable candidates for replacing eutectic Sn/Pb system. Many of the systems are based on adding a small quantity of third or fourth element to binary alloy systems in order to lower the melting point and increase the wetting and reliability. It is reported that with increasing amount of additive elements, (a) melting point of system decreases, (b) bond strength is affected positively or negatively depending on the amount of element added, and (c) the wettability increases rapidly, reaches the maximum at a particular composition and then a decrease in bond strength may decrease. [13]

Table 2.1: Properties to look for in a new solder [12]

Preferable Properties of solders from DFM	**Preferable properties of solder from solder fatigue**
Low Melting/ liquidus temperature	Electrical Conductivity
Good wettability to Copper/Aluminum	Good thermal Conductivity
Cost	Coefficient of thermal expansion
Environmental Friendliness	Shear Properties
Avaliability and no. of suppliers	Tensile properties
Manufacturability using current processes	Creep Resistance
Ability to be made into balls	Fatigue properties
Copper pick up rate	Corrosion and oxidation resistance
Recyclability	Intermetallic compound formation
Ability to be made into paste	

- Sn 96.5/Ag3.5:

Sn96.5/Ag3.5 (221oC) is considered as one of the most promising alloys and is well researched in the automobile and telecom industry. Indium Corp. reports this alloy to have poorest wetting for reflow solder among high Sn alloys [14].

- Sn/Ag/Cu

Sn/Ag/Cu (SAC) is a ternary eutectic solder alloy system with melting point of around 217^{o}C. Cu is added to the existing Sn-Ag system to get this system of alloys. There are a lot of alloys that are being used in the industry from this alloy system. Some of the early reports about this lab came from International Tin Research institute, Lucent, Ford and Sandia National Labs to have greater fatigue life than the eutectic Sn/Pb alloy. Brite-Euram reported 0.5% Sb addition may strengthen the alloy further. Hossain et.al [15] reported that adding gold increases the

strength considerably in tensile test. SAC alloy system is one of the most popular alloy systems in amongst the lead free alloy systems. Typically SAC 105, SAC 305 and SAC 405 alloys are very popular in consumer electronics, surface mount technology and also wafer level packaging industry. The intermetallics formed in soldering of SAC alloys are Cu_6Sn_5 and Cu_3Sn. These intermetallics are known to be brittle in structure.

- Sn/Ag/Cu/X

Sn96.2/Ag2.5/Cu0.8/Sb0.5 (213-218^oC) is reported by International Tin research institute, Lucent, Ford and Sandia National Labs, to have a greater fatigue life as compared to eutectic Pb/Sn alloy. Brite-Euram project reported that 0.5%Sb addition the alloy further. Sn 97/Sb0.8/Ag0.2 (226oC-228oC, Kester, SAF-A-LLOY) is considered for wave and hand soldering application.

- Sn/Cu/X

Sn99.3/Cu0.7 (227ºC) is reported by Nortel to have soldering quality equal to eutectic Sn/Pb in telephone manufacturing. In air reflow the wettability reduced, fillet exhibits rough and textured apperance. Probably the “poorest” in mechanical properties available from all lead-free solders. Preferably this material is used for wave soldering because low material cost and also inserting of waves not costly. 99.3Sn/0.7Cu is one of the cheapest solders as no silver is present in the solder. This solder is not very complicated as only a binary system of intermetallics is present. It has a low environmental impact and hence does not complicate recycling. One of the major problems associated with this solder is it is difficult to use because for reflowing this solder temperatures as high as 300oC are required. The solder joints formed are dull and they have high incidence of bridging hence not suitable for manufacturing. [16,17]

- Sn/Ag/Cu + XAu

Park et.al [18] reported an increase in strength with the Golde (Au) addition of Sn-Ag-Cu near eutectic alloys. From the thermal and microstructural characterization of Sn-3.8Ag-0.7Cu

alloys containing various amounts of Au, it was found that the Au promotes the formation of a quaternary-eutectic reaction at 204.5℃± 0.3℃.

Kabade and Kim [19] performed four points cyclic bending of the Pb-Sn, SAC and SAC +1.5 Au alloys at 2Hz speed and 0.125” maximum deflection. Figure 8 shows that the SAC + Au solder is more reliable when compared to SAC and Pb-Sn solder. Addition of small weight percentage of Au into SAC, thus improved the four point bending reliability further. Lifetime comparison showed the trend:

SnPb<SAC<1.5 Au-SAC

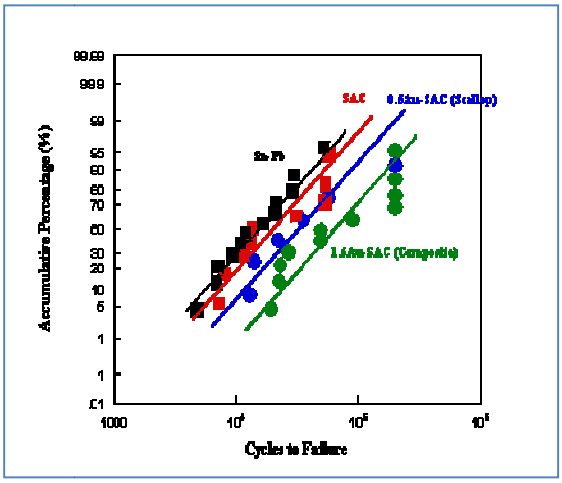


Figure 2.1: Four point bending reliability results of solders [18, 19]

Addition of gold significantly affects the microstructure of solder as was described by Kim et al [8]. Fig 9 shows comparison of SAC solder Vs SAC solder with gold addition. These SEM were taken after the reflow process at 260^{o}C for 3 min.

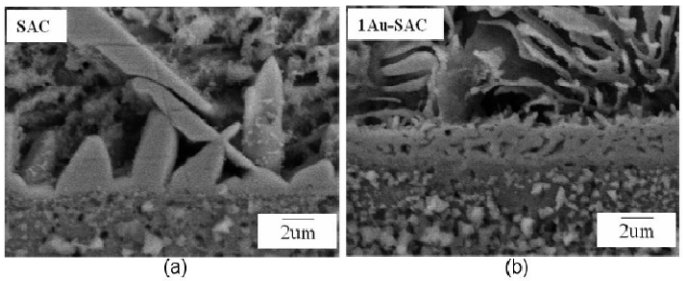


Figure 2.2: Comparison of SEM's for (a) SAC Solder and (b) SAC solder with gold addition [19,20]

Figure 2.2 (a) shows the solder joint with SAC alloy showing well-documented morphology of the Cu_6Sn_5 interface microstructure, a consistent observation that the first phase formed at the Cu interface is Cu_6Sn_5 when the Cu substrate is reacts with Sn bearing alloys. With further reaction a few Cu_6Sn_5 grains preferentially grow to produce scallops. Figure 2 (b) depicts a completely different story. The interface microstructure of 1.0 Au-SAC and 2.0 Au-SAC alloys show completely different interface microstructures; interface phase, $(Au_xCu_{1-x})_6Sn_5$ does not show the same scallop formation. Rather, the $(AuCu)_6Sn_5$ shows grains with finely dispersed pores. Hossain et.al performed tensile testing of SnAgCu alloy with gold addition on a dog bone type of sample and reported that with addition of gold the tensile strength of gold increases by as much as 1.5 times.

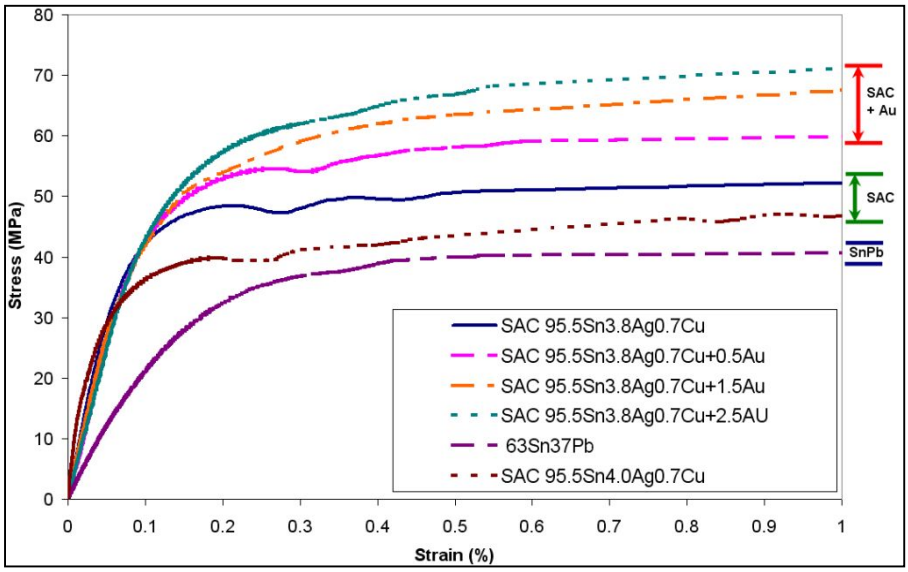


Figure 2.3: Tensile stress-strain curves of SAC alloy with Gold addition [21]

- Sn/Ag/Cu/X

Addition of upto 0.05% Nickel (Ni) in the SAC solder completely changes the metallurgical structure of the alloy. Nickel is a well known diffusion barrier between Copper and Tin. Nickel atoms reduce the rate of reaction for the formation of Cu_6Sn_5 and instead Ni_6Sn_5 is formed which is much stronger intermetallic. Hence typically devices with SAC+Ni solders perform better in accelerated tests as compared to the regular SAC alloys.

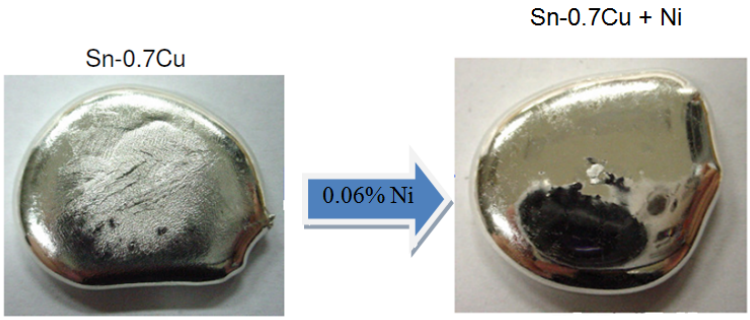


Figure 2.4: Rheological changes that happen because of addition of Nickel to lead free alloy [76]

Thus additions of foreign materials in lead free solders can definitely help improving the properties of solders. However, a judicious of foreign material and the quantity to be is

necessary is necessary because excess addition can prove to be detrimental for reliability of the solder interconnects.

2.2 Constitutive properties of solder

Accurate prediction of fatigue life of solder bumps is important for safe and reliable operation of all electronic equipment. It takes a lot of time and can cost thousands of dollars to design and test a prototype using traditional methods, which in turn slows down the entire product development. The advantage of using software tools is that their post processing capabilities make it possible to visualize the stresses and strains that are imposed in the system due to testing conditions. Current commercial software provides a very powerful method for carrying out thermo-mechanical simulations. However it is important to understand the physics behind the software. In this section, constitutive properties of materials will be discussed. As this dissertation involves plasticity dominated failures and fatigue dominated failures we will be talking about both types of loading and material behavior in both the loadings.

2.2.1 Solder Constitutive behavior

Solder stress/strain behavior is traditionally divided into three parts: elastic strain, plastic time independent plastic strain and time depended creep strain. Solder is a ductile material and hence it plastically deforms and even creeps under the action of force. The force is temperature for accelerated thermal cycling. Creep is the slow deformation of a material under elastic stress (less than the yield stress) that results in a permanent change in shape, and even failure. Although creep can occur at any temperature, it is significant at temperatures exceeding about one half of the melting temperature of the solder alloy. A constitutive equation describes the stress strain relation in the materials involved in testing. Constitutive equation can be derived by testing solders under different loadings and different temperatures. The finite element method analysis requires a valid constitutive (stress, strain and strain rate) equations

and damage criteria. Based on the stress strain relation of a solder joint determined from the constitutive equation by finite element simulation, a FEM model is constructed to find out the maximum stresses induced in case of a plasticity dominated failure or to predict the fatigue life in case of a fatigue dominated failure. The stress strain behavior for engineering materials is complicated and depends generally on temperature, strain and strain rate [8]. The total strain induced in solder is typically is the sum of three portions

$$\varepsilon_{tot} = \varepsilon_{el} + \varepsilon_{pl} + \varepsilon_{cr} \quad 2.1$$

In the next section details of elastic, plastic and creep strains are discussed in one dimensional term. As described in equation (total strain) the strain induced in the solder can be divided into elastic strain, plastic strain and creep strain. Stress induced in a material is material's response of the applied strain. The same equation in terms of different stresses can be expressed as

2.2 $$\varepsilon_{total}(t) = \frac{\sigma}{E(T)} + \left[\frac{\sigma}{K(T)}\right]^{\frac{1}{n_p(T)}} + tA(\sigma)^{\frac{1}{n_c}} e^{\frac{-Q}{RT}} \quad 2.2$$

Mechanical constitutive behavior describes the deformation of a material in response to an applied load. In order to evaluate isothermal mechanical and thermo-mechanical reliability of lead free solders, their constitutive properties need to be understood. In this chapter a literature review of different types of methods used to characterize the materials. Reliability of SAC solders can be best analyzed using strain controlled tests. In general, the mechanics community divides the different constitutive approaches in two categories namely (a) Partitioned Constitutive models and (b) Unified plasticity models. In case of Partitioned constitutive models the inelastic deformations are divided into two categories plastic and creep. Plastic being the time independent plastic deformations and creep being the time dependent constitutive deformations however, both the type of deformations are temperature dependent. The Unified constitutive model differentiates between elastic deformations and inelastic deformations but integrates the creep and plastic deformations into a single inelastic term which is expressed in

terms of internal state variables. In the next section we describe partitioned constitutive models and unified constitutive models [8].

2.3 Partitioned Constitutive Model

In this section elastic, plastic and creep strain are their calculations are discussed.

2.3.1 Elastic Strain

Elastic strain follows the hook's law wherein the strain induced in the solder is a function of stress applied and Young's modulus. Equation gives the equation describing the elastic strain.

$$\varepsilon_{el} = \frac{\sigma}{E} \qquad 2.3$$

Where σ is the applied stress in MPa, and E is the young's modulus in MPa. For solders Young's Modulus typically a temperature dependent property. Young's modulus of a solder is has been traditionally represented at various temperatures by the following equation.

$$E(T) = E_o - E_T(T) \qquad 2.4$$

Where T is the temperature, E_o is the modulus at 0°C and E_T is the temperature dependent value of young's modulus. For most solders the young's modulus also rightly called as elastic modulus is temperature and strain dependent. Hossain [8] in his dissertation compared stress strain behavior of Sn95.5 Ag3.8Cu0.7 alloys at different temperatures. The tests were done in displacement mode and at different temperatures.

Figures 2.5 – 2.8 show the material behavior of Sn95.5 Ag3.8Cu0.7solder as a function of temperature. It can be seem from figures that the yield stress (at which the material starts deforming inelastically) keeps on decreasing as the test temperature is increased. Tests were done at 25C, 75C, 125C and 150C and the yield stress recorded was 48MPa, 33MPa, 28MPa and 16MPa respectively.

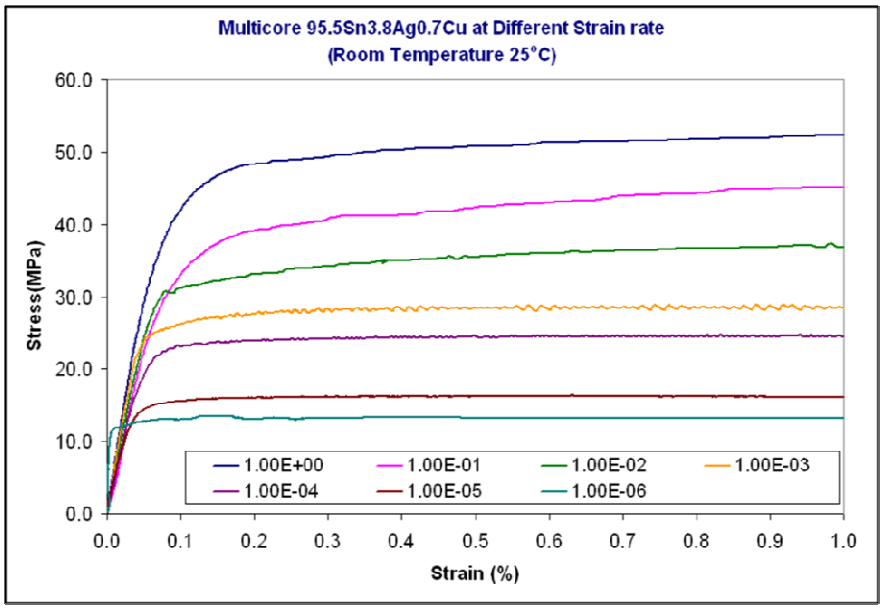


Figure 2.5: Stress – Strain behavior of SAC 3807 alloy at different strain rates at 25°C [77]

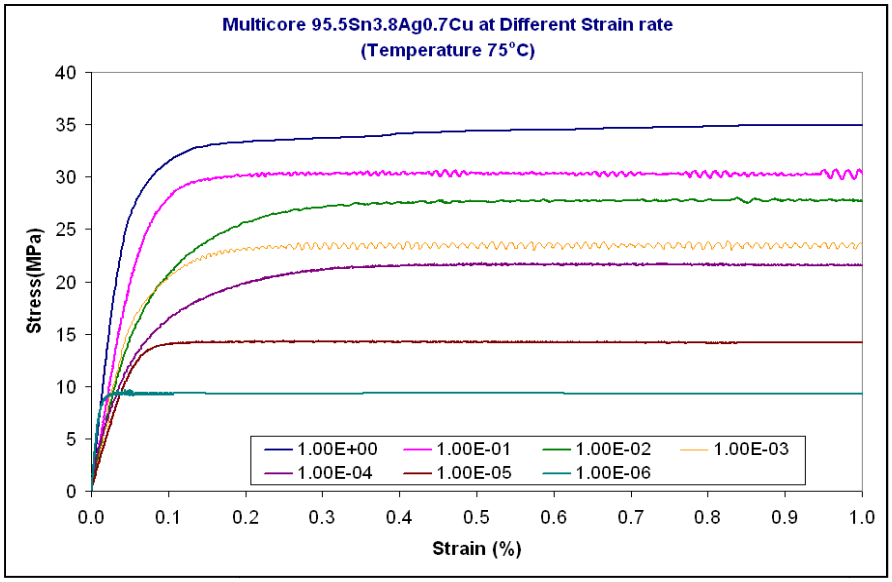


Figure 2.6: Stress- Strain behavior of SAC 3807 alloy at different strain rates at 75ºC [77]

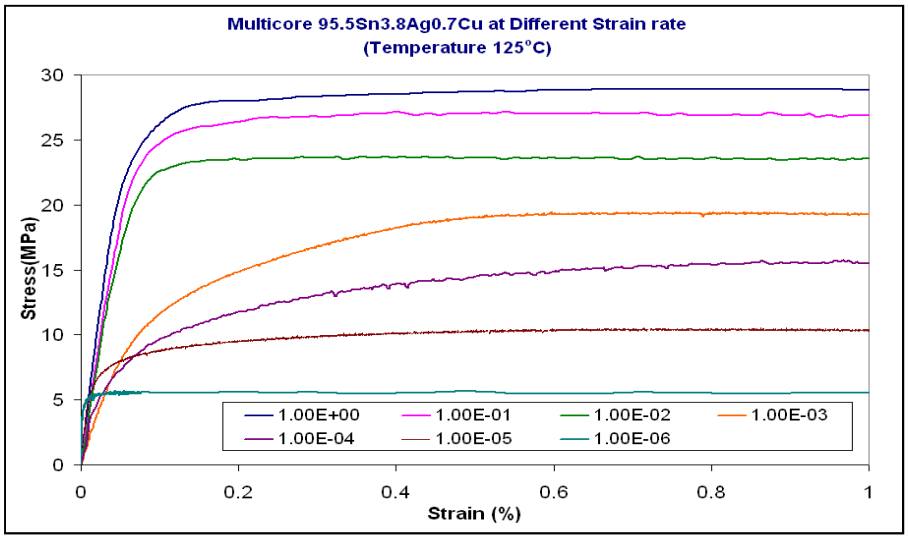


Figure 2.7: Stress- Strain behavior of SAC 3807 alloy at different strain rates at 125ºC [77]

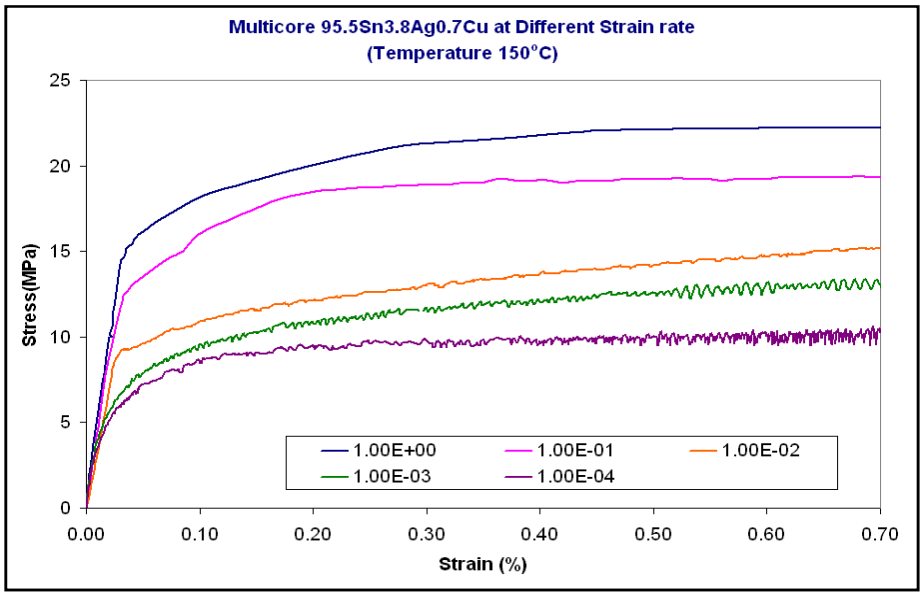


Figure 2.8: Stress- Strain behavior of SAC 3807 alloy at different strain rates at 150ºC [77]

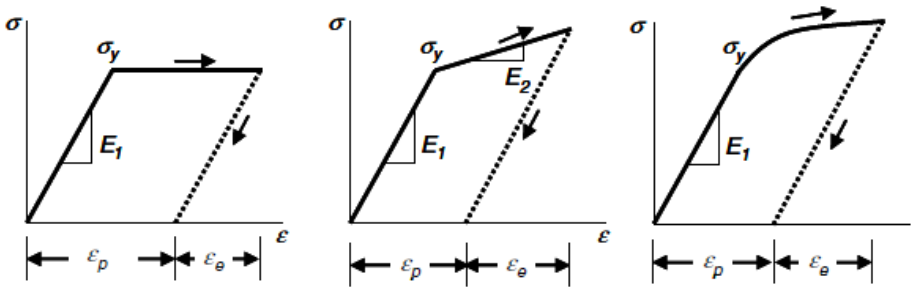
Thus, it can be observed that young's modulus varies with temperature. Variation of young's modulus with temperature has been well documented in literature. Table 2.2 shows the effect of temperature on young's modulus as reported by investigators.

Table 2.2: Comparison of various Young's modulus reported in literature

Number	Researcher	Solder	Young's Modulus (MPa)
1	Vianco [23]	Sn3.9Ag0.6Cu	53000-80T
2	Darveaux [24]	Sn3.5Ag	103735-188T
3	Schubert [25]	SnAgCu	61251-58.5T
4	Zhang [26]	Sn3.9Ag0.6Cu	24224-0.0206T
5	Morris [27]	Sn3.0Ag0.5Cu	74419-110T
6	Wiese [28]	Sn4.0Ag0.5Cu	59533-66.66T
7	Hossain [8]	Sn3.8Ag0.7Cu	75842-152T

2.3.2 Plastic Strain

Plastic strain is a time independent non-recoverable deformation that happens typically due to dislocation pileups from lattice defects. As a material is loaded up to a specified strain level, the stress increases linearly until it reaches the yield stress at which plastic deformation begins to occur. Generally the stress-strain behavior of materials is modeled in three ways (i) perfectly elastic (ii) elastic linear hardening and c) Non-linear Hardening. Figure 2.9 shows stress strain behavior of all three methods.



(a) (b) (c)

Figure 2.9: Types of modeling plasticity (a) perfectly elastic (b) elastic linear hardening and (c) non-linear hardening. [29]

Solder plasticity is best modeled with a non-linear hardening model during loading as shown in figure c. Time independent plasticity is typically modeled using a power law which in which stress is an exponential function of strain. It is known typically as exponential hardening model. Where σ is the equivalent stress, K is a pre-exponential factor, n is plastic

$$\sigma = K\left(\varepsilon_p\right)^n \tag{2.5}$$

strain hardening exponent. Typically both K and n are temperature dependent constants. The plastic behavior of solder is temperature dependent, specifically the yield stress σ.

The point at which yielding occurs when the loading is reversed is also interesting. There are two main models that specify the point at which the reverse yielding occurs, linear isotropic hardening model and multi-linear kinematic hardening (MKIN). The difference between the two is shown in figure 2.10. The multi-linear kinematic hardening model can capture bauschinger effect [30]. Bauschinger effect is observed in all ductile metals [31, 32]. In commercially available finite element codes Multi-linear kinematic hardening model use the Besseling model or sublayer model, so that the bauschinger effect is included. KINH (kinematic hardening model) also allows more number of points to be defined for each stress strain curves at different temperatures. These properties of the model come very handy when performing a ball shear type of analysis at different temperatures hence, in this dissertation the kinematic hardening model is used. In this study three points were used to define the material behavior of SAC 305 and SAC 405 solders. The three data points were taken at 0.001, 0.002 and 0.01 strain rates respectively. Temperature dependent material properties of various solders were calculated from temperature dependent elastic modulus and strain rates considered.

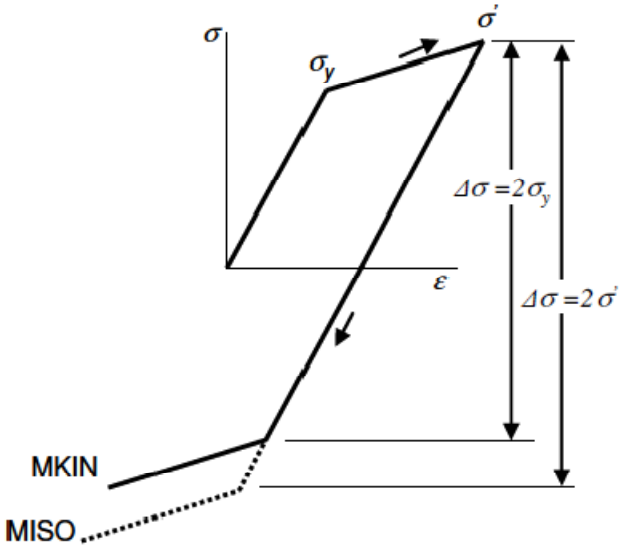


Figure 2.10: Bauschinger effect captured by Multi-linear kinematic hardening model [29]

2.4 Unified Constitutive Model/ Anand Constitutive model

Haswell et.al [33] talks about an experimental evidence of inherent rate-dependency and creep-plasticity interactions on structural alloys at elevated temperatures, which implied that the inelastic deformation was controlled by a single overall mechanism and this, could be treated in a unified manner. The time-independent plastic deformation arise from the same fundamental mechanism of dislocation motion. Hence, a constitutive model which captures both of these mechanisms is desirable. Such a constitutive model is referred to as a unified plasticity model. A commonly used unified plasticity model is the Anand' model. Anand's model was initially formulated for the metal hot working process to simulate large visco-plastic deformations at extremely high temperatures [Dongkai Shannguan Lead free interconnect reliability]. A simple set of constitutive equations for large, isotropic, viscoplastic deformations at extremely high temperatures. A simple constitutive equations for large, isotropic deformations but small elastic deformations is the single scalar internal variable model proposed by Anand and Brown. There are two basic characteristics of Anand's model. First no explicit yield criterion is specified, and

second a single internal state variable (ISV) s, deformation resistance, represents the isotropic resistance to elastic strain hardening. Anand's model can represent the strain rate and temperature sensitivity, strain rate history effects, strain hardening and restoration process of dynamic recovery. Equation 2.6 shows the functional form of the flow equation that accommodates the strain rate dependence on the stress:

$$\dot{\varepsilon}_p = Ae^{-\left(Q/RT\right)}\left[\sinh\left(\xi\frac{\sigma}{s}\right)^{1/m}\right] \qquad 2.6$$

Where ε_p is the inelastic strain rate, A is the pre-exponential factor, Q is the activation energy, m is the strain rate sensitivity, ξ is the multiplier of stress, R is the gas constant and T is the absolute temperature. The ISV enters the flow equation only as a ratio with the equivalent stress. The evolution for the internal state variable s is given by

$$\dot{s} = h\left(\tilde{\sigma}, s, T\right)\dot{\varepsilon}_p - r\left(s, T\right) \qquad 2.7$$

Where h(σ,s,T) is associated with dynamic strain hardening and recovery processes, while static recovery is accommodated through the function r(s,T). however, load-unload and hold-reload test results showed that the contribution f the static recovery for the solder is negligible. The hardening function has the following form:

$$h = h_0\left|1-\frac{s}{s^*}\right|^a sign\left(1-\frac{s}{s^*}\right), a \geq 1 \qquad 2.8$$

Where h_0 and a are material parameters representing the strain hardening, s* means the saturation values of s.

From (2.6) and (2.7) we obtain

$$\dot{s} = \left\{h_0\left|1-\frac{s}{s}\right|^a sign\left(1-\frac{s}{s^*}\right)\right\}\dot{\varepsilon}_p \qquad 2.9$$

Where

$$s^* = \tilde{s}\left[\frac{\dot{\varepsilon}^p}{A}\exp\left(\frac{Q}{RT}\right)\right]^n \qquad 2.10$$

From the above three equations we obtain

$$\sigma^* = \frac{\tilde{s}}{\xi}\left[\frac{\dot{\varepsilon}^p}{A}\exp\left(\frac{Q}{RT}\right)\right]^n \sinh^{-1}\left[\left(\frac{\dot{\varepsilon}^p}{A}\exp\left(\frac{Q}{RT}\right)\right)^m\right] \qquad 2.11$$

The above equation to the saturation stress, temperature, and strain rate. For isothermal, and s*>s conditions

$$\frac{d\sigma}{d\varepsilon^p} = ch_o\left|1-\frac{\sigma}{\sigma^*}\right|^a sign\left(1-\frac{\sigma}{\sigma^*}\right), a \geq 1 \qquad 2.12$$

The integration form of 2.11 is

$$\tilde{\sigma} = \tilde{\sigma}^* - \left[\left(\tilde{\sigma}^* - \tilde{\sigma}_o\right)^{(1-a)} + (a-1)\left\{\left(ch_o\right)\left(\tilde{\sigma}^*\right)^{-a}\right\}\varepsilon_p\right]^{\frac{1}{(1-a)}}; a \neq 1 \qquad 2.13$$

Where σo=cso and so is the initial value of s. for a=1 equation 9 integrates to the classical vocce equation. Material parameters will be determined by 2.13 [35].

The material parameters that should be determined in these constitutive equations are A,Q,m,n,ζ,ŝ,a,ho and so. This unified Viscoplastic isotropic hardening model describes the rate-dependent inelastic deformation characteristic of the material (creep behavior), but it disregards an explicit yield point and time independent plastic deformation. It uses nine material parameters to describe strain rate as a function of applied stress, the material deformation resistance and of the temperature. On the other hand, the deformation resistance of the material depends on the strain rate value due to strain hardening and strain softening effects. This leads to a recursive formulation of the equation system, which is made up of the strain rate equation and the evaluation for the deformation resistance. The interrelationship of these equations can be seen in figure 2.4.

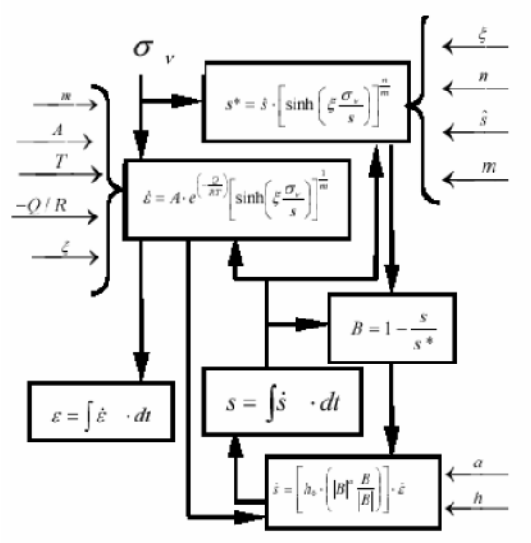


Figure 2.11: Interrelationship between the set of equations in ANAND's model [35]

Anand's model has been extensively used by a number of researchers and that too on different types of solders. Table 2.3 shows compilation of a few researchers who have derived anand's model and have implemented it on various solders. The material constitutive model plays an important role in development of finite element models for microelectronic packaging assembly. Under thermo-mechanical loading, solder alloy undergoes elastic and inelastic deformation. Elastic deformation is recoverable, while inelastic deformation, consisting of time-independent and time-dependent creep deformation is not recoverable. The constitutive behavior can be represented by a combination of elastic, plastic (isotropic or kinematic hardening) viscoelastic, Viscoplastic/creep models. The use of accelerated tests to characterize thermo-mechanical reliability of electronic packages is very well established.

Table 2.3: Comparison of Anand's parameters obtained by different researchers

No.	Material Constants	Sn-3.5Ag [37]	Sn-40Pb [37]	Amagai Sn 3.5Ag 0.7Cu [38]	Reinai-kenen Sn2.0Ag 0.5Cu [39]	Hossain Sn3.8 Ag 0.7Cu [40]	Sn1.0 Ag 0.5Cu [38]	Sn3.0 Ag 0.5Cu [40]	Sn4.0 Ag 0.5Cu [41]
1	A (s-1)	$1.49x10^{7}$	$1.49x10^{7}$	$4.61x10^{6}$	500	$1.77x10^{5}$	$2.42x10^{7}$	5870	325
2	Q/R	10830	8900	8400	8500	1.03e4	8400	7460	10561
3	α	11	6	0.038	4.3	4e6	0.043	2	10
4	M	0.303	0.182	0.162	0.16	1.3976	0.168	0.0945	0.32
5	S	80.42	73.81	1.04	28.7	48.65	1.005	58.3	42
6	N	0.0231	0.018	0.0046	0.03	0.0094	$8.1x10^{-4}$	0.015	0.02
7	h_o	2640.75	3321.15	3090	6100	4950	3162	9350	80e5
8	A	1.34	1.82	1.56	1.59	1.3	1.59	1.5	2.57

According to the fundamental mechanism that is viewed as being responsible for inducing damage, the models proposed for predicting fatigue life of solder joints can be divided into five major categories: (a) Stress based, (b) plastic strain based, (c) Creep strain based, (d) Energy based and (e) Damage accumulation based []. Non-linear octagonal model are used with ANSYS finite element solver.

2.5 Fatigue Life Prediction models

2.5.1 Stress based models

Stress based models are very good in predicting high cycle fatigue. Typically the fatigue is classified as high cycle fatigue when the cycles to typically are around 10^{6},[42] in electronic packaging industry on an average the typical fatigue life of solder materials ranges from 500 cycles to 3500 cycles depending on the type of loading, type of material and the experimental conditions. Hence in the field of electronic packaging most use of strain based models is almost unanimously accepted.

2.5.2 Strain Based models

Among the strain based models, the Coffin-Manson model, the Solomon model and the Engelmaier model are widely used. It can be observed from literature that each of these models is an empirical relationship between cycles-to-failure, and analytically, numerically or experimentally determined plastic shear strain range per cycle.

2.5.2.1 Coffin-Manson Model

Coffin-Manson model is one of the most famous models to determine the number of cycles to failure, denoted by Nf, is related to plastic strain range per cycle, Δεp, through a power law with

$$N_f = \frac{1}{2}\left[\frac{\Delta\gamma}{2\gamma_f'}\right]^{\frac{1}{c}} \qquad 2.14$$

Where N_f is the number of cycles to failure, the shear strain Δγ[43] . Englemair observes that Δγ should be taken as potential shear strain range at complete stress relaxation. γ_f '=0.325 is called as the fatigue ductility coefficient in shear for solder material. In fact the basic coffin manson equation is modified in so far as the fatigue ductility exponent c depends on the frequency of cyclic loading (dwell times at high temperature)

$$c = -0.442 - 6.10^{-4} T_{mean}\left[^{o}C\right] + 1.76.10^{-2} \ln(1 + 360/t_{highdwell}\left[\min\right]$$

Where Tmean is the mean temperature of solder during a cycle, and thigh dwell is the duration of the high temperature dwell. Coffin manson equation is surely the easiest approach since the potential strain range at complete stress relaxation may be simply from a purely elastic model. The expression of the creep ductility exponent c accounts for the actual stress relaxation. Coffin-Manson equation is essentially a uniaxial criterion. From [44] a phenomenological expression of the potential shear strain range at complete stress relaxation can be given as

$$\Delta\gamma = \frac{\Delta u}{h} \text{ Where } \Delta u/2 \qquad 2.16$$

is the relative displacement amplitude in shear and h, where h is the height of solder joint. However, the equation may be also used with multiaxial loadings, like simultaneous shearing and traction/compression, and even with non-proportional loadings. The passage to multiaxiality is quite a delicate subject and very few articles from electronics deal with this question. A priori, it would be easy to take the range of the equivalent strain, but this approach is not entirely correct. To correct the this approach one of the approaches that can alter is the use of strain range tensor and is used in [45].

$$\Delta\varepsilon_{eq} = \frac{1}{(1+\nu^{in})\sqrt{2}}\left[\Delta(\varepsilon_{11}-\varepsilon_{22})^2 + \Delta(\varepsilon_{11}-\varepsilon_{33})^2 + \Delta(\varepsilon_{33}-\varepsilon_{11})^2 + 6\Delta\varepsilon^2{}_{12} + 6\Delta\varepsilon_{23}^2 + 6\Delta\varepsilon_{31}^2\right]^{\frac{1}{2}} \quad 2.17$$

Where the Δ's represent variations of the strain tensor εij over a whole cycle. The equivalent strain range must be multiplied by√3 in order to get the equivalent strain range to be used in coffin-manson equation.

2.5.2.2 Strain rate partitioning model

Strain range partioning uses essentially the same concept as strain range method. It indends to differentiate the damage caused by rapid loading and unloading and damage caused during the dwells (creep and stress relaxation). According to the strain range partiioning model a single load cycle can be divided into four sub cycles as described below:

1. Plastic damage in one sub-cycle, plastic damage in other sub-cycle (pp).
2. Plastic damage in one sub-cycle, creep damage in other sub-cycle (pc).
3. Creep damage in one sub-cycle, plastic damage in other sub-cycle (cp)
4. Creep damage in one sub-cycle, creep damage in other sub-cycle (cc)

After the inelastic strain range has been partitioned into

$$\Delta\gamma_{in} = \Delta\gamma_{pp} + \Delta\gamma_{pc} + \Delta\gamma_{cp} + \Delta\gamma_{cc} \quad 2.18$$

The median cyclic fatigue life can be calculated by linear damage accumulation as expressed in the equation[46-47].

$$\frac{1}{N_f} = \frac{1}{N_{pp}}\frac{\Delta\gamma_{pp}}{\Delta\gamma_{in}} + \frac{1}{N_{pc}}\frac{\Delta\gamma_{pc}}{\Delta\gamma_{in}} + \frac{1}{N_{cp}}\frac{\Delta\gamma_{cp}}{\Delta\gamma_{in}} + \frac{1}{N_{cc}}\frac{\Delta\gamma_{cc}}{\Delta\gamma_{in}} \qquad 2.19$$

In case of 60Sn40Pb solder alloy, some data can be found in literature that gives properties of the pp and pc data. Overall, the problem with strange range partioning model is that the properties of pp,pc,cp and cc are difficult to obtain and even more difficult to be found in literature. [48,49]

$$N_{cc} = \frac{1}{2}\left(\frac{1}{1.25}\frac{\Delta\gamma_{cc}}{2}\right)^{-1} \qquad 2.20$$

$$N_{pp} = \frac{1}{2}\left(\frac{1}{1.4}\frac{\Delta\gamma_{pp}}{2}\right)^{-1/0.57} \qquad 2.21$$

A general observation is that englemair's fatigue ductility coefficient lies between pp and cc exponents. The distinction between plastic strain and creep strain can be difficult to determine because they both are plastic deformations. In fact, the choice of the constitutive model plays a very important role in determining creep in the given deformation. Some models whereas make an explicit partition of the inelastic strain into time independent deformation and time dependent deformation. Some models even implement different constitutive models for ramps and dwells which result into either pure plasticity or pure creep. Strain range partitioning is one such model it has a term for all the different parts of a given accelerated thermal cycle. Overall summary of the strain range partioning (SRP) approach gives us the liberty to calculate pure plasticity and pure creep in any given solder but its difficult to implement due to lack of

data. The values of material constants in different axes of loading are very difficult to find and hence SRP apprach is stictly uniaxial and not multi-axial.

2.5.2.3 Energy Criterion

Energy criteria are intrinsically multiaxial. Simiarly to the strain range criteriaon. An energy regime criterion expreses the mean cyclic fatigue life as a power function of the visco-plastic energy density per cycle. ΔWave (homogenous to J/m3). In darveaux's approach, the expression of mean cyclic fatigue life has two terms, the first for crack initiation and the next is for crack propagation. Typically crack initiation takes approximately 10% of the total fatigue life. Equation 2.21 gives the expression for fatigue life for eutectic tin lead solder.

$$N_f = C_3\left(\frac{\Delta W_{ave}}{U_{ref}}\right)^{C_4} + \frac{a}{C_5}\left(\frac{\Delta W_{ave}}{U_{ref}}\right)^{-C_6} \qquad 2.22$$

ΔW_{ave} is averaged along the interface where the crack propagates, over a given arbitrary thickness a, is the diameter of solder joint, thus the length of crack at the rupture [48]. Even though the expression distinguishes crack initiation and propagation, this isnt a real rupture mechanical approach. Unfortunately, this criterion depends on the arbitrary thickness over which average is made. This condition presents can create a big confustion for a modeler who is trying to use darveaux's approach to determine the fatigue life. If the viscoplastic energy desnsity is averaged over the entire solder bump then the value of the fatigue life can be off by as much as 50%. Hence for all the modelers it is extremely important to have a grid sensitivity analysis of solution done before publishing the fatigue life predictions. The procedure followed in calculating the fatigue life using Darveaux's method is expressed in the flow chart as explained in figure. Figures 2.12 show the methodology of solder joint fatigue life prediction method.

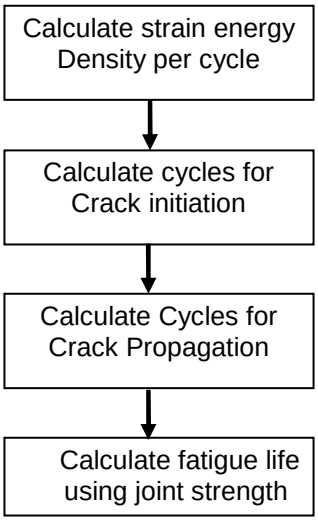


Figure 2.12: Flow chart for implementing Darveaux's approach [50]

The strain energy of each element is normalized by the volume of the element. Equation gives the formula for calculating the viscoplasitc strain energy density accumulated per cycle for the interface elements. ΔW is the average viscoplastic strain energy density accumulated per cycle for each element, and V is the volume of each element.

$$\Delta W_{avg} = \frac{\sum \Delta W * \upsilon}{\sum V} \qquad 2.23$$

2.5.2.4 Energy partitioning approach

The energy partioning approach method is applicable to strain partioned constituve models where elastic, plastic and creep energies can be distinguished. In the case of unified visco-plastic model, difficulties arise because creep cannot be seperated from plasticity and hence from inelastic strain. The basic assumption of the criterion is that dameage is caused

$$U_e = U_o N_{fe}^{\ b}$$
$$W_P = W_{po} N^{c'}{}_{fp} \qquad 2.24$$
$$W_c = W_{co} N^{d'}{}_{fc}$$

independently by elastic strain (high cycle fatigue) by plastic energy dissipation and by creep energy dissipation (low cycle fatigue including theral cycling). Elastic energy density range in a cycle is given by

The median cycle fatigue life is given by linear damage accumulation (Miner's Rule)

$$\frac{1}{N_f(50\%)} = \frac{1}{N_{fe}} + \frac{1}{N_{fp}} + \frac{1}{N_{fc}} \qquad 2.25$$

$$= \left(\frac{U_e}{U_o}\right)^{1/b'} + \left(\frac{W_p}{W_{po}}\right)^{1/c'} + \left(\frac{W_c}{W_{co}}\right)^{1/d'} \qquad 2.26$$

The values of the constants for eutectic Sn-Pb solder are Uo=0.698MPa, Wpo=32.4MPa, Wco=94MPa, b'=-0.18, c'=-0.47 and d'=-1. This criteria is multi-axial.

2.5.2.5 Clech's (SRS) model

Solder Reliability solutions (SRS) and its application to surface mount array and chp scale assemblies. The highlights of clech's model are

- Bending and stretching of parts (board and component) is accounted for in the case of leadless assemblies. These effects are important for leadless assemblies. These effects are important for leadless area-array plastic packages and CSPs where the important flexural compliance, which depends on the package contents and construction, can provide for stress and strain relief in the solder joints.
- Inelastic strain energy is from complete hysteresis loops with different dwell times on the hot and cold sides of thermal cycles.
- The local mismatch stress/strain response is determined from the combined and simultaneous action from the combined and simultaneous action of solder/board

and solder/lead (or component) CTE and modulus mismatches. The analysis uses a tri-layer model which also accounts for the local effects of board to lead (or component) CTE and modulus mismatches.

- Fatigue life from component test vehicles is correlated on a joint per joint basis.

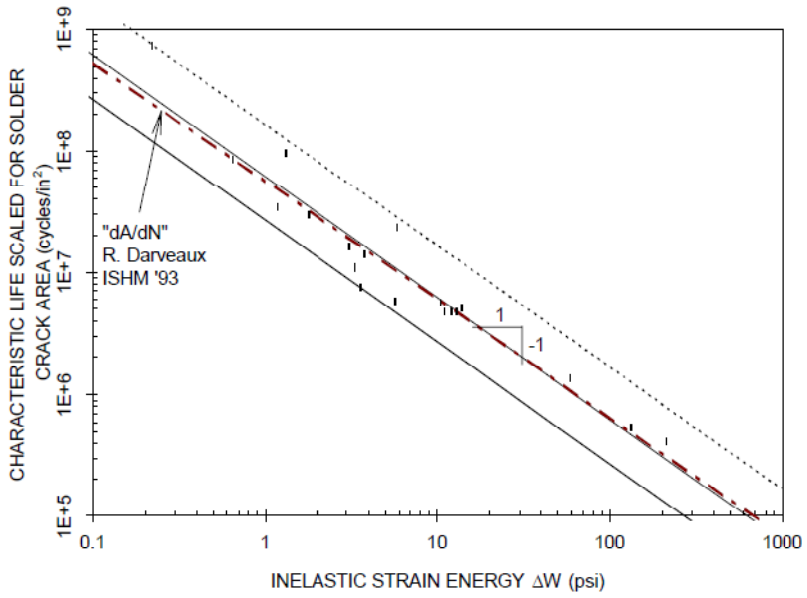


Figure 2.13: Solder Reliability Solutions correlation of accelerated data [51]

$$\frac{\alpha_{jo\,\mathrm{int}}}{A} = \frac{6.149 * 10^{7} * C}{\Delta W^{0.998}} \qquad 2.27$$

Where:

- α_{JOINT} (cycles) is the characteristic life or cycles to 63.2% failures in the joint population.
- A (in^2) is the solder crack area for fully cracked, electronically open solder joints (also the minimum solder joint load bearing area).
- ΔW ($lb.in/in^3$ or psi) is the cyclic inelastic strain energy per unit volume obtained as the sum of strain energies due to global and local CTE mismatches
- C is a model calibration factor. C equals 1 for the centerline of the correlation band, 0.434 for the lower bound, and 2.7 for the upper bound.

The parameter α_{JOINT} /A (with units cycles/in2) is the inverse of an area crack propagation rate (in2/cycle) and is interpreted as the number of cycles it takes for a crack, or several micro-cracks, to propagate through a unit solder attach area. The least squares goodness –of-fit correlation coefficient for the data in figure is 0.965. Scatter is 2.3 times below the centerline and 2.7 times above, which is typical of fatigue and of similar amplitude as in other models. The slope of the life data correlation is about -1, close to those of Darveaux's [52] crack growth model. It can also be seen from figure that a straight line of inverted mean propagation rates (da/dN) from R. Darveaux's crack propagation. The two models are consistent and validate one another. Clech [51] has applied the solder reliability solutions to various types of packages including Alloy 42 and Cu TSOPS, PBGA assemblies, Chip Scale Package applications and Flip Chip Assemblies. The SRS model has been implemented as a PC-based design for reliability tool which streamlines the assembly reliability assessment process. The tool consists of

- A pre-processor for input of component, substrate, assembly, thermal profiles, design life and statistical parameters, and component specific stiffness and CTE calculations.
- An analysis module to compute hysteresis loops.
- A post-processor to examine stress/strain plots and life prediction results.

Solder Reliability Solutions (SRS) is a property of EPSI Inc.

2.6 What's the right model to use?

Choosing the right model for analysis and post processing of data is extremely important for getting the right results and duplicating the correct failure mode computationally. Fatigue life prediction of lead free packages under mechanical and thermo-mechanical loading is a major concern and has driven research efforts to develop computational models for different packages in order to improve design that are capable of failure initiation and propagation under different fatigue loads. Typically, the reliability problem is approached using a combination of experimental measurements and numerical simulations. As mentioned in chapter 1, in this

dissertation accelerated thermal cycling and ball shear test are performed separately. Ball shear test is essentially a plasticity dominated test. The time spent in the actual test is very less and hence there is no chance of having creep strain inducted in the solder during the test. Hence, a multi-linear kinematic hardening model is used for modeling ball shear tests. In this study solder was assumed visco-plastic and hence it was meshed with visco-plastic elements. In ANSYS visco-plasticity is solved using ANAND's model and hence it was used. Darveaux's approach was used to analyze the results and crack initiation and crack propagation was calculated using the darveaux's constants for an octant model. Next two sections give details about what elements are best compatible with the models selected to simulate the two tests.

2.6.1 Ball shear testing

Ball shear test is considered to be a plasticity dominated test. The model used for ball shear test is Kinematic hardening model. PLANE183 was used to model the solder and other solids. Advantages of using PLANE183 are that it can solve for plasticity and can take body loads as input and gives stresses (principal, equivalent, shear and Von-Misses) and strains as output. Solder's outer surface is modeled using TARGE169 elements. TARGE169 elements overlay themselves describing the boundary of a deformable body. These elements are potentially in contact with the target surface. TARGE 169 can capture any translational or rotational deformation caused by the contact surface. CONTA172 is used to model the point of shear tool that comes in contact with solder. These contact elements work very well with the above selected target elements and body elements.

2.6.2 Accelerated thermal cycling

In case of accelerated thermal cycling SOLID45 was used to model all of the structure except for solder balls. SOLD45 has the ability to solve plasticity, creep, swelling, stiffening, large and small deflections. SOLID45 takes young's modulus, poisson's ratio and CTE as input. Temperature dependent material properties can also be defined. It takes input as temperature and the can give structural stresses and strains as outputs. Solder was modeled using

VISCO107 element. Special features of this element include the ability to solve the rate dependent plasticity (ANAND model). The outputs of element include plastic work and plastic work/volume which are required to cycles to failure using Darveaux's approach.

2.7 Conclusion

The following were the conclusions that can be drawn from chapter 2.

- The migration of electronic industry from eutectic tin-lead to lead free solder was a major shift changed from electronic manufacturing point of view.
- This change kick started a lot of research on lead free solders, deriving their characteristic equations, choosing the best lead free solder amongst a group of lead free solders. In general, there was a feeling in industry that lead-free solder is not as forgiving as tin lead solder.
- A literature review of different lead free solders their characteristic equations, the failure reliability models and how they are modeled using various commercially available finite element analysis software.
- The element types that go with the failure reliability models that were selected for ball shear test and accelerated thermal cycling were selected and appropriate reasoning was discussed.

CHAPTER 3

BALL SHEAR TEST – LITERATURE REVIEW

3.1 What is Ball shear Test

Ball shear test is a widely accepted test method used to assess the integrity of solder ball interconnection in area array packages. Its popularity is because of its ease of implementation and simple concept. In ball shear test, a solder interconnection is sheared using a specialized shear tool. Ball shear test became very popular when DAGE Precision Industries (NASDAQ:NDSN) [53] launched its first ball shear tester and then extended it to cold bump pull for solder bump testing. This shear test became a standard test, and is employed in wafer fabs when JEDEC launched the first standard [54] in the year 2000. Since then, ball shear and ball pull have been researched quite extensively all over the world. In this chapter a brief literature review of ball shear test is presented.

Generating transistors and in turn devices on a silicon wafer is a long and complicated process as discussed in chapter 1. Solder bumping is the last process in wafer fabrication process. Bumping process can be divided into two main processes in the first process a flux is applied to the bump pads using a stencil printing process. After the application of flux the wafer goes to the next equipment where the real bumping happens. In bumping process, solder bumps are pressed against bond pads and then wafer goes through a reflow oven where the solder gets soldered to the bond pad. During soldering, the solder alloy melts and reacts with the pad metallization of the wafer to form IMCs at the interface. In general, when an IMC layer is formed, it is desirable to achieve a reliable metallurgical bond. Excessively thick intermetallic

Layers are very sensitive to stress and can provide sites of crack initiation and paths of propagation. As the inter-metallic layers are brittle a microstructural mismatch exists between the solder and pad metallization. It has been reported in literature that the interface between pad metallization and intermetallic layer is very susceptible to failure [55]. Ball shear test gives a great opportunity to find about the structure before the packages are mounted on board. The two main advantages of this testing methodology are, wafer level testing is cheap and because testing can be done at a very large scale a DOE with lots of legs can be designed to understand issues with processes and process parameters. Wafer level tests can give an inkling of what's going to happen at the board level, trends have been observed and in some cases even correlations between board level accelerated tests and wafer level tests have also been derived [56, 57]. Board level accelerated testing (drop tests and accelerated thermal cycling) is very expensive and time consuming and in turn increase the time to market for products thus having such correlations can certainly help. However, having correlations between wafer level tests and board level tests does not reduce the importance of board level tests. Board level tests are important to determine the failure mechanisms that exist in the board assemblies. Generally speaking, if by using the wafer level correlations even one of the board levels accelerated test runs can be avoided for each of the products launched; it will save lots of money and time in reliability testing.

3.2 How is Ball shear Test performed?

Figure 3.1 describes the mechanism of ball shear test. In a Ball shear test a dedicated ball shear tester is employed to perform the operation. The shear tool has a programmable speed and a shear height which can be changed as per the requirement.

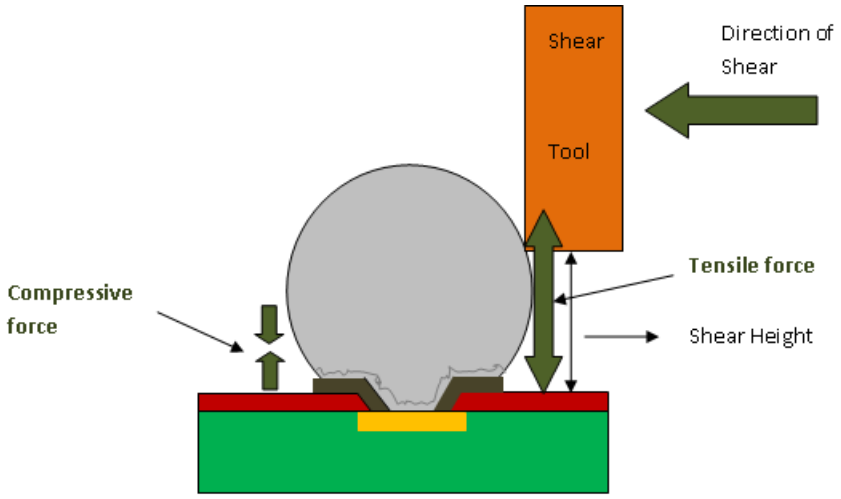


Figure 3.1: Schematic of a Ball shear test

A JEDEC standard JESD22-B117 [54] has been developed for ball shear testing. The following section describes ball shear test procedure and failure modes that are observed in experimental conditions.

3.2.1 Factors affecting ball shear test

In this study, a commercially available ball shear tester is used. The shear tool was positioned in such a way that solder balls are sheared off in a direction parallel to the device planar surface. The device is positioned in such a way that one ball shear test will not damage any other solder bump in its vicinity. Sufficient number of solder balls should be sheared to ensure a statistically valid quantity of parts being verified, and reflects cost/manufacturing constraints. Depending on failure distribution, desired sensitivity, confidence limits and other solder ball sample quantities may be appropriate. Shear force and/or failure modes are known to be sensitive to shear speed, shear tool standoff (shear height) and time between the shear test and the last solder ball reflow. Several researchers have investigated the solder ball shear test over the years. The following are the factors that affect result of solder ball shear test

3.2.1.1 Solder ball composition and effect of Multiple reflows

The solder ball shear strength is a very strong function of the solder ball composition (SnPb, SnAgCu, SnAg,SnAgCu+X) etc. Different solder ball compositions have different intermetallic layer thicknesses. Intermetallic layers essentially join the solder with bond pad. Lee and Huang report that SAC 405 has exhibit better ball shear strength over a wide range of speeds as compared to Sn-Pb solders [57]. Song et.al studied the effect of shear speed ranges from 25μm/s to 500μm/s. it was observed that as speed increases the shear force recorded increases, as observed by song et.al as speed increases from 25 μm/s to 500 μm/s the shear force increases by almost 13% and a similar behavior was exhibited by Sn-Pb solder too. A similar observation was also observed by other investigators [58-61]. In [57] effect of multiple reflows was on solder joint strength was also analyzed. it was noted after 10 reflows in Sn-Ag-Cu alloy grew extensively near the pad structure and formed a planar type structure, which was much more that after one reflow. This type of structure was less thick in case of Sn-Pb solder and hence brittle failure occurrences was more in lead free solders as compared to Tin lead solders. Effect of aging of solder has also been studied. Koo et.al reported studied the effect of aging on two different types of solders namely Sn-37Pb and Sn-3.5Ag and an electroplated Ni/Au BGA substrate. It was observed by Koo et.al that after reflow there was a fine layer or Gold Tin intermetallic alongside the bond pad. As reported by Koo the ball shear strength of solder joint with Sn 37Pb and Sn3.5Ag solders reduced with aging. Number of brittle failure increased significantly as the solder joints were aged and the displacement rate of shear tool increased. Lee and Song [62] reported intermetallic formations are dependent on the surface finish of pad. They reported that with isothermal aging the intermetallic with ENIG and OSP finish increased to 3.5μm and 9 μm repectively. Lee and Song divided the type of failures into four categories namely ductile mode, Quasi-Ductile mode, Quasi Brittle mode and Brittle mode, and it was observed that increase in IMC thickness actually proved to be detrimental for the

failure mode. Samples with OSP pads generated more brittle solder joint failures in ball shear tests as compared to ENIG pads.

3.2.1.2 Solder Volume and shear speed

Shihua et.al [64] investigated the effect of solder volume on shear strength for 96.5Sn3.0Ag0.5Cu and copper metallization. Shihua studied five different solder diameters ranging from 200μm to 600 μm to investigate the solder volume effect on the shear strength of solder joints at five different shear speeds upto 10000 μm/s. it can be understood that at low speeds the grain boundaries or interphase boundaries sliding and dislocation movement is sufficient and at high speed the boundary behavior and dislocation movement was limited under the fast straining which resulted in the strengthening of crystal. Shear force was increased by as much as 4 times as the solder volume increased from 0.01mm^3 to 0.11mm3. This really happens because of the reduction in the loaded area. Smaller joints have larger ratio of interface area A and solder surface S to volume of solder joints V which can result in the fast solidification and larger undercooling. Moreover, the smaller solder joints get saturated with Cu quickly. When Cu concentration reaches the threshold limit of Cu-Sn intermetallic compound (IMC) formation, the IMCs precipitate in the bulk solder which contributes to the high strength of bulk solder via a particle hardening mechanism. In the small joints, the precipitate volume fraction is much larger than the bigger joints that lead to the higher shear strength. Chia et.al [65] examined the mechanics of solder ball test and effect of dynamic loading on solder interconnects at high shear rates of upto 5000mm/min. In [65] effect of shear rate on the shear strength, the shear load-displacement and fracture morphology are discussed. Shear tool markings are often spotted at the fracture plane, as the shear speed increases the possibility of voiding/tearing in the latter part of the fracture plane increases significantly. The paper also throws light on effect on shear rate (shear speed) on the shear strength (peak force obtained in the test). Finally, the paper concludes that shear force and shear work could be apportioned to plastic deformation, fracture and friction. The plastic work was shown to be proportional to the

cube of the ball diameter while the fracture work was proportional to the square of the diameter. However, the specific shear work after maximum load, in the absence of interfacial or unstable solder fracture is relatively insensitive to the shear rate suggesting that the toughness of the solder is relatively strain rate insensitive. Ball shear test has been investigated computationally too. Lee [66] studied ball shear test computationally and it was concluded that using 2D model can actually predict and validate the experimental ball shear test in a better way as compared 3 dimensional model. In this study the ball shear test has been conducted computationally but the sole aim of computational test is to validate the experimentation.

3.2.1.3 Position of shear tool

As discussed in previous section the position of shear tool is very important in getting consistency in the ball shear test results. The shear tool standoff should be no greater than 25% of the solder height, and ensure that the shear tool does not contact the device surface throughout the monitored shear tool travel distance. Alignment is best achieved with a movable stage/tool holder which permits movement in the plane perpendicular to the loading direction. Yew *et.al* [68] studied chip on polymer and chip on board configurations in detail using experimental and computational methods. It was concluded that the type of structure can have a significant effect on ball shear strength and in turn board level accelerated tests. Yew also studied the effect of direction in which solder bump is sheared using ball shear test. Solder joint was sheared in six different angles varying from 0 degrees to 306 degrees in anti-clockwise direction and observed that there was about 20% variation when going from 0 degree to 306 degrees. Maximum shear force was observed at 36 degrees and 216 degrees. In experimentation it is difficult to fix the shear tool exactly at 36 degrees just by shear guess. However, it is practical to have the wafer fixed at 45 degrees. Hence, in this study the solder bump is fixed at 45 degrees to and then the structure with solder bumps are sheared to get consistent results. Effect of shear height has also been investigated by many investigators. JESD22-B117 suggests that the solder height should be 10% of the total shear height.

However, during ball shear testing, the sidewalls of the SMD (solder mask defined) area array bond pads tend to support the solder joint, which can change the failure mode. Therefore, there is a reluctance to fully embrace the shear technique for monitoring susceptibility to brittle interfacial failures. [7]

Kim [68], Kim and Jung [69] reported that the shear speed affects the shear test of In-48Sn, which has a low melting temperature; Sn-Ag and Sn-Ag-Cu solder balls which have high melting temperatures using similar experimental and finite element techniques [6]. The objectives of ball shear test in this study are to evaluate the effect of pertinent shear test parameters, such as shear height and shear speed, on different structures, on different sized and different solder compositions. All these tests were performed on wafer level CSPs on wafer. In this study, the shear tool was positioned at 45° with respect to the solder ball as shown in figure 4.1. The ball shear test was done at 25µm and 125µm height from wafer surface. The ball shear tests were carried out at 400µm /s. Strain rate for ball shear test was calculated using shear speed and bond diameter. The tool moves in the direction of black arrow and it shears off the solder joints in the direction of the red arrow.

3.3 Conclusion

From all the studies that we have reviewed following are the comments

1. Ball shear test is a wafer level test method that is used to test the interconnection formed by the process.
2. As shear speed increases the shear strength detected by the shear tool also increases.
3. Effect of temperature aging on different solder ball compositions was examined and it was observed that as aging time increases the brittle fracture incidence also increases.
4. Ball shear test was modeled using commercially available finite element softwares and it was concluded that 2D model can be as effective as 3D model. Ball shear test being a uni-axial test it is not necessary to model it in three dimensions.

5. It was observed that lead free solder demonstrated more shear strength as compared to tin lead solder but is found to be more susceptible to brittle failure as compared to tin lead solder.

In this study, a DOE was established to study ball shear test under various conditions. The DOE comprised of three different structures, three different solder materials, and all the configurations were sheared at two different heights. Chapter 4 talks more about ball shear test.

CHAPTER 4

BALL SHEAR TEST – COMPUTATIONAL AND EXPERIMENTAL

4.1 Experimental ball shear test

In this experimental study a dedicated ball shear tester was used. The types of structures were ball on pad (BOP), Ball on RDL (BOR) and Ball on Stub (BOS). Results are presented for Sn 96.5Ag 3.0Cu 0.5 (SAC 305), Sn 98.25 Ag 1.2 Cu 0.5 Ni 0.05 (SAC 125Ni) and Sn 95.5Ag4.0 Cu0.5 (SAC 405) solder ball compositions. The ball shear test was done at 25µm and 125µm height from wafer surface. The ball shear tests were carried out at 400µm /s. Strain rate for ball shear test was calculated using shear speed and bond diameter. The following schematic shows direction in which ball shear tests were done, red arrow shows the direction in which solder ball was sheared. The tool moves from left to right.

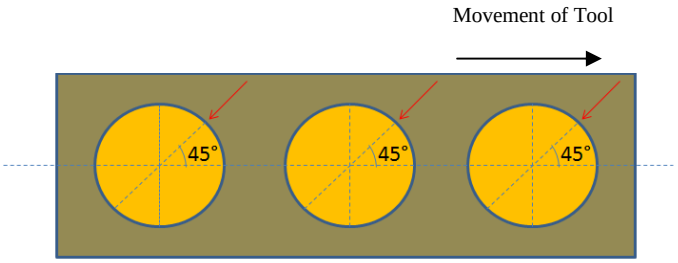


Figure 4.1: Schematic of a wafer with solder joints. Red Arrow shows motion of ball shear tool

Wafer had gone through all the dedicated processing procedures that need to be done for creating the structures. The reflow profile used for creating the ball joint consisted of a pre-heat of 150℃, a ramp up rate of 1℃/s ,peak temper ature of 255℃ and cool down ramp rate of

1.63℃/s. the strain rate was calculated based on the pad diameter . All tests were performed by shearing ball at a 45° angle as shown in figure 4.1 . The shear tool touches wafer surface and it gets lifted to the desired height and then the ball is sheared off at the desired speed. The peak value of ball shear strength (gF) and time required for each test are recorded. All the ball shear values recorded at 25µm and 125µm heights are values of peak force. Distance traveled by the tool is calculated by the time taken by tool to complete the test and the speed at which it travels shearing of the solder.

4.2 Design of experiments

A Design of experiments was carried out on the basis of the parameters discussed above, using Taguchi optimization techniques with larger-the-better methodology.. Table 4.1 shows different parameters that are varied in this DOE. Figure 4.1a,b,c show the Ball on Pad, Ball on RDL and Ball on Stub structures considered in this study.

Table 4.1: Parameters that are varied in this study

No.	Structure	Shear Height (µm)	Type of UBM	Dielectric Thickness (µm)	Solder Ball
1	Ball on Pad	25/125	Ti Ni V/Cu	3	SAC 305
2	Ball on RDL	25/125	Ti Ni V/Cu	7	SAC 405
3	Ball on Stub	25/125	Ti Ni V/Cu	12	SAC 125Ni

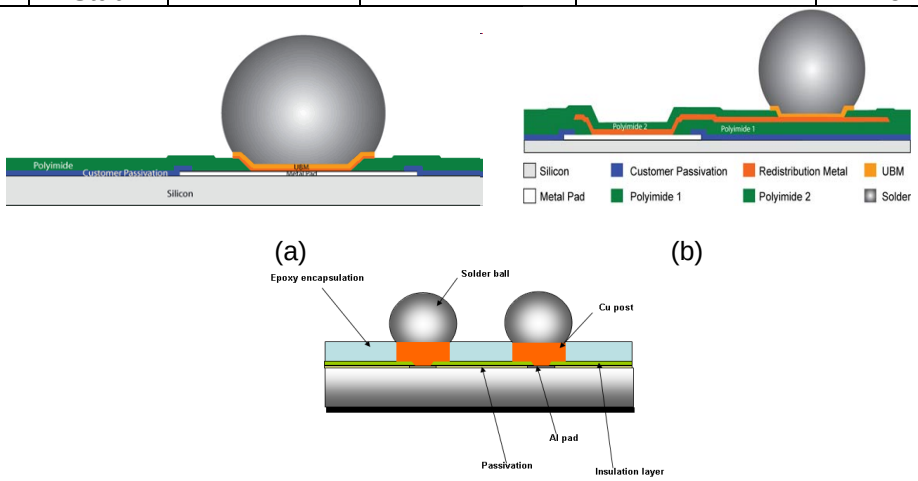


Figure 4.2: Structures under consideration (a) Ball on Pad (b) Ball on RDL and (c) Ball on Stub [70]

The DOE that comprised all these parameters resulted in 22 cases. The best case among the whole DOE was determined by signal/Noise ratio. In this analysis shear height is considered as an independent variable whereas all other wafer level structural factors are dependent variables. Signal/Noise ratio for each configuration was calculated based on larger-the-better situation. The standard Taguchi equation for larger-the better situation is given by equation 4.1. Equation 4.2 gives the equation that was modified for this study. BS is the value of shear force obtained when the shear test was conducted at 25μm. BP is the value of shear force obtained when shear test is conducted at 125μm [71].

$$SN = -10\log_{10}\left(\frac{1}{n}\sum\left(\frac{1}{y_i^2}\right)\right) \quad 4.1$$

$$SN = -10Log_{10}\left[\frac{1}{2}\left(\frac{1}{(BS)^2}+\frac{1}{(BP)^2}\right)\right] \quad 4.2$$

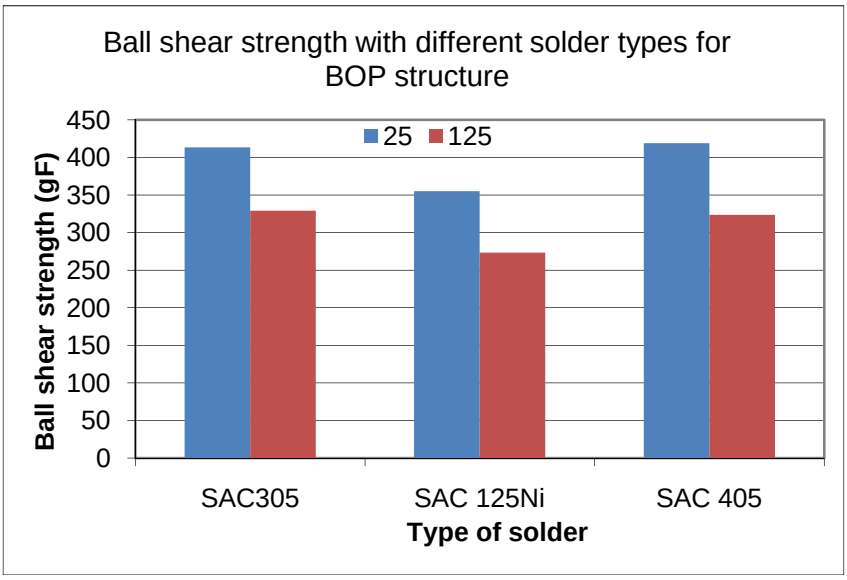
4.2.1 Results from Ball shear DOE

Table 4.2 shows the various cases that were generated with the variation of the parameters in DOE. This DOE was designed in such a way that not only sample size is enough to measure importance of different parameters but also there is enough repetition to get a good standard deviation from the readings.

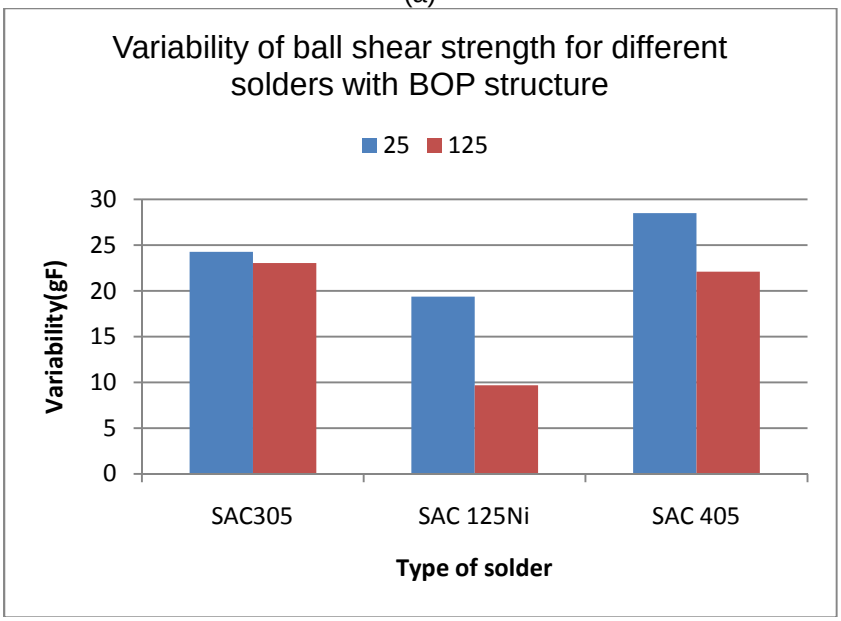
Table 4.2: Different cases based on the parameters varied

No.	Solder Size(μm)	Structure Type	Solder Solder ball Type	Ball Shear (25μm)	Ball Peal (125μm)	Mean	SN
1	300	BOP	305	413.58	329.08	371.33	51.23
2	300	BOR	305	366.66	302.17	334.41	50.36
3	300	BOS	305	372.44	309.34	340.89	50.54
4	300	BOP	125Ni	355.27	273.54	314.4	49.73
5	300	BOR	125Ni	309.69	253.71	281.7	48.87
6	300	BOS	125Ni	325.87	256.61	291.24	49.10
7	300	BOP	405	418.84	323.43	371.13	51.17
8	300	BOR	405	376.54	308.66	342.6	50.57
9	300	BOS	405	381.86	312.78	347.32	50.69
10	250	BOP	305	367.28	252.69	309.98	49.38
11	250	BOR	305	320.65	230.32	275.48	48.45
12	250	BOS	305	340.52	236.54	288.53	48.78
13	350	BOP	305	407.61	325.37	366.49	51.12
14	350	BOR	305	388.99	317.95	353.47	50.84
15	350	BOS	305	366.29	311.67	338.98	50.52
16	300	BOR	305	365.44	302.95	334.19	50.37
17	300	BOP	305	406.26	325.95	365.88	51.11
18	300	BOP	305	421.13	317.95	375.13	51.29
19	300	BOR	305	376.13	311.67	335.14	50.31
20	300	BOR	305	363.43	302.95	327.8	50.16
21	300	BOP	305	376.31	325.5	340.57	50.5
22	300	BOP	305	425.42	294.15	374.69	51.23

Figures 4.3a, 4.4a, and 4.5a show variation of ball shear strength of SAC 305 solder with different solder diameters for 25μm and 125μm heights for BOP, BOR and BOS structures respectively. Figures 4.3b, 4.4b and 4.5b show variation of ball shear strength with respect to different solder types. The tests were performed at 25μm and 125μm heights. Figures 4.7a show the variation in signal/noise ratio for SAC 305 solder with different solder ball diameters and figure 5b show variation of signal/noise ratio of different solder types for BOP, BOR and BOS respectively. From the table it can be concluded that case no. 18 is the best case with highest signal to noise ratio of 51.29

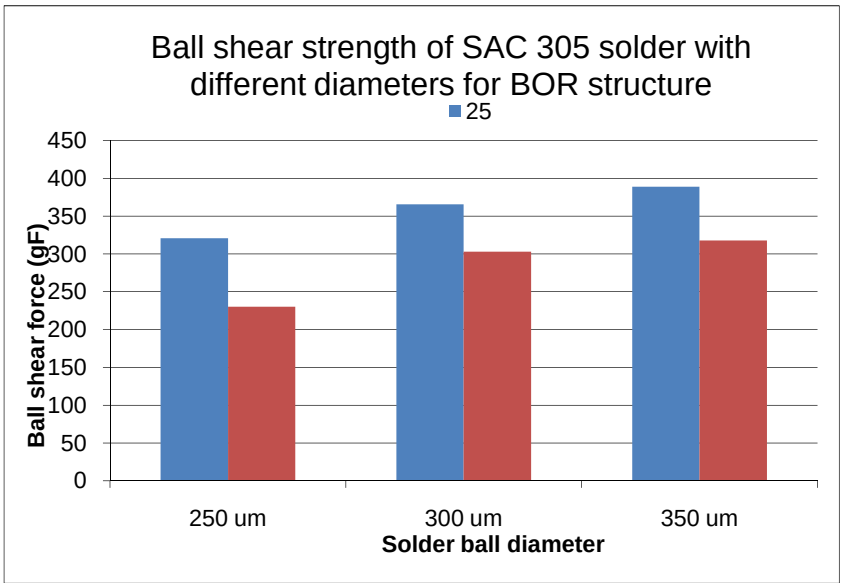


(a)

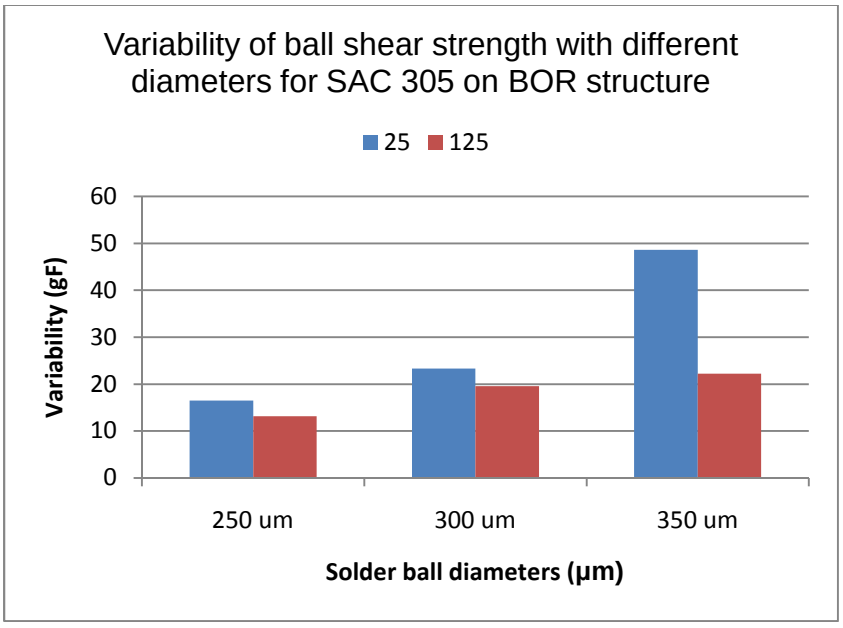


(b)

Figure 4.3: Variation of Ball Shear Strength with different solder materials on Ball on Pad structure (a) Ball Shear Strength and (b) Variability

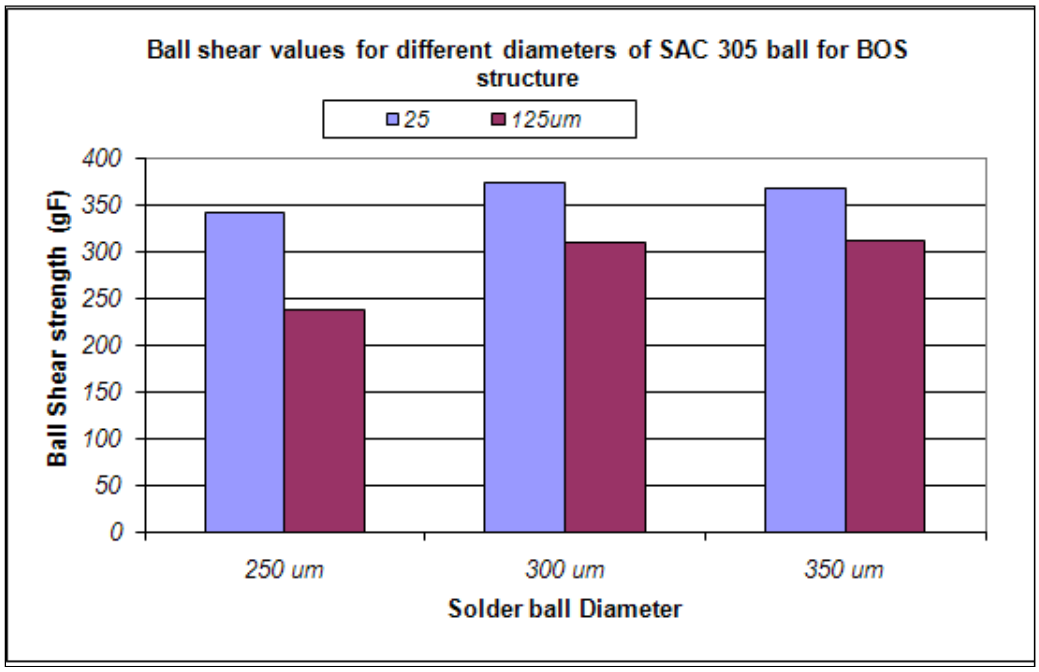


(a)

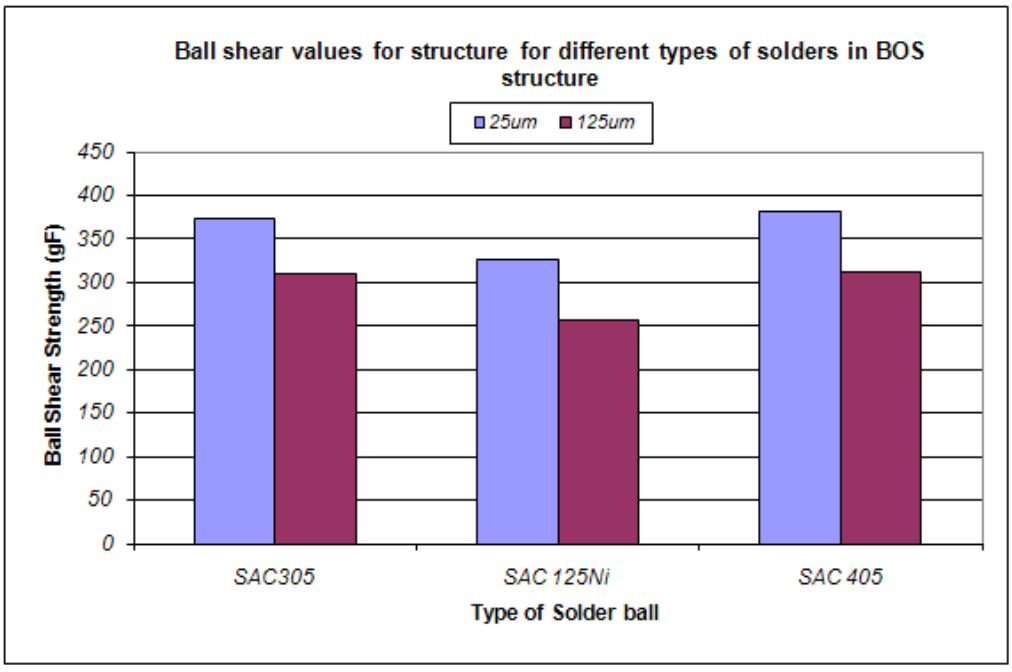


(b)

Figure 4.4: Variation of ball shear strength with different ball types with 300µm ball for BOR structure (a) Ball Shear Strength (b) Variability

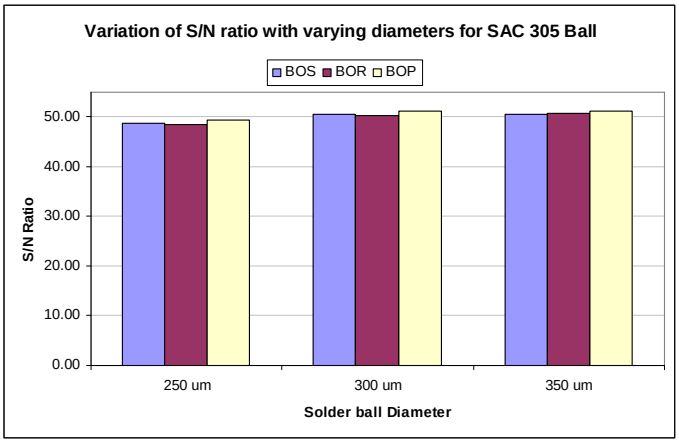


(a)

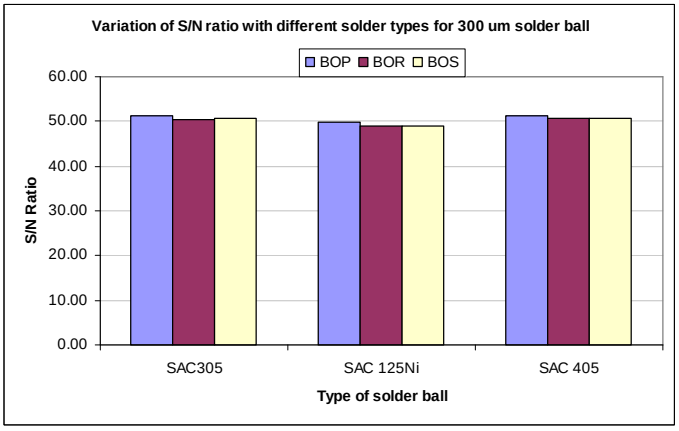


(b)

Figure 4.5: Variation of Ball shear test on BOS structure (a) SAC 305 ball with Different Diameters (b) 300µm solder ball with different materials



(a)



(b)

Figure 4.6: Variation of S/N ratio for (a) Different solder diameters mounted on different structures for SAC 305 ball and (b) Different solder materials with 300 µm diameter mounted on different structures.

From figure 4.3a it can be inferred that ball shear strength in terms of gram force increases consistently with increasing ball diameter and is true for all the structures. It can be observed from figures 4.3b – 4.5b that SAC 125Ni has the least ball shear strength amongst the three solders. SAC405 has higher ball shear strength as compared to SAC 305 in all structures. Figures 4.6a and 4.6b show the Signal/Noise ratio for SAC 305 with increasing solder diameter and various types of solders with a fixed solder diameter. It can be observed from figure 4.6a

that signal/noise ratio increases with increasing solder diameter. This is because as solder diameter increase ball shear strengths increase and hence the negative logarithm of their reciprocals increases. It can be observed from figure 4.6b that SAC 125Ni has the least signal/noise ratio because it has the least ball shear strengths.

4.3 Failure Analysis

Failure analysis in ball shear process was done by optical microscope and SEM. Figures 4.7a-4.7c show the failure mode when shear height was 25µm whereas, figures 4.7d-4.7f show the failure modes when the shear height was 125µm. The total number of failures were classified in three categories namely mode 1, mode 2 and mode 3. Mode 1 failure is the one when failure occurs in bulk solder as seen in figure 4.7a and 4.7d. Mode 1 is primarily a ductile failure. Structure of bond pad should remain intact in mode 1 failure. Mode 2 failures is the one when failure occurs in the intermetallics layer as seen in figures 4.7b and 4.7e, the black spots observed in the bond pad are intermetallics. Mode 2 is a combination failure. Structure of bond pad should remain intact in mode 2 failure. Mode 3 failure is the one in which the entire bond pad structure is ripped apart as seen in figures 4.7 c and 4.7f. Solder, Intermetallics, Under Bump Metallurgy, dielectric etc all parts of a solder joints are ripped apart by the shear tool. Mode 3 is primarily a brittle failure. It is generally said that when one encounters a mode 3 failure typically in the center of wafer then some process parameters in the wafer fabrication process needs examination.

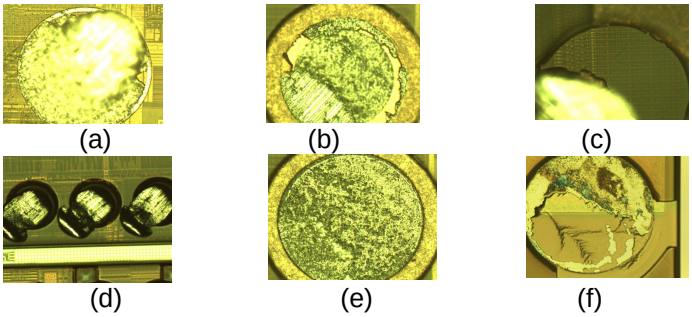


Figure 4.7: Failure modes observed in ball shear testing (a) Mode I at 25µm (b) Mode II at 25µm (c) Mode III at 25µm (d) Mode I at 125µm (e) Mode II at 125µm (f) Mode III at 125µm

In terms of shear force mode 1 requires highest force and mode 3 needs the least force. Percentage ductile failure incidence (% ductile or mode1 failure occurrences amongst total failures) is one of the most important parameters for extrapolating the results of ball shear test to accelerated thermal cycling. Many a times it happens that the force and Signal/Noise ratio are acceptable (above 250gF) but the failure mode can be different. Among the solders SAC 125 Ni had the highest % ductile failure incidence again because of flexible intermetallics. Figure 4.9 shows the cross section SEM of a sheared ball.

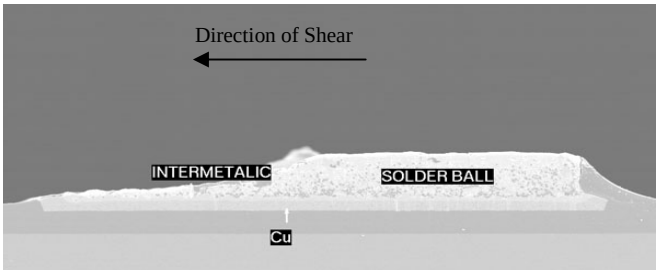


Figure 4.8: Cross-section SEM of a solder ball sheared in ball shear testing

It can be observed from figure 4.8 shows that the failure mode of this fail is mode 1; as solder is present and the structure is intact. Figure 4.10 shows the percentage ductile failure incidence for ball on pad structure with different solders for a 300µm solder ball.

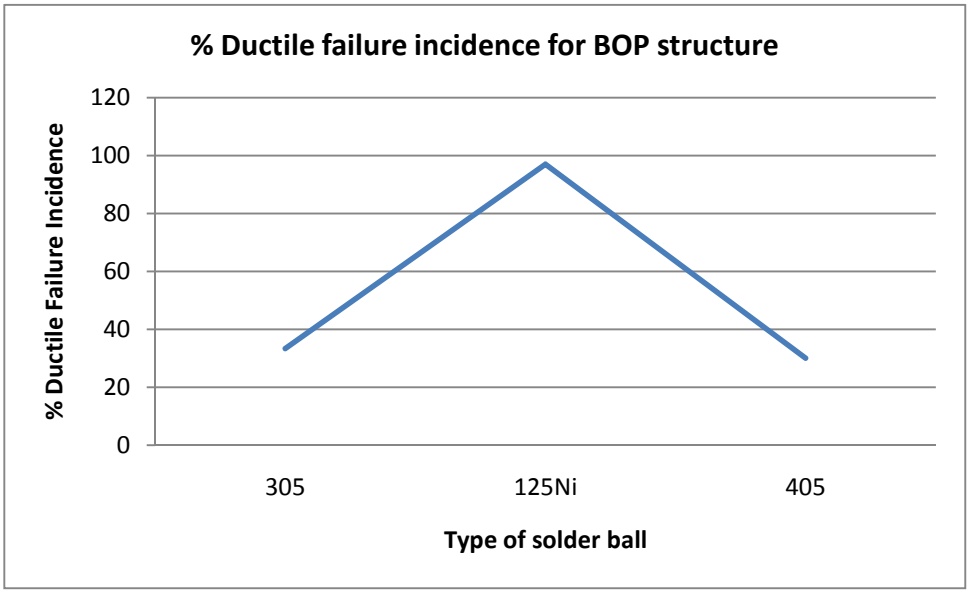


Figure 4.9: % Ductile failure incidence for different types of solder ball for ball on pad structure with a 300µm ball diameter

Table 4.3 gives a summary of different ball shear values and % ductile failure incidence (%(1&2A)) for different parameters considered in the study. All these tests were done at 125µm height.

Table 4.3: Summary of ball shear test analysis

Ball Shear analysis					
Type of structure	BOP	BOR	BOS		125Ni/300um
peal strength	245.49	254.83	252.04		
%(1&2A) mode	96.67	100.00	100.00		
Type of structure	BOP	BOR	BOS		405/300um
peal strength	290.35	306.54	292.08		
%(1&2A) mode	30.00	43.33	100.00		
Ball Size	250.00	300.00	350.00		all BOP/305
peal strength	212.94	288.52	287.72		
%(1&2A) mode	100.00	33.33	63.33		
Type of solder	305.00	405.00	125Ni		all BOP/300um
peal strength	288.52	245.49	290.35		
%(1&2A) mode	33.33	96.67	30.00		

It is observed from table 3 that there was no significant difference in ball shear values with different structures for SAC 125Ni solder. For SAC 405 solder ball on stub type of structure was observed to be the structure of choice as it had both the ball shear force value and good % ductile failure incidence. For different ball size 250μm had the highest % ductile failure incidence. SAC 125Ni had the worst % ductile failure incidence amongst the three solders for ball on pad structure with 300μm solder ball. This could be because at 125μm there is considerable torsional loading acting on the bond pad structure in addition to the shear loading. SAC 405 which has highest shear force and worst % ductile failure incidence.

4.4 Conclusions from Experimental Results

It was concluded that ball shear strength increased with increasing solder diameter consistently for all structures and all solders. Amongst all the solders SAC 125Ni was observed to have least ball shear strength and SAC 405 was observed to have the highest ball shear strength. Signal/Noise ratio was highest for SAC 125Ni as compared to SAC 305 and SAC 405. It also has highest % ductile failure incidences amongst the three solders.

4.5 Computational validation of Ball Shear Test

4.5.1 Model Creation

In this study computational study of ball shear test was done to validate the experimental results and to determine an optimum design of solder joint attachment. Computational study of ball shear test has been a topic of research for quite some time. All the cases that were studied in experimental study will be studied computationally and effects of speed, heights, structure, and material properties will be studied independently and their dependency on one another. Computational study allows us to be flexible in using different solders with different structures as fabricating all these cases can be expensive.

4.5.2 Pre-processing of Ball Shear Model

A 2D model of Ball on Pad, Ball on RDL and Ball on Stub model was made in ANSYS. Element type used for the model was Plane 82 for all the other model parts whereas visco 108 was used to model the solder ball. Shear tool was considered to be a rigid body. The contact point of shear tool and solder was modeled with targe169 elements and conta172 elements were used on the periphery of solder ball to simulate the deformation and the plasticity behavior observed in the solder ball. Multi-linear kinematic hardening model was used to simulate the plastic deformation of solder. Initially a baseline model of ball shear process was created. The purpose of creating a baseline model was to verify if a failure mode as shown in figure 9 can be created computationally. Loading of solder joint was done by moving shear tool from right to left for a fixed distance at a specified constant speed. Time of loading was varied in order to account for change in speed for individual cases. In this study speed of shear tool was varied from 100µm/s to 700µm/s. When solder breaks the shear force monitored at the shear tool drops significantly. Shear force values were considered till after first fall in shear force. Table 4.4 shows the material properties used in the modeling. Figure 4.10 shows the meshed model.

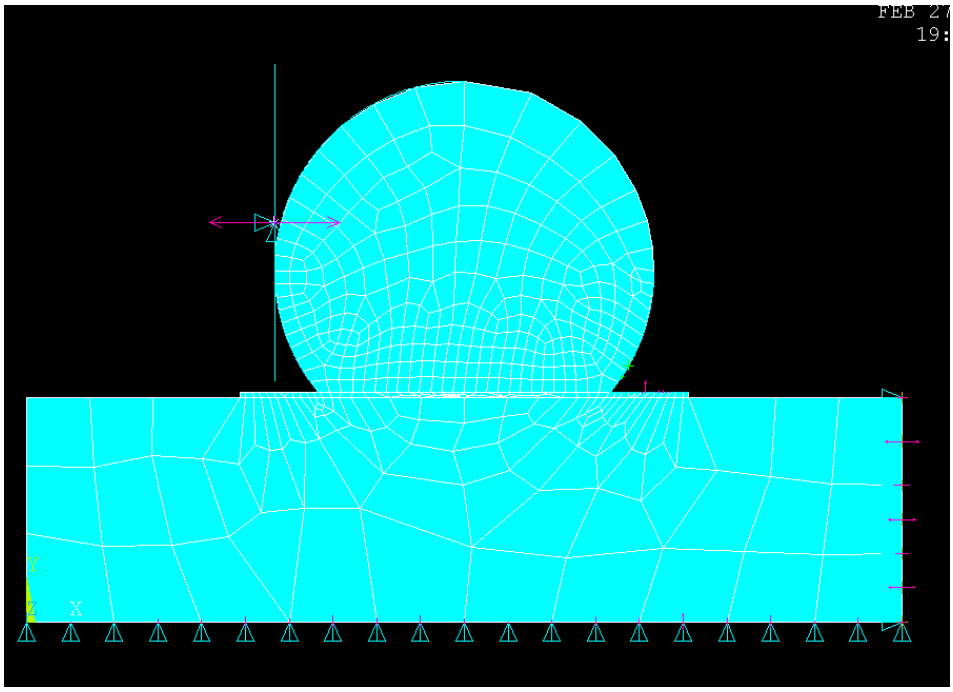


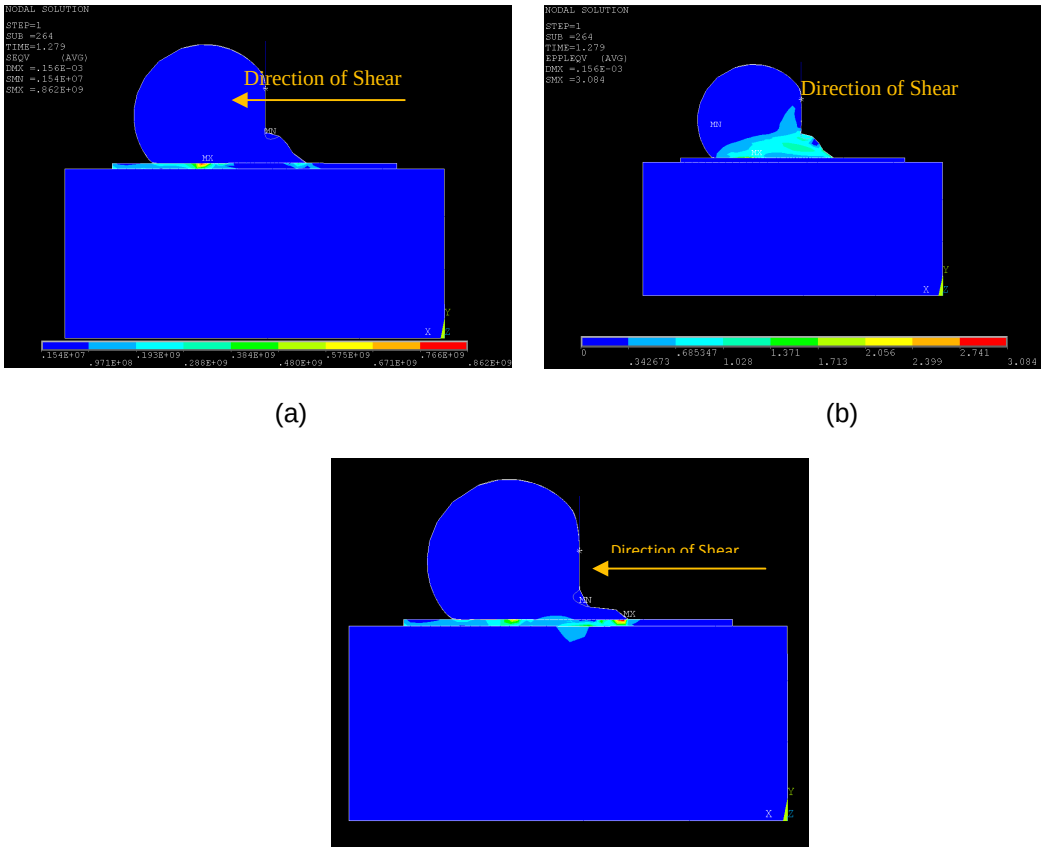
Figure 4.10: Meshed 2D model for ball shear test

Table 4 shows the material properties used in modeling. For baseline model

Table 4.4 : Material properties used in the computational study of ball shear.

No.	Material	Young's Modulus (GPa)	Poisson's Ratio	Density (Kg/m3)
1	Copper Pad	128.7	0.4	8940
2	Wafer	155.8	0.21	2329
3	SAC 305	48	0.22	7400
4	Dielectric	310	0.27	3290
5	SAC 405	52	0.22	7400

Figures 4.11a and 4.11b show the Von-Misses stress and Von-Misses strain respectively.



(a) (b)

(c)

Figure 4.11: Simulation of Ball shear test on BOR structure (a) Von-Misses stress on SAC 305 at 100 µm/s (b) Von-Misses strain on SAC 305 at 100 µm/s (c) Von-Misses stress on SAC 305 at 700µm/s.

4.6 Effect of shear speed on shear force and failure mode

Figures 4.11a and 4.11b show the von-misses stress and von-misses strain on a ball on RDL structure for SAC 305 ball. Speed of shear was 400µm/s. From Figure 4.11a it can be observed that maximum stress occurs at the joint of solder and copper pad. Figure 4.11b shows how shear strain is propagating through the solder joint. Interestingly this path matches very well with the failed solder shown in figure 4.8. This assures that modeling is predicting the failure mechanism very well. Figure 4.11c shows the Von-misses stress for a similar structure at

a speed of 700µm/s. it can be noted from figure 4.11c and 4.11a that the spot of maximum stress has been shifted from middle of solder joint structure to the start of solder joint structure. This is very interesting as now there is a very strong chance that the structure might not survive the loading and we can get a mode 2 or a mode 3 failure. Figure 4.12 gives a graph of shear force Vs displacement for solder joint with SAC 305 ball on Ball on RDL structure at various speeds in µm/s.

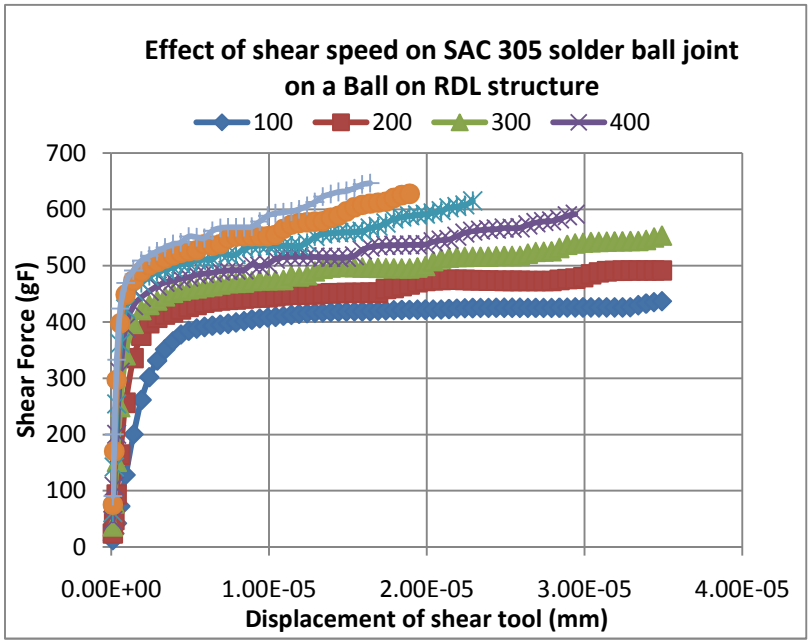


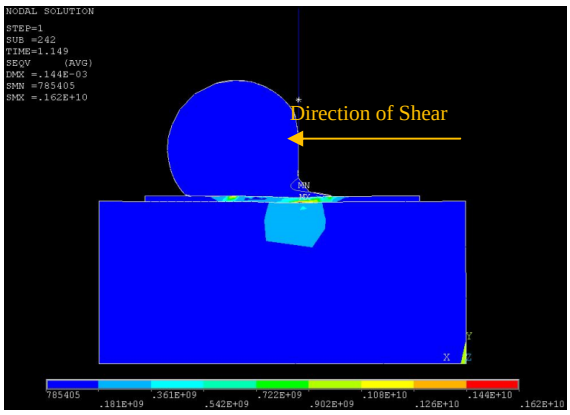
Figure 4.12: Shear force Vs displacement curve for SAC 305 BOR structure

The shear force values in this graph are taken on the shear tool where it touches the solder ball. The curves plotted in figure 4.12 are terminated at the maximum force value. Observe that as speed of shear increases the maximum shear force also increases. From figures 4.11a, 4.11b and 4.11c it can be observed that point of maximum stress moves from left hand side of solder ball to right side of structure. Hence, drop in loads at high speeds occur much quickly as opposed to less speeds. Hence, in the graph high speed curves end earlier as compared to low speed curves. This result is consistent with many similar studies reported in literature. Peak shear force noted at 700µm/s is 647gF whereas peak shear force noted at

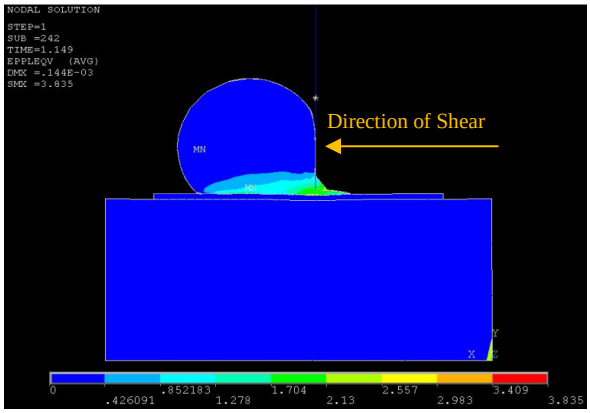
100µm/s is 436gF. The experimental ball shear force for a 300µm ball on RDL structure was 376.42gF and the computational ball shear force for a 300µm SAC 305 was 425gF and hence the percentage error in between the computational and experimental readings was closed to 11%.

4.7 Effect of Shear height on shear force and failure mode

In this section, shear speed was kept constant at 400 µm/s and shear height was varied from 10µm all the way upto 140 µm. In this section effect of shear height on shear force and shear mode is to be observed.

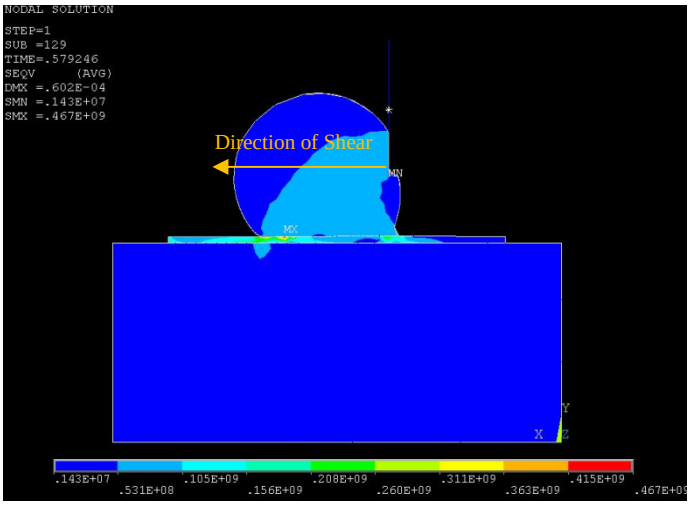


(a)



(b)

Figure 4.13: Simulation of Ball shear test for SAC 305 solder ball mounted on BOR structure sheared at 10 µm (a) Von-Misses stress and (b) Von-Misses Strain



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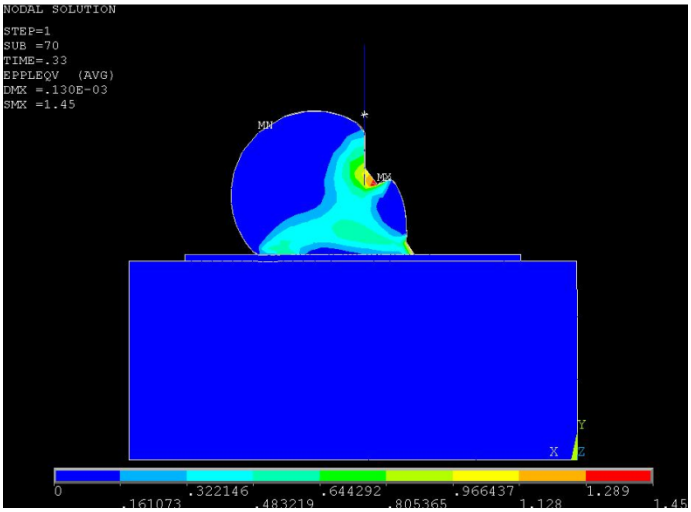
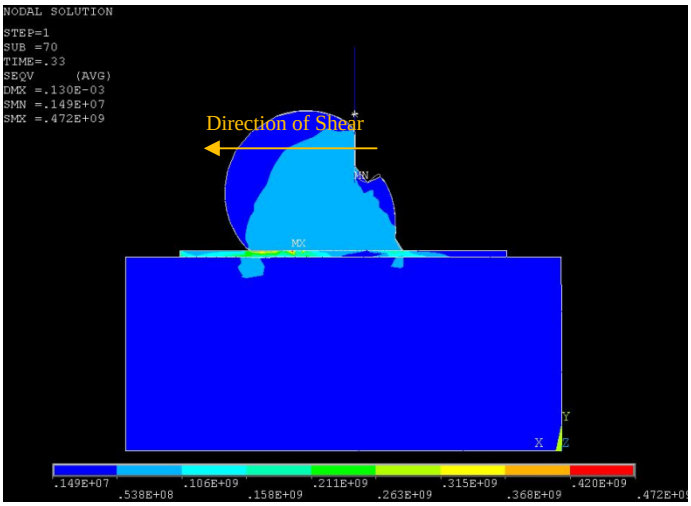


(b)

Figure 4.14: Simulation of Ball shear test for SAC 305 solder ball mounted on BOR structure sheared at 100 µm (a) Von-Misses stress and (b) Von-Misses Strain



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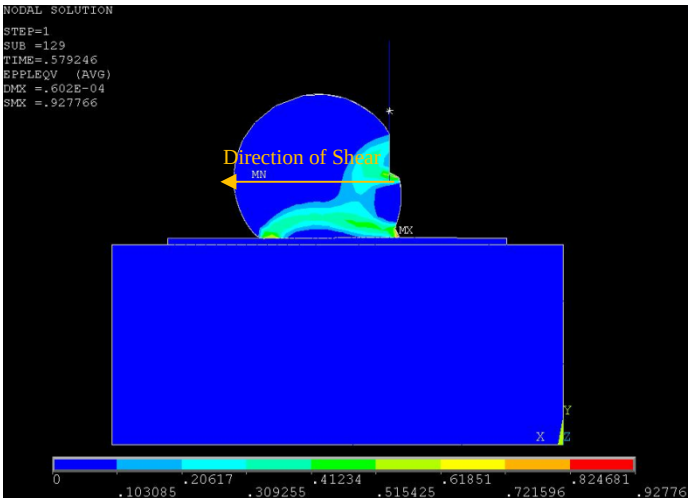


Figure 4.15: Simulation of Ball shear test for SAC 305 solder ball mounted on BOR structure sheared at 125 µm (a) Von-Misses stress and (b) Von-Misses Strain

Figures 4.13a, 4.14a, 4.15a and figures 4.13b, 4.14b and 4.15b show the Von-misses stresses and Von-Misses strains for 10µm, 100um and 125µm respectively. Figure 4.16 shows shear force (gF) plotted against displacement (mm) for various shear heights. A considerable variation is maximum shear force was not observed but a drastic variation in failure modes can be noted from figures 4.14, 4.15 and 4.16.

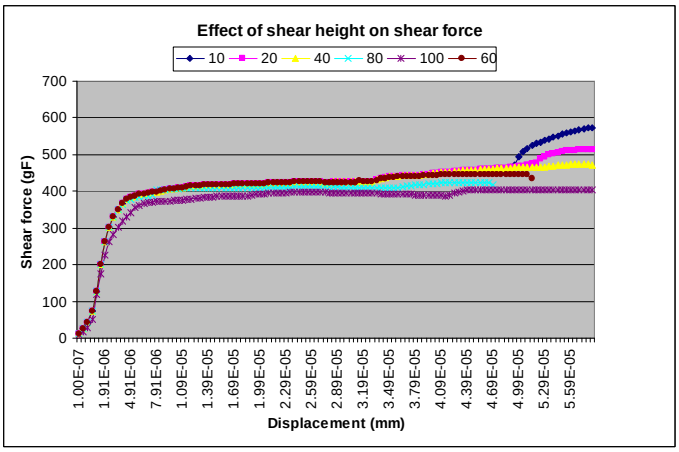


Figure 4.16: Effect of shear height studied on SAC 305 solder ball on BOR structure.

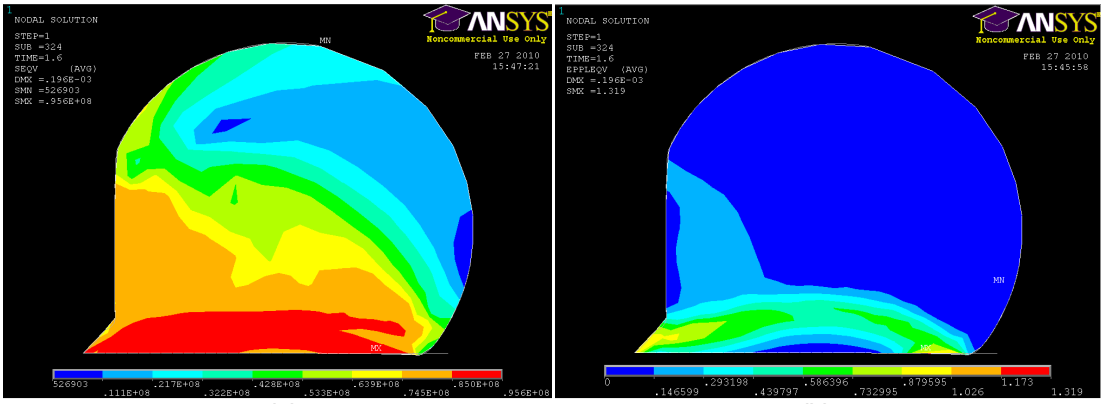
Following are the things that can be observed from the figures 4.13, 4.14, 4.15 and 4.16.

- As shear height increases, the maximum von-misses stress decreases. This is again consistent with the literature.
- Maximum Von-Misses strain decrease as shear height increase.
- Maximum stress in figure 4.13a appears at the silicon and Copper pad interface which clearly indicates that the failure is going to be a mode 3 failure.
- At 100 µm shear height it clear that the failure mode comes back to mode 1. One interesting thing to observe is solder ball is getting sheared from the point where shear tool touches the solder ball. This behavior is consistent with failure mode observed in actual experiment as seen in figure 6d.
- At 125µm height solder ball is getting sheared but is putting a significant torsional loading on the copper pad. This is clear from figure 4.15b that maximum Von-Misses strain is appearing at the start of copper pad. hence 125µm is a good height to detect brittle failures. in general brittle failures can be detected more efficiently if the solder ball is sheared at one third of its height.

Thus, speed is important to extract right strength and height is important to determine the mode. Typically, the correct shear speed and the correct shear height of the shear tool are fixed in such a way that the one should get a mixed mode of ductile and brittle modes. However, it is very difficult to duplicate the same types of modes computationally.

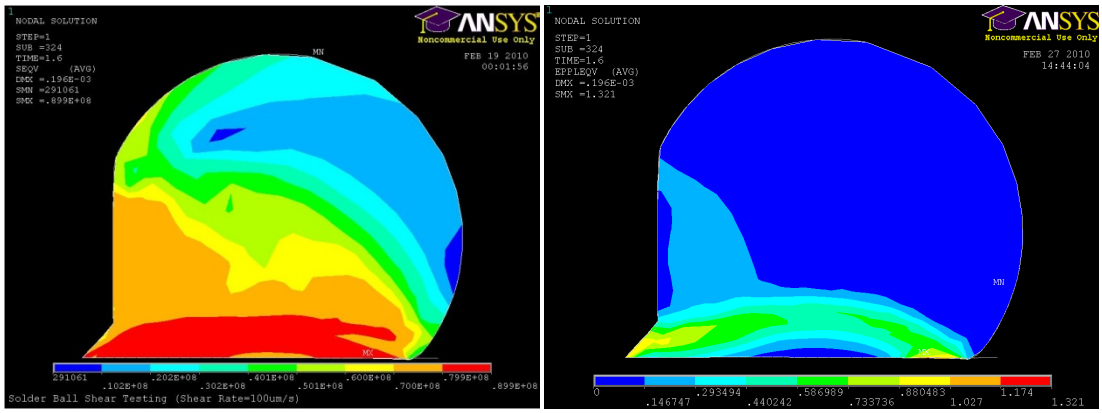
4.8 Effect of temperature on Ball shear stress

Effect of temperature on solder and in general the strength of material is very well understood and reported in literature. It is a well known fact that as temperature increases the shear strength of solder decreases dramatically. In this dissertation, the properties of SAC 305 and SAC 405 from the temperature dependent material properties and young's modulus. Properties of the solder were inserted in the multi-linear kinematic hardening models for the temperatures of 20℃, 45℃, 82.5℃ and 125℃.



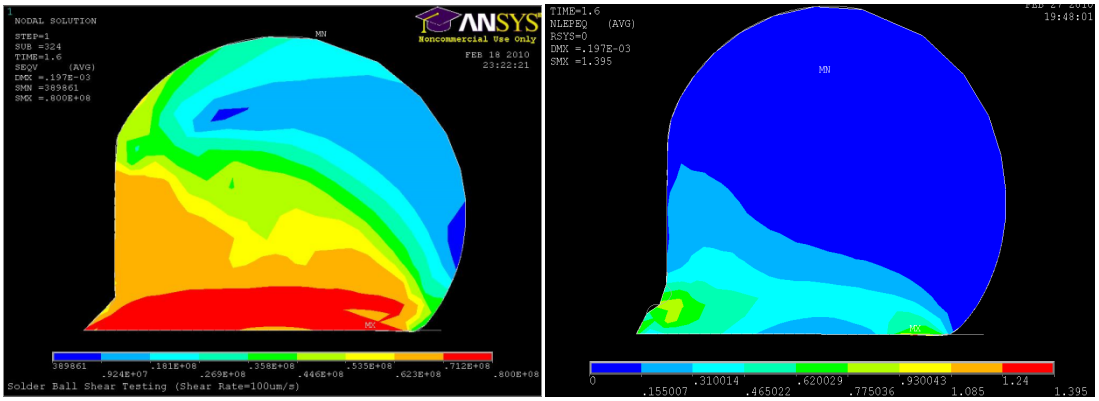
(a) (b)

Figure 4.17: Simulation of Ball shear test at 20℃ for SAC 305 (a) Von-Misses stress (b) Equivalent plastic strain



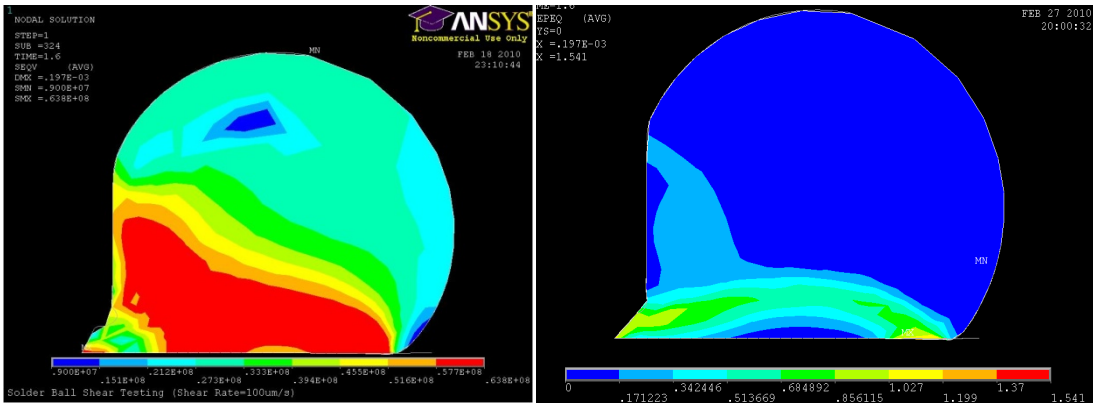
(a) (b)

Figure 4.18 Simulation of Ball shear test at 45℃ f or SAC 305 (a) Von-Misses stress and (b) Equivalent plastic strain



(a) (b)

Figure 4.19: Simulation of Ball shear test at 82.5°C for SAC 305 (a) Von-Misses stress and (b) Equivalent plastic strain



(a) (b)

Figure 4.20: Simulation of Ball shear test at 125℃ for SAC 305 (a) Von-Misses stress and (b) Equivalent plastic strain

It can be observed that as temperature increases the corresponding stress and strain decrease which is very much intuitive with the material properties that have been observed in literature. It can also be noted that the plastic strain that is generated in the solder model is also increasing possibly because some creep is getting introduced in the material. Equivalent plastic strain in material increases almost linearly from 1.319 to 1.514 as the temperature of test increases from 20℃ to 125℃.

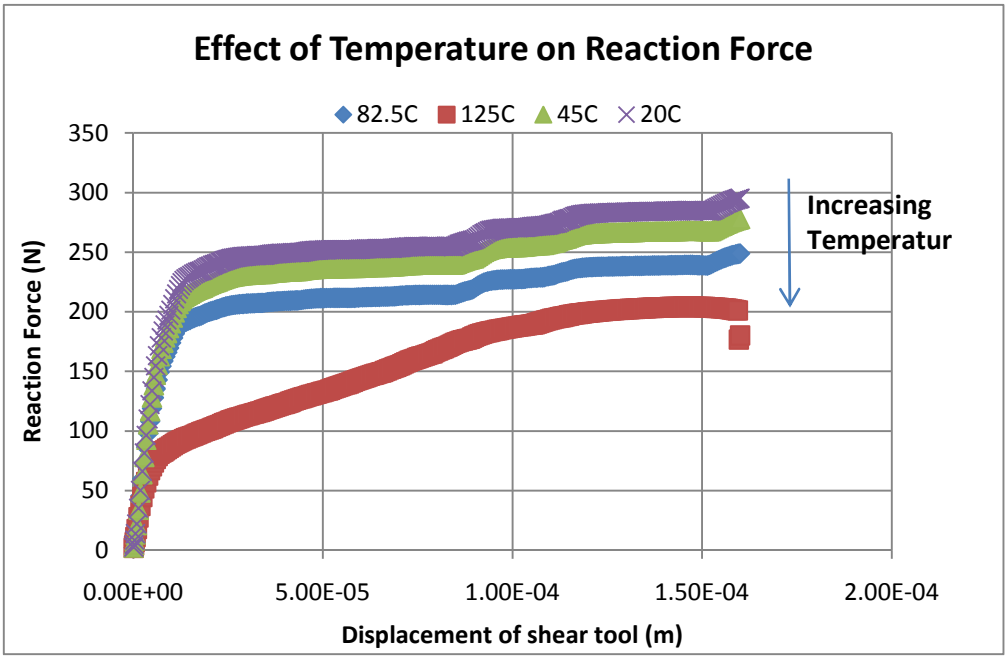


Figure 4.21: Effect of temperature on ball shear force for a SAC 305 solder bump with 250µm on RDL structure

One can observe that there is almost a net reduction of around 40% reduction in the peak force required to break the solder. This primarily is because of reduction in ductility with temperature. It is a known fact that as temperature increases ductility and hence young's modulus of a lead free solder reduces. That's the primary reason why a reduction in peak stress is observed when the test temperature is increased.

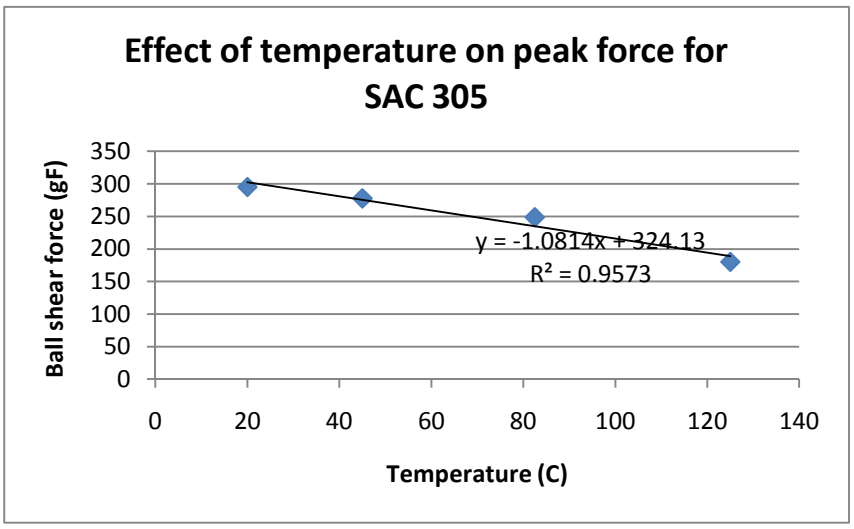


Figure 4.22: Reduction of peak ball shear force when ball shear test was done at 25µm height

Figure 4.22 shows the change in equivalent plastic strain as the test temperature increases from 20℃ to 125℃.

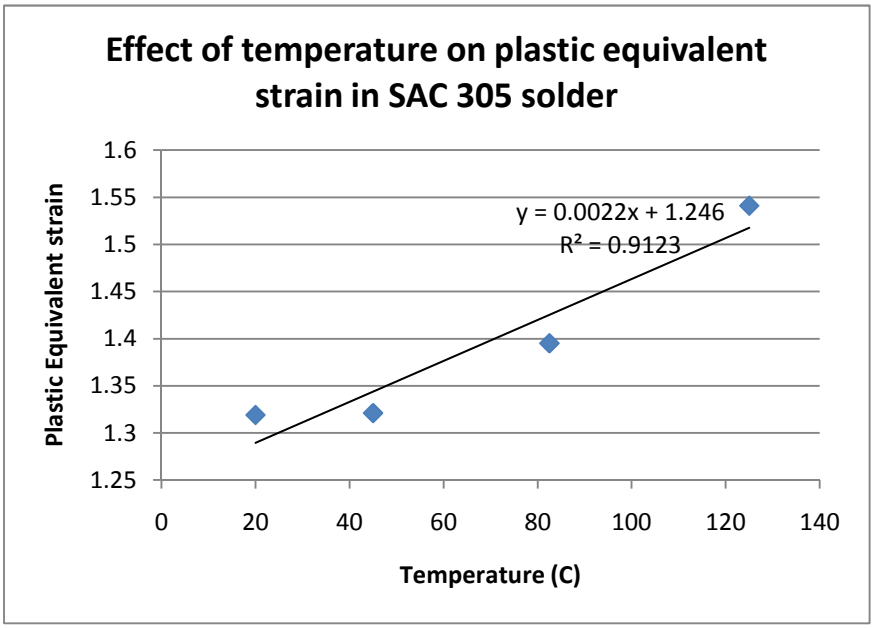


Figure 4.23: Effect of temperature on plastic equivalent strain induced in 250µm solder bump in SAC 305 ball

Table 4.5 Effect of temperature on shear strength of solder

Number	Temperature (℃)	Height (μm)	Ball shear (25 μm)
1	20	25/125	295.15
2	45	25/125	277.76
3	82.5	25/125	248.76
4	125	25/125	180.17

4.9 Conclusion

In this study, an attempt was made to determine the factors affecting ball solder joint. Type of solder, solder diameter and solder joint structure was varied to determine the optimum parameters to give maximum solder joint strength. The factors were studied experimentally and computationally. Experimentally it was determined that Ball on Pad structure with SAC 405 solder provides maximum ball shear strength. Computationally, a multi-linear isotropic hardening model was used to predict shear test. It was observed that the multi-linear isotropic hardening model was able to predict the failure mode that was observed in experiments. Overall, test conducted at 125μm height can capture brittle failure as more effectively compared to other heights. Effect of temperature on material properties was examined and it was observed that there is a net reduction of about 40% in the peak strength as predicted by the computational model.

CHAPTER 5

ACCELERATED THERMAL CYCLING - COMPUTATIONAL AND EXPERIMENTAL

5.1 Introduction to accelerated thermal cycling

Accelerated thermal cycling was performed on lead free solder joints to investigate the fatigue joint reliability and the potential failure mechanism. The experimental results were validated by using finite element analysis. In the current electronic packaging industry the use of accelerated tests is very well established. The widely used accelerated test for predicting fatigue life of solder bumps is accelerated temperature cycling (ATC). An accelerated thermal cycle can be defined in terms of high and low temperatures; dwell times at high and low temperatures. A number of recommended ATC profiles are available in literature as well as standards. The choice of an ATC profile to be utilized for qualification is governed by the intended application and the field use conditions of the packaging assembly. Figure shows the recommended ATC profiles that are commonly used in testing lead free solder assemblies.

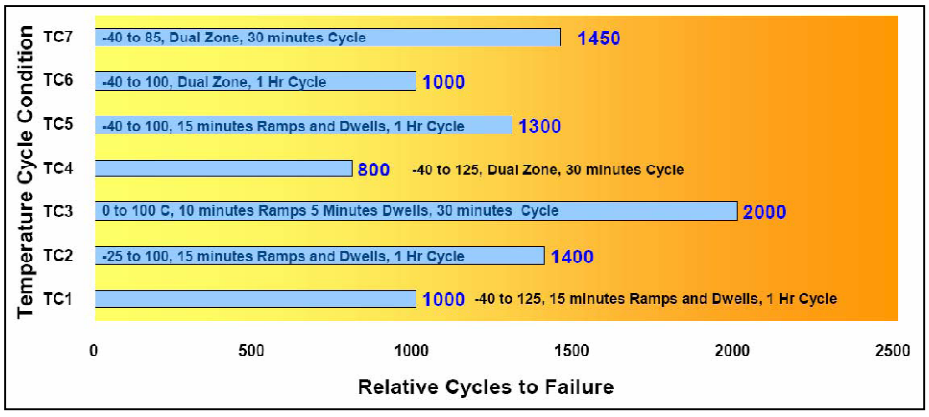


Figure 5.1: Accelerated thermal cycling profiles commonly used in Microelectronics industry [72]

In accelerated thermal cycling the board with packages assembled is subjected to a change in temperature typically from -40˚C to 125^{o}C [9]. During this cycling, at each instant, the oven operates quasi-statically, reaching a uniform temperature almost instantaneously. The Printed circuit board has a coefficient of thermal expansion of around 18ppm and the package has a coefficient of thermal expansion of around 8 PPM. Because of the temperature variation thermal stresses act on two sides of interconnection (solder ball). Figure shows the thermo-mechanical deformation of solder joints that is observed in accelerated thermal cycling.

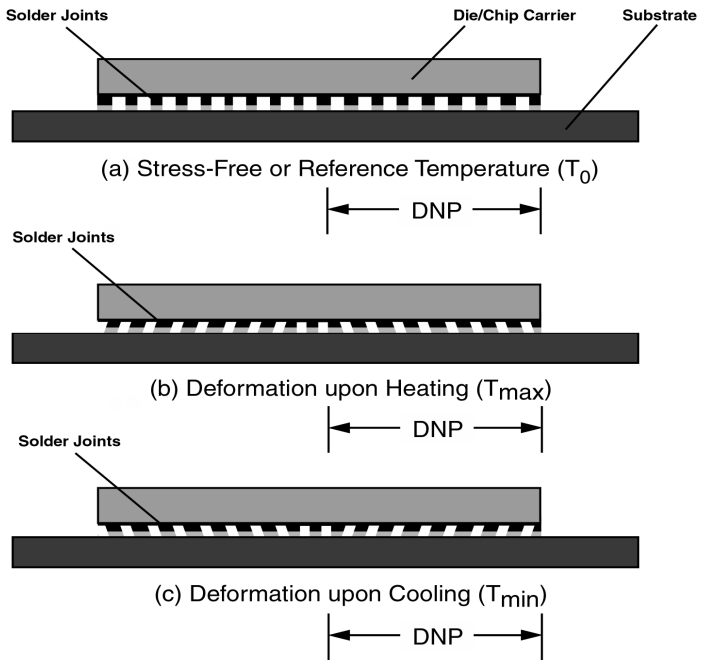


Figure 5.2: Thermo-Mechanical deformation that are observed in electronic packages during thermal cycling [1]

The failure mechanism of thermal cycling is shear and its failure signature is tension on inner side of interconnection and compression on outer side. This signature matches exactly with the failure signature of ball shear test. Thus, attempting to correlate the two types of tests

considered is not unreasonable at least empirically and statistically on a phenomenological level. In this study the accelerated thermal cycling tests were performed to investigate potential failure mechanisms and also to observe if has any connection with ball shear testing done at wafer level as described in the previous chapters of this dissertation.

5.2 Experimental Setup – Accelerated Thermal Cycling

The test boards used in this study were daisy chained, designed according to the JEDEC standard for accelerated thermal cycling. Reflow profile used in this study was the ramp up rate of 2.2℃/s , reflow temperature of 255°C , a soak time of 30-35 seconds and a cool down rate of 1.2℃/s.

Accelerated thermal cycling is done in a two stage air to air thermal shock chamber. The packages mounted on four layer boards were a 10 X 10 array wafer level chip scale packages. ENIG board finish was considered in this study for all the boards to consistency in comparison. SAC 305, SAC 405 and SAC 125Ni were solder compositions considered. 250µm, 300µm and 350µm of all three solder types were considered. The board design for this experiment was according to JEDEC standard JESD22-A104C [9]. Boards were mounted on an aluminum tray and kept in stage 1 of the chamber which is at -40°C; the boards took about 7 minutes to come to the chamber temperature. Thermocouples were mounted on boards and temperature was monitored continuously. The boards stay in this stage for 21 minutes. Thus, they are at -40°C for 14 minutes. After 21 minutes a rocker arm mechanism is activated that moves the aluminum tray to the next stage which is at 125°C. In this stage tray is kept for 21 minutes and the cycle is repeated again. In the chamber Temperatures were varied from -40°C to 125°C for two times in an hour. Failure detection was done primarily by monitoring electrical resistances. Failures were recorded when the total resistance of the daisy chain network exceeded the threshold resistance of 300 ohms and if it stays there for three consecutive measurements. Thermal resistances of the daisy chain were recorded every 100 cycles. The

test continued till 90% of the packages are failed. Failure analysis was primarily done by metallographic micro-sectioning and SEM.

5.3 Results and Discussion – Accelerated Thermal Cycling

Figures 5.3-5.6 show Weibull plots for different configurations considered in this DOE. Figure 5.3 shows the weibull plots for 300µm solder diameter with different solder types for Ball on Pad structure. It is observed that SAC 125Ni has the highest fatigue life of 874 cycles amongst all the solders for a 300µm solder ball diameter in a ball on pad structure. Figure 9 shows the weibull plot for 300µm solder diameter with different solder types for Ball on RDL structure.

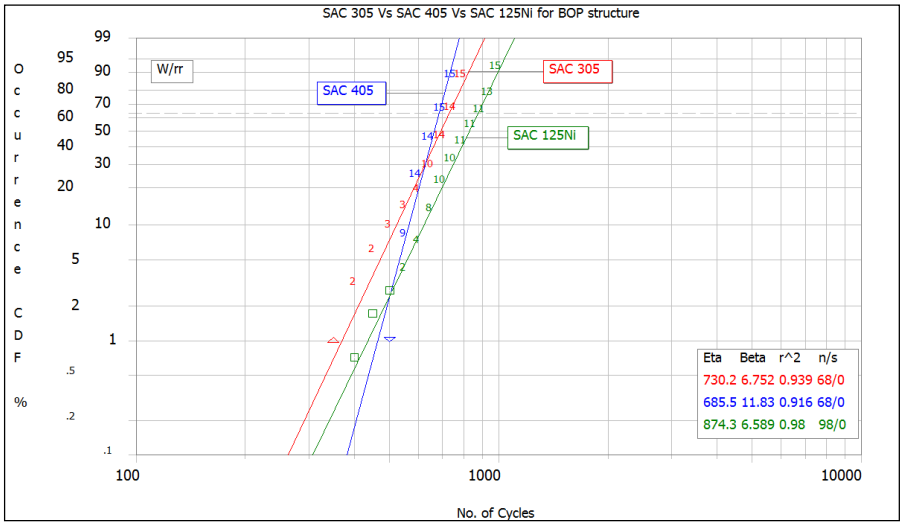


Figure 5.3: Weibull plot for 300µm solder ball with different composition for ball on pad structure

It can be observed from figure that SAC 125Ni solder bump has slightly more fatigue life as compared to SAC 305 and SAC 405 solder bumps. Primary reason for this could be the presence of Nickel in the solder which won't allow copper from copper pads to mix with Tin to form Cu_3Sn and Cu_6Sn_5 intermetallics. Instead Nickel forms a ternary intermetallic with Copper which is $(Ni,Cu)_6Sn_5$ which is much flexible intermetallic in fatigue loading. A ditto was observed in case of ball on RDL structure too.

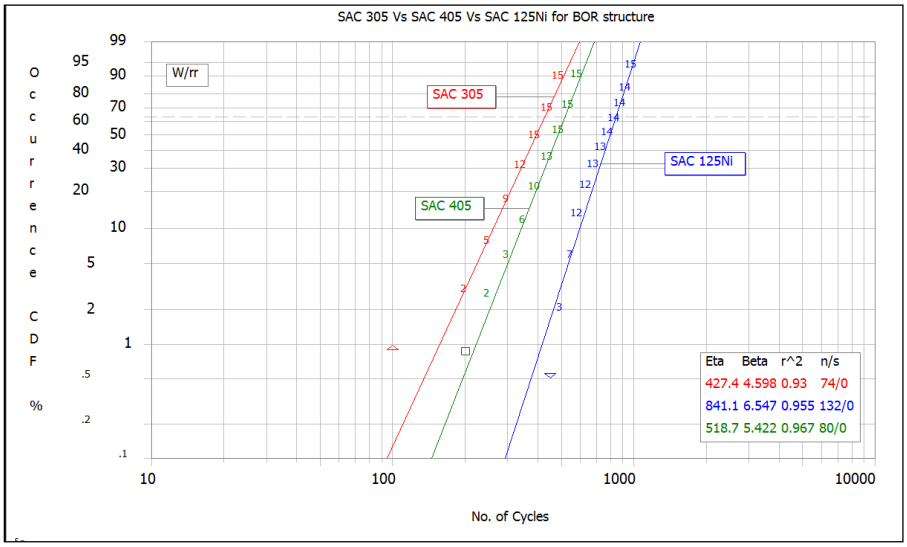


Figure 5.4: Weibull plot for 300µm solder ball with different composition for a Ball on RDL structure

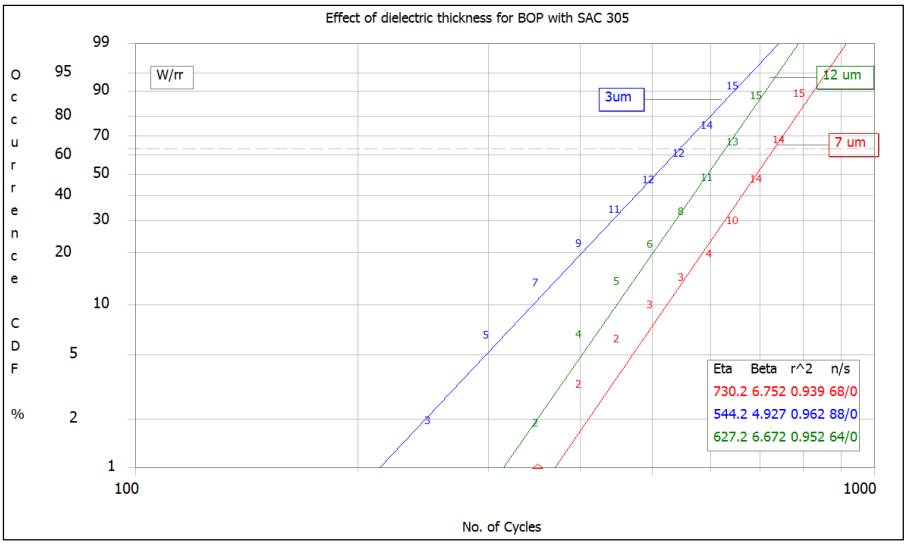


Figure 5.5: Weibull plot for Ball on pad structure with 300µm SAC 305 solder ball with different dielectric thicknesses.

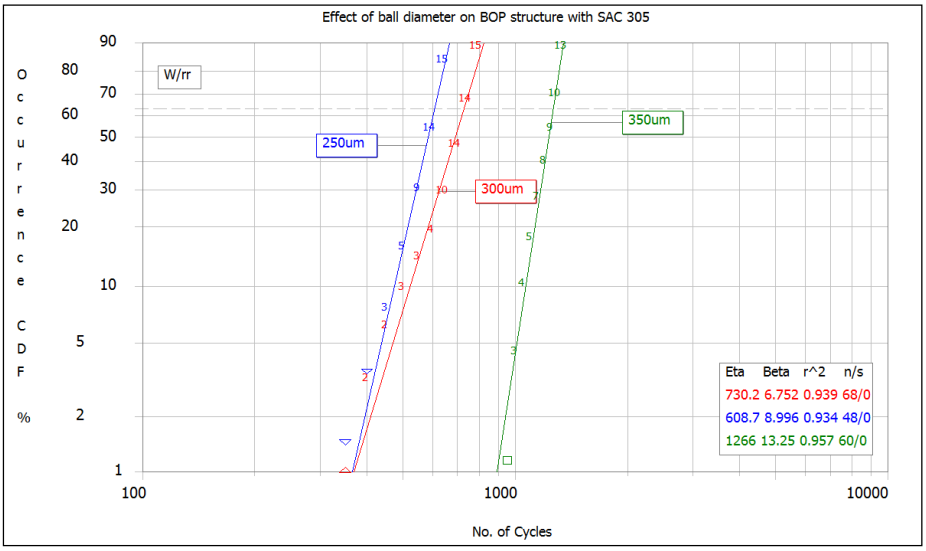


Figure 5.6: Weibull plot for ball on pad structure with different 250µm, 300µm and 350µm SAC 305 solder ball with 7µm dielectric thickness

Table 5.1 shows the summary of thermal cycling data comprising of first failure and characterisitc life of different cases considered in the DOE. Grade of importance column gives the importance of the parameter that was varied and a noteworthy increase in thermo-cycling life was obtained.

Table 5.1: Summary of thermal cycling DOE

					other parameters	Grade of Importance
No	**Type of structure**	**BOP**	**BOR**	**BOS**	**125Ni/300um**	**B**
1a	First fail	400	400	500		
1b	Char. Life	602.38	594.73	516.98		
	Type of structure	**BOP**	**BOR**	**BOS**	**405/300um**	**B**
2a	First fail	500	400	300		
2b	Char. Life	418.61	602.28	400.48		
	Ball Size	**250**	**300**	**350**	**all BOP/305**	**A+**
3a	First fail	300	400	600		
3b	Char. Life	510.58	582.49	1280.61		
	Type of solder	**305**	**405**	**125Ni**	**all BOP/300um**	**A+**
4a	First fail	400	400	400		
4b	Char. Life	582.49	418.61	602.38		

Figures 5.7-5.9 show the variation of weibull parameter with respect to different legs of DOE considered in this study. Weibull parameter is extremely important because it captures the rate of crack propagation in the solder bump. Often it is observed that weibull plot has more than one slope, in those scenarios there are often more than one failure mechanism acting

towards the failure. In figure 5.7 variation of weibull parameter in different structures for three differen solder bumps of same diameter is discussed. It is clear from the figure 5.7 that variation of weibull plot is same for ball on pad structure as well as ball on RDL structure. SAC 405 has the most weibull parameter which clearly indicates that rate of crack propagation for SAC 405 is highest amongst the solders whereas SAC 305 has the least crack propagation rate amongst the three solders considered. But the package with SAC 305 solder had crack very early and that contributed to less fatigue life of package with SAC 305 solder.

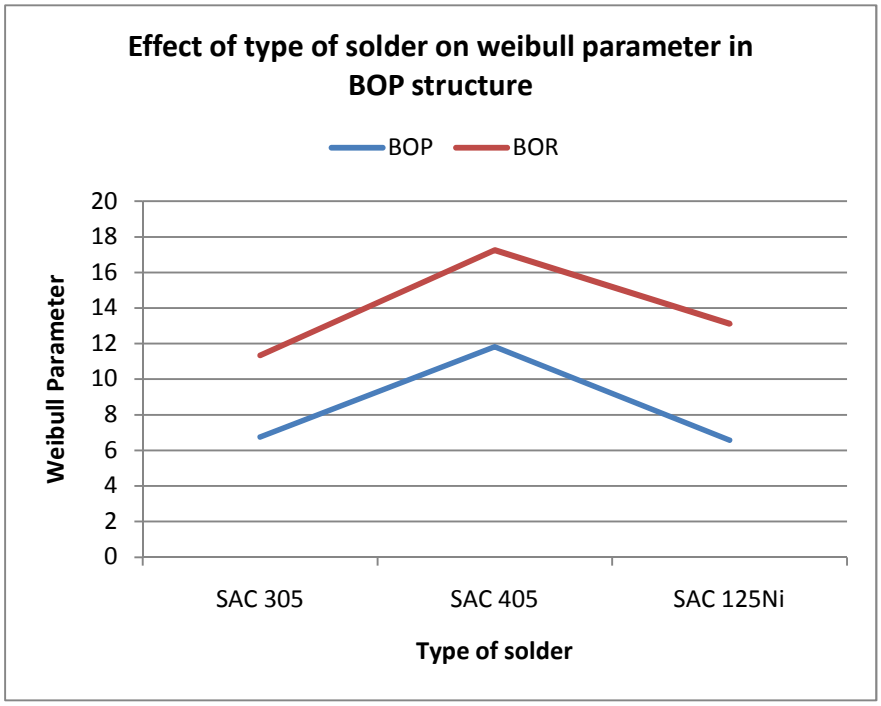


Figure 5.7: Effect of type of solder on weibull parameter tested on Ball on Pad and Ball on RDL structure.

Figure 5.8 show the variation of weibull parameter with the change in dielectric thickness for a SAC 305 soldered ball on pad structured package. Dielectric layers define the copper wetting area the ball on pad structure. The more the dielectric thickness more will be the copper wetting area which definitely adds to the fatigue life of the solder. From figure 5.8 it

can be seen that the weibull paramter is highest for dielectric thickness of 7μm and it is lowest for 3 μm.

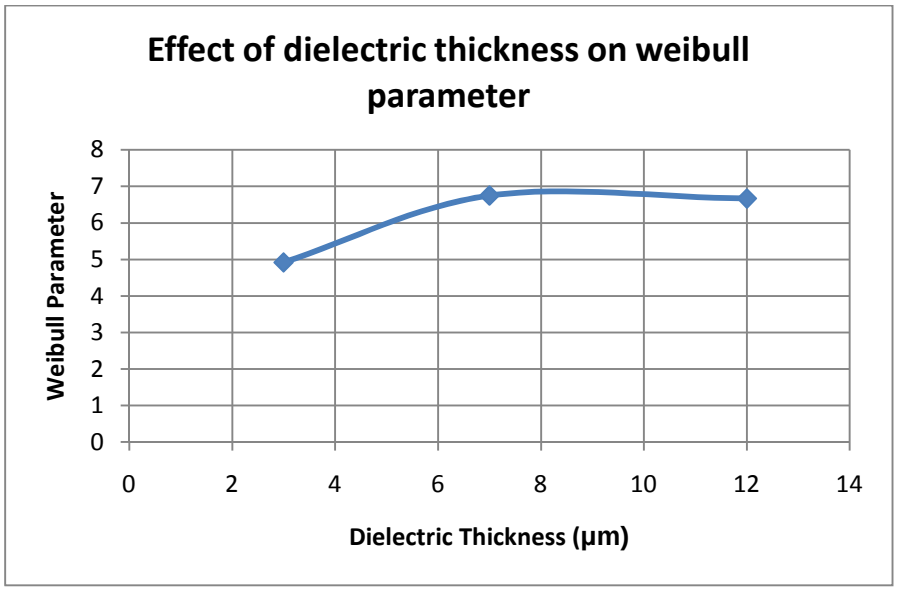


Figure 5.8: Effect of dielectric thickness on weibull parameter for Ball on Pad structure

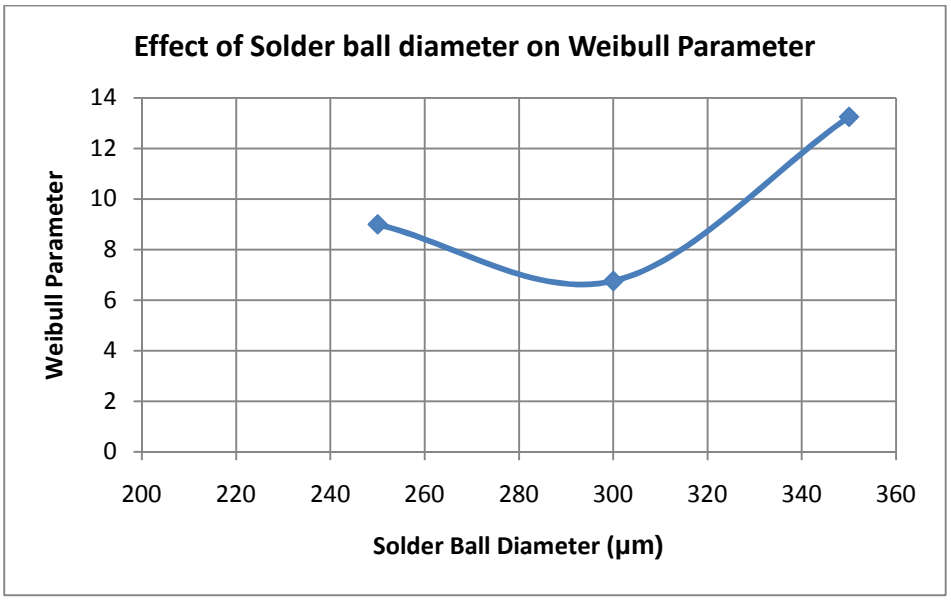


Figure 5.9: Effect of solder ball diameter on weibull parameter for Ball on Pad structure

Figure 5.9 shows the effect of solder ball diameter on weibull parameter for Ball on Pad structure. All the data presented in figure 5.9 is for SAC 305 solder. It can be observed that from

the figure that 300μm has the least weibull parameter amongst the diameters considered. However, a more important in determing solder fatigue life is the standoff height. More the solder diameter more is its height. The standoff height for a 250 μm solder ball is 212 μm for a 300 μm solder ball its 232 μm and for a 350 μm solder bump it is 252 μm as measured on an optical microspcope. Failure analysis of the failed packages was done by metalographic micro-sectioning of solder balls and examined under a scanning electron microscope.

5.4 Failure Analysis

The failure analysis is primarily done using SEM. figures 5.10 a and b show the scanning electron micrographs for ball on RDL type of structure for 250μm SAC 305 ball. From figure 5.10a it is clear the crack developed by temperature fatigue passes through the bulk solder without touching the inter-metallic layer. Some Ag_3Sn intermetallic formations can be found in the bulk solder which is a routine phenomenon for lead free solders. Figure 5.10b show a different solder ball from the same package. In this figure it is observed that the crack is ver close to the intermetallic layer, it almost touches it at a point and then again goes into the bulk solder. These SEM samples were not etched and hence it is difficult to tell if there is any dynamic recrystallization occurrence in these samples. Generally, it is observed that the crack propagation occurs along the grain boundaries. After dynamic re-crystallization the solder microstructure gets divided into several small grains and the crack propagation occurs along these grain boundaries. Figure 5.10 c shows the failure micrograph of 300μm SAC 305 ball on Ball on RDL structure. Figure shows some package rupture incidence but it doesn't really contribute to the failure of the solder bump. Figure 5.10 c also shows crack in the bulk solder on package side of the bump. It can be seen that the crack gets very wide in some areas, it won't be completely wrong to predict that the crack propagation was accelerated by presence of void in these areas. Some voiding is also observed near the bond pad due to shrinkage.

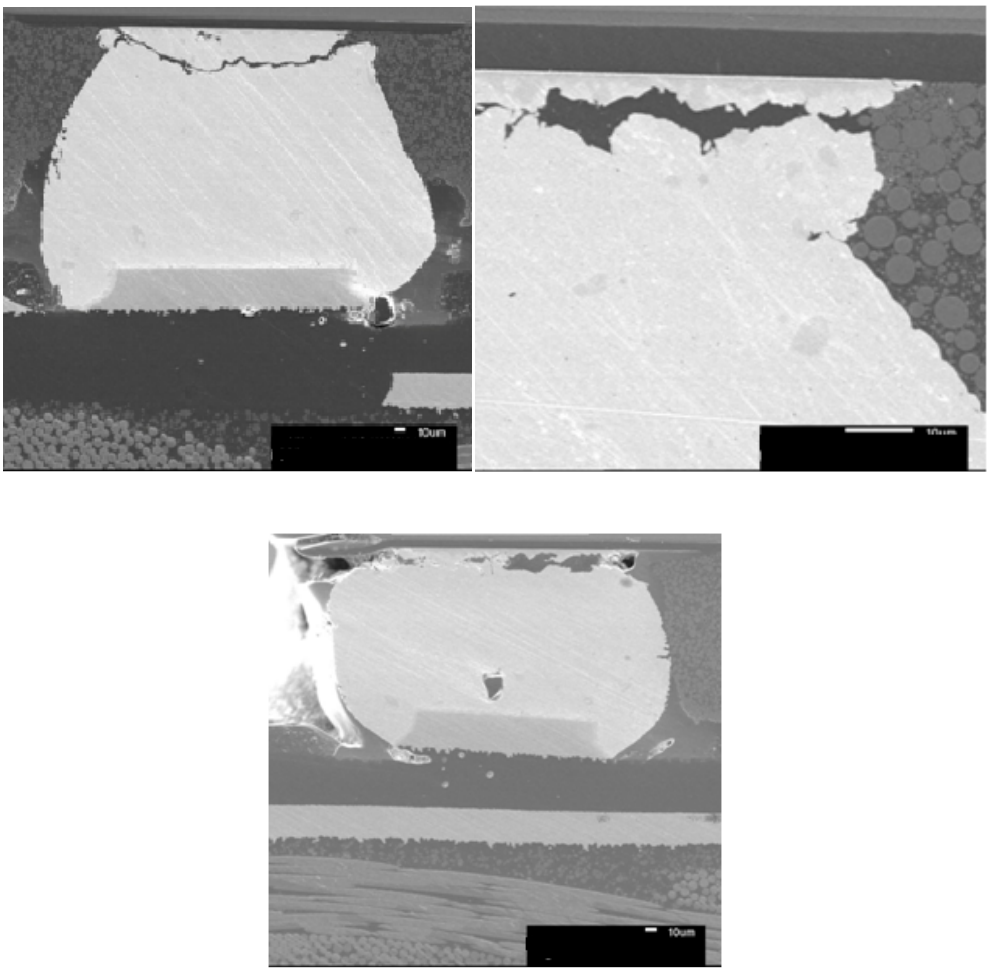


Figure 5.10: SEM Micrograph of 250 µm ball on BOR structure (a) Solder Bump (b) Focussed on Corner of bump (c) Different solder bump from the same package

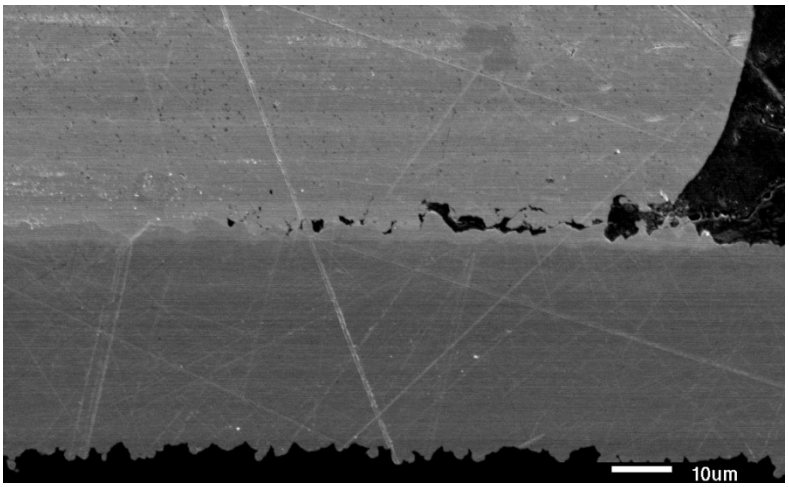
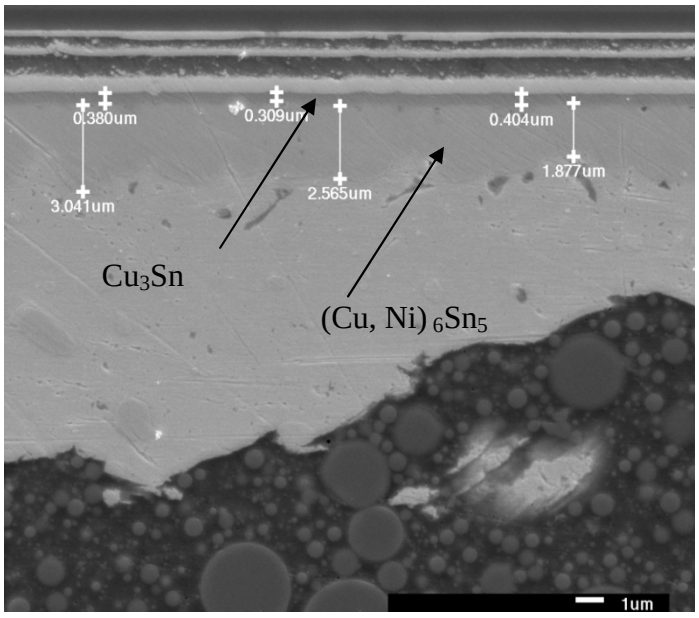


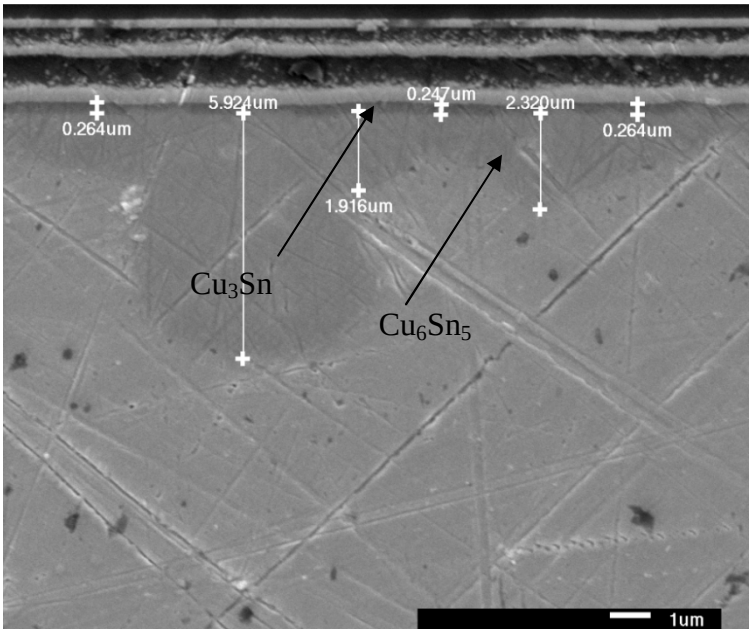
Figure 5.11: Scanning electron micrographs for 300um SAC 305 ball on BOP structure crack on PWB side

In one of the solder bumps it was observed that cracks were generated from the voids in solder bump. Figure 5.11 shows the crack getting developed near the bond pad. Crack was found to be touching the intermetallic layer. These cracks could be triggered by the formation of kirkendall voiding.

Figure 5.12 (a) and figure 5.12(b) show the intemetallic formation in the solder joints. Figure 5.12 (a) show the intemetallic formation for SAC 125Ni solder. There are two intermetallics formed the first layer is the $(Cu,Ni)_6Sn_5$ and the second layer formed is Cu_3Sn. In one particular solder bump the dimensions of the intermetallic formed is shown in figures 5.12.



(a)



(b)

Figure 5.12 Intermetallic layers observed in solder bumps (a) SAC 125 Ni and (b) SAC 405 ball

5.4.1 Classification of failure modes for accelerated thermal cycling

As discussed in chapter 4 different types of failure modes were divided in to three categories depending on the location of failure. In a similar way various the failures observed in accelerated thermal cycling were also classified into 5 categories. Mode 1 was bulk solder at package side. Mode 2 is the crack in intermetallic on package side, Mode 3 is the crack in bulk solder on the PCB side, mode 4 is the crack in intermetallic on the PCB side, and mode 5 is a failure to the die or package typically like a package rupture or a Pad lift. In this context, a crack shown in figure 5.10(a) is purely a mode 1 failure, figure 5.10(b) is can be a mixture of mode 1 and mode 2 failure. Crack shown in figure 5.11 is a mode 4 type of failure. In this study, focus was on mode 1 and mode 2 types of failures i.e. only on mode 1 and mode 2 type of failure. In chapter 6 which talks about comparing ball shear test and accelerated thermal cycling, only mode 1 or a mixture of mode 1 and mode 2 (most of the crack is in the bulk just touching the intermetallic layer) type of failure is considered in this study.

5.5 Conclusion

It was concluded that ball size was of outmost importance in improving the fatigue life due to higher standoff height. As the solder ball size increased from 300µm to 350µm the life in number of cycles increased by almost a factor of 2. Amongst the type of solders SAC 125Ni solder was observed to have highest fatigue life. One of the possible reasons could be the restriction of formation of Cu_3Sn and Cu_6Sn_5 type of intermetallics as Nickel is one of the best known barrier metals. Packages with Ball on pad type of structure in general, had better fatigue life as compared to Ball on RDL structure. The failure mechanism was concluded to be solder fatigue as for most of the failures the crack was observed through the bulk solder on package side. It was also noted from weibull plots that there exists only one failure mechanism which is confirmed by only one slope obtained in the weibull plot. Types of failures in accelerated thermal cycling were classified into five different failure modes namely mode 1 to

mode 5 depending on the location of crack in the structure. Most of the failures fit in the mode 1 type of failures (crack through bulk solder on package side). Effect of different structural parameters on weibull parameter was also studied. It was prominent from weibull plots increasing the dielectric thickness didn't really helped the fatigue life for 300μm SAC 305 ball structure with a dielectric thickness of 7μm had better reliability in terms of number of cycles than 12μm dielectric structure. However, increasing dielectric thickness proved to be useful for 350μm ball. Thus, it can be said that the dielectric thickness and solder ball diameter and hence height are the most important parameters controlling the fatigue life. In the next section accelerated thermal cycling is done computationally to confirm the failure mode obtained in the experiments.

5.6 Computational validation of Accelerated thermal cycling

Although the experimental accelerated thermal cycling is an effective way to qualify WLCSP assemblies, it takes lot of time and money to get the results in this so called build and test type of approach. Moreover, there is only a limited number of packages one can test and that too without changing the temperature extremes. Therefore, in addition to the experimental accelerated thermal cycling it is essential to simulate the accelerated thermal cycling conditions on a packaging assembly model to assess its reliability and make appropriate material, geometry and process modifications to enhance the overall reliability. Figure 5.13 shows a typical accelerated thermal cycling cycle that is very widely used in microelectronics packaging industry. As can be seen from the figure 5.13 the cycle contains two ramps, ramp up and ramp down which essentially go from -40℃ to 125℃ and v ice-versa. The cycle also contains two dwells at the two temperature extremes namely high dwell and low dwell. From loading point of view the ramps are essentially for the plastic loadings and dwells are essentially for the creep loading. In thermal cycling simulations it is usually assumed that the entire packaging assembly is at the same uniform temperature without any thermal gradients and is at equilibrium with the thermal chamber throughout the cycle. Although, such an assumption is often reasonably

correct, for the sake of simplicity it is used and the stress-strain distribution in the solder interconnects is obtained. It is also possible to get thermo-mechanical stress contours in the assemblies by performing thermo-mechanical simulations. Such thermo-mechanical stress, strain and Viscoplastic strain energy density contours are used to determine the stress strain distribution in the package / board assembly and fatigue life of solders. Themo-mechanical simulations are also used to predict the failure mode that will be observed in experiments.

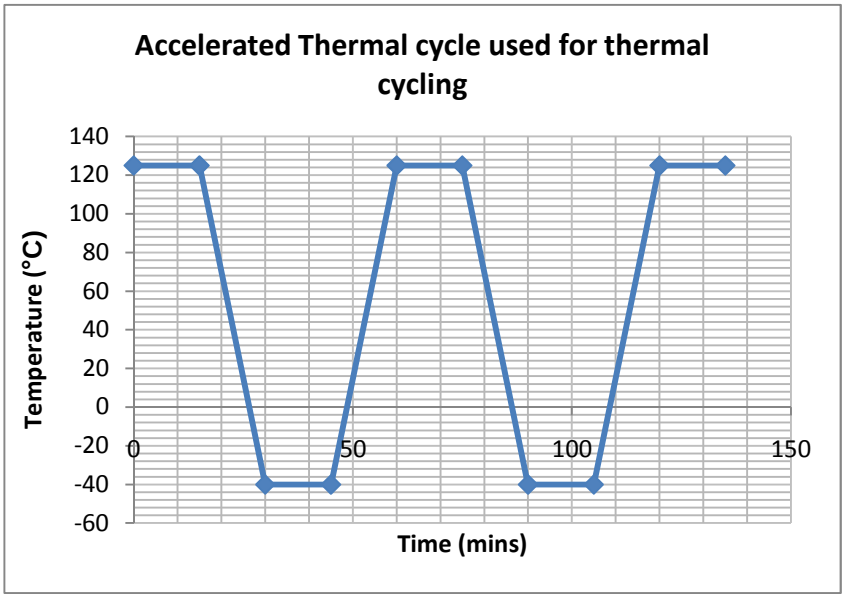
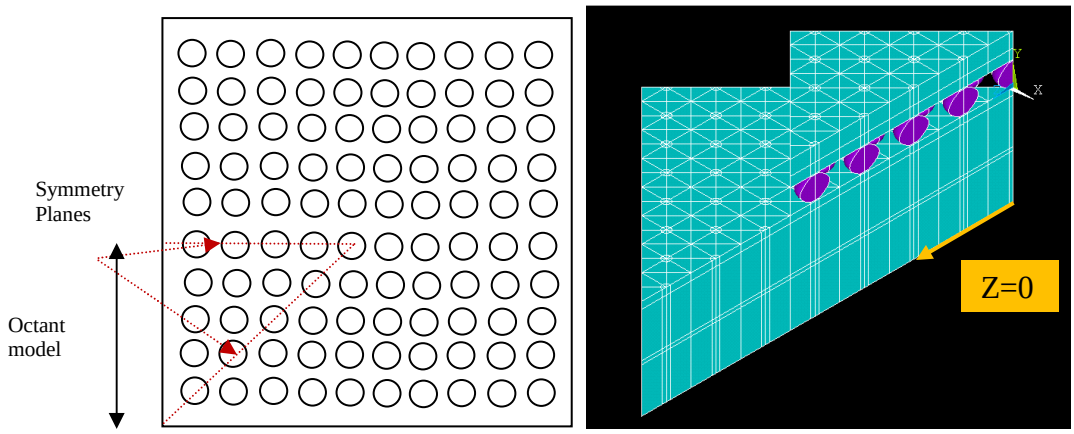


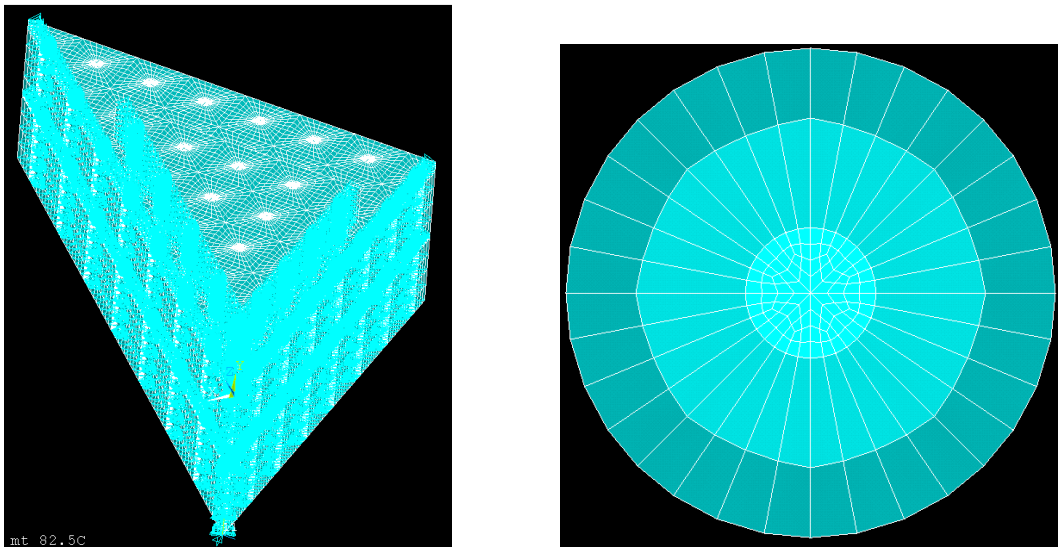
Figure 5.13: Standard accelerated thermal cycle used for accelerated thermal cycling of electronic assemblies

In this study, a Wafer level Chip Scale Package is being tested thermo-mechanically using ANSYS® classic. Description of the chip is as follows: a solder bump array of 10 by 10 solders. For simplicity and CPU time saving a 1/8th model is considered. Figure shows the symmetry planes and octant model used in the study. The solder bumps are attached to a four layer board with two signal layers and two power layers. Figure shows the 1/8th model considered in this study. Two types of elements were used in this study. All the solids in green section in the model were meshed by SOLID45 elements whereas all the solder bumps that are shown in purple section are meshed in VISCO107 elements. Since the purpose of this model

was to see the potential relationship with wafer level ball shear test. The model was positioned in such a way that the Z axis coincides with the symmetry plane. Table 5.2 gives the material properties that were supplied to the model.



(a) (b)



(c) (d)

Figure 5.14: WLCSP model under consideration (a) schematic (b) Octant Model (c) Mesh with Boundary Conditions and (d) Mesh on Solder Ball.

The FR4 test board for the wafer level chip scale packages considered in this study was expanded to the dimension of a JEDEC standard JESD51-5 four layer test board. The

dimension of the board considered was equal to the dimension of the board around package on the actual board. The 4 layer test PCB is modeled as a 1.57 mm thick which includes (1) 0.070 mm thick upper and lower trace layers (2) 0.035 mm thick internal power planes and (3) 0.45 mm thick core layers. Trace layers and layer thicknesses between the layers. Figure 5.14d display the symmetry of finite element model trace patterns for the PWB. A commercially available finite element analysis software tool (ANSYS) was applied for the thermo-mechanical simulation purposes. All three dimensional finite element model structures utilized SOLID45 for board, package and other structures except solder ball. Solder ball was assumed to be viscoplastic in nature and was solved by using Unified constitutive model (ANAND's model)

The model was meshed using structurally mapped mesh. The alterations in geometry were done using ANSYS APDL script in order to make sure that all the areas of model are meshed using structurally mapped mesh.

Table 5.2: Material properties used in the model

Component	E (MPa)	CTE (1/K)	Poisson Ratio
Ball (SAC 305)	38700	$21x10^{-6}$	0.35
Ball (SAC 405)	40000	$20x10^{-6}$	0.38
Die	162716	$-5.88x10^{-6}$ +6.261-8T-1.610-10T^2 +1.510-13T^3	0.28
Copper	128932	13.8x10-6	0.34
PCB	27294-37T (XY) 12204-16T(Z)	$16.0x10^{-6}$(XY) $84.0x10^{-6}$	0.39(XY&YZ) 0.11(XY)
Substrate	4137	$30.0x10^{-6}$	0.4
Substrate Mask	3914	$60.0x10^{-6}$	0.47
Mold Cap	15513	15.8x10-6	0.25
Dielectric	2700	$42x10^{-6}$	0.340

Figure 5.14c shows the mesh that was used to solve the problem figure also shows the local refinement done at the solder ball level. Symmetric boundary conditions were applied on

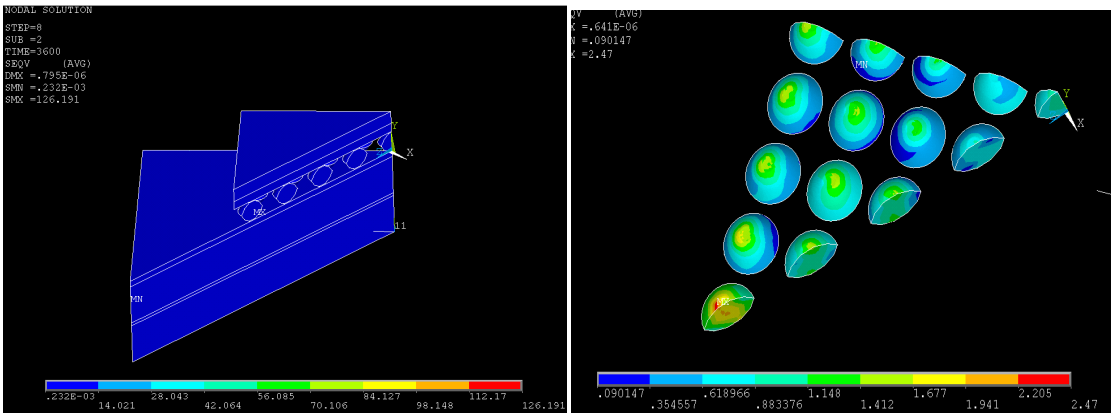
the lines drawn in the earlier figure. ANAND's model was used to model the visco-plasticity of solder interconnect. In this study, only SAC 305 and SAC 405 solders are considered in computational studies. Due to lack of material properties SAC 125Ni solder, it was not studied computationally. Two structures namely ball on pad and ball on RDL is used in this study.

Table 5.3: Anand's constants for SAC 305 and SAC 405 solder [41]

No.	Symbol	SAC 305	SAC 405
1	So (MPa)	45.9	20
2	Q/R(K)	7460	10561
3	A (1/s)	5870	325
4	α	2	10
5	M	0.0945	0.32
6	Ho	9350	8000
7	S	58.3	42
8	N	0.015	0.02
9	a	1.5	2.57

5.7 Results and Discussion- Accelerated thermal cycling

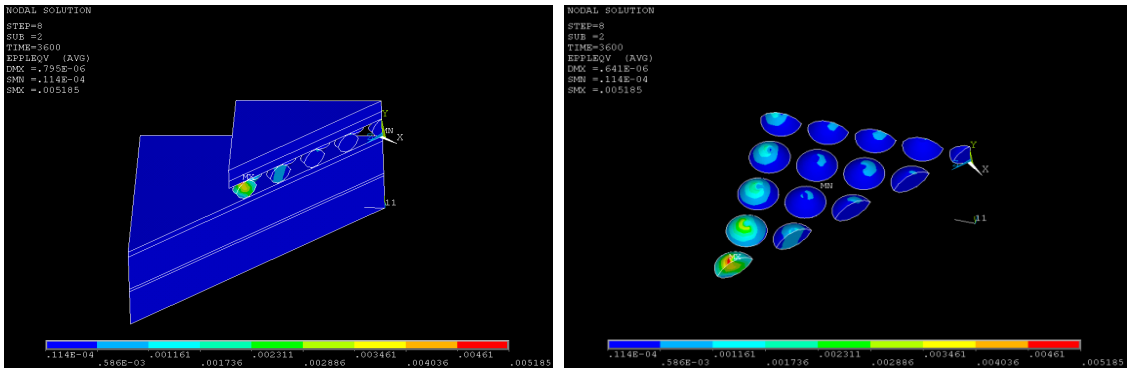
Figures 5.15, 5.16 and 5.17 show the Von-Misses stress, plastic strain and plastic work were observed the model at the end of second cycle.



(a) (b)

Figure 5.15: Simulation of the octant model (a) Von-Misses stress in complete model (b) Von-Misses stress in solder bumps.

It can be seen from figure 5.15b that the maximum stress is observed on the corner most bump. This failure mode is exactly what was observed in the experimental study hence the boundary condition applied in the model are correct and help in validating the data. Figure shows the plastic work induced in the solder bumps, it can be observed from this figure too that the corner bump was the most stressed bump in the entire package and that is consistent with the DNP effect that is observed in the typically observed in electronic packaging assemblies. Figure shows the inelastic strain induced in the solder bumps and the entire assembly at the end of packaging.



(a) (b)

Figure 5.16: Simulation of the octant model (a) Von-Misses strain induced in complete model (b) Von-Misses strain induced in solder bumps

Plastic work induced in the solder bumps at the end of accelerated thermal cycling

In this study VISCO107 elements were used to model solder bumps. Plastic work is the output of visco-plastic elements. Hence in the figure only solder bumps are seen with plastic work and everywhere else is just blue which corresponds to 0 plastic work. Figure shows the Viscoplastic strain energy density of solder which corresponds to ΔW_{ave} in the fatigue life approach.

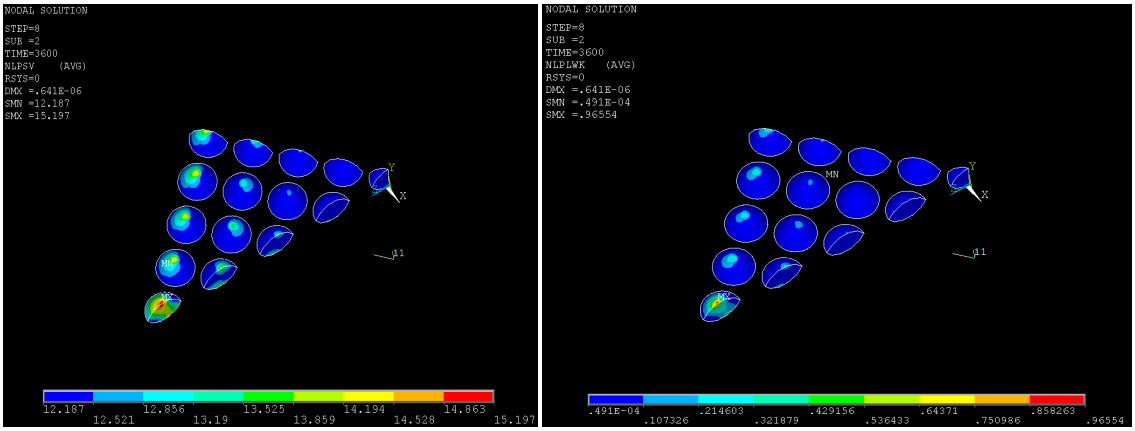


Figure 5.17: Simulation of the octant model (a) plastic work variable and (b) plastic work/volume

Fatigue life of the solder bumps is calculated by using Darveaux's life prediction approach. Equations 5.1 give the number of cycles required for crack initiation, equation 5.2 gives the number of cycles required for crack propagation and equation 5.3 gives addition of

number of cycles that were used to crack initiation and crack propagation and calculates the fatigue life.

$$N_o = C_3 \Delta W^{C4}{}_{ave} \tag{5.1}$$

$$\frac{da}{dN} = C_5 \Delta W_{ave}{}^{C_6} \tag{5.2}$$

$$\alpha = N_o + \frac{a}{\frac{da}{dN}} \tag{5.3}$$

Where N_o is the number of cycles required for crack initiation, da/dN is the number of cycles required for crack propagation and α is the fatigue life of solder bump. Characteristic life α is equivalent to 63.2% of lifetime of the solder joint. Table 5.1 shows the number of cycles obtained by numerical prediction and its comparison as with experiments. In case of 250μm solder joint this value corresponds to 20% or error between experimental thermal cycling and computational thermal cycling.

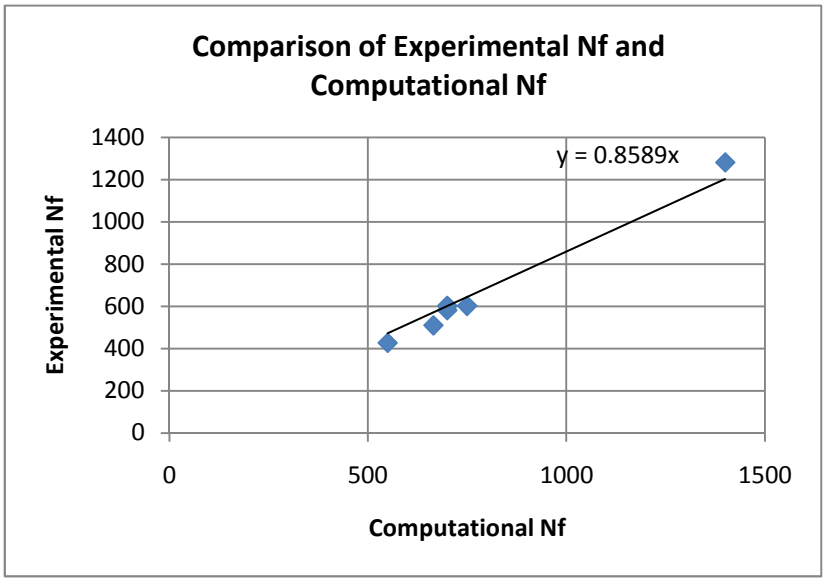


Figure 5.18: Experimental Cycles to failure Vs Computational cycles to failure

Figure 5.18 shows the comparison of experimental cycles to failure and computational cycles to failure. In figure 5.18 the intercept of trend line has been set to zero. In general it can be observed that there is an error of around 15% amongst various cases considered.

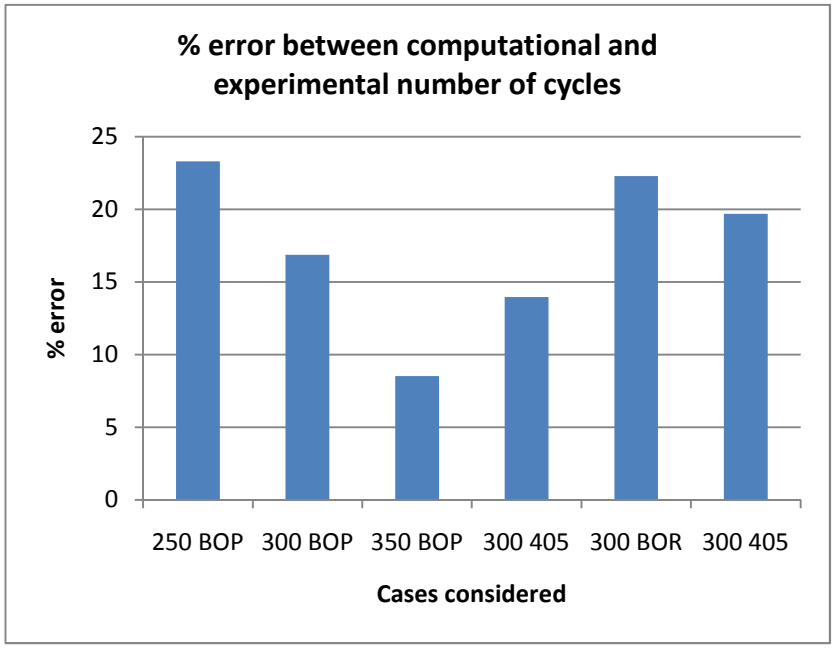


Figure 5.19: % Error in between computational life cycles and experimental life cycles

Figure 5.19 shows the % error in different cases that were considered in both experimental thermal cycling life and computationally calculated thermal cycling life. In general it was observed Darveaux's model over predicts the fatigue life as compared to experimentally calculated fatigue life by around 20%. There are two possible sources which be contributing to the error (a) Darveaux's approach of determining fatigue life is very much dependent on mesh and (b) the failures were determined by measuring electrical resistance. Electrical resistance of packages was measured after every 100 cycles when the environmental chamber was stopped for de-freezing.

The aims of performing accelerated thermal cycling in this study are to investigate possible failure mechanisms that exist in the package and to see if there is any possible correlation with the ball shear testing that was done in prior part of the study. Monotonic loading

can be compared to cyclic loading using Basquin's equation. In order to use the data obtained by thermal cycling in the Basquin's equation obtaining a stabilized hysteresis loop is extremely important. It has been a proven fact from bauschinger's effect that a fatigue cycle stabilizes after a number of cycles as the amount of inelastic strain that builds up in the solder joint becomes constant. In the current study, the model was thermal cycled for 10 cycles and at the end of 10 cycles a stabilized Hysteresis loop was observed. The criteria for having a stabilized hysteresis loop was that the changes between maximum and minimum shear stress induced in the corner most solder joint should not be more than 0.001 MPa, at the end of loop 10 the model finally stabilized. Figure 5.20 shows the hysteresis loop observed in corner most solder bump. Area under the hysteresis loop essentially represents the strain energy that is stored in the solder bump. Higher the area under hysteresis loop lower is the fatigue life. As the number of cycles increases the Viscoplastic strain energy density also increases per cycle. Figure 5.21 shows the Viscoplastic strain energy density which is nothing but the Viscoplastic strain induced in each solder per volume or it is also called as the plastic work/volume.

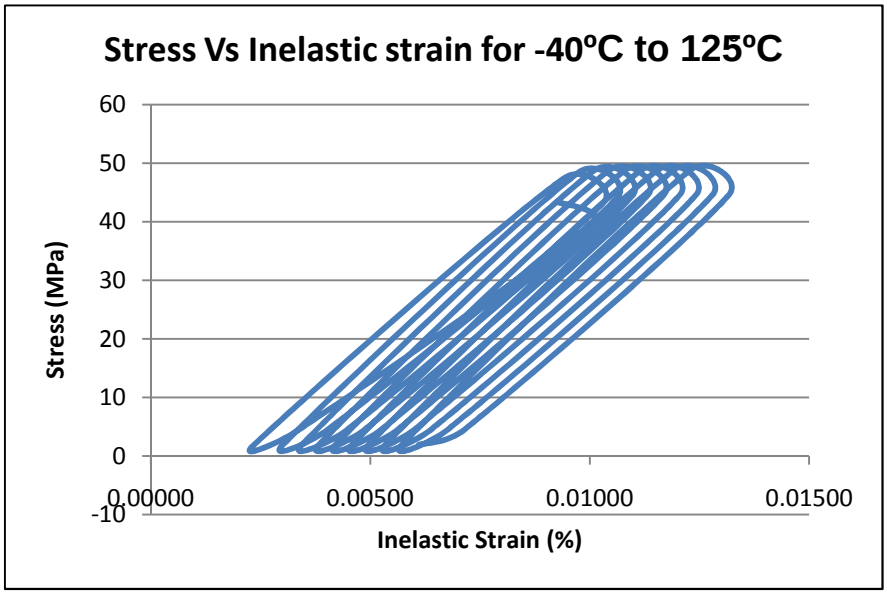


Figure 5.20: Hystersis loops observed in the corner most solder bump.

A stable hysteresis loop essentially has the same extremes of stresses and strains as the loops that come after the stable loop. This hysteresis loop is obtained for temperature extremes of -40ºC to 125ºC which corresponds to the mean temperature of 82.5ºC. Hence, in figure 5.20 a ratcheting effect is observed, because of the non-zero mean stress in this case mean temperature. Figure 5.21 shows the stable hysteresis loop. Area under the hysteresis loop essentially represents the strain energy that is stored in the solder bump. Higher the area under hysteresis loop lower is the fatigue life. As the number of cycles increases the Viscoplastic strain energy density also increases per cycle.

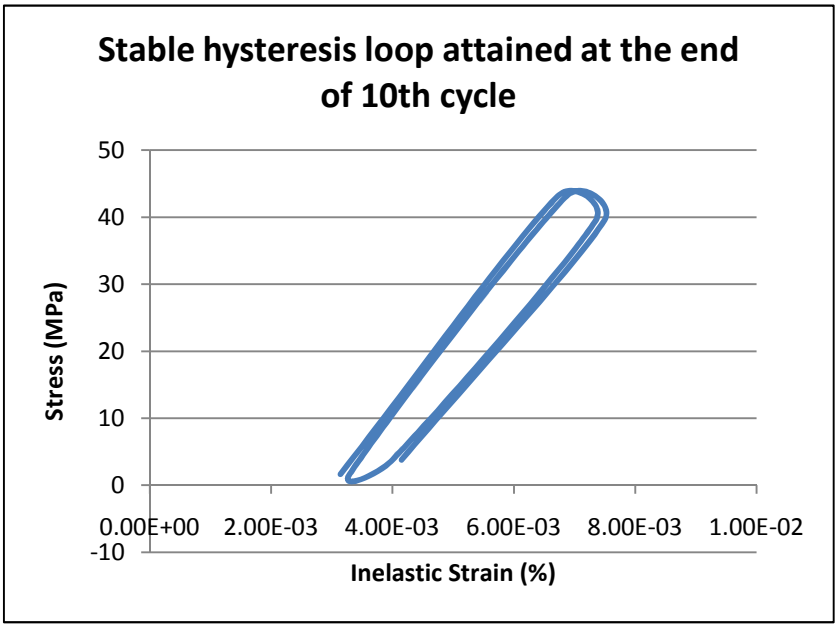


Figure 5.21: Stable hysteresis loop obtained at the end of 10th cycle.

Figure 5.22 shows the Viscoplastic strain energy density which is nothing but the Viscoplastic strain induced in each solder per volume or it is also called as the plastic work/volume.

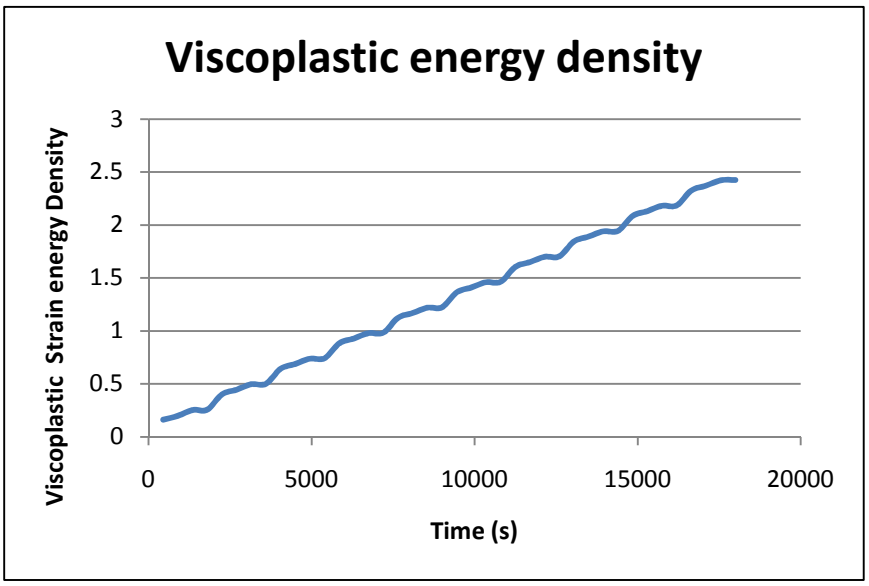


Figure 5.22: Viscoplastic strain energy density build up in corner bump over time.

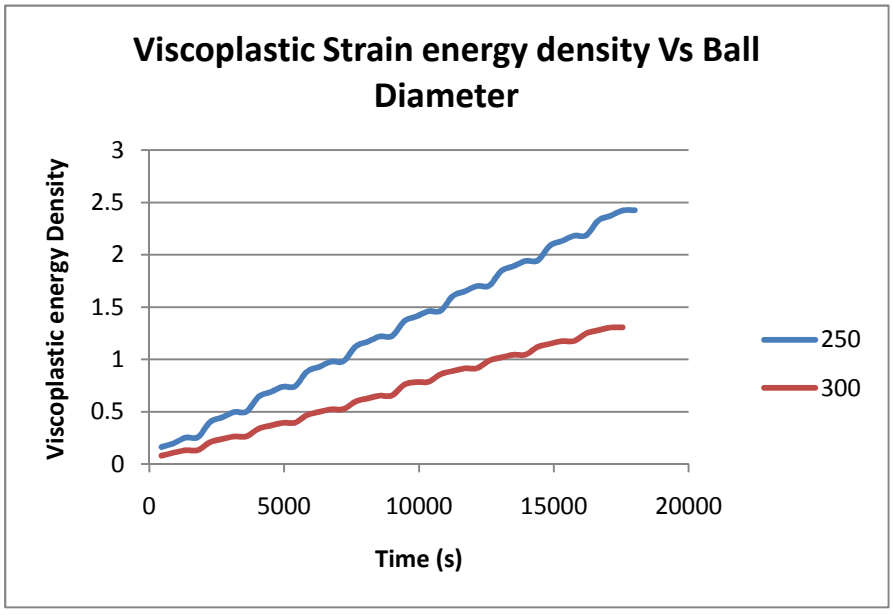


Figure 5.23: Effect of ball diameter on Viscoplastic strain energy density

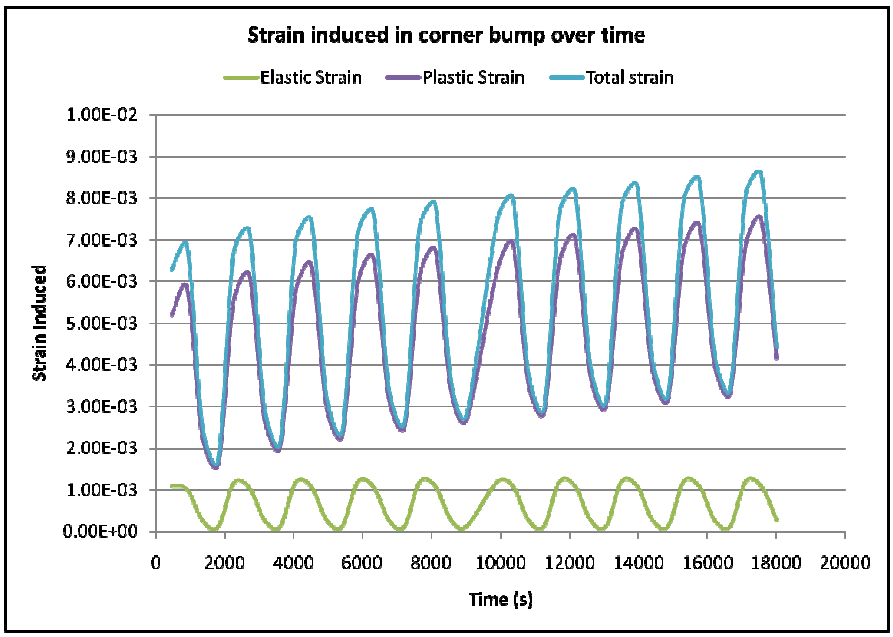


Figure 5.24: Comparison of Elastic and Inelastic strain induced in Corner solder bump with time

Figure 5.23 shows the effect of standoff height on Viscoplastic strain energy density of solder interconnects. It can be seen that the Viscoplastic strain energy density reduces as the standoff height and hence ball diameter increases. In order to confirm that the strain induced is elastic or plastic a time variable plot of elastic strain plastic strain and total strain was plotted against time and it was absolutely clear that the elastic strain typically stays constant per cycle whereas the plastic or inelastic strain is increasing per cycle as noted in figure 5.25. It can be observed from figure that the elastic stress stays fairly constant at 1E-03 whereas the inelastic (plastic strain) goes from 6E-03 to 7.5E-03 which is equivalent of 20% increase in the shear inelastic strain induced in the solder bump. Equation 5.4 gives a relationship between strain range and package parameters and boundary conditions applied in the accelerated thermal cycling process.

$$\Delta\gamma = \frac{L \cdot \Delta\alpha \cdot \Delta T}{h} \qquad 5.4$$

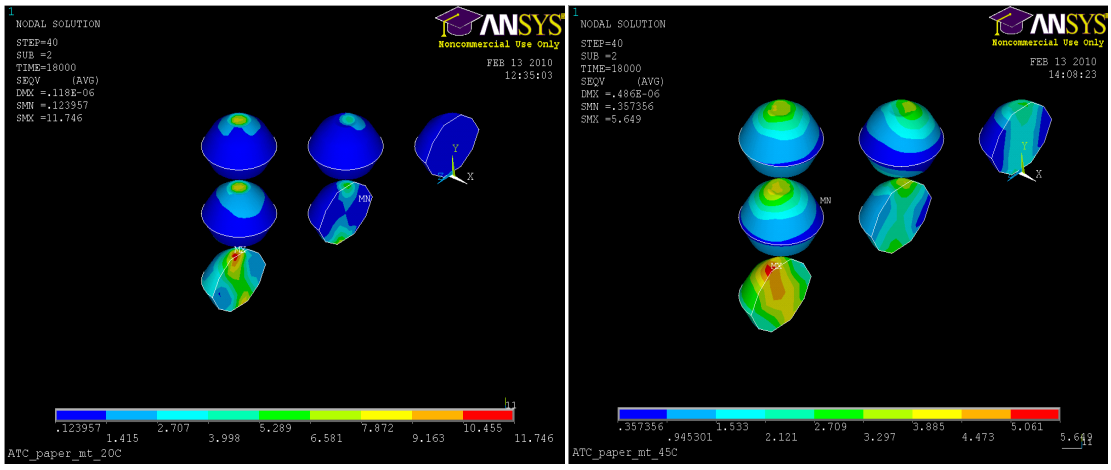
Where L is the Distance to Neutral Point of the package under study, Δα is the difference between the Coefficient of thermal expansion between package and board, ΔT is the difference in temperature extremes and h is the standoff height of C5 (between package and board) solder bumps. DNP, standoff height and CTE mismatch are related to the package and board. Thus, one can note that for varying the strain range, varying the temperature extremes is the only knob can be varied practically in a test run.

5.8 Effect of mean stress on fatigue life of solders

Accelerated thermal cycling is a fatigue loading where the stress is provided by temperature. Fatigue life of electronic packages is affected by the mean stress of Fatigue loading. It was observed that in the previous study that due to non-zero mean temperature ratcheting effect was observed in the hysteresis loop. To study the effect of mean stress four different temperature extremes were considered. There were two aims for this particular study; a) to observe changes in hysteresis loop because of change in mean temperature and b) change in temperature extremes affect the strain rate that with which the strain is induced in the solder. In this part of dissertation four different extreme cycles were considered as shown in table. Table 5.4 shows the temperature extremes and the mean temperatures. In fatigue loading temperature extremes are very important because they control the strain energy induced in the corner bump. Figures 5.25 and figures 5.26 show the Von-Misses stresses induced in solders at different mean temperatures. In these figures only half of all the bumps considered are shown as the maximum stress and minimum stress both appeared in the same region of package.

Table 5.4: Temperature extremes and corresponding mean temperatures considered in this study

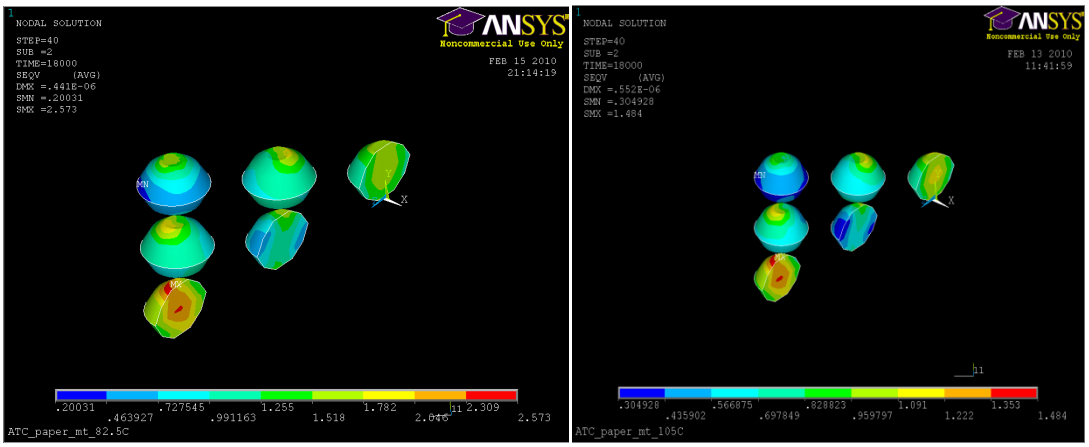
Number	Temperature limits (°C)	Mean Temperature(°C)
1	-10°C to 30°C	20°C
2	-15°C to 85°C	50°C
3	-40°C to 125°C	82.5°C
4	-55°C to 155°C	105°C



(a) (b)

Figure 5.25: Von-Misses stress for various mean temperatures (a) 20C and (b) 45C

Figures 5.26 (a) and 5.26(b) show the Von-Misses stress for mean temperatures of 82.5℃ and 105℃.



(a) (b)

Figure 5.26: Von-Misses stress for various mean temperatures (a) 82.5℃ (b) 105℃

The results obtained in figure are consistent with rest of the data as the most stressed bump is essentially the corner bump. As it can be noted, from figure 5.27 that as mean temperature of the accelerated thermal cycling Von-Misses stress induced in the corner bump increases. Figures 5.27-5.29 show the time-history plots of effect of Von-Misses stress, inelastic strain and Viscoplastic strain energy density for corner bump.

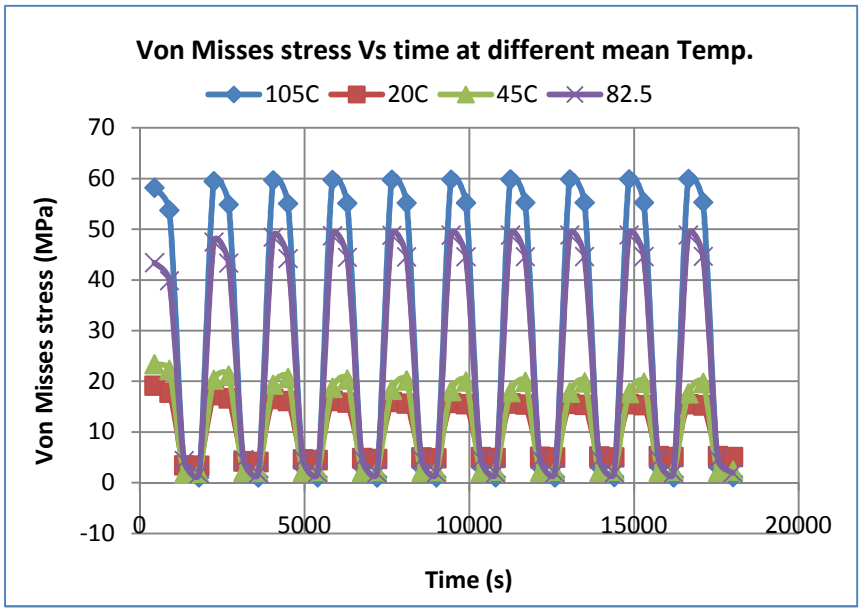


Figure 5.27: Von-Misses stress of corner bump at various mean temperatures

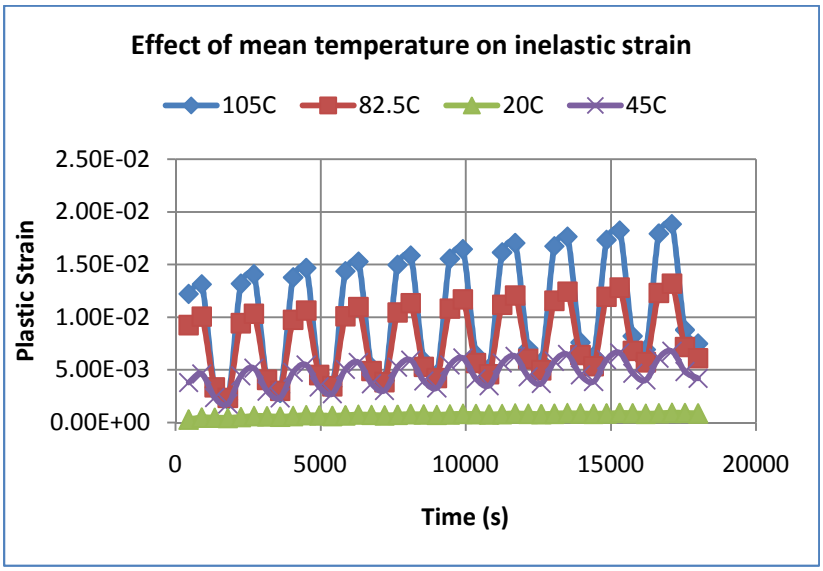


Figure 5.28: Von-Misses inelastic strain of corner bump at various mean temperatures

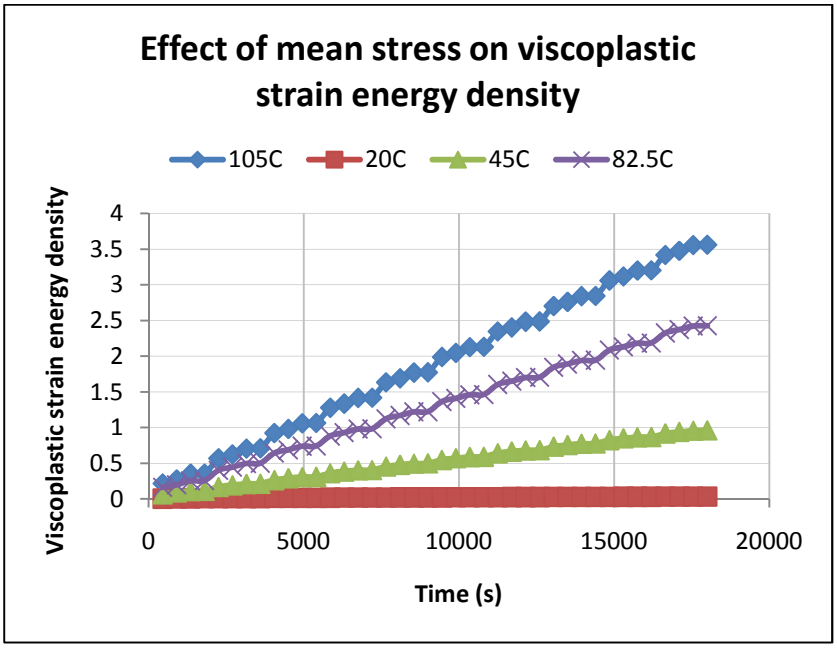


Figure 5.29: Effect of mean stress on Viscoplastic strain energy density for corner bump

It can be clearly seen from figure 5.29 that mean temperature severely affects the Viscoplastic strain energy density. For mean temperature of 0℃ the Viscoplastic strain energy density is almost equal to 0 and it increases as the mean temperature increases and it is a known fact that Viscoplastic strain energy density increases the fatigue life decreases.

5.9 Hysteresis loops obtained at different mean temperatures considered

As mentioned in section 5.6 that in order to use data from accelerated thermal cycling has to come from a stabilized hysteresis loop. Hence, accelerated thermal cycling of packages was done at mean temperature of 20℃. It can be obs erved from 5.30 that at the end of cycle 10 the loop becomes stabilized. Note that the stress range for this case is between 5MPa to 15MPa.

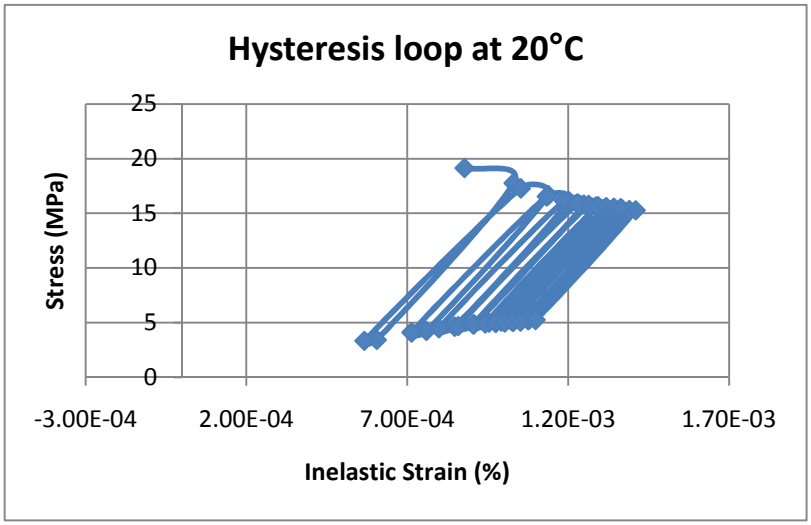


Figure: 5.30 Hysteresis loop obtained for corner bump at 20℃ mean temperature

It can be observed from 5.31 that at the end of cycle 10 the loop becomes stabilized. Note that the stress range for this case is between 2.5MPa to 20MPa.

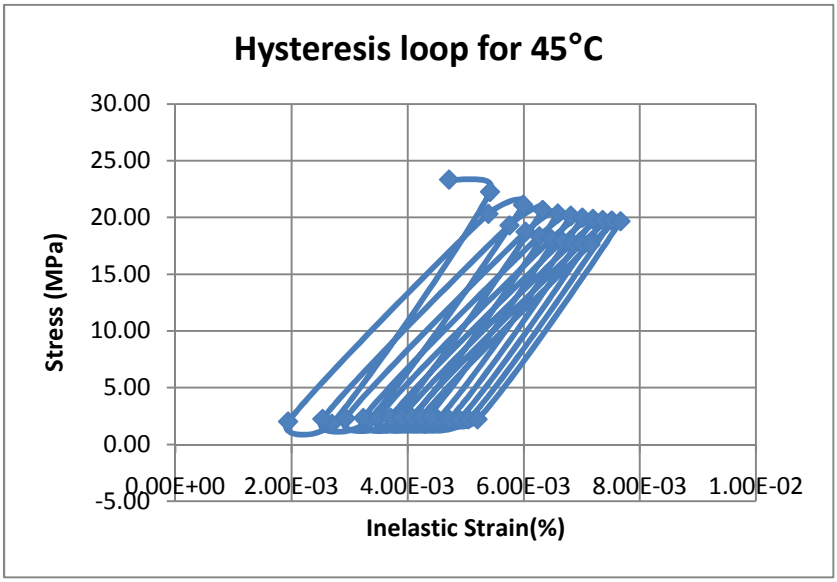


Figure 5.31: Hysteresis loop obtained for corner bump at 45℃ mean temperature

It can be observed from 5.32 that at the end of cycle 10 the loop becomes stabilized. Note that the stress range for this case is between 0MPa to 50 MPa.

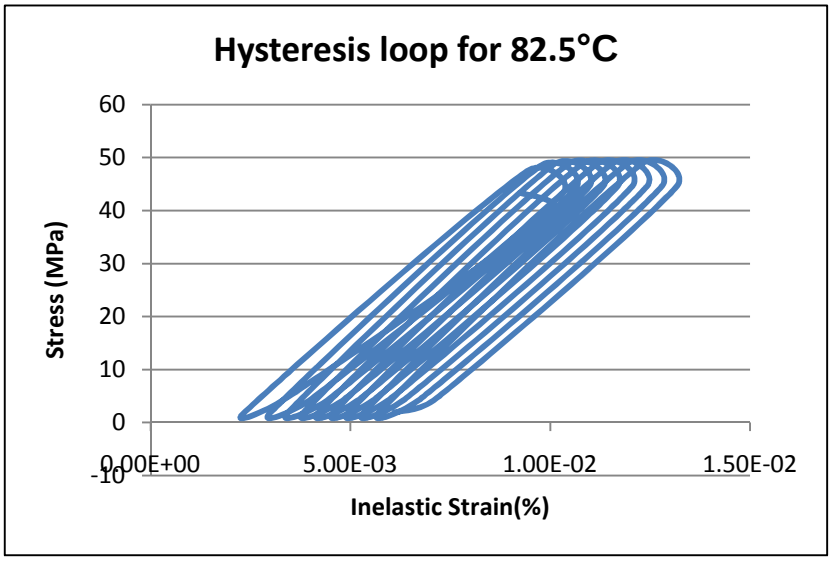


Figure 5.32: Hysteresis loop obtained for corner bump at 82.5℃ mean temperature

It can be observed from 5.33 that at the end of cycle 10 the loop becomes stabilized. Note that the stress range for this case is between 0MPa to 60MPa.

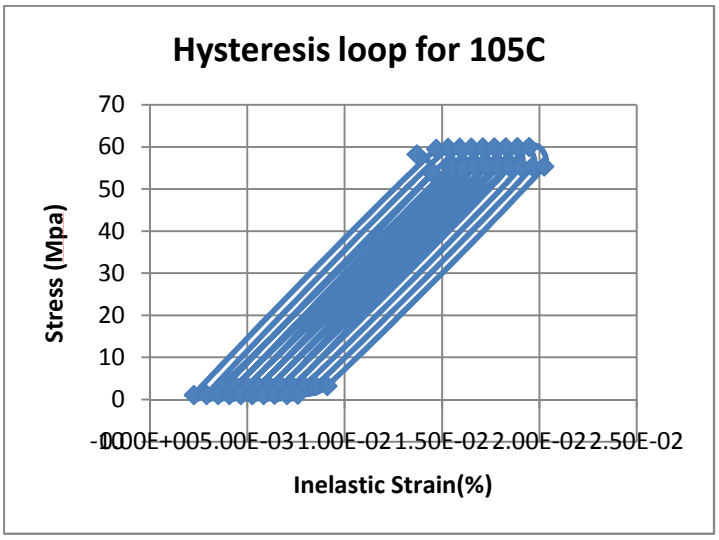


Figure 5.33: Hysteresis loop obtained for corner bump at 105℃ mean temperature

Figure 5.34 show all the stable hysteresis loops at different strain rates at different mean temperatures and hence at different inelastic strain.

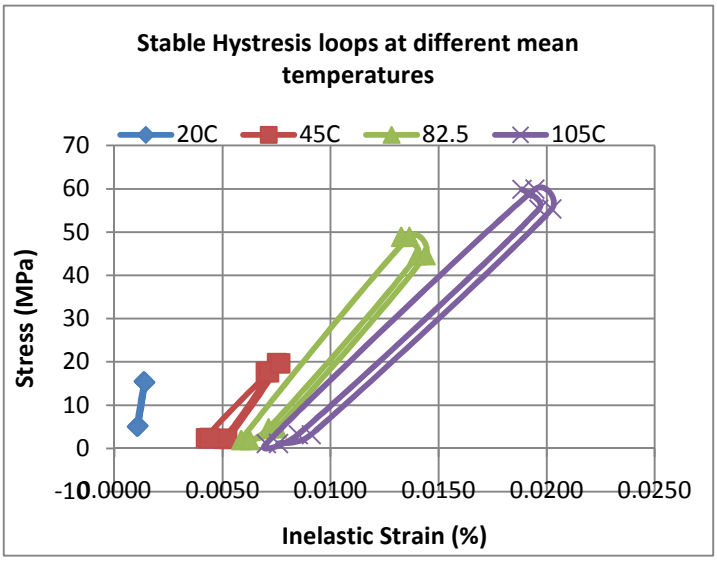


Figure 5.34: Stable hysteresis loops obtained for corner bump at different mean temperatures

A procedure that is generally followed in creating a monotonic loading curve from cyclic loading is to join all the points of the stable hysteresis loops together. Figure 5.36 shows points of top points of all the hysteresis loops.

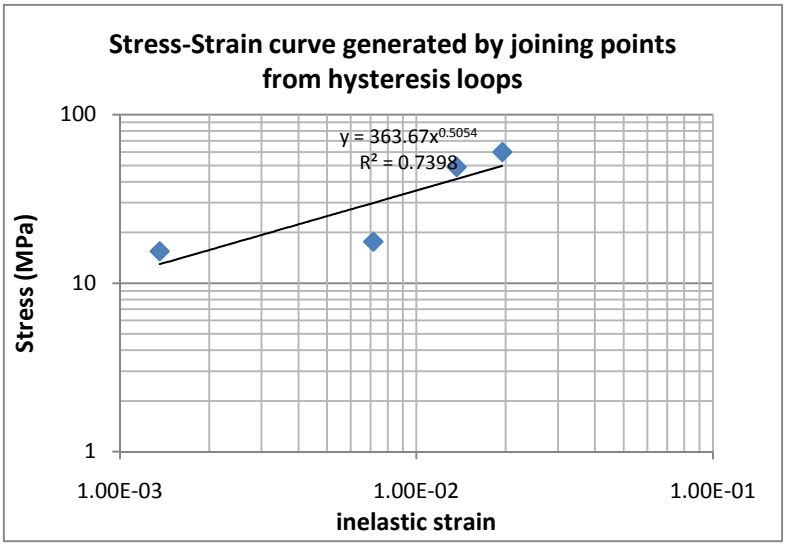


Figure 5.35: Monotonic loading curve generated by joining points of hysteresis loops

All the points from upper section of hysteresis loop were put together and were curve-fitted with a power law with a strain hardening exponent of 0.50 for solder. In next chapter, the curve obtained by cyclic loading is compared with monotonic loading curve obtained by ball shear test.

5.10 Conclusion from Accelerated thermal Cycling Tests

The following were the conclusions that can be drawn from the accelerated thermal cycling tests.

- 1/8th model of the complete package was used to model the wafer level chip scale package that is meshed structurally using SOLID45 and VISCO107 elements. All the configurations that were tried in chapter 4 were modeled in chapter 5 mounted on a 4 layer board.
- Properties of SAC 305 and SAC 405 were taken from literature and used in ANAND's model to simulate the lead free solder. Darveaux's model was used to post-process and calculate the life in number of cycles. The solder bump was integrated over the 10% from the package side. It was predicted by the finite element model that the failure will

occur on package side and this was correct as a similar failure mode was observed from experiments.

It was confirmed from this chapter that the element choices and the failure reliability models predicted the failure mode and number of cycles with sufficient accuracy

CHAPTER 6

CORRELATION BETWEEN WAFER LEVEL RELIABILITY AND BOARD LEVEL RELIABILITY

6.1 Literature Review

Traditionally, ball shear has been used to gauge the quality of WLCSP interconnects. One can note from the failure signature that accelerated thermal cycling and ball shear have similar failure signatures. Accelerated thermal cycling is one of the commonly used accelerated tests for characterizing board level WLCSP packages. It is however, not feasible from an economical standpoint to use accelerated thermal cycling to monitor the quality of WLCSP interconnects. Well defined test methods capable of detecting brittle fracture failure methods are needed that will allow for testing at interconnect/component level. It is clear from previous chapters that in this dissertation three types of solders, in three sizes are mounted on two different types of structures. The packages have been tested on wafer level packaging using ball shear test and similar packages are mounted on JEDEC level accelerated thermal cycling board. These boards are thermally cycled using standard accelerated thermal cycle. Ball shear test aand ing general wafer level testing can be performed in a quick, efficient way as compared to board level drop testing.

Establishing correlations between board level package reliability and wafer level package reliability has been reported in literature. Valota et.al [56] assessed the feasibility of component level pull testing to establish a correlation between board level drop reliability tests for plastic BGA packages. Valota concluded that the impact life parameter from weibull analysis of drop test results is inversely-correlated with the incidence of brittle fracture in pull testing of BGA solder joints. The non-ductile fracture mode incidence in pull testing can be used as an indicator of board level drop test performance. Song and lee [57] investigated the effect of IMC thickness on the attachment strength of Sn3.5Ag and SAC405 solder balls with cold bump pull

method. They concluded that ball pull is a better metric in evaluating the brittle fractures in solder joint due to intermetallic formations. Song et.al investigated joint strength and fracture energy of lead free solder balls in high speed shear/pull tests and obtained correlations with board level drop tests. Song et.al investigated shear tests were done at 10,100, 500, 1000 and 3000 mm/s and pull speeds were done at 5, 50, 100, 250 and 500 mm/s. In this publication a new metric energy was developed and was proved to be a better metric as compared to force and failure mode. Johnson et.al [73] concluded that high speed shear and high speed cold ball pull are valuable tools in gauging board level drop test performance. The drawback of high speed shear and cold ball pull is that these techniques are destructive in nature hence cannot be used for product wafer testing. As the products wafers are very expensive to break for testing. It has been reported that cold ball pull test is at least twice as expensive as compared to the conventional ball shear test and moreover are very much subjected to operator skills [74].

In this study, correlations are established based on two factors. In the first metric cyclic stress, strain and monotonic stress, strain is superimposed on each other on a log-log plot. In the second type of metric statistical correlations are established based on ANOVA without replication analysis. The confidence level for ANOVA two factor without replication was 95%. The two factor without replication form of ANOVA analysis was used because in this study we are not repeating experiments for the same variable. In the current study, the ANOVA two factor without replication was setup in Excel [75]. When it was confirmed that the null hypothesis was acceptable for the particular set of measurements CORREL [75] function was applied to determine correlation coefficient for those set of experiments.

6.2 Assumptions considered in Comparing the two tests and different metrics for comparison

Following are the assumptions considered in this comparison

- An important point in this study is that only failures which can be classified as mode 1 failure in accelerated thermal cycling are only considered. This implies that the primary failure mechanism for the failure is solder fatigue.
- If the failure mechanism is any other of the modes described or even more than one active failure mechanisms within the package the correlations might not give accurate results.
- Any failure which is related to pad cratering, pad side intermetallic or any other failure on board side cannot be predicted using this methodology.

In chapter 5, a detailed study of accelerated thermal cycling at various inelastic strain rates was performed primarily by changing the temperature extremes. Figure 6.1 shows the figure obtained by joining points that occur in first quadrant of for the stable hysteresis curves. As mentioned in chapter 2 any cyclic stress-strain curve can be approximated to be a power law expression. Based on this assumption a trend line with least square fit at a confidence level of 95% and following a power law was approximated with the data points. It can be clearly seen from figure 6.36 that the trend line fits the data with a regression fit of 0.73. In a very similar way a power trendline was set to match the monotonic loading which is ball shear in this case. The two curves were superimposed on each other at the same inelastic strains on a log log plot as shown in figure.

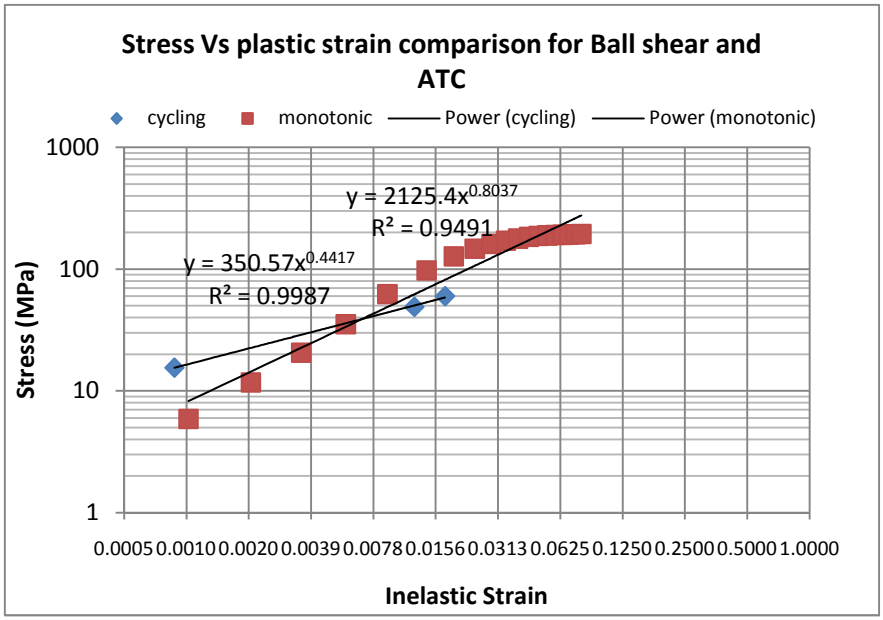


Figure 6.1: Superimposing Stress Vs Inelastic strain for monotonic loading and cyclic loading

It can be clearly seen from figure 6.1 that the two trend lines cross each other completely. The monotonic loading and cyclic loading was for 250µm RDL structure. It is crystal clear from figure 6.1 that there is no correlation between cyclic loading and monotonic loading when compared apples-to-apples. Similar type of crossing was observed for other structures too. It is confirmed that ball shear force and hence monotonic stress is not a good metric for comparing cyclic loading and monotonic loading for deriving correlations between them. Hence, for deriving correlations shear and peal mode at different heights is a better metric.

6.3 Statistical correlations between Ball shear test and Accelerated thermal cycling

6.3.1 Comparative charts between Ball shear test and accelerated thermal cycling

In order to get a feel whether there is a possibility of any correlation between the ball peal mode in ball shear test and number of cycles for accelerated thermal cycling both were put on the same axis and are compared against different metrics. Figure 6.6 shows the comparison of Number of thermal cycles and % ductile failure incidence for different types of solder bumps mounted on Ball on Pad structures. All other parameters that are part of DOE are maintained constant in this comparison.

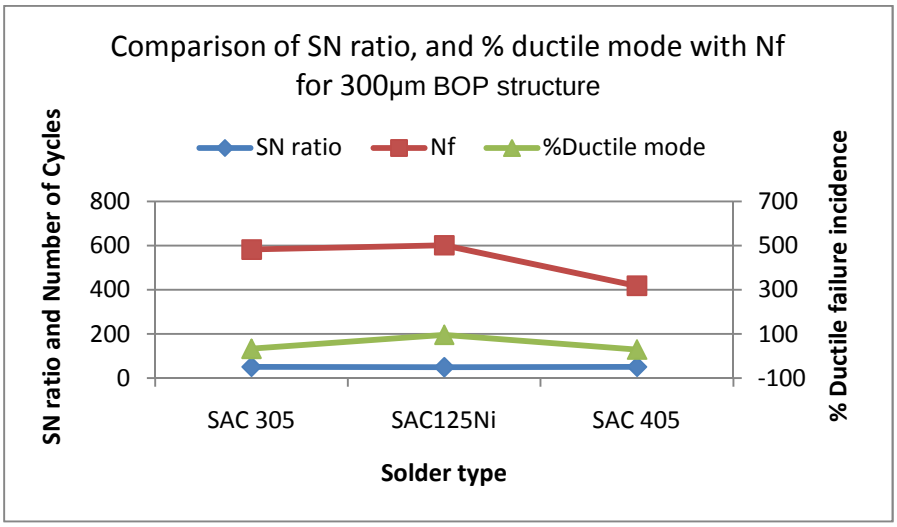


Figure 6.2 Comparing the metrics - SN ratio, % Ductile failure incidence and No. of cycles Vs different solder ball compositions for a 300µm ball with BOP structure.

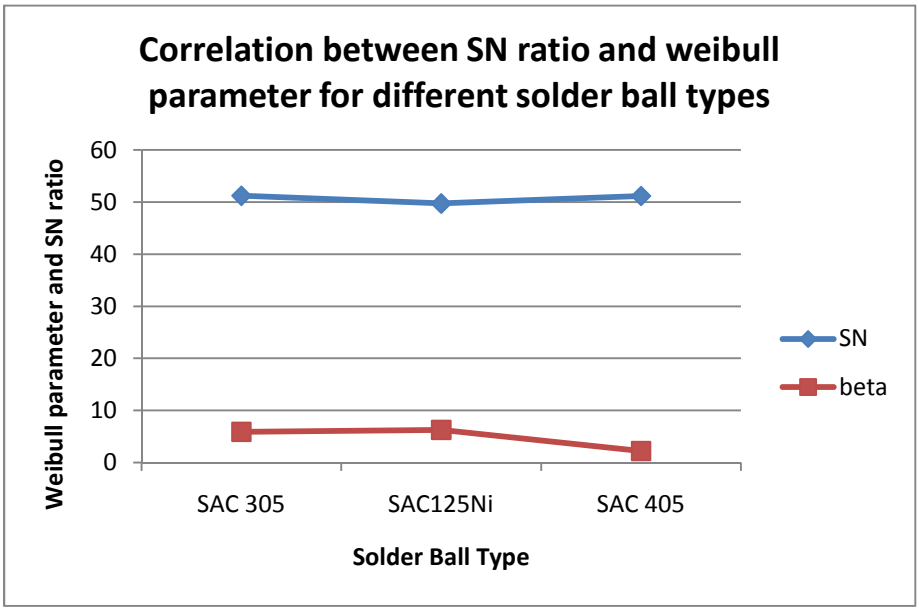


Figure 6.3: Correlation between Signal to Noise ratio and Weibull parameter for different solder compositions on 300µm solder diameter.

As it is clear, in this study ball shear and accelerated thermal cycling are being compared. The metrics used are apples to apples comparison of power law trendlines for accelerated thermal cycling and ball shear test as shows in figure 6.1. In figure 6.2 the other two

metrics namely SN ratio and % ductile failure mode from ball shear test are compared with Fatigue life from accelerated thermal cycling for different solder types on same structure and same ball size. In figure 6.2 there are two vertical axes one on left representing Signal to Noise ratio and Number of cycles and the one on left representing % Ductile failure incidence. The range of two Y axes have been matched in order to get a clear comparison as to which metric is better in predicting the solder joint reliability. It can be clearly seen that % ductile failure mode is actually a better metric as compared to SN ratio. In next few pages several of comparison charts between accelerated thermal cycling and % ductile failure mode for different configurations considered.

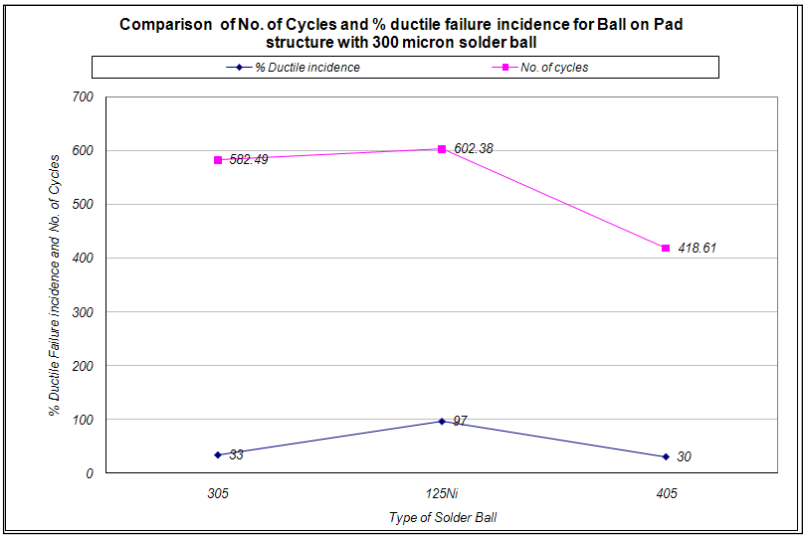


Figure 6.4: Relationship between % ductile failure incidence and No. of cycles for 300 µm ball with different solder compositions mounted on BOP structure

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Figure 6.4 show trend between % ductile failure incidences and Number of cycles of accelerated thermal cycling. In figure 6.6 the Y axis is divided into two parts from 0 to 100 is the percentage ductile failure incidence and from 100 onwards it is the no. of cycles in accelerated temperature cycling. As one can see that the distance between curves essentially reflects the

existence of correlation factor between the % ductile failure incidence which is a wafer level metric and no. of cycles in accelerated thermal cycling which is essentially a board level metric.

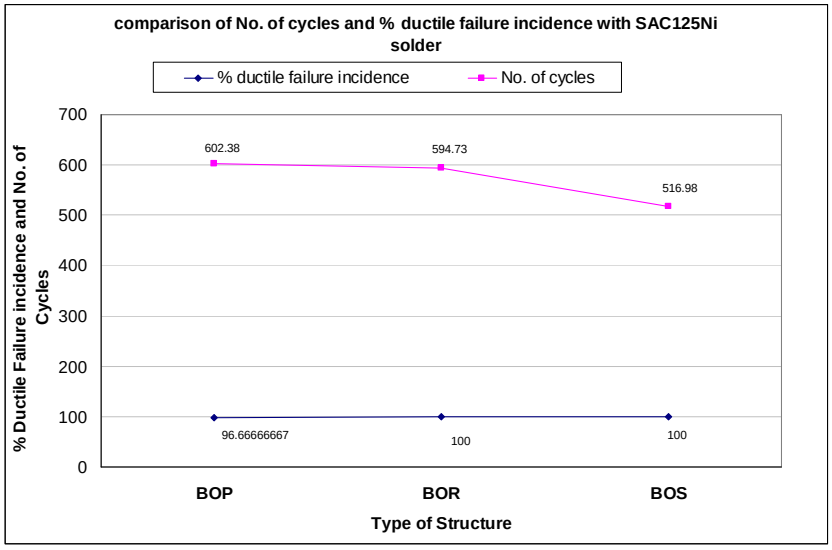


Figure 6.5: Relationship between % ductile failure incidence and No. of cycles for 300 µm SAC 125Ni ball on different structures.

Figure 6.5 shows trend between % ductile failure incidence and no. of thermal cycles for 300 µm SAC 125Ni solder in different configurations. there exist a clear coorelation between the wafer level metric and the board level metric for ball on pad and ball on RDL type of structure except that for ball on stub type of structure. In figure 6.8 the Y axis is divided into two parts from 0 to 100 is the percentage ductile failure incidence and from 100 onwards it is the no. of cycles in accelerated temperature cycling.

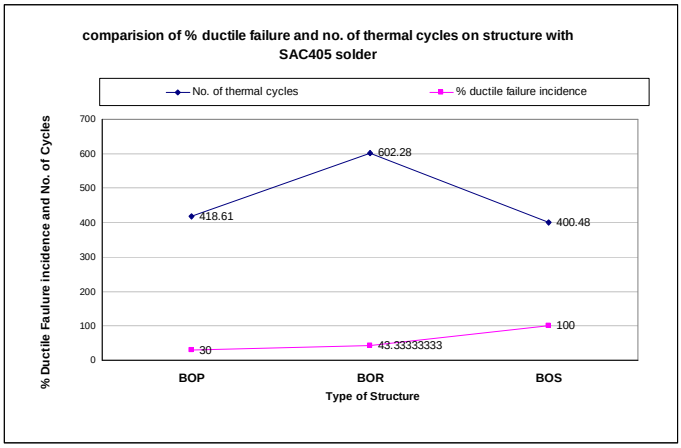


Figure 6.6: Relationship between % ductile failure incidence and No. of cycles for 300 µm SAC 405 ball on BOP structure.

Figure 6.6 shows the comparison of % ductile failure incidence and no. of thermal cycles. It can be noted from the figure that there is no particular trend between the two parameters. In figure 6.9 the Y axis is divided into two parts from 0 to 100 is the percentage ductile failure incidence and from 100 onwards it is the no. of cycles in accelerated temperature cycling.

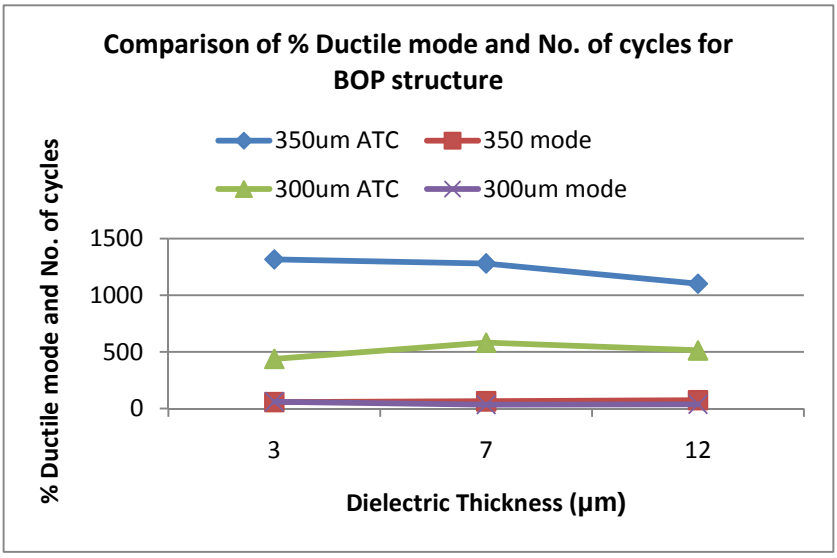


Figure 6.7: Relationship between % ductile failure incidence and No. of cycles for 300 and 350µm SAC 305 ball on BOP structure.

Figure 6.7 shows the variation of % Ductile failure incidence and No. of cycles for BOP structure for 300μm and 350μm solder ball size. Figure 6.10 illustrates the results for varying dielectric thicknesses for 3μm, 7μm and 12μm respectively. Figure 6.10 shows very interesting results it can be observed that the presence of a thick dielectric actually hurts the Number of cycles. Having a thin dielectric increases the fatigue life in case of 350 μm structure this result basically indicates that such a thin dielectric layer doesn't have any effect on the life of solder. Its strictly the solder ball size that is more important for that structure.

6.3.2 CORREL function

CORREL function is useful when data is classified on two different arrays as in the two factor case with replication. However, for this tool it is assumed that there is a single observation for each pair. The CORREL function calculates the correlation coefficient between two measurement variables when measurements on each variable are observed for each on N subjects. The correlation analysis is particularly useful when there are more than two measurement variables for each on N subjects. It provides an output table (value), a correlation matrix that shows the value of CORREL applied to each possible pair of measurement variables. One can use the correlation analysis tool to examine each pair of measurement variables to determine whether the two measurement variables tend to move together- that is, whether large values of one variable tend to be associated with large values of the other (positive correlation), whether small values of one variable tend to be associated with large values of the other (negative correlation), or whether values of both variables tend to be unrelated (correlation near zero) [CORREL function description from Microsoft Excel]. Equation 6.8 gives the correlation coefficients.

$$Correl(x,y) = \frac{\sum (x-\bar{x})(y-\bar{y})}{\sqrt{\sum (x-\bar{x})^2 \bullet \sum (y-\bar{y})^2}} \qquad 6.8$$

To confirm the correlation that was observed in figures 6.7-6.10 we used a standard function that gave correlation coefficient between the two quantities. Equation 3 gives the correl

function used to calculate correlations factors in statistical analysis [14]. In this study, weibull parameter and fatigue life from accelerated thermal cycling were correlated to the strenghts and failure modes from ball shear test data.

Table 6.1: Statistical correlation between Weibull parameter, Number of cycles and % ductile failure incidence for different solder compositions with 300µm diameters.

Solder ball type	Beta	%incidence	No. of cycles
SAC 305	6.75	33	730.2
SAC 125Ni	6.58	97	874.3
SAC 405	11.83	30	685.5
Correlation	-0.56		0.98

From table 6.1 it is clear that there exist a clear cut relation between the type of solder and % ductile incidence. One can also see that there exists a strong inverse correlation between the weibull parameter and % ductile failure incidence.

Table 6.2: Statistical correlation between Weibull parameter, Number of Cycles and % ductile failure incidence for SAC 305 solder with different ball diameters on BOP structure.

Ball diameter (um)	Beta	% incidence	No. of Cycles
250	8.99	100	608.7
300	6.75	33.33	730.2
350	13.25	63.33	1266.1
Correlation	0.284413		0.87

Table 6.3: Statistical correlation between Weibull parameter, Number of Cycles and % ductile failure incidence for different solders with 300 µm diameter on RDL structure.

Solder ball type	Beta	%incidence	No. of cycles
SAC 305	4.59	100	427.4
SAC 125Ni	6.54	100	841.1
SAC 405	5.42	100	518.7
Correlation	#DIV/0!		#DIV/0!

Table 6.4: Statistical Correlation between Weibull parameter, Numberof Cycles and % ductile failure incidence for different dielectric thicknesses with 300µm SAC 305 ball

Dielectric Thickness	ATC	failure mode	Beta
3	438.7	60	3.17
7	582.49	33.33	5.88
12	513.302	36.66	3.94
	-0.92		**-0.79**

Table 6.4 gives correlation coefficient between weibull parameter and % ductile failure incidence for varying dielectric thickness for Ball on Pad structure and 300µm solder bump. Negative correlation coefficients indicate that there is an inverse relationship between the accelerated thermal cycling and weibull parameter for varying dielectric thicknesses. From the data it is clear that there is a strong role that the dieelectric thickness plays in determining the fatigue life of accelerated thermal cycling. Dielectric thickness plays a role in the package CTE and even more than that it gives the strength to the structure. This correlation is even more prominent because of the low standoff height. If this test would have been performed on an even smaller solder bump the relation would be even more dominant.

Table 6.5: Statistical Correlation between Weibull parameter, Number of cycles and % ductile failure incidence for different dielectric thicknesses with 350µm SAC 305 ball

Dielectric. Thickness	ATC	% Ductile mode	Beta
3	1316.102	56.66	3.61
7	1280.61	63.33	11.53
12	1101.78	73.33	3.78
	-0.968		-0.09589

Table 6.5 shows the corrleation coefficient between weibull parameter and accelerated thermal cycling with failure mode for 350µm for a ball on pad structure. From data it can be seen that there is not much of a correlation in between the two for that particular ball size. The reason for such poor result is that for ball shear 350 µm size is too big and hence many a times one can expect a ductile failure in most cases. As far as accelerated thermal cycling is concerned ball size is more important parameter than dielectric thickness. As the plastic strain induced in the solder bump is inversely proportional to the standoff height. Change in dielectric thickness is going to contribute to the change in CTE of the package which is a small parameter to alter the fatigue life as compared to standoff height.

6.3.3 *Correlations between fatigue life and geometrical design parameters considered in this study*

The ultimate aim of this study is to establish correlations between structural design parameters (geometrical and material parameters) which affect the ball shear result and at the

same time influence accelerated thermal cycling life. Figures 6.8 gives relationship between normalized solder ball diameter which is a structural design parameter Vs normalized number of cycles and % ductile failure incidence. The three diameters considered in plotting of this graph are 250µm, 300 µm and 350 µm. The type of ball considered was SAC 305. The diameter was normalized by 350µm and plotted in a reverse way for convinence. So the diameters are plotted in decreasing order. The highest diameter which is 350µm is equal to 1 in this scale, 300µm becomes 0.85 and 250 µm becomes 0.71. One can observe that there is a linear decrease in fatigue life as diameter is reduced. The regression value for this correlation is 0.81 which implies that the relationship is strong and it is intuitive too. Figure 6.8 also shows the normalized ball shear mode plotted on the same axis as Normalized Number of cycles. In the ball shear mode too the ball shear mode for 350 µm solder ball size was used to normalize the ball shear mode values. It can be observed that there is not a strong correlation between the % ductile failure incidence and Number of Cycles when considering the solder ball size is considered.

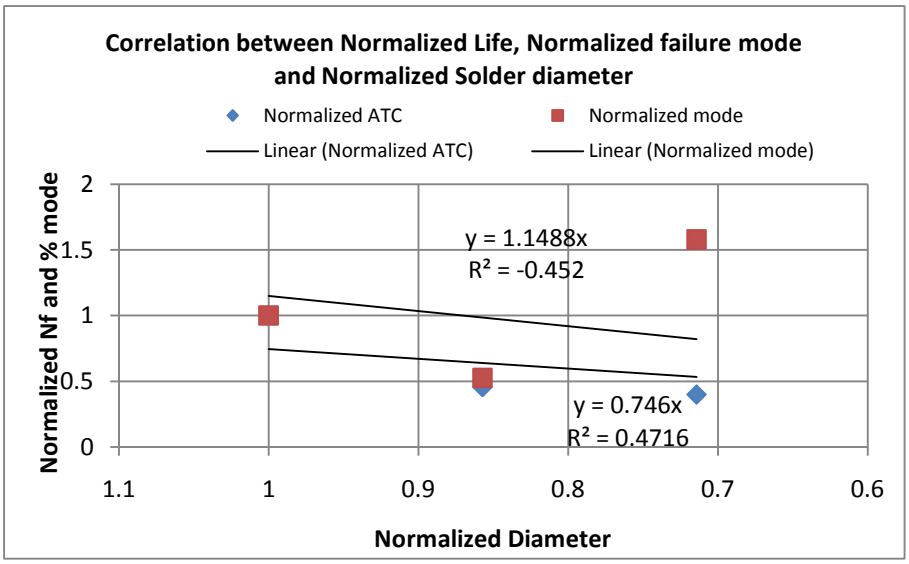


Figure: 6.8 Correlation between Normalized life, Normalized failure mode and Normalized solder diameter

Figures 6.9 gives relationship between normalized dielectric thickness which is a structural design parameter Vs normalized number of cycles and % ductile failure incidence.The

three dielectric thicknesses considered in plotting of this graph are 3μm, 7μm and 12μm. The type of ball considered was SAC 305 and solder diameter considered is 300 μm. The dielectric thickness was normalized by 12μm and plotted in a reverse way for convinence. The highest dielectric thickness which is 12μm is equal to 1 in this scale, 7μm becomes 0.58 and 3 μm becomes 0.25. One can clearly see that there exist a linear relationship between the dielectric thickness and Number of cycles as number of thickness controlls the solder wetting area of UBM. % ductile failure incidence has also been included in the same graph for comparative purposes. In order to have a better correlation the intercepts of the trendlines have been adjusted to 0. One can see that there exist a slight relation between the two metrics. For predicting the life of a package based on the wafer level metric one has to select the appropriate dimension from normalized dielectric thickness find out the appropriate % ductile failure incidence and then just find the normalized life from Y axis.

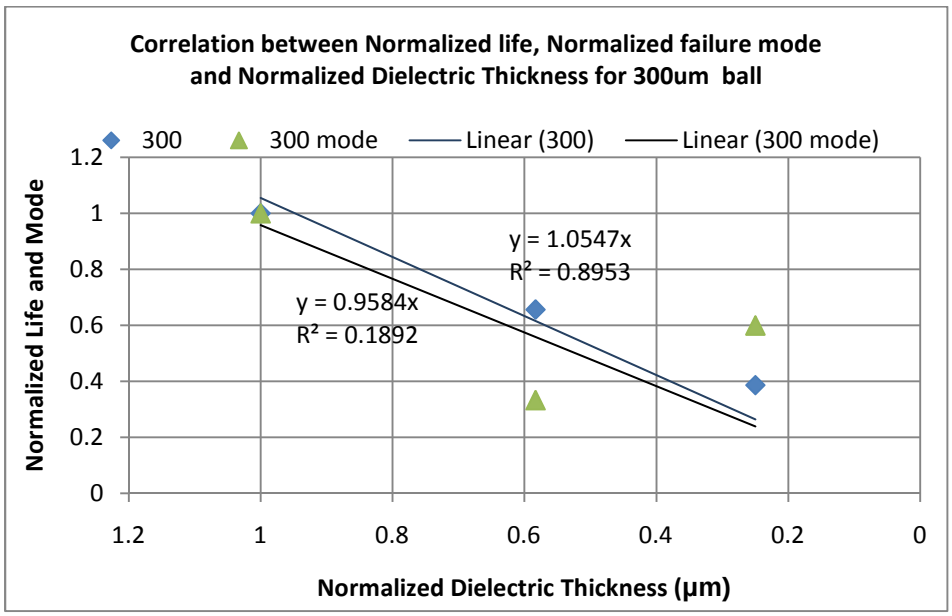


Figure 6.9 Correlation between Normalized life, Normalized failure mode and Normalized Dielectric thickness for 300μm ball

Figures 6.9 gives relationship between normalized dielectric thickness which is a structural design parameter Vs normalized number of cycles and % ductile failure incidence.The

three dielectric thicknesses considered in plotting of this graph are 3μm, 7μm and 12μm. The type of ball considered was SAC 305 and solder diameter considered is 300 μm. The dielectric thickness was normalized by 12μm and plotted in a reverse way for convinence. The highest dielectric thickness which is 12μm is equal to 1 in this scale, 7μm becomes 0.58 and 3 μm becomes 0.25. One can clearly see that there is a very remote relation between the two curves. The intercepts for both the trendlines are set to 0 one can see from the regression value which is negative in case of accelerated thermal cycling and positive in case of the the ball shear mode. This indicates that there is very vague or very inaccurate relationship that exists between the two parameters considered. One of the primary reasons for this disparity in results is that ball shear diameter is more important parameter for a 350μm ball and hence one might have to to go higher speeds to correct the % ductile failure mode incidence and a revised correlation can be established which can establish a better relationship between the two parameters.

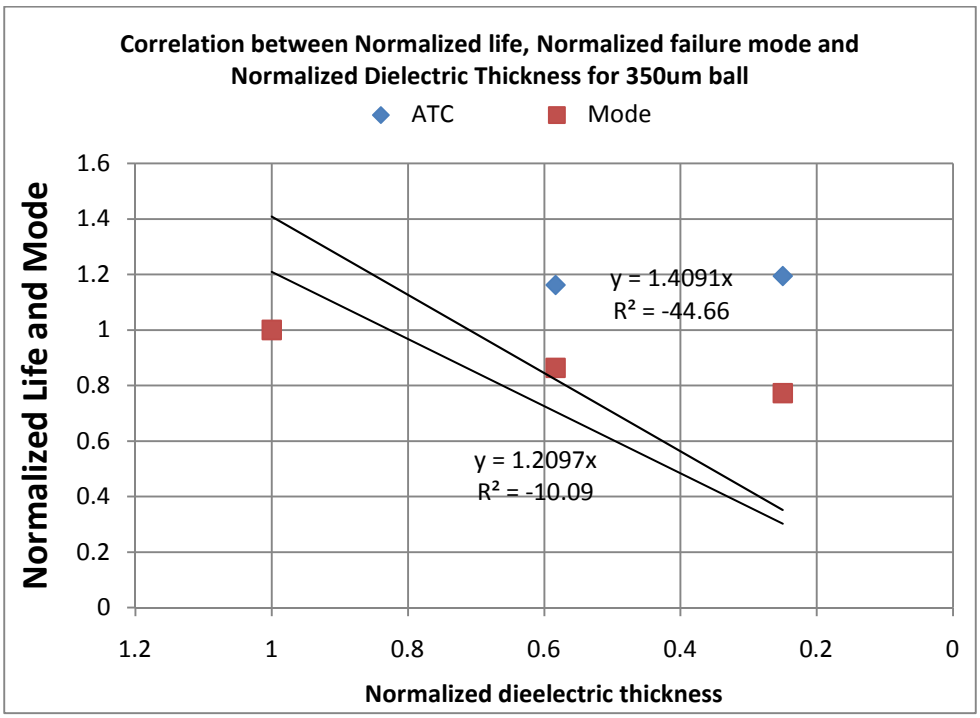


Figure 6.10: Correlation between Normalized life, Normalized failure mode and Normalized Dielectric thickness for 350μm ball

6.4 Conclusion

In this chapter two metrics from ball shear test namely Signal to Noise ratio and % ductile failure mode incidence are compared against weibull parameter and Number of cyles in acclerated thermal cycling. Following are the conclusions from this study.

- After an extensive comparison of various parameters against % Ductile failure incidence and Number of thermal cycles it can be confirmed that % ductile failure incidence is definitely a better metric when compared to the shear force. This result is in accordance to some of the comparisons done between Board level drop test and high speed pull / Cold ball pull by Valota et.al and Song et.al. This study proves that such correlations are also observed in Board level accelerated thermal cycling and Ball shear test. It is confirmed that there is no possible computational correlation between the two types of tests.
- In case of ball on pad structure type of solder is extremely important as the curve changes slope by exactly the same angle. One can note from figures 6.4-6.6 that the material of solder bump affects actually has the same effect both on ball shear mode and accelerated thermal cycling this proves that both the tests have similar failure signatures. This effect can be seen in a more pronounced way in Ball on Pad type of structure as compared to Ball on RDL type of structure.
- Solder ball size is an important parameter that affects the Number of cycles in accelerated thermal cycling. It can be noted from this chapter ball size is even more important than the structure itself. However, there is a weak correlation between Number of cycles and % ductile failure incidence based on Normalized solder ball diameter as a metric which can be concluded from figure 6.8. One of the possible reasons for this disparity is that the speed at which the solder ball was sheared was same for all the sizes and this affected the failure mode.

- Effect of dielectric thickness on ball on pad structure was studied for 300µm and 350 µm SAC 305 solder bump on Ball on Pad structure. For 300µm case one can see a correlation between Number of cycles and % ductile failure incidence but varying the same dimensions didn't had any effect. This conclusion makes sense because as the dielectric thickness increases the solder wetting area increases. As the solder wetting area increases the solder fatigue life increases and this result is pretty intuitive.
- Possible reason for this difference in the 350µm is that ball diameter is a stronger parameter that controls the fatigue life. Solder wetting area is important but not as important as solder diameter.

CHAPTER 7

CONCLUSION

The following are conclusions drawn from this dissertation

- An attempt of correlating wafer level reliability and board level reliability for wafer level chip scale packages was made in this dissertation. This dissertation is primarily divided into two parts wafer level reliability (ball shear) and board level reliability (accelerated thermal cycling). In the first part of this dissertation a DOE comprised of ball size, ball composition, and type of structure was designed and implemented. Similar packages were mounted on a accelerated thermal cycling boards and are subjected to accelerated thermal cycling according to JEDEC standard JESD22-A104C and the results are compared
- Chapter 2 gives a good literature review of solder materials their good and bad properties of individual solders. It was noted from literature search that Tin-Silver Copper (SAC) family of alloys that has been adopted primarily by the telecom industry. As this disseration is limited for portable electronics and telecom industry uses a lot portable devices, hence SAC family of alloys were selected for this study. SAC 305 and SAC 405 along with SAC 125Ni were selected for this study. Chapter 2 also reviews various failure reliability models for ball shear testing and accelerated thermal cycling. Multi-linear Kinematic hardening model was selected for modeling solder ball for ball shear testing because it can model the plasticity better and can accommodate Bauschinger's effect which is observed very prominently in all metals and solders. ANAND's model which is a unified plasticity model and it essentially unites the time-dependent and time-indepenedent plastic strain into an inelastic strain which is

appropriate for this dissertation. Darveaux's model was chosen for calculating the Number of cycles in accelerated thermal cycling.

- Chapter 3 reviews the ball shear testing, various parameters that are changed in a typical ball shear test, it also reviews the JEDEC standard JESD22-B117 which talks about ball shear test and impact of various testing parameters on the result of ball shear test.
- In Chapter 4 various compositions and scenarios for ball shear test are considered. A DOE comprised three solder bumps, three dielectric thicknesses, three sizes of solder bumps and three different solder ball configurations is implemented. Ball shear test is carried out at two heights. All the configuations are tested in ball shear test and the best configuration is determined by signal to noise ratio. It was concluded that SAC 125 Ni solder with Ball on Pad and Ball on RDL structure were found to be the most reliable cases in ball shear testing. As mentione above, multi-linear kinematic hardening model was used to model the solder bump in case of a ball shear test computationally. Computational and expermental testing validated each other. Effect of test temperature on solder ball shear strength was observed and temperature dependency of strain was modeled. It was concluded that the best configuration of structure with a solder ball diameter of 300µm SAC 305 ball mounted on ball on pad structure is the best combination amongst all the configurations considered.
- In chapter 5 of this dissertation, similar package assemblies (those were sheared in chapter 4) were mounted on PWB and subjected to accelerated thermal cycling. Accelerated thermal cycling was carried out in JEDEC standard JESD22-A104C. accelerated thermal cycle had 125ºC and -40ºC with a frequency of 2 cycles per hour. For accelerated thermal cycling it was concluded that ball size was the most important parameter in increasing fatigue life of solder. ANAND's model was used to mode the Visco-plasticity of solder interconnects. Only SAC 305 and SAC 405 solders were

modeled due to availability of material properties. Ball on pad and Ball on RDL structures were modeled as per specifications. Darveaux's approach was used to calculate the number of cycles computationally. It was observed that there was approximately 20-23% error in Number of cycles calculated computationally and number of cycles obtained experimentally. Effect of mean temperature on fatigue life of solder was also checked. It was observed that total strain induced in the cornermost solder bump increased linearly with respect to the mean temperature.

- In chapter 6 results from ball shear test and accelerated thermal cycling are compared. Ball shear strength and ball shear mode was used to compare and establish correlations with inelastic strength and Number of cycles from accelerated thermal cycling respectively. It was observed that % Ductile failure incidence which is the ratio of ductile failures to the total failures is a better metric as compared to shear strength (gF) obtained in the testing. Also in chapter 6, CORREL function was used to derive the correlation coefficients between % Ductile failure incidence from ball shear test and weibull parameter and number of cycles from accelerated thermal cycling. It was observed that in general, ball on pad structure exhibits better correlation with the ball shear testing reliability performed at the wafer level. Correlations between different structural parameters and number of cycles were obtained by normalizing both the dimensions and number of cycles independently and plotting them against structural parameter. It was concluded that solder wetting diameter has effect on determining the % ductile failure mode and Number of cycles in accelerated thermal cycling. However, this solder wetting diameter is not as important as the solder diameter. If one can increase the solder wetting diameter by adding steps to the UBM the accelerated thermal cycling reliability can be increased.
- The overall conclusion from this dissertation is that some trends are confirmed from experimentation but further investigation are warranted to substantiate the findings. In

comparing Ball shear and accelerated thermal cycling it is important to recognize that Ball Shear is plasticity dominated whereas Accelerated thermal cycling is a creep dominated failure. Also, there is a significant difference in microstructure as solder structure in ball shear test have as cast microsturucture which has very large grains whereas after the accelerated thermal cycling the solder microstructure is changed to many small grains. Despite, all the differences in failure mechanism and microstructure, a good correlation was noted for SAC 305 solder, reasonably good correlation for SAC 125Ni. However, the correlation fails for SAC 405 solder all even though all tested on Ball on pad structure. The correlations drawn from this study are statistical and empirical and it is yet to be determined if they will hold true for any other area array package architectures.

APPENDIX A

MECHANICAL DESIGN OPTIMIZATION OF A PACKAGE ON PACKAGE

A.1 Abstract

In the past decade, compact components such as Chip Scale Packages and flip chips were the work horses of miniaturization. However, emerging applications are now demanding even higher packaging density. In order to fulfill this requirement, three dimensional packaging was evolved. Advantages of three dimensional packaging structure include minimal conductor length and eliminate speed limiting inter chip interconnects. In order to reduce signal delays and to increase heat dissipation lot of solutions like through silicon Vias, thermal vias, stacking were implemented. Stacked packages are finding applications ranging from high-end servers to mobility products. Most common applications of stacked packages include high performance memory, DRAM, logic-memory stack, system in a package etc. Stacked packages can be package-on-package or die stacked (with several dice inside the same casing) or both. The thermo-mechanical design of package on package is very complex and often requires elaborate models and analysis with considerable CPU time. In this paper we have considered a package with both die stacking and package on package. In the first part of this study we considered a variety of cases resembling the applications that stacked CSP can go into they are as mentioned. In this study, we have considered various geometries to optimize the design mechanically in thermo-cycling loading the optimization function for this study is to minimize the package height without compromising its reliability in terms of thermo-cycles. “Package on package” family of packages is expensive to operate and to fabricate hence a prior simulation of various geometry of interconnects is necessary to understand how the package is going to behave in terms of number of cycles. In this study we have considered different sizes of solder balls to Optimize solder joint fatigue life. In this study SAC405 is considered.

A.2 Introduction

The expectations of today's customers from electronics industry are that they should offer products that are smaller, with more functionality, better performance and lower cost. The technology these industries are relying upon to increase the packaging density is stacked packaging [71]. Vertical integration of chips in a single package multiplies the amount of silicon that can be squeezed in a given package footprint and more data functions per cubic centimeter (cm) of application space, conserving less board real estate. Stacked packaging can be carried out using two or more dice within a single package, or by stacking and connecting completed packages (Package on Package). Some of the advantages that stacked package offers over the conventional package are size (40-50% reduction), volume (5-6 times reduction over conventional Multi Chip Module) and more than 100% silicon efficiency [72]. Stack package enables shorter routing of interconnects from chip to chip, which benefits in speed. Another benefit is the simplification of surface mount system-board assembly as it doesn't require any special infrastructure and also, fewer components can be placed on board minimizing the pick and place errors [73].

Some of the major challenges involved in package on package are thermal and thermo-mechanical simulation of the complete package. Due to the complex and expensive nature of the package it is good to have a detailed simulation which can tell the optimized dimensions of critical components in order to have maximum solder joint fatigue reliability. Previous work has been done on modeling and thermal simulation of various stacked packages. These include package in package, die stacked package, different architectures in die stacked packages [74-77]. Most of the packages involved in these simulation studies are low powered memory dice.

Mao *et al.* focused on the analysis of a twin die stacked package under a cyclic thermal loading. Viscoplastic finite element analysis and Darveaux theory were applied to investigate the solder joint reliability of the stacked die package. The authors used a 3D-slice model and

concluded that solder joint under the die edge overhang area is always the critical especially for stacked die package [78]. Rodgers *et al.* used substructuring and submodeling finite element techniques on a 9x9 ball grid array package. Darveaux's method was used to estimate the fatigue life of solder joints under various thermal loading. The innermost solder joint on the diagonal of the BGA was predicted to fail first in the accelerated thermal cycling (ATC) and accelerated thermal cycling plus constant power cases. The outermost solder joint was predicted to fail first in power cycling in comparison to ATC and ATC plus power cases [79]. Hossain *et al.* have discussed about the viscoplastic finite element simulation to predict the solder joint fatigue life of different die stacking architectures for flash memory applications. Pyramid stack, Rotated stack, stacking with spacers and staggered die stacking keeping the interconnection architecture (solder joint) constant were considered. Effects of different package reliability parameters like die size, die and die attach thickness were varied and their stress effects were studied. It was found that spacer-die architecture had better solder joint reliability performance than the other three die architectures [80].

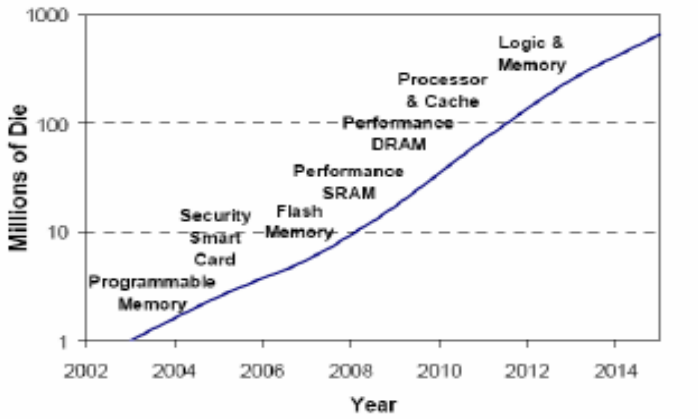


Figure A.1: Die stacking trend forecasted [73]

This study is a continuation of [11]. In [11] we studied the package from thermal loading point of view; however this part concentrates on the thermo-mechanical challenges of the same package. For the 3D stack package yield, the availability of fully tested memory is very important. The overall cost of the 3D stacked package can be affected badly if it has a single

bad die in the package. Hence Package on Package (PoP) is preferred for such application. The memory and logic packages can be combined based on the system needs with lower cost by PoP concept. However the reduction in system volume comes at the expense of complications in mechanical design and more thermal expansion mismatch. Generally solder joint is considered as a weakness in the whole structure. The aim of this study is to optimize the package height and the optimization variables are diameters and height of solder balls.

A.3 Comparison of Stacked CSP Vs Package-on-Package

Stacked CSP and Package on Package both represent the latest generation of packages that are considered as packages for the future. The advantages of stacked CSP are as follows

- Stacked CSP has a low package profile
- One of the major advantages of Stacked CSP is that one can use the existing Surface Mount Technology infrastructure.
- Stacked CSP has very low packaging cost.

The disadvantages of stacked CSP are as follows

- This CSP requires to have Known Good die for its fabrication
- Cost of escapees is very high for the stacked CSP kind of device.

Following are the advantages of a Package on Package

- The package on package type of device has a low cost of ownership.
- Package on Package has the flexibility of selecting different packages and stacking on one another.
- Testing is done on individual packages before they are mounted in the stacked package and hence this type of 3D stack has a very high yield which reduces the cost of packages.

Following are the disadvantages of Package on Package

- Package on Package type of device has high package profile.

- Package on Package type of device needs a new package infrastructure which can be very high initial investment but as the number of packages with package on package type of architecture increase the per package cost will go down.

A.3 Package description and Modeling Procedure

In this study, a molded ball grid array stacked package on package is considered for the analysis. Top package constitutes of two memory dice stacked on each other. Bottom package which is a logic die, is a flip-chip package. Figure 2 shows the front view of the package on package under study.

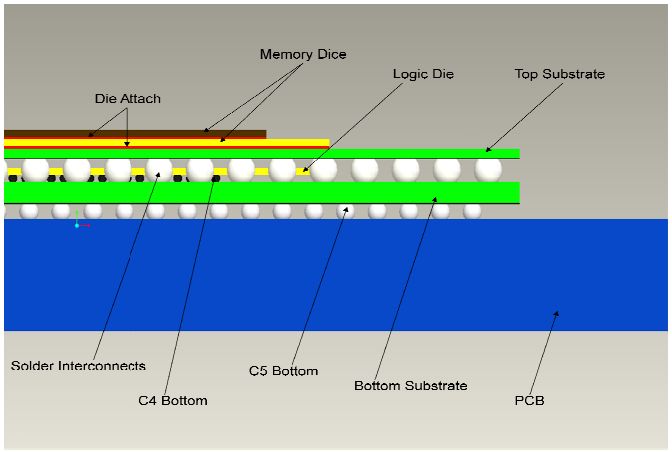


Figure A.2: Details of the package on package under study.

The package on the bottom of the stack as shown in figure 2 is a flip chip package with a fully populated solder ball matrix with a ball count of 26x26. The dimensions are: the standoff height is 0.21mm, the diameter and ball pitch for the C5 interconnects are 0.3mm and 0.5mm respectively, the die size is 7.62mm x 7.62mm x 1mm, the ball pitch for the C4 interconnects is 0.3mm with a diameter of 0.14mm and height of 0.1mm.

As mentioned earlier, the top package consists of two stacked dice. The top and bottom dice are 6mm x 6 mm and 8mm x 8mm respectively with a thickness of 0.1mm each. The two dies are attached to each other and to the substrate by a die attach that has a thickness of 0.0318mm. Mold cap covering the entire package is considered.

The wire bonded stacked BGA package (memory dice) is attached to the flip chip BGA package (logic die) via solder balls which has a height of 0.32mm and a diameter of 0.45mm. The solder interconnects are arranged at the periphery in an array of 21x21 and 19x19. The substrate dimensions used for the package are 14mm x 14mm.

The board was modeled as a block which is 1.5 times the dimension of substrate in diagonal direction. For a robust design towards maximizing thermo-mechanical reliability of package on package we consider effects of different control factors including thicknesses of die, die attach, top and bottom substrates by keeping the total height of package constant. The ultimate aim of this research paper is to increase fatigue life of package under study.

The geometries are modeled as “Parts” using Pro/E Wildfire 3.0. Then, an “Assembly” is created for the package on package. Figure A.3 shows the Pro-E model of the PoP. Once the assembly is created it is imported to Ansys [82]. Owing to the symmetric nature of the problem, an octant model is considered. Once the octant model is generated, material properties are assigned to the respective components.

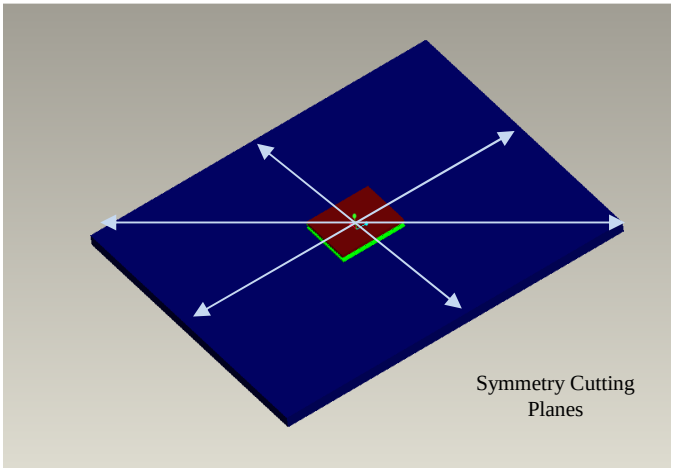


Figure A.3: CAD Model –Package and PCB

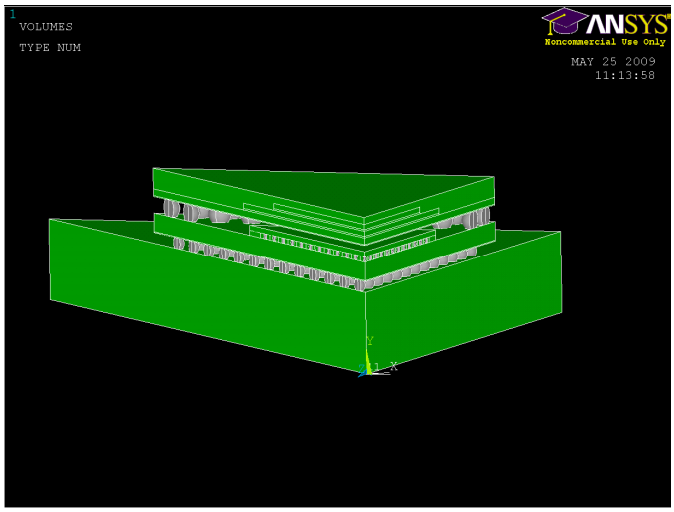


Figure A.4: Octant model imported into ANSYS

Table 2 shows the package dimensions and Table 3 shows the material properties of the components.

Table A.2: Package Dimensions

Component	Top Package (mm)	Bottom Package (mm)
Substrate	14 x 14	14 x 14
Substrate Thickness	0.13	0.3
Die	6 x 6 / 8 x 8	7.62 x 7.62
Die thickness	0.1 / 0.1	0.1
Die attach thickness	0.0318 / 0.0318	NA
Mask thickness	0.0175	0.0175
Solder ball diameter	0.457	0.14 (C4) / 0.3 (C5)
Solder ball height	0.32	0.1 (C4) / 0.21 (C5)
Solder Pitch	0.65	0.3 (C4) / 0.5 (C5)
Ball Count	152	529 (C4) / 676 (C5)

Table A.3: Mechanical Properties of different components

Component	E (GPa)	Shear Moduli (MPa)	CTE (1/K)	Poisson Ratio
Ball	162716	-	24.5e-6	
Die		-	$-5.88x10^{-6}+6.261-8T-1.610-10T^{2}+1.510-13T^{3}$	
Copper	128932	-	$13.8x10^{-6}$	0.34
PCB	27294-37T (XY) 12204-16T(Z)	-	$16.0x10^{-6}$(XY) $84.0x10^{-6}$	0.39 (XY &YZ) 0.11 (XY)
Substrate Mask	4137	-	$30.0x10^{-6}$	0.4
Mold Cap	15513	-		
Underfill	14.5	-	$20.0 x10^{-6}$	0.28

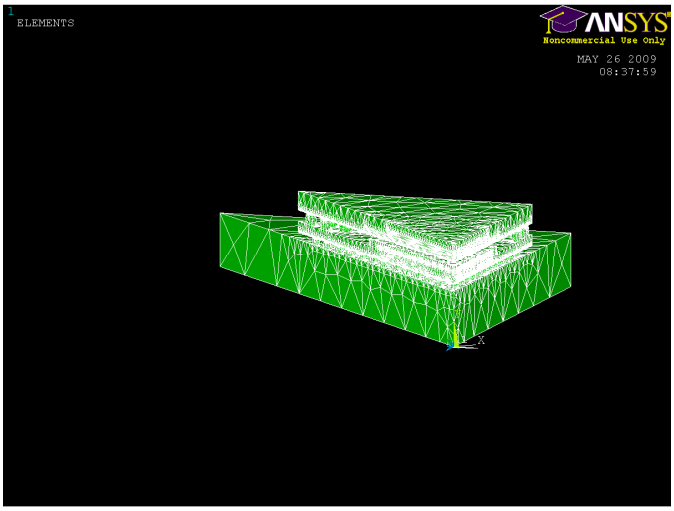
Linear and non-linear, elastic and plastic, time and temperature independent and dependent material properties were incorporated in FE models. The detailed package was meshed using SOLID45 elements. The solder ball was meshed VISCO 107 with unified Anand's constitutive equation. Structured mesh was used for 3D model of analysis.

Table 4 shows the material constants for Anand's constitutive equations.

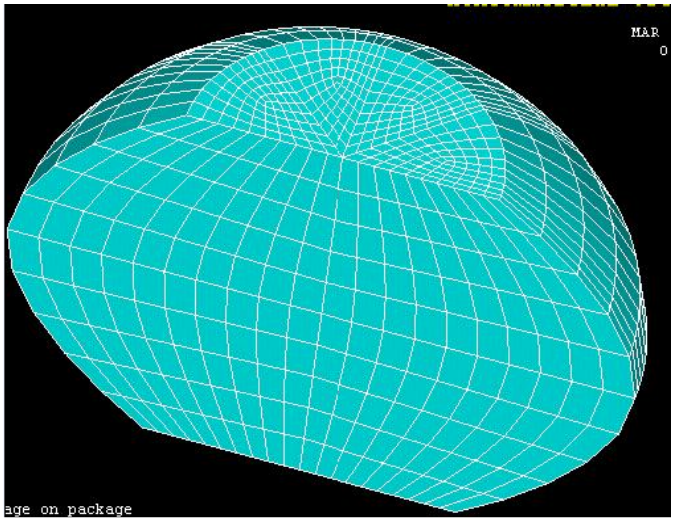
Table A.4: Material constants for Anand's constitutive equations [14].

Constant	Parameter	Value	Definition
C1	So (MPa)	12.41	Initial value of Deformation Resistance
C2	Q/R (Kelvin)	9400	Activation energy / Boltzmann's constant
C3	A (1/sec)	4.0e-6	Pre-exponential factor
C4	ς (dimensionless)	1.5	Multiplier of stress
C5	M (dimensionless)	0.303	Strain rate sensitivity of stress
C6	ho(Mpa)	1378.95	Hardening Constant
C7	S (Mpa)	13.79	Coefficient of deformation resistance saturation value
C8	N(dimensionless)	0.07	Deformation resistance value
C9	a(dimensionless)	1.3	Strain rate sensitivity of hardening

A.4 Meshing and Boundary conditions



(a)



(b)

Figure A.5: Meshing (a) Global mesh in model and (b) localized mesh on solder ball.

Figure 5a and b show meshed octant model and mesh on solder ball respectively. In this study Visco107 element was used for modeling solder ball and solid45 was used for modeling rest of the model. Solder ball was densely meshed whereas meshed was made coarse on far side of PCB to reduce the overall mesh count. The baseline case was meshed in

about 322,518 total number of elements. The total number of elements was divided into 268590 SOLID45 and 53928 VISCO107 numbers of elements.

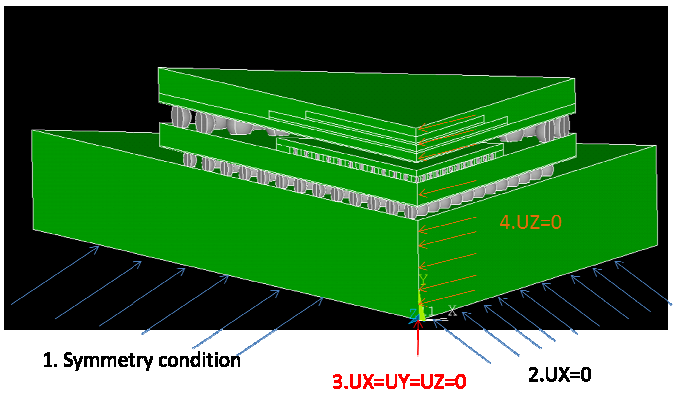


Figure A.6: Boundary conditions applied on the model

Following boundary conditions were applied on the octant model. Total of four boundary conditions

Symmetry boundary condition exists in the inner x and y directional plane. In all the analyses in this study, Uz=0 for the lowest node in the inner section of the x and y direction intersection of the PWB. A temperature input of -40^{o}C to 125^{o}C with 15 minutes high and low dwells and 15^{o}C/min low and high ramp was given as input load for the simulation. Figure A.7 shows the input cycle for simulation. The problem was solved for two cycles and hence 8 substeps. The plastic work of solder balls was monitored at 4th and 8th substep and using Darveaux's approach thermo-cycling life for the package under consideration was obtained.

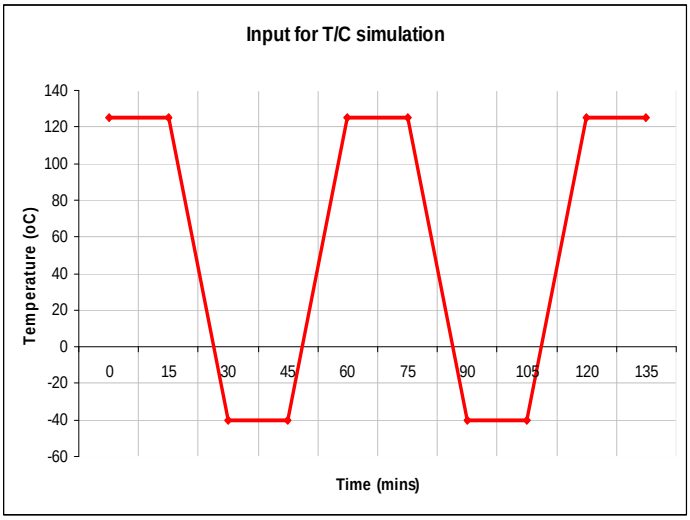


Figure A.7: Input for T/C simulation

A.6 Results and Discussion

Figures 8-10 show von-mises stress, warpage induced and plastic work at the end of cycling. From figure 8 it can be seen that maximum stress occurs at the far end of C4 solder ball in the underfill which makes sense as it is at the far end that has been a traditional failure mode in accelerated thermal cycling simulations. One of the reasons why the maximum stress does not occur in the solder interconnect is because of its height. the more height of solder ball more compliant it is for the fatigue loading. Figure 9 shows the warpage induced in the model. Warpage induced in the package was calculated by calculating the difference between minimum and maximum Y displacement of the model. As expected the maximum warpage is induced in the far end of PWB. This result confirms that the boundary conditions that are applied to the model are correct.

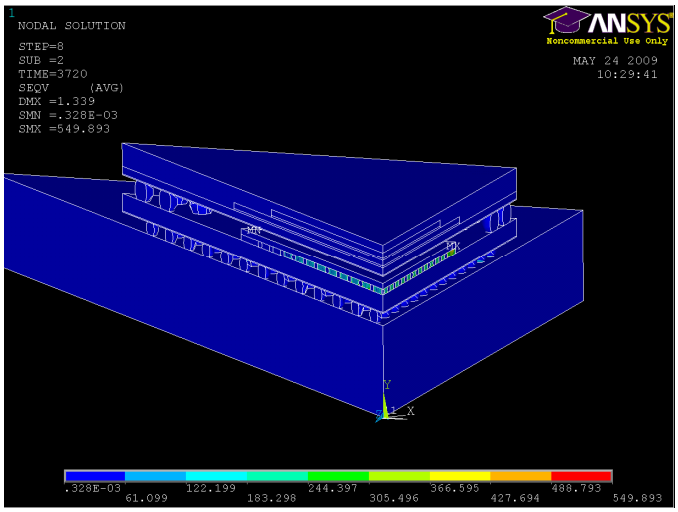


Figure A.8: Von-mises Stress at the end of thermal cycling

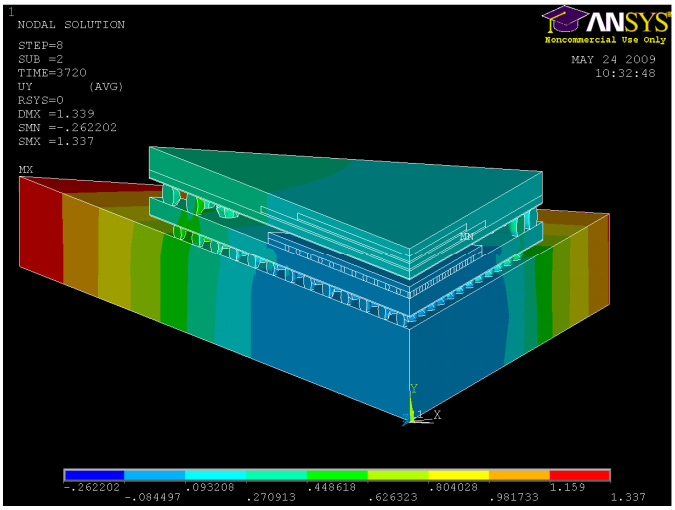


Figure A.9: Warpage induced at the end of thermal cycling

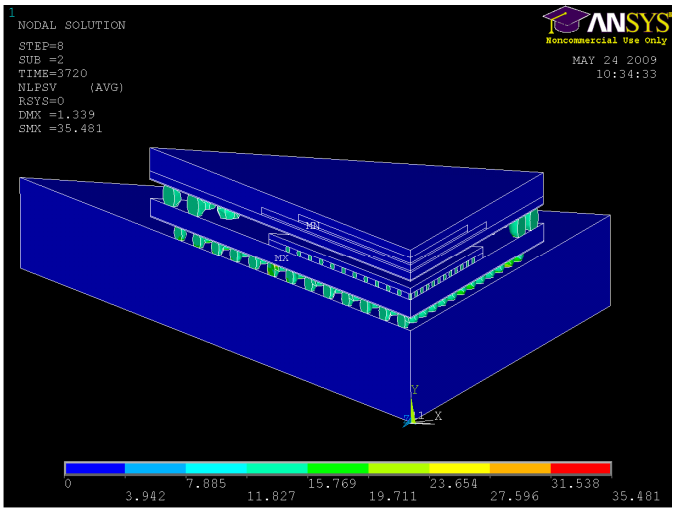


Figure A.10: Plastic work at the end of thermal cycling

A.7 Calculating Fatigue life of solder

ANSYS APDL script was used for incorporating Darveaux's energy based fatigue life model to predict solder joint fatigue life. The layer of elements having maximum plastic work density is included in the calculation of the weighted average plastic work density $\Delta W_{avg.}$ Equation 1 gives the equation to calculate the average plastic work per cycle.

$$\Delta W_{avg} = \frac{\sum_{i=1}^{Element} \Delta W_i * V_i}{\sum_{i=1}^{Element} V_i} \text{ ---------- (1)}$$

Where ΔW_i denotes the plastic work density in the ith element and V_i is the volume of that element.

Thermal cycles to crack initiation "N_o"

$$N_o = K_1 \Delta W_{avg}^{K2} \text{ ---------- (2)}$$

Crack propagation rate per thermal cycle "da/dN"

$$\frac{da}{dN} = K_3 \Delta W_{avg}^{K4} \text{ ---------- (3)}$$

Where ΔW_{avg} is the element volumetric average of the stabilized change in plastic work within the controlled solder element thickness. K1, K2, K3 and K4 are crack growth constants,

which depend on geometry, loading and the finite element analysis method. Table 5 gives the values of K1, K2, K3 and K4 used in this study [13].

Table A.5: Constant Values K1,K2,K3 and K4

No.	Constant	Value
1	K1	22400 (cycle/psi)
2	K2	-1.52
3	K3	5.86 x10^{-7} in/cycle/psi
4	K4	0.98

Figure A.11 gives the flow chart used in modeling per Darveaux approach.

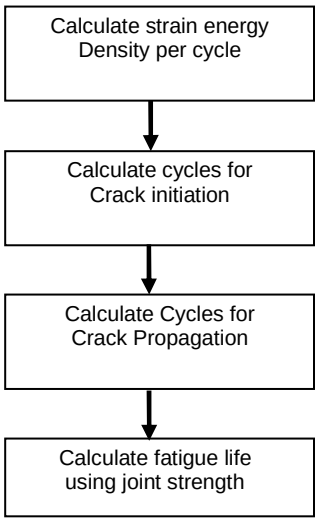


Figure A.11: Flow chart of Darveaux approach [13]

When substituted the values of plastic work into Darveaux model the thermo-cycling life of the package under consideration came to 768.38, 2017.63 and 668.25 for C5, C4 and solder interconnect respectively. Reason for having such a high life for C4 is the presence of underfill. This statement is corroborated from figure 8 where the maximum Von-Mises stress is occurs in underfill. This result was strange as one can observe a significant difference in fatigue life of three solders. To investigate this issue further, we decided to study the effect of die thickness, die attach thickness and substrate thickness on fatigue life of different solder interconnections.

These thicknesses were varied in the range of ± 20% and hence a DOE of 9 cases was generated as seen in the following paragraph.

A.8 DOE cases

In the package under study there are three different solder interconnections, three dies, two substrates and two die attaches. The objective of this study is to optimize the fatigue life of all three interconnects in order to have high reliability in thermo-cycling test. Following table gives the different cases in which die, die attach, top substrate and bottom substrate are varied. Each case has been designated with a name which can help a reader identify a particular case.

Table A.6: Different cases of thickness variation

No.	Name	Die	Die attach	Top Substrate	Bottom Substrate
1	Bline	0.1	0.0318	0.13	0.3
2	BSI	0.1	0.0318	0.13	0.36
3	BSD	0.1	0.0318	0.13	0.24
4	DAI	0.1	0.03816	0.13	0.3
5	DAD	0.1	0.02544	0.13	0.3
6	TSI	0.1	0.0318	0.156	0.3
7	TSD	0.1	0.0318	0.104	0.3
8	DI	0.12	0.0318	0.13	0.3
9	DD	0.08	0.0318	0.13	0.3

A.8.1 DOE Results

Following section gives details of the results that were obtained by solving all the problems defined by the DOE. The fatigue life was calculated using the same methodology as described in the earlier section. Table A.7 gives the detail about fatigue life of each of the solders involved in the package.

Table A.7: Different fatigue lives obtained because of thickness variation

No.	Name	C5	C4	Solder Interconnect
1	Baseline	768.38	2017.63	668.25
2	BSI	3092.85	1682.98	1818.63
3	BSD	402.27	970.20	1398.92
4	DAI	2539.16	1136.55	2944.71
5	DAD	3017.82	1810.51	1956.43
6	TSI	2931.05	1577.81	2645.42
7	TSD	2783.89	1225.62	615.03
8	DI	2831.01	1370.34	3274.44
9	DD	2497.3	1842.74	2606.19

Figures A.12-A.15 shows the effect of variation of bottom substrate, die attach, top substrate and Die thickness on the fatigue life of solder.

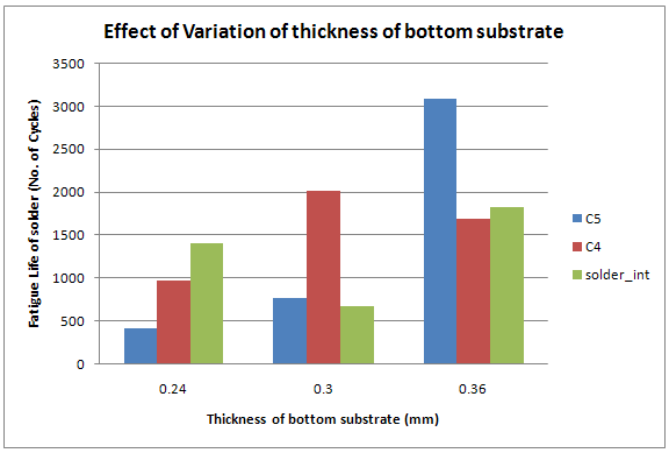


Figure A.12: Effect of variation of bottom substrate on fatigue life of solder

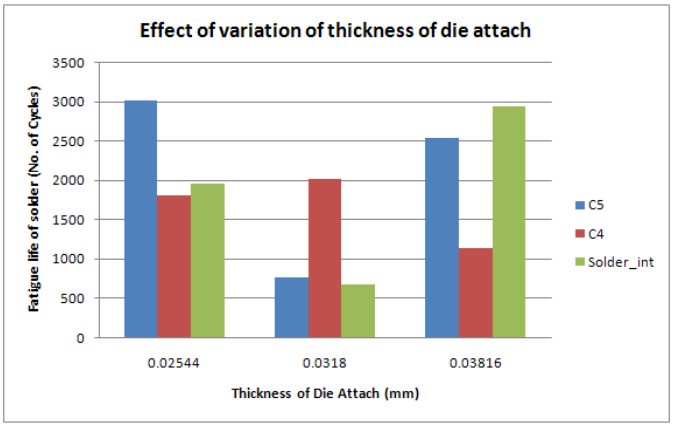


Figure A.13: Effect of variation of die attach on fatigue life of solder

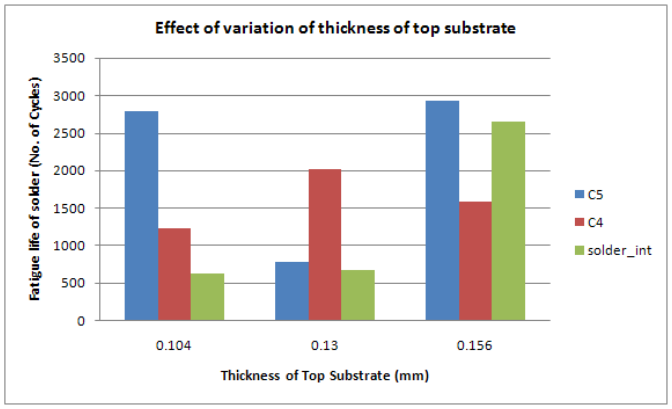


Figure A.14: Effect of variation of top substrate on fatigue life of solder

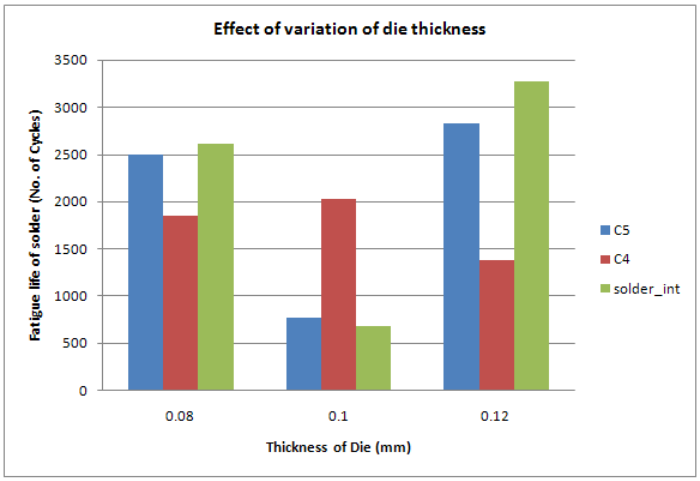


Figure A.15: Effect of variation of Die on fatigue life of solder

It can be observed from figures above that having the existing configuration gives a very high life for C4 solder ball as opposed to C5 and solder_int. variation of thickness of bottom substrate significantly varies fatigue lives of all three solder interconnects and is most beneficial to C5 solder. having a thicker die and die attach are good as an increase in fatigue life can be observed for all the three solder interconncts.

Total warpage induced in model is calculated by monitoring the displacement in Y direction. Note that the warpage reported in figure 16 is the global warpage induced in the model and not the local warpage in package.

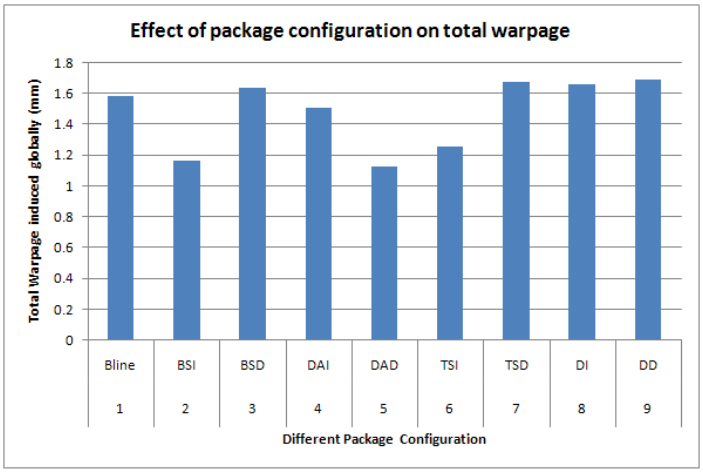


Figure A.16: Total warpage induced in the model

A.9 Summary and Conclusion

A thermo-mechanical modeling and simulation was conducted in ANSYS using Darveraux energy portioning model. Temperature dependent and independent properties were modeled for different components in model. Solid 45 and Visco107 was used to mesh all components and solder respectively. In this study, thicknesses of die, die attach, top substrate and bottom substrate was varied and their effect on Solder fatigue life is monitored. Figures 12-16 show these effects, it can be seen that there is no fixed trend in the data. The variation of these thicknesses affect C4,C5 and solder_int in different ways. Increasing die and die attach

are good options for improving fatigue lives of the three interconnects but are not advisable as the warpage for both cases are 1.63 mm and 1.58 mm respectively. Overall it can be concluded increase in thickness of bottom substrate is a good solution which enhances solder fatigue life of all three solder interconnects and also reduces warpage from 1.59 mm to 1.18 mm.

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