EFFECTIVE THERMAL MANAGEMENT OF ELECTRONIC DEVICES FROM SYSTEM TO DIE LEVEL

by

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ABSTRACT

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FROM SYSTEM TO DIE LEVEL

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In any electronic device, the resistance to the flow of current through the transistors, interconnects, etc. results in a significant heat generation. If this heat is not removed from the device by providing appropriate cooling solutions, the possibility of thermal run away is very high. Under this condition the temperature would continue to rise until it reaches a point at which the device ceases to operate or loses its physical integrity. In presence of a cooling mechanism, the temperature rise is moderated as it asymptotically reaches an acceptable steady state value.

Before any device is introduced in the market, it undergoes several levels of packaging. Primary function of the package is to provide a mechanical support, protect the electronics from external contaminants and provide a path for heat removal. In its most basic form, packaging can be divided into three levels. First level of packaging addresses the issues at the package level, while second and third levels of packaging addresses the issues at the board level and system level (enclosures) respectively. As mentioned earlier, one of the key functions of the package (at all three levels) is to provide a path for heat removal. Making such provisions is

termed as "thermal management" of electronic devices. The method adopted for thermal management of electronic devices should be practical, efficient, reliable and cost effective. In addition, thermal management at any level is a multi-physics phenomenon. Optimal thermal management also requires a multi-objective optimization with many design variables. In this work, such a analysis is performed at the facility, the package and the die level. For the thermal management at the facility level, data centers are considered. For thermal management at the package level a 3D package architecture is considered and at the die level, the effect of non-uniform power distribution was considered for a Pentium IV microprocessor.

With regards to data centers, the power trend for Server systems continues to grow thereby making thermal management of Data centers a very challenging task. Although various configurations exist, the raised floor plenum with Computer Room Air Conditioners (CRACs) providing cold air is a popular operating strategy. These rising heat load trends in data center facilities have raised concerns over energy usage. The environmental protection agency has reported that the energy used in 2006 by data center industry was 1.5% of the total energy usage by the entire nation. The experts agree that by year 2010, this usage will approach 2% of the annual energy use nationwide. This has been the driving force behind the new solutions or technologies such as free cooling. Recent studies show that the outside air can be drawn in to cool the IT equipment without any undue electronic component failure due to contaminants. In this study, different cases employing air side economizer are discussed. A computational technique is proposed by the aid of which energy consumption by the cooling infrastructure of a data center can be estimated.

For thermal management at the package level, a 3D package architecture is considered. 3D packaging has been a strong technology for applications in low density interconnects (LDI's). It has to serve the demand for continuous miniaturization in applications related to consumer electronics, memories, processors, etc. However, in order for 3D packaging to further move from LDI to HDI applications, it has to overcome critical challenges like thermal

management. In order to have effective thermal management, it is necessary to perform thermal characterization through which heat dissipation of a typical stacked package structure can be studied. Recently, there has been a growing concern in PoP stacking architecture as reliability is reduced to individual package rather than the entire PoP. In this work, such thermal analysis of PoP is performed for different power combinations of logic and memory dice. Based on the results thermal design guidelines are provided.From the results, it was also concluded that the only path through which the heat from the packages is conducted to PCB is through the C4, C5 and BGA solder interconnects.

Moving forward into stacking HDI's, it is important to figure how to take advantage of all the surfaces of the PoP to significantly improve the thermal performance. Solder bumps serve as electrical as well as thermal interconnects. Typically, solder interconnects are considered to be a weak link in a BGA structure. At elevated temperature and under higher operating current, interconnects are subjected to a catastrophic failure known as electromigration. When, electromigration occurs, metal atoms are physically dislocated to form voids. These voids increase the thermal resistance and the current density which further accelerates the electromigration phenomenon and eventually results in a device failure. As we march forward on the roadmap, electromigration would be one of the other challenge that needs to be addressed. Hence, for increased reliability of the interconnects, design guidelines to reduce bump electromigration are developed.

Post Pentium II, it was critical to include the non-uniformity of the power distribution on a die; a model ignoring the non-uniformity would significantly under-predict the thermal performance of the die. In this comprehensive study, a multi-objective optimization is performed to study the effect of relocation of functional units of a non-uniformly powered microprocessor on architectural and device performance. Integration of different functional components such as level two (L2) cache memory, high-speed I/O interfaces, memory controller, etc. has enhanced microprocessor performance. In this architecture, certain functional units on the microprocessor

dissipate a significant fraction of the total power while other functional units dissipate little or no power. This highly non-uniform power distribution results in a large temperature gradient with localized hot spots that may have detrimental effects on computer performance, product reliability and cooling cost. Moving the functional units may reduce the junction temperature but can also affect performance by a factor as much as 30%. In this study, a multi-objective optimization is performed to minimize the junction temperature without significantly altering the computer performance. The analysis was performed for 90nm node Pentium IV Northwood architecture and for 3 GHz clock speed.

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CHAPTER 1

INTRODUCTION

1.1 Need for Thermal Management

The resistance to the flow of current through the transistors, interconnects, etc. results in significant heat generation within an operating microelectronics device. If this heat is not removed from the device by providing appropriate cooling solutions, then the temperature would rise at a constant rate until it reaches a point, at which, the device ceases or loses its physical integrity. In presence of a cooling mechanism, the temperature rise is moderated as it asymptotically reaches an acceptable steady state value.

Every device is different and thus requires different cooling strategies for effective thermal management. It can be achieved by conduction, convection, radiation or a combination thereof. The need for thermal management of microelectronic devices has further resulted in the development of advanced heat transfer techniques such as use of phase change materials, spray impingement etc. As a result, today, it is commercially possible to fabricate miniaturized high power microelectronic devices without compromising its reliability. Thermal management of any device is essentially to provide an acceptable thermal environment in which the device can operate satisfactorily.

Based on a survey by the U.S. Air Force, 55% of all the electronics failure are caused due to improper thermal management. Vibration, humidity and dust together constitute the remaining 45% as shown in Fig. 1.1 [1, 2]. Thus, thermal management plays a key role in current as well as in development of any new technology. For all microelectronic devices, reliability and performance can be improved by decreasing its operating temperature. For example, reliability of a silicon chip is decreased by about 10% for every 2℃ of temperature rise [3]. Table 1 further summarizes device failures under various thermal conditions [1].

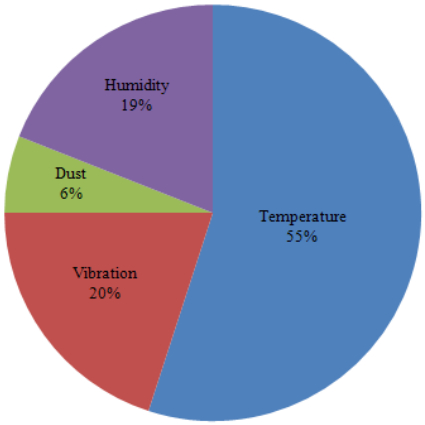


Figure 1.1 Major causes for electronics failure [1, 2]

Table 1.1 Effect of thermal conditions on part failures [1]

Condition	Cause	Effect	Possible failure
Steady-state (hot)	Ambient exposure, equipment-induced	Aging-discoloration Insulation deterioration Oxidation Expansion Softening/hardening Chemical changes	Alteration of properties Shortening Rust Physical damage, increased wear Dielectric loss
Steady-state (cold)	Ambient exposure, mission induced	Contraction Viscosity increase Embrittlement Ice formation	Wear, structural failure Loss of lubricity Cracked parts Alteration of electric properties
Thermal cycling	Ambient-induced, mission operation	Temperature gradients Expansion/Contraction	Mechanical failure of parts, solder joints and connections Delaminating of bonding line
Thermal shock	Mission profile	High temperature gradients	Mechanical failure, cracks, rupture.

1.2 Levels of thermal management

Methods adopted for effective thermal management largely depends on the packaging level. Level 1 packaging which is at the die/package level commonly uses heat sinks, heat spreader, phase change materials etc. to lower the chip temperature. At level 2 which is at the board level, heat is first removed by conduction in the printed wiring board and then by convection to the

ambient air. Level 3 which is at the module or rack (system) level involves the use of air handling units, refrigeration systems, heat exchangers etc. to dissipate heat into ambient. For low power systems, natural or free convection could be sufficient at the system level.

1.3 Scope of dissertation

Method adopted for thermal management at any level should be practical, efficient, reliable and cost effective. Thus, thermal management at any level is a multi-objective process. In this work, a multi-objective analysis is performed at the system, package and the die level. The work is divided in 5 chapters. Chapters 2, 3, and 4 each addresses thermal management at different levels of packaging. Further details about each chapters are mentioned in the following paragraphs.

In chapter 2, the impact of air side economizers on data center cooling is discussed. Three different configurations are studied to show the effectiveness of air side economizers along with a methodology to numerically estimate the energy savings (under identical thermal conditions).

In chapter 3, thermal analysis of a package-on-package (PoP) is performed. The top package consists of two memory dice stacked on each other. The bottom package is a flip-chip with a logic die. The two packages are connected via BGA. Eleven different scenarios are numerically analyzed.

In chapter 4, results of the two analysis are combined to develop a robust design guidelines to minimize device failures due to bump electromigration. In first analysis, a full factorial DOE was formed to study the effect of Al trace thickness, UBM thickness, UBM diameter and PO diameter on current density in Al trace and the bump. In second analysis, a full factorial DOE is formed to study the stresses induced in the bump due to reflow process as a function of attributes of the package architecture. The package architectural attributes such as die thickness, die size, substrate thickness, substrate size and PO size are studied in detail.

In chapter 5, a multi-objective optimization is performed to minimize the junction temperature without significantly altering the computer performance. The analysis is performed for 90nm node Pentium IV Northwood architecture and for a clock speed of 3 GHz.

CHAPTER 2

COOLING OF DATA CENTERS USING AIR SIDE ECONOMIZERS

2.1 Data Centers

With rapid advance of technology, economies around the world are experiencing a paradigm shift in information management. Paper based information exchange is being replaced by digital information. For example, today online banking is very common and each day probably more than million transactions occur such as online money transfers, deposits, bill pay services, etc. In order for these transactions to be successful, banks need equipments that are capable of high-performance computing, networking and large data storage. Such equipments are collectively known as "IT Equipments" and the facility which houses such equipments is termed a data center. Apart from IT equipments, a typical data center also includes backup power supplies, air conditioning, security applications, etc. Thus, data center essentially is a physical place where several racks (servers that are mounted in 19 inch cabinets) are placed in a specific layout in order to facilitate its intended purpose under specific operating conditions. Apart from banking facilities, the data center facilities are commonly used in universities, IT industries (Microsoft, Google, Yahoo etc.), airline industries, Government, etc. Figure 2.1 shows the layout of a typical data center.

Typical data centers are housed within buildings that have no windows and minimal fresh air. This is due to the fact that data centers are primarily designed for remote transactions and not for the people. It is essential that the operating conditions within facility are within the manufacturer's limits. In its thermal guidelines for data processing environments, ASHRAE TC 9.9 [4] has introduced four classes of data processing environments and provides the data for following criteria:

- Steady state temperatures
- Relative humidity

- Maximum dew point temperature
- Temperature rise

These four classes and their requirements are summarized in Table 2.1.

Figure 2.1 Typical layout of a data center [5]

Table 2.1 Class Requirements for Data Processing Environments

Class	Air Conditioning	Environmental Control
1	Yes	Tight
2	Yes	Loose
3	Yes	No
4	No	No

This discussion is focused on Class 1 environment which requires air conditioning of the facility along with tighter controls of criteria stated above.

2.2 Data Center Power Trends

In recent years data center facilities have witnessed rapidly increasing power trends that continue to rise at an alarming rate. The combination of increased power dissipation and increased packaging density has led to substantial increases in chip and module heat flux. As a result, heat load per square feet of server footprint in a data center has increased. Recent heat loads published by ASHRAE [6] as shown in Figure 2.2 indicate that for the period 2000-2004, heat load for storage servers has doubled while for the same period, heat load for compute servers has tripled. According to these trends, compute server rack

heat fluxes in 2006 was around 4,000 W/ft^2. This corresponds to 27KW for a typical 19 inch rack. There are 19 inch racks commercially available in market that dissipate more than 30KW which corresponds to 4,800 W/ft^2 rack heat flux.

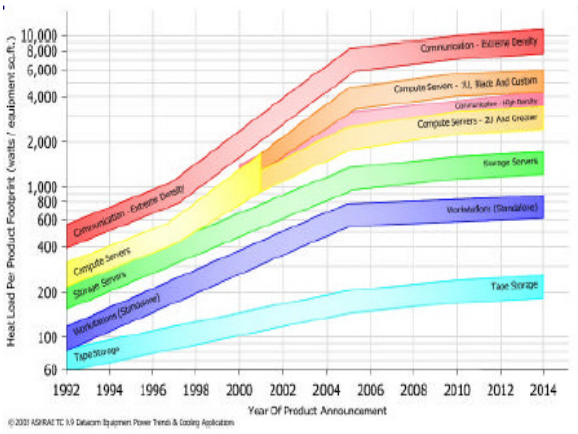


Figure 2.2 Heat load trends [6]

2.3 Data Center Cooling

Any active electronics requires provision for cooling. Shown in figs. 2.3 and 2.4 are the two commonly used configurations of air supply namely, underfloor and overhead. Both these configurations use hot aisle – cold aisle layout in an attempt to isolate chilled air supply from hot air. The front face of the rack, which generally is air inlet for the equipment, is placed facing the perforated tiles. The backside of the rack, from where the hot air exhausts, faces the backside of an another rack. This forms the hot aisle. A typical arrangement of underfloor air supply configuration is shown in Fig. 2.3.

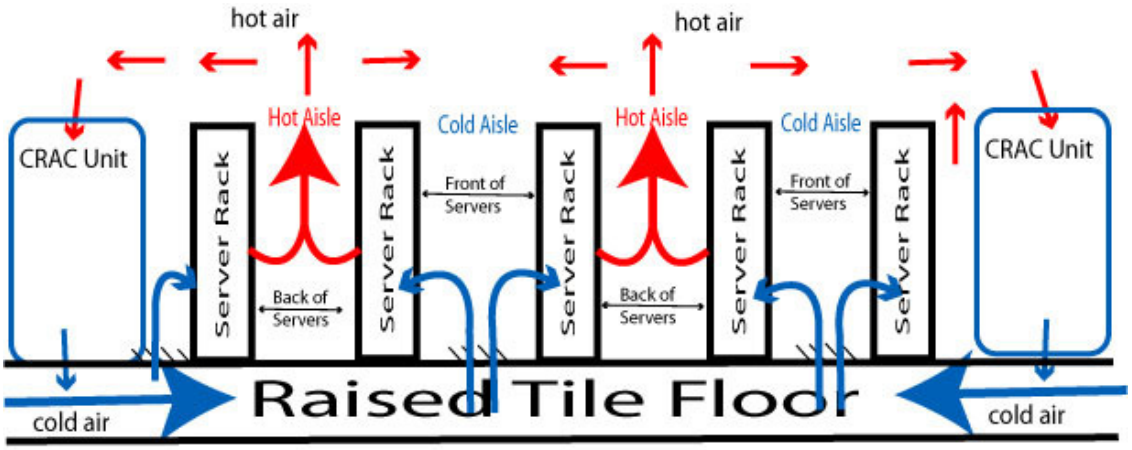


Figure 2.3 Raised floor data center [7]

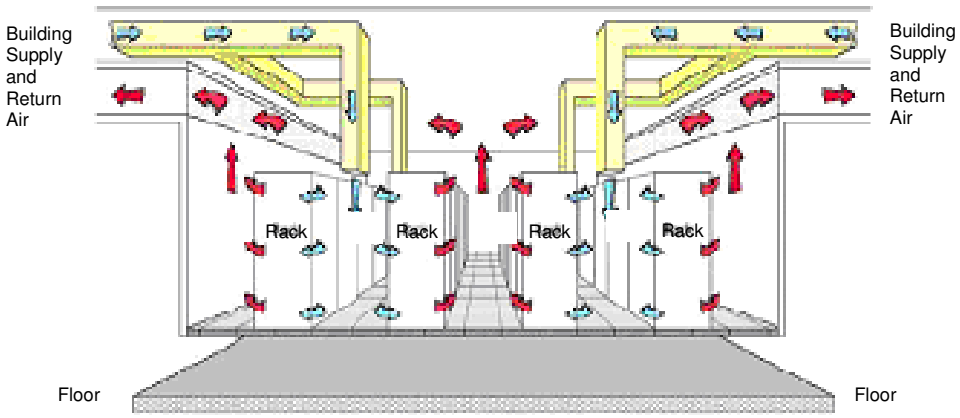


Figure 2.4 Overhead air supply configuration [6]

The Computer Room Air Conditioning unit (CRAC) delivers the chilled air into the space below the raised floor. This chilled air enters the room through the perforated tiles, passes through the racks (over the electronics) and gets heated up. This hot air then returns to the CRAC intake. In overhead supply configuration (Fig. 2.4), chilled air enters the room via overhead diffusers. After passing through racks, the heated air then exits room via vents on the wall. This hot air eventually passes through heat exchanger and is then supplied back as chilled air through diffusers.

2.4 Energy Consumption in Data Center

Generally, data centers are connected to utility grid from where electricity is received at building envelope. This is then split into two broad streams:

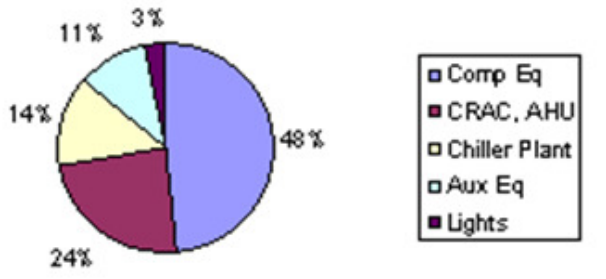
1. Uninterruptible loads such as IT equipment that requires continuous operation.
2. Other loads, which can sustain temporary interruption

Electricity for uninterruptible loads is channeled through Uninterruptible Power Supplies (UPS). The UPS acts as battery in the event of power outage and supplies electricity to IT equipment till backup generator is operational. It also absorbs any fluctuations in incoming supply and provides more uniform power. All incoming AC power is converted to DC and the batteries are charged. This DC power is then converted again to AC before it leaves UPS.

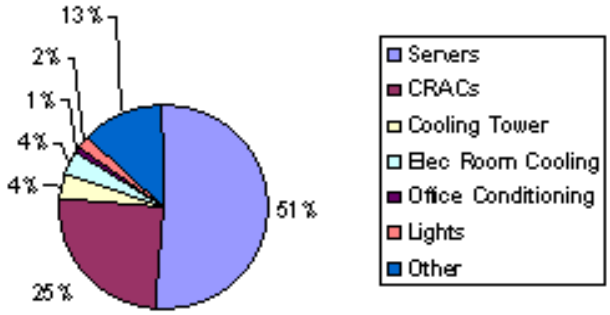
Electricity leaving UPS is then received by Power Distribution Units (PDU) and is supplied to server racks. These servers have Power Supply Unit (PSU) that converts AC power into low voltage DC

power which is then consumed by internal components such as Central Processing Unit (CPU), memory, disk drive, chipset and fans. Thus, data centers have three principal components that require significant energy namely IT Equipment, Cooling System and PDUs. A study from Lawrence Berkeley National Laboratory (LBNL) [8] has reported that for year 2005, server driven power usage in U.S. and Worldwide was 5000 MW and 14000 MW respectively which was 1.2% and 0.8% of the total energy consumption. This consumption translated into energy cost of $2.7B for U.S. and $7.2B for the world. With costs running so high and server density on increase, there is growing interest in understanding and improving the energy efficiency of data centers.

A break-down of power consumption of data center has been studied. Two such break-downs from two different case studies [9, 10] are presented in Fig. 2.5. Although slight variations are inevitable, these case studies confirm general estimate that server load constitutes half the power of total consumption where as cooling infrastructure claims almost one third of the total power.



(a)



(b)

Figure 2.5 Break-down of Power Consumption of Data Centers- (a) [4] and (b) [5]

Until recently, data center operators' prime concern was data center operating reliability and not the energy efficiency. Hence most of the data centers were over provisioned based on worst case scenario. However, with power densities reaching to levels that lead to limitations, energy efficiency is now seen as a way to solve these problems. The benefits of reducing energy inputs at various levels are:

- Reduction in cost.
- Lesser demand on utility grid hence improved reliability.
- Avoided investment in power plants.
- Reduced dependence on fossil fuels.
- Less greenhouse emissions.

2.5 Energy Consumed for Data Center Cooling

Since cooling infrastructure consumes about one third of total data center power, it also provides potential for cooling solutions that will be energy efficient. A case study [11] of a typical data center gives further break down of energy consumption by various components of data center cooling. This break-down of energy is shown in Fig. 2.6. The study shows that chiller compressors are the largest contributor of cooling energy consumption at 41.2% followed by CRAC units that utilize 27.6% of the total cooling power.

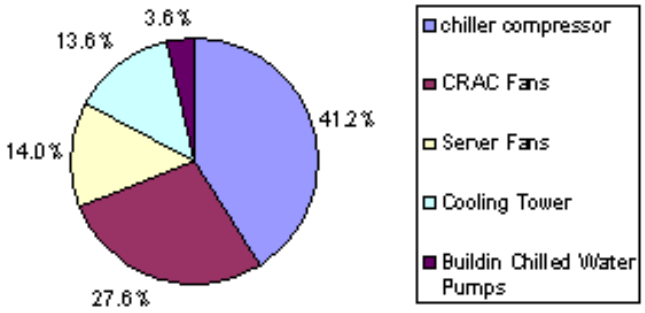


Figure 2.6 Break-down of Cooling Energy Consumption [11]

2.6 Airside Economizers

The use of airside economizers leads to different configuration than what is discussed above. The air handling units in this scenario are placed outside the data center, often on rooftop. The air is then ducted into the data center and also from the data center. The outside air can be utilized 100% for the cooling of IT equipment when the outside temperature is either less than or equal to the supply temperature. This eliminates the use of chiller circuit entirely. However, when the temperature of outside air is greater than the supply temperature but still less than the temperature of return air, then the outside air can be used with chiller circuit. A schematic arrangement of airside economizer is shown in Fig. 2.7.

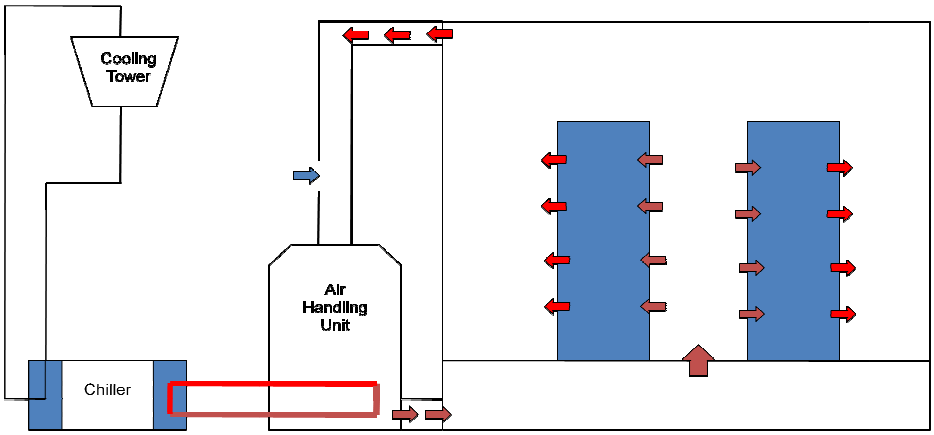


Figure 2.7 Schematic of Airside Economizer Configuration

In their proof of concept test, Intel IT has been running 900 production servers at very high rate of utilization [12]. This high density data center used 100% air exchange at 90°F and without humidity restrictions. The filtration was kept at the minimal level. It was estimated that with the economizer in use 91% of the time, 67% of the energy can be saved. This translates to about USD 2.87 million in a 10MW data center. The proof of concept test by Intel also showed no significant rise in server failure rates when air side economizer is used.

A study by Shehabi *et al.* [13] compares the energy implications of conventional data centers with newer technologies employing waterside and air side economizers in five different climate zones in the state of California. They report that airside economizer performs consistently better in all climate zones. In

fact according to another study by Syska Hennessy Group [14], outside air can be used for almost entire year in San Francisco.

2.7 Objective

The cooling strategy for data center is layout specific. Each data center has different set of parameters for its energy efficient operation. In the proof of concept by Intel [12], they showed that the air side economizers can be used to significantly reduce the energy consumption. They did this by performing a yearlong experiment in their New Mexico facility. Data center performance is layout specific and performing experiments each time would be extremely time consuming and expensive. Numerical technique to estimate the amount of energy saving would be beneficial. Thus, the objective of this study is to establish a numerical technique to determine the impact of air side economizer on the energy consumption. This would save time and money.

2.8 Numerical Modeling

Impact of air side economizers is numerically analyzed for four different layouts. In each case, rack inlet temperature and energy consumption by the cooling equipment is estimated. For a steady state analysis and assuming the flow to be incompressible, the governing equations are given by equations 2.1 - 2.3. Equations 2.1, 2.2 and 2.3 are the continuity, momentum and energy equation with k-ε turbulence model which form the governing equations..

$$\frac{\partial \mathrm{u}}{\partial \mathrm{x}}+\frac{\partial \mathrm{v}}{\partial \mathrm{y}}+\frac{\partial \mathrm{w}}{\partial \mathrm{z}}=0 \tag{2.1}$$

$$\begin{aligned}
\rho\left(u\frac{\partial u}{\partial x}+v\frac{\partial u}{\partial y}+w\frac{\partial u}{\partial z}\right) &= X-\frac{\partial P}{\partial x}+\mu\left(\frac{\partial^2 u}{\partial x^2}+\frac{\partial^2 u}{\partial y^2}+\frac{\partial^2 u}{\partial z^2}\right)\\
\rho\left(u\frac{\partial v}{\partial x}+v\frac{\partial v}{\partial y}+w\frac{\partial v}{\partial z}\right) &= Y-\frac{\partial P}{\partial y}+\mu\left(\frac{\partial^2 v}{\partial x^2}+\frac{\partial^2 v}{\partial y^2}+\frac{\partial^2 v}{\partial z^2}\right)\\
\rho\left(u\frac{\partial w}{\partial x}+v\frac{\partial w}{\partial y}+w\frac{\partial w}{\partial z}\right) &= Z-\frac{\partial P}{\partial z}+\mu\left(\frac{\partial^2 w}{\partial x^2}+\frac{\partial^2 w}{\partial y^2}+\frac{\partial^2 w}{\partial z^2}\right)
\end{aligned} \tag{2.2}$$

$$\begin{aligned}
\frac{\partial}{\partial t}(\rho k)+\frac{\partial}{\partial x_i}(\rho k u_i) &= \frac{\partial}{\partial x_i}\left[\left(\mu+\frac{\mu_t}{\sigma_k}\right)\frac{\partial k}{\partial x_i}\right]+G_k+G_b-\rho\varepsilon\\
\frac{\partial}{\partial t}(\rho k)+\frac{\partial}{\partial x_i}(\rho\varepsilon u_i) &= \frac{\partial}{\partial x_i}\left[\left(\mu+\frac{\mu_t}{\sigma_\varepsilon}\right)\frac{\partial \varepsilon}{\partial x_i}\right]+C_{1\varepsilon}\frac{\varepsilon}{k}(G_k+C_{3\varepsilon}G_b)-C_{2\varepsilon}\rho\frac{\varepsilon^2}{k}
\end{aligned} \tag{2.3}$$

The baseline case (Case 1) is the conventional data center configuration with CRAC units and underfloor supply. In addition, three different configurations are also modeled to represent the airside economizer scenario of supplying the outside air into the datacenter. The rack layout, cold aisle specifications (tile opening), heat load and flow requirement of each case is identical. Also, for all the cases the server room dimensions remains unchanged. Detail numerical modeling of each case is explained in the following sub-sections.

2.8.1 Case 1

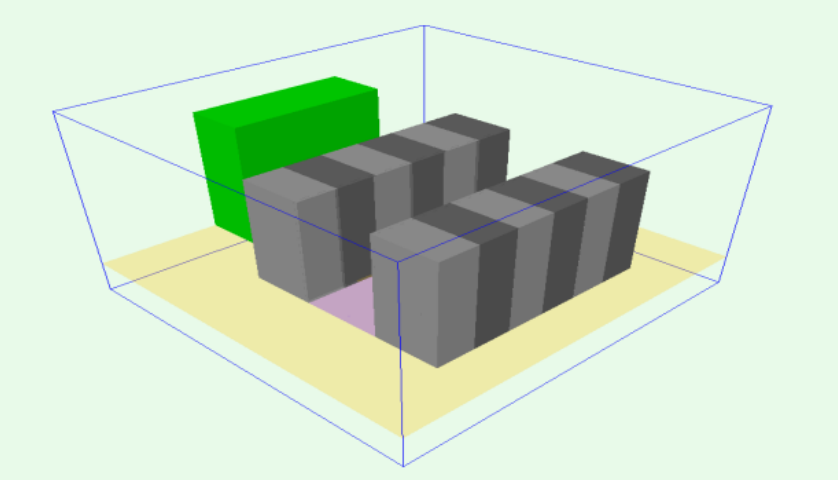


Figure 2.8 Representative model of data center in Case 1

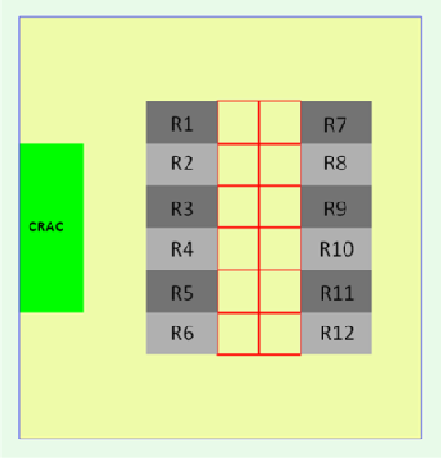


Figure 2.9 Data center layout for Case 1

A representative data center with underfloor configuration as shown in Fig. 2.8 is modeled using commercially available CFD code [15]. The half symmetry model of data center "cell" has 12 racks arranged in cold aisle – hot aisle layout as shown in Fig. 2.9. The footprint dimensions of the half-symmetry "cell" are 19ft (5.7 m) by 20 ft (6.0 m), and the room was 10 ft (3.0 m) tall. It has the raised floor with a plenum of 2 ft depth. The cabinets are 600mm wide, 1000mm deep and 45U or 2000mm tall. The air-moving device inside the racks is assumed to force the air straight through the rack, with a constant velocity across the front and back of the racks. Each rack is assumed to be a 11 kW (37,534 Btu/h) rack, with a rack airflow rate of 965 cfm (0.45 m^3/s). This corresponded to an air temperature rise through the rack of 20°C (36°F) a data supplied by OEM, considering the specific heat of air 1.006 kJ/kg°K and the density 1.2 kg/m^3. The temperature of the chilled air entering the room through the perforated tiles was fixed at 15°C (56°F). The CRAC unit had a 3 ft × 8 ft (0.91 m x 2.4 m) footprint and was 2.4 m (8 ft) high. Figure 6 shows the data center layout for case 1 wherein R1, R2,....,R12 refer to the rack numbers.

2.8.2 Case 2

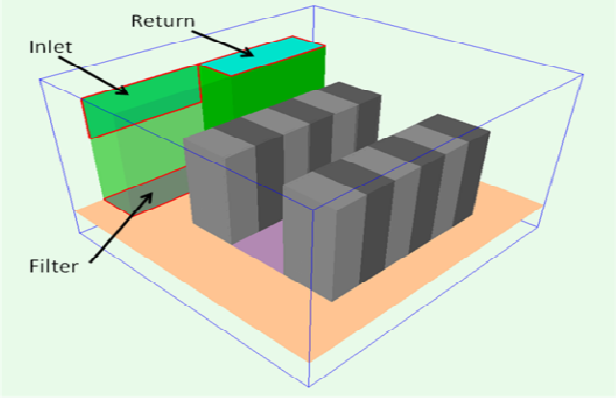


Figure 2.10 Data center model for Case 2

Figure 2.10 shows the model used in case 2. This model is similar to case 1 except that the CRAC is replaced by two air handling units. One of the unit delivers the outside air into the data center while the other acts as the outlet for returning hot air which is subsequently dumped into the ambient. Depending upon the outside temperature, various possibilities of chiller usage exist. If the temperature outside is cooler than the supply temperature, the chiller is not used at all. If outside temperature is more

than the supply temperature but less than the temperature of returning air, partial chiller operation is required to obtain set point temperature. However if the outside temperature is more than the return temperature, the conventional CRAC unit is operational. Here however, it is assumed that the outside temperature is same as the supply temperature and no chiller or mixing is required.

2.8.3 Case 3

In this model, as shown in Fig. 2.11, a duct is created which has two fans at either end. Each of the fans deliver 5790 cfm of outside air into the duct. Through the opening in the duct, the air is introduced into the under floor plenum and subsequently delivered into the room. This is the simplest configuration wherein depending upon the requirement either the air side economizer or the CRAC unit can be used.

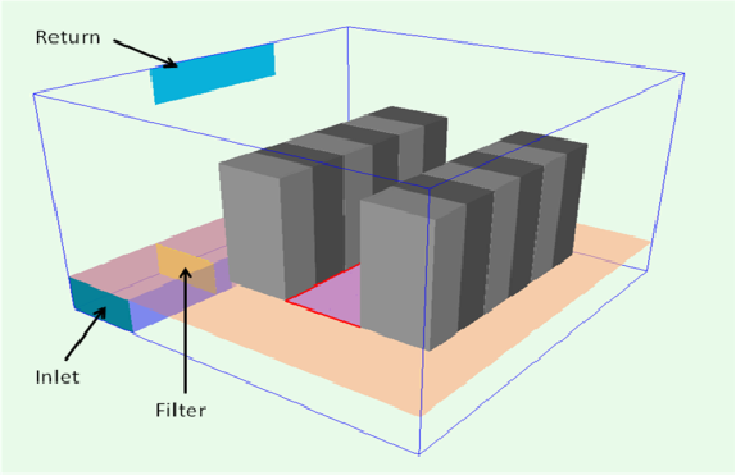


Figure 2.11 Data center model for case 3

2.8.4 Case 4

In this case, as shown in Fig. 2.12, a duct is used in under floor plenum to deliver the cold air into the data center room through the perforated tiles. The outside air is pumped into this duct by a fan. The returning hot air is released into the ambient.

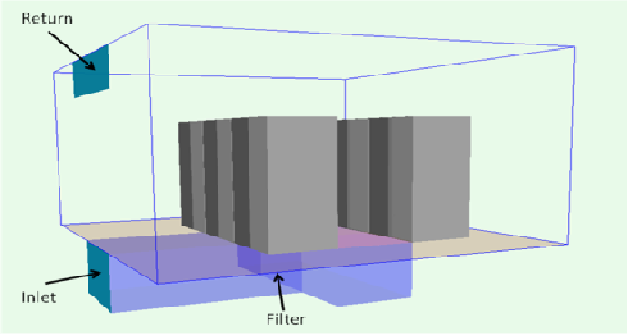


Figure 2.12 Data center model for Case 4

Whenever air side economizer is used, filtration is required in order to prevent the dust particles from entering the data center. Intel in their proof of concept facility in New Mexico used common household filters to test the air quality. Typically MERV 11-7 filters are recommended[16]. In the numerical analysis (cases 2- 4), the air filter was modeled using a planar resistance.

2.9 Mesh Sensitivity

A mesh sensitivity analysis was carried out for each case to insure the grid independence of output variables. The grid cells count selected is within the range where output variables show no variation. Figure 2.13 shows the graph for case 1.

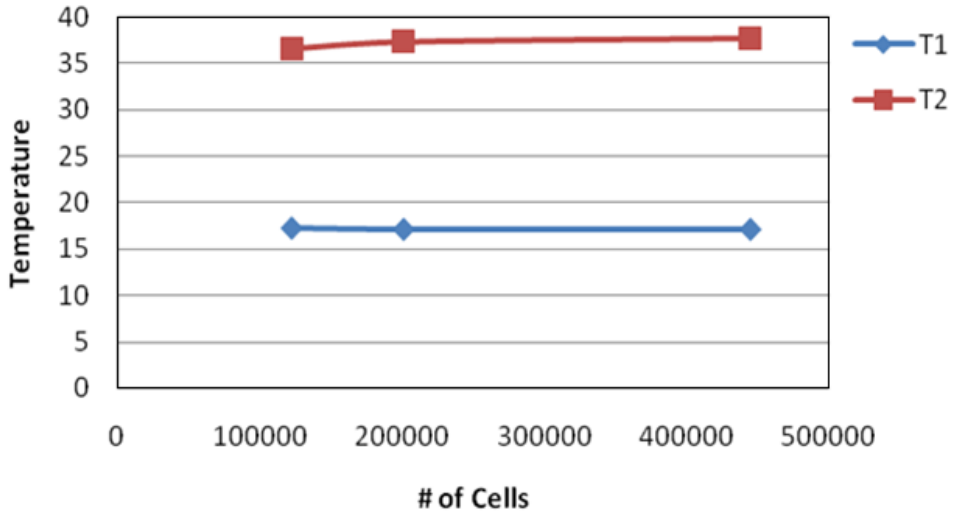


Figure 2.13 Mesh sensitivity analysis for case 1

2.10 Results

Aforementioned cases were solved using K-ε turbulence model in Flotherm [10]. The rack inlet temperature was monitored for all the racks along the height at the interval of 300mm. Figures 2.14 through 2.17 indicate the variation in RIT.

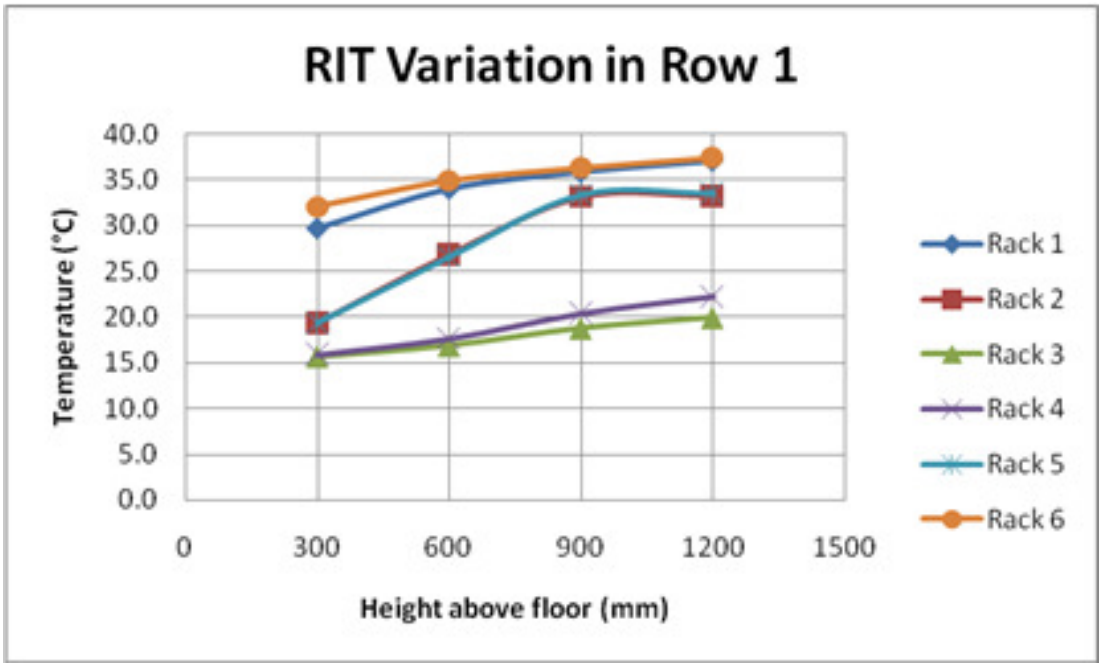
For case 1, the RIT recorded at the outer racks is higher than the RIT's at inner racks. The temperature profiles are symmetric in nature. Typically, hot air infiltrates the top region of the outside rack resulting in RIT's that are higher than the design guidelines. Racks 1 and 6 show similar trends and so do the inner pairs of racks 2 and 5, and racks 3 and 4. There are at least 10 instances where the critical temperature of 35°C is exceeded.

In case 2, the temperature profiles do not follow the pattern described above for case 1. This irregularity is attributed to the uneven distribution of air as a result of inlet and return locations not being centrally located. Five instances exceeding 35° are reported in this scenario.

In case 3, the temperature profile pattern hold good as the pair of racks indicate similar temperatures. The rack inlet temperatures recorded in second row are lower than those recorded in the first row. All recorded rack inlet temperatures are at or below 35°C.

Amongst all the four cases, the minimum rack inlet temperatures are recorded in case 4. It follows the pattern of similar profiles. Also, as noted in case 3, the rack inlet temperatures recorded in second row are lower than those recorded at first row.

In all the cases, variation in rack inlet temperature is due to the mal-distribution of air in the cold aisle. Each tile is ideally supposed to dispense the required airflow for the rack next to it. However in practice, some tiles deliver more air than required whereas other tiles deliver less amount of cold air. This mal-distribution results in severe recirculation as a result of which the rack inlet temperatures increase. Also, the variation in rack inlet temperature along the height of the rack depends upon the flow delivered by the tile next to it. Figure 2.18 shows the formation of recirculation cells for case 4.



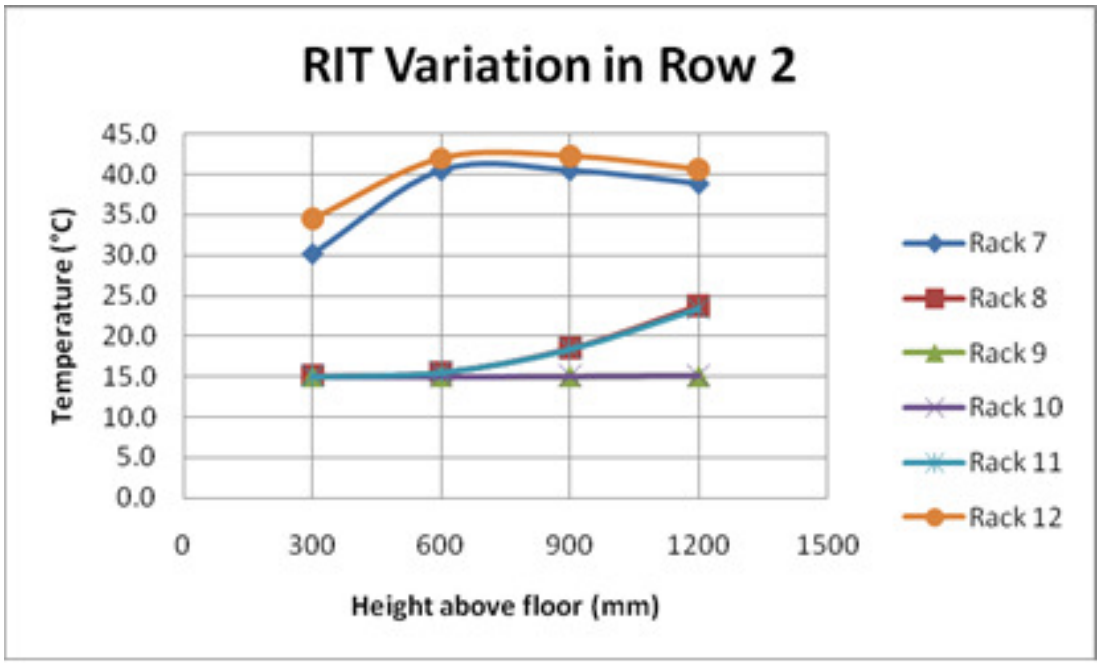
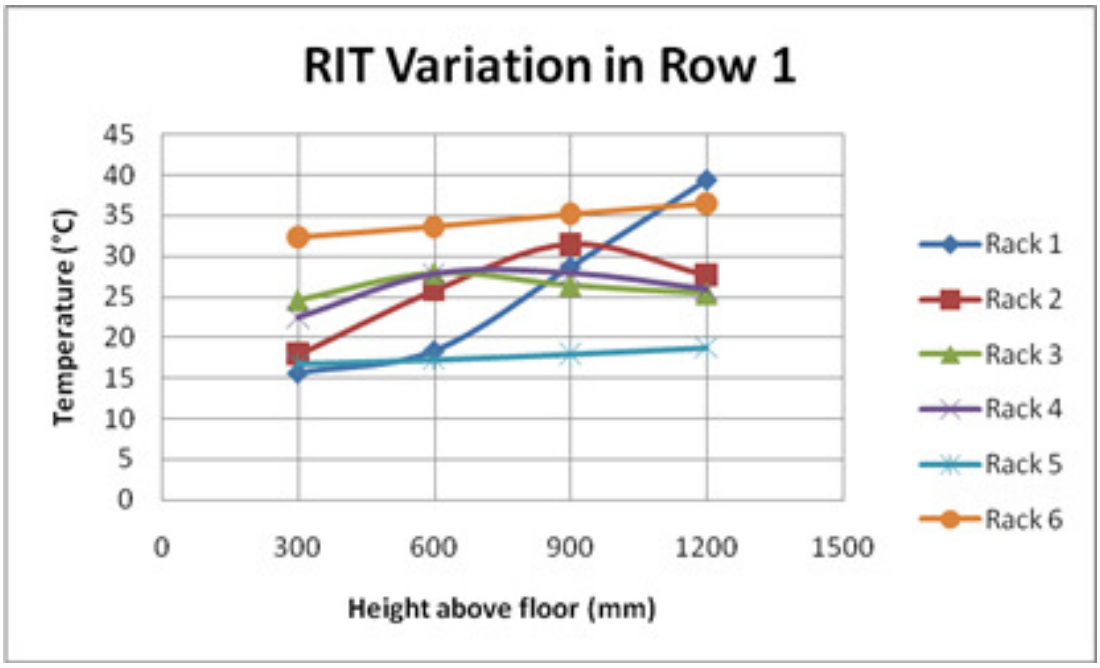


Figure 2.14 Variation in RIT for case 1



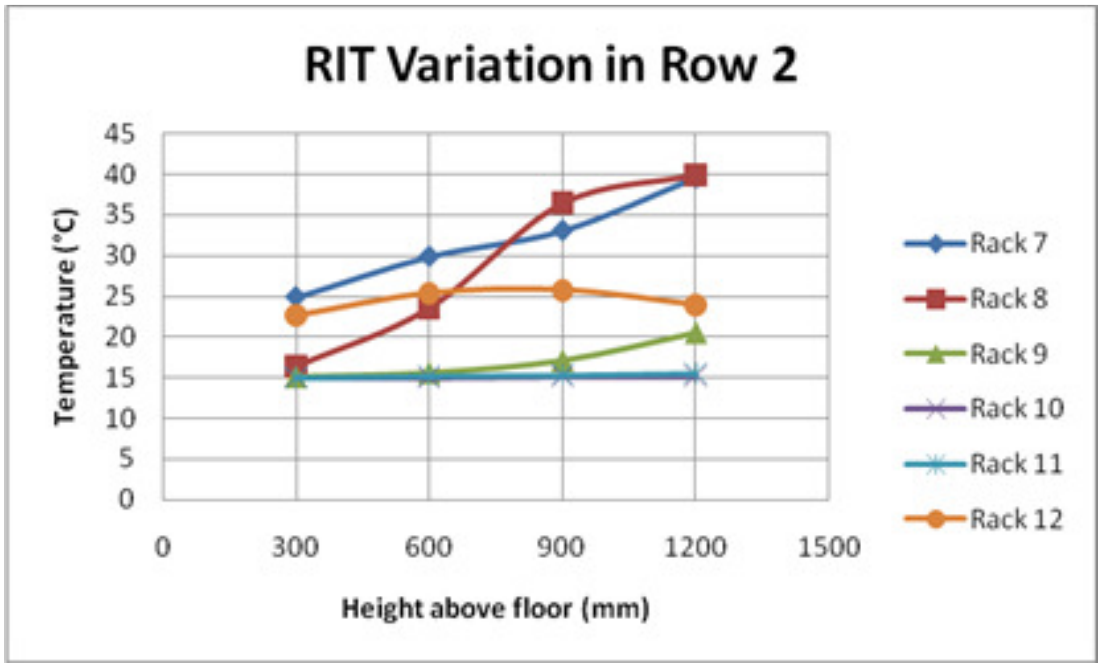
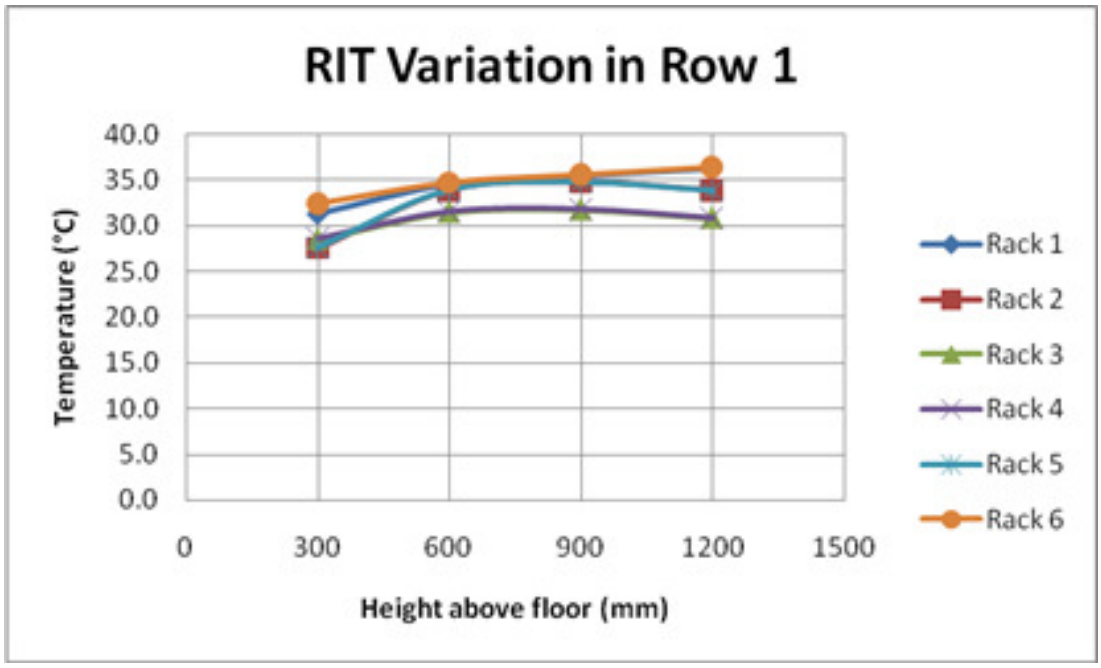


Figure 2.15 Variation in RIT for case 2



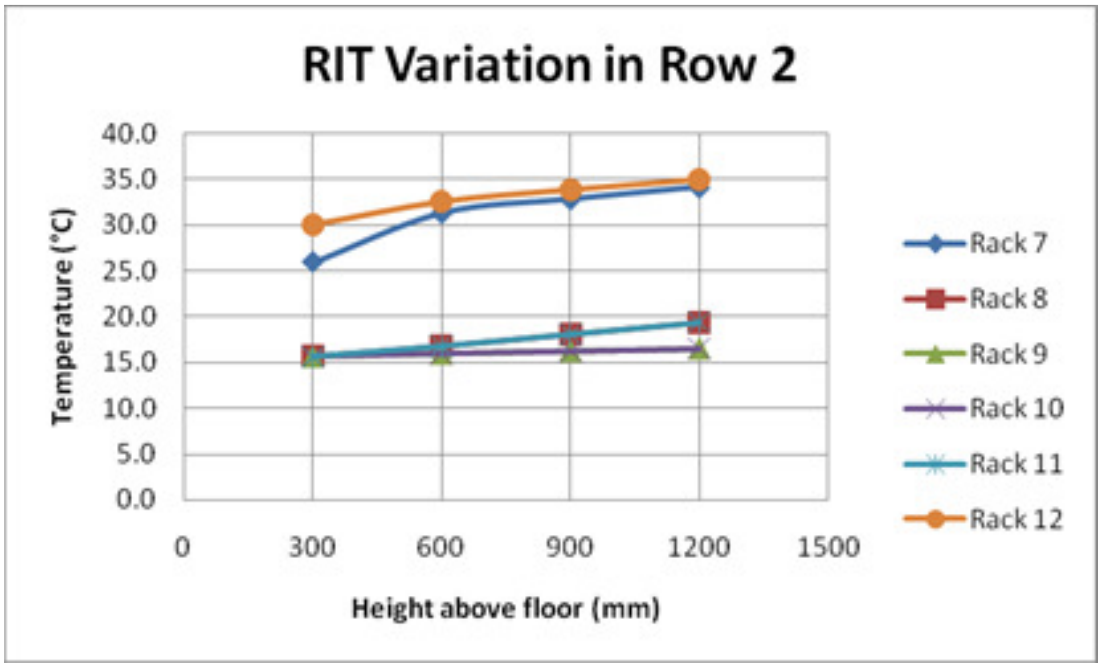
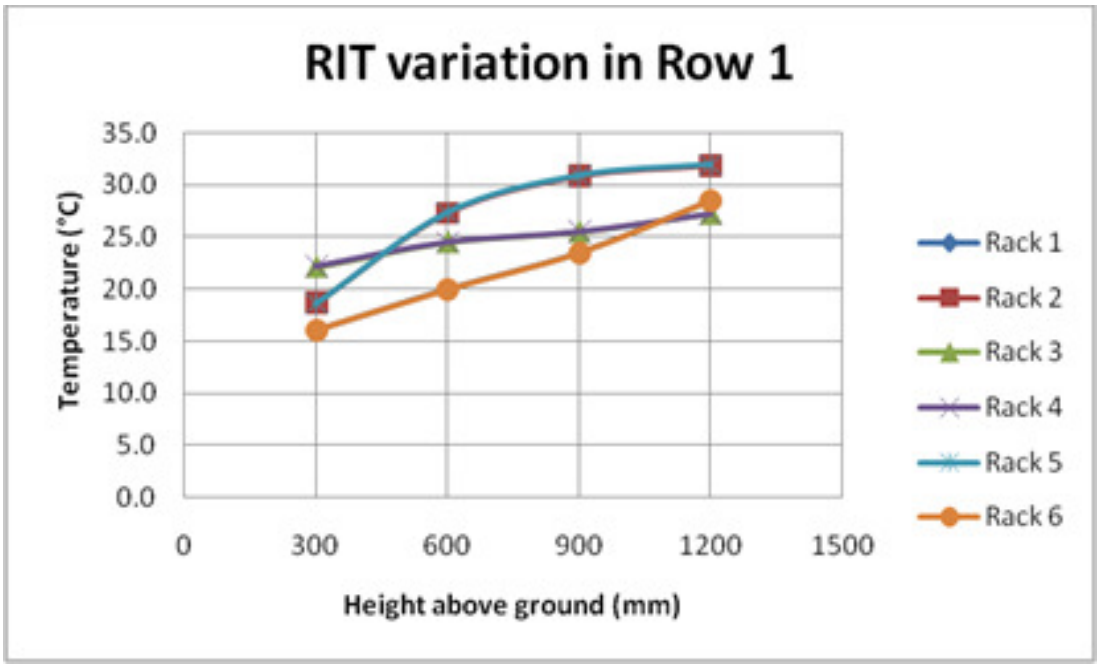


Figure 2.16 Variation in RIT for case 3



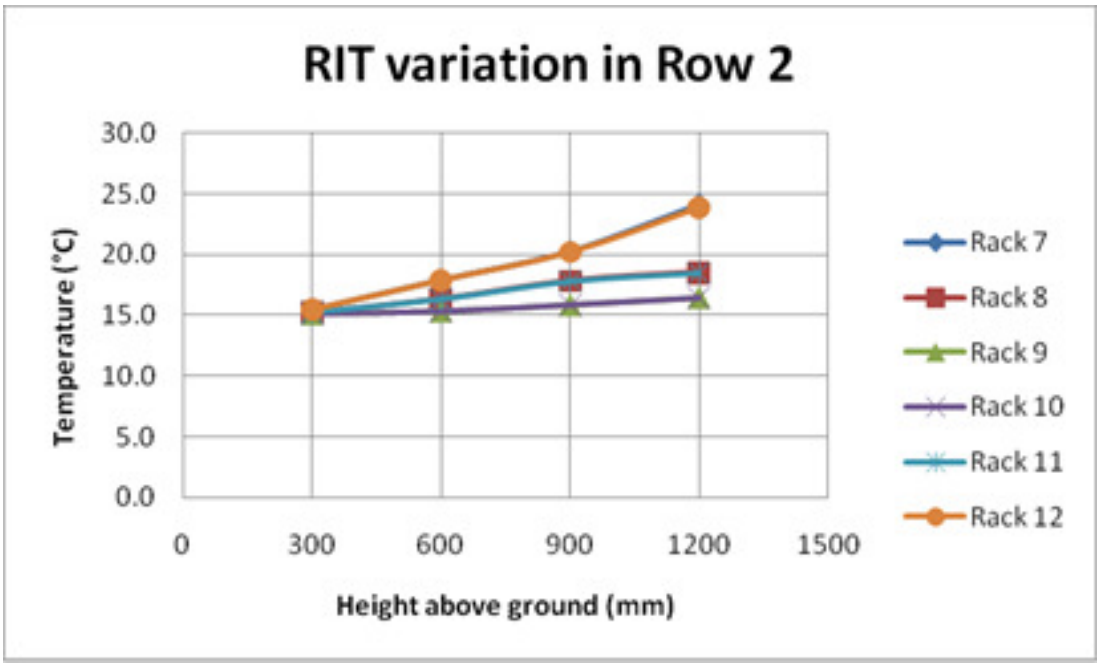


Figure 2.17 Variation in RIT for case 4

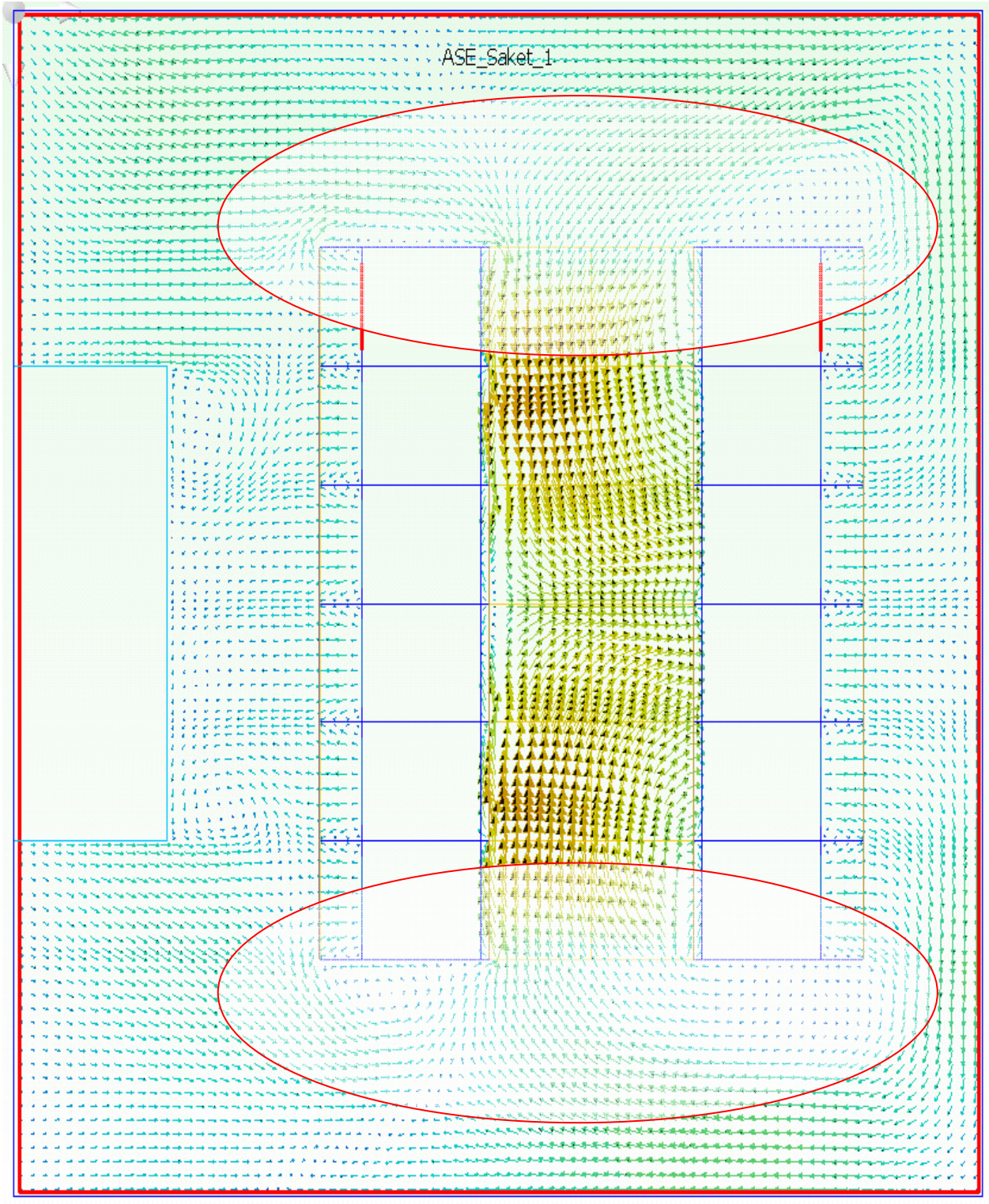


Figure 2.18 Recirculation in outer racks for case 4

2.11 Energy Consumption

The advantage offered by airside economizer is the savings in energy due to reduced or no chiller operation. In conventional data center operation, typical power consumption of a 30 ton CRAC unit is about 7.5kW [17]. Although in case 1, the cooling required is more than 30 ton, for comparison purpose, the consumption is considered to be 7.5kW. The energy consumed by the fans in cases 2-4 is estimated using the equations 2.4-2.7 [18]. Table 2.2 provides the summary of the estimates.

Power P, consumed by fan:

$$P(hP) = \frac{Q \times TP}{6356 \times \eta_m} \tag{2.4}$$

$$P(KW) = \frac{P(hP)}{1.3} \tag{2.5}$$

Total Pressure,

$$TP = SP + VP \tag{2.6}$$

Velocity Pressure,

$$VP = \left[\frac{V\ (fpm)}{4005}\right]^2 \tag{2.7}$$

In the above equations, 'Q' is the flow rate (cfm), 'SP' is the static pressure (in. of water), 'V' is the cross sectional velocity (fpm), 'VP' is the velocity pressure (in. of water) and 'η_m' is the mechanical efficiency which was assumed to be 75%.

Table 2.2 Power consumption estimate

Case	Power Consumption (kW)
1	7.5
2	0.9
3	2.38
4	1.97

2.12 Summary

The impact of airside economizers on thermal management of data center is discussed. Three different data center configurations are modeled which utilize airside economizer thereby eliminating the need for computer room air conditioning units. The conventional data center with CRAC units is also modeled. The results indicate that in the air side economizer scenario, substantial energy savings can be gained. However, if parameters such as duct size, air filter and location of the fans are critically selected then the fan static pressure may increase resulting in more energy consumption. Also, it is necessary to determine the total cost of operation as the reduction in energy consumption may increase the maintenance cost due to additional infrastructure for air side economizers. The study presented in this paper, is the first step towards the robust computational modeling which will predict the energy expended considering various components of the air handling systems.

CHAPTER 3

THERMAL ANALYSIS OF A PACKAGE ON PACKAGE

In microelectronics, a package is an enclosure that provides a platform for component mounting to printed circuit board (PCB) protecting the components from moisture, contaminants and mishandling [19]. It also provides a path for heat removal. Some of the package functions are [19]:

- Electrical and functional connections between various devices.
- Mechanical structure and support to allow manufacturing assembly operations.
- Power distribution to all components and chip circuits.
- Protecting from environment and mechanical damage.
- Shielding from external electromagnetic radiation going out of the box.
- Heat removal generated by the chip circuits and other components.
- Support of the system's organizational requirements.
- Allowing removal and replacements of failed components.

Thus, in order to ensure proper functioning of any electronic devices that are used for consumer electronics, medical devices, military applications etc., it needs to be packaged so that it can fulfill the entire package functions mentioned above.

Based on the interconnect technology that is utilized, packages can be classified as wire bond packages, flip chip packages, tape automated bonding (TAB) packages, ball grid array (BGA) packages and chip scale packages (CSP). In wire bond packages, gold or aluminum wires are used to establish electrical connections. The typical wire size that is used, ranges from 0.025 to 0.05 mm [19]. Figure 3.1 shows a schematic representation of a wire bond package.

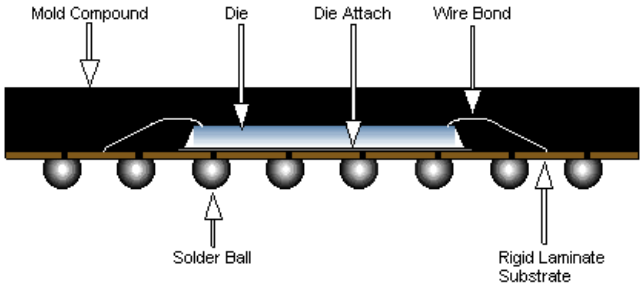


Figure 3.1 Wire bond package [20] (Courtesy of Amkor Technology)

In flip chip packages, the active side of the chip is flipped down. The chip terminal pads face down and are then connected to the carrier pads via solder or gold bumps. This particular technology provides the highest interconnection density for a given area and electrical performance [19]. Figure 3.2 shows a schematic representation of a flip chip package.

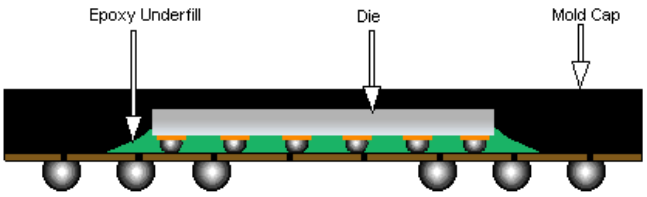


Figure 3.2 Flip-chip package [20] (Courtesy of Amkor Technology)

In TAB packages, flat metal fingers are used to form an interconnection between the chip pads and leads on the carrier tape. Typically, the leads on the chip side are of smaller size and then fan out to a larger pitch for tape pads. Figure 3.3 shows a schematic representation of a TAB package.

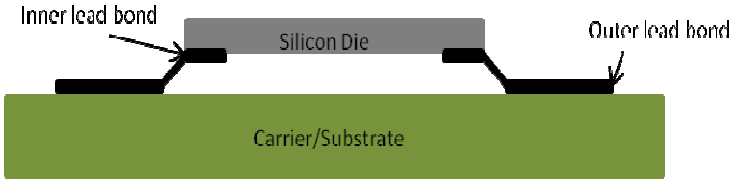


Figure 3.3 Tape automated bonded package

In BGA packages, an area array of solder balls is used for second level interconnects. The BGA packages have small footprint, high I/O count and are lightweight. For these reasons they are typically used for portable electronics. Figure 3.4 shows a schematic representation of a BGA package.

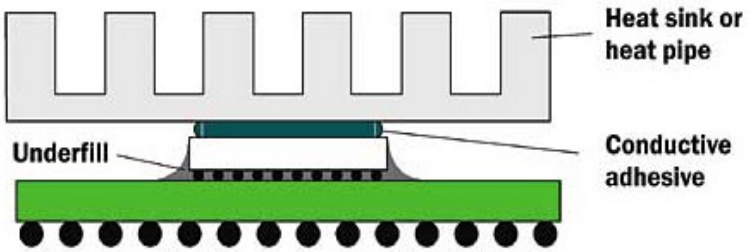


Figure 3.4 Schematic representation of a BGA package [21]

CSP are similar to BGA packages with a exception that the footprint is 1.2 times the die size. They are sometimes referred as "mini-BGA" or "micro-BGA" [19]. They are typically used for low I/O packages (memory). Figure 3.5 shows a schematic representation of a flip chip CSP.

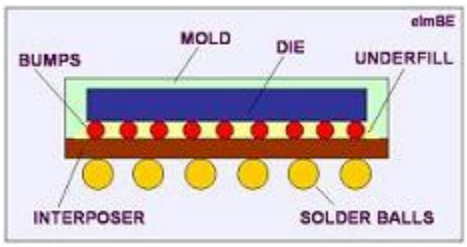


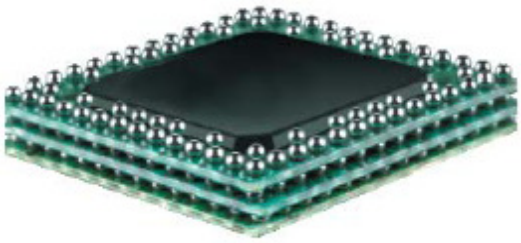
Figure 3.5 Schematic representation of a flip chip CSP [22]

A microelectronic device may consist of several packages (memory, logic, etc.) that are mounted near to each other on a single PCB. This consumes lot of real estate on the PCB which results in larger device dimensions. This type of configuration is referred as 2-dimensional (2D) or planar packaging. In the past few years, due to demand of increased functionality and reduced size, different packages are now stacked on each other. Such

configuration is known as 3D packaging. This technology is been further discussed in the following sections.

3.1 3D Packaging

In response to the demand for smaller, lighter devices along with the increased functionality, technology is forced to move from conventional 2D packaging to 3D packaging. In 3D packaging, various units such as computational processing units (CPUs), memory, logic, RF antennas are stacked on each other, taking advantage of the third dimension and providing a volumetric packaging solution for higher integration and performance. Many commercial 3D packages already exist in market providing maximum silicon integration and area efficiency at a minimal cost. Figure 3.6 shows example of 3D packages that are commercially available [23, 24]. It is important to note that the profile or height in the third direction is reduced by goingto "thinner wafers" and "die attaches."



(a)

(b)

Figure 3.6 Examples of 3D packaging (a) Stacked CSP by Amkor [23]
(b) 8 die µZ-Ball stack by Tessera [24]

Today over 30 companies such as Amkor, 3D-plus, ASM international, Tessera, Intel, Infineon, Texas Instruments, IBM, Freescale, Fujikura, Zycube etc. are in the market with functional 3D packages. The market for 3D packaging mainly includes but not restricted to consumer electronics such as mobile phones, mp3 players, digital cameras, camcorders, laptops etc.

3.2 Advantages of 3D packaging

In one of the webcast [25] and also mentioned in white papers by WaytroniX [26], Steven Koester from IBM Fishkill said, "3D integration will establish a new scaling path that will extend Moore's Law beyond its expected limits." With reference to that, 3D packaging has following advantages:

1. Shorter interconnects:

   As per an article [27], an IBM researcher Thomas Brunschwiler said, "Electrical interconnects are in a wiring crisis; the wiring does not scale the way transistors scale, because the width of the wires is shrinking but their lengths is not." He then mentioned stacking of dice is a viable solution to this crisis, which will permit the interconnects to go in between the dice; thus reducing their lengths by up to 1,000 times.

2. Higher electrical performance:

   By reducing length of electrical interconnects, shorter communication paths and increased bus speeds are obtained thus enabling high performance through more economic parallel, fabric communications [26].

3. Reduced power consumption.
4. Reduced size and weight.
5. Heterogeneous packaging of different modules such as memory, logic, RF devices for communication etc on smaller footprint is possible.

3.3 3D Packaging configuration

Similar to conventional packages, 3D packages can also be classified based on the technology and configuration. They are categorized as stacked architecture, package-on-package (PoP), package-in-package (PIP) and through silicon vias (TSVs).

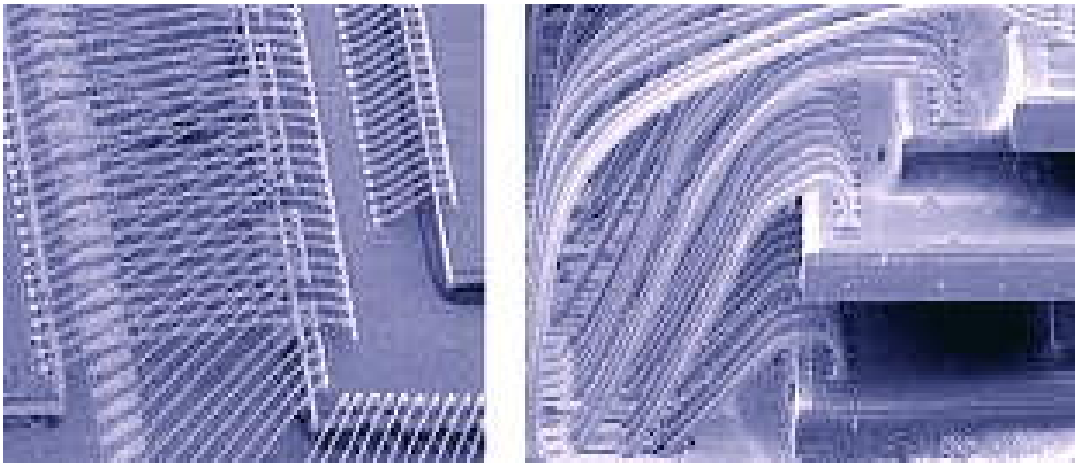


Figure 3.7 Wire bonded stack die package [22]

In stacked architecture, multiple dice are mounted on top of each other in a single package. Based on the method of stacking they are sub-classified as pyramid, spacer, rotated and staggered die configurations. Figure 3.7 shows the schematic view of each configuration. As many as six or more dice can be used for an integrated use of various functions such as memory, logic, analog, mixed-signals etc. For electrical interconnects, wire bonding, flip chip or a combination of both are used, wire bonding been more common. Wire bonding being a peripheral technology can only accommodate interconnects at the edge (4n-4) of the die. Conversely, a flip chip package is an area array technology enabling n^2 interconnects. For stack configurations with more than four dice, wire bonding may become complex as shown in Fig. 3.7. As a result, use of flip chip interconnects is now becoming more popular as it also facilitates smaller package dimensions.

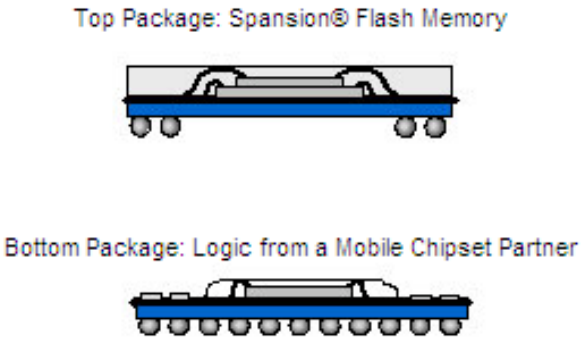


Figure 3.8 Flexibility in PoP [28]

PoP involves stacking individually packaged die in vertical direction. For example, memory and logic are packaged separately and then mounted on top of each other with a standard interface (BGA interconnects) to route signals between them. Because of the space saving ability they are typically used in mobile handsets, digital cameras, PDAs and MP3 players. Figure 3.8 shows the flexibility in PoP packages as top and bottom packages are fabricated independently by different vendors.

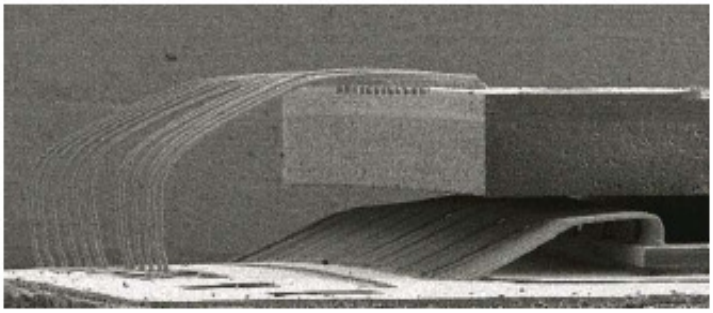


Figure 3.9 Qualcomm's PiP [29]

In PiP, two are more packages are assembled together and over molded to form a single package which is then mounted on a PCB. It is more expensive than stacked die or PoP but is extremely reliable. Figure 3.9 shows the PiP fabricated by Qualcomm.

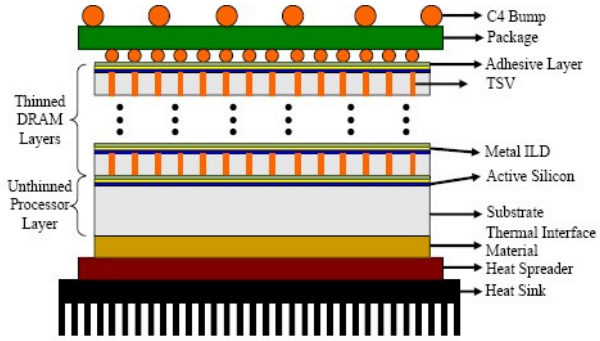


Figure 3.10 3D package with TSVs [30]

In TSVs, traditional method of electrical interconnections between all the dice (wire bond and flip chip) is established by vertical channels (vias filled with copper) through the silicon. These vias serve as electrical interconnect as well as path for heat removal. Few of the advantages of adopting TSVs are; more speed per package, more memory integration and capability to manufacture smaller circuits on a larger wafer. Figure 3.10 shows an example of 3D package with TSV.

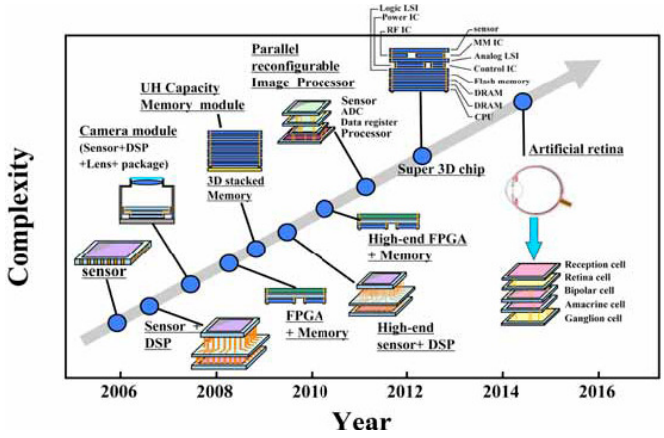


Figure 3.11 Technology roadmap for 3D packaging [31]

3D packaging is receiving increased attention as a result of which industries are now moving from R&D phase to commercialization phase. Figure 3.11 shows the technology roadmap for 3D packaging. In order to follow the roadmap, one of the major challenges to overcome is the thermal management of these packages. As more and more dice are stacked

on each other, thermal management of the center die becomes increasingly difficult. This issue is further discussed in the following section.

3.4 Thermal management of 3D packages

Even though a 3D package offers various advantages, many times its development as a product is restricted due to its poor thermal management. Chip stacking results in increased heat dissipation along with higher thermal resistance from the junction to the ambient. Few of the thermal issues are:

- Chips in the stack may overheat if appropriate cooling is not provided.
- Thin wafers result in formation of hot spots.
- Cooling solution must be cost effective for volume production.

As mentioned earlier, PiP are typically very expensive to fabricate and hence are not commonly used. However, stacked, TSVs and PoP architectures are now used in many low power applications. Thus, researchers have addressed several thermo-mechanical issues for stacked and TSVs architectures. However, very few research articles address thermal challenges for PoP architecture. Yang *et al.* [32] developed a network model to determine the junction temperature and also investigated thermal interactions between the bottom and top packages. In another study, Lee *et al.* [33] experimentally compared the thermal performances of dual die package and dual stack package for DRAM (Dynamic Random Access Memory) devices. However, none of the study performed thermal characterization of PoP. Also, from literature it can be observed that many studies [34-43] have been conducted on thermo-mechanical reliability of PoP.

Lately, focus has moved from air cooling to liquid cooling of stacked packages. WaytronX has developed a WayCool architecture for cooling 3D structures. It is a hybrid i.e. air and cooling configuration comprising of passive and active elements are designed to work independently in order to cool the system [26].

Also, IBM Zurich demonstrated liquid cooling (water) for stacked packages. Water flows through 50 micron channels, sandwiched between the stacked chips to cool it at the rate of 180 W per layer. This technology removes heat right at the source and provides effective way of cooling stacked chips. However, the product will not be commercialized before 2013 [9]. Even though liquid cooling provides efficient thermal management, the fabrication and maintenance cost is very high. Thus it becomes necessary to explore alternate techniques for efficient thermal management especially for hand held portable low power electronics where use of liquid cooling is not viable.

3D packaging is emerging as the technology for future. It has to serve the demand for continuous miniaturization in application related to consumer electronics, memories, processors etc. However, in order for 3D packaging to further move from research phase to commercialize phase, it has to overcome critical challenges like thermal management. In order to have effective thermal management, it is necessary to perform thermal characterization through which heat dissipation of a typical PoP structure can be studied. In this work, such thermal analysis of PoP is performed for different power combinations of logic and memory dice. Based on the results thermal design guidelines are provided.

3.5 Package Description and Modeling Procedure

In this study, a molded ball grid array PoP architecture is considered for the analysis. Figure 3.12 shows the front view of the PoP architecture under study. As seen from Fig. 3.12, two packages are considered.

The top package consists of two dice (both memory) stacked on each other in a pyramid configuration. For the top package, two die attaches are considered. One is used to isolate the top die from the bottom die while the other is used to mount the stacked pyramid structure on the substrate (top). Electrical interconnects is achieved via wire bond. A mold cap is also considered in order to protect the dice from any external contaminants, moisture or mechanical

damage. In Fig. 3.12 both wire bond and mold cap are deliberately not shown in order to make the stacked pyramid configuration visible.

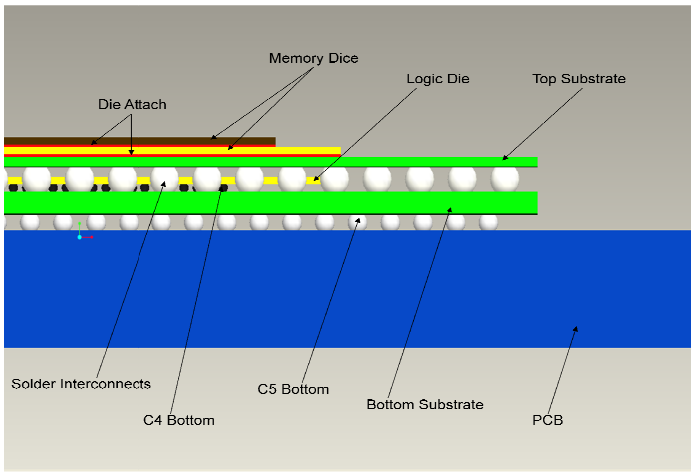


Figure 3.12 Schematic representation of the package details
(Note: Molding compound is not shown on purpose)

The bottom package is a flip chip package. The die (logic) with active side down is mounted on the substrate (bottom) via fully populated solder ball array of 26x26. These solder balls are typically referred as C4 interconnects as shown in Fig. 3.12.

The top substrate is connected to the bottom substrate via solder balls (BGA). These solder balls which also serve as electrical interconnects between the two packages are peripherally located in an array of 21x21 and 19x19. The array is depopulated in order to facilitate room for flip chip package on the bottom substrate. The standoff height for these solder balls depends on the thickness of the bottom package (flip chip + C4 interconnects). Thus, the two packages are mounted on each other to form the PoP architecture. This PoP is then mounted on the PCB via fully populated solder ball matrix of 14x14. These solder balls are often referred as C5 interconnects.

The PCB dimensions (76mm x 76mm x1.57mm) were as per the JEDEC standards. The remaining package dimensions are summarized in Table 3.1.

Table 3.1 Package Dimensions

Component	Memory Package (mm)	Bottom Package (mm)
Substrate	14 x 14	14 x 14
Substrate Thickness	0.13	0.3
Die	6 x 6 / 8 x 8	7.62 x 7.62
Die thickness	0.1 / 0.1	0.1
Die attach thickness	0.0318 /0.0318	NA
Mask thickness	0.0175	0.0175
Solder ball diameter	0.457	0.14(C4)/0.3(C5)
Solder ball height	0.32	0.1(C4)/0.21(C5)
Solder Pitch	0.65	0.3 (C4)/0.5(C5)
Ball Count	152	529(C4)/676(C5)

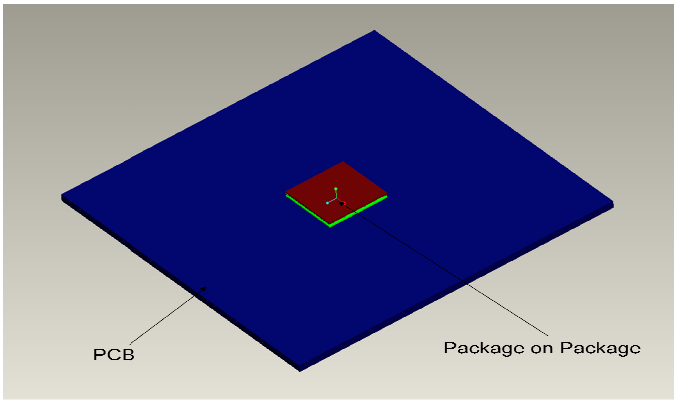


Figure 3.13 CAD model of the PoP

Due to the number of components and their complex assembly, individual models for die, BGA, C4, C5 interconnects, top and bottom substrate, etc. were created using Pro/E Wildfire 3.0 as “Parts”. Then, an “Assembly” of individual part is created to form the PoP architecture. Figure 3.13 shows the CAD model of the PoP architecture. Once the assembly is created it is imported to Ansys. Owing to the symmetric nature of the problem, an octant model is considered.

After, importing the model in ANSYS, respective material properties are applied. Material properties considered for analysis are as mentioned in Table 3.2. For most of the scenarios

(explained later), thermal conductivity of PCB in Table 3.2 is considered. However, in the last scenario to study the effect of conductive PCB and substrate, in-plane conductivity of 80W/m K and out-of-plane conductivity of 0.2 W/m K is considered.

Table 3.2 Material properties [23-25]

Component	**Thermal Conductivity (W/m-K)**
Die	120
Die Attach	0.3
Mold Cap	0.88
Substrate	0.418
Substrate Mask	200
Solder ball (SAC405)	57
PCB: In plane Out of plane	9 0.29
Underfill	0.8

Model was later meshed in order to generate approximately 285,000 elements. It was ensured that the results obtained are mesh independent. Convective heat transfer coefficient of 10W/m^2-K (natural convection) was applied for an ambient reference temperature of 20℃. Heat transfer coefficient was defined on mold top, mold side, top substrate side, bottom substrate side and on top and bottom side of PCB as shown in Fig. 3.14. An initial thermal analysis is conducted assuming that the logic die in the bottom package dissipates 1 W and the two memory dice in the top package dissipate 0.1 W each. Eleven different cases each with distinct power combination was considered for thermal characterization of PoP. Table 3.3 shows the steady state power assigned to each die for the DOE considered.

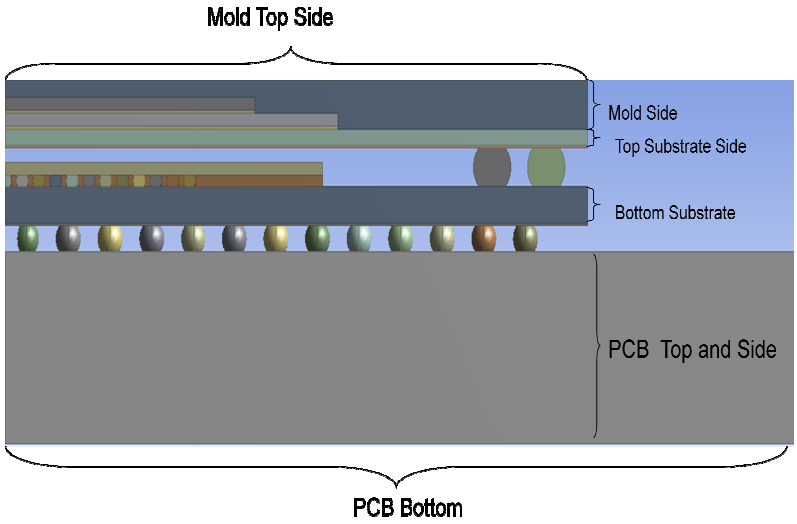


Figure 3.14 External surfaces of the PoP where convective boundary condition is defined

Table 3.3 Design of Experiments

Scenarios	Memory Die-Top [W]	Memory Die – Bottom [W]	Logic Die [W]
1	0.1	0.1	1
2	0.1	0.1	2
3	0.1	0.1	3
4	0.2	0.2	1
5	0.2	0.2	2
6	0.2	0.2	3
7	0.3	0.3	1
8	0.3	0.3	2
9	0.3	0.3	3
10	1	1	1
11	0.3	0.3	3

3.6 Results and Discussion

A steady state thermal analysis is performed using ANSYS. As shown in Table 3.3, the DOE consists of 11 scenarios. The top package consists of two memory dice stacked on each other.

The power for memory dice varies from 0.1 W to 0.3 W in steps of 0.1 W. The bottom package consists of a logic die (flip chip). The power for the logic die varies from 1 W to 3 W in steps of 1 W. The top package is mounted on the bottom packages via BGA solder balls. These solder balls also serve as electrical and thermal interconnects. For each case, maximum temperatures for both the top and bottom packages are noted. Table 3.4 summarizes the results for all the scenarios in Table 3.3.

Table 3.4 Maximum temperature noted on logic and memory dice

Scenarios	Power Cases [W]	T_{max} in bottom package [°C]	T_{max} in top package [°C]
1	0.1, 0.1, 1	68.6	52.9
2	0.1, 0.1, 2	112.9	73.7
3	0.1, 0.1, 3	157.3	94.7
4	0.2, 0.2, 1	72.2	64.9
5	0.2, 0.2, 2	117.1	85.8
6	0.2, 0.2, 3	161.5	106.7
7	0.3, 0.3, 1	76.9	76.8
8	0.3, 0.3, 2	121.8	97.8
9	0.3, 0.3, 3	165.6	118.7
10	1, 1, 1	106.3	160.6
11	0.3, 0.3, 3	100.8	89

Maximum temperature of 165.6°C was noted for scenario 9 in which the bottom package dissipated 3 W and top package dissipated 0.6 W (0.3 W per die). Minimum temperature of 52.9°C was noted for scenario 1 in which the bottom package dissipated 1 W and top package dissipated 0.2 W (0.1 W per die). Figure 3.16 shows the temperature contours for first 9 scenarios.

For all the scenarios (except 10) higher temperatures were noted for the bottom package than the top package. Also, for the bottom package it can be seen that, for each Watt rise in power, temperature increases sharply by 45℃. However, for the top package, for each 0.1 W rise in power, temperature increases merely by 4℃. This can be attributed to the fact that the power on the bottom package is greater by an order of magnitude than the power on the top package. It is also observed that for the top package, heat is dissipated partly through the mold and partly through the BGA interconnects. For the bottom package, all of the heat is conducted through the solder balls (C4 interconnects) underneath and eventually to the PCB via C5 interconnects. Thus, maximum PoP temperature is dominated by the power on the bottom package. This can be clearly noted from Fig. 3.15 were change in memory die power (for the same logic die power) does not significantly alter the thermal performance whereas change in logic die power (for the same memory die power) significantly alters the thermal performance.

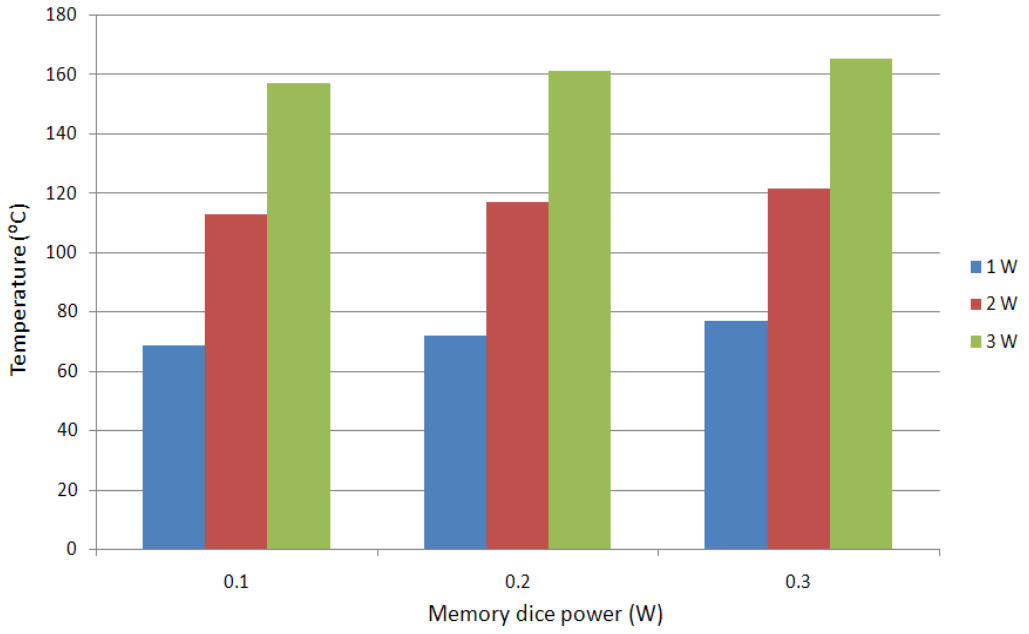
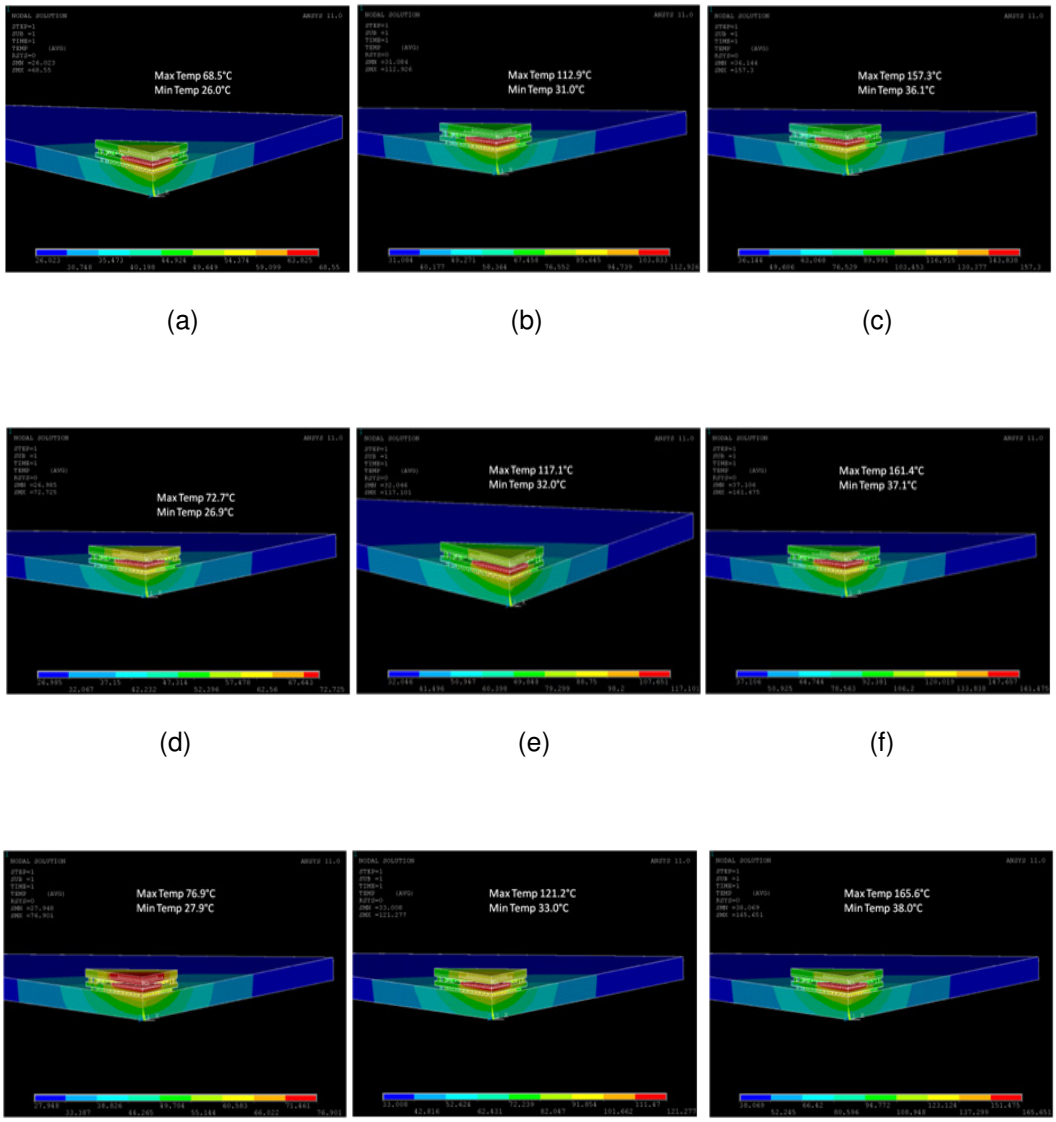


Figure 3.15 Temperature variations for various power combinations of logic and memory dice



(a) (b) (c)

(d) (e) (f)

(g) (h) (i)

Figure 3.16 Temperature contours for the scenarios (a) Power 0.1, 0.1 and 1W; (b) Power 0.1, 0.1 and 2W; (c) Power 0.1, 0.1 and 3W; (d) Power 0.2, 0.2 and 1W; (e) Power 0.2, 0.2 and 2W; (f) Power 0.2, 0.2 and 3W; (g) Power 0.3, 0.3 and 1W; (h) Power 0.3, 0.3 and 2W; (i) Power 0.3, 0.3 and 3W

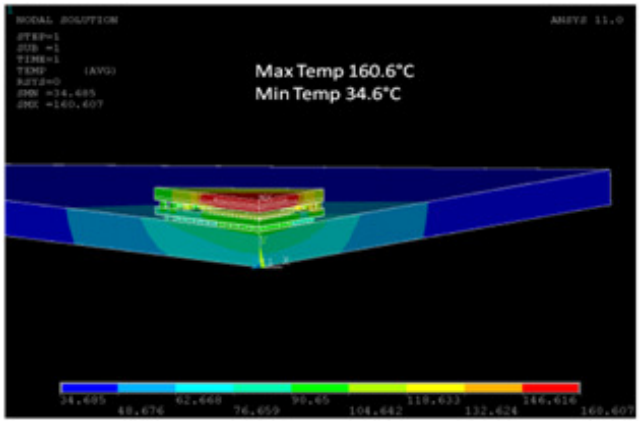


Figure 3.17 Temperature contours for scenario 10 (1 W each)

The aforementioned fact is valid only when the bottom package dissipates higher power than the top package. When the power on both the packages is comparable as in scenario 10, then the maximum PoP temperature is dominated by the die power in top package. In this case, maximum temperature is noted for the top package. This can be clearly observed in Fig. 3.17.

In this case, heat from the top package is primarily conducted through BGA interconnects due to poor thermal conductivity of the molding compound. As a result, the heat from the memory dice encounters very high thermal resistance due to which the temperature of top package increases.

In order to better understand the phenomenon, heat dissipation on individual surfaces for all the scenarios were itemized. Table 3.5 shows the itemized heat distribution. It was noted that for all the cases (except 11), approximately 92% of heat is dissipated through PCB while approximately 5% of heat dissipates through the mold cap. Remaining 2% of heat dissipates through package sides. This shows that the BGA interconnects play a vital role in conducting heat from the top package to the bottom package. It is also observed that, for all scenarios, the minimum temperature is observed on the PCB which can be attributed to its large area available for heat transfer.

For high power devices to be used for PoP architecture, first and foremost forced convection will be required. Also, the path of least resistance is through the BGA, C4 and C5 interconnects

(as the thermal conductivity of the molding compound is extremely poor), a method through which heat can be effectively conducted to the surface of the molding cap needs to be developed. As mentioned earlier almost 92% of the heat is dissipated through PCB. For the current architecture, one of the effective way for better thermal management is to use high conducting PCB. From Table 3.4 it can be observed that with use of high conducting PCB, significant drop in temperature for both the packages is noted. Under similar conditions (scenarios 9 and 11), temperature of bottom package drops by 64.8℃ (from 165.6℃ to 100.8℃) while temperature of top package drops by 29.7℃ (from 118.7℃ to 89℃). The temperature contour for scenario 10 is shown in Fig. 3.18.

Table 3.5 Itemized power distribution for first 9 scenarios

Power Cases	Mold Cap [W]		Mold Cap side [W]		Top Substrate Side [W]		Bottom Substrate Side [W]		PCB Top [W]		PCB Bottom [W]	
	Actual Power	% Total Power	Actual Power	% Total Power	Actual Power	% Total Power	Actual Power	% Total Power	Actual Power	% Total Power	Actual Power	% Total Power
0.1,0.1,1	0.065	5.435	0.009	0.82	0.014	1.168	0.008	0.725	0.732	61.000	0.37	31.230
0.1,0.1,2	0.108	4.916	0.016	0.744	0.025	1.156	0.027	1.253	1.4	63.636	0.622	28.273
0.1,0.1,3	0.114	3.583	0.023	0.715	0.029	0.911	0.046	1.449	2.05	64.063	0.93	29.063
0.2,0.2,1	0.087	6.249	0.013	0.941	0.017	1.187	0.001	0.1	0.84	60.000	0.44	31.429
0.2,0.2,2	0.13	5.435	0.019	0.824	0.028	1.167	0.017	0.727	1.5	62.500	0.71	29.583
0.2,0.2,3	0.173	5.099	0.026	0.772	0.039	1.16	0.026	0.778	2.152	63.294	0.982	28.882
0.3,0.3,1	0.109	6.86	0.016	1.03	0.019	1.2	0.012	0.72	0.94	58.750	0.503	31.438
0.3,0.3,2	0.153	5.873	0.023	0.885	0.031	1.177	0.007	0.281	1.6	61.538	0.786	30.231
0.3,0.3,3	0.196	5.435	0.029	0.821	0.042	1.167	0.026	0.727	2.25	62.500	1.057	29.361
1, 1, 1	0.264	8.8	0.03	1	0.021	0.7	0.1824	6.08	1.6	53.333	0.902	30.067
0.3,0.3,3	0.139	3.876	0.06	1.677	0.001	0.014	0.152	4.21	2.97	82.500	0.457	12.694

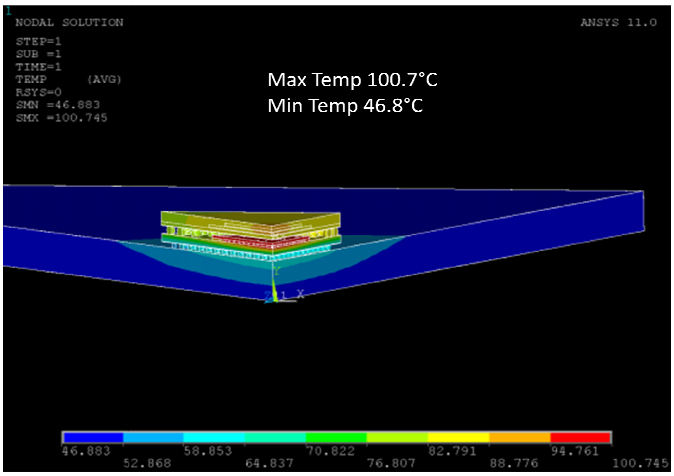


Figure 3.18 Temperature contour for scenario 11 with high thermal conductivity

3.7 Summary

In this chapter, thermal characterization of PoP was performed. Effect of die power on logic and memory dies was analyzed. Also, effect of highly conductive PCB and substrate was studied. For PoP, maximum temperature is always noted on the bottom package (logic die). For the highest power distribution case, the junction temperature far exceeded the design requirement. As 92% of the heat is dissipated through PCB, one potential solution is to use high thermal conductivity PCB. As demonstrated in Case 11, the impact of using high thermal conductivity on the PCB is significant as seen by the huge reduction in junction temperature. Case 10 clearly demonstrates when the power on memory die is of the same order as that of the logic die, maximum temperature may be noted in the top package. In this scenario, it may necessitate to use alternative packaging techniques such as the use of TSVs or use micro channel cooling.

The only path through which heat form the packages is conducted to PCB is through C4, C5 and BGA solder bumps. Thus these solder bumps serve as electrical as well as thermal interconnects. Solder interconnects are considered to be the weak link in a BGA structure. Excessive temperatures at the solder ball severely affect the thermo-mechanical reliability of

solders. High temperature coupled with higher operating current, these bumps may be subjected to a catastrophic failure known as electromigration. As we march forward on the roadmap, electromigration would be one of the other challenge that needs to be addressed. Hence, for better thermal management of not only PoP but all the devices, design guidelines in order to reduce bump electromigration must be developed. These guidelines and the necessity of such guidelines are further discussed in detail in the following chapter.

CHAPTER 4

BUMP ELECTROMIGRATION AND BACK END DESIGN RULES

4.1 Introduction

Since the invention of a transistor in 1947 and development of integrated circuits (ICs) in 1959, there has been a revolutionary breakthrough in the field of micro-electronics and its packaging. As per the Moore's law, the number of transistors per unit area has been doubling every 24 months [44]. The industry has followed the trend and most recently the number of transistors on Intel Itanium chip has exceeded a billion transistors.

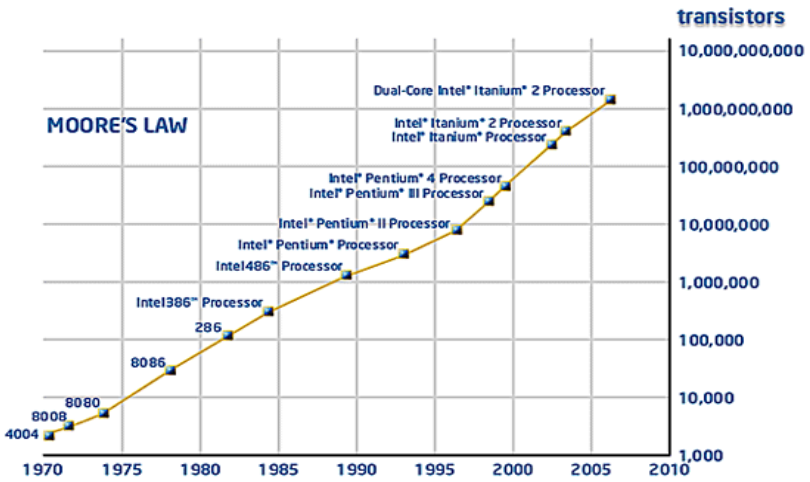


Figure 4.1 Moore's Law [44]

As the microelectronics industry followed Moore's law, different packaging technologies evolved. Initially, during 1960s flat pack and dual in line packages were popular but due to increasing demand of I/O later in 1970s and 1980s small outline transistors (SOT) and small outline IC (SOIC) were developed. However, thr goal of the micro-electronics industry has always been not only to increase the number of I/O but also package them as closely as

possible. Packaging the I/O closely reduces the circuit length and also results in die with smaller foot-print. As a result, in 1990 different packaging technologies such as quad flatpacks (QFP) and pin grid array (PGA) primarily while ball grid array (BGA) dominantly emerged. Later, chip scale packages (CSP) became a popular choice for industry as they had small die size and high I/Os compared to other packages. CSP is typically a flip chip, in which solder bumps serve as first level as well as second level interconnects. These solder bumps can be arranged in various configurations such as uniformly over the entire area (area array), staggered array or around the periphery of the die. As a result they are used in variety of applications such as cell phones, hand held electronics, workstations etc. Figure 4.2 shows a cross-sectional view of a flip chip.

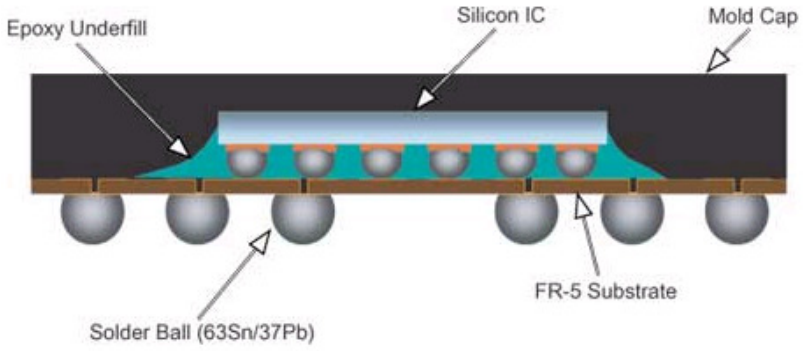


Figure 4.2 Cross-sectional view of a flip chip [45]

In today's world, packages have to be designed to withstand harsh environments. Due to increased functionality of electronic devices, packages have to be designed not only for high temperatures, mechanical vibrations, moisture etc but also for high current. Because of these high currents, solder bumps become a victim of catastrophic failure known as electromigration. Because of electromigration, initially voids are formed and eventually it results in an electrical open leading to device failure. This has added another variable in design for reliability. In this study, aim is to develop a clear guideline for design engineers in order to prevent or reduce the device failure due to electromigration.

4.2 Electromigration

Electromigration is defined as a mass transport phenomenon due to momentum transfer between conducting electrons and diffusing metal atoms [46]. Electromigration was first reported by a French scientist Geradin [46] in 1861. In 1967, James Black [47] in his pioneering work mentioned that electromigration largely depends on temperature and current density. He also explained the effect of grain size and formation of voids and hillocks. He proposed an equation, which is now known as Black's equation to determine mean time to failure (MTTF) for a device due to electromigration. Since then there has been numerous published studies on electromigration.

Electromigration in its simplest form is defined as transport of mass in metals when they are stressed at high current densities [48]. This mass transport is a result of two forces acting on metal atom. One force is due to interaction between positive metal ions and the electric field. This force is known as direct force. The second force is caused by momentum transfer between electrons and metal ions. This second force is known as wind force. Depending upon the magnitudes of these two forces, the metal atoms move either in the direction of current (in case of Al) or in the opposite direction.

4.3 Electromigration: A concern

According to Black's equation [47], the mean time to fail (MTTF) is given by,

$$MTTF = Aj^{-n}e^{-\frac{Q}{kT}} \tag{4.1}$$

where 'A' is constant based on the conductor length and width, 'j' is the current density, 'Q' is the activation energy, 'k' is the Boltzmann constant, 'T' is the temperature of the interconnect and 'n' is a constant. Based on equation 4.1, it can be said that the failure rate exponentially depends on temperature and has power dependence on current density. Thus for any electromigration related problem, parameters of concern are current density (which is the ratio of current to cross-sectional area perpendicular to the direction of current) and temperature. Zhao [49] describes electromigration in interconnects as self-accelerated thermal

runaway process. He mentions that, at early stage of electromigration, voids or cracks in the metallization are small when compared to the line width. As the crack propagates, cross-sectional area decreases causing local increase in current density. This phenomenon is known as current crowding, which in turn results in temperature rise due to Joule heating. The elevated temperature accelerates the growth of cracks due to its exponential dependence which in turn further increases the current crowding effect, eventually leading to catastrophic failure. This process is summarized in Fig. 4.3.

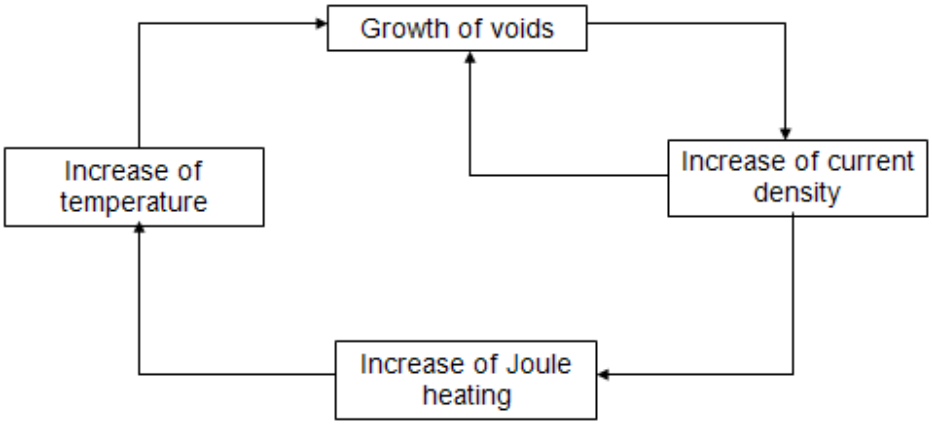


Figure 4.3 Thermal acceleration loop of Electromigration [49]

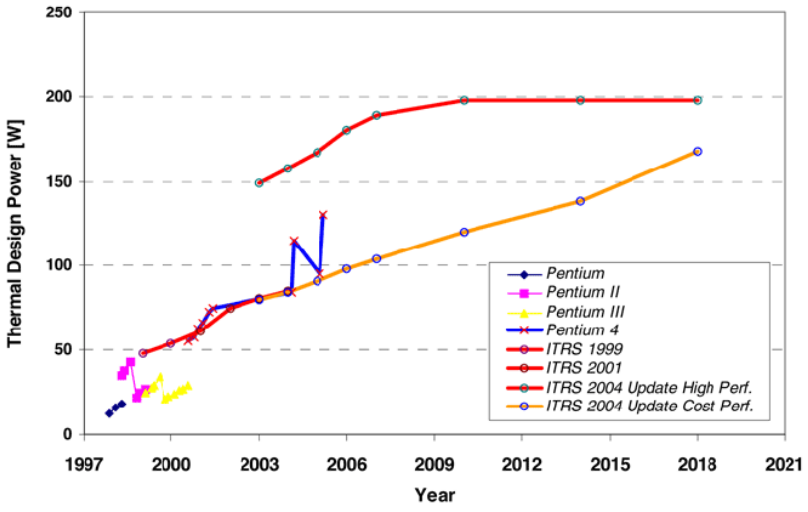


Figure 4.4 ITRS roadmap for power [50]

As published in ITRS roadmap [50], microelectronics transistor count has increased from 5000 to 42,000,000 while increase in die area is only 7%. In addition, frequency has doubled every two years. As a result, the number of active devices on the chip is adding resulting in increased die power. Figure 4.4 shows the present and the future power trend for high performance systems which requires higher number of I/O's. In response to this demand, along with the miniaturization of devices, flip chip technology has now become a popular choice of packaging industry. In flip-chip, electronic circuits on the die are connected to the module and/or board via the solders balls. Depending upon the requirements, solder balls are either placed on the periphery or spread over the entire area. Due to continuous demand for miniaturization, today pitch as less as 50 microns is used. Figure 4.5 depicts the commonly used pitch between the solder balls.

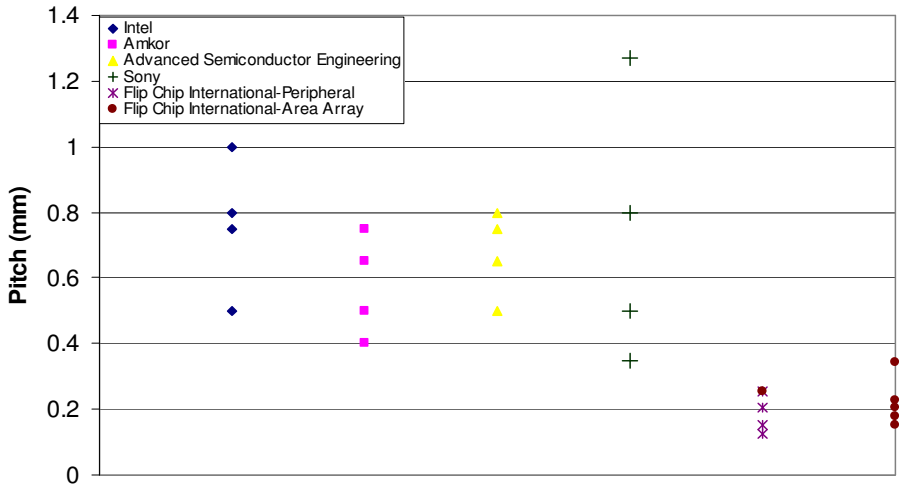


Figure 4.5 Flip chip packages with different solder pitch for different industries [51-54]

With technology, device functionality has also increased. For example, compare the communication devices used in early days to that of today's devices. Apart from communication they can be used as a personal organizer, calculator, music player etc. Improved functionality requires more current to be passed through the interconnects and the solder bumps. Figure 4.6

shows the increase in current requirements for the microprocessors by Intel [55]. Also, decreasing the device dimensions, demands thinner line width of the interconnects. This increases the current density in interconnects. Electromigration thus become a reliability concern in signal traces as well as in the flip-chip solder joints.

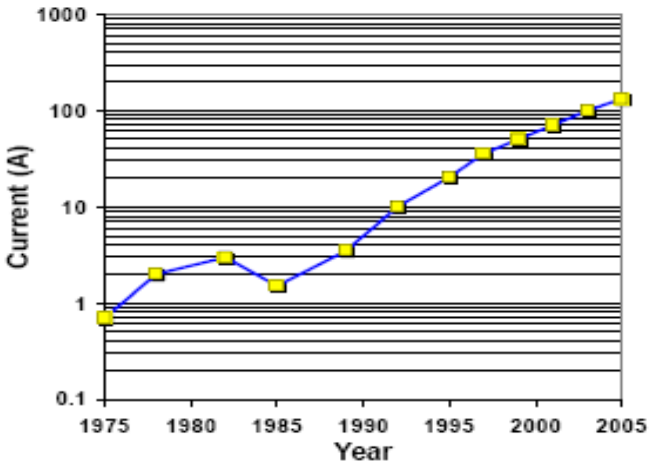
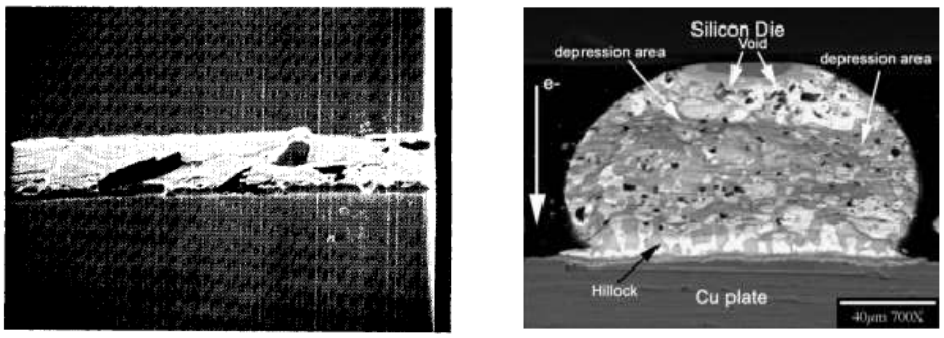


Figure 4.6 Current requirements for Intel's microprocessors [55]

A flip chip package typically fails at the Al and/or Cu metallization and at the interface of under bump metallurgy (UBM) and solder ball. Figure 4.7 shows the occurrence of failure (formation of voids) due to electromigration at the above mentioned locations.



(a) (b)

Figure 4.7 Formation of voids due to electromigration in an microelectronic device (a) Voids observed in metallization [48] and (b) Voids observed in solder [56]

For electromigration, maximum permissible current is 0.2 A/bump [57]. For this input current and for a solder bump of 50 μm in diameter, current density in the metallization will be of an order $3x10^3$ A/cm^2 while in solder bump it will be of an order $1x10^4$ A/cm^2 [57]. Even though current density in solder bump is less than that in metallization, it is still a reliability concern for the following reasons [57]:

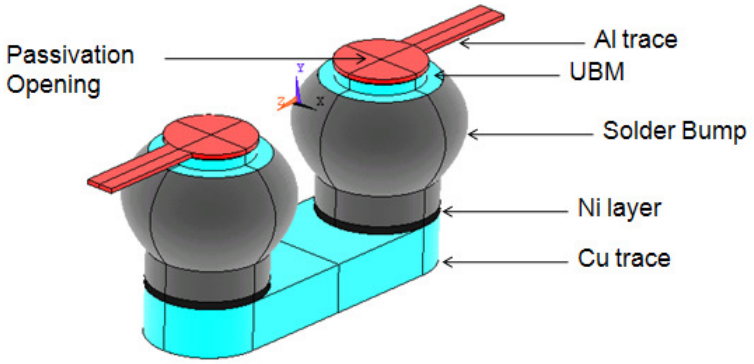
1. Rate of electromigration near room temperature is high due to low melting point and high diffusivity of solder alloys.
2. The difference in geometry of the interconnect line and the solder bump results in a very large change in current density. As a result current crowding is observed at the junction of UBM and solder.
3. Electromigration can result in a very large compositional redistribution of solder alloys.
4. Noble and near noble metal alloys are used as UBMs in solder joints which diffuses very rapidly in solder alloys.
5. Intermetallics are formed at the edge of UBM and solder.

4.4 Bump Terminologies

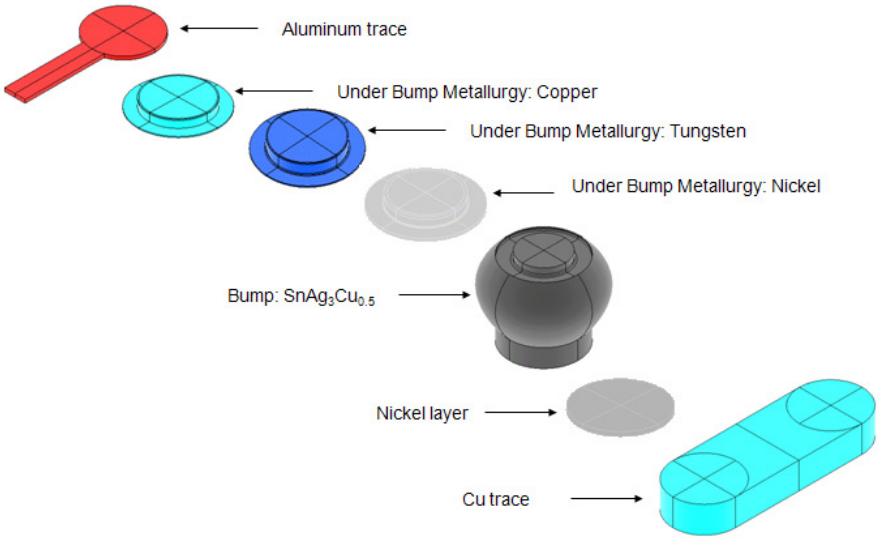
A flip chip solder bump consists of die side trace, voltage pad, under bump metallurgy (UBM), passivation layer/opening, solder ball, Ni/Au barrier layer and substrate side trace. Figure 4.8 (a) is a schematic representation of the solder bump showing different components. Figure 4.8 (b) is the exploded view of the solder bump showing three layers of UBM. Each parameter is explained below:

a. Die side trace: It is the metallization on the Si die which forms the circuitry and is the primary path for current. It is also referred to as metallization or Al trace in the current study.
b. Voltage pad: Metal area on the die that the bump or wire is attached to.
c. UBM: It is the stack of metal layers (typically 3 layers) that is deposited under the bump during the solder bumping process. Its function is to serve as adhesion layer, diffusion

barrier, wetting layer and protect from oxidation. Commonly adopted combinations of for UBM are NiV/Cu, Al/NiV/Cu, or Al/NiV/Cu/Ti/NiV/Cu.



(a)



(b)

Figure 4.8 Schematic representation of solder bump configuration (a) Flip chip solder bump configuration (b) Exploded view to show UBM configuration

d. Passivation layer: It is used for circuit protection. It is deposited on the metallization and part of voltage pad. The uncovered part of the voltage pad is known as passivation

opening. Nitride, Polyimide, Oxide, or Oxi-Nitride are typically used as passivation materials.

e. Solder ball: It is a metal alloy which serves as an electrical connection between die and substrate.

f. Ni/Au layer: It serves as a barrier layer between solder ball and substrate side trace.

g. Substrate side trace: It is a metallization which forms the circuitry on the substrate.

4.5 Literature Study

Since the early work by Black [47], many studies have been published on electromigration. Till date, detailed investigations on the various failure mechanisms of electromigration have been presented [47, 57, 58].

As mentioned earlier, one of the factors responsible for electromigration is current density which depends on the trace width. More the trace width better will be the resistance to electromigration. However, Argarwala *et al.* [59] and Cho *et al.* [60] in their work showed that dependence of the electromigration lifetime on the line width is complex. If the line width is reduced to the average grain size of the wire, then the resistance to electromigration increases despite an increase in current density. This is because at that particular line width, grain boundaries are perpendicular to the width of the wire and form a bamboo like structure. The variation in MTTF with the line width is shown in Fig. 4.9.

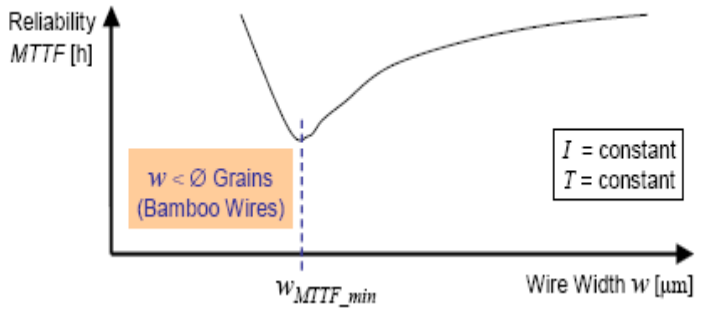


Figure 4.9 Dependence of MTTF due to electromigration on line width [61]

The electromigration lifetime also depends upon the line length. Lines shorter than a particular length do not exhibit failure due to electromigration [61]. This length is known as Blech's length. Within this length the critical stress required to form a void is never reached and hence no failure due to electromigration is observed. Thus, along with current density and temperature (Black's law) stress in the interconnect also plays a critical role.

Other studies [62-76] include location of failure in flip chip solder bump, effect of different parameters such as trace materials, UBM configuration, different solder configurations etc.

Some researchers claim that voids are created only on the die side [63, 65-67], while others reported formation of the voids on both sides [68, 69]. For example, Shao *et al.* [65] observed failure on the die side in Sn3.5Ag solder bumps with Cu/CrCu/Ti UBM. Lin *et al.* [67] reported that voids are formed only on the die side irrespective of the direction of current flow in Sn3Ag0.5Cu solder bumps with Al/Ni(V)/Cu UBM. Chae *et al.* [66] studied the effect of electromigration on Sn3.5Ag solder bumps for nickel and copper UBMs, and reported that failure was observed only on the die side. Similar to [62, 66], Lai *et al.* [68] also showed that voids are formed around the UBM and crack may initiate around the current crowding region, which is at the die side. On the other hand, Wu *et al.* [69] and Ye *et al.* [70] reported failures on both sides.

Yiping *et al.* [71] studied the effect of different Ni/Au UBM thickness on electromigration in Sn/3.5Ag/0.5Cu solder bumps. UBM consisted of electroplated nickel (5/10 µm) on copper as diffusion barrier layer and gold (0.1 µm) on the surface as an anti-oxidization layer and concluded that MTTF for UBM with 10 µm thickness is longer than that of UBM with 5 µm thickness.

Ebersberger *et al.* [64] reported that electroplated SnAg solder bumps with thick UBM on CuOSP substrates show excellent reliability during high temperature storage (HTS) and high current stressing (HCS) tests.

Su *et al.* [72] tested Sn10Pb90 (high lead) and Sn96.5Ag3.5 (Pb-free) solders with TiW/Cu and Ti/Cu/Ni UBM under 3.5-4.1 x 10^4 A/cm^2 current density. Current density was calculated as a ratio of applied current (0.85 - 1 A) to the area of via opening (2.42x10^{-5} cm^2). They concluded that electromigration performance can be increased by increasing the UBM thickness or reducing the current crowding near the UBM .

Liang *et al.* [73] studied effect of 5 µm, 10 µm and 20 µm thick copper UBM on the current density distribution for the Sn63Pb37 solder joint. They used 3D Finite Element Analysis (FEA) for their analysis. Based on their modeling results, they concluded that solder joints with thicker Cu UBM has lower maximum current density inside the solder since the current spreads out more uniformly in the solder joints with thicker copper UBM.

Chieu *et al.* [74] studied the effect of joule heating through 3D FEA for SnAg3.5 solder and noted the existence of hot spots near the entrance points in aluminum trace.

Nah J-W *et al.* [75] considered SnPb and SnAg solder with copper column and concluded that copper column increased the electromigration resistance by decreasing the current crowding in the solder and that the copper column bump with SnPb eutectic has lower reliability.

Lai *et al.* [68] tested 96.5Sn3Ag0.5Cu solder with T/Ni(V)/Cu UBM on copper and Au/Ni/Cu substrate surface finish and reported that copper surface finish offers better electromigration resistance than the Au/Ni/Cu one, although more voids are created in copper metallization. In their study, they applied a constant electric current of 0.32 A, which resulted in an average current density of about 5,000 A/cm2, considering the area of passivation opening to be 90 μm^2 as a reference.

The current guidelines available for design engineers are based on the simple rule that the maximum current density in any trace should not exceed the permissible limit. If the current density exceeds, the engineer has to redesign the circuit. This approach designs for the worst case scenario and eventually results in over designing. In order to prevent electromigration in metal traces following conditions need to be satisfied [76]:

$$i_{dc} < I_{dc} \tag{4.2}$$

$$i_{rms} < I_{rms} \tag{4.3}$$

$$i_{peak} < I_{peak} \tag{4.4}$$

In the above equations, '*i*' is the current and subscripts dc, rms and peak denotes the average DC current, RMS current and peak current respectively. These current values depend on switching factor, switching time T_0 and the current waveform *i(t)*. Their correlation is as mentioned below.

$$i_{dc} = \frac{s}{T_0}\int_0^{T_0} i(t)dt \tag{4.5}$$

$$i_{rms} = \sqrt{\frac{S}{T_0}\int_0^{T_0} i^2(t)dt} \tag{4.6}$$

$$i_{peak} = \max\left[\left|i(t)\right|\right] \tag{4.7}$$

I_{dc}, I_{rms} and I_{peak} values depend on the trace width and the metallization layers.

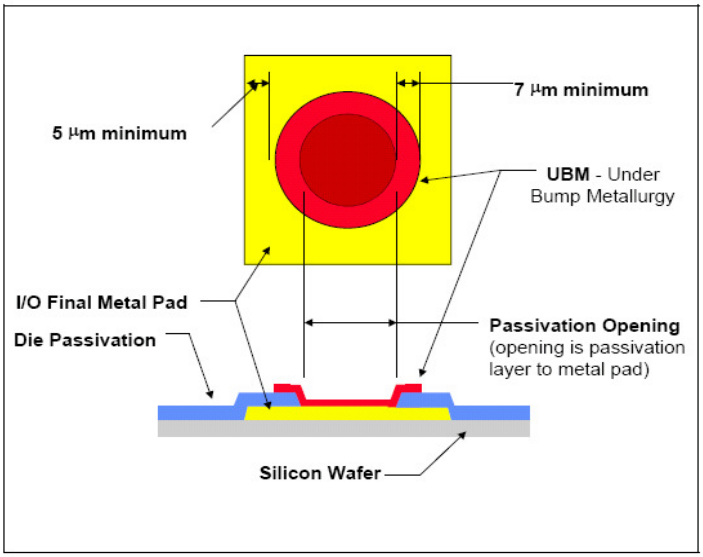


Figure 4.10 Golden rule of flip chip [77]

The only guideline available for solder bumps is the one available from foundry which is known as golden rule of flip chip [77]. According to this guideline, the UBM must overlap the I/O

passivation opening by at least 7μm and the I/O final metal pad must extend at least 5μm past the end of the UBM as shown if Fig. 4.10. In order to determine MTTF for the solder bump, Black's equation is used. Experiments are performed at accelerated test conditions (current and temperature) in order to determine the constants A, n and Q (refer equation 4.1). This process is very time consuming and can only be performed after fabrication. New guidelines need to be developed which can help engineers to implement design for reliability during designing phase itself. The guidelines should be based on current density in metal trace as well as in the solder bump. To summarize, there is a need for some standards as:

1. Failure of solder bump due to electromigration is very complex phenomenon.
2. Reliability of solder bumps based on high current and high temperature is difficult to determine as it varies significantly with the bump configuration.
3. Accelerated testing is very time consuming and hence could be limited.
4. Determining permissible current from the test data is highly arbitrary.
5. Different vendors have different set of foundry rules to fabricate solder bumps. Hence test results cannot be compared to predict resistance to electromigration for the same.

The literature survey revealed that very few agreements exist despite the increasing number of papers on the topic. The most common conclusions were on the inferior resistance of eutectic SnPb solder, the positive effect of thick UBM. In so many years of study, many different techniques have been proposed and demonstrated to minimize damage due to electromigration but none of them is capable for generalized use in production environment. This might be because electromigration phenomenon is dependent on various parameters such as bump/trace composition, structure, geometry, deposition, electrical and mechanical stressing and many more. It can be seen that most of the research addresses the metallurgical aspects of electromigration.

It was observed that most of the researchers have studied effect of different bump parameters on electromigration independently. However, all the parameters play a significant role in determining the MTTF due to electromigration, and their combined effect should be considered. In this work, combined effect of four different parameters on current density is evaluated using commercially available finite element code. Four parameters are passivation opening, trace width, UBM size and UBM thickness.

4.6 Numerical Modeling

Numerical analysis was performed using ANSYS [78]. Figure 4.11 shows the schematic of the solder bump pair considered for analysis. The metal traces on the chip side and substrate side are considered to be made up of Al and Cu respectively. The UBM is comprised of Cu, Ni and Ti metal layers. Thickness of Cu, Ni and Ti metal layers is defined as percentage of total UBM thickness. It was 26%, 20% and 54% respectively. The solder bump configuration considered is SnAg3Cu0.5. A thin layer of Ni which acts as a barrier layer for electromigration is considered between the bump and the Cu trace.

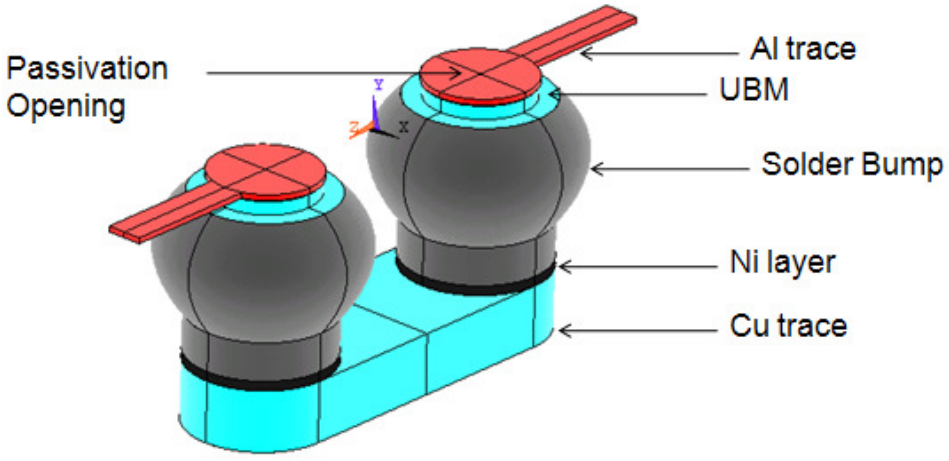


Figure 4.11 Schematic representation of solder bump

Thickness of the passivation layer, Ni layer, Al trace and Cu trace was kept constant for all the cases. The dimensions were 8 µm, 5 µm, 2 µm and 32 µm respectively. Dimensions of all other parameters are shown in Fig. 4.12.

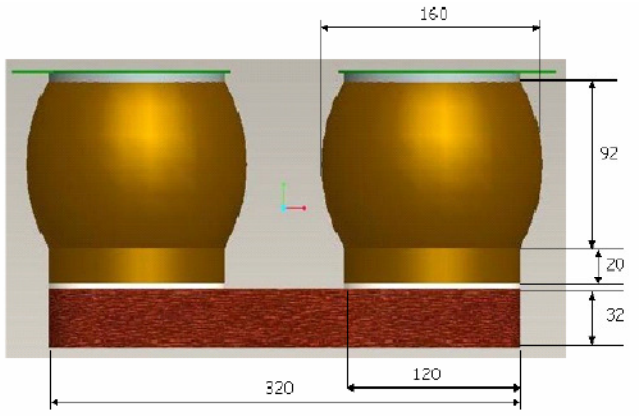


Figure 4.12 Dimensions of each parameter considered for analysis

SOLID 69 element was considered owing to its ability to do electro-thermal coupled analysis. The coupled problem assumes a steady state heat distribution and is governed by the standard heat flow equation as shown by equation 4.8.

$$\nabla.(k\nabla T) + Q = 0 \tag{4.8}$$

In the above equation, 'k' is the thermal conductivity, 'Q' is the heat generated per volume and 'T' is the temperature. 'Q' is also known as the source term which is a result of Joule heating due to passage of current and is given by equation 4.9.

$$Q = \sigma(\nabla\varphi)^2 = \sigma j^2 \tag{4.9}$$

In the above equation, 'σ' is the electrical resistivity of the material, 'φ' is the electric potential and 'j' is the current density. The electric potential 'φ' is governed by equation 4.10 which is very similar to equation 4.8.

$$\nabla.(\sigma\nabla\varphi) = 0 \tag{4.10}$$

The model was meshed in order to generate approximately 122,000 elements. Four parameters of the back end design rules, each with two values are studied. These attributes and their ranges are:

- PO diameter with 60 and 100 µm
- UBM diameter with 120 and 160 µm
- UBM thickness with 2 and 7 µm, and
- Al trace width with 10 and 60 µm.

Based on the above parameters, a full factorial design of experiments (DOE) was employed to study their effect on current density in the solder bump. Table 4.1 shows the DOE for the current analysis. Material properties for all the components of solder bump are as shown in Table 4.2.

Table 4.1 Design of experiments to study impact of back end design parameters on current density in solder bump

Leg	PO diameter (µm)	UBM diameter (µm)	UBM thickness (µm)	Al Trace width (µm)
1	60	120	2	10
2	60	120	2	60
3	60	120	7	10
4	60	120	7	60
5	60	160	2	10
6	60	160	2	60
7	60	160	7	10
8	60	160	7	60
9	100	120	2	10
10	100	120	2	60
11	100	120	7	10
12	100	120	7	60
13	100	160	2	10
14	100	160	2	60
15	100	160	7	10
16	100	160	7	60

Table 4.2 Material properties considered for analysis [79]

Material	Electrical resistivity $x10^{-8}$ (Ω-m)	Thermal conductivity (W/m K)
Aluminum	2.7	210
Copper	1.7	385
SnAg3Cu0.5	12.1	57.26
Titanium	55.4	17
Nickel	6.4	60.7

4.7 Results and Discussion

Using the conditions of accelerated electromigration testing, analysis was performed for input currents of 0.1 A and 0.5 A. The current was defined on one of the Al trace while zero voltage was defined on the other Al trace. A constant temperature boundary condition was defined at the bottom of the Cu trace. Results are discussed below.

Figures 4.13 and 4.14 show the variability chart for maximum current density in the Al trace for an input current of 0.1 A and 0.5 A respectively. In Al trace, when the current was increased from 0.1 A to 0.5 A, the maximum current density also increased by a factor of five. Al trace width, PO diameter and UBM diameter were found to have significant contribution in deciding the current density in Al trace. However, the variation in current density with respect to UBM thickness was insignificant.

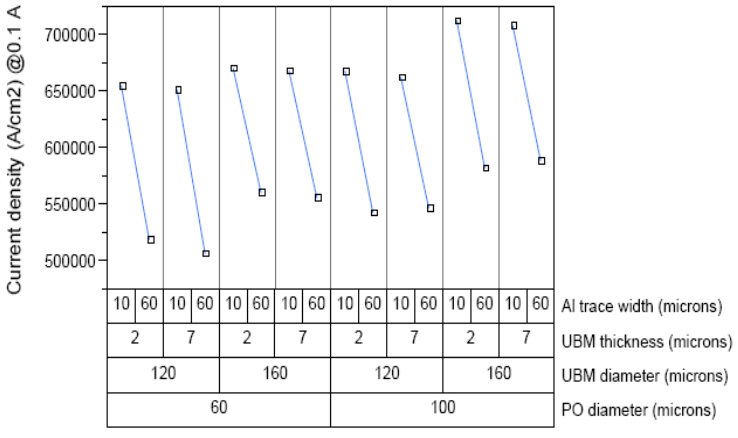


Figure 4.13 Variability chart for maximum current density at 0.1 A in Al trace width

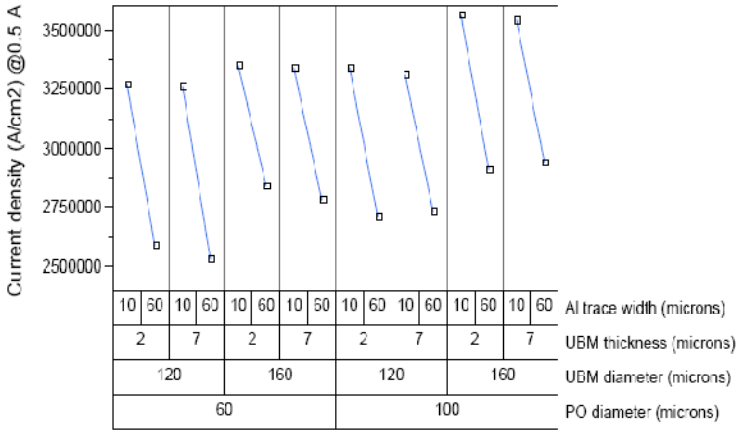


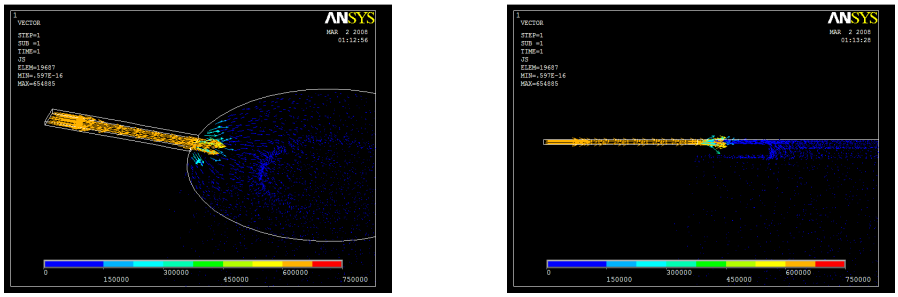
Figure 4.14 Variability chart for maximum current density at 0.5 A in Al trace width

Figure 4.15 shows that for narrow trace width, the current density is uniform in the Al trace. However, current density in the Al trace is approximately twice of that observed in the pads or UBM opening. Thus there is a very large change in current density at the junction of Al trace and the UBM. This sudden change results in current crowding which accelerates void formation and may reduce the life of the solder bump. This current crowding effect can be reduced by increasing the Al trace width. Thus, when the Al trace width is increased from 10 µm to 60 µm, there is a gradual change in current density at the interface of Al trace and UBM. This phenomenon is clearly observed in Fig. 4.16.

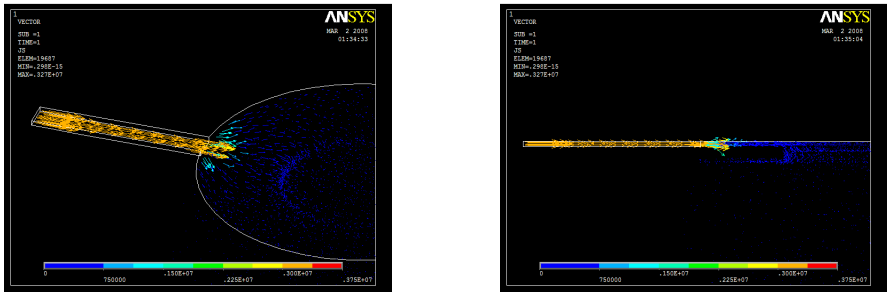
As mentioned earlier variation in current density is insignificant when the UBM thickness was changed from 2 µm to 7 µm, specially for small trace width. However, for large trace width, thick UBM (7 µm) has lower current densities than thin UBM (2 µm). This shows that UBM thickness has strong dependence on trace width. Wider trace width and thicker UBM together facilitate spreading of current in the UBM. This reduces the current crowding due to increased contact surface between the two.

For solder bumps with higher PO diameter (100 µm) and UBM diameter (160 µm), higher current density is observed when compared to other bump configurations. This is

because when the passivation opening is bigger and in this case is of the same size as that of voltage pad, the current directly passes into the UBM and does not spread in the pads as observed in other cases. This phenomenon can be clearly seen in figs. 4.17 and 4.18. Thus, smaller UBM diameter and PO diameter yields lower current density. Similar trends were observed for input current of 0.1 A and 0.5 A. Refer figs. 4.13 and 4.14. It is recommended to have larger PO diameter in order to reduce stress on the bump during fabrication and reflow process [60]. In later section of the chapter, effect of package attributes on the stress induced in the PO is studied. The results are then combined to develop guidelines for design engineer.

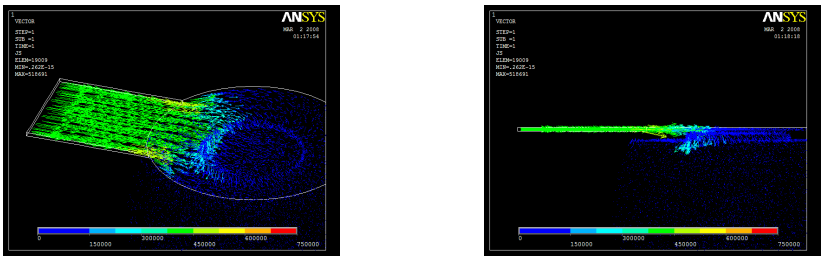


(a)

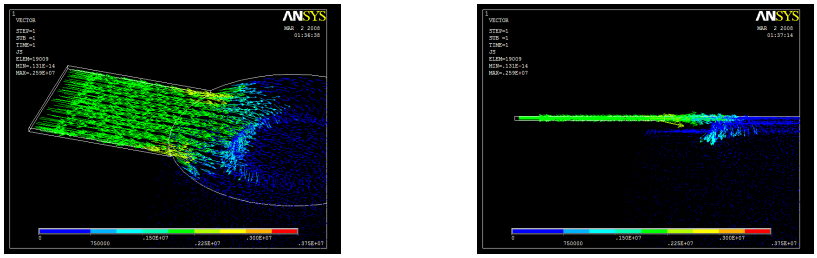


(b)

Figure 4.15 Vector plots of current density for leg 1 (a) 3D and 2D view of current density for input current of 0.1 A (b) 3D and 2D view of current density for input current of 0.5 A

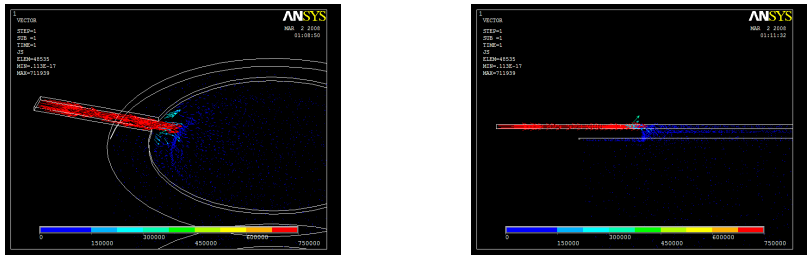


(a)

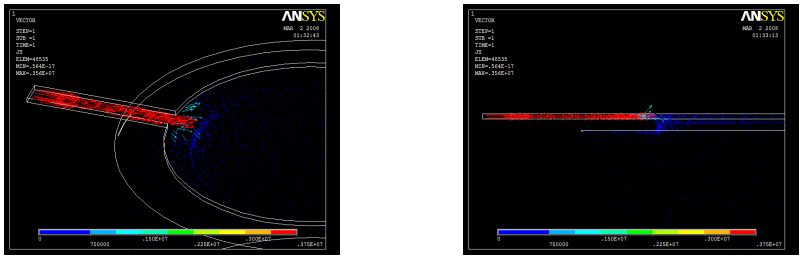


(b)

Figure 4.16 Vector plots of current density for leg 2 (a) 3D and 2D view of current density for input current of 0.1 A (b) 3D and 2D view of current density for input current of 0.5 A

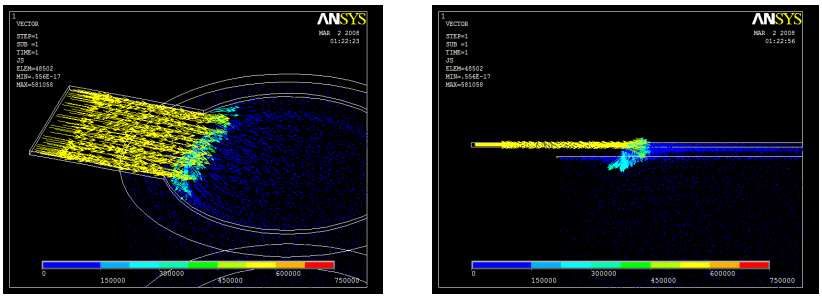


(a)

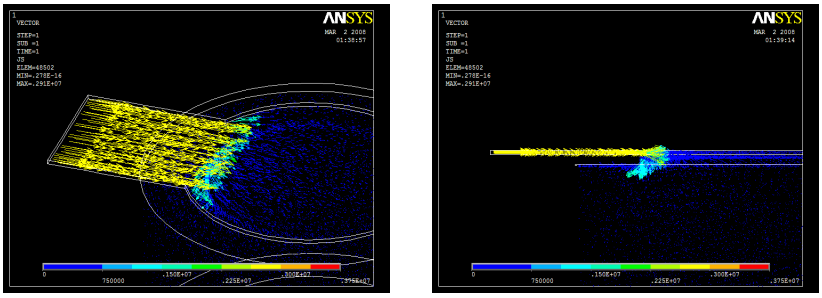


(b)

Figure 4.17 Vector plots of current density for leg 13 (a) 3D and 2D view of current density for input current of 0.1 A (b) 3D and 2D view of current density for input current of 0.5 A



(a)



(b)

Figure 4.18 Vector plots of current density for leg 14 (a) 3D and 2D view of current density for input current of 0.1 A (b) 3D and 2D view of current density for input current of 0.5 A

Figures 4.19 and 4.20 show the variability chart for maximum current density in the bump for an input current of 0.1 A and 0.5 A respectively. Similar to Al trace width, in case of bump, when the current was increased from 0.1 A to 0.5 A, the maximum current density also increased by a factor of five. However, current density in solder bump was noted to be significantly less than current density in Al trace. This is due to the large volume of the bump compared to that of Al trace. Al trace width and UBM thickness were found to have significant contribution in deciding the current density in the bump. Variation in current density with respect to PO diameter and UBM diameter was insignificant.

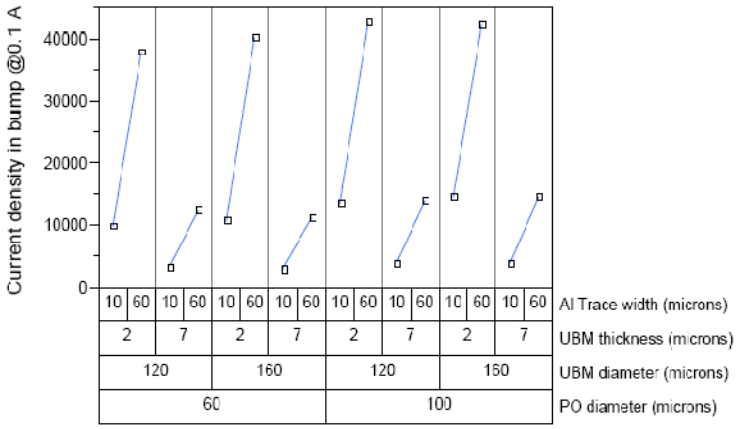


Figure 4.19 Variability chart for maximum current density in bump for input current of 0.1 A

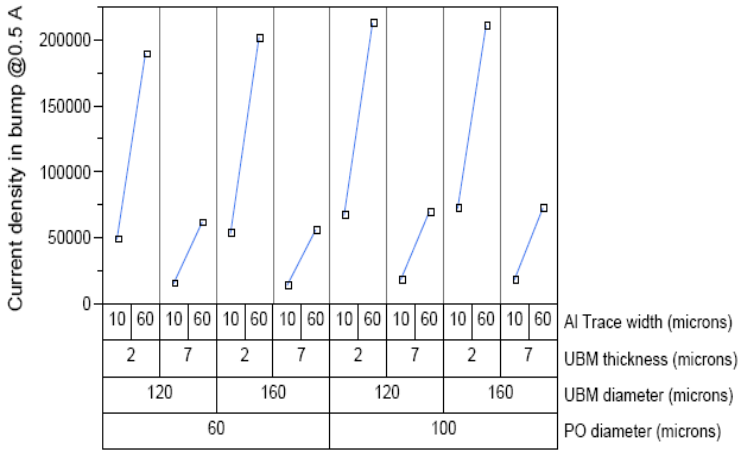


Figure 4.20 Variability chart for maximum current density in bump for input current of 0.5 A

Figures 4.19 and 4.20 show the effect of Al trace width on maximum current density in the bump. It is observed that current density in the bump increased with increase in Al trace width. This contradicts with the findings reported by Chiu *et al.* However, their conclusion was based on Joule heating effect in Al trace. In the present study, for wider Al trace, a zone of crowded current is observed in the solder. This can be clearly seen in Fig. 4.16 and 4.18.

Change in UBM thickness from 2 μm to 7 μm lowers the current density in the bump. This agrees with the result reported by Liang *et al.* [73] and Su *et al.* [72]. As mentioned earlier, variation in current density with respect to PO diameter and UBM diameter is insignificant. Similar trends were observed for input current of 0.1 A and 0.5 A. Refer figs. 4.19 and 4.20.

It has been stated that electromigration is also impacted by the stress present in the bump [64]. It is also known that the stress in the bump depends on its location in the bump array [65]. Thus, results shown above may be affected by the stress acting on the bump and hence it is necessary to consider effect of stress within the PO. This is further discussed in the following section.

4.8 Effect of Flip Chip Package Architecture on Stresses in the Bump

Electromigration in solder bumps depends on parameters like current density, temperature, material (per Black's equation), grain size and the stress in the bump. In section 4.7 of this chapter it was shown that the current densities in the bump and in the metallization are functions of PO size, UBM size, trace width and UBM thickness. It has also been stated that the electromigration may be impacted by the stress present in the bump at the PO [80-83]. Electromigration failure is essentially the erosion of UBM due to the current crowding. The stresses induced in the bump after the reflow process may accelerate this phenomenon and hence the conclusions drawn in the prior section needs to incorporate the same. The stress induced during reflow process depends on the package architecture and the material.

Kanatharana *et al.* [84] in their study evaluated the residual stress distribution in Si substrates due to the solder bump reflow using white beam synchrotron x-ray topography (WBSXRT) and compared this observed stress with finite element modeling (FEM). They concluded that the strain was particularly large near the peripheries of the bumps after the reflow process. A comparison of WBSXRT topographs and FEM models indicate similar strain distributions within the Si substrate.

Ren *et al.* [85] in their paper investigated the combination of electromigration effect and stress effect in lead free solder joints with a diameter of 300μm. They concluded that the longer electromigration time or higher current density reduced the tensile strength of the bump. They also reported the effect of the shear test on the metallurgical properties of the inter-metallic compounds.

In the paper by Biswas *et al.* [86], 1st level and 2nd level solder joint reliability analysis of a flip chip package was done emphasizing the effect of detailed substrate modeling and solder layout design. They concluded that fatigue life for board level solder bumps increases with the increase in the die thickness.

Koo *et al.* [87] in their paper discussed the interfacial reactions between the In-48Sn solders and electrolytic Au/Ni/Cu BGA substrates, and their effects on the shear properties of the solder joints in terms of various reflow temperatures and duration times.

Davoine *et al.* [88] studied the impact of pitch on residual stress and strain after the reflow. They concluded that the maximum stress was induced in the corner bump and the stress is inversely proportional to the pitch for constant bump diameter and stand-off height.

Lei *et al.* [89] studied the impact of pad size and the substrate thickness on second level interconnects and concluded that thicker substrate improves the reliability of second level interconnects. They also mentioned that the pad size is extremely crucial and sometimes thin substrate with large pad size can have better reliability than thick substrate and small pad size.

Several papers reported the effect of thermal cycling on creep and fatigue failure of solder bumps. After reviewing the literature, it can be seen that no clear guidelines exists to assist the design engineers in finalizing the back end design parameters based on the stress and electromigration that will minimize the device failure. Most literature report the stresses induced by electromigration but few have mentioned the effect of stress on electromigration. Thus, the design requirements to minimize the device failure both due to electromigration and stress, together and independently may be different.

In order to minimize the device failure due to bump electromigration, small PO size was recommended initially. In this section, additional DOEs were formed to demonstrate the stresses acting on the bump as a function of package architectural attributes. Package architectural attributes such as die thickness, die size, substrate thickness, substrate size and PO size are studied in detail and the results are then combined with previously reported design guidelines. A commercially available finite element analysis tool is used to evaluate stresses induced in the bump (at the PO) due to coefficient of thermal expansion (CTE) mismatch during the standard reflow process.

4.8.1 Numerical Modeling

The non-linear numerical analysis was performed using ANSYS [78]. Figure 4.21 shows a schematic representation of a package to show the section along which the slice model was considered for analysis. Slice model helps in reducing the mesh count and hence significantly reduces the solution time. The number of solder bumps in a slice model depends on the die size and the pitch of the solder bumps. Figure 4.22 shows the package configuration. The metal traces on the die side and the substrate side are considered to be made up of Al and Cu respectively. The solder is capped by Cu UBM. A thin layer of Ni which acts as a barrier layer for electromigration is considered between the bump and Cu trace.

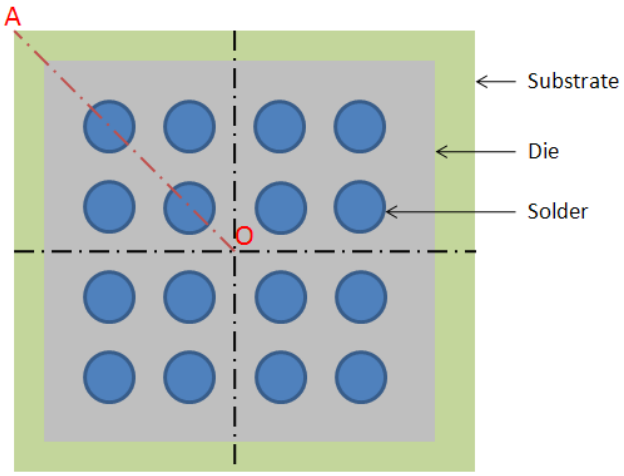


Figure 4.21 Schematic representation to show the section along which the slice model was considered.

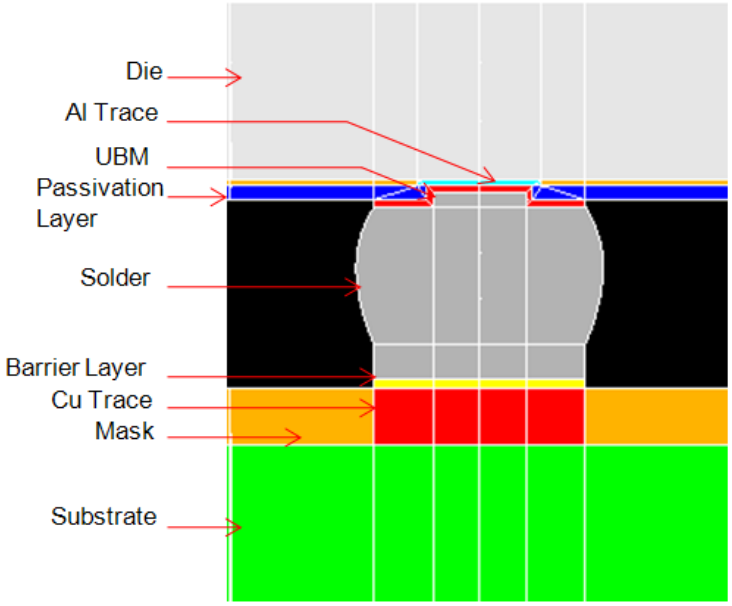


Figure 4.22 Package details showing different components

Bump pitch, bump diameter, thickness of passivation layer, Ni layer, UBM, substrate mask, Al trace and Cu trace are kept constant. The dimensions are 8 µm, 5 µm, 4 µm, 32 µm, 2 µm and 32 µm respectively.

SOLID 45 element was considered owing to its ability to do thermo-mechanical coupled analysis. The model was map meshed in order to generate approximately 100,000 elements. Five parameters of the back end design rules, each with two values were studied. These attributes and their values are

- PO diameter with 60 and 100 µm
- Die size with 6000 and 10,000 µm
- Die thickness with 100 and 800 µm
- Substrate size of 1.5 and 2 times the die size, and
- Substrate thickness with 600 and 1200 µm.

The full factorial DOE based on above parameters is shown in Table 4.3. The material properties considered for the analysis are as shown in Table 4.4.

Table 4.3 DOE to study effect of package architectural attributes on stress in the PO

DOE	Die thickness (µm)	Substrate thickness (µm)	Die size (µm)	Substrate size (µm)	PO size (µm)
1	100	600	6	9	60
2	100	600	6	9	100
3	100	600	6	12	60
4	100	600	6	12	100
5	100	600	10	9	60
6	100	600	10	9	100
7	100	600	10	12	60
8	100	600	10	12	100
9	100	1200	6	9	60
10	100	1200	6	9	100
11	100	1200	6	12	60
12	100	1200	6	12	100
13	100	1200	10	9	60
14	100	1200	10	9	100
15	100	1200	10	12	60
16	100	1200	10	12	100
17	800	600	6	9	60
18	800	600	6	9	100
19	800	600	6	12	60
20	800	600	6	12	100
21	800	600	10	9	60
22	800	600	10	9	100
23	800	600	10	12	60
24	800	600	10	12	100
25	800	1200	6	9	60
26	800	1200	6	9	100
27	800	1200	6	12	60
28	800	1200	6	12	100
29	800	1200	10	9	60
30	800	1200	10	9	100
31	800	1200	10	12	60
32	800	1200	10	12	100

Table 4.4 Material properties considered for analysis [79]

Material	Young's Modulus (GPa)	Poisson's Ratio	CTE (ppm/℃)
Silicon	162	0.28	2.6
Aluminum	70	0.35	22
Polyimide	3.2	0.34	3
Copper	128	0.34	16.5
Solder	57.26	0.35	25.5
Nickel	200	0.31	13.4
Substrate	15.3	0.28	12.4
Mask	6.9	0.35	19

The flip chip assembly was subjected to standard reflow process. The reflow process was executed in six phases as follows:

- Phase 1: 60 seconds @150℃
- Phase 2: 120 seconds @150℃
- Phase 3: 30 seconds@200℃
- Phase 4:17.5 seconds@240℃
- Phase 5: 5 seconds@240℃
- Phase 6: 97.5 seconds@25℃

In addition, following boundary conditions were defined as slice model was considered:

- Symmetry on the slice plane (along 'OA').
- Nodes in the opposite plane parallel to OA were coupled to prevent out of plane motion.
- Symmetry on the plane perpendicular to 'OA' passing through 'O'.
- Nodes in the opposite plane parallel to the above plane were coupled to prevent out of plane motion, and

- The node at the bottom and common to the two symmetric planes was fixed in all directions to prevent rigid motion.

4.8.2 Results and Discussion

Based on the aforementioned package attributes, a full factorial DOE with 32 legs was formed and analyzed for maximum stress induced in PO due to the reflow process. For all the simulations, it was assumed that no pre-stress condition exists, the temperature is uniform during the loading and there is perfect adhesion among of all the materials.

When the flip-chip package is subjected to a temperature change (during reflow), the stress is induced at the PO as a result of CTE miss-match between the die and the substrate. For die, the CTE is 2.6 ppm/°C while that of substrate is 12.4 ppm/°C, thus giving a difference of 9.8 ppm/°C which exerts a high stress on the bump. Similarly the difference in CTE between the die (2.6 ppm/°C), Al trace (22 ppm/°C) and Cu UBM (16.5 ppm/°C) locally exerts a high stress at the PO. This CTE miss-match between the adjacent materials is known as local CTE miss-match whereas that between the non-adjacent (between the die and the substrate) materials is known as global CTE miss-match. In the following three sections, stress is analyzed at the PO for the corner bump, outer eight bumps and center bumps respectively of the slice model.

4.8.2.1. Stress in the PO of the corner bump

For each leg of the DOE, maximum stress (at the PO) was always noted for the outermost (corner) bump. Thus, each leg of the variability chart in Fig. 4.23 shows the maximum stress at the PO for the corner bumps. The maximum stress of 138 KPa was noted for leg 29 of the DOE, with the die thickness of 800 µm, substrate thickness of 1200 µm, die size of 10 µm, substrate size of 15 µm (1.5 times the die size) and PO size of 60 µm. The minimum stress of 7 KPa was noted for leg 2 of the DOE with the die thickness of 100 µm, substrate thickness of 600 µm, die size of 10 µm, substrate size of 15 µm (1.5 times the die size) and PO size of 60 µm. Thus, thick die, thick substrate and small PO size induces higher stress in the PO while thin die, thin substrate and large PO size induces smaller stress in the PO. It is observed that the

most important design attributes concerning the stress at the PO are the die thickness, PO size and the substrate thickness respectively. Following paragraphs discuss this in further detail.

From Fig. 4.23 it can be observed that the stress increases with increase in the die thickness. Increase in the die thickness, increases the local CTE miss-match between the die and the trace (Al) resulting in higher stresses at the PO. The change in stress is more significant for the bumps with larger PO size. This can be again attributed to the local CTE miss-match as mentioned above.

Previously, the smaller PO size was recommended to minimize the device failure due to electromigration. Figure 4.15 shows the variation in current density in the bump for the input current of 0.1 A. While considering only the effect of PO size, from Fig. 4.15, it can be observed that current density in the bump is less for small PO size. However, post reflow process, the bumps with small PO size exhibit higher stress than bumps with large PO size, especially for the scenarios 17 to 24 where the die thickness (800 µm) is greater than the substrate thickness (600 µm). Otherwise, the effect of PO size becomes more prominent with the increase in substrate thickness to die thickness ratio. Thus, under identical thermal load, the stress induced in the PO inversely depends on the size of PO.

Similar to die thickness, the stress in PO is also proportional to the substrate thickness as shown in Fig. 4.23. With increase in substrate thickness, the global CTE miss-match between the die and the substrate is enlarged which induces high stress in the bump at the PO.

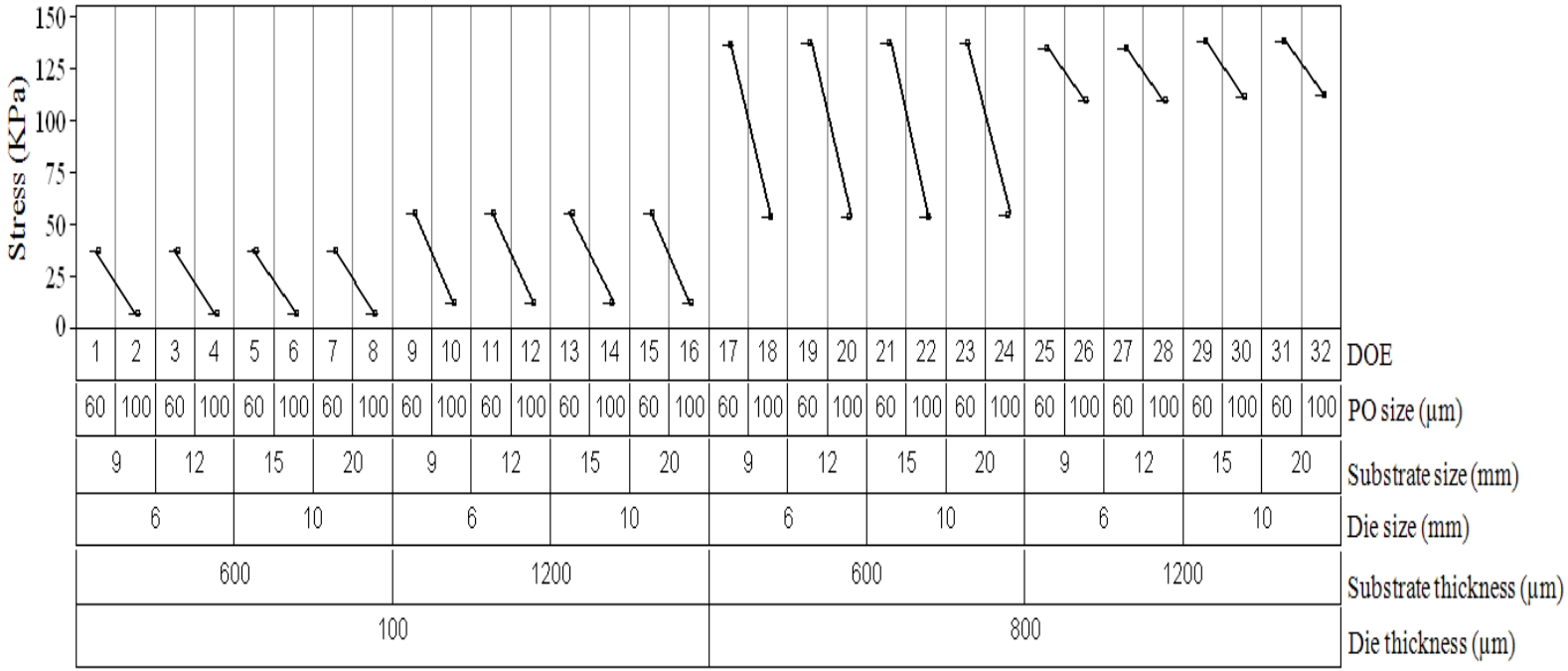


Figure 4.23 Variability chart for the maximum stress at passivation opening for the corner bumps

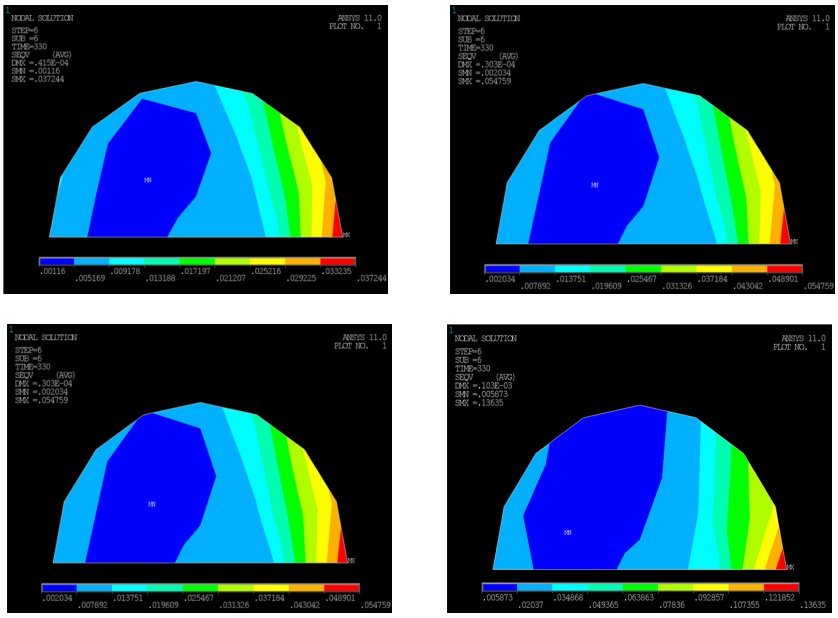


Figure 4.24 Stress contours for small PO size

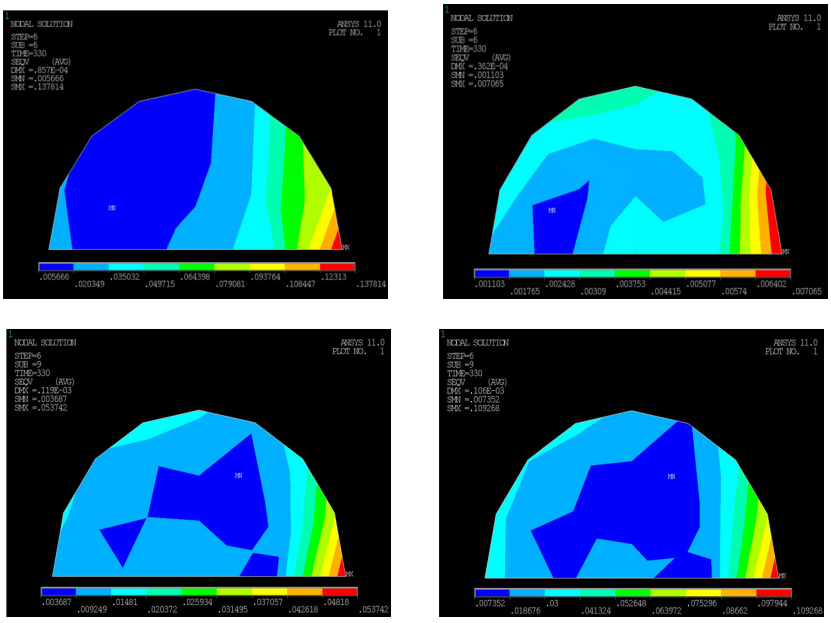


Figure 4.25 Stress contours for large PO size

In this study, the effect of substrate size and the die size on the stress was also studied in the form of two different ratios (substrate size/die size) of 1.5 and 2. From Fig. 4.23, it can be

observed that the variation in the stress is insignificant for both the ratios. However, it has been reported elsewhere that if the substrate size is kept constant and die size is increased, the global maximum stress also increases [91]. For all the scenarios, the maximum stress was always observed on the periphery. The stress contours however vary with the PO size. For large PO size, stress is induced in the area closer to circumference of the PO. In the case of small PO size, the stress contours are lateral bands with diminishing stress values as you travel away from the periphery (where maximum stress is observed) towards the center. This phenomenon can be clearly seen in Fig. 4.24. Since the stress contours for scenarios with small PO as well as large PO are similar, stress plots for selected legs are shown in Fig. 4.25.

4.8.2.2 Stress in the PO for the outer eight bumps

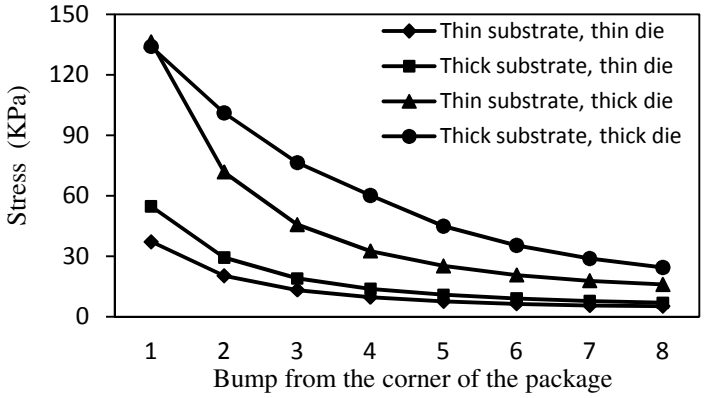


Figure 4.26 Stress at PO in outer eight bumps for small PO size

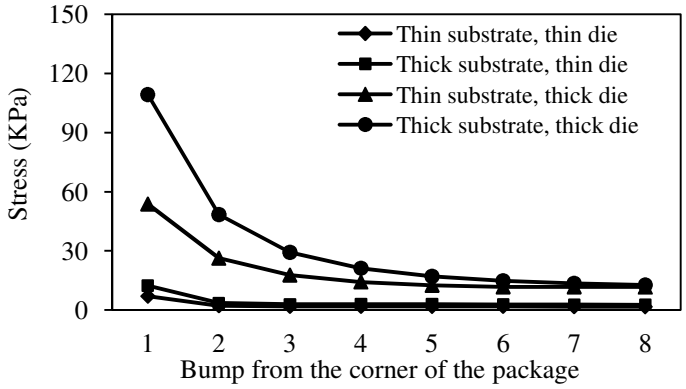


Figure 4.27 Stress at PO in outer eight bumps for large PO size

Induced stress depends on the DNP (distance from neutral point) and hence noticeable variation in stress is observed for outer bumps (maximum for the corner bump). This variation in stress at the PO for the outer eight bumps is shown in figs. 4.26 and 4.27. The variation in stress for the remaining bumps (termed as center bumps) is discussed in the later section of the chapter. Figures 4.26 and 4.27 show the stress for selected legs of the DOE. In Figs. 4.26 and 4.27, the thinness and the thickness of the substrate are 600 µm and 1200 µm respectively, while the thinness and thickness of the die are 100 µm and 800 µm respectively. Die size and substrate size do not alter the stress results and hence are not shown. Bump 1 is the corner most bump in Fig.s 4.26 and 4.27. From these two figures, it can be seen that the same trend is observed as that in Fig. 4.23. Packages with thin substrate, thin die and large PO size exhibit less stress post-reflow process. Stress at the PO decreases as we migrate from the corner bump towards the center of the package. In Fig. 4.26, stress in the small PO for the case of thin substrate and thin die exhibit different trend than the others. This may be attributed to the enlarge CTE miss-match between the die and the substrate.

4.8.2.3 Stress in the PO of the center bumps

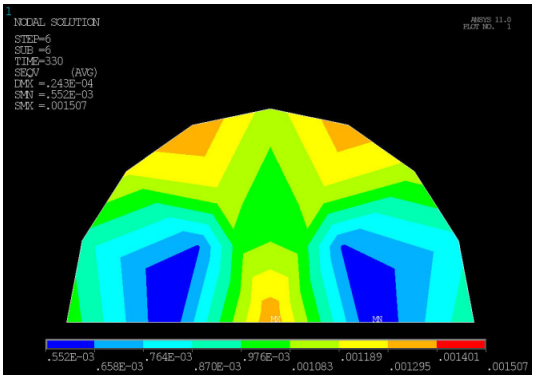


Figure 4.28 Stress contour at PO for inner bump for large PO size

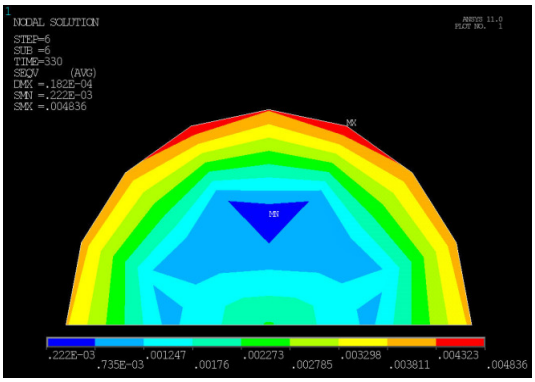


Figure 4.29 Stress contour at PO for inner bump for small PO size

As mentioned earlier, the maximum stress was always observed at the outer bump and the stress reduced as we move towards the center of the package. These results were in agreement with the literature [83, 84]. For all the scenarios, stress in the PO of the center bumps (bumps other than outside eight bumps along the diagonal) was comparatively small. As we move towards the center of the package, the variation in stress in the adjacent bumps is not significant. In these bumps, PO size has no effect on the induced stress. Unlike the outside eight bumps, stress pattern at the PO for inner bumps is symmetrical for both small and large PO, as shown in figs. 4.28 and 4.29 respectively.

Table 4.5 Effect of location and PO size on the current crowding and stress in the bump

Location	PO Size			
	60 µm		100 µm	
	Current crowding	Stress	Current crowding	Stress
Corner bump	Low	High	High	Low
Center bump	Low	Low	High	Low

Based on the results of the computational analysis, the center bumps where the effect of PO size on stress is not significant may be used as electrical interconnects (with small PO as recommended previously to minimize the current crowding) with high operating currents to improve the MTTF of the device. However, at the periphery, it is necessary to consider the effect of PO size. The trace connections should be designed so as to avoid the coincident location of the maximum stress and current crowding. The point of maximum stress and the maximum current crowding will significantly impact the MTTF. Table 4.5 summarizes the effect of bump location and the PO size on the current crowding and the stress in the bump.

4.9 Summary

In this chapter, results of two analysis were combined to develop design guidelines to improve the package reliability from electromigration stand point. First, analysis was performed in order to study the effect of Al trace width, UBM thickness, UBM diameter and PO diameter on current density in Al trace and the bump. Maximum current crowding was always observed in the metallization. In the metallization the most important design attribute found was the Al trace width. For the solder, the most important parameters found are Al trace width and UBM thickness. Solder configuration with Al trace of 60 μm, UBM thickness of 7 μm, UBM diameter of 120 μm and PO diameter of 60 μm yielded minimum current density in the Al trace. Whereas, solder configuration with Al trace of 10 μm, UBM thickness of 7 μm, UBM diameter of 120 μm and PO diameter of 60 μm yielded minimum current density in bump. In general, larger trace width and UBM thickness while smaller UBM diameter and PO diameter yields minimum current density.

Later, a full factorial DOE was formed to study the stresses induced in the bump due to reflow process as a function of attributes of the package architecture. The package architectural attributes such as die thickness, die size, substrate thickness, substrate size and PO size were studied in detail.

For all the legs, the maximum stress was always noted at the corner bump. The packages with thick substrate exhibited higher stress than packages with thin substrate. Bumps with small PO size exhibited higher stress than the bumps with large PO size. For bumps with small PO size, the stress contours are lateral bands where as in case of bumps with large PO size, high stress is noted at the periphery and diminishes towards the center. The packages with thick die yielded higher stress than packages with thin die. The effect of ratio of substrate size to die size (between 1.5 and 2) on the stress induced in the bump at the PO is insignificant. Stress in the PO is directly proportional to the DNP. However, the effect of PO size is insignificant for the center bumps.

Based on the results, it is recommended that center bumps with small PO should be used for I/Os requiring high operating currents. Small PO size will have better resistance to bump electromigration and also would not be impacted by the stress. Outer bumps with large PO size should be used for I/Os requiring low operating currents. Large PO size will also facilitate higher heat transfer rate from the die to the board. Thus, a hybrid package with the combination of high and low PO size bumps would increase the package reliability.

CHAPTER 5

MULTI OBJECTIVE OPTIMIZATION FOR NON UNIFORMLY POWERED MICROPROCESSOR

5.1 Microprocessors

Microprocessor is the heart of any computer. They are sometimes referred to as a logic chip or central processing unit (CPU). A microprocessor consists of millions of transistors that work together in order to process a specific set of instructions. While performing any task, for example, listening music, web surfing etc., a microprocessor processes the data in three steps [92]. In the first step, the microprocessor gets instruction from the memory regarding what to do with the data. In the second step, the microprocessor interprets the instructions and in the third step, it executes the instructions to complete the process. These three steps in the microprocessor language are known as fetch, decode and execute respectively. These steps are repeated for millions of times in a second [92].

Microprocessors were first introduced in early 70's by Intel (Intel 4004), Texas Instruments (TMS 1000) and Central Air Data Computer (CADC) [93]. Since then, many different microprocessors were introduced by Motorola, IBM, HP, AMD and others. Today, for the desktops and the mobile computers, Intel and AMD processors are more commonly used.

Microprocessors are primarily distinguished based on instruction set (set of instructions that a microprocessor can process), bandwidth (number of bits processed per instruction) and clock speed (number of instructions that a microprocessor is able to execute per second). Larger the bandwidth and higher the clock speed, superior is the microprocessor. For example, a 64 bit microprocessor is better than a 32 bit microprocessor while a 2.53 GHz (Pentium IV) will be faster than 1.5 GHz (Pentium III) microprocessor.

Table 5.1 Summary of Intel microprocessors and their attributes [94]

Sr. No.	Microprocessors	Year introduced	Clock speed	No. of transistors	Manufacturing technology
1.	Intel 4004	1971	108 KHz	2,300	10µ
2.	Intel 8008	1972	500-800 KHz	3,500	10µ
3.	Intel 8080	1974	2MHz	4,500	6µ
4.	Intel 8086	1978	5 MHz	29,000	3µ
5.	Intel 8088	1979	5 MHz	29,000	3µ
6.	Intel 286	1982	6 MHz	134,000	1.5µ
7.	Intel 386	1985	16 MHz	275,000	1.5µ
8.	Intel 486	1989	25 MHz	1,200,000	1µ
9.	Intel Pentium	1993	66 MHz	3,100,000	0.8µ
10.	Intel Pentium Pro	1995	200 MHz	5,500,000	0.6µ
11.	Intel Pentium II Intel Pentium II Xeon	1997	300 MHz	7,500,000	0.25µ
12.	Intel Pentium III Intel Pentium III Xeon	1999	500 MHz	9,500,000	0.18µ
13.	Intel Pentium 4 Intel Xeon	2000 2001	1.5 GHz	42,000,000	0.18µ
14.	Intel Pentium M	2002	1.7 GHz	55,000,000	90nm
15.	Intel Itanium 2	2002	1 GHz	220,000,000	0.13µm
16.	Intel Pentium D	2005	3.2 GHz	291,000,000	65nm
17.	Intel Core 2 Duo Intel Core 2 Extreme Dual-core Intel Xeon	2006	2.93 GHz	291,000,000	65nm
18.	Dual-core Intel Itanium 2 9000 series	2006	1.6 GHz	1,720,000,000	90nm

Table 5.1 *Continued*

19.	Quad-Core Intel Xeon Quad-Core Intel Core 2 Extreme Intel Core 2 Quad	2006 2007	2.66 GHz	582,000,000	65nm
20.	Quad-Core Intel Xeon (Penryn) Dual-Core Intel Xeon (Penryn) Quad-Core Intel Core 2 Extreme (Penryn)	2007	>3GHz	820,000,000	45nm

In microprocessor fabrication, one of the important features is the minimum feature size (gate length) that can be fabricated which in technical terms is referred as manufacturing technology. Smaller feature size allows more number of transistors as well as other components to be packaged on a single microprocessor. This improves the microprocessor performance. The roadmap for the transistor count is very well defined by Moore's law [95] which states that the number of transistors on a chip would double about every two years. Later, it was modified to say that the number of transistors on a chip would double every 18 months. Pertaining to Intel microprocessors, Table 5.1 summarizes the microprocessors, the year in which they were introduced, their clock speed, the number of transistors and the corresponding manufacturing technology [94].

5.2 Computer architecture

The concept of the computer architecture is similar to that of a building architecture. Building architecture is a plan or layout of different functionalities such as kitchen, dining etc. A structural engineer carefully reviews the requirements and then designs the layout based on several factors such as stress, strain etc. Similarly, the computer architecture is a plan of overall functionalities of the computer or more specifically a microprocessor which includes the basic operations it can perform, the sequence of the instructions and so on. Based on these

requirements, a circuit designer puts together the basic components such as transistors, resistors, capacitors etc. on a single silicon die.

There are two architectural levels namely the instruction set and the microarchitecture. The instruction set architecture (ISA) refers to the lowest level visible to a programmer [96]. Microarchitecture level is a level which addresses the interconnection and the operation of the constituent parts of the system in order to execute the ISA [97].

The microprocessors are mainly based on two architectural designs, the Complex Instruction Set Computer (CISC) and the Reduced Instruction Set Computer (RISC). The primary difference between the two is the type of the instruction set. As the name goes, the microprocessors based on CISC architectures have a different and complex set of instructions whereas the microprocessors based on RISC architectures have simple set of instructions. In short, the CISC microarchitecture is slower but needs little instructions when compared to the RISC microarchitecture [97]. Examples of the CISC architectures are VAX, Motorola 680x0, Intel 80x86, etc. Examples of the RISC architectures are SUN's SPARC, HP's PA-RISC, DEC's Alpha, etc. Virtually all new instruction sets since 1982 are based on RISC. In 1993, Motorola, IBM and Apple together introduced a Power PC architecture which was hybrid of both CISC and RISC architectures. It was then commonly used in Apple Macintosh and in IBM's mainframe.

Industries also tend to have their own architecture classifications based on design. For example, since the advent of first microprocessor, Intel has several architectures namely, Willamette, Northwood, Prescott, Cedar Mill, Nehalem, Core/Penryn, etc. Similarly, AMD has several architectures namely K5, K6, K7, Griffin, Bulldozer, etc.

5.3 Microprocessor Components

As mentioned earlier, a microprocessor consists of several million transistors. Recently, Intel announced the world's first 2 billion transistor microprocessor (Intel Itanium, codenamed Tukwila) which would have higher processing speed [100]. These transistors and other components such as resistors, capacitors etc are grouped to form a functional unit. Each

functional unit is programmed to execute specific set of instructions. Figures 5.1 and 5.2 show the pictorial view and the floor plan of Pentium IV microarchitecture.

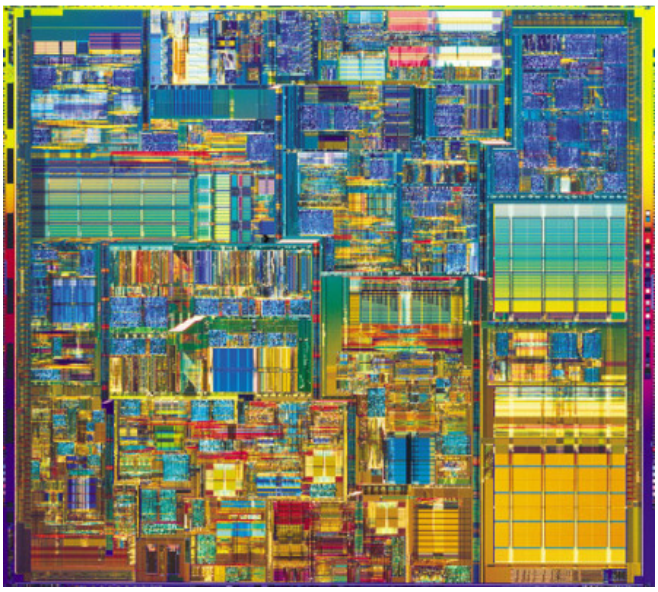


Figure 5.1 Pictorial view of Pentium IV microprocessor [98]

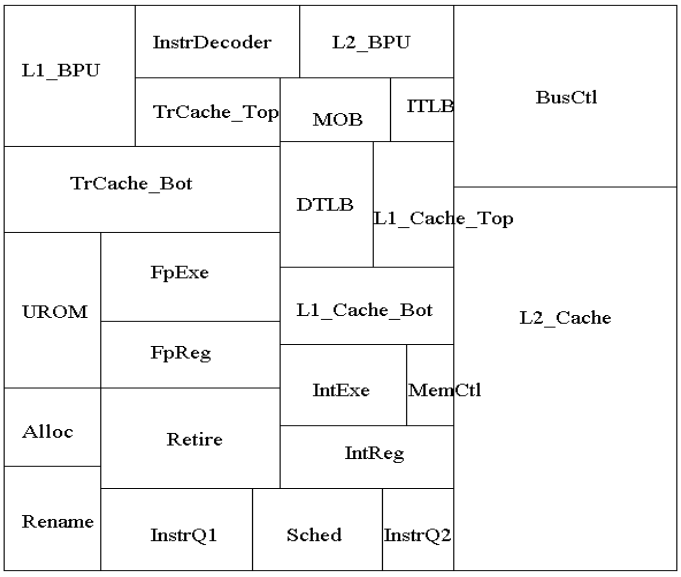


Figure 5.2 Floor plan of Pentium IV microprocessor [99]

From Fig. 5.2, it can be observed that there are 24 functional units such as L1 Cache, L2 Cache, BPU (Bits Processing Unit), etc. These functional units can broadly be classified under five categories as,

- Control unit
- I/O units
- Arithmetic Logic Unit (ALU)
- Registers
- Cache.

The control unit assists in execution and coordination of other units by providing timing and control signals. The pre-stored logic interprets the instructions and then generate signals necessary for the execution of those instructions. For example, an instruction to add two numbers would trigger the control unit to activate the addition module.

The I/O units are used for the communication between the microprocessor and the external components such as RAM, hard disk, etc. It is also referred to as the Bus interface and may consume a significant amount of the microprocessor floor plan.

The ALU is a combinational circuit (generalized gate circuit with m inputs and n outputs) which is capable of performing basic operations such as addition, subtraction, multiplication, etc. or any other logical operations. It is the most fundamental block of the microprocessor and is very powerful and complex, specially the modern day microprocessors.

A register is a microprocessor's internal storage (fastest accessible memory location) which is used for storing data and performing operations on it. The size of the registers defines the size of the microprocessor. For example, a 32 bit microprocessor has registers that are 32 bit long.

The cache is the memory located on the chip itself. Frequently needed data is stored in the cache as accessing it is much faster than communicating with external memory such as RAM or

hard disk. Typically, each microprocessor has two levels of cache namely L1 cache and L2 cache. The L1 cache is smaller but faster than the L2 cache. The cache can occupy upto 50% of the chip real estate.

5.4 Microprocessor performance

While selecting a microprocessor, one of the deciding criteria is the microprocessor performance. However, the performance is a very relative term and in general its definition varies with the microprocessor application. For example, when running a program on two different workstations, the one which executes the program faster has better performance. But for a computer center (shared systems) where multiple jobs are submitted, the workstation which processes most jobs during a day has better performance. Thus, performance can be measured by two means:

1. Rate at which a single job is processed, and
2. The number of jobs that are processed in a specific time.

The first method to evaluate performance is termed as "response time" while the second method is termed as "throughput". One may argue that decreasing response time (by increasing the clock speed) will always increase the throughput then why the "throughput" is considered as a separate measure for performance. To illustrate this, Hennesy *et al.* [97] discussed two scenarios in order to increase the throughput, reduce the response time or both. In the first scenario, the processor in a computer is replaced with a faster version whereas in the second scenario a second processor is added to the system and thus have the multi-processing capability for separate tasks. In the first scenario, both the response time and the throughput are improved whereas in the second scenario, only the throughput is increased. The response time and the throughput are further discussed in detail in the following sections.

5.4.1 Response time

The performance of any microprocessor is inversely proportional to its execution time. Thus, in order to maximize the performance, the response time needs to be minimized. The program

execution time is measured in seconds per program. The CPU execution time (also known as CPU time) is the actual time the CPU spends on the task and does not include time spent on waiting for input/output (I/O). The CPU time can be divided further into user CPU time and system CPU time. The time spent in the program is referred as user CPU time while the time spent in the operating system performing the task is referred as system CPU time [97]. The CPU time can be estimated based on the number of clock cycles and time for each clock cycle as shown in equation 5.1.

$$\begin{bmatrix} CPU\ execution\ time \\ for\ a\ program \end{bmatrix} = \begin{bmatrix} CPU\ clock\ cycle \\ for\ a\ program \end{bmatrix} x \begin{bmatrix} Clock\ cycle \\ time \end{bmatrix} \quad (5.1)$$

A microprocessor always executes the instructions and the execution time depends on the number of instructions in the program. Also, each microprocessor has a clock which runs at a constant rate and determines when the events occur (such as executing an instruction) in the hardware. Thus, number of clock cycles required for a program is given by equation 5.2 [97].

$$\begin{bmatrix} CPU\ clock \\ cycles \end{bmatrix} = \begin{bmatrix} Instructions\ per \\ program \end{bmatrix} \text{ x } \begin{bmatrix} clock\ cycles \\ per\ instruction \end{bmatrix} \quad (5.2)$$

The term clock cycles per instruction (CPI) is the average number of the clock cycles each instruction takes to execute. Thus, the performance of a microprocessor can now be written in terms of the instruction count, the CPI and the clock cycle time as shown in equations 5.3 and 5.4. These equations defines the three key factors that affect the performance and hence can be used to compare two different microprocessors.

$$[CPU\ time] = [Instruction\ count] \text{ x } [CPI] \text{ x } [Clock\ cycle\ time] \quad (5.3)$$

$$CPU\ time = \frac{Instruction\ count \text{ x } CPI}{Clock\ rate} \quad (5.4)$$

One of the ways to improve the performance by reducing the CPU time is to use parallel processing. However, this may not be true according to Amdahl's law [101]. Amdahl's law states that the performance improvement to be gained by using a faster mode of execution is limited by the fraction of the time the faster mode can be used. To illustrate this, consider a program which has two loops with total execution time of 5 hours. Loop 1 consists of 200 lines and utilizes 4 hours of the total execution time. Loop 2 consists of 10 lines and uses the remaining 1 hour of the total execution time. Now let's say, only loop 2 (and not loop 1) can be executed on a parallel processor, then irrespective of the number of processors, the reduction in the CPU performance will not be more than one hour (which is the limiting case). Thus, the performance enhancement to be gained by using a faster mode of execution is limited by the fraction of the time the faster mode can be used. Mathematically, the law is given by equation 5.5. In equation 5.5, *S* is the improvement factor, *f* is the fraction of the problem that must be computed sequentially and *N* is the number of processors.

$$S \leq \frac{1}{f+(1-f)/N} \tag{5.5}$$

To summarize, for a given instruction set architecture, microprocessor performance can be enhanced by [97]:

- Increase in the clock rate
- Improvement in the processor organization
- Improving the compiler that lowers the instruction count or generates the instructions with a lower average CPI (by using simpler instructions).
- In some cases, parallel processing may be used depending upon the process.

5.4.2 Throughput

As mentioned earlier, throughput is the amount of work done by a microprocessor within a given time. The speed at which the work is done largely depends on the I/O systems or the I/O

performance. Impact of the I/O on system performance can be best explained through one of the examples in [97]. Let us suppose that we have a program which executes in 100 seconds of the total time, where 90 seconds is the CPU time and the rest is the I/O time (10 seconds). Now, if the CPU time improves by 50% per year for the next five years but the I/O time remains the same, then the performance improvement that is achieved each year is summarized in Table 5.2.

Table 5.2 Summary of performance improvement [97]

After *n* years	**CPU time (sec)**	**I/O time (sec)**	**Elapsed time (sec)**	**%I/O time**
0	90	10	100	10%
1	90/1.5 = 60	10	70	14%
2	60/1.5 = 40	10	50	20%
3	40/1.5 = 27	10	37	27%
4	27/1.5 = 18	10	28	36%
5	18/1.5 = 12	10	22	45%

It can be observed that the improvement in the CPU performance over five years is 7.5 (90/12) while improvement in the elapsed time is only 4.5 (100/22). The I/O time has increased from 10% to 45% of the elapsed time which shows that the I/O cannot be ignored. In gauging the throughput, the I/O performance can be evaluated through the I/O bandwidth which further can be measured in two different ways as follows [97]:

- How much data can be moved through the system in a given time?
- How many I/O operations can be done per unit of time?

The first method is adopted where transfer bandwidth is important, for example in case of the supercomputer operation where all the data is transferred from the work-station to the supercomputer. The second method is used where large number of small (in size), repetitive

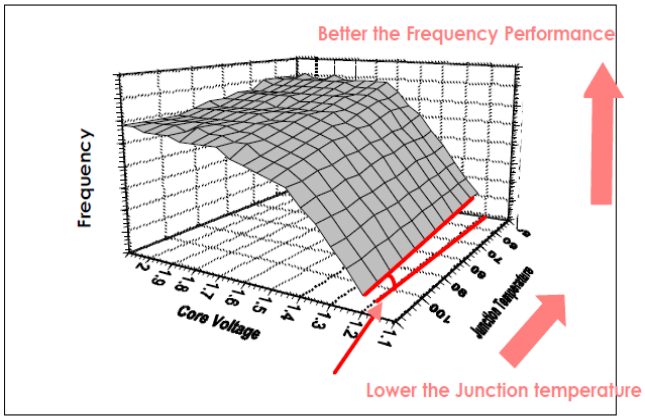
processes occur, for example a network printer where the only task is to print different jobs submitted by different users.

5.5 Thermal management of microprocessors

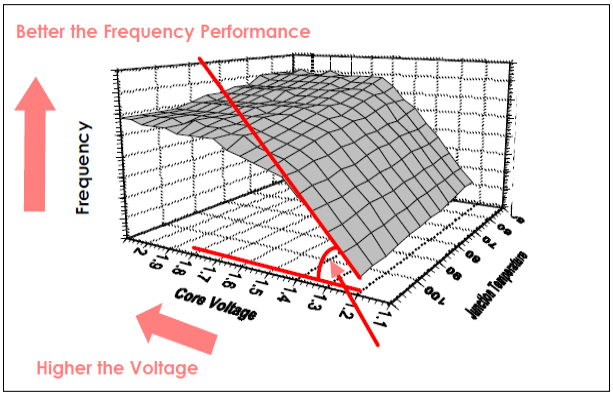
Let's suppose that we have a microprocessor which has very high performance (in comparison with the microprocessors that are commercially available) but has a very short life. Such microprocessor is of no use and hence along with the performance, reliability or life of the microprocessor is equally important. As mentioned in the previous chapter , reliability has a strong relationship with the microprocessor temperature. For example, the reliability of the silicon chip is decreased by about 10% for every 2℃ of temperature rise [3]. Thus, the thermal management is a process to maintain the microprocessor (from thermal perspective, it is referred as die) temperature at or below the threshold value (typically 85℃) to assure performance and reliability while dissipating power to a local ambient [102]. The performance in this case is the execution time and is often gauged in terms of MHz or delay (in seconds). The power is the product of the voltage and the current through the microprocessor components. Mahajan *et al.* showed the dependence of performance on die temperature and the operating voltage (one of the parameter while estimating power). Figure 5.3 shows the same.

From Fig. 5.3 it can be observed that the microprocessor performance is inversely proportional to the die temperature and directly proportional to the voltage. But higher voltage leads to high power and thus affects the reliability. However, if the die is packaged appropriately by virtue of which the heat can be dissipated into the ambient, then a reliable microprocessor can be designed which operates at a lower junction temperature and higher voltages thus enhancing the performance.

Depending upon the application for which the microprocessors are used, natural or forced convection is used to maintain the junction temperature below the threshold limit. The cooling of the microprocessors in applications such as calculators, mobiles etc. is achieved through the natural convection whereas forced convection is the choice of cooling for the microprocessors in



(a)



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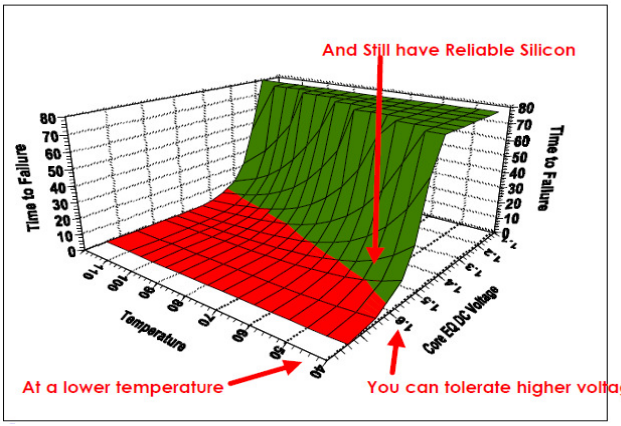
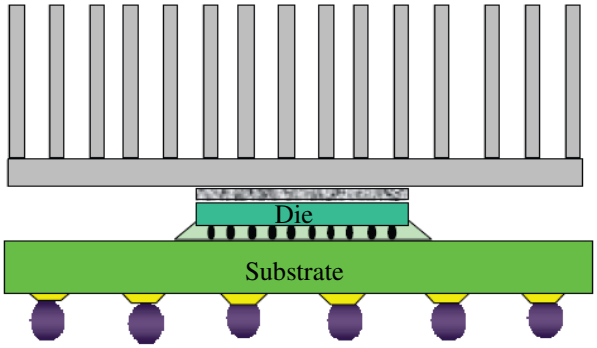


(c)

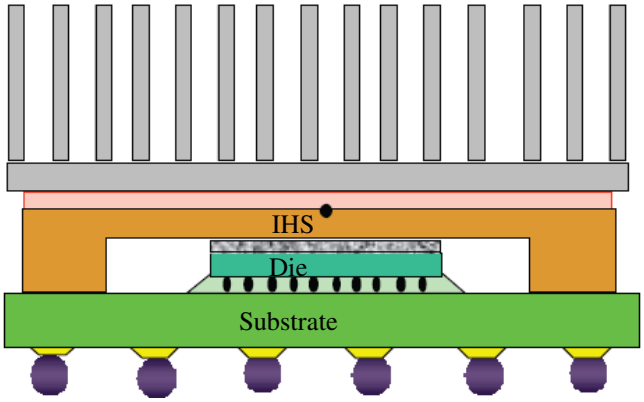
Figure 5.3 Correlation between temperature, voltage, performance and reliability [102] (a) Performance Vs. Junction temperature, (b) Performance Vs. Voltage, (c) Reliability Vs. Temperature and Voltage

applications such as desktop, laptop, servers etc. This work focuses on the high end microprocessors which are discussed in detail in the following sections.

The thermal management of the high end microprocessors is achieved through both the conduction and the forced convection. The heat from the die is conducted to the heat sink which is then cooled by remotely located fans. However, increase in the power density demands an aggressive cooling solution. This demand has led to the use of Integrated Heat Spreader (IHS) and the Thermal Interface Materials (TIMs) with high thermal conductivity such as Indium. IHS is the surface used to make contact between a heat sink and a microprocessor. It facilitates spreading of the heat thereby enhancing the heat transfer. Figure 5.4 shows the schematic of the two methods (with and without heat spreader) described above.



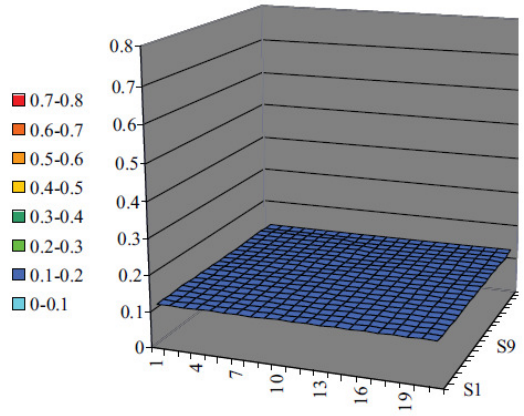
(a)



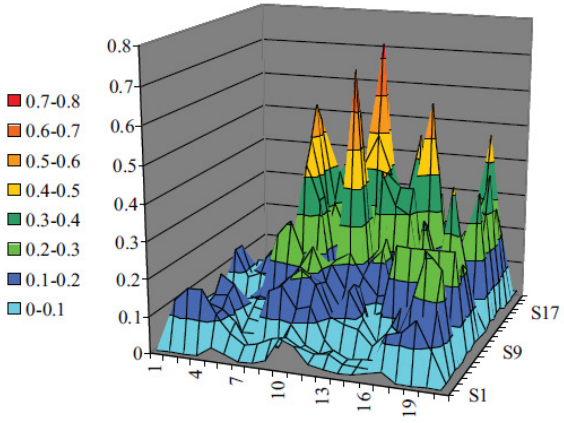
(b)

Figure 5.4 Methods of microprocessor packaging for effective thermal management (a) Heat sink attached to bare die, (b) Use of IHS between the die and the heat sink

The modern die architecture is an integration of the various functional units with distinct powers, frequencies and operating voltages. Although, the integration of various functional units has improved the microprocessor performance, it has further raised the thermal challenges, especially due to the non-uniform power distribution. The traditional approach of assuming uniform power can no longer give reliable results. Figure 5.5 shows the difference between the traditional assumption of the uniform power and the realistic representation of the power distribution for one of the microprocessors [102].



(a)



(b)

Figure 5.5 Difference between the traditional uniform power assumption and reality [102] (a) Uniform power distribution (assumption), (b) Non-uniform power distribution (reality)

Non-uniform power is further more challenging as even with the use of high capacity heat sink, we first need to spread the heat and then dissipate it in the ambient. The high heat flux locally increases the temperature on the surface of the die leading to the formation of hot spots. Because of these hot spots, the die is subjected to large temperature gradients which may induce high thermal stress in the die as well as in the first level interconnect. Figure 5.6 shows the effect of non-uniform power on spreading the heat in a typical heat sink with IHS configuration. In short, non-uniform power reduces the power handling capacity and thus increases the cooling costs.

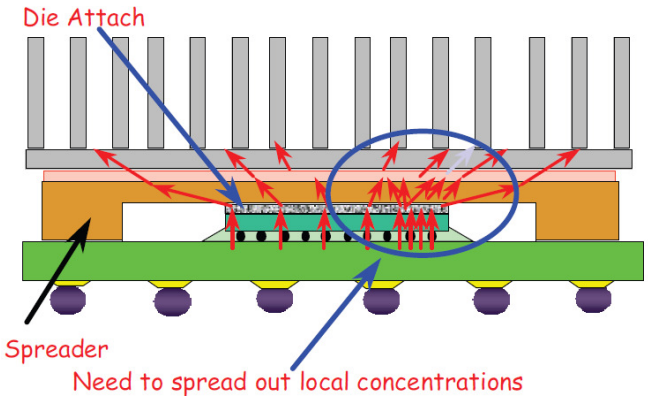


Figure 5.6 Effect of non-uniform power on heat spreading [102]

5.6 The Need for Co-architectural Design Guidelines

In earlier microprocessor generations, the required instructions for the core processor were stored and channeled via the bus from the main memory. In the contemporary generations, technology has made it practical to integrate the level two (L2) cache into the microprocessor architecture. This integrated L2 cache stores the frequently used data, thereby reducing the delay in accessing the necessary information from the L2 cache rather than the main memory. Other on-die functional units such as high-speed I/O interfaces, memory controller, etc. have further enhanced microprocessor performance. Out of many techniques, some of the techniques that improves the microprocessor performance are discussed further.

Ishihara. [103] proposed a compiler based code placement technique that offsets the performance degradation due to the cache defects. The proposed technique is especially effective if there is a faulty cache lines that may affect the microprocessor performance. They showed experimentally that their technique can compensate the performance degradation even when the 5% of the cache lines are faulty.

Nagaraj. [104] proposed a novel post silicon clock tuning system to overcome the clock skew and the path delay due to the process changes, the process variations and the supply voltage variations. The authors claim that by implementing their technique, a 10% improvement in performance was achieved for a benchmark program.

Gebis *et al.* [105] proposed a Virtual Vector Architecture (ViVA) which provides an effective and practical approach to latency hiding. Latency hiding is an commonly adopted optimization technique in which the local computation and the remote communication are overlapped. Authors claim that the implementation of ViVA requires minimal changes to the core design and thus can be easily integrated in any conventional microprocessor. They further showed that for Apple G5 architecture using ViVA, significant enhancement in the performance (2x-13x) can be achieved in comparison to other scalar techniques.

Zu *et al.* [106] showed that the flip chip packages are superior in performance than the wire bonded packages. By performing the electrical modeling, the authors showed that the performance of the microprocessor would increase by 5-9% by moving from wire bond to the flip chip packages. The results were verified using speed test and statistical analysis on electrically similar chips.

Galanis *et al.* [107] mentioned that by adopting a high performance data path in a generic single chip microprocessor, better performance and energy reductions can be achieved. The data path acts as a coprocessor that accelerates the computationally intensive kernel sections thereby increasing the overall performance.

Suri *et al.* [108] proposed a mechanism to improve the pre-core performance without affecting the scalability. They proposed to integrate a Reconfigurable Hardware Unit (RHU) in the resource-constrained cores to improve their performance. In order to improve the performance, the RHU executes the frequently encountered instructions to the cores' overall execution bandwidth. In the experiments performed by the authors, the proposed architecture improved the pre-core performance by an average of 23% over the wide range of applications [108].

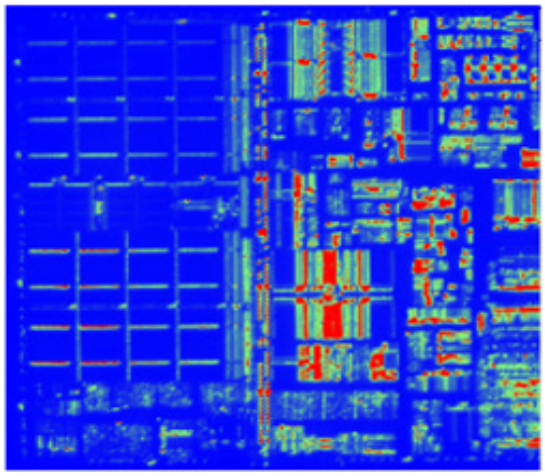
Greskamp *et al.* [109] proposed "Paceline" leader-checker microarchitecture. In this architecture, there are two cores namely a leader core and a checker core. A leader core runs the thread at higher-than-rated frequency while passing the execution hints to the checker core. The checker then redundantly executes the thread faster without the leader while checking the results to guarantee accuracy. In this architecture, the leader and checker cores periodically swap functionality. The authors estimate that by overclocking the leader by 30%, the Paceline improves the performance by roughly 21%.

In conjunction to the performance improvement, power density on the chip has also been doubling and this trend is expected to increase as the feature sizes and the frequencies scale faster than the operating voltages [110-112]. This causes the power on the die to be highly non-uniform and results in a large temperature gradient, with localized hot spots. This may have detrimental effects on the product reliability as well as on the yield. Figure 5.7 shows the hot spots because of non-uniform power on Intel's Pentium® III and Itanium processors [113].

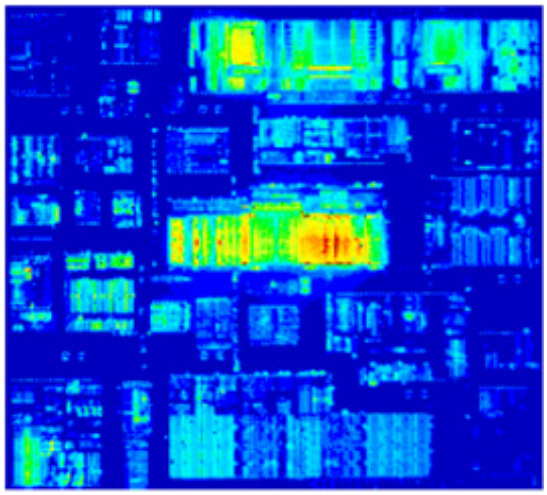
The junction temperature or the temperature gradient on the die depends on the power and the size of each functional unit. Several techniques to determine the junction temperature have been reported. Huang *et al.* [114] reported the presence of the hot spots and their locations as a function of non-uniform power distribution on the die.

Goh *et al.* [115] studied the effect of non-uniform power on the temperature gradient of the die using the concept of superposition and a genetic algorithm approach. They also reported the

effect of the heat source placement distance, the mode of convection heat transfer, and the level of power or heat dissipation.



(a)



(b)

Figure 5.7 Hot-spots as an effect of non-uniform power on Intel microprocessors [113] (a) Pentium III processor, (b) Itanium processor

Getkin *et al.* [116] studied the effect of heat sink using a simplified fin modeling approach for uniformly and non-uniformly powered die. For the identical package conditions, they reported a difference of approximately 20℃ in junction temperature for uniformly and non-uniformly powered die.

Sikka [117] proposed an analytical method for predicting the die temperature for a chip-on-spreader geometry with a non-uniform power distribution. His analysis assumed the one-dimensional heat transfer through the chip and the thermal interface material (TIM) attached to the heat spreader.

June *et al.* [118] proposed a technique to reduce the die hot spot temperatures by using metallic cap integral standoffs that reduce the die-to-lid internal resistance. They demonstrated that appropriate placement of such metallic cap can drastically reduce the maximum junction temperature, especially in the case of non-uniformly powered die.

Skardon *et al.* [119] developed a compact model for the "hot spots" that deals with temperature-aware micro-architecture. It describes a thermal modeling approach that is easy to use and computationally efficient for modeling the thermal effects and the thermal management techniques at the processor architecture level.

Kaisare *et al.* [120, 121] randomly varied the location of different power blocks (functional units) and developed design guidelines pertaining to the placement of different high- and low-power blocks on a single die.

A typical microprocessor comprises of several functional blocks. These functional blocks are fabricated on a single die, each with distinct power, voltage, and frequency. From the literature, it can be seen that several techniques have been proposed to improve and/or analyze the performance and the temperature of the microprocessor. However, none of them considered the effect of one on another parameter. Typically, improving the performance increases the power consumption and thus have challenging issues. Also, from the literature it can be concluded that the temperature gradient along the die depends on the location of these functional blocks. Moving the functional blocks may reduce the temperature gradient but will also affect the wiring length, clock frequencies, etc., which can have detrimental effects on the microprocessor performance. Thus there is a need to perform a co-architectural (performance

and temperature) analysis in which both performance and junction temperature are analyzed. In the following sections such analysis is performed.

5.7 Proof of Concept

Before going into in-depth analysis, it is necessary to see the impact of co-architectural design. For this, a Pentium IV architecture is considered. Obtaining a closed form solutions for a problem where multiple heat sources are applied to the surface of the multilayer body is complicated and not practical for engineering applications and hence computational analysis was performed. Analysis was performed using commercial CFD code [122]. Equations 5.5 and 5.6 are the governing equations for the problem under consideration. Equation 5.5 is a general differential equation for conduction and reduces to equation 5.6 for a steady state condition. Equation 5.6 is also known as Poisson's equation. Boundary conditions of second and third kind are defined on chip surface and on the top of heat sink base respectively. The modeling approach, methodology and results are further discussed in the following sections.

$$\frac{\delta}{\delta x}\left(k_x \frac{\delta T}{\delta x}\right) + \frac{\delta}{\delta y}\left(k_y \frac{\delta T}{\delta y}\right) + \frac{\delta}{\delta z}\left(k_z \frac{\delta T}{\delta z}\right) + q''' = \rho c \frac{\delta T}{\delta t} \tag{5.5}$$

$$\frac{\delta^2 T}{\delta x^2} + \frac{\delta^2 T}{\delta y^2} + \frac{\delta^2 T}{\delta z^2} + \frac{q'''}{k} = 0 \tag{5.6}$$

5.7.1 Modeling Approach

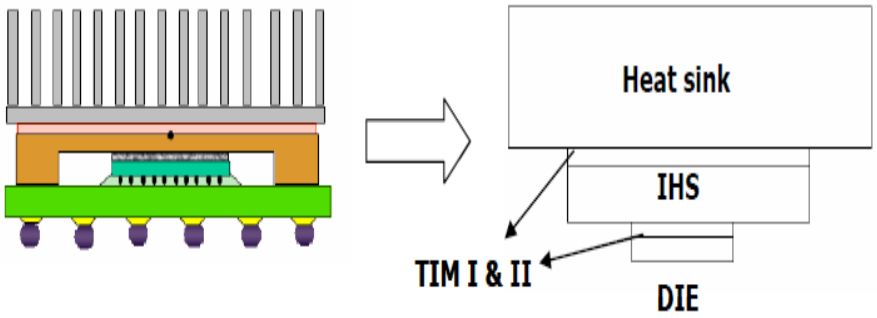


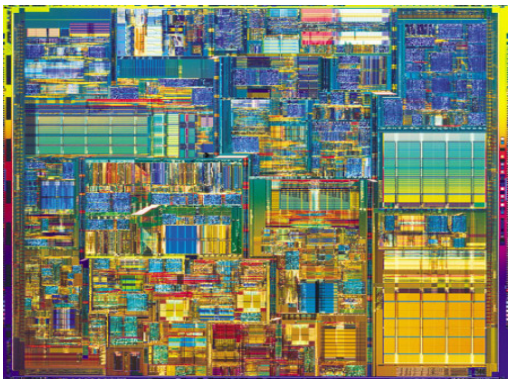
Figure 5.8 Flip-chip package considered for analysis

Figure 5.8 shows the schematic diagram of the flip-chip package considered for analysis. In the analysis, a high end microprocessor is considered and hence it is assumed that heat will only be dissipated through the top of the package. An effective heat transfer coefficient (h) of 1200 W/m^{2}K is defined on top of the heat sink base (fins are not modeled but the increased area is mitigated by using a higher heat transfer coefficient). This h is an effective heat transfer coefficient applied per unit area of the heat sink base (equal to the fin average h times the fin/base area ratio). For the current heat sink dimensions and assuming an external resistance of 0.15°C/W, h is approximately 1,627 W/m^{2}K. Conservatively, we are assuming a value of 1200 W/m^{2}K. The heat from the chip is dissipated to the ambient via thermal interface material (TIM) I (Indium), heat spreader (Copper), TIM II (thermal grease), and heat sink (copper). Dimensions and material properties of all the components of the numerical model are described in Table 5.3.

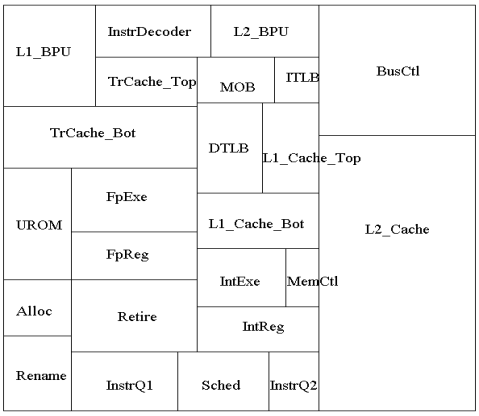
Table 5.3 Dimensions and material properties of the packages in Fig. 5.8

Component	Dimension (mm)	Thickness (mm)	Conductivity (W/mK)
Die	10 x 10	0.75	120
TIM I	10 x 10	0.025	50
Heat spreader	31 x 31	1.8	390
TIM II	31 x 31	0.075	3
Heat sink	64 x 64	6.35	390

Figure 5.9 shows the Pentium IV architecture considered for the analysis. It consists of the core and the cache of the microprocessor. The architecture shows non-uniformly powered functional units. The location of the functional units on the die depends on its function and the criticality of its information. In all, there are 24 functional units on the Pentium IV architecture. However, for the numerical analysis, the die was divided into 36 blocks of equal areas. Depending upon the size, functional units in the numerical model are represented by one, two, three, four or six blocks. The placement and attributes of all 24 functional units are shown in Fig. 5.10 and Table 5.4, respectively.



(a)



(b)

Figure 5.9 Pentium IV floor plan (a) Pictorial view [123], (b) Functional block redistribution [99]

Figure 5.10 Grouping of different functional blocks for the baseline case of Pentium IV architecture

Table 5.4 Attributes and power consumed by the different functional blocks represented in Fig. 5.10

Block No.	**Functional Unit**	**Power** (W) [99]
1	Allocation + Rename + Instruction	7
2	L2 cache	12.9
3	Bus control	11
4	Retire	2.5
5a	Integer register	0.5
5b	Integer execution	0.5
6	UROM	3
7a	Fp register	1.8
7b	Fp execution	1.8
8	Memory control	0.5
9	L1 cache	2.6
10	Dtlb	6.1
11	MOB	13.5
12	IITB	3.5
13	L2 Bpu	7.7
14	Trace cache	2.5
15	L1 Bpu	6.8
16	Instruction decoder	10

5.7.2 Objective and Methodology

The objective of the current analysis is to optimize the location of the functional units to minimize the junction temperature with minimum penalty on the clock performance. It is practically difficult to create a design of experiment (DOE) in which the location of each functional unit is varied owing to the irregular (functional block 1) and dissimilar (functional blocks 2, 3, 6, etc.) sizes of the functional units. Hence, in this analysis, location of the

functional units that are represented by more than two blocks is not changed. Thus, with reference to Fig. 5.10, the position of blocks 1, 2, 3, 5a, 6, 9, and 14 remains unchanged. A DOE with 450 scenarios is created in which the locations of the remaining blocks (4, 5b, 7a, 7b, 10, 11, 12, 13, 15 and 16) are interchanged. Thus, in the DOE, ten functional units can occupy any of these ten positions subjected to the following conditions:

- Any single functional unit cannot occupy more than one position for any given scenario of DOE
- No two functional units can occupy the same position for any given scenario of DOE
- Total power on the die remains constant.

A steady-state thermal analysis is carried out for all the scenarios of the DOE. As mentioned earlier, separation of certain functional blocks will affect the performance. Hence, the following performance criteria were considered for the optimization [124]:

- The penalty of separating FP register (7a) and FP execution (7b) by a distance comparable to the lateral dimension of any one of these units would result in a performance loss of 5%.
- Similar penalties for separating Integer register (5a) and Integer execution (5b).
- Separating any of the blocks at the front end - L1 BPU (15), Instruction decoder (16), trace cache (14), and UROM (6), the performance loss is as high as 25%.

5.7.3 Results and discussion

Subjected to the aforementioned constraints, all the scenarios in the DOE were solved using ANSYS Icepak [122]. Maximum (junction) temperature for each case is noted and the distance between the functional blocks (which affects the performance) is calculated.

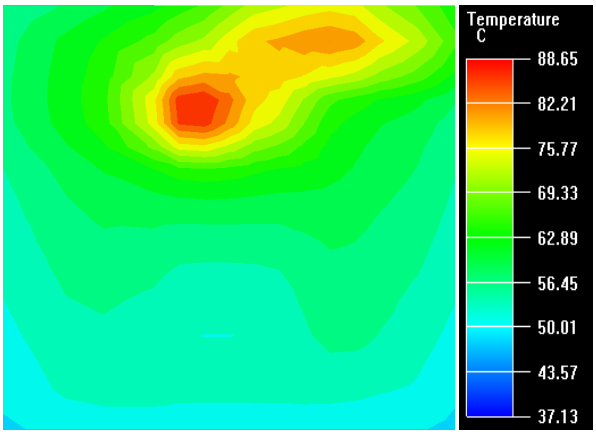


Figure 5.11 Temperature distribution of the baseline case

Figure 5.11 shows the temperature distribution for the baseline case (scenario 1) of the Pentium IV architecture. The maximum temperature was 88.7℃ and since it is the baseline case, penalty on performance was assumed to be zero. For the scenarios in which the performance was altered, a cumulative penalty is reported. For example, if FP register and FP execution are separated by a distance comparable to lateral dimensions of these blocks, then the penalty on the performance is reported as 5%. If, in the same scenario, Integer register and Integer execution are also separated, then an additional 5% penalty is incurred and the cumulative penalty of 10% on the performance is reported. Penalties incurred due to redistribution of the certain functional units are tabulated in Table 5.5. The performance penalty was estimated using MPTlism, a full cycle simulator. Detailed methodology is further mentioned in section 5.8.2 of this document.

Table 5.5 Penalty on performance incurred due to repositioning of function blocks

Functional blocks	**Penalty on performance**
Integer register/ Integer execution or FP register/FP execution	5%
Integer register/ Integer execution **and** FP register/FP execution	10%
L1 BPU/Trace cache/UROM/Instruction decoder	25%

Table 5.5 *Continued*

L1 BPU/Trace cache/UROM/Instruction decoder **and** FP register/FP execution	30%
L1 BPU/Trace cache/UROM/Instruction decoder **and** Integer register/ Integer execution	30%
L1 BPU/Trace cache/UROM/Instruction decoder **and** Integer register/ Integer execution **and** FP register/FP execution	35%
Anything Else	0%

The results of the DOE are categorized based on the penalty incurred and are presented in figs. 5.12-5.17 and are summarized in Table 5.6. The minimum and the maximum temperatures were 82.4℃ and 94.5℃ respectively. The corresponding penalty on the performance was 35% and 0%.

Maximum temperatures are noted for the scenarios in which the high-powered functional blocks (Dtlb, MOB, L2 BPU, L1 BPU and Instruction decoder) are located peripherally. When these high-powered blocks are scattered, low temperature is observed. However, scattering of these high-power blocks also results in high penalty on performance. For example, separating Instruction decoder (10 W), L2 BPU (7.7 W), and L1 BPU (6.8 W) will definitely yield lower temperatures but at a cost of a 25% penalty on the performance. Thus, from the results, it can be noted that, as the penalty on performance increases, more scenarios depict temperatures lower than the baseline scenario. Table 5.6 summarizes the minimum temperature for each penalty on performance. For the optimized scenario, a temperature of 83.2℃ is achieved for a penalty of 5%. In the optimized floor plan, the highest power functional unit (MOB -13.5 W) is swapped with the least power functional unit (Integer register - 0.5 W). Figure 5.18 shows the location of the functional blocks for the baseline case and the optimized case.

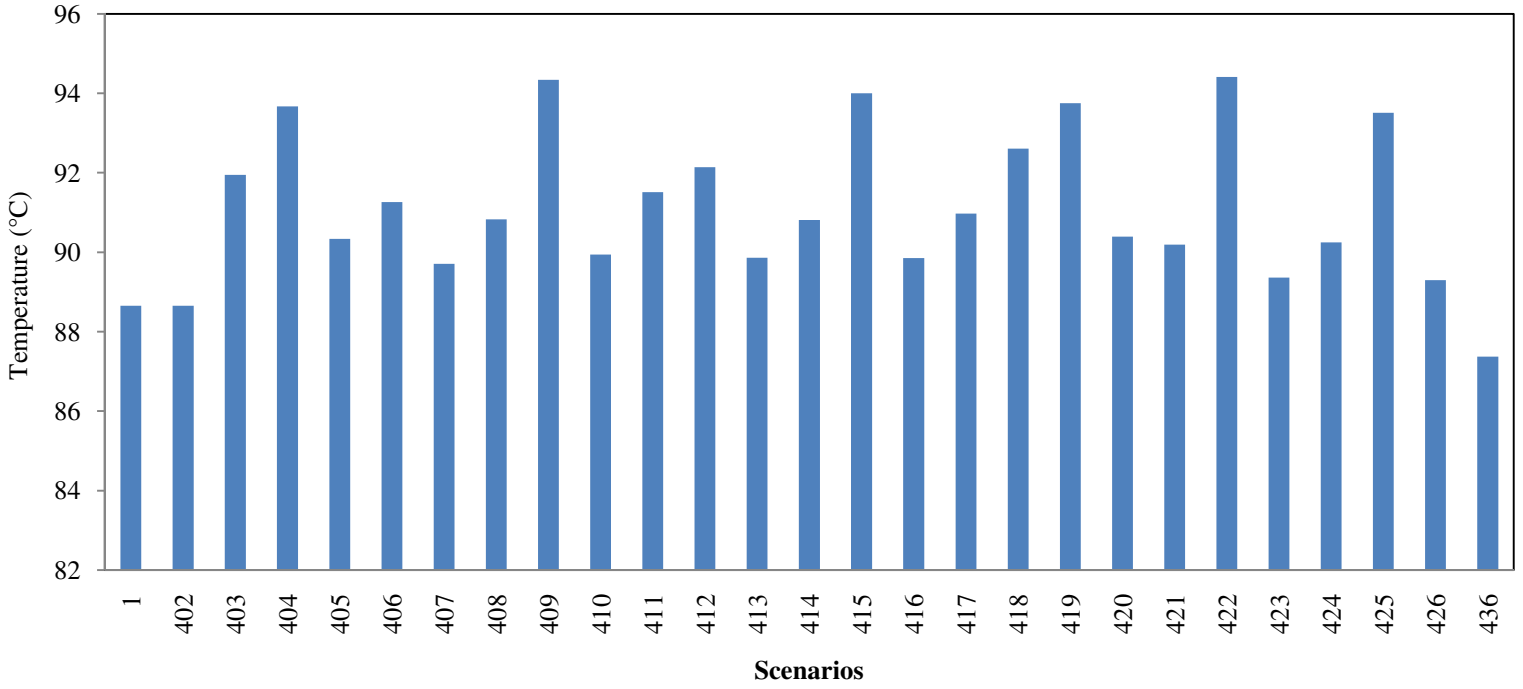


Figure 5.12 Maximum temperature of various scenarios for 0% penalty on performance

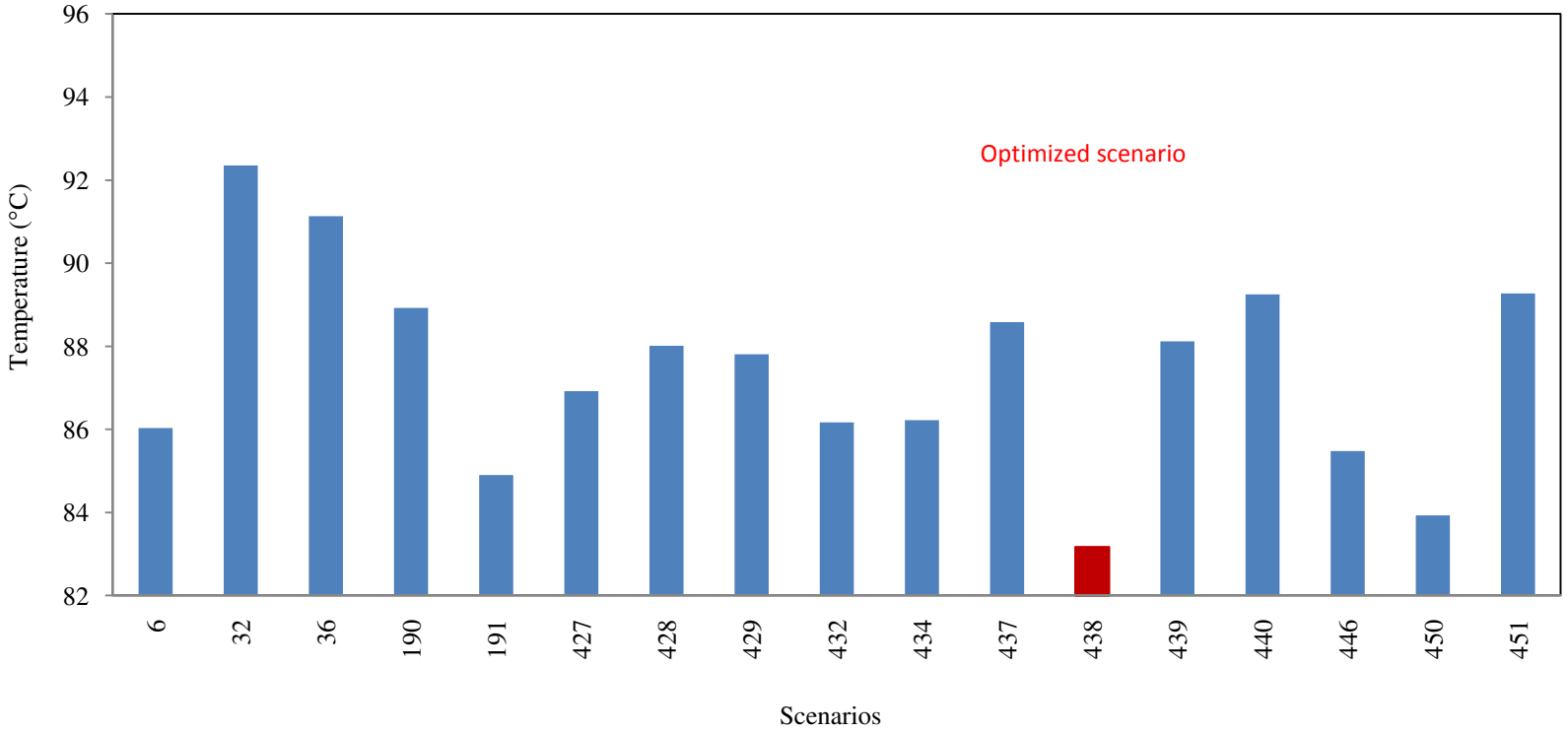


Figure 5.13 Maximum temperature of various scenarios for 5% penalty on performance

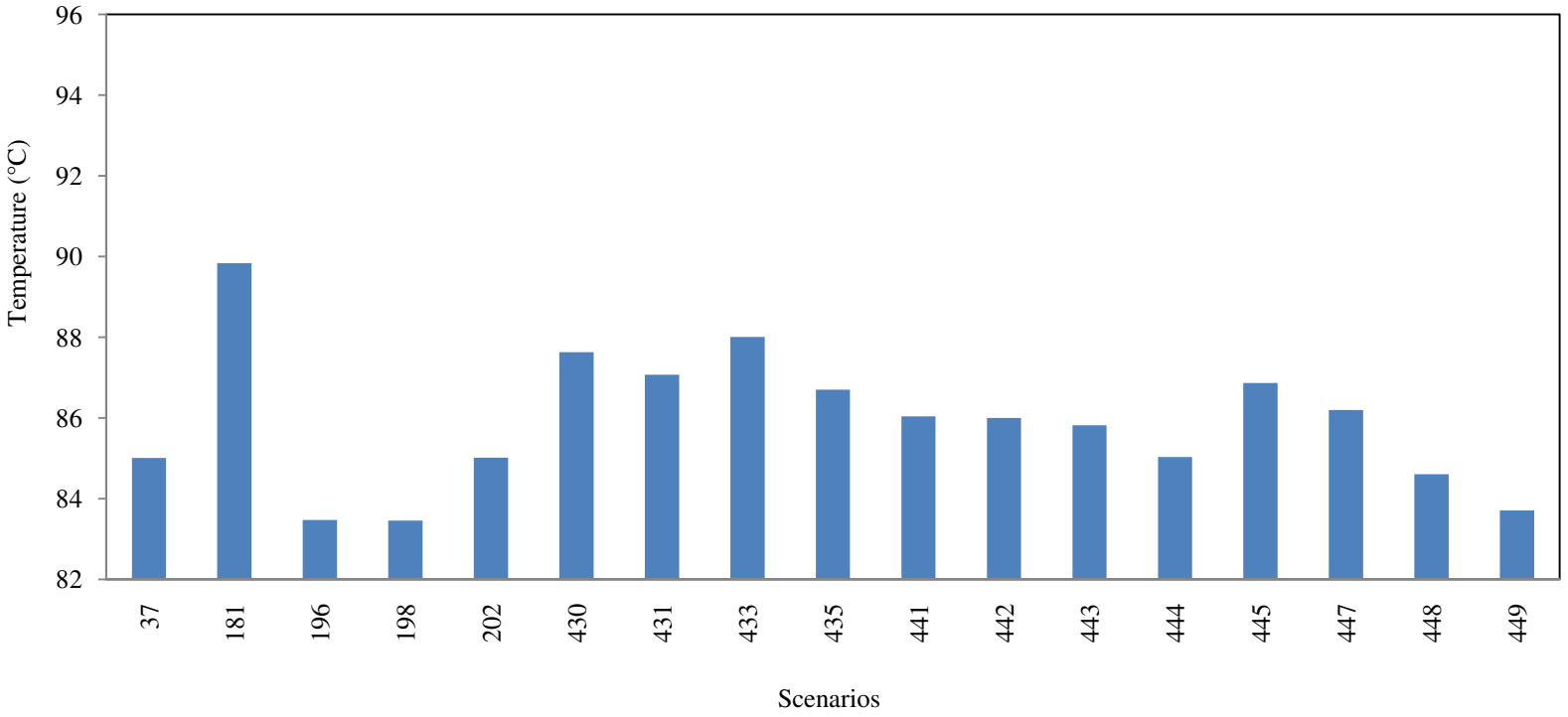


Figure 5.14 Maximum temperature of various scenarios for 10% penalty on performance

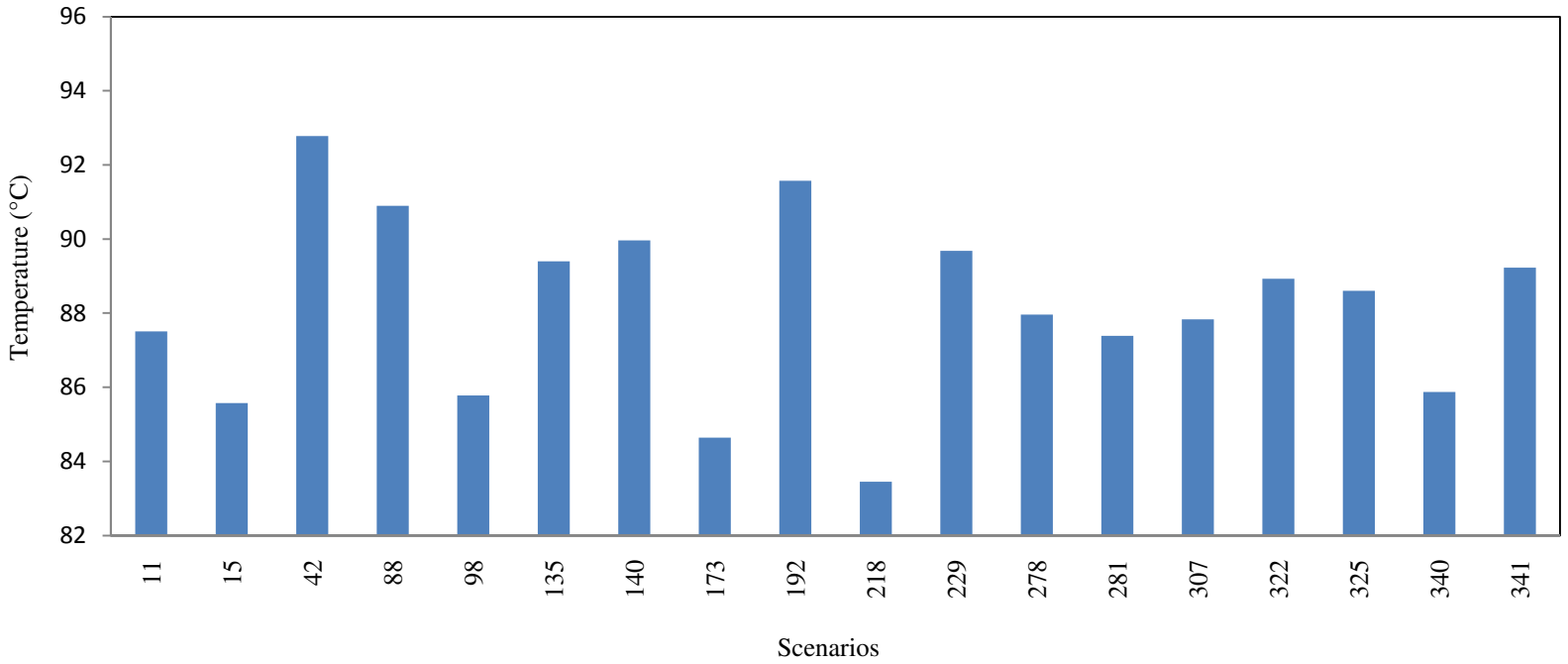


Figure 5.15 Maximum temperature of various scenarios for 25% penalty on performance

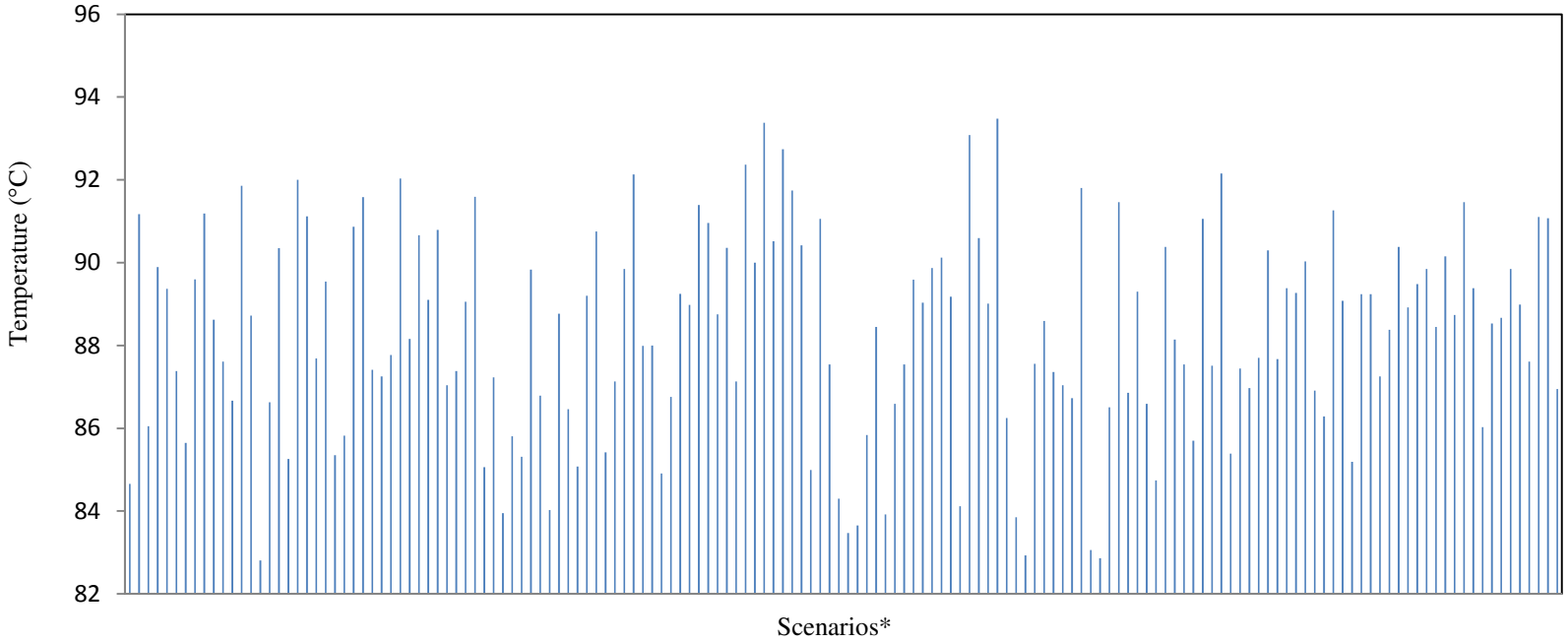


Figure 5.16 Maximum temperature of various scenarios for 30% penalty on performance
(Note: * Due to large number of data points, X-axis labels for plots are not mentioned)

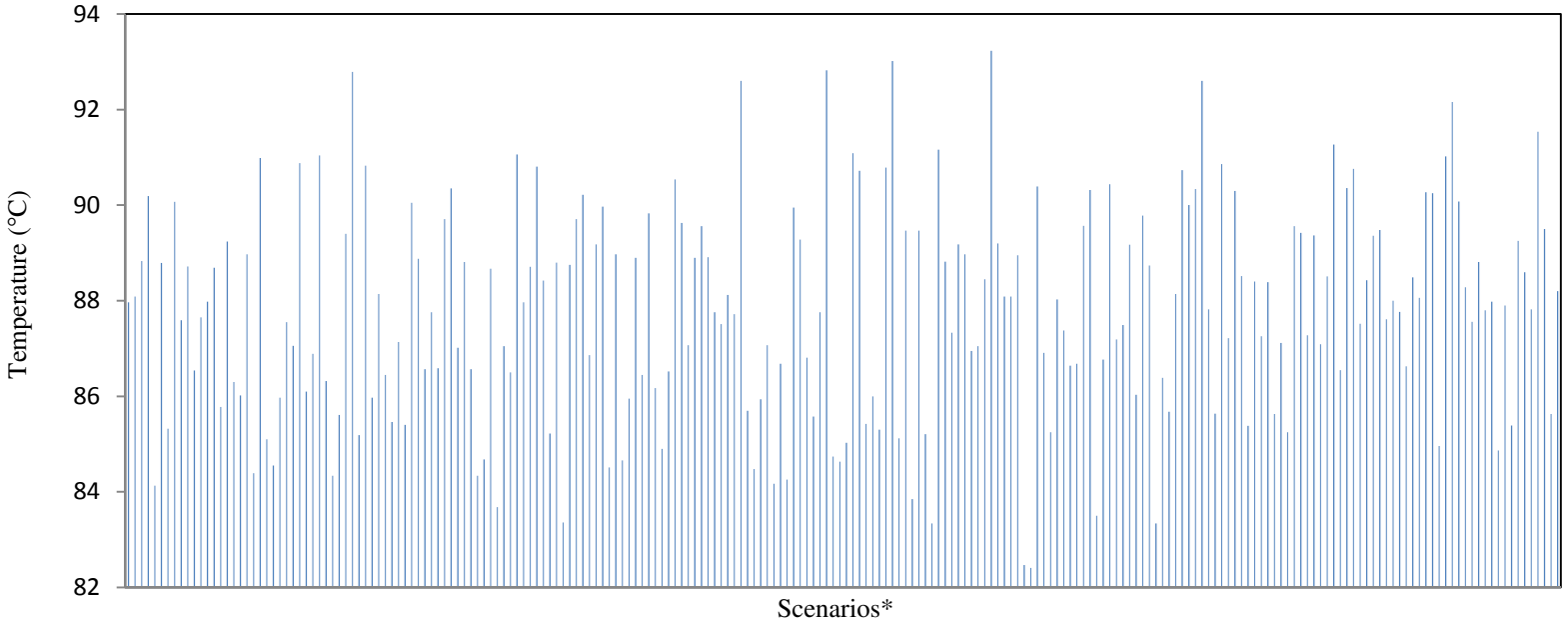
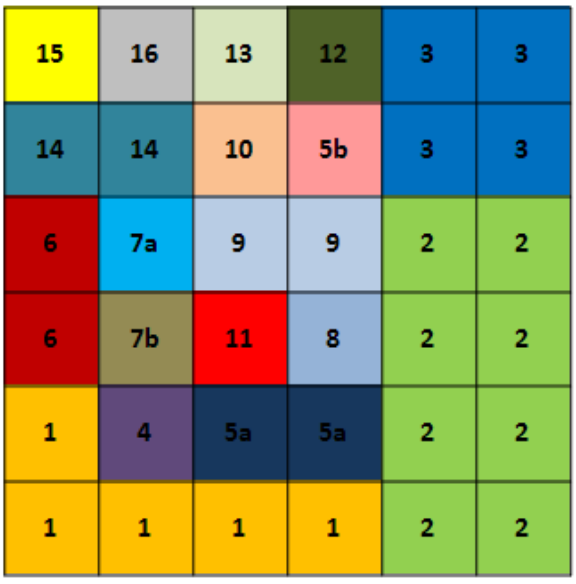


Figure 5.17 Maximum temperature of various scenarios for 25% penalty on performance

(a)



(b)

Figure 5.18 Original and optimized floor plan for Pentium IV architecture
(a) Baseline, (b) Optimized

Table 5.6 Minimum temperature for each penalty

Penalty (%)	Minimum Temperature (°C)
0	87.4
5	83.2
10	83.4
25	83.4
30	82.8
35	82.4

Figures 5.19 and 5.20 each represent one of the scenarios in which minimum and maximum temperatures were observed. In Fig. 5.19, two hot spots are observed while only one hot spot is observed in Fig. 5.20. This trend was noted for the scenarios with junction temperature less than 84°C and more than 93°C respectively. This can again be attributed to the location of functional blocks. When the high-power functional blocks are scattered, multiple regions of the die are subjected to high heat flux. This results in multiple hot spots. However, when they are clubbed together, a single hot spot (although at higher temperature) is noted. From cooling perspective, multiple hot spots are not a desirable condition.

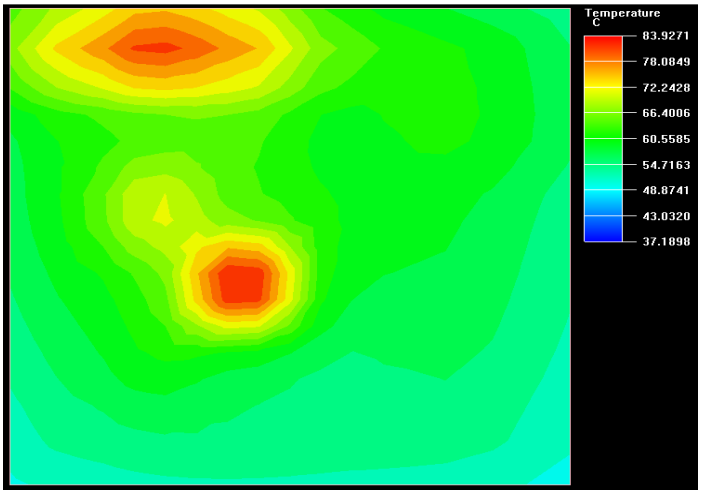


Figure 5.19 Temperature contour for one of the scenario exhibiting temperatures lower than 84°C

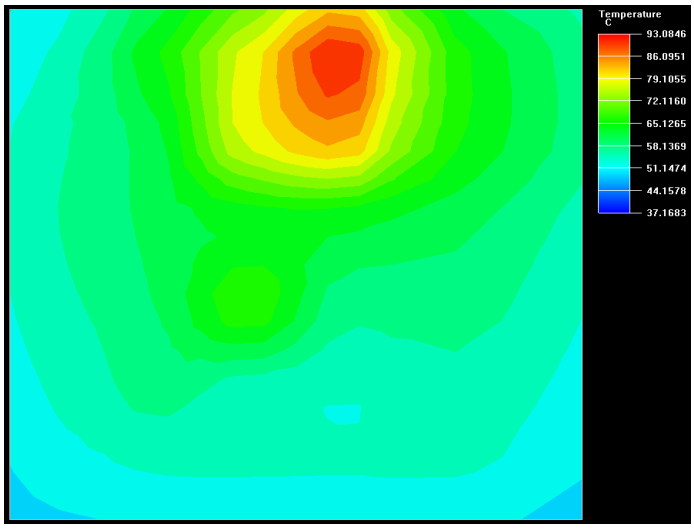


Figure 5.20 Temperature contour for one of the scenario exhibiting temperatures greater than 93℃

5.7.4 Summary

In the proof of concept, the various functional units of the Pentium IV micro-architecture were repositioned to minimize the junction temperature without, or only minimally, affecting the microprocessor performance. The die was divided into 36 equal blocks, which were then grouped based on their functionality to form 16 functional units. These 16 functional units are a representation of the Pentium IV architecture. Based on the size, selected functional units were repositioned and the results were evaluated. The results depicted a ΔT of 12℃ between the minimum and the maximum temperatures for a performance loss of 35% and 0% respectively. For scenarios depicting lower temperatures, multiple hot spots were observed. For scenarios depicting higher temperatures, single hot spots were observed. The optimum results were obtained by swapping the highest power block with the lowest power block. The optimized scenario from the formed DOE resulted in a temperature of 83.2℃ for a performance loss of 5%. However, the main objective was to emphasize that repositioning functional blocks may result in lower temperatures but at the same time it may also alter the processor performance. To further study the impact, a more in-depth analysis is performed which is discussed in the following section.

5.8 Multi-objective optimization of a non-uniformly powered die based on both thermal and device performance

In the proof of concept, the impact of relocating specific functional units on both thermal and device clock performance was mentioned. However, the analysis considered a limited number of scenarios and was based on the power map provided by Wu. et. all [99]. To further study the impact of co-architectural design, a power map was generated using MPTLism by Ghose [34] for 3 GHz clock speed. The die size was considered to be 146 mm^2 to specifically represent the 90 nm Pentium IV Northwood architecture for 3 GHz clock speed. An extensive analysis is performed to optimize the location of the functional units to minimize the junction temperature with minimal penalty on the clock performance.

5.8.1 Detailed Approach

A computational model similar to that mentioned earlier was considered except for the die size, power and the performance. The total power in this case is 60.2 W (against 94 W in the proof of concept) which is measured during any process.

The performance metric used for the processor is IPC, the number of instructions committed per cycle. This is a direct measure of the processor's throughput. The relocation of the functional blocks results in increased length of the interconnections which causes communication delays. These delays have two consequences:

1. An extra pipeline stage has to be added if the delays are significant compared to the processor's clock period.
2. If the delays are relatively small, they can be accommodated without any penalty.

In this analysis, it is assumed that an extra pipeline stage is added when the increase in the interconnection delay resulting from the relocation of a block exceeded 20% of the clock cycle time. Where the increase in the delay was higher than a single clock period, two or more pipeline stages were assumed to be added, depending on the magnitude of the increase. If the increase in the interconnection delay was less than 20% of the clock period, it is assumed that

the delay could be accommodated without any changes to the pipeline structure. The performance penalties are introduced when the additional pipeline stages are inserted to accommodate the increases in the interconnections. These additional stages impact the IPC adversely for two reasons. First, they tend to increase the time it takes to satisfy a data dependency within the program (from one instruction that produces a result to a following instruction that uses this result). Second, when a branch instructions are mispredicted, the penalty (in number of cycles) introduced from the need to flush instructions in the mispredicted path also goes up. This is because each extra pipeline stage added to the front end of the pipeline directly contributes to this delay.

The architecture still consists of core and the cache of the microprocessor. As shown in Fig. 4.7, it consists of 24 functional units. However, for the computational analysis, the die was divided into 36 blocks of equal areas. Depending upon the size, functional units in the numerical model are represented by one, two, three, four or six blocks. The placement and attributes of all 24 functional units are shown in Fig. 5.10 and Table 5.7, respectively.

Table 5.7 Attributes and power consumed by the different functional blocks represented in Figure 5.10

Block No.	Functional Unit	Power (W)	Area[1] (mm^2)
1a	Allocation	0.73	2.885
1b	Rename	3.15	3.846
1c	InstrQ1	1.14	4.74
1d	Scheduler	3.84	4.003
1e	InstrQ2	0.65	2.212
2	L2 cache	6.66	33.02

[1] Area of functional units defined in Table 2 is the actual area on 146 mm^2 die. For numerical solutions die was divided in 36 equal blocks of area 4.052 mm^2 each. Thus depending upon the number of blocks, area of each functional unit may vary in multiples of 4.052.

Table 5.7 *Continued*

3	Bus control	8.20	15.64
4	Retire	1.3	6.878
5a	Integer register	0.59	4.221
5b	Integer execution	1.24	3.898
6	UROM	1.67	5.77
7a	Fp register	1.13	4.586
7b	Fp execution	3.79	6.181
8	Memory control	0.29	1.474
9	L1 cache	5.55	9.153
10	Dtlb	0.71	4.469
11	MOB	9.42	2.649
12	ITLB	0.59	1.49
13	L2 Bpu	2.92	4.138
14	Trace cache	5.43	13.07
15	L1 Bpu	3.81	7.236
16	Instruction decoder	6.78	4.415

Each functional unit has a specific role to play and hence it is critical to place the functional units with similar roles near each other. Based on this and for convenience of analysis, the die was divided in four main groups:

- Group 1- Front-end (FE)
- Group 2- Execution cores (EX)
- Group 3- Bus and L2 (BL2)
- Group 4- Out-of Order Engine (OE)

Constituents of each group are detailed here and shown in Fig. 5. The number in parentheses indicates the block number for the numerical model:

- Group 1 includes L1_BPU (15), L2_BPU (13), Instruction decoder (16), Trace cache (14) and UROM (6).
- Group 2 includes Integer register (5a), Integer execution (5b), Fp register (7a), Fp execution (7b), Memory controller (8), L1_Cache (9), DTLB (10), MOB (11) and ITLB (12).
- Group 3 includes L2 Cache (2) and Bus controller (3).
- Group 4 includes Allocation (1a), Rename (1b), InstrQ1 (1c), InstrQ2 (1d), Scheduler (1e) and Retire (4). These groups are shown in Fig. 5.21.

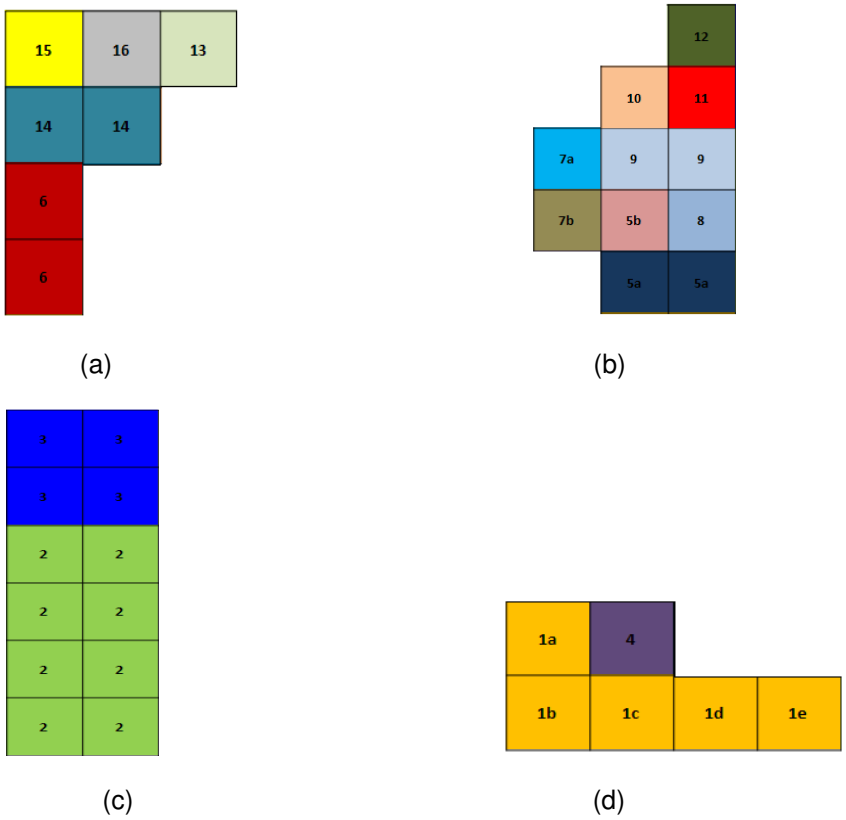


Figure 5.21 Functional groups of Pentium IV architecture (a) Group 1, (b) Group 2, (c) Group 3, (d) Group 4

5.8.2 Penalty on Performance

For the baseline case, the penalty on the performance was assumed to be zero. The power map in Table 5.7 and the performance loss reported in Table 5.8 were obtained from the micro architectural simulator (MPTLsim) which simulated over 200 million cycles. For the scenarios in which the performance was altered, a cumulative penalty is reported. For example, if FP register and FP execution are separated i.e. if these blocks are not placed adjacent in any direction (including diagonal), then the penalty on the performance is reported as 8%. If, in the same scenario, Integer register and Integer execution are also separated, then an additional 11% penalty is incurred and the cumulative penalty of 19% on the performance is reported. The penalties incurred due to the redistribution of a single functional unit are tabulated in Table 3. It should be noted that the blocks in a group must always remain together. Violating this constraint can impose a penalty of 25% or more. Also, the location of each group is also very critical. Groups 2 (EX) and 4 (OE) have to be adjacent. Separating Groups 1 (FE) and 4 (OE) will result in a performance loss of 18%. Hence, in the current analysis, any functional unit or group will not violate this rule.

Table 5.8 Penalty on performance incurred due to repositioning of function blocks

Group	**Blocks**	**Penalty (%)**
1	15 and 16	4
	15 and 14	4
	6 and 14	3
2	7a and 7b	8
	5a and 5b	11
	5b and 8	5
	9, 10 and 11	6
3	2 and 3	18
4	No serious performance loss2 and 3	<2

5.8.3 Objective

The objective of the current analysis is to optimize the location of the functional units to minimize the junction temperature with minimal penalty on the microprocessor performance. It should be noted that the location of the functional units is varied within the group. Inter-group relocation results in extremely severe performance penalties. The DOE formed is subjected to the following conditions:

- Any single functional unit cannot occupy more than one position for any given scenario of DOE.
- No two functional units can occupy the same position for any given scenario of DOE.
- Only functional units of same size can exchange positions.
- Total power on the die remains constant.

5.8.4 Results and Discussion

A steady-state thermal analysis was performed using a commercial CFD code. Before repositioning the functional units, it is necessary to analyze the baseline case (actual power map). This will identify the location of any hot spots. Figure 5.22 shows the temperature distribution for the baseline case (original floor plan) of the Pentium IV architecture. The maximum temperature was 60.1°C. From the temperature contours two hot spots are observed. These hot spots are due to the high powered block 16 (Instruction decoder, 6.78 W) and block 11 (MOB, 9.42 W). The hot spot due to block 16 measures about 55.5°C while the hot spot due to block 11 measures 60.1°C, which is also the global maximum temperature. Thus, intuitively relocating functional units from groups 1 and 2 may help in reducing the junction temperature.

The lowest achievable temperature would be for the scenario in which we have uniform power distribution. This will provide us the lower limit for the analysis. Figure 5.23 shows the temperature contours for uniform power distribution of 68.2 W. The maximum temperature noted is 48°C. Thus, the baseline scenario and the ideal scenario (uniform power) results in a

ΔT of 12.1℃. This justifies the need to consider non-uniform power distribution for high powered microprocessors. The effect of relocation on the junction temperature and the performance for each group is discussed below.

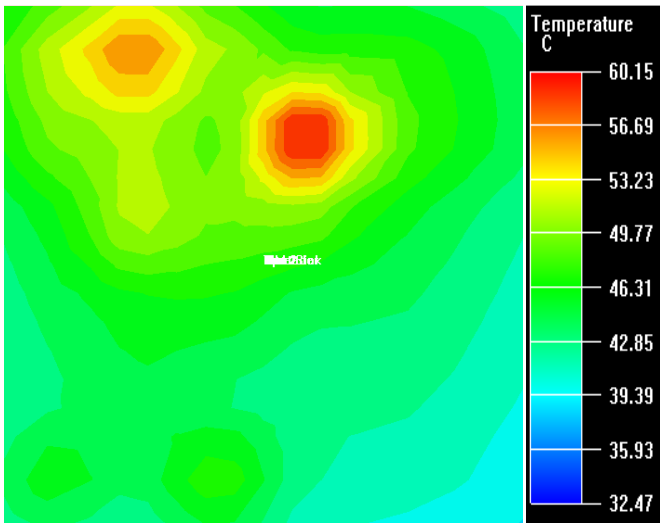


Figure 5.22 Temperature contours for the baseline scenario

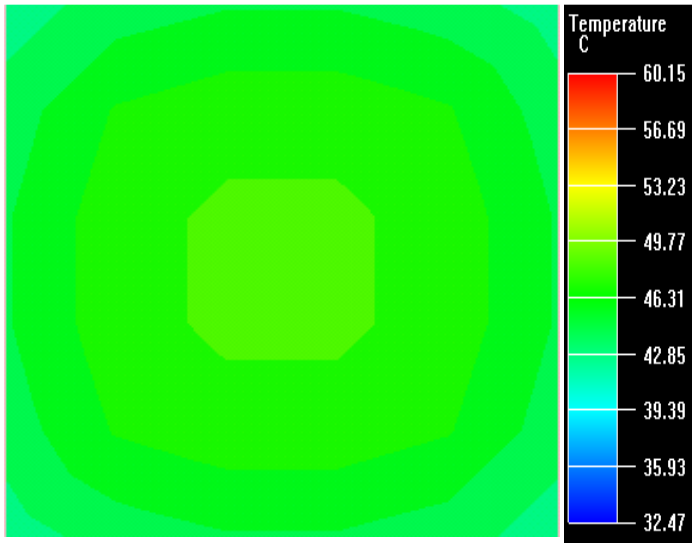


Figure 5.23 Temperature contours for uniform power distribution

5.8.4.1 Group 1: Front-End

As mentioned earlier, Group 1 includes L1_BPU (15), L2_BPU (13), Instruction Decoder (16), Trace Cache (14), and UROM (6). In all, 12 scenarios were simulated to study the effect of relocation of each functional unit in Group 1. It was mentioned earlier that for the baseline case, two hot spots were noted. One of them was due to block 16 and hence its temperature along with the maximum temperature is summarized in Table 5.9. It can be seen that, there is no variation in the maximum temperature which is observed at different location and is discussed later. However, a variation of about 2°C is observed for the temperature of block 16. Less temperatures were noted for the scenarios in which the block 16 was located in the corner, which isolated it from the other high powered blocks in Group 2. Also, swapping the location of block 6 with 14 (scenarios 7-12) results in drop of temperature by about 1°C with a performance loss of atleast 4%. It is critical to reduce not only the temperature but also the temperature gradient across the die. Large temperature gradients will have higher reliability concerns as it induces higher stress in the die. From Table 5.9, best case would be scenario 6 (block 16, temperature 57.3°C and minimal performance loss) in which functional units 15 and 16 are swapped. However, at this point it is difficult to comment about the optimized scenario for Group 1 as it depends on the global maximum temperature.

Table 5.9 Summary of temperature and performance loss for various scenarios in Group 1

Scenario	Maximum Temperature (°C)	Temperature of block 16 (°C)	Performance loss (%)
1	60.1	57.1	Minimal
2	60.5	57.1	4
3	60.6	57.4	Minimal
4	60.0	56.7	Minimal
5	60.1	56.5	4

Table 5.9 *Continued*

6	60.3	57.3	Minimal
7	60.0	56.4	4
8	60.3	56.6	8
9	60.4	56.9	4
10	59.8	55.9	4
11	59.8	55.6	8
12	60.1	56.5	4

5.8.4.2 Group 2: Execution Cores

Group 2 includes Integer register (5a), Integer execution (5b), Fp register (7a), Fp execution (7b), Memory controller (8), L1 cache (9), DTLB (10), MOB (11) and ITLB (12). Number of scenarios by relocating functional units represented by single block is *7!* i.e. 5,040. In addition, there are two functional units that are represented by two blocks (5a and 9) resulting in two scenarios. Thus, the total number of scenarios analyzed for this group is 10,080 (2 x 5,040). For such a large set, the results are summarized in two Tables, 5.10 and 5.11. Table 5.10 summarizes the number of scenarios for a specific temperature range. This is particularly important as it will give the design engineer a flexibility to choose an appropriate layout out of all possible number of design layouts for a particular temperature requirement. Table 5.11 summarizes the thermal performance for various performance loss.

Table 5.10 Summary of scenarios for corresponding temperature range

Temperature Range (℃)	Number of Scenarios
56-57	24
57.1-58	18
58.1-59	1,094
59.1-60	3,238

Table 5.10 *Continued*

60.1-61	3,186
61.1-62	2,258
>62	262

Table 5.11 Summary of thermal performance based on performance penalty

Performance Penalty (%)	**Minimum Temperature (℃)**	**Maximum Temperature (℃)**	**No. of Scenarios**
0 (No serious performance loss)	58.6	63.3	128
5	58.8	62.2	364
6	58.6	63.3	448
8	57.6	62.7	182
11	58.6	62.2	954
13	57.7	62.2	446
14	56.6	62.2	628
16	58.6	62.2	400
17	58.6	62.2	770
19	56.6	62.2	1,774
22	58.6	62.2	832
24	58.6	62.2	560
25	58.6	62.2	936
30	58.6	62.2	1,658

From Table 5.11 it can be seen that, maximum number of scenarios depicts temperatures greater than the baseline case. The best case scenario depicted junction temperature of 56.6℃ whereas the worst case scenario depicted junction temperature of 63.3℃. After careful review of all the scenarios it was observed that location of functional block 11(MOB) plays a key role in determining the maximum temperature. For the scenarios in which

the functional block 11 is placed at its original location, temperatures greater than 60℃ are noted. Similar phenomenon is observed when block 11 is placed at the original locations of functional units 10 and 12. This is particularly because of the high power blocks like 3 (8.2 W), 9 (5.5 W) and 16 (6.78W) in the neighborhood. For the remaining scenarios higher temperatures are observed if functional unit 7b (FP Execution) which is the second high power block after block 11 in Group 2, is located in the neighborhood of functional block 11. There are 12 scenarios which depicts temperature of 56.6℃. For all these 12 scenarios, the functional unit 11 is placed at the original location of functional unit 8 where it is well isolated from aforementioned high power blocks. However, the minimum penalty incurred is 14%. Minimum and maximum temperature along with number of scenarios for all the penalties is summarized in Table 5.11.

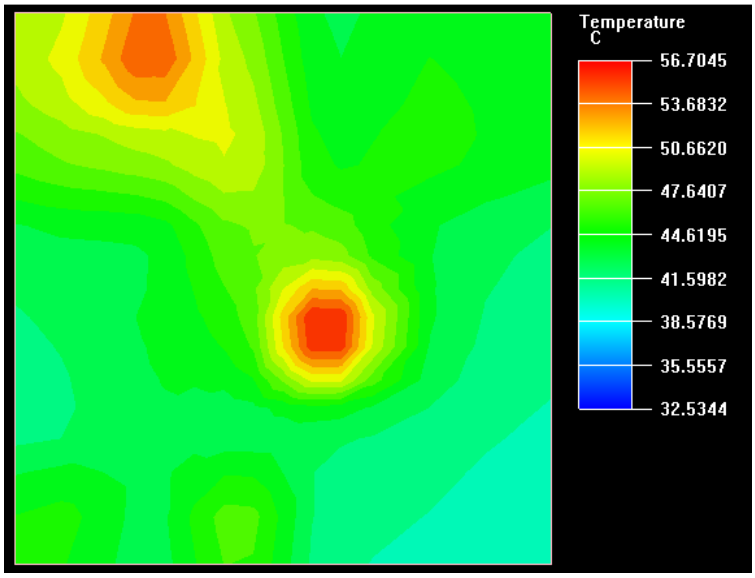
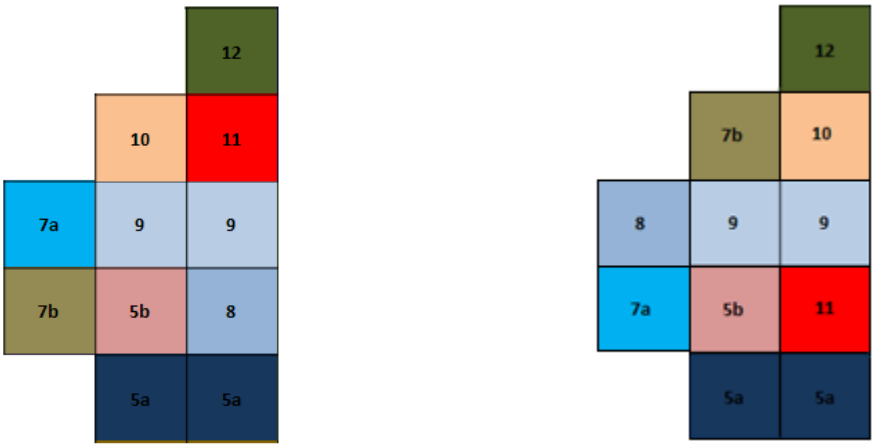


Figure 5.24 Temperature contours and the corresponding functional unit location for one of the scenarios depicting junction temperature less than 57℃



(a) (b)

Figure 5.25 Original and new (corresponding to Fig. 5.19) locations of functional units in Group 2 (a) Original location, (b) New/optimized location

Figure 5.24 shows the temperature contours for one of the scenarios depicting temperatures less than 57℃. Figure 5.25 shows original and new location (corresponding to Fig. 5.24) of functional units in Group 2. From the Fig.5.24 it is evident that multiple hot spots are observed irrespective of the location of functional unit 11. From cooling perspective, multiple hot spots are not a desirable condition. Also, maximum global temperature is still observed at the location of functional unit 11. This indicates that even if the location of functional units placed in other groups (1, 3 and 4) is changed, the global maximum temperature will not go below 56.6℃.

5.8.4.3 Group 3: Bus and L2

As the name suggests this group includes Bus(3) and L2 cache (3) which constitutes about 33.3% of the total die area. Swapping the locations of blocks 2 and 3 did not alter the temperature and performance of the baseline scenario.

5.8.4.4 Group 4: Out-of-Order Engine

This group includes functional units Allocation (1a), Rename (1b), InstrQ1 (1c), InstrQ2 (1d), Scheduler (1e) and Retire (4). In all, 720 (6!) scenarios were simulated to study the effect of relocation of each functional unit in Group 4. As mentioned in Table 5.8, relocating functional

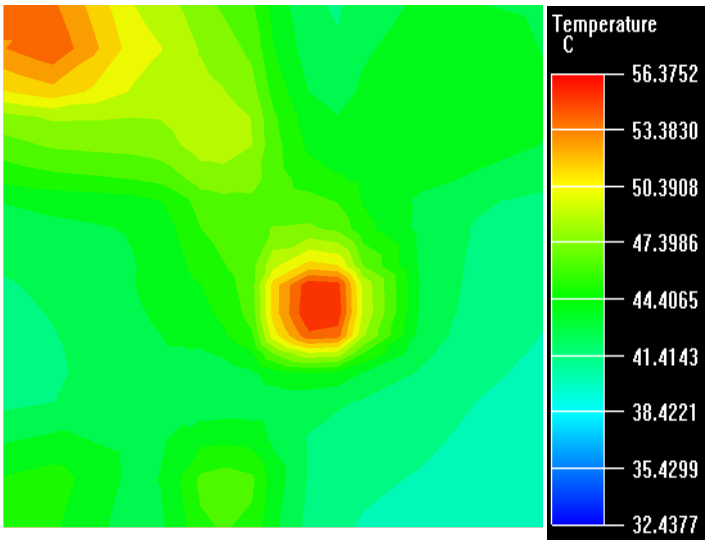
units in this group does not incur any performance loss. After reviewing the thermal performance for all the scenarios, the variation in temperature was merely 0.3°C (minimum noted temperature: 60.0°C). This implies that, functional units of Group 4 does not impact the thermal as well as clock performance of the die.

Thus, from both the thermal and performance perspective, location of functional units in Groups 2 and 1 are critical respectively. Based on each scenario it can be concluded that for effective thermal management, the high power blocks should be scattered and preferably located at the periphery. This would reduce the spreading resistance and help in achieving lower junction temperature. In Group 2, the scenario which depicted temperature of 56.6°C for a performance loss of 14% along with scenario 4 of the Group 1 may be considered as the optimized scenario. This would lower the junction temperature as well as thermal gradient. Figure 5.26 shows the relocated functional units along with the temperature contours for the same.

It was mentioned earlier that the two hot spots observed are due to functional units 11 (MOB, 9.42 W) and 16 (Instruction Decoder, 6.78W). However, from Table 5.7 it can be seen that functional units 2 (L2 Cache, 6.66 W), 3 (Bus Ctl, 8.2 W), 9 (L1 Cache, 5.55 W) and 14 (Trace Cache, 5.43 W) dissipate powers comparable to functional units 11 and 16. Inspite of that, location of functional unit 11 is critical. This can be attributed towards the heat flux. For functional units 11 and 16, heat fluxes are 2.26 W/mm^2 and 1.64 W/mm^2 respectively. On the other hand heat fluxes for functional units 2, 3, 9 and 14 are 0.2 W/mm^2, 0.5 W/mm^2, 0.67 W/mm^2 and 0.69 W/mm^2 respectively.

For the current analysis, power dissipated by each functional block was estimated for 3 GHz clock speed and 90 nm technology. For higher clock speeds, power dissipated by each block would increase by a certain factor say 'x'. This would correspond to the increase in the heat flux by a factor of 'x'. Therefore, for 3 GHz clock speed, if ΔT of 5.7°C (between best and worst scenario) is observed, then for higher clock speeds the ΔT observed would also increase

by the same factor, 'x'. Also, the manufacturing technology (45nm, 26nm and 11nm) will have significant impact on the thermal performance of the processors. For example, for one of the Intel processors (P4 Prescott architecture), for 3.8 GHz clock speed, the thermal design power is 115W [35] against 60.2W considered in the above analysis.



(a)

16	15	13	8	3	3
14	14	7b	10	3	3
6	12	9	9	2	2
6	7a	5b	11	2	2
1a	4	5a	5a	2	2
1b	1c	1d	1e	2	2

(b)

Figure 5.26 Temperature contour and location of functional units for the optimized scenario (a) Temperature contour, (b) Location of functional units

5.9 Summary

In this work, functional units of the Pentium IV micro-architecture were repositioned to minimize the junction temperature without, or only minimally, affecting the microprocessor performance. The die was divided in 36 equal blocks. Based on their functionality, these blocks were grouped to numerically represent the actual 24 functional units. Based on the functionality of each unit, they were categorized in four groups namely Front-end (FE), Execution-cores (EX), Out-of-Order engine (OE) and Bus and L2 (BL2). Numerical analysis was performed using a commercially available CFD code to optimize the location of the functional units for improved thermal management. The results of over 10,000 scenarios depicted a ΔT of 5.7°C between the minimum and the maximum temperatures. Performance penalties ranged from minimal (less than 2%) to 30% (cumulative). From thermal perspective, location of the functional units in Groups 2 and 1 is most critical. Location of the functional units in Groups 3 and 4 do not have any impact on the junction temperature as well as on the device performance. In Group 2, location of high power block 11 is most critical. For lower junction temperatures, it is desirable to scatter the high power units and preferably place them at the periphery. Most of the scenarios depicted multiple hot-spot, which from cooling perspective, is not a desirable condition. Also, the thermal performance of any micro-architecture depends on the heat flux rather than the power dissipated by individual functional units. From the results, the minimum and the maximum temperature was 56.6°C and 62.2°C. The temperature difference will vary depending upon the type of architecture, clock speed, bus speed and cache size. Based on the analysis, optimized scenario resulted in a junction temperature of 56.6°C for a performance loss of 14%. The aforementioned analysis can be effectively used to estimate the thermal performance for microprocessors based on 45nm, 26nm and 11 nm technologies. This methodology can be used for the design of cost effective cooling technologies for future high end processors.

CHAPTER 6

CONCLUSION

Almost 55% of all the electronics fail due to improper thermal management. Thus, thermal management plays an key role in current as well as in the development of new technology. For all electronic devices, reliability and performance can be improved by decreasing its operating temperature. Every device is different and thus requires different cooling strategies for effective thermal management. These cooling strategies can be implemented at system (or facility), package and die level. In this work, for the thermal management at the facility level, data centers were considered. At the package level a 3D package architecture is considered and at the die level effect of non-uniform power distribution was considered for a Pentium IV microprocessor. Thermal management at all the aforementioned levels is further summarized below.

As mentioned earlier, at facility level, data centers were considered. The growth in server systems power trend has made thermal management of data centers a very challenging task. These rising heat load trends in data center facilities have raised concerns over energy usage. The environmental protection agency has reported that the energy used in 2006 by data center industry was 1.5% of the total energy usage by entire nation. By year 2010, this usage will approach 2% of the annual energy use nationwide. In order to reduce the energy consumption, especially by the cooling infrastructure, air side economizers are used. In air side economizer, the conventional air conditioning units are replaced by air handling units, which use the ambient air (provided the temperature is within the permissible limits, typically less than 25°C) to cool the electronics. This reduces the energy consumption by about 68%. In the analysis performed, a methodology was proposed to computationally estimate the impact of air side economizers on

the energy consumption. The analysis was based on four different layouts but can be used for any generic data center layout.

At package level, a 3D architecture was considered. In 3D packaging, various units such as computational processing units (CPUs), memory, logic, RF antennas are stacked on each other. In the study performed, a PoP architecture is considered. The top package consisted of two memory dice stacked on each other. The bottom package was a flip-chip package with a logic die. The two packages were connected via BGA. Eleven different scenarios were taken into consideration for the numerical analysis. The power on memory dice was varied from 0.1 W to 0.3 W in step of 0.1 W. The power on the logic die was varied from 1 W to 3 W in step of 1 W. The analysis showed that almost 92% of the heat is dissipated through PCB while rest of the heat is dissipated through mold cap and substrate sides. As the power on logic die was greater than memory die by an order of magnitude, maximum temperature was always noted for the bottom package. However, in a scenario, where the power on all three dice was 1 W, maximum temperature was noted on the top package. It was also shown that, by using PCB with high thermal conductivity, maximum temperature of the package can be reduced significantly.

From the results, it was also concluded that the only path through which the heat from the packages is conducted to PCB is through the C4, C5 and BGA solder interconnects. At elevated temperatures and under higher operating current, interconnects are subjected to a catastrophic failure known as electromigration. As a result of electromigration, voids are formed which offer very high thermal resistance to the heat flow. This may reduce the interconnect (and hence the device) reliability. In order to improve the device reliability, two different non linear analysis were performed. Results of the two were then combined to develop a robust design guidelines.

First, a full factorial DOE was formed to study the effect of Al trace thickness, UBM thickness, UBM diameter and PO diameter on current density in Al trace and the bump.

Maximum current crowding was always observed in the metallization. In the metallization, the most important design attribute found was the Al trace width. In the solder bump, the most important parameters that were found to be are the Al trace width and the UBM thickness. Solder configuration with Al trace of 60 µm, UBM thickness of 7 µm, UBM diameter of 120 µm and PO diameter of 60 µm yielded minimum current density in Al trace. Whereas, solder configuration with Al trace of 10 µm, UBM thickness of 7 µm, UBM diameter of 120 µm and PO diameter of 60 µm yielded minimum current density in bump. In the metallization, the current density varied from $5x10^5$ A/cm^2 to $7x10^5$ A/cm^2 and from $2.5x10^6$ A/cm^2 to $3.5x10^6$ A/cm^2 for operating current of 0.1 and 0.5 A per bump, respectively. In the solder, the current density varied from $2.8x10^3$ A/cm^2 to $4.2x10^4$ A/cm^2 and from $1.4x10^4$ and $2.1x10^5$ A/cm^2 for operating current of 0.1 and 0.5 A per bump, respectively. In general, larger trace width and UBM thickness while smaller UBM diameter and PO diameter yields minimum current density.

In a follow-up study, a full factorial DOE was formed to study the stresses induced in the bump due to reflow process as a function of attributes of the package architecture. The package architectural attributes such as die thickness, die size, substrate thickness, substrate size and PO size were studied in detail. For all the legs, the maximum stress was always noted at the corner bump. The packages with thick substrate exhibited higher stress than packages with thin substrate. Bumps with small PO size exhibited higher stress than the bumps with large PO size. For bumps with small PO size, the stress contours are lateral bands where as in case of bumps with large PO size, high stress is noted at the periphery and diminishes towards the center. The packages with thick die yielded higher stress than packages with thin die. The effect of ratio of substrate size to die size (between 1.5 and 2) on the stress induced in the bump at the PO is insignificant. Stress in the PO is directly proportional to the DNP. However, the effect of PO size is insignificant for the center bumps. Based on two studies, it can be concluded that the packages with thin substrate, thin die and center bumps (to be used as electrical interconnects for high current) with small PO and peripheral bumps (to be used for thermal

dissipation or low current electrical interconnects) with large PO may improve the device reliability.

At die level, effect of location of non-uniform power distribution on the junction temperature and device performance was studied. In the study performed, functional units of the Pentium IV micro-architecture were repositioned to minimize the junction temperature without, or only minimally, affecting the microprocessor performance. The die was divided in 36 equal blocks, which were then grouped based on their functionality to numerically represent the actual 24 functional units. Based on the functionality of each unit, they were categorized in four groups namely Front-end (FE), Execution-cores (EX), Out-of-Order engine (OE) and Bus and L2 (BL2). Numerical analysis was performed using a commercially available CFD code to optimize the location of functional units for improved thermal management. The results of over 10,000 scenarios depicted a ΔT of 5.7°C between the minimum and maximum temperatures. Performance penalties ranged from minimal (less than 2%) to 30% (cumulative). From thermal perspective, location of functional units in Groups 2 and 1 is critical. Location of functional units in Groups 3 and 4 do not have any impact on junction temperature as well as on device performance. In Group 2, location of high power block 11 is most critical. For lower junction temperatures it is desirable to scatter the high power units and preferably place them at the periphery. Most of the scenarios depicted multiple hot-spot, which from cooling perspective is not a desirable condition. Also, the thermal performance of any micro-architecture depends on the heat flux rather than the power dissipated by individual functional units. From the results, the minimum and the maximum temperature was 56.6°C and 62.2°C. The temperature difference will vary depending upon the type of architecture, clock speed, bus speed and cache size. Based on the analysis, optimized scenario resulted in a junction temperature of 56.6°C for a performance loss of 14%. However, it is to be noted that the optimized scenario will change depending upon the requirements. For example, in the afore mentioned scenario, temperature was the most important criteria and then the performance penalty. Temperature was considered

as a deciding parameter because it affects both reliability and performance. Also, lower junction temperature improves the microprocessor performance. Some applications may require better performance, in which case the scenario with minimal penalty would be the deciding criteria. Also, it can be seen that, for a given combination of temperature and performance, several scenarios exists. This gives the design engineer flexibility in designing the microprocessor for manufacturability. The aforementioned analysis can be effectively used to estimate the thermal performance for microprocessors based on 45nm, 26nm and 11 nm technologies. This methodology can be used for the design of cost effective cooling technologies for future high end processors.

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