ISSUES IN FRONT-END ENGINEERING OF CMOS NANOELECTRONICS

by

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ABSTRACT

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Several issues exist in current CMOS front-end engineering such as interfacial layer formation at high-*k*/Si interface, high metal/Si contact resistance in source and drain regions, and absence of a quantitative model for silicon-germanium alloy growth. In this dissertation, monolayer Se passivation is employed to create a Si (100) surface free of dangling bonds. Since dangling bonds are the origins of surface reaction sites and surface states, interfacial layer formation at high-*k*/Si interface can be suppressed and metal/Si contact resistance can be lowered by Se passivation. Firstly, results on interface engineering between HfO_2 and n-type Si (100) with Se passivation are reported. HfO_2 on Se-passivated sample by dry oxidation at 300°C shows much improved properties: a smaller *EOT* (equivalent oxide thickness) 31 Å compared with

EOT 65 Å for control sample, and a smaller leakage current with about 2 order of magnitude lowering. These results indicate Se passivation can effectively suppress the interfacial layer formation at the HfO_2/Si interface and reduce the gate leakage current. Secondly, experimental results for Ti/n-type Se-passivated Si (100) contacts are presented. The sheet resistance of Se-passivated 10^{19} cm^{-3} doped n-type Si (100) shows a 30% reduction as compared with control (non-passivated) samples. The extracted contact resistance decreases by about one order of magnitude. Up to 29 times reduction in contact resistivity is achieved by Se passivation on heavily-doped n-type SOI substrates. Finally, a kinetic model is proposed for $Si_{1-x}Ge_x$ growth from SiH_4 and GeH_4 by chemical vapor deposition (CVD). Growth behaviors like growth rate and Ge content are discussed by considering both the heterogeneous and homogenous reactions. The model agrees well with the experimental data.

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CHAPTER 1

INTRODUCTION

Since the first transistor devised by John Bardeen[1] in 1947 and the first integrated circuit invented by Jack Kilby[2] in 1958, the rapid development of computer and communications technology has catapulted electronics to its current status as the dominant global industry. Exploitation of electron and hole conduction in silicon has resulted in electronic memory and logic circuits such as dynamic random access memory (DRAM) and the microprocessor. Especially during the last 20 years, there has been rapid progress in the complementary metal-oxide-semiconductor (CMOS) integrated circuit technology. This has pushed the IC industry to its highly-developed age. The demand for greater integrated circuit functionality and performance (such as high speed and low static power consumption) at lower cost requires an increased circuit density, which has translated into a higher density of transistors on a wafer. This integration trend had been successfully projected by Gordon Moore[3,4] in 1965 that the growth of the number of transistors per chip quadruples every two years, subsequently modifying to about three-to-four years in 1995 which is well recognized as Moore's Law and is shown in Figure 1.1. In early 2006, Intel groups published their test static random access memory (SRAM) chips using a 45 nm process with an integrated density of over 1×10^9 transistors/chip. Compared with previous 65 nm process technology, this process technology offers more than 20% enhancement in transistor switching speed or

more than a five-fold reduction in transistor current leakage, and more than 30% reduction in transistor switching power, which show the latest but not final improvement of the transistor performances.

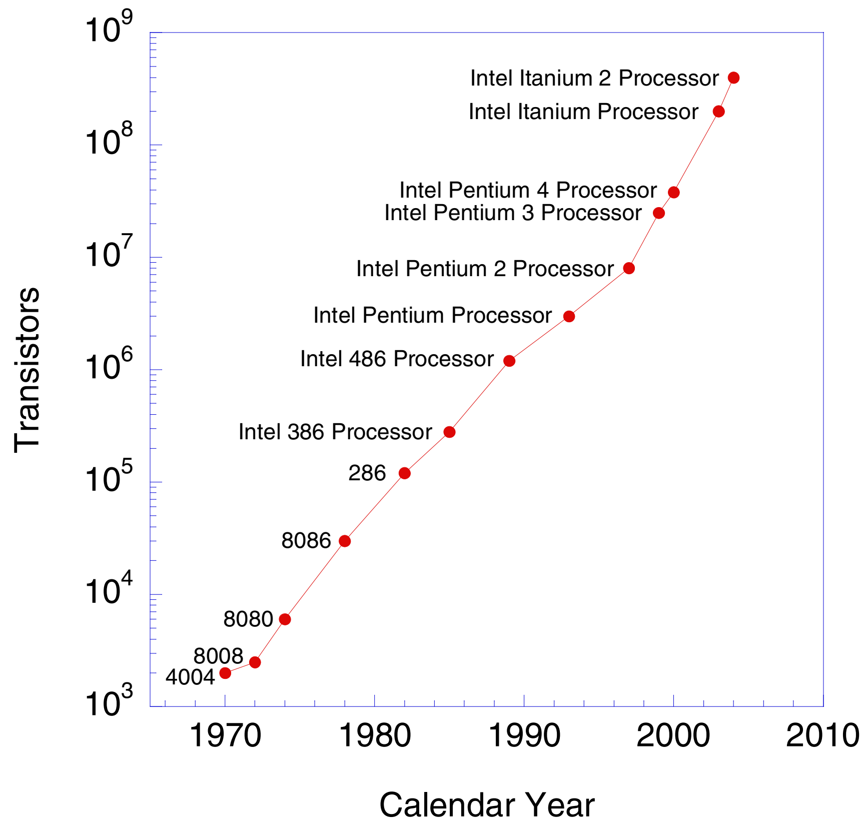


Figure 1.1 Projections of transistors per chip by Moore's Law.

The high transistor integrated density towards high circuit functionality and performance is accomplished by reducing the feature size of the active device in the circuit (called down-scaling),[5-7] which can be clearly seen by the performance metrics shown below. For a CMOS circuit, the dynamic response, or the switching response time, is given by[8]

$$\tau = \frac{C_L V_{DD}}{I_D} \quad (1.1)$$

where C_L is the load capacitance, V_{DD} is the supply voltage, I_D is the drive current. The switching response time gives the delay for the signal transportation from the upper logic level to the lower logic level. Eq. (1.1) indicates that to reduce the switching response time, the drive current should be increased. By considering a simple model for the drive current associated with a MOSFET, in the ohmic region, the drive current I_D can be written as[8]

$$I_D = \frac{W}{L} \mu C_{gate} (V_{GS} - V_T - \frac{V_{DS}}{2}) V_{DS} \quad (1.2)$$

where W and L are the width and length of the transistor channel, respectively, μ is the channel carrier mobility, C_{gate} is the gate capacitance, V_{GS} and V_{DS} are the voltage applied on gate and drain, and V_T is the threshold voltage. Eq. (1.2) shows the drain current is proportional to the average charge across the channel and the average electric field (V_{DS}/L) along the channel direction. Initially, I_D increases linearly with V_{DS} and then eventually saturates to a maximum when $V_{Dsat} = V_{GS} - V_T$ to yield

$$I_{Dsat} = \frac{W}{2L} \mu C_{gate} (V_G - V_T)^2 \quad (1.3)$$

By considering the gate dielectric as a parallel plate capacitor, the gate capacitance is given as

$$C_{gate} = A \frac{\varepsilon_0 k}{t} \quad (1.4)$$

where A is the capacitor area, k is the gate oxide relative dielectric constant, ε_0 is the

free space permittivity and t is the gate dielectric thickness. Eq. (1.3) and Eq. (1.4) indicate that drive current can be increased by either reducing the channel length or increasing the gate capacitance by reducing the thickness of the gate dielectric, which is recognized as down-scaling. The conventional SiO_2 gate dielectric thickness has proceeded from the range of 75~100 nm for the 4K DRAM in 1974 to 1.1 nm for today's leadership MPU in 2005. Likewise, the physical gate length has decreased from 7.5μm for the 4K DRAM to a physical gate length of about 35 nm for the MPU at the 90 nm technology generation. Figure 1.2 shows the projections by ITRS 2005[9] (International Technology Roadmap for Semiconductor) of physical gate length and gate equivalent oxide thickness (*EOT*) for both high-performance and low standby-power devices, which gives the tendency for the future CMOS transistor generations. It indicates that CMOS technology has already stepped into the nanometer era.

However, in the past several years it has become clear that despite advances in these crucial process technologies and the resultant ability to produce ever-smaller feature sizes, front-end process technologies have not kept pace, and scaled device performance has been compromised. The rapid shrinkage of the feature size has forced the CMOS industry to face several problems in the traditional transistors such as high gate leakage current, high source/drain parasitic resistances and channel mobility degradation, etc. The crux of these problems comes from the fundamental materials used in traditional transistors. Silicon, silicon dioxide and silicide, have been pushed to their fundamental material limits and continued scaling requires the introduction of new

materials.

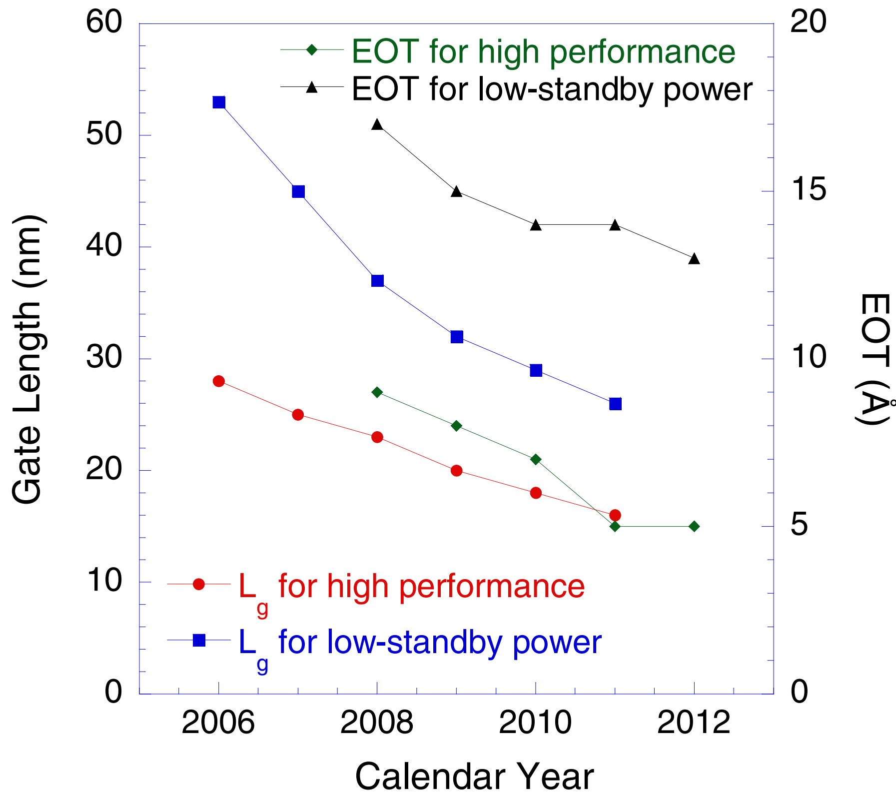


Figure 1.2 2005 ITRS projections of physical gate length and *EOT* for both high performance logic and low-standby power devices.[9]

In summary, an introduction is given in Chapter 1. Three issues in current CMOS front-end engineering are addressed in Chapter 2. Chapter 3 presents the surface passivation on Si (100) surface by monolayer Se atoms. Chapter 4 gives the experiments and results of HfO_2 on Se-passivated n-type Si (100). Chapter 5 shows the experiments and results of low resistance Ti/n-type Si (100) contacts by Se passivation. In Chapter 6, a kinetic model for $Si_{1-x}Ge_x$ growth from SiH_4 and GeH_4 by CVD is proposed. Conclusion and future scopes are given in Chapter 7.

CHAPTER 2

CHALLENGES IN TRANSISTOR FEATURE SIZE DOWN SCALING

Several issues associated with the transistor feature size down scaling exist within current CMOS front-end technology, such as high gate leakage current due to the thin gate SiO_2 film, high source/drain parasitic resistance with smaller transistor dimension, and electron/hole mobility degradation at the surface of the channel, which have already restricted the extension and development of IC industry to even greater functionality and higher performance. High dielectric constant (high-k) materials have been investigated to replace SiO_2 as the gate material. However, continued research is needed before using them as the gate materials. A significant part of the source/drain parasitic resistances is the metal/Si contact resistance. This emerges as the dominant component with the transistor feature size down scaling. Research works and techniques towards lowering the metal/Si contact resistance must be studied and developed to meet the future requirement on source/drain parasitic resistance. Strained-Si technology has been successfully applied to current CMOS technology to enhance the transistor surface channel mobility. Since the Ge content in the strained-Si plays a key role to determine the mobility enhancement, a quantitative and comprehensive kinetic model for SiGe alloy (Strained-Si) growth is needed.

2.1 High Gate Leakage Current

The key element enabling the scaling of Si-based metal-oxide-semiconductor field effect transistor (MOSFET) is the gate dielectric material used to isolate the transistor gate from the Si channel in CMOS devices for decades: silicon dioxide (SiO_2). The amorphous silicon dioxide is the most commonly used material as the gate dielectric since it offers several key advantages such as large band gap (E_g ~ 8.9 eV), large band offsets with Si (ΔE_c = 3.1 eV, ΔE_v = 4.6 eV), high hard breakdown fields of 15 MV/cm, low surface states density at the Si/SiO_2 interface (D_{it} ~ 1-3×10^{10}/eV·cm^2), good thermal stability and well-established fabrication processes. However, with the increase in transistor integration density and resultant decrease in transistor feature size, SiO_2 has already been pushed to its fundamental limitations as the gate dielectric.

2.1.1 Limitations of SiO_2 as the Gate Dielectric Layer

With the down scaling of the feature size, the thickness of the gate SiO_2 turns much thinner than before. As shown in Figure 1.2, the required gate dielectric thickness has already reached below 12 Å with SiO_2 as the gate material. Previous works[10-12] indicate that the CMOS devices with SiO_2 gate oxide thinner than 10~12 Å result in no gains in transistor drive current. Therefore, 10~12 Å could serve as a practical limit for reducing the SiO_2 thickness.[13, 14] Besides, there are two main issues that remain with such a thin SiO_2 film. Firstly, the gate leakage current will increase dramatically due to direct tunneling through the thin SiO_2 film. This is shown below [15]

$$J_{DT} = \frac{A}{t_{gate}^2} \exp\left(-2t_{gate} \sqrt{\frac{2m^* q}{\hbar^2} (\Phi_B - \frac{V}{2})} \right) \tag{2.1}$$

where A is a constant, t_{gate} is the gate physical thickness, m^* is the electron effective mass in SiO_2, $\hbar$ is the Planck constant, Φ_B is the barrier height, and V is the voltage drop across SiO_2. Eq. (2.1) indicates that thin SiO_2 will promote the increase of the gate leakage current, and sequentially increase the static power consumption. This undesired gate leakage current degrades the device reliability since the IC design rules generally assume no appreciable gate current. Secondly, the traditional CMOS transistor usually uses poly-Si with boron highly-doped as the gate electrode. Thin SiO_2 will enhance boron diffusion from the poly-Si gate electrode into the surface of Si substrate (called boron penetration) during thermal annealing in the fabrication process. This will result in a higher concentration of boron in the channel region, which changes the channel doping level and causes instability in the threshold voltage since the threshold voltage, V_{th}, is a function of channel doping concentration, which is shown below [15]

$$V_{th} = V_{FB} + 2\psi_B + \frac{1}{C_{gate}} \sqrt{4\varepsilon_s q N_A \psi_B} \quad \text{for p-type substrate} \tag{2.2a}$$

$$V_{th} = V_{FB} - 2\psi_B - \frac{1}{C_{gate}} \sqrt{4\varepsilon_s q N_D \psi_B} \quad \text{for n-type substrate} \tag{2.2b}$$

where V_{FB} is the flat-band voltage, $q\psi_B$ is the potential difference between the Fermi level E_F and the intrinsic Fermi level E_i, C_{gate} is the gate capacitance, ε_s is the permittivity of Si, N_A and N_D are the channel doping concentrations for p-type substrate and n-type substrate, respectively. Boron penetration will alter the intended device properties in an unacceptable way.[16] All these problems, especially high gate leakage

current, force the CMOS industry to replace the SiO_2 with a high dielectric constant (high-*k*) material for the gate dielectric.

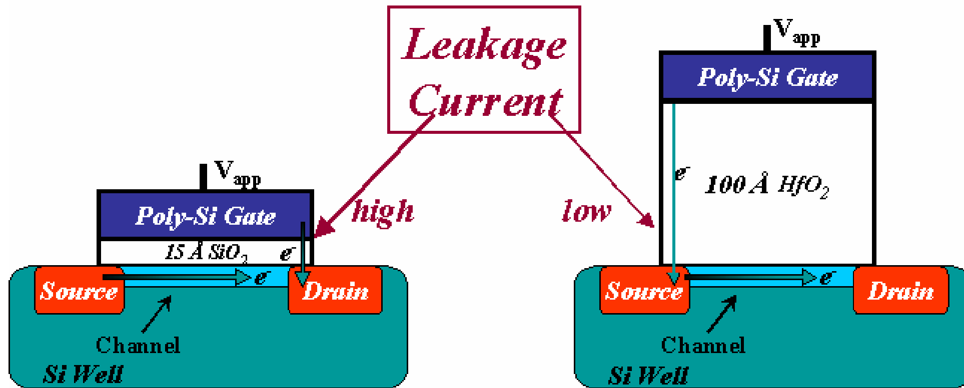


Figure 2.1 Leakage current reduced by replacing SiO_2 with a high-*k* dielectric as the gate material.

2.1.2 High-k Materials as the Gate Dielectric Layer

Eq. (2.1) indicates the direct tunneling current depends on gate physical thickness. In order to keep or reduce the direct tunneling current to the acceptable level, the SiO_2 gate physical thickness can not be too thin. However, the high performance improvement requires large drain current, which needs thin gate film as a result of feature size down scaling. So using high-*k* materials will increase the physical gate thickness thus lowering the direct tunneling gate leakage current and resulting in no loss of the performance as a result,[17] which is illustrated in Figure 2.1. The high dielectric constant *k* is used to compensate the loss of gate capacitance due to the increase of physical thickness, which maintains and even enhances the necessary device drive current. It can be easily seen by a simple equation below [17]

$$C_{gate} = \frac{\varepsilon_0 k_{SiO2}}{t_{SiO2}} = \frac{\varepsilon_0 k_{high-k}}{t_{high-k}} \qquad (2.3)$$

For the electrical design of a device the precise material does not matter, so it is convenient to define an "electrical thickness" of the new gate material in terms of its equivalent silicon dioxide thickness or "equivalent oxide thickness" (*EOT*). *EOT*, is used to represent the theoretical thickness of SiO_2 that would be required to achieve the same capacitance as the high-*k* dielectric, which can be derived from Eq. (2.3) and shown below

$$EOT = \frac{k_{SiO2}}{k_{high-k}} t_{high-k} \tag{2.4}$$

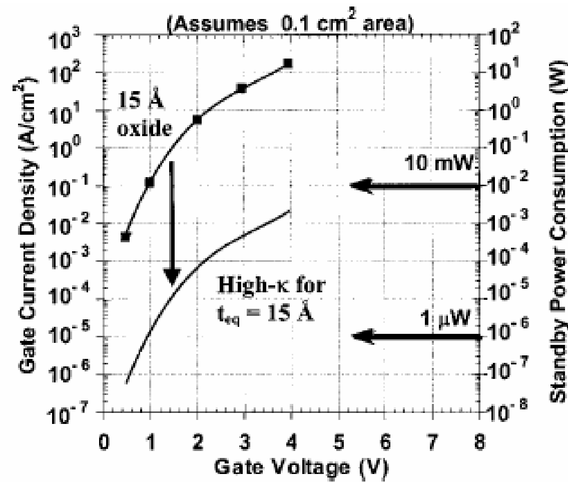


Figure 2.2 Comparisons of device power consumption and leakage current between 15 Å SiO_2 gate and 15 Å *EOT* HfO_2 gate. [17]

By introducing high-*k* dielectric materials, the direct tunneling gate leakage current and thus static power consumption can be decreased with the increase of gate physical thickness, which is illustrated in Figure 2.2. Increasing the *k* value can increase drive current without increasing direct tunneling current, which causes transistor performance improvement. In this way, the traditional down-scaling of SiO_2 thickness turns into down-scaling of the *EOT* of the high-*k* gate dielectrics. The objective is to develop

high-*k* materials which allow scaling to continue to ever lower values of *EOT*.

2.1.3 High-k Gate Material Property Considerations

Many high-*k* dielectric materials[18] have been investigated as the candidate gate material for future CMOS transistors. All these materials must meet a set of criteria to perform as a successful gate dielectric. Several aspects need to be considered for the appropriate material properties used for gate dielectric applications.

The requirements of a new dielectric material are five-fold.

1. Its *k* value must be high enough to be used for a long term of scaling and it must have band offsets with Si of over 1 eV to minimize carrier injection into its bands.

2. The high-*k* material is in direct contact with the Si channel, so it must be thermodynamically stable and form a good electrical interface with Si.

3. It must be amorphous in order to act as an insulator and prevent the leakage current.

4. It must be compatible with the metal gate electrode.

5. The deposition of the high-*k* materials must be compatible with the standard CMOS fabrication process.

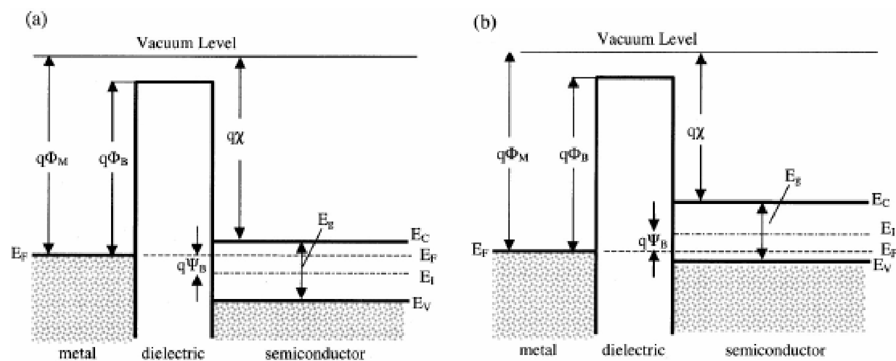


Figure 2.3 Energy band diagrams for ideal MOS capacitors for (a) n-type and (b) p-type semiconductor structure.[17]

2.1.3.1 Dielectric constant and barrier height

Obviously a gate material with a higher dielectric constant than that of SiO_2 is needed. However, the required dielectric constant must be balanced against the barrier height for the tunneling process of electrons or holes. For electrons tunneling from the Si substrate to the gate, the conduction band offset, $\Delta E_c = q[\chi\text{-}(\Phi_m\text{-}\Phi_B)]$; for electrons tunneling from the gate to the Si substrate, this offset is $q\Phi_B$ (see Figure 2.3). The leakage current increases exponentially with decreasing barrier height and gate thickness for electron direct tunneling transport, as shown in Eq. (2.1). However, almost all the high-*k* materials show a tradeoff tendency between the *k* value and band offset, which requires reasonably large band gaps.[19] Figure 2.4(a) shows the bad gaps and Figure 2.4 (b) shows the band offset for a number of potential high-*k* gate dielectric materials. Previous research work[17] pointed out that if the band offsets, ΔE_c, of some dielectric materials are less than 1.0 eV, it will likely preclude using these materials as gate dielectric, since tunneling leakage current will lead to an unacceptable value. For the dielectric materials with small band gap (like $SrTiO_3$ ~ 3.3 eV), their bands must be aligned symmetrically with respect to those of Si for both barrier height to be over 1 eV. In practice, the conductance band offset is smaller than the valence band offset. This limits the choice of dielectric materials to those with band gaps over 5 eV. So to keep the balance of dielectric constant and band offset, it is suggested from Figure 2.4(a) that materials with *k* values of 20-25 and band gap of ~ 6 eV are the potential candidates as the gate dielectric materials.

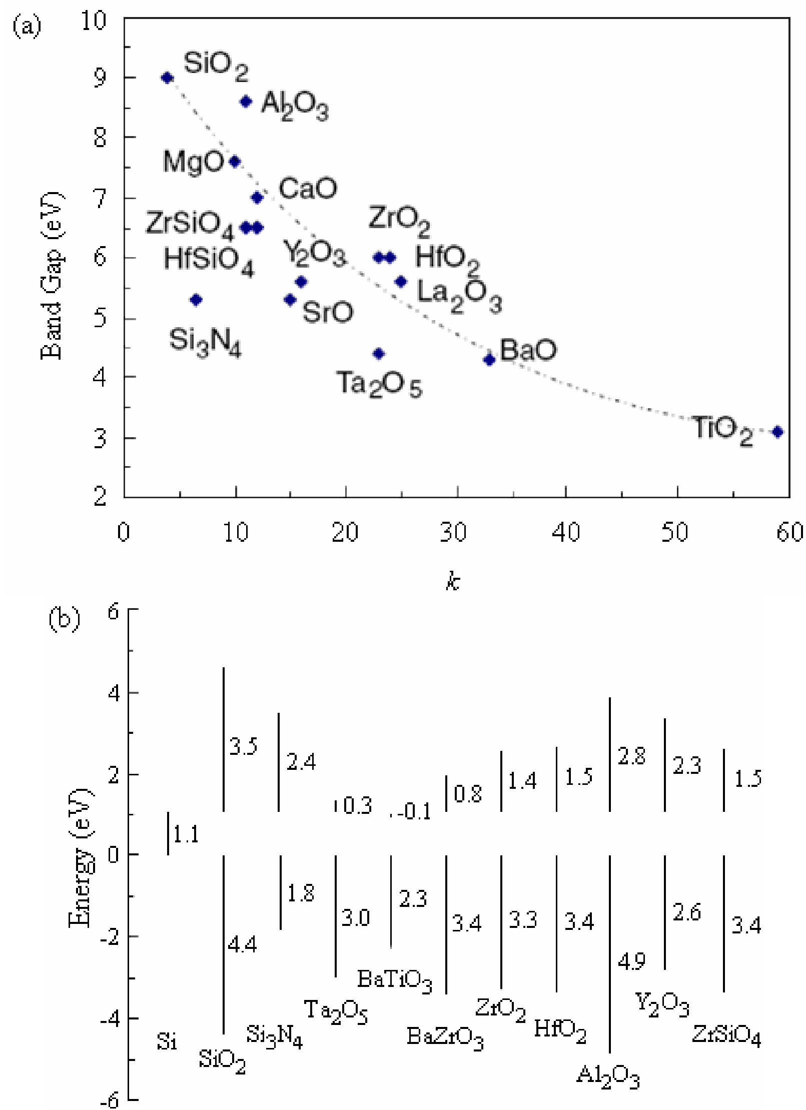


Figure 2.4 (a) Dielectric material band gaps as a function of the dielectric constant values; (b) Dielectric material band offset with Si. [17]

2.1.3.2. Stability and interface quality.

For all gate dielectrics, the interface with Si plays a key role in determining the overall electrical properties. Most of the high-*k* metal oxide materials under investigation have an unstable interface with Si: they will react with Si to form an undesirable interfacial layer (either SiO_2 or silicate) because this interfacial layer will

increase the *EOT* and negate the effect of using the high-*k* dielectrics. Besides, the dielectric is in direct contact with the Si channel. The carriers in the channel flow within angstroms of the Si/high-*k* interface. Hence, this interface must be of the highest electrical quality, in terms of roughness and the absence of interface states. Most of the high-*k* materials show a high interface state density D_{it} ~ 10^{11} - 10^{12}/eV·cm^2 while SiO_2 has an interface state density as low as D_{it} ~ 1-3×10^{10}/eV·cm^2.

2.1.3.3. Film morphology

It is desirable to select an amorphous dielectric material because the grain boundaries of poly-crystal will introduce extra defects which enhance the leakage current. But most of the advanced gate dielectrics studied to date are easily crystallized during the thermal treatment in fabrication process. Since an amorphous dielectric must be chosen, a material with high crystallization temperature is preferred. According to the standard CMOS fabrication process, the high-*k* dielectrics must withstand a rapid thermal anneal for 5 seconds at 1000°C. But if an amorphous material is desired, this is a strenuous condition in that most high-*k* materials are not good glass formers, unlike SiO_2.

2.1.3.4. Gate compatibility

Boron penetration still exists between poly-Si gate electrode and high-*k* gate material. In addition, the interfacial layer will also form at poly-Si and high-*k* interface. So metal gates are desired when high-*k* dielectric material is used as the gate dielectric. In general, a metal with a low work function is preferred for nMOS and a metal with a high work function is preferred for pMOS. A key issue for gate metal electrode

materials will be the control of the gate metal work function after CMOS process, which is the main factor to determine the transistor threshold voltage.

2.1.3.5. Process compatibility

A crucial factor in determining the final film quality and properties is the method used for the dielectrics deposition in a fabrication process. The deposition process for the dielectric must be compatible with current or expected CMOS processing, cost, and throughput. Several methods have already been used for high-*k* dielectric deposition including physical vapor deposition (PVD) (e.g. sputtering and evaporation), chemical vapor deposition (CVD) (involving MOCVD, ALCVD *et al*) and molecular beam epitaxy (MBE).

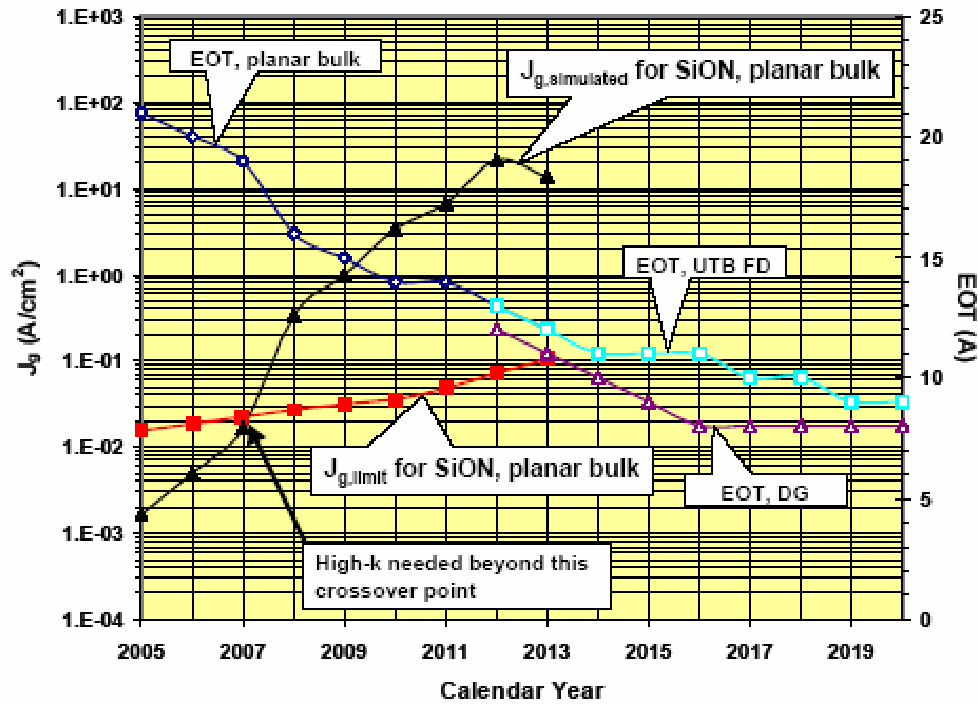


Figure 2.5 Leakage current limitation of SiON as gate dielectric for low standby power by ITRS 2005. [9]

2.1.4 Current Status with High-k Materials

The concerns regarding high leakage current, boron penetration of thin SiO_2 have led to the material stack such as silicon-oxynitride (SiON). This material provides a slightly higher *k* value (*k* ~ 5) than SiO_2 and reduces the leakage current and boron penetration (since the film is physically thicker). The addition of N to SiO_2 greatly reduces the boron diffusion through the dielectric.[20, 21] Furthermore, small amounts of N incorporation at or near the Si channel has been shown to improve device performance.[22] However, due to the relatively low *k* value (although higher than SiO_2), the scaling of SiON appears to be limited to an *EOT* ~ 8 Å. Below this, the effects of gate leakage current will prevent further improvement in device performance, which is shown in Figure 2.5. So SiON dielectric only represents a near-term solution for scaling the CMOS transistor. Materials with even higher dielectric constant are still needed.

Among those high-*k* dielectric materials, Hf-based materials such as HfO_2, $HfSiO_4$, $HfSiO_xN_y$ *et al* have recently attracted much more attention as potential gate dielectric materials. HfO_2 shows high dielectric constant (*k* ~ 25) and large band offset (ΔE_c = 1.5 eV). Although HfO_2 shows a low crystallization temperature below 600°C, it forms a nano-crystalline phase without introducing extra leakage current. Lee *et al*[23] and Kim *et al*[23] find that the leakage currents of amorphous and nanocrystalline HfO_2 are similar. However, two main issues hinder the utilization of HfO_2 as the gate dielectric.

One of the issues is the formation of the interfacial layer between HfO_2 and Si substrate.[25-30] Figure 2.6 shows a high-resolution transmission electron microscope (HRTEM) image of an interfacial layer formation between the HfO_2 gate dielectric and

Si substrate.[31] This interfacial layer contributes to the *EOT*, and thus defeats the purpose of using high-*k* dielectric material to replace the SiO_2 as the gate dielectric, which is given below

$$EOT_{total} = EOT_{high\text{-}k} + EOT_{IL} \tag{2.5}$$

Another issue is the high trap density at the HfO_2/Si interface. Unlike the SiO_2/Si interface, HfO_2/Si interface possesses a high surface states density, which can easily trap electrons and pin the interface Fermi energy level, and thus the threshold voltage of the transistor. Moreover, channel mobility degradation is partially due to the scattering by interface traps, in additional to scattering by phonons and fixed charges in high-*k* dielectrics.

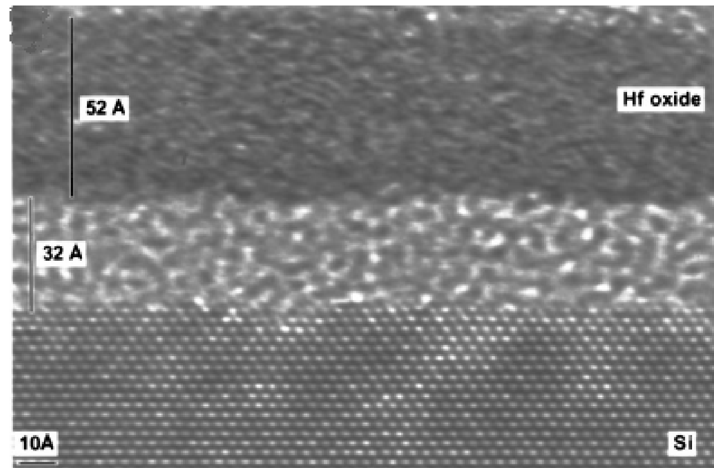


Figure 2.6 HRTEM image of interfacial layer between HfO_2 and Si substrate.[31]

Since the formation of the interfacial layer and the high density of interface traps severely degrade the transistor performance, suppressing the interfacial reaction and lowering the interface trap density between HfO_2 and Si substrate are needed to get a good HfO_2/Si interface for improving transistor performance.

2.2 High Source/Drain Metal/Si Parasitic Resistance

Metal/Si contacts have always been an integral part of Si device technology. With the continued shrinkage of feather size in Si CMOS technology, source/drain parasitic resistances represent a significant fraction of the total device resistance and contribute to a loss of device performance. Figure 2.7 shows the projections by ITRS 2005 for the channel "on" resistance R_{on} and parasitic resistance $R_{parasitic}$ for different CMOS nodes. A key source/drain requirement is to limit the $R_{parasitic}$ to a small fraction of the R_{on}. The parasitic resistance, $R_{parasitic}$, mainly includes the silicide resistance R_{sili}, junction extension resistance R_{ext}, junction overlap resistance R_{ol} and metal/Si contact resistance R_c, which are shown in Figure 2.8.

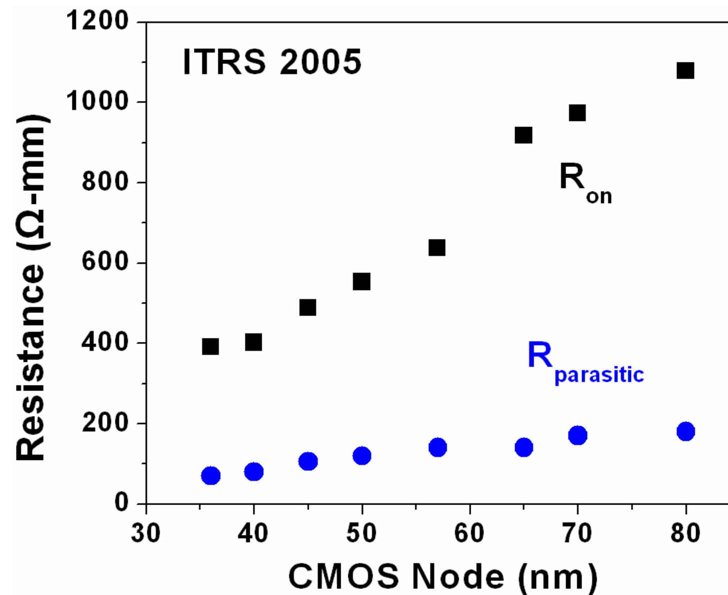


Figure 2.7 Projections by ITRS 2005 for the channel "on" resistance and parasitic resistance of high performance devices. [9]

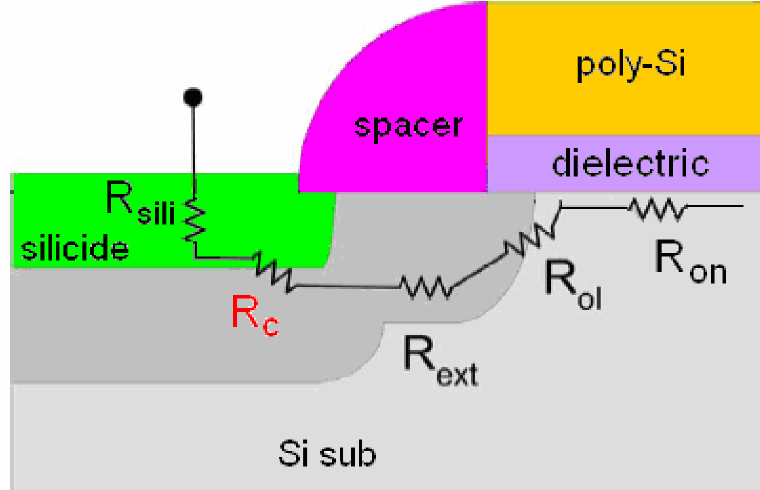


Figure 2.8 MOSFET parasitic resistances which cause device performance loss.

2.2.1 Silicide, Junction Extension and Overlap Resistance

Silicide resistance, R_{sili}, is an important part in the parasitic resistance. $TiSi_2$ always acted as the low resistance silicide material for source/drain contact till 1990s, in which the resistance increased sharply with lines narrower than 350 nm. Then $CoSi_2$ was used to replace $TiSi_2$ as the silicide material with low resistance. However, when the line width is below 50 nm associated with the down scaling of transistor feature size, $CoSi_2$ also showed a rapid rise in resistance. CMOS industry now focuses on NiSi as the silicide material since[32-36] NiSi shows several advantages such as low resistivity in narrow dimension below 50 nm, low thermal budget for formation, low Si consumption and low transistor leakage current.[37]

As the gate length decreases, the depth of source and drain extensions has to be reduced to suppress short channel effects. At the same time, low sheet resistance of the source/drain extensions has to be realized to take full advantage of the reduced channel resistance in shorter gate length MOSFETs. So it requires junction high doping

concentration for the junction extension resistance R_{ext} and abrupt lateral junction for overlap resistance R_{ol}, it requires junction high doping concentration and abrupt lateral junction to keep it to a relatively low value.

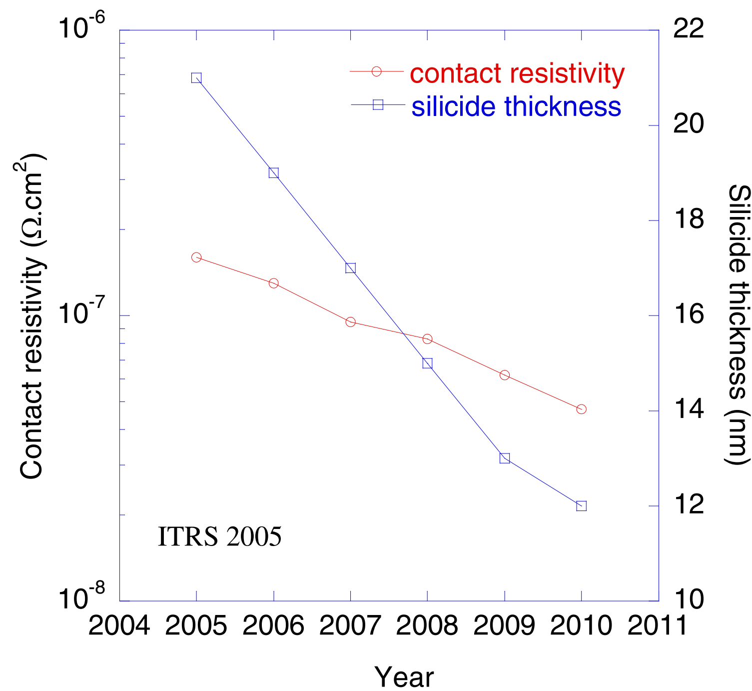


Figure 2.9 ITRS 2005 projections for contact resistivity and silicide thickness. [9]

2.2.2 Contact Resistance

The metal/Si contact resistance, R_c, is a significant part of the total parasitic resistance. With continued scaling of device feature size, the contact resistance is emerging as the dominant component of the parasitic resistance. Figure 2.9 shows the required contact resistivity and silicide thickness from ITRS 2005.[9] Future MOSFETs will require contact resistivity values as low as 10^{-8} $\Omega \cdot cm^2$, which is an order of magnitude less than the current contact resistivity 10^{-7} $\Omega \cdot cm^2$. A report by Ozturk *et al*[38] indicates that if the contact resistivity is kept at current value, the contact resistance

alone will produce series resistance values that are unacceptable for physical gate lengths smaller than ~30 nm. Since the physical gate length for high performance devices has already reached below 30 nm as shown in Figure 1.2, it's important and urgent to lower the contact resistance R_c or practically, contact resistivity ρ_c to meet the requirement of source/drain engineering.

Theoretically the contact resistivity is defined as $\rho_c \equiv \left(\frac{\partial J}{\partial V}\right)^{-1}_{V=0}$, J and V are the current density and voltage bias, respectively. For metal-semiconductor contacts with lower doping concentrations (<10^{17} cm^{-3}), the thermionic-emission current dominates the current transport while for contacts with higher doping concentration (>10^{17} cm^{-3}), the tunneling current dominates the current transport. The equations are expressed below [15]

$$J = A^*T^2 \exp(-\frac{q\Phi_B}{kT})(e^{\frac{qV}{kT}} - 1) \quad \text{for low doping} \tag{2.6a}$$

$$J \sim \exp(-\frac{q\Phi_B}{E_{00}}) \text{ and } E_{00} = \frac{q\hbar}{2}\sqrt{\frac{N}{\varepsilon_s m^*}} \quad \text{for high doping} \tag{2.6b}$$

Since $\rho_c \equiv \left(\frac{\partial J}{\partial V}\right)^{-1}_{V=0}$, the contact resistivity is a function of Schottky barrier height Φ_B and Si substrate doping level N, which is shown below [15]

$$\rho_c = \frac{k}{qA^*T}\exp(\frac{q\Phi_B}{kT}) \quad \text{for low doping} \tag{2.7a}$$

$$\rho_c \propto \exp(\frac{2\Phi_B}{\hbar}\sqrt{\frac{\varepsilon_s m^*}{N}}) \text{ for high doping} \tag{2.7b}$$

where A^* is the effective Richardson constant, k is the Boltzmann constant, T is the absolute temperature, $\hbar$ is Planck constant, q is the unit charge, N is the bulk doping concentration and m^* is the effective mass of electron or hole. A small contact resistance has been achieved by applying heavily-doped Si on both source and drain regions. This kind of metal/Si contact with linear current-voltage characteristic, which is called ohmic contact, has been the most widely used technique. However, from Eq. (2.7a) and Eq. (2.7b), lower contact resistivity can also be realized by lowering the Schottky barrier height especially when the doping level in Si is reaching its solubility[39] or high doping levels are undesirable.[40, 41] From Eq. (2.7a) and Eq. (2.7b), the improvement of contact resistivity by lowering the Schottky barrier height is given below and shown in Figure 2.10

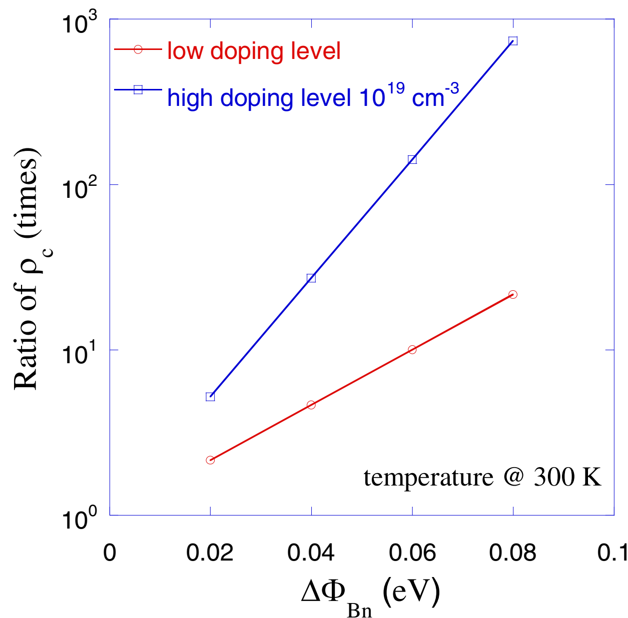


Figure 2.10 Improvement of contact resistivity by lowering the Schottky barrier height for electrons.

$$\frac{\rho_c(\Phi_B)}{\rho_c(\Phi_B - \Delta\Phi_B)} = \exp(\frac{q\Delta\Phi_B}{kT}) \quad \text{for low doping} \tag{2.8a}$$

$$\frac{\rho_c(\Phi_B)}{\rho_c(\Phi_B - \Delta\Phi_B)} = \exp(\frac{2\Delta\Phi_B}{\hbar}\sqrt{\frac{\varepsilon_s m^*}{N}}) \quad \text{for high doping} \tag{2.8b}$$

Figure 2.10 indicates that theoretically by lowering the Schottky barrier height by 0.06 eV, the contact resistivity for electron can be lowered by one order of magnitude for low doping level and two orders for high doping level. So the Schottky barrier height should be lowered to lower the contact resistivity at metal/Si interface.

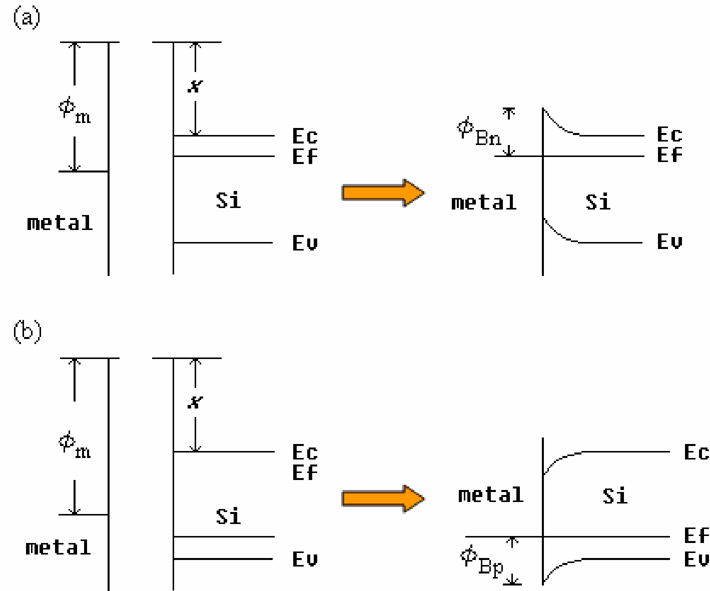


Figure 2.11 Ideal metal/Si contact energy band diagram for (a) n-type and (b) p-type.

2.2.3 Schottky Barrier Height

Before a metal and Si contact with each other, the system is not in thermal equilibrium. After the metal contacts with Si, the Fermi energy level of the metal lines up with the Fermi energy level of the Si, thermal equilibrium is established and a

Schottky barrier is formed. Ideally, the Schottky barrier height Φ_{Bn} for electron is determined by the difference between the metal work function and the Si electron affinity. The Schottky barrier height for hole, Φ_{Bp}, is determined by the difference between metal work function, Si electron affinity and Si band gap, which is shown in Figure 2.11. The equations are given below, respectively[15]

$$\Phi_{Bn} = \Phi_m - \chi \tag{2.9a}$$

$$\Phi_{Bp} = E_g - (\Phi_m - \chi) \tag{2.9b}$$

where Φ_m is the metal work function, χ is the Si electron affinity, and E_g is the Si band gap. Eq. (2.9a) and Eq. (2.9b) shows that a low Schottky barrier height can be obtained by choosing a small work function metal like Al and Ti for electrons and by choosing a large work function metal like Ni and Pt for holes.

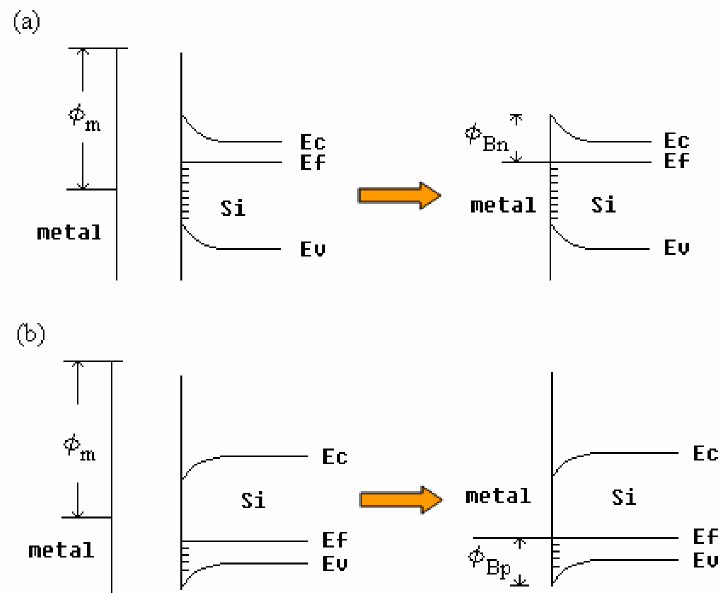


Figure 2.12 Metal/Si contact energy band diagram with surface states for (a) n-type and (b) p-type.

However, the Si surface is inherently dominated with a large density of

surface states. Surface states will introduce surface Fermi level in the band gap of Si, so the bulk Fermi level will line up with the surface Fermi level or in another word, Fermi level is pinned at the Si surface. The actual barrier height is mainly determined by the pinned Fermi level and largely independent of metal work function, which is shown in Figure 2.12. The equations are shown below, respectively:

$$\Phi_{Bn} \approx E_{cs} - E_{fs} \quad (2.10a)$$

$$\Phi_{Bp} \approx E_{fs} - E_{vs} \quad (2.10b)$$

where E_{cs} and E_{vs} are the surface conductance and valence band energy levels, respectively, E_{fs} is surface pinned Fermi energy level. According to Eq. (2.9) and Eq. (2.10), to lower the Schottky barrier height, the surface state density needs to be minimized to tune the barrier height by choosing a metal with a proper work function according to the ideal metal/Si contacts.

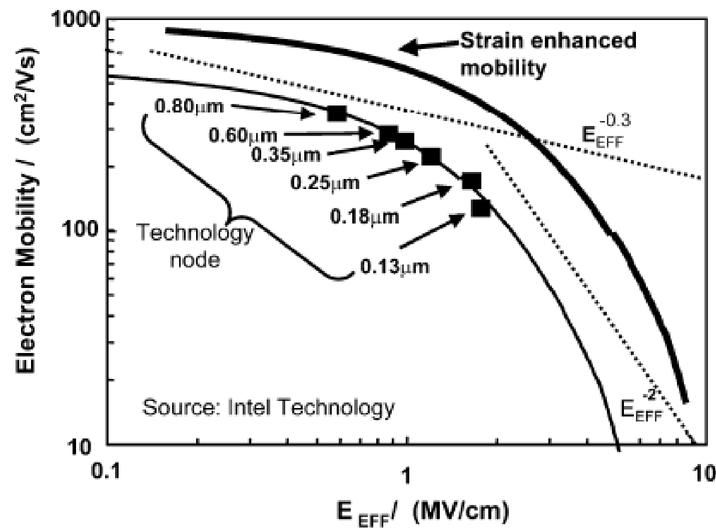


Figure 2.13 Mobility versus scaling trend for Intel process technology. [42]

2.3 Channel Mobility Degradation

A key scaling problem in nanoscale transistors is mobility degradation caused by the large vertical electric fields. Figure 2.13 shows the mobility versus technology scaling trend for various Intel process technologies.[42] The mobility has decreased from 400 to 120 $cm^2/V\cdot s$ during the last decade. To counteract this undesirable mobility trend, it is very important to incorporate mobility enhancing mechanisms in nanometer logic technology.

2.3.1 Strained Silicon

Strained Si[43-45] technology enables improvement in CMOS performance and functionality since strained Si has electronic properties that are superior to those of bulk Si. Specifically, the strained Si film has greater electron and hole mobilities, which translate into greater drive current for CMOS transistors. A recent report by Thompson *et al*[42] indicated an increase in hole mobility of more than 50% for p-type strained Si transistor and an increase in electron mobility of ~ 20% for n-type strained Si transistor. The key to get high quality strained Si for high performance devices is the growth of a low-defect-density SiGe film. Figure 2.14 shows a simple illustration for the strained Si structure. Growing a Si layer on SiGe, which has a larger lattice constant than Si, generates a strained Si heterostructure, which can be tailored to enable various properties. One of the main factors for performance enhancement with strained Si technology is the amount of strain introduced to the strained Si film, which is determined by the Ge content in the underlying SiGe film. Since the deposition of SiGe has a great effect on performance improvement, it is very important to understand the

SiGe growth behavior.

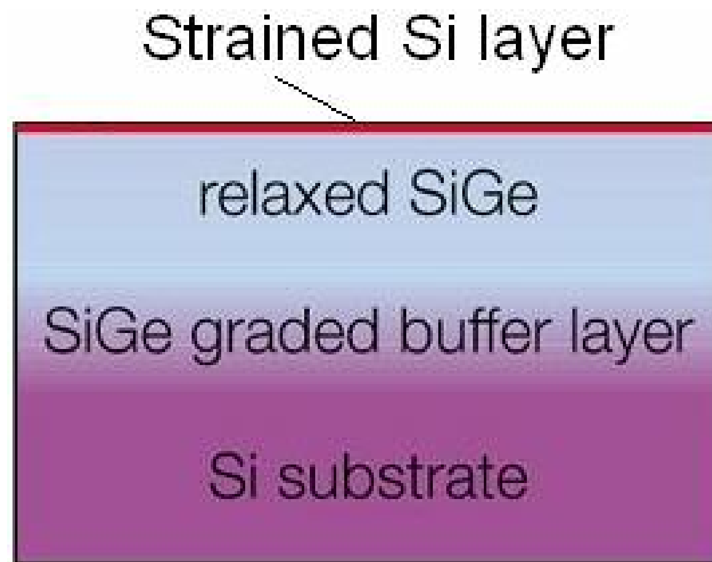


Figure 2.14 Illustration of structure for strained Si.

2.3.2 SiGe Alloy Growth Behavior

In the early 1990's, heteroepitaxtial silicon-germanium alloys ($Si_{1-x}Ge_x$) were successfully applied to Si-based heterojunction bipolar transistors to achieve better performance in current gain and cutoff frequency.[46,47] More recently, $Si_{1-x}Ge_x$ attracted more attention for its important application in the strained-Si complementary MOSFET for mobility enhancement. A number of growth techniques have been used to deposit $Si_{1-x}Ge_x$ including various chemical vapor deposition (CVD) techniques: ultrahigh vacuum CVD (~10^{-5} Torr),[48,49] very low pressure CVD (~10^{-3} Torr),[50,51] low pressure CVD (~10^{-2} Torr),[52-54] rapid thermal CVD (~1 Torr),[55,56] atmospheric pressure CVD (~740 Torr)[57,58] plasma-enhanced CVD,[59]as well as gas source molecular beam epitaxy.[60-62] Several precursors have been investigated for $Si_{1-x}Ge_x$ deposition as the Ge source, such as germane (GeH_4)[48-59] and digermane (Ge_2H_6),[49,62] and as the Si source,

such as silane (SiH_4),[48,49,50,51,53,63] disilane (Si_2H_6),[49,62] and dichlorosilane (SiH_2Cl_2).[54,56,58,64] $Si_{1-x}Ge_x$ growth by CVD is a much more complicated process than the growth of pure Si by CVD. For example, the Ge content in the film is controlled by several parameters, including deposition temperature, deposition pressure, SiH_4 flow rate, and most importantly, GeH_4 flow rate. Different behaviors in growth rate have been observed with respect to the effect of Ge content incorporated in the film. With GeH_4 and SiH_2Cl_2 as the precursors, a monotonic increase in growth rate has been reported with increasing Ge content by Hartmann *et al*[54] in low pressure CVD at deposition temperature of 650°C, 700°C and 750°C, by Kamins *et al*[58] in atmospheric pressure CVD at 625°C, by Garone *et al*[56] in rapid thermal CVD between 625°C and 700°C, and by Hoyt *et al*[64] in rapid thermal CVD at 640°C. With SiH_4 and GeH_4 as the precursors, Jang *et al*[65] demonstrated that the effect of Ge content on growth rate is more complicated in very low pressure CVD. A monotonic growth rate increase was observed with Ge content at 570°C, but a monotonic growth rate decrease with Ge content at 700°C. Between 600°C and 675°C, the growth rate exhibited first an increase and then a decrease, resulting in a maximum with Ge content. Using ultrahigh vacuum CVD, Meyerson *et al*[48] reported a growth rate increase with Ge at 550°C, Robbins *et al*[53] reported a growth rate decrease with Ge at 700°C, and Racanelli *et al*[66] reported that the growth rate first increased and then decreased with Ge between 577°C and 665°C.

2.3.3 Previous Models for SiGe Growth

Several kinetic models have been proposed to explain the complicated growth behavior in $Si_{1-x}Ge_x$ CVD from SiH_4 and GeH_4. Robbins *et al*[53] attributed the growth rate maximum with Ge content to a competition between desorption of H from the surface and adsorption of H from the gas phase. A scaling factor was introduced in order for their model to fit the experimental data. Russell *et al*[67] proposed a model by treating SiH_4 and GeH_4 deposition as two parallel processes. Each is a competition between adsorption of precursor and desorption of H, and there is a fast equilibration between Si and Ge hydrides on the surface. Malik *et al*[68] attempted to explain the growth behavior on the basis of Langmuir-Hinshelwood's adsorption theory. Lee[69] presented a model based on competitive adsorption of GeH_4 and SiH_4 on vacant surface sites, coupled with GeH_4-assisted H desorption. Jang[65] explained the growth behavior with two mechanisms: (1) enhanced H desorption by the presence of Ge at low Ge content and/or temperature and (2) reduced reaction probability of GeH_4 and SiH_4 with the incorporation of Ge at high Ge content and/or temperature.

These models attempted to quantitatively explain the growth behavior of $Si_{1-x}Ge_x$ by various CVD processes. Although many of them provide reasonable explanations for several aspects, they are best described as semiquantitative or qualitative models. A comprehensive and quantitative model is still needed for SiGe growth from SiH_4 and GeH_4 by CVD.

CHAPTER 3

SURFACE PASSIVATION OF SILICON (100) BY MONOLAYER SELENIUM

3.1 Si (100) Surface Structure in Vacuum

Surface atoms on Si (100), due to the discontinuity of lattice atoms above them, have to undergo reconstruction in ultrahigh vacuum to minimize surface energy.[70] Figure 3.1 shows the atomic structure of clean Si (100) in vacuum. Each surface atom has a dangling bond and shares a dimer bond with its neighboring surface atom. Both the dimer bonds and back bonds are strained on this surface. Because dangling bonds are not saturated at the Si (100) surface, they are the sites for surface chemical reactions. When a metal oxide dielectric material is deposited on the surface of Si (100), oxygen atoms can easily react with the surface Si atoms to form an interfacial layer between high-*k* dielectric and Si substrate. These dangling bonds also give rise to interface states within the energy band gap of Si, which cause interface traps at the high-*k*/Si interface. When a metal is deposited on Si, the interface Fermi energy is often pinned by these interface states, making the Schottky barrier height independent of metal work function. Since the dangling bonds are the origin of surface reaction sites and surface states, it is important to remove the dangling bonds in order to suppress the interfacial layer formation between the high-*k* dielectric and the Si substrate, minimize the interface trap density at high-*k*/Si interface, and lower the metal/Si (100) contact resistivity.

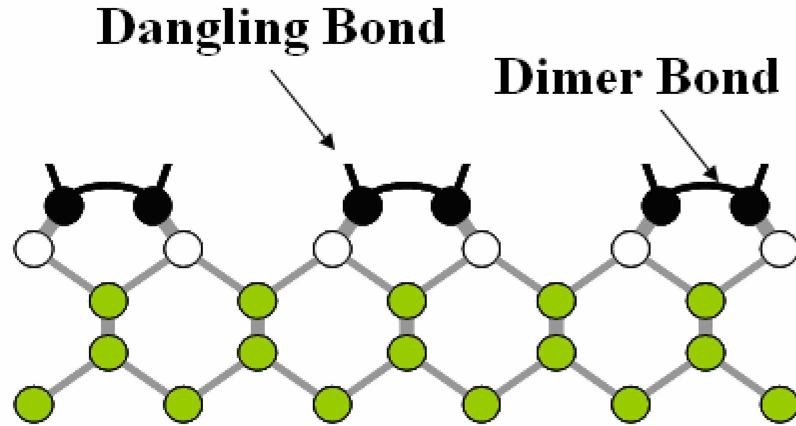


Figure 3.1 Atomic structure of the clean Si (100) surface in ultrahigh vacuum. [70]

3.2 Si (100) Surface Structure with Se Passivation

The idea of surface passivation by adsorbates has been studied more than three decades ago. The most important aspect of surface passivation is a valence difference between the substrate and the adsorbate such that, when adsorbate atoms replace the bulk-terminated plane, all broken covalent bonds are eliminated. Forming gas (95% N_2 + 5% H_2) annealing has been a standard CMOS process used to passivate the Si (100) surface for a long time. During the annealing, each dangling bond at Si (100) surface will be terminated by one H atom. However, the dimer bonds are still intact and can break again to act as dangling bonds especially when oxygen-contained high-k dielectric is applied. So it's desirable that the passivation on Si (100) can both terminate dangling bonds and relax the dimer bonds.

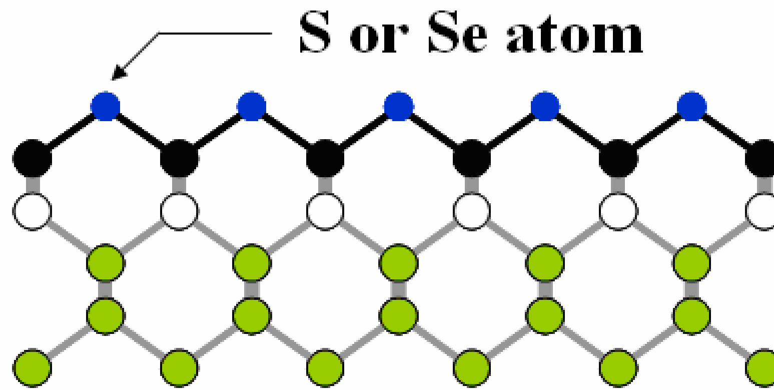


Figure 3.2 Atomic structure of the Se-passivated Si (100) surface. [71]

In 1991, Kaxiras[71] introduced the concept "valence-mending" to passivate the Si (100) surface. He concluded that natural "valence-mending" choices for Si (100) would be elements with valence 2 or 6. The best choices would be group-VI elements (O, S, Se, and Te) because they tend to form structures with twofold coordination and sp^3 bonding hybrids, precisely as required for restoration of Si (100). O and Te can be dismissed since O can easily diffuse into Si and form SiO_2 and Te has bulk bond length which is different from that of Si by 22%. As shown in Figure 3.2, atoms of sulphur (S) and selenium (Se) can bridge between two surface atoms on Si (100), thereby terminating dangling bonds and relaxing the strained dimer bonds. Se was predicted to be a better choice than S for passivating Si (100) because the Se atom has several proper factors with Si: covalent and atomic radius; bond length and angle, which are shown in Table 3.1 and 3.2. It will introduce less strain in the passivated surface. The Se-passivated Si (100) surface is stable so that it is expected that Se passivation will suppress interfacial layer formation between high-*k* dielectric and Si substrate. The interface trap density will also decrease due to the removal of dangling bonds. As a

result, Schottky barrier heights between metals and Se-passivated Si (100) are more closely correlated to metal work functions `than the surface properties of Si (100) without passivation.

Table 3.1 Covalent and atomic radius of Si and group VI elements

	Si	Se	S	Te
Covalent Radius (Å)	1.17	1.17	1.04	1.37
Atomic Radius (Å)	1.18	1.16	1.06	1.42

Table 3.2 Structural parameters of bulk phases of S and Se and of the ideal and restored Si (100) surfaces.

	Bond length(Å)	Bond angle(degrees)
Monoclinic Se	2.34	105.5
Rhombohedral S	2.06	102.2
Ideal Si (100)	2.35	109.4
Restored Si (100):S	2.24	118.4
Restored Si (100):Se	2.34	110.2

3.3 Se passivation on Si (100) surface by molecular beam epitaxy

In this research work, monolayer Se atoms are deposited on Si (100) surface to passivate the dangling bonds by molecular beam epitaxy (MBE) system. The Si (100) wafer is first rinsed in de-ionized water for 2 minutes and then immediately dipped into 2% HF for 35 seconds to remove the native oxide. It is then terminated by H atoms. After the HF dip, wafer is blown dry with N_2 and loaded into the MBE system. In the MBE chamber, ultrahigh vacuum (~10^{-10} Torr) is maintained as the base pressure. The Si (100) wafer is first annealed at 600°C for 25 minutes. This is to desorb the surface H atoms. Then the wafer is transferred to the Si source chamber. A Si buffer layer of 100~1000 Å is deposited at 600°C and then annealed at 800°C for 1 hour. This is to have a perfect Si (100) surface for the Se passivation. In Figure 3.3(a) is shown a sharp

2×1 surface reconstruction atom structure. That is obtained with reflection high-energy electron diffraction (RHEED) after annealing, which indicates that the Si surface is in the structure shown in Figure 3.1. The wafer is then transferred to the Se source chamber for passivation. The Se source temperature is 224°C, while the Si wafer is kept at a temperature of 300°C during the passivation. Once the shutter of the Se source is open, Se atoms will deposit on the Si surface. The in situ RHEED shows the Si (100) surface gradually changes in 60 seconds from 2×1 structure to 1×1 structure, which is shown in 3.3(b). This indicates that one monolayer of Se atoms is deposited on the Si (100) surface, which forms the surface atomic structure in Figure 3.2. Then the shutter of the Se source is closed and Si wafer is kept inside the MBE chamber till it cools down to room temperature.

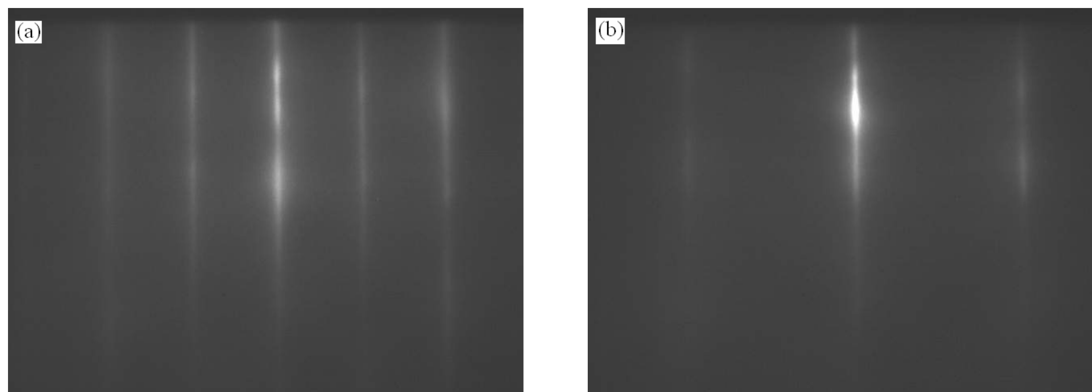


Figure 3.3 (a) RHEED image of bare Si (100) with 2×1 surface structure and (b) RHEED image of Se-passivated Si (100) with 1×1 surface structure.

CHAPTER 4

HAFNIUM DIOXIDE ON N-TYPE SILICON (100) WITH SELENIUM PASSIVATION

In this chapter, experiments are designed to verify the interfacial layer suppression effect at HfO_2/Si interface by Se passivation. Results for HfO2 on Se-passivated n-Si (100) are reported. [72] Capacitance-voltage (C-V) and current-voltage (I-V) measurements are utilized for characterization analysis.

4.1 Experiments

4.1.1 Wafer Preparation

N-type Si (100) wafer with resistivity 1-10 Ω·cm is chosen. The wafer is first rinsed in de-ionized water for 2 minutes. This is to oxidize the surface. Then the wafer is dipped into 2% HF for 35 seconds to remove the surface native oxide and be terminated by H atoms. After HF dip, the wafer is blown dry with N_2 and loaded into the MBE system.

4.1.2 Se Passivation

This is described in section 3.3. A 500 Å Si buffer layer is deposited during Se passivation. A control wafer with 500 Å Si buffer layer is also fabricated without Se passivation for comparison.

4.1.3 HfO_2 Growth

Three methods are employed to grow HfO_2 on the control and Se-passivated samples.

— HfO_2 growth by reactive sputtering

Both control and Se-passivated samples are loaded into a 4-inch target reactive sputtering system. After pumping to ~ 4×10^{-6} Torr, Ar and O_2 with a ratio of 10 sccm/40 sccm are introduced into the chamber. The pressure during sputtering is kept at 10 mTorr. Hafnium oxide is deposited on both the control and Se-passivated samples at room temperature for 3 minutes. The plasma power is chosen at 40 watts. A 99.95% Hf target is used for the sputtering.

— HfO_2 growth by O_3 oxidation

Both control and Se-passivated samples are loaded into the E-beam evaporator system. After pumping to ~ 8×10^{-7} Torr, 40 Å of Hf is deposited on both control and Se-passivated samples. Then samples are cut into small pieces and loaded into a home-made furnace. After pumping, ultra-pure O_2 is introduced to the furnace at 1 atm. O_3 is generated by a UV-lamp. Then both samples are oxidized and annealed simultaneously at 360, 440, 520, and 600ºC for 10 minutes. Step (d) is skipped since samples have been already annealed during oxidation. 99.95% Hf metal pellets are used for the evaporation.

— HfO_2 growth by dry oxidation

The HfO_2 growth by dry oxidation is similar with the HfO_2 growth by O_3 oxidation. The differences are for HfO_2 growth by dry oxidation, dry O_2 is introduced

instead of O_3 and oxidation temperatures are chosen at 300, 400, 500, and 600ºC.

4.1.4 Post-Deposition Annealing

After HfO_2 deposition, both control and Se-passivated samples are cut into small pieces and loaded into a home-made furnace. After pumping to a base pressure 10^{-6} Torr, ultra-pure N_2 is introduced into the furnace chamber at 1 atm. The samples are annealed at 400, 500 and 600ºC for 1 minute. (This step is only applied for HfO_2 growth by reactive sputtering. For HfO_2 growth by O_3 and dry oxidation, it can be skipped because annealing has been performed simultaneously during oxidation.)

4.1.5 Photolithography

All the samples are spin-coated with HMDS (Hexamethyldisilazane) at 4000 rpm for 30 seconds and S1808 (photoresist) at 2000 rpm for 30 seconds, consecutively. Then a post baking is applied to all the samples at 90°C for 35 seconds. After that, samples will be exposed under mask by UV lamp for 50 seconds. Then samples will be dipped in develop solution for 35 seconds for pattern transformation.

4.1.6 Metal Deposition

The metal electrodes are fabricated by using a lift-off process. After photolithography, both control and Se-passivated samples are loaded into an E-beam system. After pumping to ~ 2×10^{-6} Torr, 1000 Å Al is deposited for top electrodes and 500 Å Ti is deposited on the back side for contact.

Figure 4.1 shows the main fabrication process flow for the experiments.

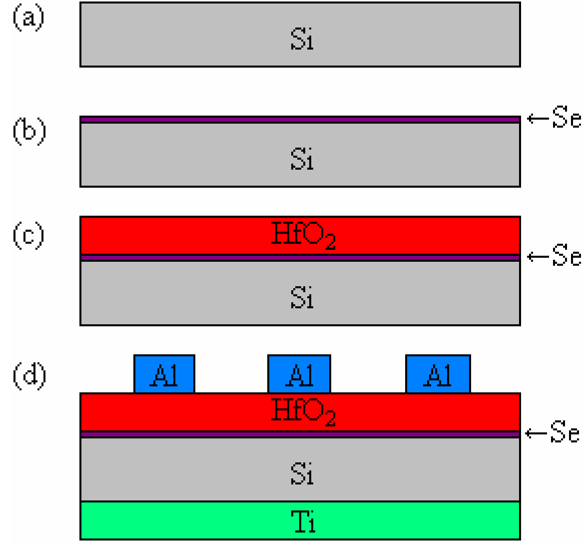


Figure 4.1 Fabrication processes of the experiments: (a) wafer preparation; (b) Se monolayer passivation; (c) HfO_2 growth; (d) Photolithography, Al deposition for front contact and Ti deposition for back contact

4.2 Characterization

High frequency C-V characterization is performed to determine the *EOT* of the gate dielectric and flat-band voltage. On the C-V curve, the maximum capacitance in accumulation region is the gate oxide capacitance. The *EOT* can be extracted by

$$EOT = A\frac{\varepsilon_0 k_{SiO_2}}{C_{accu}} \tag{4.1}$$

The flat-band voltage V_{FB} can be extracted from the C-V curve, which reveals the shift in threshold voltage due to interface and fixed charges. Theoretically the ideal flat-band voltage V_{FB} is determined by the difference between the metal work function Φ_m and the semiconductor work function Φ_S, which is given below [15]

$$V_{FB} = \frac{1}{q}(\Phi_m - \Phi_S) = \Phi_{ms} \tag{4.2}$$

But the actual flat-band voltage will shift from the ideal flat-band voltage by an amount ΔV_{FB} due to the interface charge Q_{it} and fixed charges Q_f in the dielectric, which is given by

$$\Delta V_{FB} = -\frac{Q_{it} + Q_f}{C_i} \tag{4.3}$$

So the actual flat-band voltage is

$$V_{FB} = \Phi_{ms} + \Delta V_{FB} = \Phi_{ms} - \frac{Q_{it} + Q_f}{C_i} \tag{4.4}$$

Since the actual flat-band voltage V_{FB} corresponds to flat-band capacitance C_{FB}, it can be determined by finding the corresponding voltage to C_{FB} on the C-V curves. The C_{FB} is given by [15]

$$\frac{1}{C_{FB}} = \frac{1}{C_i} + \frac{1}{C_D} \tag{4.5}$$

where C_i is gate dielectric capacitance and equals to maximum capacitance C_{accu} in accumulation region, C_D is extrinsic Debye capacitance, which is given by[15]

$$C_D = A\frac{\varepsilon_0 \varepsilon_{Si}}{L_D} \quad \text{and} \quad L_D = \sqrt{\frac{kT\varepsilon_0\varepsilon_{Si}}{N_{bulk} q^2}} \tag{4.6}$$

The dielectric constant of the high-k material can be calculated below:

$$k = \frac{3.9 t_{high-k}}{EOT_{total} - EOT_{IL}} \tag{4.7}$$

where $t_{high\text{-}k}$ is the physical thickness of high-k dielectric, EOT_{IL} is the equivalent oxide thickness contributed by interfacial layer (equals to interfacial layer physical thickness if the interfacial layer is assumed to be SiO_2), EOT_{total} is the equivalent oxide thickness

from the gate dielectric and it can be calculated by Eq. (4.1). I-V characterization is used to directly measure the gate leakage current.

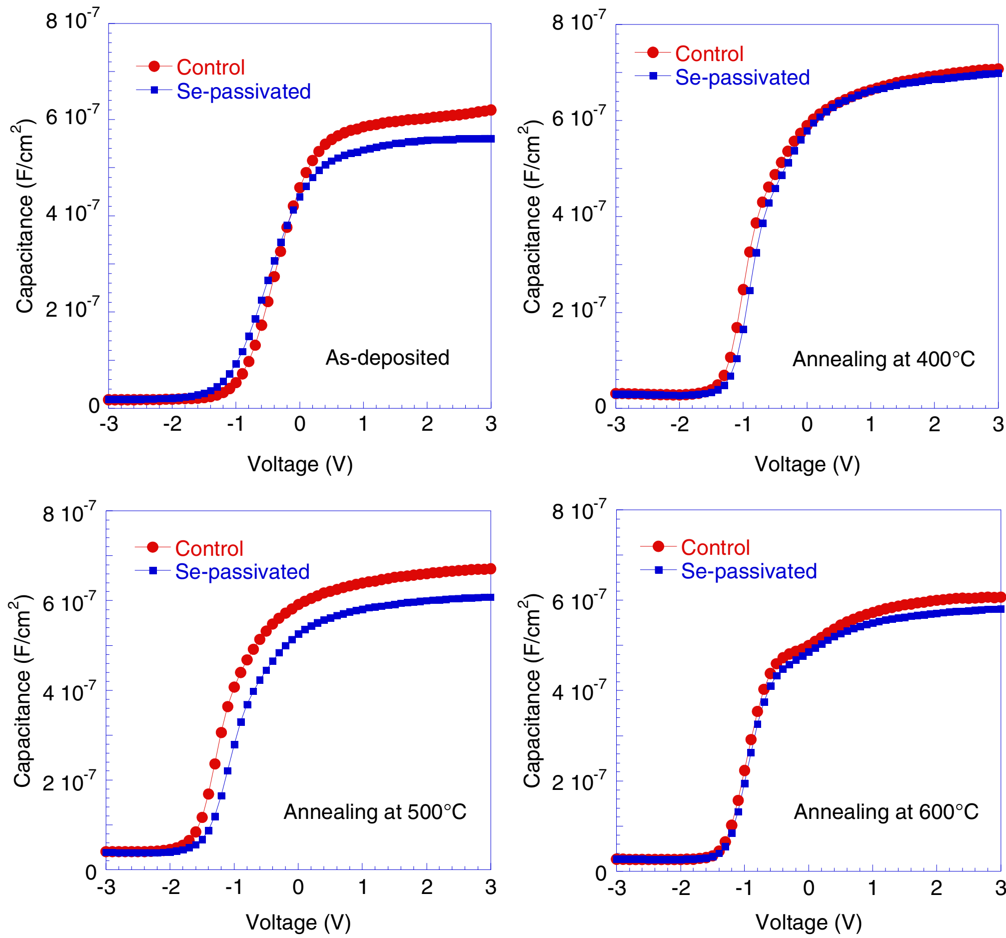


Figure 4.2 C-V characterizations of control and Se-passivated samples by reactive sputtering at different annealing temperatures. [72]

4.3 Results and Discussion

4.3.1 HfO_2 by Reactive Sputtering

Since sputtering is the standard process in the CMOS industry devices fabrication , the author started with HfO_2 by reactive sputtering. Figure 4.2 shows high frequency (500 MHz) C-V curve for both control and Se-passivated samples. It shows

no obvious difference between control and passivated samples. With 40 Å Hf, after fully oxidized into HfO_2, it forms ~ 49 Å HfO_2 with *EOT* of ~ 10 Å. The *EOT* obtained here is between 48 and 61 Å and is much larger than 10 Å. This indicates a thick interfacial layer about 38 to 51 Å formed between HfO_2 and Si.

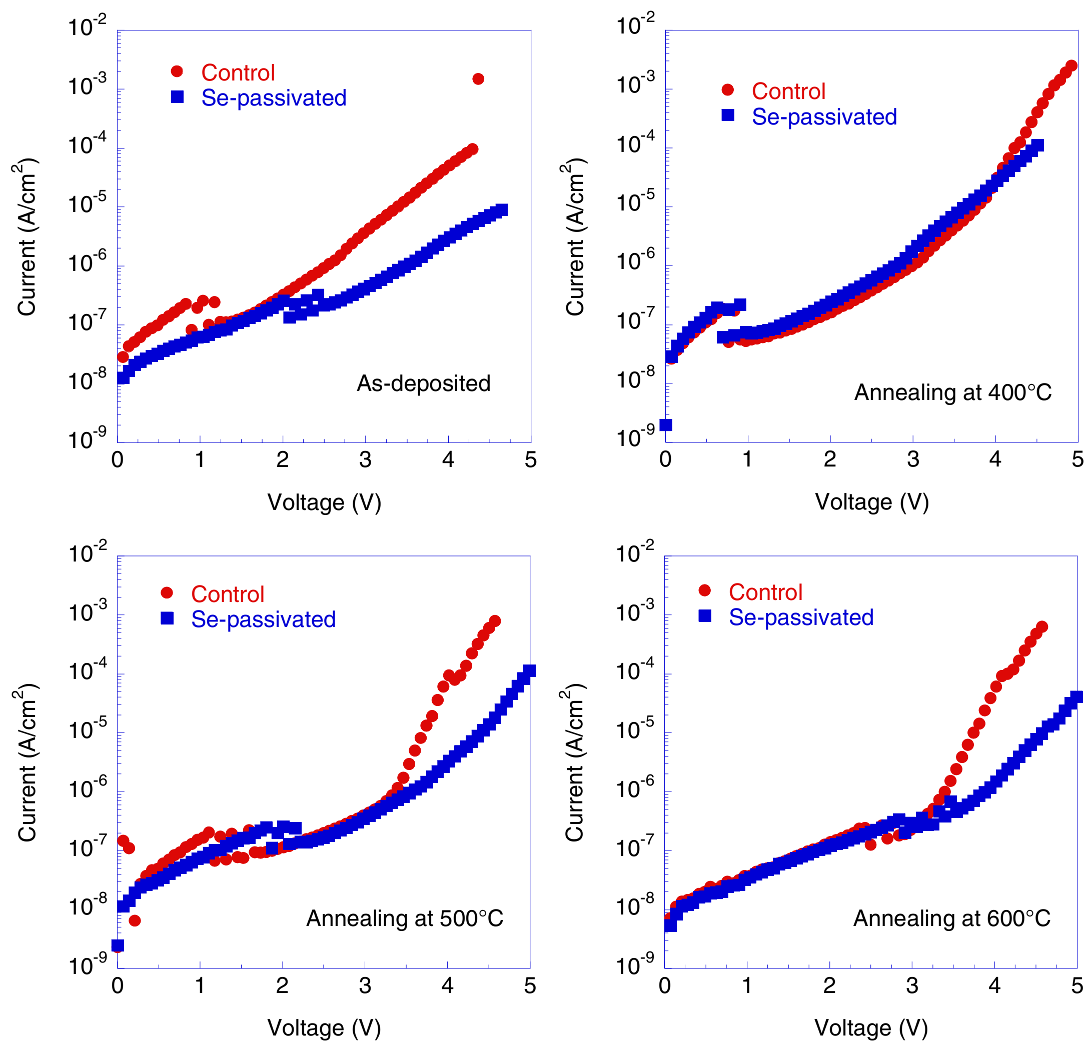


Figure 4.3 I-V characterizations of control and Se-passivated samples by reactive sputtering at different annealing temperatures.[72]

I-V curves in Figure 4.3 also show similar characteristics. The effect of Se passivation disappears. The possible reason can be due to the plasma during HfO_2

deposition process. Because the plasma is so reactive, it can damage the Se passivation layer. Hence, O atoms can easily react with Si to form the interfacial layer without Se passivation.

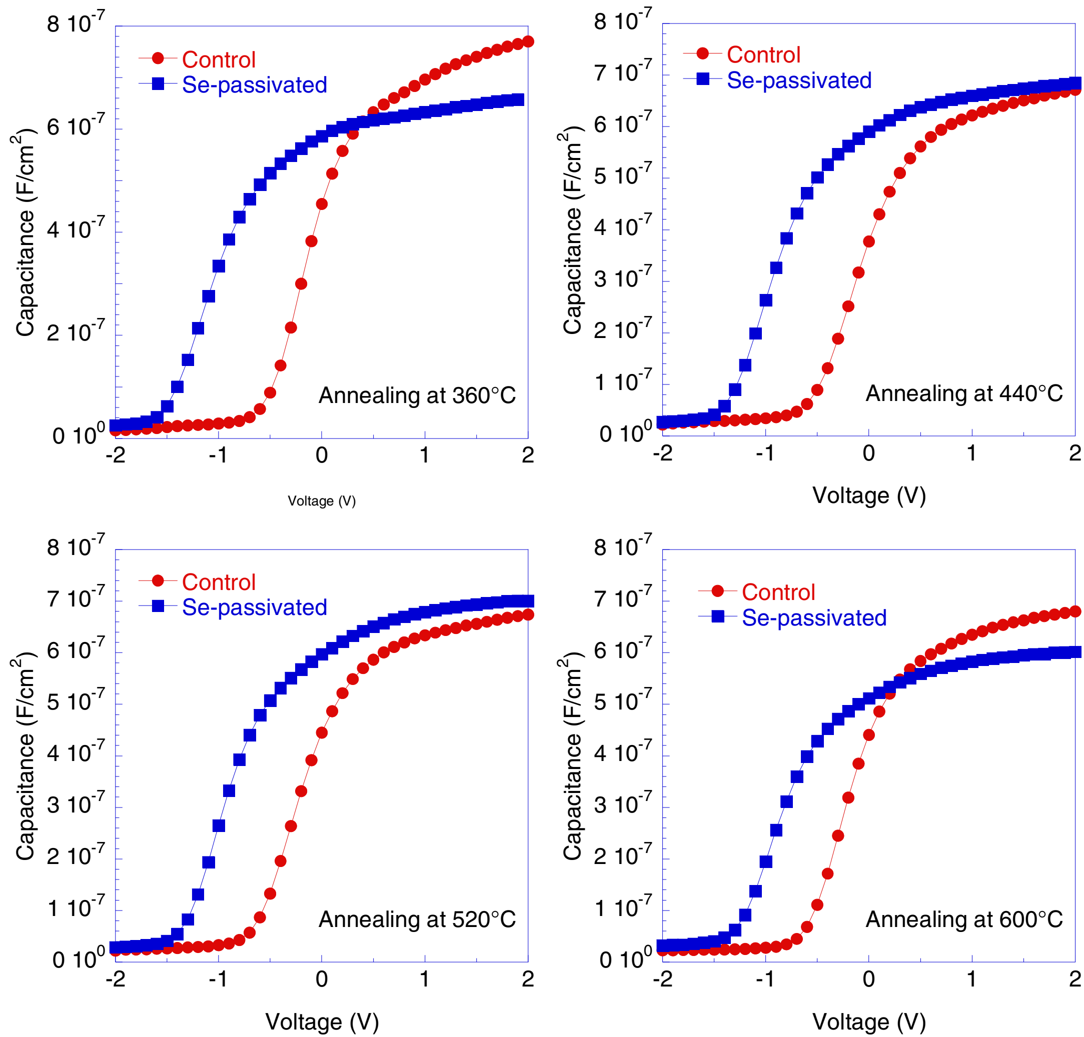


Figure 4.4 C-V characterizations of control and Se-passivated samples by O_3 oxidation at different annealing temperatures. [72]

4.3.2 HfO_2 by O_3 Oxidation

Figure 4.4 shows the C-V results for the control and Se-passivated samples formed by O_3 Oxidation. The most noticeable difference between control and

Se-passivated samples is the large negative shift of C-V curves for Se-passivated samples. With the methods described in section 4.2, Figure 4.5 plots the flat-band voltage and ΔV_{FB} between control and Se-passivated samples as a function of oxidation temperature. For the Se-passivated samples, V_{FB} decreases slowly to zero as the temperature increases, while the tendency for control samples is opposite. So the ΔV_{FB} decreases with the oxidation temperature, from 0.95 V at 360°C to 0.36 V at 600°C. The range of *EOT* is between 44 and 57 Å.

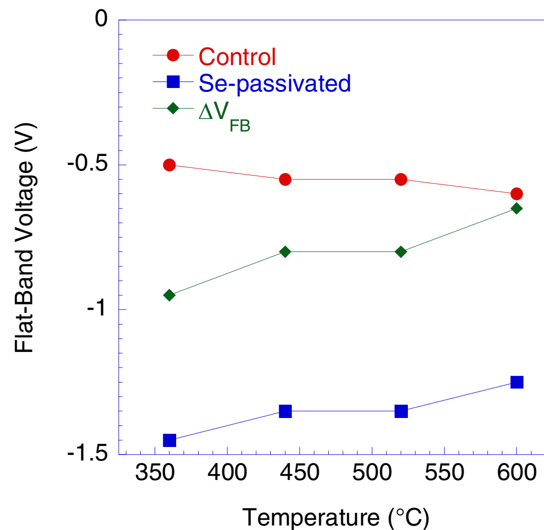


Figure 4.5 Flat-band voltages as a function of oxidation temperature for control and Se-passivated samples oxidized in O_3. [72]

Figure 4.6 shows the *EOT* as a function as the oxidation temperature. The samples show a different *EOT* trend with different oxidation temperature. For the control samples, *EOT* increases first and then saturates as the temperature increases. For the Se-passivated samples, *EOT* first decreases, and then increases. Since the *EOT* of HfO_2 is about 10 Å, the total *EOT* obtained by O_3 oxidation is still large and shows no improvement by Se passivation. Here, two reasons are proposed to account for the large

EOT. Firstly, O_3 is too reactive. Even at the lowest oxidation temperature 360°C, Se passivation can not prevent the O atom diffusion into the Si, which leads to the formation of the interfacial layer. Therefore, the Se-passivated samples are over-oxidized. Secondly, the large *EOT* is partially due to contamination on the wafer surface before Hf deposition. This contamination is inevitable because of the wafer exposure to air during transportation from the MBE system to the E-beam evaporation system. In general, the contamination layer is around 10-20 Å thick. For the control samples, this is chemisorbed contamination, while for the Se-passivated samples, it is physisorbed contamination.

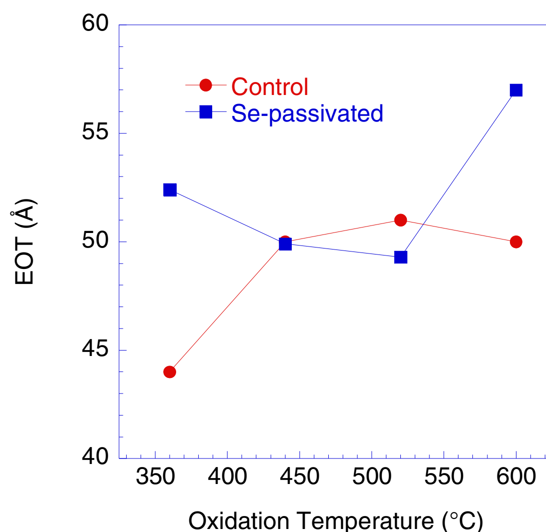


Figure 4.6 *EOT* as a function of oxidation temperature for control and Se-passivated samples oxidized in O_3. [72]

The analysis above depicts a possible structure for the Se-passivated samples, which is shown in Figure 4.7. The O atoms will pass through the Se passivation layer and react with Si to form the SiO_2 interfacial layer. The Se monolayer is sandwiched between the contamination and SiO_2. It is likely that Se monolayer forms a layer of

positive charges, causing the negative shift of the flat-band voltage.

Figure 4.8 shows the leakage current of the passivated and control samples. At 360°C, the leakage current of the Se-passivated sample is one order of magnitude lower than that of the control sample. As the oxidation temperature increases, leakage current of the control and Se-passivated samples behave quite similarly and effect of Se passivation disappears.

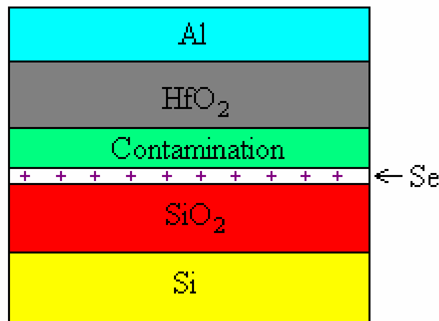


Figure 4.7 Illustration of the Se monolayer sandwiched in the dielectric stack after O_3 oxidation. [72]

Since Se-passivated samples with HfO_2 by sputtering and O_3 oxidation show no improvement on *EOT* and leakage current partially due to the "hard" fabrication process, a "soft" HfO_2 growth is needed, which leads to the HfO_2 formed by dry oxidation.

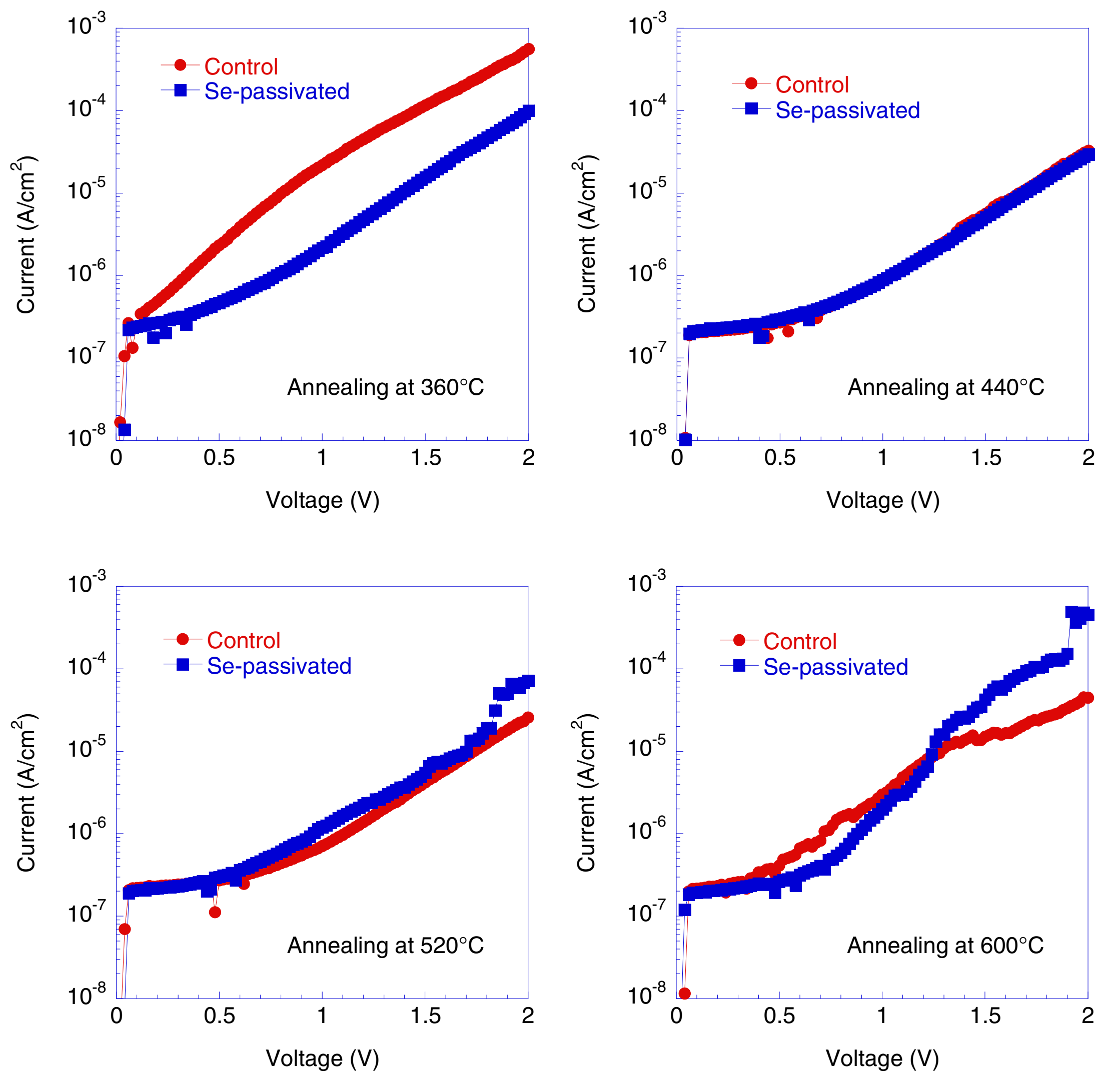


Figure 4.8 I-V characterizations of control and Se-passivated samples by O_3 oxidation at different annealing temperatures. [72]

4.3.3 HfO_2 by Dry Oxidation

Dry oxidation was performed from 300 to 600°C at intervals of 100. Figure 4.9 shows the high frequency C-V curves for control and Se-passivated samples. The smallest *EOT* of 31 Å is from the Se-passivated samples oxidized at 300°C while the *EOT* of control samples is 65 Å. Since a contamination layer is easily formed on the Si

surface before HfO_2 deposition, the total *EOT* has three contributors: high-*k*, interfacial layer, and surface contamination layer. By assuming a 15 Å contamination layer on the surface, the interfacial layer of the Se-passivated sample only contributes 6 Å to the *EOT* since *EOT* of HfO_2 is ~10 Å, while the interfacial layer of the control sample contributes 40 Å to the *EOT*. This indicates Se passivation can effectively suppress the interfacial layer formation at HfO_2/Si interface. Also, the corresponding flat-band voltage of Se-passivated sample at 300°C is -0.2 V, which is close to the theoretical value -0.14 V for this MOS capacitor: Al gate electrode and low 10^{14} cm^{-3} n-type Si.

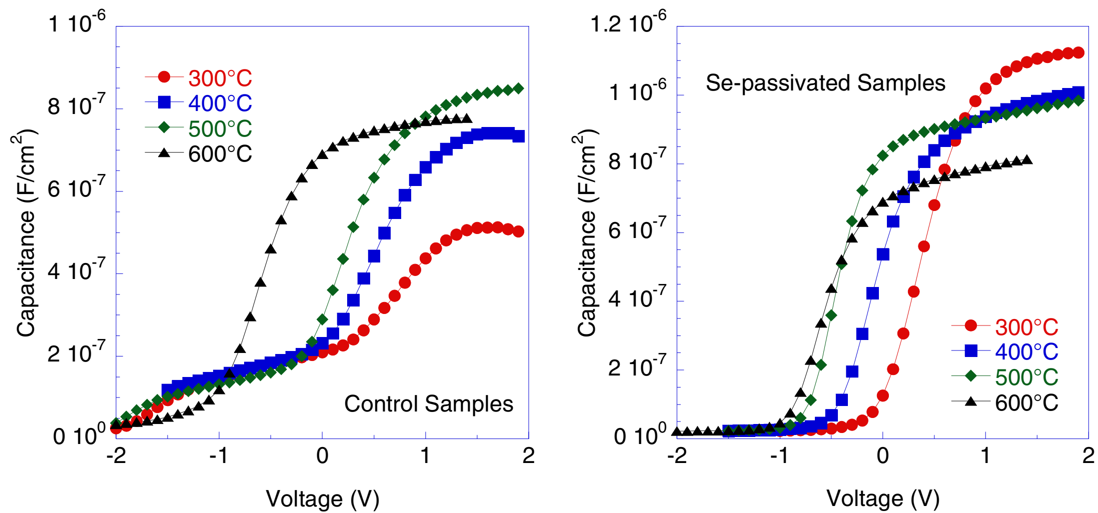


Figure 4.9 C-V characterizations of control and Se-passivated samples by dry oxidation at different temperatures. [72]

As shown in Figure 4.10, the *EOT* of the Se-passivated samples increase from 31 Å at 300°C to 42 Å at 600°C and the *EOT* of the control samples decrease from 65 Å at 300°C to 45 Å at 600°C when the oxidation temperatures increase. Obviously the *EOT* of the Se-passivated samples is always smaller than that of control samples, indicating that the Se monolayer suppresses Si oxidation up to 600°C. In addition, the

Se-passivated samples show gradual negative shift in flat-band voltage from -0.2 V at 300°C to -0.95 V at 600°C, which is shown in Figure 4.11. So the combination of the trend of *EOT* and shift of flat-band voltage supports our theory that Se monolayer becomes a layer of positive charge sandwiched between the contamination and SiO_2. As the oxidation temperature increases, O atoms will pass through Se monolayer to react with Si and Se atoms will be trapped in the dielectric stack and becomes a layer of positive charge. Then the *EOT* of Se-passivated samples increases and flat-band voltage moves towards negative direction.

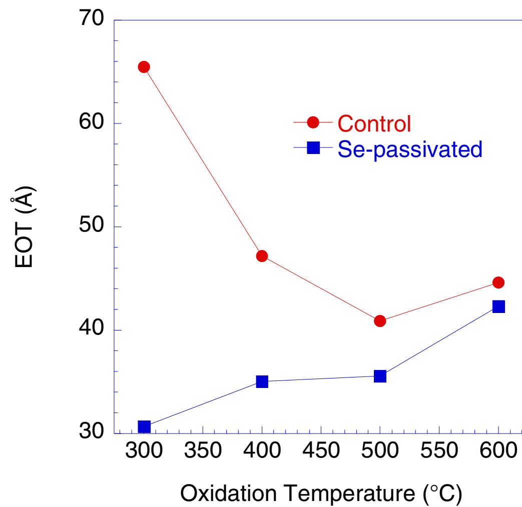


Figure 4.10 *EOT* as a function of oxidation temperature for control and Se-passivated samples by dry oxidation. [72]

For the control samples, C-V curve at 300 and 400°C show that the accumulation capacitance does not stay at a constant. On the contrary, it decreases when the bias voltage goes more positive. This indicates that the dielectric stack is leaky under large positive bias. The possible reason is that Hf film is only partially oxidized at 300 and 400°C. Compared with Se-passivated samples oxidized at the same temperature,

it seems that the Hf on Se-passivated samples is fully oxidized. At 500 and 600°C, the control samples show well-behaved C-V curves, which suggest that 450°C could be the minimum temperature for Hf to be fully oxidized into HfO_2 in O_2 on bare Si (100). This agrees quantitatively with a previous study of Hf oxidation.[73]

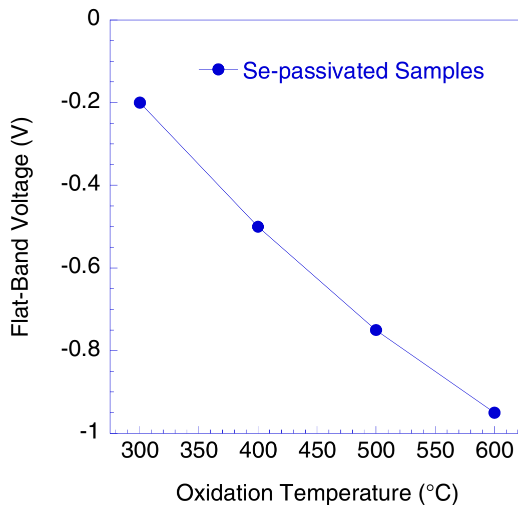


Figure 4.11 Flat-band voltage as a function of oxidation temperature for Se-passivated samples by dry oxidation.[72]

Figure 4.12 illustrates the leakage current of the passivated and control samples. At all the temperatures, the passivated samples show orders of magnitude lower leakage current than the control samples. At 300 and 400°C, the Hf film on the control samples is partially oxidized, which explains the larger leakage current for these samples. At 500 and 600°C, the Se-passivated samples show a smaller leakage current, while *EOT* is also smaller for the Se-passivated samples compared with the control samples. This indicates the improvement of high-*k*/Si interface quality by Se passivation: small *EOT* with low leakage current.

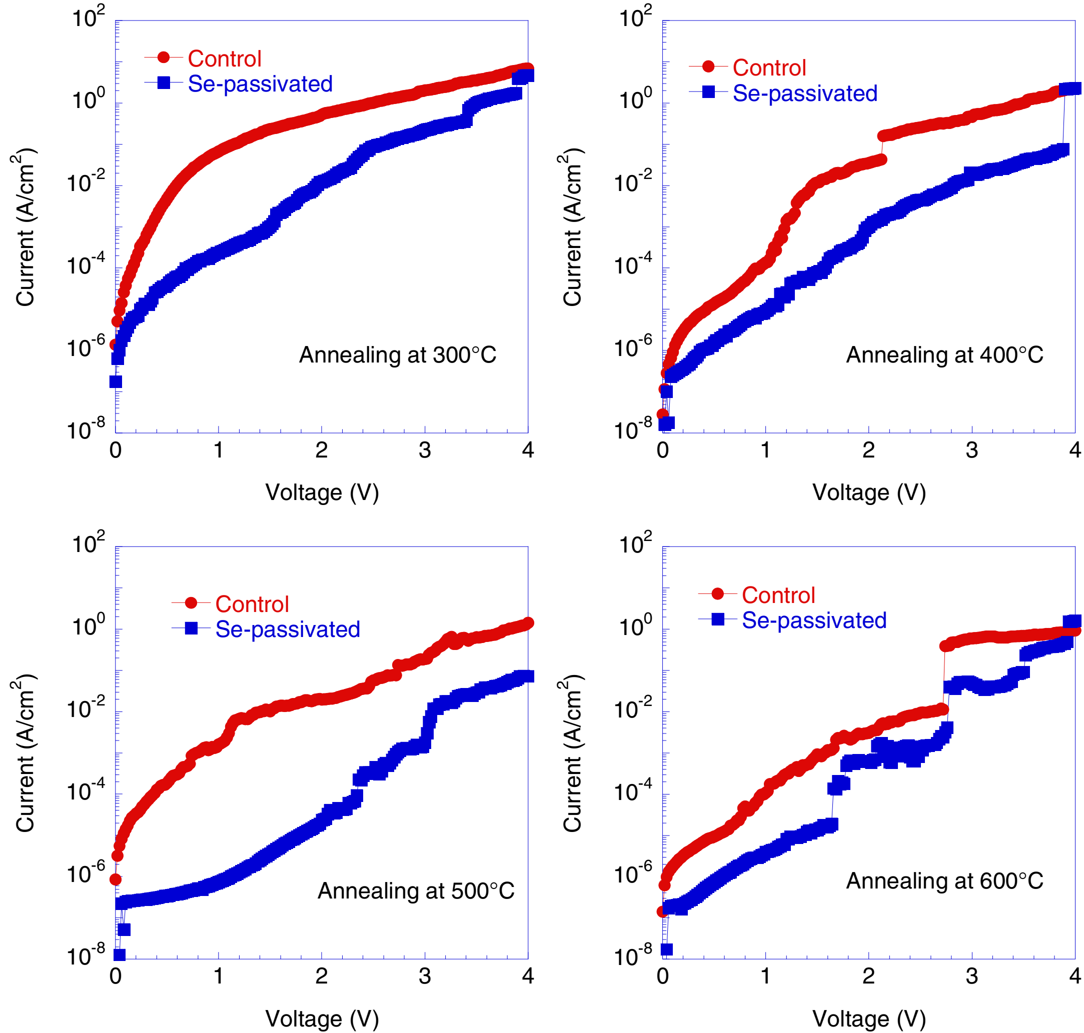


Figure 4.12 I-V characterizations of control and Se-passivated samples by dry oxidation at different temperatures. [72]

4.4 Summary

Se passivation is utilized to engineer the high-*k*/Si interface for future CMOS nanoelectronics. C-V and I-V characterization for HfO_2 by reactive sputtering and O_3 oxidation show no improvement by Se passivation. With HfO_2 formed by dry oxidation, Se-passivated sample oxidized at 300°C shows much improved properties: the smallest *EOT* ~31 Å, a flat-band voltage -0.2 V close to theoretical value, and a small leakage

current which is orders of magnitude lower than the control samples. The Se-passivated samples always show smaller *EOT* than the control samples up to 600°C, which indicates the effect of interfacial layer formation suppression by Se passivation.

CHAPTER 5

LOW RESISTANCE TITANIUM/N-TYPE SILICON (100) CONTACTS BY MONOLAYER SELENIUM PASSIVATION

With the removal of dangling bonds by monolayer Se passivation, a small work function metal will lead to a low Schottky barrier height for electron, and sequentially, a low contact resistivity on n-type Si. In this chapter, result for Ti/n-Si (100) contact resistance lowering by Se passivation is reported. [74]

5.1 Experiments

5.1.1 Wafer Preparation

Three n-type Si (100) wafers with different resistivities (16-24 Ω·cm, 0.075-0.085 Ω·cm and <0.004 Ω·cm) are chosen. The wafers are first rinsed in de-ionized water for 2 minutes and then dipped into 2% HF for 35 seconds to remove the native oxide and be terminated by H atoms. After HF dip, the wafer is blown dry with N_2 and loaded into the MBE system.

5.1.2 Se Passivation

Using the method described in section 3.3, a 500 Å Si buffer layer is deposited for sheet and contact resistance measurements. 10 and 50 Å Si buffer layers are deposited on SOI wafer for contact resistivity measurement. A control wafer is fabricated without Se passivation for comparison.

5.1.3 Photolithography

The wafers are spin-coated with HMDS (Hexamethyldisilazane) at 4000 rpm for 30 seconds and S1808 (photoresist) at 2000 rpm for 30 seconds, consecutively. Then a post baking is applied to the wafers at 90°C for 35 seconds. After that, wafers are exposed under mask by UV lamp for 50 seconds. Then the wafers are dipped in develop solution for 35 seconds for pattern transformation.

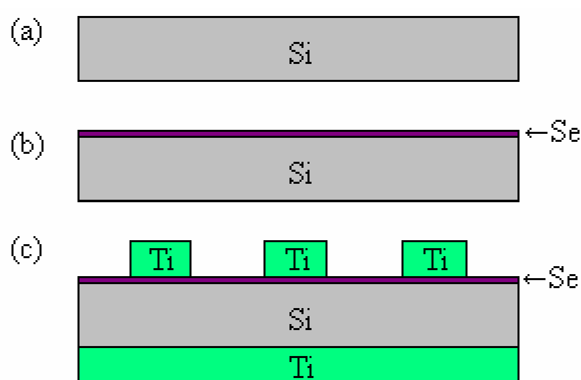


Figure 5.1 Fabrication processes of the experiments: (a) wafer preparation; (b) Se monolayer passivation; (c) Photolithography, Ti deposition for front contact and back contact followed by thermal annealing.

5.1.4 Metal Deposition

After photolithography, both control and Se-passivated samples are cut into small pieces and loaded into the E-beam evaporator. After pumping to ~ 2×10^{-6} Torr, 1000, 500, 300 and 100 Å Ti are deposited on the passivated side and 500 Å Ti is deposited on the back side for contact.

5.1.5 Post-Deposition Annealing

Both control and Se-passivated samples are loaded into a home-made furnace. After pumping to a base pressure ~ 10^{-6} Torr, ultra-pure N_2 is introduced into the

furnace at 1 atm. The samples are annealed at 300, 400, 500, 600 and 700ºC for 1 minute.

Figure 5.1 shows the fabrication process flow for the experiments.

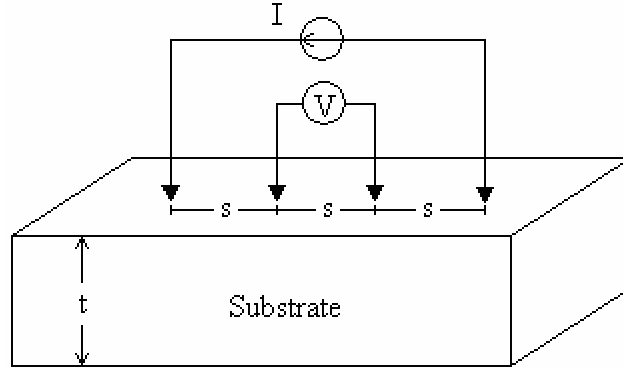


Figure 5.2 Sheet resistance measurements by four-point probe method.

5.2 Characterization

5.2.1 Current-Voltage Characterization

Current-voltage (I-V) measurement is the method to estimate the barrier height. For lower doping concentration substrate, the I-V characteristics is given by[15]

$$I = AA^* T^2 \exp(-\frac{q\Phi_B}{kT})(e^{\frac{qV}{kT}} - 1) \tag{5.1}$$

where Φ_B is the barrier height, A is the contact area, and A^* is the effective Richardson constant and. The extrapolated value of current density at zero voltage is the saturation current I_s and the barrier height can be obtained from the equation

$$\Phi_B = \frac{kT}{q} \ln\left(\frac{AA^* T^2}{I_S}\right) \tag{5.2}$$

5.2.2 Four-Point Probe Method

The four-point probe technique is one of the most common methods for measuring the semiconductor sheet resistance. Figure 5.2 shows a simple plot for the four-point probe technique. For the thin film layer with constraint $t \leq s/2$, the sheet resistance R_s is given by[75]

$$R_s = \frac{\pi}{\ln 2}\frac{V}{I} = 4.532\frac{V}{I} \tag{5.3}$$

where t is the layer thickness and s is the probe space. When the metal is deposited on the Si substrate, a two layer structure is formed.

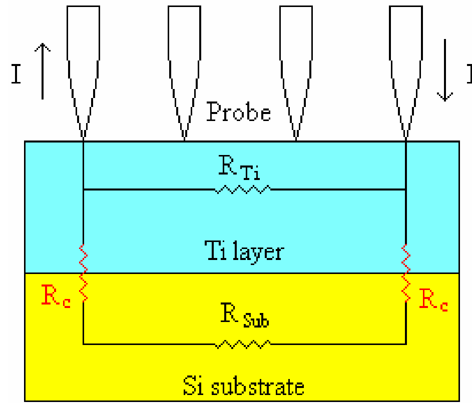


Figure 5.3 Current paths for Ti/Si two layer structures in R_s measurements.

The sheet resistance measurement for this two layer structure is illustrated in Figure 5.3. It indicates that current will flow in two parallel paths: the metal layer path and the substrate layer path. Before entering and exiting the substrate path, current has to pass the metal/Si contact. So the total resistance R_{total} can be expressed by

$$\frac{1}{R_{total}} = \frac{1}{R_m} + \frac{1}{R_{sub} + 2R_c} \tag{5.4}$$

so

$$\frac{1}{R_{s-total}} = \frac{1}{R_{s-m}} + \frac{1}{R_{s-sub} + 2GR_c} \tag{5.5}$$

where R_m is the metal resistance, R_{sub} is the substrate resistance, R_c is the metal/Si contact resistance, $R_{s\text{-}total}$ is the total sheet resistance, $R_{s\text{-}m}$ is the metal sheet resistance, $R_{s\text{-}sub}$ is the substrate sheet resistance, and G is the geometric factor. Rearranging Eq. (5.5),

$$R_c = \frac{1}{2G}\left(\frac{R_{s-m}R_{s-total}}{R_{s-m} - R_{s-total}} - R_{s-sub}\right) \tag{5.6}$$

Eq. (5.6) indicates that contact resistance can be extracted by the sheet resistance measurement.

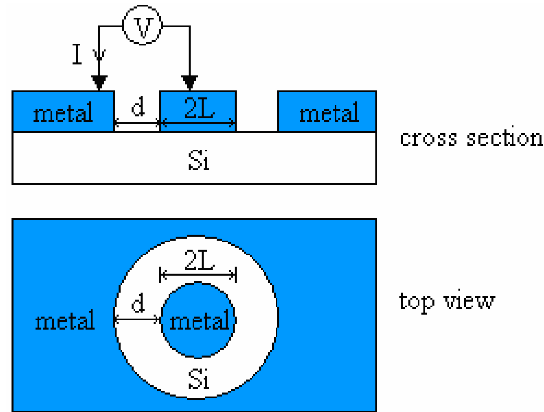


Figure 5.4 Structure of circular transmission line method for contact resistivity measurements.

5.2.3 Circular Transmission Line Method

The circular transmission line method (C-TLM) is a commonly used technique for the contact resistivity extraction.[76] Figure 5.4 shows the structure for C-TLM. The blue region is covered with metal as contact and blank region is the Si substrate. When $\rho_c > 0.2R_s t^2$ (t is the substrate thickness) is satisfied, the measured resistance R between

the internal and external metal contacts is given by[76]

$$R = \frac{R_s}{2\pi}\left[\frac{L_T}{L} + \frac{L_T}{L+d} + \ln\left(1+\frac{d}{L}\right)\right] \quad (5.7)$$

In Eq. (5.7), R_s is the sheet resistance of substrate, L_T is the transfer length given by $L_T = \sqrt{\rho_c / R_s}$, ρ_c is the contact resistivity, L is radius of internal contact, and d is the space between internal and external contacts. For $2\pi(L + d) >> d$, Eq. (5.7) simplifies to

$$R = \frac{R_s}{2\pi L}(d + 2L_T) \quad (5.8)$$

Eq. (5.8) indicates that by plotting the measured resistance R as the function of the space d, the transfer length L_T can be determined by the intercept on the resistance axis. Then the contact resistivity can be extracted from $L_T = \sqrt{\rho_c / R_s}$. It is noticed that Eq. (5.8) is valid with two assumption $\rho_c > 0.2 R_s t^2$ and $2\pi(L + d) >> d$. So for the substrate, a n-type Si-On-Insulator (SOI) wafer with 2.5 ± 0.5 µm Si and high doping concentration 10^{19} cm^{-3} is chosen to achieve a low substrate sheet resistance and thin substrate layer, which is to satisfy $\rho_c > 0.2 R_s t^2$. For the structure pattern, L is chosen at 50 µm and d is chosen from 10 to 60 µm with an interval of 10 µm to meet $2\pi(L + d) >> d$.

5.3 Results and Discussion

5.3.1 I-V Characterization

Figure 5.5 shows the I-V characteristics for the Se-passivated and control samples with low 10^{15} cm^{-3} n-type doping Si (100). Both samples show linear I-V behaviors at room temperature. But the control sample starts to show signs of rectification at 244 K, while the Se-passivated sample remains ohmic till 141 K, the

lowest temperature in our probe station. This suggests that the Schottky barrier height with Se passivation is much lower that that without Se passivation. This is because Eq. (5.1) depicts the ideal measurement for I-V characterization. Actually, the series resistance R_s (from the bulk neutral region and/or probe station holder and/or the metal layer especially when the metal layer is thin) must be considered in the practical measurement. The applied voltage will be divided into two parts: the voltage drop on the metal/Si contact and the voltage drop on the series resistance. So Eq. (5.1) should be adjusted as below:

$$I = AA^*T^2 \exp\left(-\frac{q\Phi_B}{kT}\right)\left[\exp\left(\frac{q(V-IR_s)}{kT}\right)-1\right] \tag{5.9}$$

For the measurement at room temperature, the contact resistance of control and Se-passivated samples are smaller than the series resistance. Both samples show linear I-V curves because most of the bias voltage is applied on the series resistance. As the measurement temperature decreases, Eq. (2.7a) indicates that the contact resistance of both control and Se-passivated samples will increase. So at 244 K, the contact resistance of the control sample is larger than the series resistance, and the current-voltage behavior shows signs of rectification, while at 141 K the contact resistance of the Se-passivated sample is still smaller than series resistance and the current-voltage behavior remains ohmic. So the contact resistance of the control sample increases faster than that of Se-passivated samples. Since the measurement temperature for the Se-passivated sample is even lower than that of control sample, Eq. (2.7a) suggests that the Schottky barrier height of Se-passivated samples is lower than that of control sample.

A simple-minded fitting of the I-V curves indicates a barrier height of less than ~ 0.1 eV for the Se-passivated sample and less than ~ 0.3 eV for the control sample. The significant lowering of barrier height will lead to Ti/n-type Si (100) with low contact resistance.

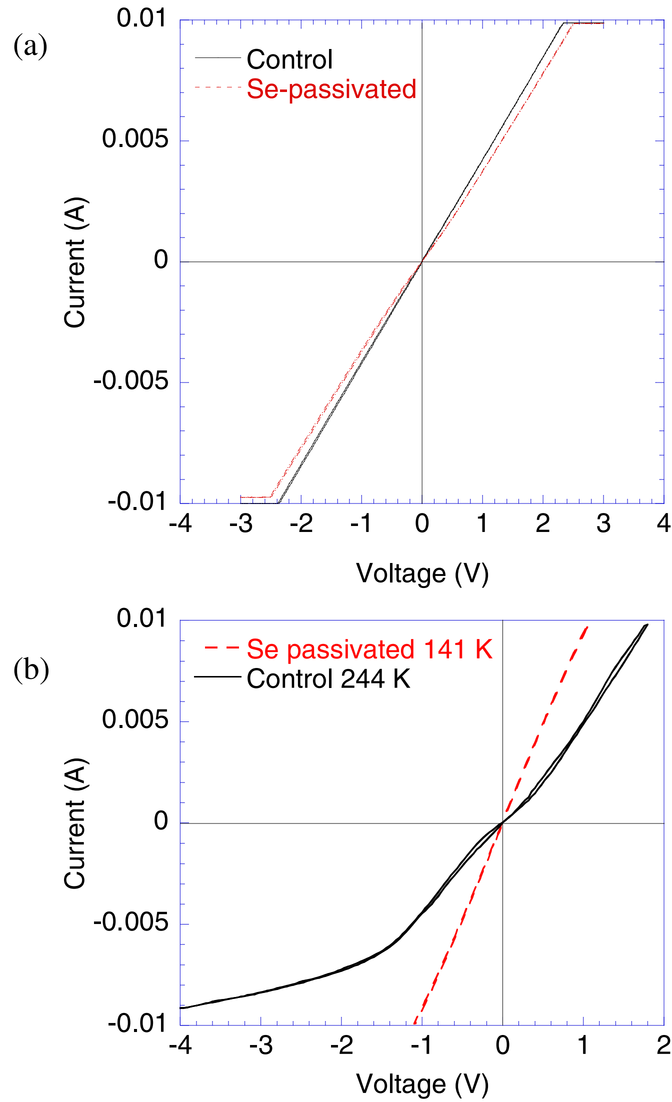


Figure 5.5 I-V characteristics for the Se-passivated and control samples with low 10^{15} cm^{-3} n-type doping Si (100) at (a) room temperature (b)low temperature. [74]

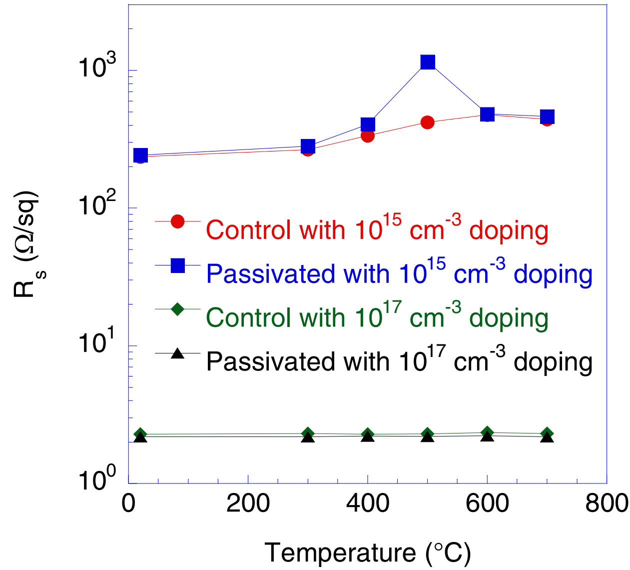


Figure 5.6 Sheet resistance as a function of annealing temperature for 100 Å Ti on Se-passivated and control n-type Si (100) samples. [74]

5.3.2 Sheet Resistance and Contact Resistance

Figure 5.6 shows the comparison of sheet resistance between Se-passivated and control samples under different annealing temperatures with 100Å Ti on low and moderately doped n-type Si (100) substrates. The difference in sheet resistance between passivated and control samples is not significant. The reason is that for the low and moderately doped substrates, the contact resistance is much smaller than the substrate series resistance, so reduction of sheet resistance by contact resistance reduction is too small to be observed. The effect of Se passivation is overshadowed.

The measured sheet resistance is given below:

$$\frac{1}{R_{s-total}} = \frac{1}{R_{s-m}} + \frac{1}{R_{s-sub} + 2GR_c} \tag{5.10}$$

For the low doped 10^{15} cm^{-3} substrate, R_{s-sub} is about 460 Ω/sq, and $2GR_c$ is less than

0.03 Ω/sq. Since $R_{s\text{-}sub} >> 2GR_c$, then $R_{s\text{-}total} \approx R_{s\text{-}m} // R_{s\text{-}sub}$. As the annealing temperature increases, Ti will gradually react with Si and form silicide phases with higher sheet resistance ($R_{s\text{-}m}$ > 440 Ω/sq). Therefore, the measured sheet resistance will increase with the annealing temperature due to the increasing of $R_{s\text{-}m}$. So quantitatively, $R_{s\text{-}sub}$ > 460 // 440 Ω/sq = 225 Ω/sq, which is consistent with the curves in Figure 5.6.

For the moderately doped 10^{17} cm^{-3} substrate, $R_{s\text{-}sub}$ is about 2.2 Ω/sq. With $R_{s\text{-}m} >> R_{s\text{-}sub} >> 2GR_c$, Eq. (5.10) points out that the $R_{s\text{-}total}$ approximately equals the $R_{s\text{-}sub}$. Since the substrate sheet resistance does not change during the annealing, the measured sheet resistance keeps constant at 2.2 Ω/sq with the annealing temperature, which is illustrated in Figure 5.6.

Since the sheet resistance of low and moderately doped substrate is much higher than the contact resistance, high doped substrate is chosen for minimizing the substrate resistance overshadow effect.

With high doping level 10^{19} cm^{-3}, since $R_{s\text{-}m} >> R_{s\text{-}sub}$ and $2GR_c$, Eq. (5.10) indicates $R_{s\text{-}total} \approx R_{s\text{-}sub} + 2GR_c$. In Figure 5.7, the sheet resistances of Se-passivated samples are ~ 30% lower than those of control samples on highly doped 10^{19} cm^{-3} Si (100) substrates. It suggests that on highly-doped substrates, substrate series resistances $R_{s\text{-}sub}$ are relatively small and contact resistances R_c contribute a significant fraction of the overall sheet resistances. Therefore, reduction in contact resistance by Se passivation becomes evident. By assuming parallel pathways in sheet resistance measurement of the Ti-Si contacts, Eq. (5.6) indicates that contact resistance can be extracted from the measured sheet resistance with known substrate sheet resistance and

Ti layer sheet resistance. The extracted contact resistances for control and Se-passivated samples are also shown in Figure 5.7. The results confirm that the contact resistance for the Se-passivated samples is generally lower than that of the control samples at all annealing temperatures. Se-passivated samples before annealing show about one order of magnitude lower contact resistance as compared with the control samples. The variation in contact resistance for the control samples with annealing temperature is thought to be caused by silicidation. On the contrary, the contact resistance for the Se-passivated samples does not fluctuate much with annealing temperature, which suggests, and has been confirmed, that Se passivation suppresses silicidation at the metal-Si interface.[77]

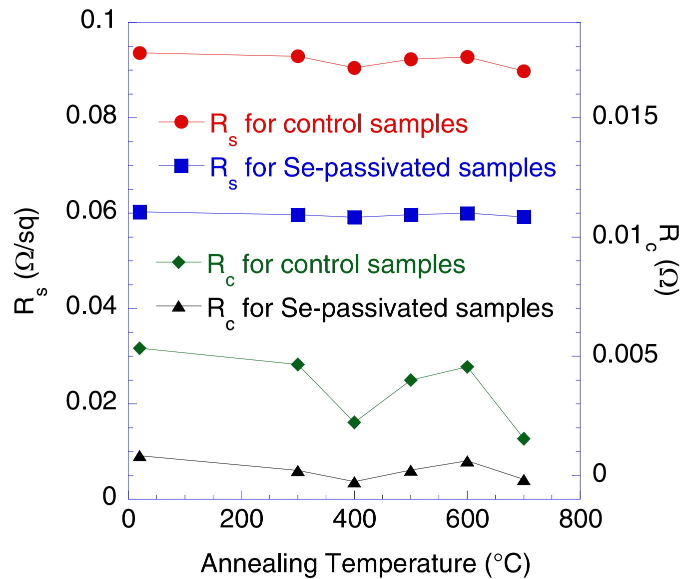


Figure 5.7 Comparison of sheet resistance and contact resistance as a function of annealing temperature for 100 Å Ti on Se-passivated and control n-type Si (100) samples with 10^{19} cm^{-3} doping.[74]

The comparison of contact resistance as a function of substrate doping level and Ti layer thickness for Se-passivated and control samples is shown in Figure 5.8. On 10^{17}

cm^{-3} doped n-type Si (100) substrates, contact resistances for the passivated and control samples cross each other and no consistent trend is observed. For 10^{19} cm^{-3} doped samples, contact resistances for the passivated samples are always lower then those for the control samples. These results are consistent with the sheet resistance measurements. Another interesting fact is that the contact resistance associated with thinner Ti layers is higher than that with thicker Ti layers for both passivated and control samples on the highly-doped substrates. This could be explained by interfacial reactions between the Ti layer and contaminants on the Si (100) surface since the percentage of the reacted volume for thinner Ti layers is larger.

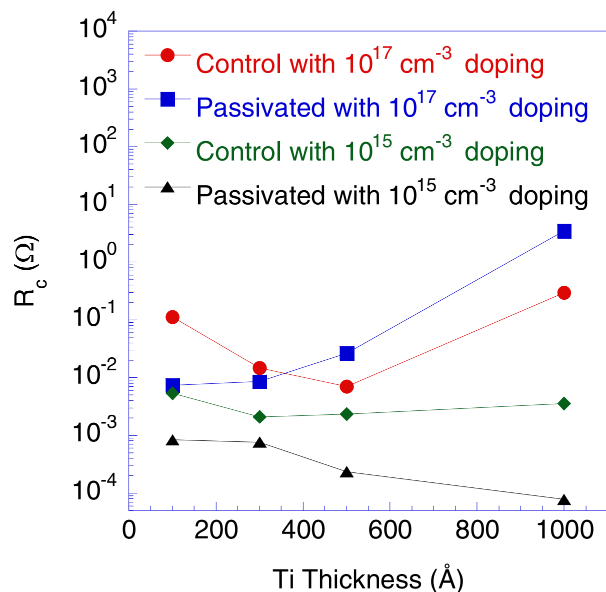


Figure 5.8 Comparison of contact resistance as a function of n-Si (100), substrate doping level and Ti layer thickness for Se-passivated and control samples. [74]

5.3.3 Contact Resistivity

Contact resistivity measurements by C-TLM for passivated and control samples on SOI substrates with 500-Å Si buffer layer and 500-Å Ti layer are shown in Figure 5.9. By fitting the data with a linear relation between measured resistance *R* and space *d*, the contact resistivity can be extracted by the method mentioned above.[74] The passivated samples show a much lower contact resistivity than the control samples, 6.23×10^{-6} $\Omega\cdot cm^2$ versus 1.82×10^{-4} $\Omega\cdot cm^2$. This is a 29 times reduction in contact resistivity between Ti and n-type Si (100) by Se passivation.

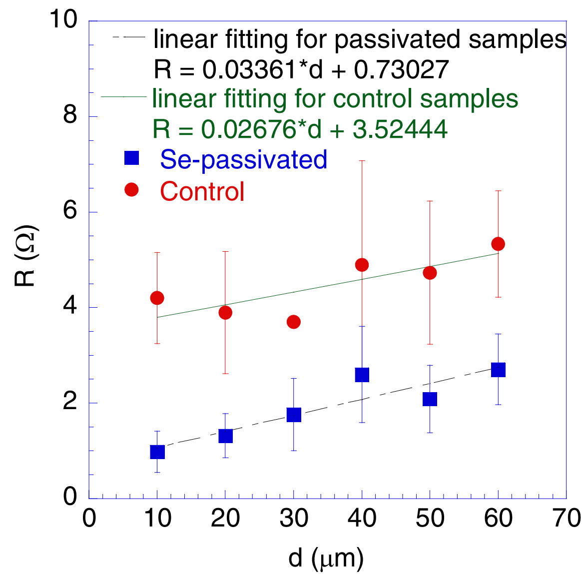


Figure 5.9 Linear fittings of the experimental data from the circular transmission line measurements of Se-passivated and control samples with 500 Å Si buffer layer and 500 Å Ti layer.[74]

Since contact resistance depends strongly on depletion layer thickness, an effect of the un-doped Si buffer layer thickness is expected on contact resistivity. As shown in Figure 5.10, the reduction in contact resistivity is a function of the Si buffer thickness for both passivated and control samples with 500 Å Ti plus 1500 Å Al. When the buffer

layer is 500 Å thick, Se passivation reduces the contact resistivity by ~ 125% in this experiment. If the buffer layer thickness is reduced to 50 and 10 Å, there is little difference between passivated and control samples. High resolution transmission electron microscopy has confirmed the existence of a moisture layer of ~ 1.5 nm shown in Figure 5.11 between Ti and Se-passivated Si (100) when the substrates are exposed to air before Ti deposition. The measured contact resistance R_c, therefore, has two components, the resistance through the Schottky barrier R_B and the resistance through the moisture layer R_T, $R_c = R_B + R_T$. With a thinner buffer layer, the resistance due to the Schottky barrier decreases significantly and the resistance through the moisture layer dominates. Therefore, the effects of Se passivation are overshadowed.

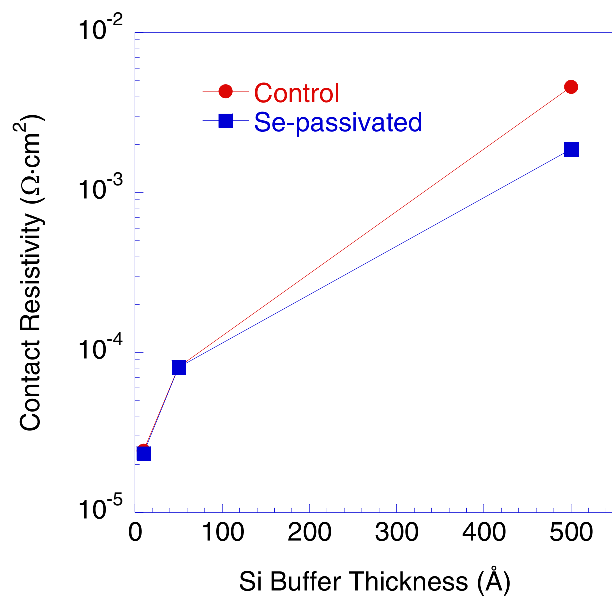


Figure 5.10 Comparison of specific contact resistance as a function of Si buffer layer thickness for Se-passivated and control samples with 500 Å Ti at bottom and 1500 Å Al on top.[74]

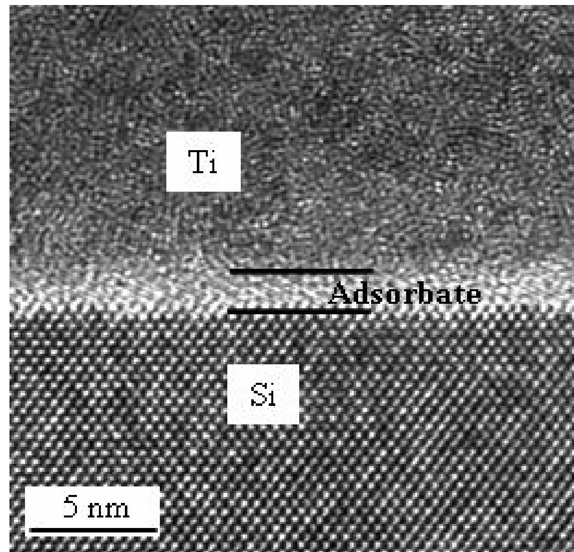


Figure 5.11 HRTEM image of surface adsorption layer between Ti and Si substrate.

5.4 Summary

The effect of Schottky barrier lowering on contact resistance between Ti and n-type Si (100) substrates by Se passivation is studied with four-point probe and C-TLM measurements. Sheet resistance of the Ti-Si contacts on Se-passivated 10^{19} cm^{-3} doped substrates shows a ~ 30% reduction as compared to the control samples. Accordingly, the extracted contact resistance decreases by about one order of magnitude for samples with different Ti thicknesses and different annealing temperatures. Reduction in contact resistance is not observed for substrates with 10^{15} and 10^{17} cm^{-3} doping levels. A 125%–2900% reduction in contact resistivity is achieved by Se passivation on highly-doped SOI substrates with 500 Å un-doped Si buffer layer. When the buffer layer thickness is reduced to 50 and 10 Å, the contact resistivities of the passivated and control samples reveal little difference.

CHAPTER 6

KINETIC MODEL FOR SILICON-GERMANIUM GROWTH FROM SILANE AND GERMANE BY CVD

In this chapter, a quantitative kinetic model[78] is presented for $Si_{1-x}Ge_x$ growth by CVD with GeH_4 and SiH_4 as the precursors. The model considers both heterogeneous and homogeneous reactions of the precursors. An analysis of the heterogeneous and homogeneous reactions points out that $Si_{1-x}Ge_x$ growth by CVD can be divided into two regimes: a heterogeneous decomposition dominated regime and a homogeneous decomposition dominated regime.

6.1 Process Principles and Deposition Mechanism

In general, the CVD process involves the following key steps:

(1) Generation of active gaseous reactant species.

(2) Transport of the gaseous species into the reaction chamber.

(3) Gaseous reactants undergo gas phase reactions forming intermediate species.

(4) Absorption of gaseous reactants onto the heated substrate, and the heterogeneous reaction occurs at the gas–solid interface (i.e. heated substrate) which produces the deposit and by-product species.

(5) The deposits will diffuse along the heated substrate surface and coarse forming a continuous film.

(6) Gaseous by-products are removed from the surface by desorption, diffusion and

convection.

(7) The unreacted gaseous precursors and by-products will be transported away from the deposition chamber.

6.2 Kinetics

6.2.1 Heterogeneous Decomposition

For a gas-solid heterogeneous unimolecular elementary reaction, there are two essential conditions for reactant molecules to deposit onto the substrate:

(i) The reactant molecules must be activated.

(ii) The reactant molecules must interact with the substrate.

If no surface process inhibits decomposition and deposition of activated reactant molecules, the growth rate depends only on the number of the activated reactant molecules which strike the substrate. Conditions (i) and (ii) point out that the energy of reactant molecules must be higher than a threshold energy E_a to decompose and deposit when they strike the substrate. Otherwise they will return into the gas phase after collisions.

Based on the collision theory of heterogeneous unimolecular reactions and statistical physics, the activated flux of a precursor, i.e. the number of precursor molecules or species that decomposes upon collision with the substrate, can be approximated by[79,80]

$$J = \frac{P}{(2\pi mkT)^{1/2}}\left(\frac{E_a}{kT}+1\right)\exp\left(-\frac{E_a}{kT}\right) \tag{6.1}$$

where k is the Boltzmann constant, T is the absolute deposition temperature, P, m, and

E_a are the precursor's partial pressure, molecular mass, and activation energy for its heterogeneous decomposition reaction on the substrate, respectively.

Table 6.1 Most likely heterogeneous reactions in $Si_{1-x}Ge_x$ CVD from GeH_4 and SiH_4

Notation	Description	Reactions
$J_{GeH4/Ge}$	GeH_4 flux on Ge sites	$GeH_4(g) + 2\text{-}Ge(s) = H_3Ge\text{-}Ge(s) + H\text{-}Ge(s)$
$J_{GeH4/H\text{-}Ge}$	GeH_4 flux on H-Ge sites	$GeH_4(g) + H\text{-}Ge(s) = H_3Ge\text{-}Ge(s) + H_2(g)$
$J_{GeH4/Si}$	GeH_4 flux on Si sites	$GeH_4(g) + 2\text{-}Si(s) = H_3Ge\text{-}Si(s) + H\text{-}Si(s)$
$J_{GeH4/H\text{-}Si}$	GeH_4 flux on H-Si sites	$GeH_4(g) + H\text{-}Si(s) = H_3Ge\text{-}Si(s) + H_2(g)$
$J_{SiH4/Ge}$	SiH_4 flux on Ge sites	$SiH_4(g) + 2\text{-}Ge(s) = H_3Si\text{-}Ge(s) + H\text{-}Ge(s)$
$J_{SiH4/H\text{-}Ge}$	SiH_4 flux on H-Ge sites	$SiH_4(g) + H\text{-}Ge(s) = H_3Si\text{-}Ge(s) + H_2(g)$
$J_{SiH4/Si}$	SiH_4 flux on Si sites	$SiH_4(g) + 2\text{-}Si(s) = H_3Si\text{-}Si(s) + H\text{-}Si(s)$
$J_{SiH4/H\text{-}Si}$	SiH_4 flux on H-Si sites	$SiH_4(g) + H\text{-}Si(s) = H_3Si\text{-}Si(s) + H_2(g)$

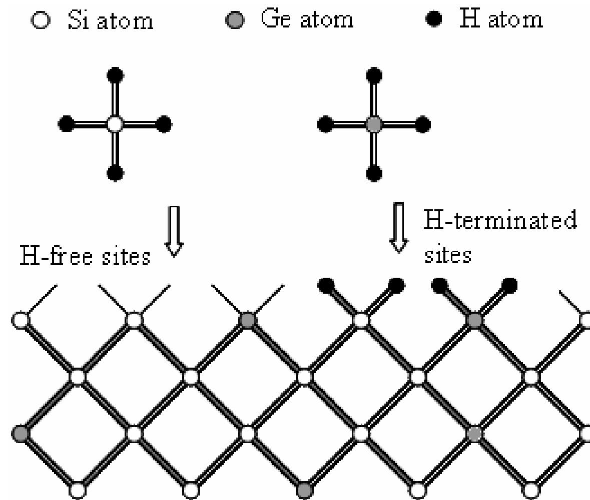


Figure 6.1 Heterogeneous reactions in $Si_{1-x}Ge_x$ CVD from SiH_4 and GeH_4. [78]

In $Si_{1-x}Ge_x$ CVD, there are four types of surface sites on the substrate: H-terminated Si sites (H-Si), H-terminated Ge sites (H-Ge), H-free Si sites (-Si), and H-free Ge sites (-Ge). With two precursors involved (SiH_4 and GeH_4), there are a total of eight most likely heterogeneous reactions on the substrate, which are listed in Table 6.1 and depicted in Figure 6.1. The activation energies for reactions on H-terminated Si and Ge sites are larger than those on H-free Si and Ge sites. As an example, the

activation energy of SiH_4 adsorption on H-free Si sites is ~30 kcal/mol,[81] whereas that on H-terminated Si sites is ~51 kcal/mol.[82] Therefore, reaction fluxes on H-terminated Si and Ge sites can be neglected as compared to those on H-free Si and Ge sites. This reduces the number of reactions to consider down to four: GeH_4 flux on Ge sites ($J_{GeH4/Ge}$), GeH_4 flux on Si sites ($J_{GeH4/Si}$), SiH_4 flux on Ge sites ($J_{SiH4/Ge}$), and SiH_4 flux on Si sites ($J_{SiH4/Si}$). The total Ge and Si fluxes are given by[78]

$$J_{Ge} = J_{GeH_4/Ge} + J_{GeH_4/Si} \tag{6.2}$$

$$J_{Si} = J_{SiH_4/Ge} + J_{SiH_4/Si} \tag{6.3}$$

Table 6.2 Primary Ge and Si fluxes in $Si_{1-x}Ge_x$ CVD from GeH_4 and SiH_4

Flux	Reaction Equations
$J_{GeH4/Ge}$	$x(1-\theta_{Ge})\frac{P_{GeH_4}}{(2\pi m_{GeH_4}kT)^{1/2}}(\frac{E_{GeH_4/Ge}}{kT}+1)\exp(-\frac{E_{GeH_4/Ge}}{kT})$
$J_{GeH4/Si}$	$(1-x)(1-\theta_{Si})\frac{P_{GeH_4}}{(2\pi m_{GeH_4}kT)^{1/2}}(\frac{E_{GeH_4/Si}}{kT}+1)\exp(-\frac{E_{GeH_4/Si}}{kT})$
$J_{SiH4/Ge}$	$x(1-\theta_{Ge})\frac{P_{SiH_4}}{(2\pi m_{SiH_4}kT)^{1/2}}(\frac{E_{SiH_4/Ge}}{kT}+1)\exp(-\frac{E_{SiH_4/Ge}}{kT})$
$J_{SiH4/Si}$	$(1-x)(1-\theta_{Si})\frac{P_{SiH_4}}{(2\pi m_{SiH_4}kT)^{1/2}}(\frac{E_{SiH_4/Si}}{kT}+1)\exp(-\frac{E_{SiH_4/Si}}{kT})$

Based on Eq. (6.1), we can write down the equations for these four reaction fluxes as shown in Table 6.2. In these equations, x is the Ge content in the film. θ_{Si} and θ_{Ge} represent the ratio of H-terminated Si sites to all Si sites and the ratio of H-terminated Ge site to all Ge sites, respectively. P_{SiH4}, m_{SiH4}, P_{GeH4}, and m_{GeH4} are the SiH_4 partial pressure, SiH_4 molecular mass, GeH_4 partial pressure, and GeH_4 molecular mass, respectively. $E_{GeH4/Ge}$, $E_{GeH4/Si}$, $E_{SiH4/Ge}$, and $E_{SiH4/Si}$ are the activation energy for GeH_4

decomposition on H-free Ge sites, GeH_4 on H-free Si sites, SiH_4 on H-free Ge sites, and SiH_4 on H-free Si sites, respectively.

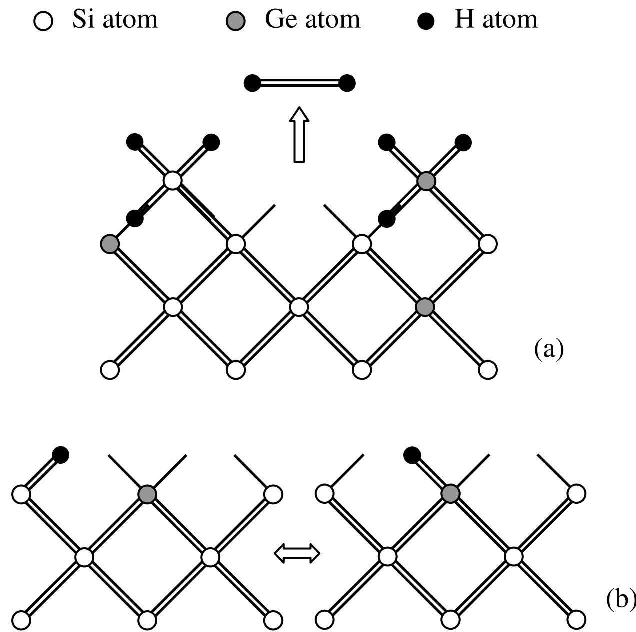
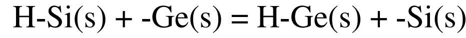


Figure 6.2 (a) H desorption from surface sites and (b) H diffusion between Ge and Si sites. [78]

6.2.2 Surface H Coverage

The effect of surface H coverage, θ_{Si} and θ_{Ge}, needs to be taken into account to understand the growth behavior of $Si_{1-x}Ge_x$ CVD. Liehr *et al*[83] and Greenlief *et al*[84] showed that in SiH_4 CVD, the H coverage of Si sites, θ_{Si}, decreases with higher temperatures and increases with larger flow rates of SiH_4. Surface H coverage in $Si_{1-x}Ge_x$ growth is more complicated due to the presence of Ge. Ning *et al*[85] observed H desorption at lower temperatures with increasing Ge content on the surface, which explained the significant increase in $Si_{1-x}Ge_x$ growth rate with the presence of Ge. Suemitsu *et al*[86] confirmed these results. The adsorption of SiH_4 and GeH_4 brings H to

the surface and H desorption removes H from the surface. In addition, H atoms diffuse between Ge and Si sites on the surface



H-Si(s) + -Ge(s) = H-Ge(s) + -Si(s)

which enhances H desorption. Figure 6.2 depicts these reactions. All of these processes make it difficult to derive an analytical equation for surface H coverage in $Si_{1-x}Ge_x$ CVD. For simplification, our model assumes that θ_{Ge} is negligibly small, i.e. $\theta_{Ge} \approx 0$. This is supported by the fact of the weaker Ge-H bond (90.8 kJ/mol enthalpy of formation for GeH_4) compared with the stronger Si-H bond (34.3 kJ/mol enthalpy of formation for SiH_4).[87] For θ_{Si}, we have found that one of the simplest mathematical relations provides a good fit to the experimental data at different GeH_4/SiH_4 ratios in the temperature range of 570–750°C

$$\theta_{Si} = \frac{1}{g(T, P_{SiH_4}) + h(T, P_{SiH_4}) P_{GeH_4}} \qquad (6.4)$$

where $g(T, P_{SiH4})$ (dimensionless) and $h(T, P_{SiH4})$ (in 1/sccm) are dependent only on temperature and SiH_4 partial pressure. Although Eq. (6.4) is empirical and $g(T, P_{SiH4})$ and $h(T, P_{SiH4})$ are fitting parameters, it indicates that, at any given temperature and SiH_4 partial pressure, θ_{Si} decreases with increasing GeH_4 partial pressure. This agrees with the fact that Ge incorporation enhances H desorption from the surface.

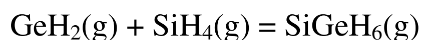
6.2.3 Homogeneous Decomposition

Depending on deposition pressure, SiH_4 homogeneously decomposes into SiH_2 and H_2 at temperatures as high as 950°C.[88,89] However, the temperature for $Si_{1-x}Ge_x$ growth by CVD is often between 450°C and 750°C, and thus homogeneous

decomposition of SiH_4 is not considered in our model. GeH_4 also homogeneously decomposes to GeH_2

$$GeH_4(g) = GeH_2(g) + H_2(g)$$

Tamaru *et al*[90] studied the kinetics of GeH_4 thermal decomposition and concluded that heterogeneous and homogeneous decomposition of GeH_4 can take place simultaneously. Hall[91] reported that heterogeneous decomposition of GeH_4 predominates at 300°C and/or small GeH_4 flow rates and homogeneous decomposition of GeH_4 predominates at 450°C and large GeH_4 flow rates. Hall also observed Ge deposition on the reactor wall prior to reaching the substrate at high temperatures and large GeH_4 flow rates due to homogeneous decomposition of GeH_4. A side effect of GeH_4 homogeneous decomposition is that it complicates the gas phase chemistry for both GeH_4 and SiH_4, especially at high temperatures and/or large GeH_4 flow rates. For example, GeH_2 can react with SiH_4 in the gas phase



$$GeH_2(g) + SiH_4(g) = SiGeH_6(g)$$

$SiGeH_6$ is more reactive than SiH_4, which can cause Si deposition on the reactor wall along with Ge and thus a decrease in $Si_{1-x}Ge_x$ growth rate. Since the temperature for homogeneous decomposition of GeH_4 is close to the deposition temperature of $Si_{1-x}Ge_x$ by CVD, GeH_2 is taken into account in our model.

6.3 Growth Rate

Jang *et al*.[65] reported an extensive study on ultrahigh vacuum CVD of $Si_{1-x}Ge_x$ from GeH_4 and SiH_4. In one experiment, they changed the flow ratio of GeH_4/SiH_4 from 1.25% to 5.75% and the deposition temperature from 570°C to 700°C, while keeping a

constant SiH_4 flow rate of 40 sccm and a constant H_2 flow rate of 80 sccm as the carrier gas. The resultant deposition pressure varied from 15 mTorr to 17 mTorr.

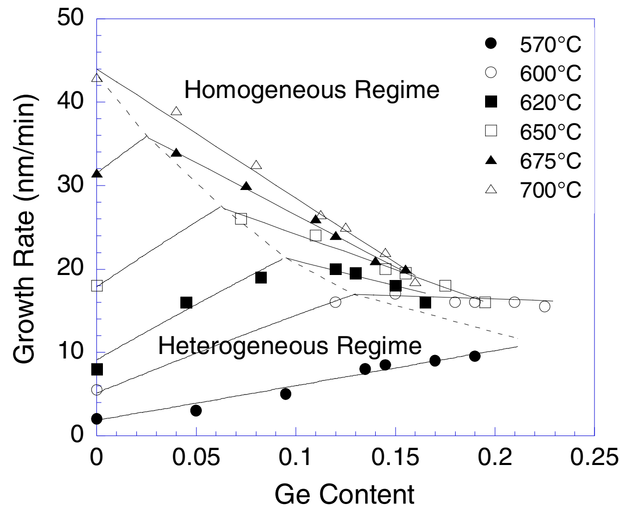


Figure 6.3 Growth rate as a function of Ge content at different temperatures. Solid lines are model predictions and experimental data from Ref. 65. SiH_4 flow rate is 40 sccm. The dash line is the boundary between homogeneous and heterogeneous regimes. [78]

Another experiment was carried out at a constant deposition temperature of 620°C with the SiH_4 flow rate ranging from 20 sccm to 80 sccm (GeH_4/SiH_4 ratio from 1.25% to 5.75%) without a carrier gas. In both experiments, they found that, as the Ge content in the film increased, the growth rate first increased and then decreased. The decrease in growth rate at high deposition temperatures and/or large GeH_4 flow rates (i.e. high Ge content) can be attributed to the effect of GeH_4 homogeneous decomposition on gas phase chemistry. Therefore, $Si_{1-x}Ge_x$ growth by CVD can be divided into two regimes: (1) a heterogeneous decomposition dominated regime at low temperatures and/or small GeH_4 flow rates where the growth rate increases with Ge content and (2) a homogeneous decomposition dominated regime at high temperatures

and/or large GeH_4 flow rates where the growth rate decreases with Ge content. The two regimes are illustrated in Figure 6.3.

6.3.1 Growth Rate in Heterogeneous Regime

In the heterogeneous decomposition dominated regime, the overall growth rate G (in nm/min) is proportional to the sum of J_{Ge} and J_{Si}[78]

$$G \propto J_{Ge} + J_{Si} = J_{GeH_4/Ge} + J_{GeH_4/Si} + J_{SiH_4/Ge} + J_{SiH_4/Si} \quad (6.5)$$

substituting the four equations in Table 6.2 into Eq. (6.5) and rearranging

$$G \propto xP_{GeH_4}A(T) + (1-x)(1-\theta_{Si})P_{GeH_4}B(T) + xP_{SiH_4}C(T) + (1-x)(1-\theta_{Si})P_{SiH_4}D(T)$$

(6.6)

where $A(T)$, $B(T)$, $C(T)$, and $D(T)$ (all in molecules/cm^2·s·Torr) are the rate constants for the four unimolecular reactions on the substrate, i.e. GeH_4 on Ge sites, GeH_4 on Si sites, SiH_4 on Ge sites, and SiH_4 on Si sites, respectively

$$\begin{aligned}
A(T) &= \frac{1}{(2\pi m_{GeH_4}kT)^{1/2}}\left(\frac{E_{GeH_4/Ge}}{kT}+1\right)\exp\left(-\frac{E_{GeH_4/Ge}}{kT}\right) \\
B(T) &= \frac{1}{(2\pi m_{GeH_4}kT)^{1/2}}\left(\frac{E_{GeH_4/Si}}{kT}+1\right)\exp\left(-\frac{E_{GeH_4/Si}}{kT}\right) \\
C(T) &= \frac{1}{(2\pi m_{SiH_4}kT)^{1/2}}\left(\frac{E_{SiH_4/Ge}}{kT}+1\right)\exp\left(-\frac{E_{SiH_4/Ge}}{kT}\right) \\
D(T) &= \frac{1}{(2\pi m_{SiH_4}kT)^{1/2}}\left(\frac{E_{SiH_4/Si}}{kT}+1\right)\exp\left(-\frac{E_{SiH_4/Si}}{kT}\right)
\end{aligned} \quad (6.7)$$

Eq. (6.6) suggests that the growth rate is a function of Ge content (x), GeH_4 partial pressure (P_{GeH4}), SiH_4 partial pressure (P_{SiH4}), and surface H coverage θ_{Si} at any given temperature. In several previous studies,[53,63,66,67] the relation between Ge content in the

film and GeH_4 and SiH_4 partial pressures is approximated by

$$x = m\frac{P_{GeH_4}}{P_{SiH_4} + P_{GeH_4}} \tag{6.8}$$

where m (dimensionless) is an experimentally determined factor. Hartmann *et al* summarized the m values from the literature:[63] 2.92–3.12 by Robbins *et al*,[53] 2.7 by Hartmann *et al*,[63] 3.06 by Racanelli *et al*,[66] and 2.7–3.1 by Suemitsu *et al*.[69] As discussed later in this paper, an analytical equation is derived in this model for the relation between x and P_{GeH4} or P_{SiH4}, which is more complicated than Eq. (6.8). By substituting that relation and Eq. (6.4) into Eq. (6.6), the growth rate can be calculated for the heterogeneous regime as a function of Ge content at any temperature. The values for $g(T)$ and $h(T)$ in Eq. (6.4) used to obtain a good fit in Figure 6.3 are listed in Table 6.3. No clear trend is observed for $g(T)$ and $h(T)$ values in Table 6.3. In all the calculations, the partial pressure of each precursor is obtained from the total deposition pressure and the ratio of flow rates (SiH_4, GeH_4, and H_2) under the ideal gas law.

Table 6.3 Fitting parameters used in Eq. (6.4) and thus Eq. (6.6) for Figure 6.3

Fitting parameters	*g(T)*	*h(T)* (1/sccm)
570°C	2.41	1.02
600°C	9.01	1.98
620°C	14.22	5.02
650°C	31.94	7.94
675°C	59.81	1.20

6.3.2 Growth Rate in Homogeneous Regime

In the homogeneous decomposition dominated regime, the growth rate decreases with Ge content due to complicated gas phase chemistry. With the difficulty in simulating gas phase chemistry in the homogeneous regime, we have applied one of the simplest mathematical relations to describe the growth behavior in the homogeneous regime

$$G = -s(T)x + b \tag{6.9}$$

where $s(T)$ (in nm/min) is assumed to be only temperature-dependent and b (in nm/min) is dependent on both temperature and SiH_4 partial pressure. Although Eq. (6.9) is purely empirical, it does allow extraction of the boundary conditions between the heterogeneous regime and homogeneous regime, as discussed later in this chapter.

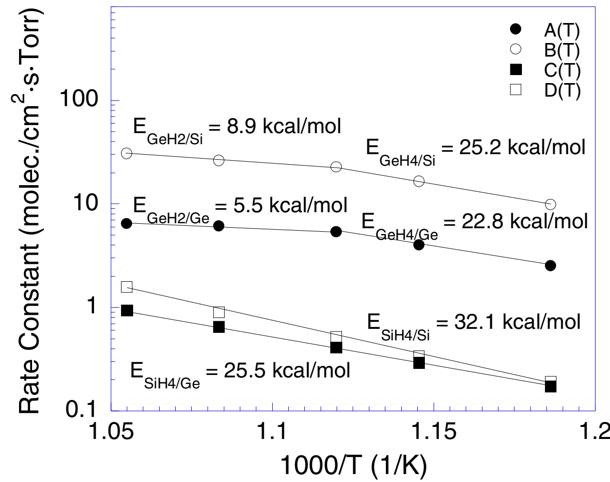


Figure 6.4 Arrhenius plot for rate constants used in Eq. (6.6). Activation energies for different heterogeneous unimolecular reactions on the surface sites are extracted. [78]

Figure 6.3 compares the model with experimental growth rate obtained by Jang *et al*[65] as a function of Ge content in the film at different deposition temperatures. The

model includes two parts, heterogeneous growth from Eq. (6.6) and homogeneous growth from Eq. (6.9). The Arrhenius plot for the rate constants *A(T)*, *B(T)*, *C(T)*, and *D(T)* used in this model for Eq. (6.6) is shown in Figure 6.4, from which the activation energies for GeH_4 and SiH_4 decomposition on H-free Ge and Si sites can be obtained according to Eq. (6.7). The activation energies for SiH_4 adsorption on H-free Ge and Si sites are $E_{SiH4/Ge}$ = 25.5 kcal/mol and $E_{SiH4/Si}$ = 32.1 kcal/mol, respectively. They do not change in the temperature range of 570–675°C, suggesting that there is only one precursor, i.e. SiH_4, present in the temperature and pressure ranges involved. The activation energy for SiH_4 adsorption on H-free Si sites, 32.1 kcal/mol, agrees well with a previously reported value of 30 kcal/mol.[81] However, the activation energies extracted from *A(T)* and *B(T)* decrease with increasing temperature, as shown in Figure 6.4. This suggests that there is more than one Ge-containing species in the temperature range involved, i.e., GeH_4 undergoes homogeneous decomposition into GeH_2. The kinks in Figure 6.4 for *A(T)* and *B(T)* likely indicate the temperature at which this homogenous decomposition takes place, 620°C. Therefore, the activation energies extracted from the Arrhenius plot at high temperatures correspond to GeH_2 adsorption on H-free Ge and Si sites, as listed in Table 6.4. The activation energy for GeH_2 adsorption on H-free Ge sites, 5.5 kcal/mol, agrees well with previously reported values of 8.7 kcal/mol by Garone *et al*,[56] 6.9 kcal/mol by Hartmann *et al*,[92] 4.8 kcal/mol by Green *et al*.[93] The activation energy for GeH_4 adsorption on H-free Ge sites, 22.8 kcal/mol, agrees well with a previously reported value of 21 kcal/mol by Cao *et al*.[94]

Figure 6.5 shows a comparison between the experimental data by Jang *et al*[65]

and this model for growth rate at 620°C as a function of Ge content at different SiH_4 flow rates. The model again includes two parts: heterogeneous growth from Eq. (6.6) and homogeneous growth from Eq. (6.9). The values for $g(P_{SiH4})$ and $h(P_{SiH4})$ in Eq. (6.4) for a good fit in Figure 6.5 are listed in Table 6.5. Again, no clear trend is observed for $g(P_{SiH4})$ and $h(P_{SiH4})$ values in Table 6.5. An excellent agreement is achieved between our model and experimental data in both Figures 6.3 and 6.5.

Table 6.4 Activation energy for GeH_4 and GeH_2 adsorption

$E_{GeH4/Ge}$	$E_{GeH4/Si}$	$E_{GeH2/Ge}$	$E_{GeH2/Si}$
22.8 kcal/mol	25.2 kcal/mol	5.5 kcal/mol	8.9 kcal/mol

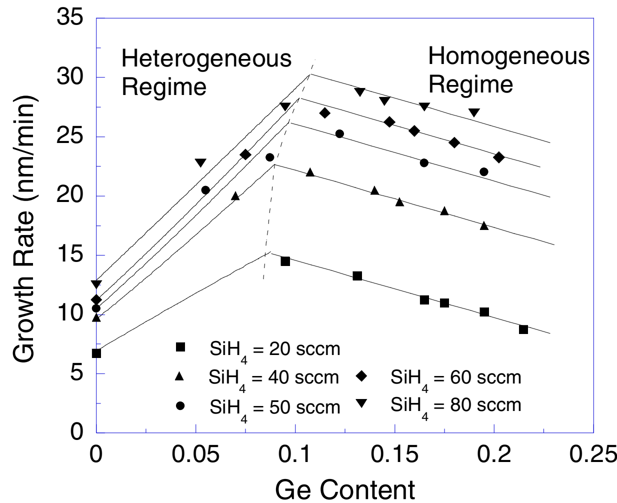


Figure 6.5 Growth rate as a function of Ge content at different SiH_4 flow rate. Deposition temperature is 620°C. Solid lines are model predictions and experimental data from Ref. 65. The dash line is the boundary between homogeneous and heterogeneous regimes. [78]

Table 6.5 Fitting parameters used in Eq. (6.4) and thus Eq. (6.6) for Figure 6.5

SiH_4 flow rate (sccm)	$G(P_{SiH4})$	$h(P_{SiH4})$ (1/sccm)
20	3.01	1.10
40	1.21	0.21
50	1.67	0.58
60	1.58	0.69
80	1.46	0.78

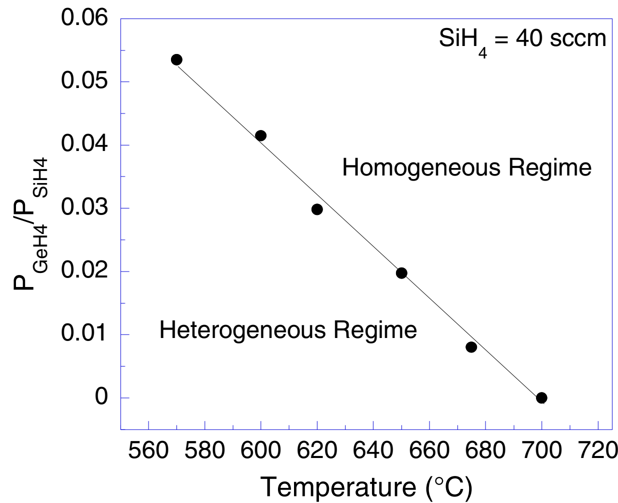


Figure 6.6 Boundary between heterogeneous and homogeneous regimes as experimentally defined in Figure 6.3 by P_{GeH4}/P_{SiH4} ratio and temperature. [78]

6.3.3 Conditions for Homogeneous Decomposition

The growth rate maxima as experimentally defined in Figures 6.3 and 6.5 are the boundary between the heterogeneous regime and homogeneous regime. If the P_{GeH4}/P_{SiH4} ratio at these maxima is plotted as a function of deposition temperature, a linear relation is obtained, as shown in Figure 6.6. The growth is dominated by homogeneous decomposition of GeH_4 if the deposition conditions (P_{GeH4}/P_{SiH4} ratio and temperature) are above this line and it is dominated by heterogeneous decomposition of GeH_4 if the deposition conditions are below this line. This line also suggests that it takes

lower GeH_4 partial pressures at higher temperatures or lower temperatures at higher GeH_4 pressures for homogeneous decomposition to occur.

Figure 6.7 shows the P_{GeH4}/P_{SiH4} ratio at growth rate maxima in Figure 6.5 as a function of SiH_4 flow rate, which gives the boundary between heterogeneous and homogeneous regimes. As SiH_4 flow rate increases from 20 sccm to 80 sccm, the boundary line is almost constant, suggesting that GeH_4 homogeneous decomposition at 620°C is more or less independent of SiH_4 flow rate.

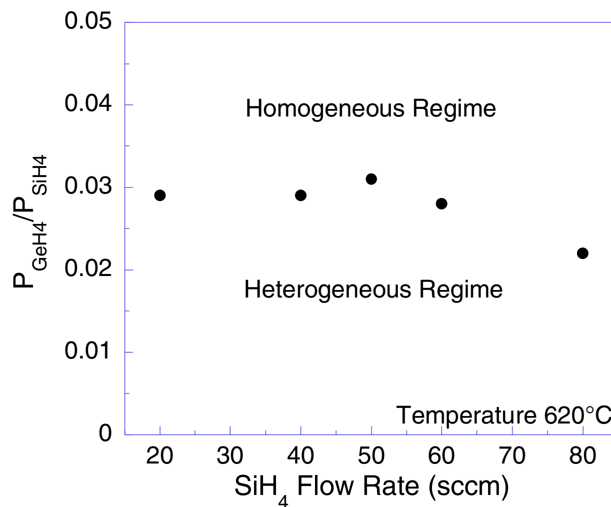


Figure 6.7 Boundary between heterogeneous and homogeneous regimes as experimentally defined in Figure 6.5 by P_{GeH4}/P_{SiH4} ratio and SiH_4 flow rate.[78]

6.4 Germanium Content

Jang *et al*[65] also reported on Ge content as a function of deposition conditions. They first examined the Ge content as a function of deposition temperature and the GeH_4/SiH_4 flow ratio. The experiment was carried out by changing the GeH_4/SiH_4 flow ratio from 1.25% to 5.75% at constant SiH_4 flow rate of 40 sccm and H_2 low rate of 80 sccm as the carrier gas. The resultant deposition pressure ranged from 15 mTorr to 17

mTorr. The deposition temperature was varied from 570°C to 700°C. They observed that the Ge content decreases with increasing temperature. They also examined Ge content as a function of SiH_4 flow rate. The experiments were carried out by changing the SiH_4 flow rate from 20 sccm to 80 sccm (GeH_4/SiH_4 ratio from 1.25% to 5.75%) at a constant deposition temperature of 620°C without H_2 as the carrier gas. The resultant pressure ranged from 3 mTorr to 11 mTorr. The Ge content decreased as the SiH_4 flow rate increased.

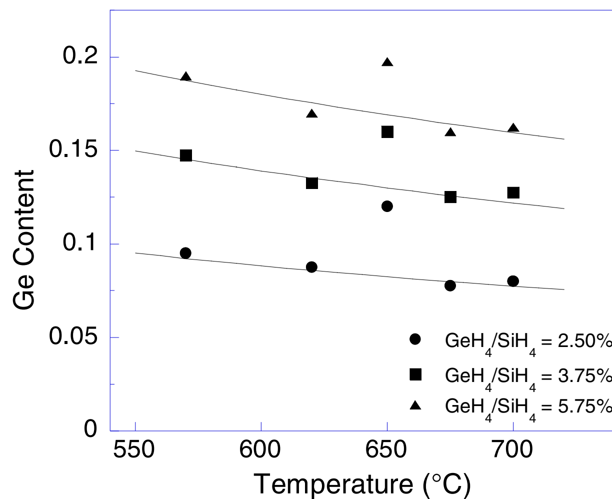


Figure 6.8 Ge content as a function of temperature at different GeH_4/SiH_4 ratio. SiH_4 flow rate is 40 sccm. Solid lines are model predictions and experimental data from Ref. 65. [78]

Several previous studies[53,63,66,67] have approximated the relation between Ge content in the film and GeH_4 and SiH_4 partial pressures using Eq. (6.8), where a fitting parameter m is needed to account for the discrepancy between the equation and the experimental data. From the concept of competitive adsorption, the Ge content in the film is equal to the ratio of the Ge flux J_{Ge} to the total flux J_{total}, which is given by

$$x = \frac{J_{Ge}}{J_{total}} = \frac{J_{Ge}}{J_{Ge} + J_{Si}} \tag{6.10}$$

By substituting the equations in Table 6.2 into Eq. (6.10) and rearranging, the Ge content x is given by

$$x = -\frac{b}{2a} + \frac{\sqrt{b^2 - 4ac}}{2a} \tag{6.11}$$

Where

$$\begin{aligned}
a &= \frac{P_{GeH4}}{P_{SiH4}} A(T) + C(T) - (1-\theta_{Si}) \frac{P_{GeH4}}{P_{SiH4}} B(T) - (1-\theta_{Si}) D(T) \\
b &= 2(1-\theta_{Si}) \frac{P_{GeH4}}{P_{SiH4}} B(T) + (1-\theta_{Si}) D(T) - \frac{P_{GeH4}}{P_{SiH4}} A(T) \\
c &= -(1-\theta_{Si}) \frac{P_{GeH4}}{P_{SiH4}} B(T)
\end{aligned} \tag{6.12}$$

a, b, and c are all in molecules/cm^2·s·Torr. $A(T)$, $B(T)$, $C(T)$, and $D(T)$ are rate constants as given in Eq. (6.7) and their values in Figure 6.4. Eq. (6.11) gives the Ge content for the heterogeneous regime. When the growth is dominated by homogeneous decomposition of GeH_4, the Ge content can not be deduced analytically. For simplicity, Eq. (6.11), which describes the Ge content in the heterogeneous regime, is extended to describe the Ge content in the homogeneous regime.

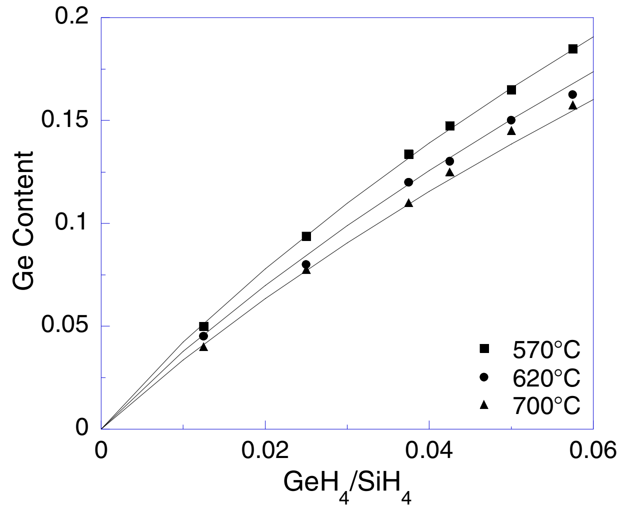


Figure 6.9 Ge content as a function of GeH_4/SiH_4 ratio at different temperatures. SiH_4 flow rate is 40 sccm. Solid lines are model predictions and experimental data from Ref. 65. The m values extracted from Eq. (6.8) are 3.38 at 570°C, 3.12 at 620°C and 2.91 at 700°C for comparison. [78]

Figures 6.8 shows a comparison of Eq. (6.11) with experimental data by Jang *et al*[65] for Ge content as a function of deposition temperature at different GeH_4/SiH_4 ratios. Figure 6.9 shows a comparison of Eq. (6.11) with experimental data[65] for Ge content as a function of GeH_4/SiH_4 ratio at different deposition temperatures. In both cases, excellent agreements are achieved. Intuitively, SiH_4 decomposition on H-free Ge and Si sites requires larger activation energies than GeH_4. Therefore, when the temperature increases, the Si flux J_{Si} increases faster than the Ge flux J_{Ge}, and the Ge content decreases. In the homogeneous regime, the good agreement between Eq. (6.11) and experimental data[65] could be attributed to the effect of GeH_4 homogeneous decomposition on SiH_4 gas phase chemistry. Figure 6.10 shows the Ge content at 620°C as a function of SiH_4 flow rate at different GeH_4/SiH_4 ratios. Excellent agreement is again obtained between experimental data[65] and this model.

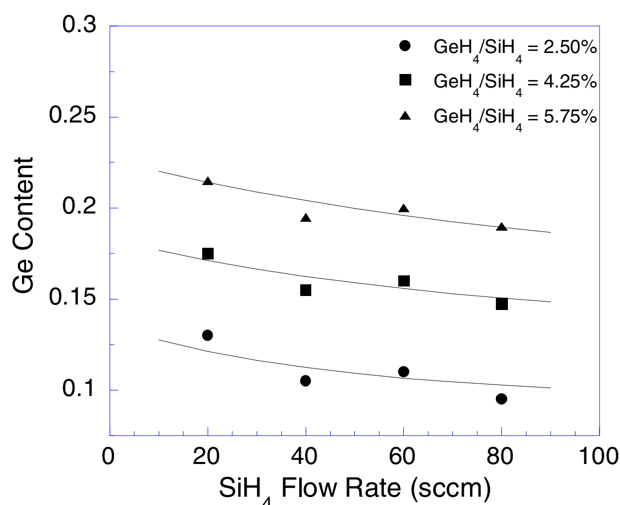


Figure 6.10 Ge content as a function of SiH_4 flow rate at different GeH_4/SiH_4 ratios. Deposition temperature is 620°C. Solid lines are model predictions and experimental data from Ref. 65. [78]

Finally, this model is applicable for a wide range of deposition conditions, including deposition pressure/temperature and precursor/carrier gas flow rates. The model will become more complicated when SiH_4 begins to homogeneously decompose, which requires higher deposition temperatures.

6.5 Summary

A quantitative kinetic model is proposed for $Si_{1-x}Ge_x$ growth from SiH_4 and GeH_4 by CVD. The growth of $Si_{1-x}Ge_x$ is divided into two regimes: a heterogeneous decomposition dominated regime and a homogeneous decomposition dominated regime. When deposition temperature and/or GeH_4/SiH_4 ratios are low, the growth is dominated by heterogeneous decomposition and the growth rate increases with increasing Ge content. When deposition temperature and/or GeH_4/SiH_4 ratios are high, the growth is dominated by homogeneous decomposition of GeH_4 and the growth rate decreases with

Ge content. Based on the collision theory of heterogeneous unimolecular reactions, statistical physics, and the concept of competitive adsorption, analytical equations are derived to describe growth rate and film composition in heterogeneous regimes. Homogeneous decomposition of GeH_4 into GeH_2 complicates the gas phase chemistry for both GeH_4 and SiH_4, causing the growth rate to decrease with increasing Ge content. An empirical linear relation is employed to describe the deposition kinetics in the homogeneous regime. The temperature and GeH_4/SiH_4 ratio conditions for homogeneous decomposition of GeH_4 are established from experimental data. Analytical equations show that Ge content in the film is a complicated function of deposition conditions. The model agrees well with the experimental data for $Si_{1-x}Ge_x$ growth from GeH_4 and SiH_4 by CVD.

CHAPTER 7

CONCLUSIONS AND FUTURE SCOPES

7.1 Conclusions

In this dissertation, monolayer Se passivation is employ to remove dangling bonds on the Si (100) surface. HfO_2 by different growth methods on Se-passivated n-type Si (100) is studied for suppression of interfacial layer formation at high-*k*/Si interface. Ti is deposited on n-type Se-passivated Si (100) to reach a low metal/Si contact resistance. A kinetic model is proposed for $Si_{1-x}Ge_x$ growth from SiH_4 and GeH_4 by CVD.

For HfO_2 on Se-passivated n-type Si (100), three growth methods were used, including reactive sputtering, O_3 oxidation and dry oxidation. C-V and I-V characterization for HfO_2 by reactive sputtering and O_3 oxidation show no improvement by Se passivation. Possible reason could be due to the damage of the Se passivation layer by plasma during reactive sputtering, and the diffusion of O atoms into the Si substrate enhanced by O_3. With HfO_2 formed by dry oxidation, Se-passivated samples always show smaller *EOT* than the control samples up to 600°C, which demonstrates the effect of interfacial layer formation suppression by Se passivation. Especially, the Se-passivated sample oxidized at 300°C shows much improved properties. The smallest *EOT* ~31 Å with a small leakage current (orders of magnitude lower than the control

samples) indicates the improvement of the high-*k*/Si interface quality. By assuming the surface contamination of ~15 Å, the interfacial layer of Se-passivated samples only contributes 6 Å to the *EOT* while the interfacial layer of control samples contributes about 40 Å to the *EOT*. In addition, the flat-band voltage -0.2 V of Se-passivated sample is close to theoretical value -0.14 V.

The effect of Schottky barrier lowering on contact resistance reduction between Ti and n-type Si (100) substrates by Se passivation is studied with four-point probe and C-TLM measurements. Three different doping concentration n-type Si (100) substrates are used: low doping level with 10^{15} cm^{-3}, moderate doping level with 10^{17} cm^{-3}, and high doping level with 10^{19} cm^{-3}. For both low and moderate doping substrate, the sheet resistance show no obvious improvement due to the overshadow effect of the high substrate series resistances. Sheet resistance of the Ti-Si contacts on Se-passivated 10^{19} cm^{-3} doped substrates shows a ~30% reduction as compared to the control samples. Accordingly, the extracted contact resistance decreases by about one order of magnitude for samples with different Ti thicknesses and different annealing temperatures. A 125%–2900% reduction in contact resistivity is achieved by Se passivation on highly-doped SOI substrates with 500-Å un-doped Si buffer layer. When the buffer layer thickness is reduced to 50 and 10 Å, the contact resistivities of the passivated and control samples reveal little difference. This is because of the surface adsorption, which can dominate the contact resistance when the buffer layer thickness is low. So an ultrahigh vacuum in situ process is needed to avoid the surface adsorption.

A quantitative kinetic model is proposed for $Si_{1-x}Ge_x$ growth from SiH_4 and

GeH_4 by CVD. It takes into account both homogeneous and heterogeneous reactions, which involve SiH_4, GeH_4, and the homogeneous decomposition product of GeH_4, GeH_2, and three types of surface sites, H-free Si sites, H-terminated Si sites, and H-free Ge sites. The growth of $Si_{1-x}Ge_x$ is divided into two regimes: a heterogeneous decomposition dominated regime and a homogeneous decomposition dominated regime. At low temperatures and/or low GeH_4/SiH_4 ratios, the growth is dominated by heterogeneous decomposition and the growth rate increases with increasing Ge content. At high temperatures and/or high GeH_4/SiH_4 ratios, the growth is dominated by homogeneous decomposition of GeH_4 and the growth rate decreases with Ge content. For the heterogeneous regime, analytical equations are derived to describe growth rate and film composition as a function of deposition conditions, including deposition temperature, GeH_4 flow rate, and SiH_4 flow rate. These equations are based on the collision theory of heterogeneous unimolecular reactions, statistical physics, and the concept of competitive adsorption. Homogeneous decomposition of GeH_4 into GeH_2 complicates the gas phase chemistry for both GeH_4 and SiH_4, causing the growth rate to decrease with increasing Ge content. An empirical linear relation is employed to describe the deposition kinetics in the homogeneous regime. The temperature and GeH_4/SiH_4 ratio conditions for homogeneous decomposition of GeH_4 are established from experimental data. Analytical equations show that Ge content in the film is a complicated function of deposition conditions. The model agrees well with the experimental data for $Si_{1-x}Ge_x$ growth from GeH_4 and SiH_4 by CVD.

This work gives promising potential solutions to several issues which seriously

hinder the development of the CMOS IC performance to even higher speed and greater functionality.

7.2 Future Scopes

7.2.1 HfO_2 on Se-passivated Si (100)

The request from ITRS 2005 on *EOT* for future high-*k* material is below 10 Å for high-performance logic. However, contamination layer on Si surface can easily contribute ~15 Å to the total *EOT*, so an in-situ ultrahigh-vacuum HfO_2 deposition after Se passivation is expected to avoid the contamination adsorption. In addition, since the oxygen atom is very reactive, at higher temperature process, it can still pass through the Se passivation layer and react with Si to form the interfacial layer. So combining with the Se passivation technique, a non-oxide dielectric material may be the candidate to replace SiO_2 as future gate dielectric material.

7.2.2 Low resistance Ti/n-Si (100) by Se passivation

An in-situ ultrahigh-vacuum Ti deposition after Se passivation is desired to avoid the Si surface contamination. This is to lower the contact resistivity to ~10^{-8} $\Omega\cdot cm^2$ to meet the future requirement on contact resistance in source/drain engineering. Also, metals with large work functions like Ni (5.2 eV) and Pt (5.7eV) can be deposited on Se-passivated p-type Si (100) to reach low contact resistance between metal and p-type Si (100).

7.2.3 Kinetic model for $Si_{1-x}Ge_x$ alloy growth from SiH_4 and GeH_4 by CVD

This model mainly focuses on SiH_4 and GeH_4 as the precursors. Since SiH_2Cl_2 is also used as precursor for Si source, this model can be used to explain the $Si_{1-x}Ge_x$

growth from SiH_2Cl_2 and GeH_4 even though it shows different growth behavior[54,56,58,64] from SiH_4 and GeH_4. This model can also be extended to explain the doping behavior in $Si_{1-x}Ge_x$ growth.[95]

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