A CMOS ULTRA-WIDEBAND DIFFERENTIAL LOW NOISE AMPLIFIER

by

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ABSTRACT

A CMOS ULTRA-WIDEBAND DIFFERENTIAL LOW NOISE AMPLIFIER

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In this thesis, a CMOS Ultra-wideband (UWB) Low noise Amplifier (LNA) was designed and simulated. In the design, specific architecture decisions were made in consideration of ultimately including this LNA in a system-on-chip implementation of an Ultra-wideband communication system. The basic architecture of the LNA designed herein exhibits a differential amplifier core with active input and output impedance matching, minimizing the number of expensive space consuming passive inductors necessary for passive impedance matching networks. The LNA maintains a gain of 16.4*dB* with a ±0.25*dB* ripple over the band of 3.1-6.2GHz. Despite the use of an active input matching stage, the LNA achieved a noise figure ranging from 3.6-3.9*dB* over the band of operation. The input active matching stage (common-gate) maintained a less than -10*dB* reflection coefficient, matching successfully with 50Ω over the band of 3-12GHz. The output active matching stage (source-follower) maintained a less than -

10*dB* reflection coefficient, also matching successfully with 50Ω, but maintaining the acceptable reflection coefficient over the band of 3-17GHz.

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CHAPTER 1

INTRODUCTION

One of the latest buzz words in research and technology today is “Ultra-wideband” or UWB for short. It has become a buzz word for a plethora of reasons. But putting these reasons aside, it is safe to say that numerous universities and companies alike have been rushing to develop novel architectures that expand the capabilities of UWB while developing cost effective systems that take advantage of the unique features of UWB. However, given the climate of the semiconductor industry today, it is blatantly obvious that the silicon IC market shows partiality toward the CMOS (Complimentary Metal Oxide Semiconductor) fabrication process. Consequently, in order to establish cost effective, high data rate, low power wireless UWB solutions in the commercial market today, these systems need to be implemented entirely in CMOS. Other silicon technologies, such as SiGe (Silicon-Germanium) or BiCMOS, require specialized fabrication plants and are typically fabricated on smaller wafers, driving costs higher and production volumes lower even during full-scale production. In addition, since CMOS is by far the most attractive digital technology, implementing the necessary UWB analog system functions with CMOS allows for a system-on-chip (SOC) design, which can significantly drive overall system cost down by reducing manufacturing complexity.

Most of the concern that surrounds the implementation of high-speed, UWB wireless technologies in a standard CMOS process is the analog front-end. The analog

front-end in UWB wireless systems is one of the most crucial stages in determining overall system performance (in terms of Signal-to-Noise Ratio (S/N)). Because of this, combined with the desire to use a CMOS process, considerable research has been done attempting to develop CMOS Low Noise Amplifiers (LNA) with exceptional performance characteristics suitable for the analog front-end of a UWB wireless system. However, to the author's knowledge, none of the CMOS ultra-wideband LNAs already developed utilize a differential architecture. Differential architectures reject large amounts of common-mode noise which would be inevitably present in a mixed-signal environment (such as in a SOC) thereby increasing the robustness of the analog circuitry and enhancing the ability of the LNA to survive in a mixed-signal environment. However, one of the drawbacks associated with differential circuits is the fact that the circuit implementation essentially doubles the usage of very costly chip die area. Therefore, given the necessity of the differential architecture for the survival of the LNA in a SOC implementation, significant design measures must be taken elsewhere to curtail the increase in size associated with differential circuits compared to their single-ended counterparts.

Many of the UWB CMOS LNAs developed, use passive impedance matching networks [1, 2, 3, 4]. The number of inductors used in these passive input impedance networks spans from two to five and only the highest order network effectively matching across the entire ultra-wideband (3.1-10.6 GHz). The only inductance available to the circuit designer in the CMOS process in order to realize the passive matching networks must come from spiral planar inductors. However, in a typical LNA

spiral inductors consume a very large fraction of the circuit area thus significantly increasing the die size of the chip. From the chip photo of the LNA designed in [1], it can be observed that even the smallest spiral inductor consumes more die area than all of the active components combined. In the TSMC 0.18μm process, it is very typical for an inductor to have a footprint area much larger than 200x200μm^2. Therefore, since in [1] five inductors are used in the wideband passive matching network, this LNA becomes very expensive to manufacture. This is because chip cost for companies rises exponentially with increasing die size [6].

Since differential amplifiers have a "doubling" size problem, implementing differential amplifiers with passive impedance matching networks becomes very expensive and impractical because of the excessive real-estate consumed. In order to reduce the overall differential LNA size, this thesis proposes realizing ultra-wideband matching networks using active devices as apposed to high order passive networks. Active matching networks have the capability of working over an ultra wide-bandwidth with only the use of one spiral loading inductor. The main problem associated with active devices, however, is that they contribute a considerable amount of noise to the system - an effect undesired for low noise amplifiers. However, as shown in this thesis, active matching networks can be utilized while still providing adequate noise performance of the LNA. There has been at least one attempt at active input matching [5], but the LNA therein does not employ a differential architecture, thus making it susceptible and possibly inoperable in the midst of mixed-signal environment.

This thesis is organized as follows. Chapter 1 provides motivation for the work that was performed, specifically, reasons for choosing CMOS technology, a differential architecture, and active impedance matching networks. In Chapter 2, some basic background material is presented to form a foundation from which to discuss the design of the CMOS UWB differential LNA. The background material consists of a basic UWB communication system overview and some microwave engineering concepts which will be used in the design and analysis of the LNA. It also gives an introduction to significant sources of noise and noise modeling of a MOSFET transistor. The purpose of Chapter 3 is to provide a broad overview of low noise amplifiers and some of the different architectures available. Also, in Chapter 3, a lower bound for noise figure for two of the architectures discussed. Chapter 4 presents the proposed UWB LNA, and the design philosophy behind each stage. Also, in Chapter 4, a detailed circuit analysis of the different stages in the proposed LNA is shown and insights into functionality are drawn from the analysis. Chapter 4 also presents the simulation of the LNA and discusses important issues about the results. At the end of Chapter 4, comparisons are made with some of the most recent published UWB LNAs. The thesis concludes in Chapter 5, followed by a tabularized listing of the component values used in the LNA design in Appendix A.

CHAPTER 2

BACKGROUND

This chapter will present an overview of basic UWB technology as well as two of the most common UWB receiver architectures. In addition, this chapter will also provide an overview of some basic microwave engineering theory pertinent to UWB LNA design. Sources of the most pertinent noise sources found in a CMOS LNA are discussed as well.

2.1 Overview of Ultra-Wideband Systems

2.1.1 Very Brief History of UWB

Ultra-wideband communications and radar systems have been in existence for some time now, although they have not always been referred to as "Ultra-wideband". In fact, the first patent was awarded in 1973 for an UWB communication system, but different nomenclature was used. Through the 1980's, UWB technology was commonly referred to as carrier-free, base-band, or impulse communication. It wasn't until 1989 that the term "Ultra-wideband" was coined by the United States Department of Defense. The Department of Defense had been using the technology since the early 1960's, but much of the technological advances prior to 1994 were classified. However, since the commercial market can benefit dramatically from UWB capable systems, the Federal Communications Commission has passed legislation allowing the use of Ultra-wideband systems.

2.1.2 Definitions and Regulations

In the spring of 2002, the Federal Communications Commission (FCC) established an unlicensed communication band (3.1-10.6 GHz) and restricted transmitted power levels within that band to be below the noise floor, specifically below -41.3dBm/MHz, thereby allowing for the possibility of commercial Ultra-Wideband (UWB) systems. The low output power restriction on UWB systems ensures friendly coexistence with already available wireless systems, i.e. tolerable mutual interference. Figure 2.1 graphically depicts the spectral mask transmission limits established by the FCC for the ultra-wideband communication channel. EIRP stands for Equivalent Isotropically Radiated Power. The outdoor transmission limit is lower from 1.61 – 3.1 GHz than the indoor limit because of existing vehicular RADAR systems that currently occupy that bandwidth. Thus, to avoid interference with these systems, the FCC placed a greater restriction on transmitted power in that spectral region.

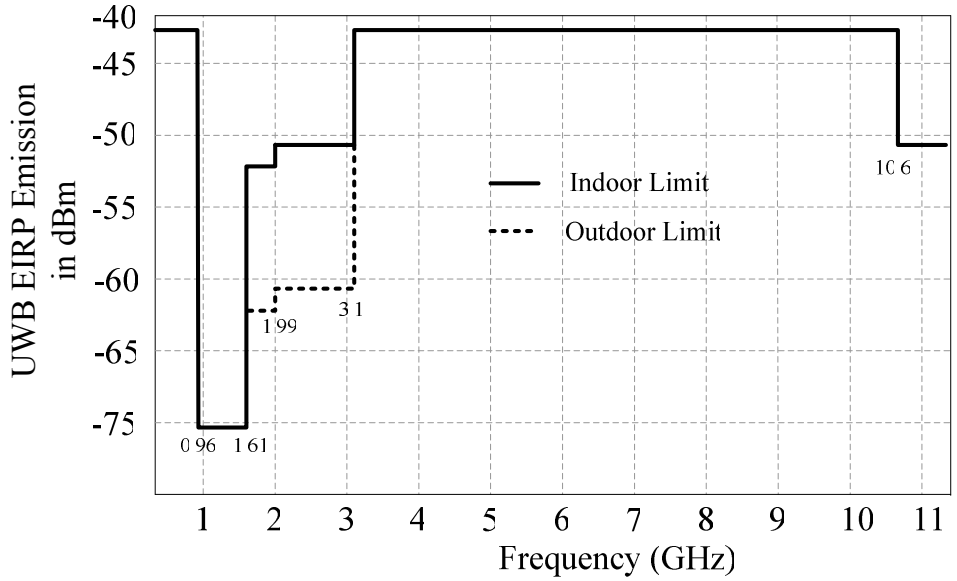

Figure 2.1 Spectral Mask specified by the FCC.

The FCC defined an UWB signal to have a spectral occupancy over 500MHz or a fractional bandwidth of more than 20%. Fractional bandwidth, as defined by the FCC, is given by,

$$F_{bw} = \frac{Bandwidth(BW)}{CenterFrequency} = \frac{f_U - f_L}{(f_U + f_L)/2}; \quad (2.1)$$

where, f_U and f_L are the upper and lower -10dB emission points, respectively. The FCC specifies that a system with center frequency in excess of 2.5GHz must have a bandwidth of at least 500MHz, but a system whose center frequency is less than 2.5GHz, must operate with a F_{bw} of at least 20% in order to be characterized as an UWB system.

2.1.3 Attractive features and applications of UWB

To have more bandwidth available for use in a system is a good thing. Therefore, to have an ultra amount of bandwidth available should be an ultra-good thing. One of the main attractive features that UWB offers is high data rates combined with low power consumption realizable because of the large amount of bandwidth available. The viability of UWB systems exhibiting these qualities is easily illustrated with Shannon's Information Capacity theorem. The theorem states that the maximum theoretical channel capacity (C in bits per second) is a function of channel bandwidth (B), signal power (S), and noise power (N), specifically,

$$C = B \cdot \log_2\left(1 + \frac{S}{N}\right). \quad (2.2)$$

In a narrowband system, the bandwidth of the channel is restricted, leaving transmitted signal power (S) the controlling factor in channel capacity (data rate). In

contrast, UWB systems exhibit very large channel bandwidths, drastically reducing the need to transmit large amounts of power at a certain frequency to establish adequate data rates. While adhering to the FCC regulations, UWB data rates can reach speeds much greater than 110 MB/s over 10 – 15 meters [8].

With the combination of low power and high data rates, there are almost a countless number of wireless applications that can benefit from UWB technology. To name a few, UWB stands to offer renovating and expanding capabilities in areas including wireless personal area networks (WPAN), sensor networks, RADAR systems, imaging, and RFID tags. Also, there are numerous biomedical applications the have been conceived specifically to take advantage of UWB. For example, because of the low power consumption capabilities and the plethora of available bandwidth, UWB technology can possibly allow for wireless real time physiological signal monitoring of the human body [9].

2.1.4 Recent standardization activity for UWB Systems

Important standardized systems that share the UWB spectrum include the global positioning system, IEEE 802.11 systems, and any other wireless system that operate in the 5.8GHz ISM (Industrial, Scientific, and Medical) band. In order to ensure seamless integration with existing wireless communication systems and to provide the highest level of quality to the end user, the IEEE is aiming to develop several standards that exploit the ultra-wideband spectrum allocated by the FCC.

Most of the recent activity for standardization of UWB systems by the IEEE has occurred in the standard for wireless personal area networks (WPAN – 802.15) task

groups. Within the 802.15 standards family, the task group 802.15.3a was formed to consider an alternative high data rate physical layer (PHY) to be implemented with UWB technology. To date the task group has remained in controversial deadlock, not able to select between two competing proposals. If included, UWB will not only augment the existing standard WPAN options, but also offer better performance and capability to systems currently utilizing the Bluetooth protocol (802.15.1).

Exploiting a different set of system wide advantages that UWB offers, the IEEE 802.15.4 standard was also re-opened to consider a specific type of UWB communication, namely, impulse-type UWB (IR-UWB). This standard will incorporate IR-UWB to enhance the low data rate, very low power, and low complexity systems it allows. Such systems include wireless sensor networks. In fact, the Zigbee Alliance (http://www.zigbee.org) is committed adhering to the IEEE 802.15.4a standard, and therefore will soon adopt a UWB technology as the standard completes. Zigbee is typically seen as the leader in wireless communications for sensor networks.

2.1.5 Two Common System Architectures

There are basically two different system level communication strategies employed to efficiently utilize the entire UWB spectrum, namely, Impulse-type UWB (IR-UWB) and carrier-based orthogonal frequency division multiplexing (OFDM). Comparisons of advantages/disadvantages between these different system architectures have received a considerable amount of attention lately. As previously mentioned, proponents of both sides have been locked in battle for several years over which architecture should be included in the IEEE 802.15.3a standard. The Multi-band

OFDM Alliance (MBOA) supports a type of OFDM architecture referred to as MB-OFDM (http://www.multibandofdm.org). The UWB-Forum is proposing a form of IR-UWB called Direct-Sequence UWB (DS-UWB) (http://www.uwbforum.org). The IEEE 802.15.4a task group has already selected a form of IR-UWB to be included in the IEEE 802.15.4 standard. This was done mainly because of the localization capability and simplicity that IR-UWB systems have as an advantage over OFDM systems.

However, in either case, because these systems are ultra-wideband, stringent, hard-to-meet specifications are placed on the RF front-end. In the IR-UWB case, the LNA must operate adequately over the entire intended spectral use (possibly 3.1-10.6GHz) of operation. For MB-OFDM, the LNA must either have a flat-gain response across the entire band of operation (potentially 3.1-10.6GHz), or exhibit tunability features to allow for frequency hopping among the different bands in the system.

2.1.5.1 IR-UWB

IR-UWB communicates using baseband pulses of very short duration (typically less than 2 nanoseconds) for signaling while using either pulse-position (PPM), pulse amplitude (PAM), or On-Off keying (OOK) as modulation schemes. The power spectral density of the fundamental pulse shape should comply with the spectral mask mandated by the FCC (as shown in Figure 2.1). However, using a spectrally conforming impulse shape does not necessarily ensure that the overall system transmitter will comply with the FCC's regulation. In [10], it is shown that in a TH-PPM (Time-Hopping, Pulse-Position Modulation) UWB system, spectral lines result in

mask violation or a reduction in transmitted power which in turn reduces the system performance.

Figure 2.2 depicts a typical coherent IR-UWB receiver. The analog correlator in conjunction with the template generator provides the functionality of an optimum matched filter. The matched filter is optimum in the sense that the signal-to-noise ratio is maximized at its output in the presence of additive noise. Typically with narrowband systems, the matched filtering process is performed in the digital domain but for UWB this approach is at best difficult and at worst impractical. An ADC designed to operate on a UWB signal at the Nyquist rate or above would need to consume impractically excessive amounts of power.

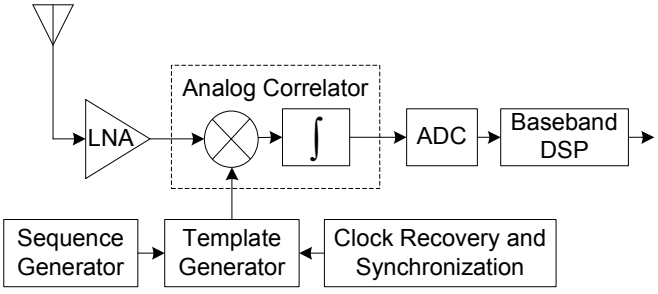

Figure 2.2 A coherent IR-UWB Receiver

As previously stated, an LNA included in an IR-UWB system must be designed to operate adequately over the entire desired spectrum of operation, if possible, 3.1-10.6GHz. Furthermore, the input and output matching networks in the LNA schematic must have low reflectivity across the entire spectrum as well. Typically, the reflectivity coefficients must be constrained below -10dB over the frequency range of operation.

2.1.5.2 MB-OFDM

OFDM techniques for wireless communication have recently been made popular by the almost ubiquitous WiFi (IEEE 802.11) products. Since a form of OFDM has become the latest architecture trend in WiFi products, in order to take advantage of the design experience and existing libraries, OFDM techniques have been proposed for realizing an UWB system.

The MB-OFDM systems can achieve Ultra-Wideband communication by essentially adding together multiple orthogonal bands of communication, i.e. frequency division multiplexing (see Figure 2.3). A given communication system was proposed to communicate on one of the major band groups, and the sub-bands (each 528 MHz wide to satisfy UWB definition requirement) form the communication channel. A time-interleaving method was proposed to specify which sub-band would be active for communication at any given moment. This time interleaving significantly cuts down on undesired multi-path effects.

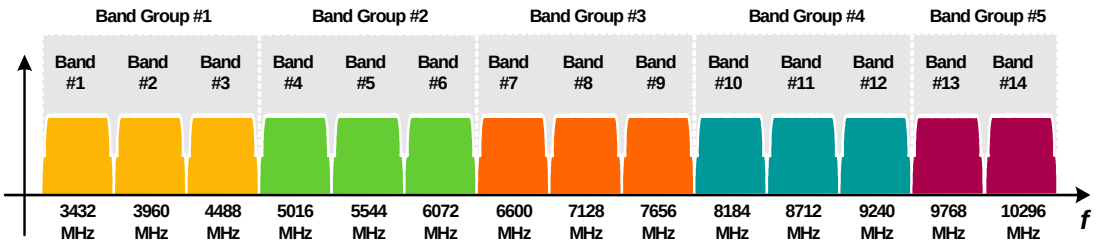

Figure 2.3 Frequency band plan of the MBOA proposal for the IEEE 802.15.3a PHY

The PHY (physical) layer of the proposed MB-OFDM is basically a descendant from 802.11a/g systems, but it has many more and larger frequency bands that it utilizes in order to transmit the data. In consequence, these systems have the potential of

achieving very high data rates. However, just like their ancestors, they are plagued by high power consumption and high circuit complexity. Even though a MB-OFDM UWB system is extremely superior to an 802.11a/g system, when compared to an IR-UWB system, it loses in power consumption and system complexity.

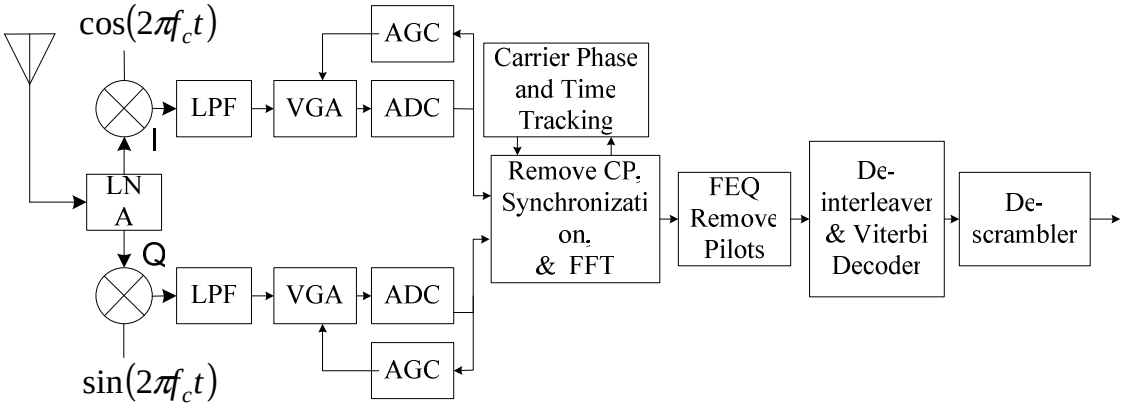

Figure 2.4 The MB-OFDM UWB receiver as proposed by the MBOA

Figure 2.4 shows the MB-OFDM UWB receiver architecture that is the most recent proposal for the IEEE 802.15.3a PHY layer by the Multiband Alliance (MBOA). As one can see from the MB-OFDM system block diagram, in comparison to a typical IR-UWB block diagram (Figure 2.2), the complexity is much greater for the MB-OFDM case. The MB-OFDM case is not a valid UWB system architecture for inclusion in the IEEE 802.15.4a standard precisely because of the complexity and power consumption of such systems as well as localization capabilities. However, when power and ranging ability is of no concern, the MB-OFDM UWB system provides a very good high data rate solution.

A MB-OFDM system also has the potential to use the entire frequency band from 3.1-10.6GHz for high speed communication; however, the LNAs used in the RF

front-end do not necessarily need to have a flat gain response over this entire spectrum. Since the system contains multiple channels with approximately 500MHz bandwidth, there are three possible LNA scenarios: 1) a different LNA could be used for each channel which satisfies the bandwidth and center frequency constraints; 2) an LNA with tunable capabilities that span the entire range of desired spectrum could be used; 3) or simply an LNA with a flat gain response across the entire UWB range of operation.

The LNA designed in this thesis satisfies the requirements to work in scenario three above for a system designed to operate from 3-6 GHz which also makes it eligible for inclusion in an IR-UWB system which works over the same frequency range. As for scenario two, there has been at least one successful attempt in designing a tunable LNA operating in the UWB frequency range in [11] which was designed fully in 0.18um CMOS technology. Scenario one can be dismissed as completely impractical.

2.1.6 UWB Initial Deployment

Even though the FCC allocated the entire spectrum from 3.1-10.6GHz, the two competing proposals for the PHY layer of IEEE 802.15.3a, DS-UWB and MB-OFDM, divide the spectrum up into two different bands (see Figure 2.3 and Figure 2.5). This is done for several reasons. First, since wireless communication products that use the U-NII band (Unlicensed National Information Infrastructure) are almost ubiquitous, the spectrum was divided mainly to avoid mutual interference with systems operating in this band. At first this may appear as sacrificing the characteristic of UWB systems, namely, the bandwidth. However, in the MB-OFDM proposal [22], they assert that the MB-OFDM systems are capable of communication with 480Mbps at less than 4*m* using

only the lower band (major band group #1 in Figure 2.3). In the DS-UWB proposal, they are much more aggressive and assert that 1320 Mbps can be achieved at less than 4*m* utilizing just the lower band. This class of data rate is unprecedented over the air, and the market would see numerous products which would initially benefit tremendously from UWB technology. Therefore, using only the lower band of the spectrum not only provides plenty of bandwidth for the development of novel systems, but it will also provide a quicker time-to-market of products because the lower frequency devices can be implemented in CMOS much easier than the upper band.

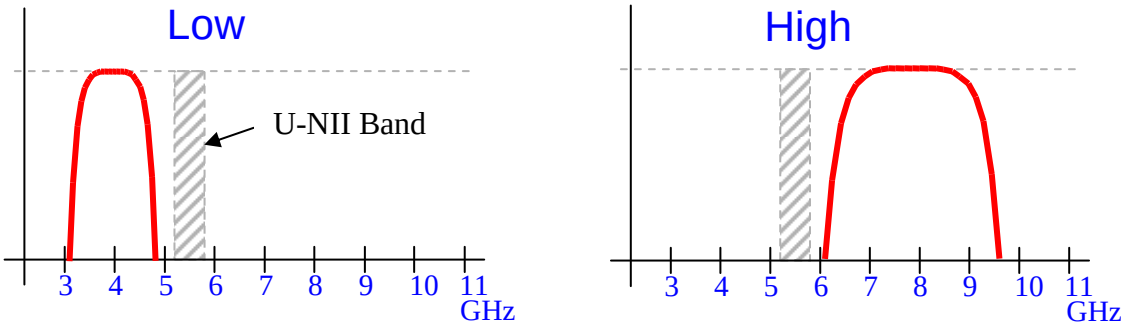

Figure 2.5 UWB divided spectrum operating bands

2.2 Background Theory

2.2.1 Two-Port S-parameters

Scattering Parameters (sometimes called S-parameters) have become the de facto standard in characterizing the performance of microwave systems and circuits. This occurred primarily because of the practical difficulty associated with measuring short circuit currents and open circuit voltages of a network at microwave frequencies [12]. At such high frequencies, it is much easier to simply measure the amplitude and direction of incident and reflective voltage waves. Just like impedance and admittance

matrices, the S-parameter matrix provides a complete description of a network at its input and output ports. While the impedance and admittance matrices relate all of the voltages and currents at and between every port within a given network, the S-parameter matrix relates the incident and reflective waves at and between every port within the network. Knowing the reflective and incident waves can fully characterize the system.

S-parameters relate incident and reflective waveform amplitude and phases between every port within a two-port network by,

$$\begin{bmatrix} V_1^- \\ V_2^- \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} V_1^+ \\ V_2^+ \end{bmatrix}. \tag{2.1}$$

In equation 2.1, V_i^- represents the voltage phasor of the waveform traveling away from port-*i* (reflected waveform), and V_i^+ represents the voltage phasor of the waveform traveling toward port-*i*. A phasor is a vector representation of a sinusoidal signal, $|V|\cos(wt+\theta)$, with vector polar notation of the form $|V|\angle\theta$. Figure 2.6 gives a graphical depiction of the traveling reflective and incident waveforms acting on a two-port network.

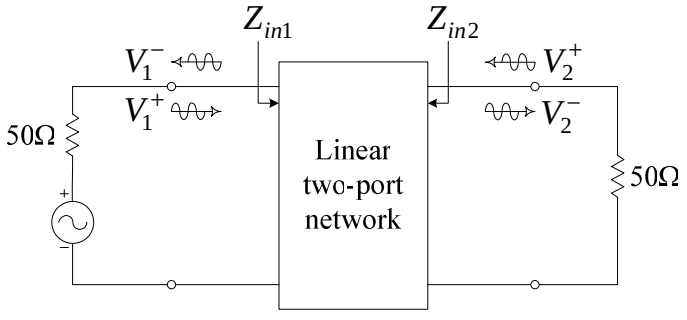

Figure 2.6 Reflective and incident waveform illustration on a two-port network

In Figure 2.6, a voltage source that has a characteristic impedance, $Z_0 = 50\Omega$, is applied to a linear two-port network which is driving a load with impedance of 50Ω. When the source and load impedances do not perfectly match Z_{in1} or Z_{in2}, respectively, a portion of the driving voltage waveform is reflected back from the mismatched impedance with or without a phase shift depending on the complex port impedance.

The individual S-parameters are given by,

$$S_{11} = \frac{V_1^-}{V_1^+} \text{ when } V_2^+ = 0 \tag{2.2}$$

$$S_{12} = \frac{V_1^-}{V_2^+} \text{ when } V_1^+ = 0 \tag{2.3}$$

$$S_{21} = \frac{V_2^-}{V_1^+} \text{ when } V_2^+ = 0 \tag{2.4}$$

$$S_{22} = \frac{V_2^-}{V_2^+} \text{ when } V_1^+ = 0 \tag{2.5}$$

In addition to the reflection caused by mismatched impedances, fractions of the waveform applied at port-2 can navigate through the network to leave port-1, thus contributing to V_1^-. Solving 2.1 for V_1^- illustrates this point and gives $V_1^- = S_{11}V_1^+ + S_{12}V_2^+$. S_{12} is commonly referred to as the "reverse isolation" factor because it represents the portion of the voltage waveform applied at port-2 that appears leaving port-1. S_{11} represents the portion of V_1^+ that appears at port-1 because of a

mismatched impedance reflection. For this reason, S_{11} is commonly referred to as the input reflection coefficient. Another common symbol used to represent the reflection coefficient is Γ. S_{22} is also commonly referred to as the reflection coefficient at port-2.

S_{21} represents the fraction of the waveform applied to the input port-1 that appears leaving port-2. This is essentially the definition of gain, and therefore S_{21} represents the gain of the two-port network.

2.2.2 Combined Differential-mode and Common-mode S-parameters

Because of various advantages that differential structures offer over their single-ended counterparts, they have become very widely used in microwave and radio frequency circuits. Therefore, S-parameter characterization has been extended to offer physically meaningful insights and analysis of differential circuits [13, 14].

Consider a four-port network representation of a differential amplifier. The network is fully characterized by the standard S-parameter matrix,

$$V^- = S_{std} V^+$$

$$= \begin{bmatrix} V_1^- \\ V_2^- \\ V_3^- \\ V_4^- \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{23} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{34} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{bmatrix} \begin{bmatrix} V_1^+ \\ V_2^+ \\ V_3^+ \\ V_4^+ \end{bmatrix}. \qquad (2.6)$$

In (2.6), the differential input is applied to both port-1 and port-2, and the differential output is taken from both port-3 and port-4. From the standard S-parameter matrix in (2.6), it is not possible to know anything other than the single ended parameters with in the differential circuit (e.g. single ended gain, single ended reverse isolation, etc.).

Therefore, there is a need to convert S_{std} in (2.6) into another matrix whose elements represent differential-mode and common-mode parameters. This has been done before and so the complete derivation will not be presented here; however, the transformation matrix will be presented (for a detailed derivation, see [13]).

The mixed mode S-parameter matrix is organized in a manner similar to the single-ended case where both mode information as well as port information is included. The mixed-mode S-parameter matrix is given by,

$$V_{mm}^{-} = S_{mm} V_{mm}^{+}$$

$$\Rightarrow \begin{bmatrix} V_{d1}^{-} \\ V_{d2}^{-} \\ \hline V_{c1}^{-} \\ V_{c2}^{-} \end{bmatrix} = \left[\begin{array}{cc|cc} S_{d1d1} & S_{d1d2} & S_{d1c1} & S_{d1c2} \\ S_{d2d1} & S_{d2d2} & S_{d2c1} & S_{d2c2} \\ \hline S_{c1d1} & S_{c1d2} & S_{c1c1} & S_{c1c2} \\ S_{c2d1} & S_{c2d2} & S_{c2c1} & S_{c2c2} \end{array}\right] \begin{bmatrix} V_{d1}^{+} \\ V_{d2}^{+} \\ \hline V_{c1}^{+} \\ V_{c2}^{+} \end{bmatrix}. \tag{2.11}$$

In (2.7), S_{didj} are the differential mode S-parameters and S_{cicj} are the common-mode S-parameters. S_{dicj} and S_{cidj} are the cross-mode S-parameters. After developing a similarity transformation matrix, *M*, and applying it to S_{std}, S_{mm} becomes,

$$S_{mm} = M S_{std} M^{-1}.$$

The similarity transformation matrix, *M*, was developed in [14] and is given as,

$$M = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & 0 & -1 & 0 \\ 0 & 1 & 0 & -1 \\ 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 \end{bmatrix}, \text{ and } M^{-1} \text{ is given as,}$$

$$M^{-1} = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 \\ -1 & 0 & 1 & 0 \\ 0 & -1 & 0 & 1 \end{bmatrix}.$$

Computing S_{mm} gives,

$$S_{mm} = \frac{1}{2} \begin{bmatrix} \begin{bmatrix} S_{11}-S_{13}-S_{31}+S_{33} & S_{12}-S_{14}-S_{32}+S_{34} \\ S_{21}-S_{23}-S_{41}+S_{43} & S_{22}-S_{24}-S_{42}+S_{44} \end{bmatrix} & \begin{bmatrix} S_{11}+S_{13}-S_{31}-S_{33} & S_{12}+S_{14}-S_{32}-S_{34} \\ S_{21}+S_{23}-S_{41}-S_{43} & S_{22}+S_{24}-S_{42}-S_{44} \end{bmatrix} \\ \begin{bmatrix} S_{11}-S_{13}+S_{31}-S_{33} & S_{12}-S_{14}+S_{32}-S_{34} \\ S_{21}-S_{23}+S_{41}-S_{43} & S_{22}-S_{24}+S_{42}-S_{44} \end{bmatrix} & \begin{bmatrix} S_{11}+S_{13}+S_{31}+S_{33} & S_{12}+S_{14}+S_{32}+S_{34} \\ S_{21}+S_{23}+S_{41}+S_{43} & S_{22}+S_{24}+S_{42}+S_{44} \end{bmatrix} \end{bmatrix} \quad (2.7)$$

Comparing (2.6) with (2.7), we can see that the differential mode gain is given by,

$$S_{d2d1} = \frac{1}{2}(S_{21} - S_{23} - S_{41} + S_{43}) \quad (2.8)$$

Equation (2.8) makes intuitive sense. Notice that the differential gain, S_{d2d1}, depends on the two single-ended gain parameters, S_{21} and S_{43}.

2.2.3 Impedance Matching

As described in section 2.2.1, when the impedance of the source does not match the impedance loading that source, part of the incident waveform will reflect back to the source due to the mismatch in impedances. The amount of the waveform reflected is given by S_{11} in the single-ended case or S_{d1d1} for the differential-mode case. Therefore, in order to reduce reflections, input and output matching networks must be added to the analog signal processing device. In addition to maximizing the power transferred (no waveform reflections) to the load, matching networks can also be used to minimize noise influence and/or to linearize the frequency response of a system.

For DC circuits, the maximum power theorem states that the maximum power available from the source will be transferred to the load provided the real internal source resistance is equal to the real impedance of the load. However, in the case of time-varying waveforms, the theorem states that maximum power transfer occurs when the complex internal impedance of the source equals the complex conjugate of the load impedance. Therefore, when the source is connected to the load, the internal impedance of the source connects in series with the load impedance and the inductive and capacitive reactance of the load and source compensate for each other and a real impedance results.

Since the imaginary part of complex impedance depends on frequency, complex impedance matching is very difficult to realize over a very large bandwidth. Circuits such as an LNA will load the source with a very complex impedance profile versus frequency, and thus a simple complex conjugate is hard to realize over all of the frequency. Wideband impedance matching can be realized with either high order passive networks or active devices. In this thesis, active devices were used to perform the wideband impedance matching.

2.2.4 Noise Sources

In electronics, noise is usually referred to as anything but the desire signal. There are numerous noise sources that contribute unwanted effects to the desired signal in electronics systems. Noise can be contributed to a signal from within the device itself or during transmission of the signal. Noise accumulated during transmission can usually be prevented or eliminated by various shielding, equalization or filtering

techniques. However, noise contributed by sources from within the device itself imposes a fundamental lower limit on the performance of the device. Therefore the noise sources considered in this section will exclude extraneous pickup of noise from external influences and only include the sources of noise internal to a device or a complete circuit. All of the noise source or noise phenomenon will not be considered here, but only noise source that will have a great impact on analog CMOS integrated circuits.

2.2.4.1 Shot Noise

Shot noise arises from direct-current (DC) flow and is present in diodes, MOS transistors, and bipolar transistors. The origin of shot noise results directly from the randomness associated with electrons jumping across depletion regions. The passage of each carrier across a pn-junction is dependent upon the carrier having sufficient energy to cross that region. This phenomenon can be modeled as a random event. Thus, an external current *I*, which appears to be a steady current, is really composed of a large number of random independent current pulses. If examined closely enough, the external current will have a small random ripple, and will in fact not be perfectly smooth as intended.

It can be shown that if the random independent current pulses have an average value I_D, then the resulting shot noise current, which rides on top of $I_{D,}$ has a mean-square value given by,

$$\overline{i^2} = 2qI_D B \tag{2.9}$$

In (2.9), q is the charge of a carrier (1.6×10^{-19} Coulombs) and B is the bandwidth in hertz. Notice how shot noise is independent of temperature.

Equation (2.9) is only valid until the frequency becomes comparable to $1/\tau$, where τ is the carrier transit time though the depletion region [6]. For frequencies smaller than $1/\tau$, shot noise spectral density is a constant function of frequency with amplitude $2qI_D$. Noise with a spectrum of constant frequency is sometimes referred to as white noise.

The probability density function (pdf) of shot noise as a function of I_D is Gaussian with a standard deviation given by, $\sigma = \sqrt{2qI_D B}$, and a variance $\sigma^2 = \overline{i^2}$.

The term shot noise is sometimes corruptly presented as originating from the name "Schottky". However, the term simply comes from the fact that if an audio system is connected to a shot noise source, the resulting output sounds like buckshot dropping on a hard surface [7].

2.2.4.2 Thermal Noise

Thermal noise is sometimes called Johnson Noise, because the first recorded measurement of this phenomenon was performed by J. B. Johnson at Bell Labs in 1928. Later, Johnson's colleague H. Nyquist was able to explain the phenomenon with a new atomic level theory (fluctuation-dissipation relationship) which accurately predicted the measured results obtained by Johnson.

Thermal noise occurs because of the random thermal motion of charge carriers in a conductor which is independent of any voltage applied across the conductor. Also, since typical electron drift velocities are much smaller than typical electron thermal

velocities, thermal noise is also independent of DC current flowing through the material. Thermal noise is present in any linear passive resistor and is usually the dominant noise contributing source in an amplifier. In MOSFET transistors, the channel acts as a resistor, and therefore a significant amount of thermal noise will be present.

In a resistor *R*, thermal noise can be modeled as a series-voltage generator ($\overline{v^2}$) for a shunt-current generator ($\overline{i^2}$), whose values are given by,

$$\overline{v^2} = 4kTRB \tag{2.10}$$

$$\overline{i^2} = 4kT\frac{1}{R}B \tag{2.11}$$

where *k* is Boltzmann's constant ($\approx 1.38\times10^{-23}\frac{m^2kg}{s^2K}$), *B* is the bandwidth, and *T* is the absolute temperature (Kelvin). Thermal noise voltage is sometimes written in rms form with units expressed as $nV/\sqrt{Hz}$ in order to emphasize the fact that the rms noise voltage is dependent on the square root of the bandwidth.

Thermal noise, like shot noise, has a amplitude distribution function that is Gaussian and a constant amplitude versus frequency. Therefore, shot noise and thermal noise are indistinguishable once they have manifested themselves in a circuit [6].

2.2.4.3 Flicker Noise (1/*f* Noise)

Flicker noise is another important noise phenomenon found in all active devices. Unlike shot and thermal noise, there is not one specific physical phenomenon to attribute as the cause of flicker noise. However, the source is mainly attributed by

charge traps associated with crystal defects in a semiconductor. The traps capture and release carriers in a random fashion thereby contributing a noise signal. Flicker noise energy is concentrated at low frequencies. Hence the reason is it sometimes referred to as *Pink Noise*.

Flicker noise is always associated with DC current, *I*, and is given by,

$$\overline{i^2} = K_1 \frac{I^a}{f^b} B \tag{2.12}$$

where *B* is a small bandwidth, K_1 is a constant for a particular device, *a* is a constant in the range of 0.5 to 2, and *b* is a constant approximately unity. Since the constants *a*, *b*, and K_1 are all different from device to device, even among devices on the same die, flicker noise cannot be characterized by a well-defined mean-square value depending on current flow and resistance such as shot and thermal noise. This is due to the randomness in the fabrication process producing defects in the crystal in the semiconductor devices.

Flicker noise is more significant in MOSFET transistors than in any other active device because of the abundance of charge flow near the S_i/S_iO_2 interface, which typically abounds with silicon defects. However, the larger size the MOSFET, the less flicker noise present because the gate oxide capacitance smoothes the fluctuations in channel charge. Nonetheless, in a MOSFET, the flicker noise can be modeled as a voltage source in series with the input gate terminal and is given by [6],

$$\overline{v^2} = \frac{K_1}{C_{ox} WL} \cdot \frac{1}{f} \cdot B \tag{2.13}$$

2.2.5 Noise Model of a MOSFET

Typically, the major noise sources in a MOSFET are caused by both thermal and flicker noise. Using the mean-square current representation of noise, the noise sources can be represented by noise-current generators as shown in the schematic in the small-signal model in Figure 2.7.

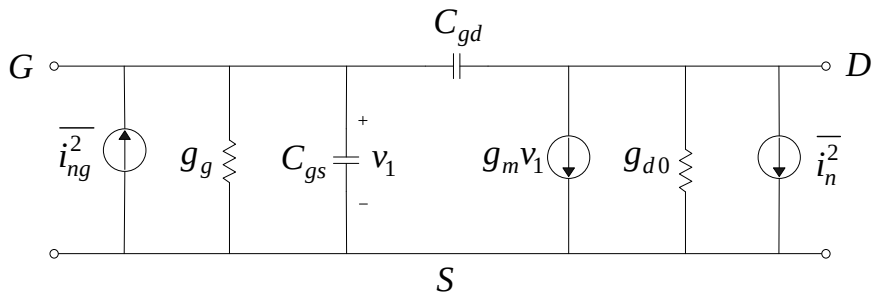

Figure 2.7 Noise sources in the MOSFET small-signal model

When the only input considered is the drain-to-source noise current, the output noise voltage of the NMOS transistor is given by $\overline{v_n^2} = \overline{i_n^2} r_o$.

The most significant noise source produced in the channel, especially for short-channel devices, is thermal noise. It can be shown that considering only thermal noise in the channel of the MOSFET, the drain to source noise current is given by,

$$\overline{i_n^2} = 4kT\xi g_{d0} B \tag{2.14}$$

where the drain noise coefficient ξ for long-channel transistors is only $2/3 < \xi < 1$, but becomes increasing more significant for short-channel devices. For example, ξ has been shown to be about 2.5 in some 0.25-μm MOS devices [15], but the amount of increase in ξ remains debatable and somewhat controversial [16].

The mean gate noise current ($\overline{i_{ng}^2}$) shown in Figure 2.7 is an induced quantity. It is induced by local fluctuations in the channel via capacitive coupling through the gate oxide. The local fluctuations in the channel can be caused by any one of the noise phenomenon mentioned above such as thermal, shot, and/or flicker noise. When only the thermal agitation of channel charge is considered, the gate noise current can be expressed as [7],

$$\overline{i_{ng}^2} = 4kT\delta g_g B \text{; where } g_g = \frac{\omega^2 C_{gs}^2}{5g_{d0}}. \tag{2.15}$$

In equation (2.15), g_g is the real part of the gate-to-source admittance, δ is the gate noise coefficient set at a value of 4/3 in long channel devices (or $\delta = 2\xi$), g_{d0} is the drain output conductance under zero V_{DS}, and C_{gs} is the gate-source capacitance. The induced gate noise becomes increasingly more significant at higher frequencies. This is due to the fact the g_g increases in value as frequency increases.

2.2.6 Noise figure

Noise figure has commonly been adopted as the metric of choice when characterizing receiver sensitivity. Consider a single device operating in the analog front-end of some RF communication receiver, such as an LNA, mixer or a filter. This device, in reality, cannot be completely noise free and will thus contribute to the noise picked up in by the desired signal propagating through the channel. Consequently, the receiver will be less sensitive, because a greater signal power to noise power ratio (S/N) will have to be applied at the input of the receiver to compensate for the noise generated from within the receiver itself. Therefore, the metric, noise factor (F), as given in

equation (2.16), indicates the degree of S/N degradation caused by a specific block within the system.

$$F = \frac{(S/N)_{in}}{(S/N)_{out}} \tag{2.16}$$

The $(S/N)_{out}$ will always be larger than the signal to noise ratio at the input, precisely because of the noise sources which exist within the block itself.

Noise figure is essentially the same metric of performance except expressed in a more convenient manner and is given by (2.17), which is simply the logarithmic to base ten of noise factor.

$$NF = 10 \cdot \log(F) \tag{2.17}$$

In order to see how noise figure cumulates throughout the system, consider the analog front-end shown in the Figure 2.8. In this Figure 2.8, each block represents a generic device in a communication receiver irrespective of functionality for illustrative purposes.

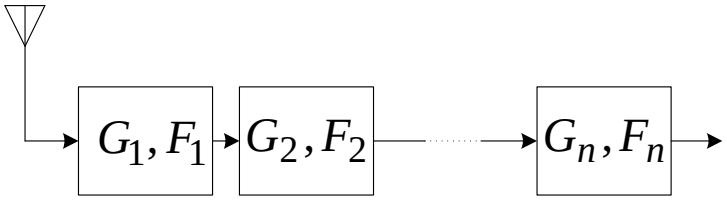

Figure 2.8 General cascaded receiver front-end with gain, G_i, and noise factor, F_i.

The signal enters into the receiver through the antenna, and is operated on by each successive block throughout the system. Each block contributes to the overall noise factor of the system governed by equation (2.18).

$$F_{tot} = F_1 + \sum_{i=1}^{n} \frac{F_{i+1} - 1}{\prod_{k=1}^{i} (G_k)} \tag{2.18}$$

Equation (2.18) shows that the noise factor of the first block, F_1, and the gain of the first block, G_1, has the greatest weighted effect on cumulative noise factor (F_{tot}) of the entire system. If G_1 is large, then terms in the sum portion of (2.18) become insignificant when compared to F_1. Therefore, the effective contribution of noise from any block downstream from the first is significantly reduced, placing the utmost importance on the first block. This means that for good system performance, the first block must not only add minimal noise to the signal, but it must also have adequate gain to relax the noise requirements on subsequent stages.

Typically, LNAs are the first system block in the receive path of a communication system (excluding the antenna), and are therefore the most influential in determining the sensitivity of the overall receiver. A large gain coupled with an extraordinary low noise figure, are both essential quality traits that LNAs in general need to exhibit. For UWB LNAs, this is an especially difficult criterion to satisfy because of the wide-bandwidth of operation.

In addition to the noise contributed by the sources from within the device itself, noise figure is also a function of the source admittance (or impedance) driving the system. The noise factor of a two-port network can be expressed as,

$$F = F_{\min} + \frac{R_n}{G_s} \left| Y_s - Y_{opt} \right|^2 . \tag{2.20}$$

In (2.20), $Y_s = G_s + jB_s$ is the source admittance presented to the two-port network, $Y_{opt} = G_{opt} + jB_{opt}$ is the source admittance that results in the optimum noise figure, $F_{\min}$ is the minimum noise figure of the network, R_n is the equivalent noise resistance of the two-port network, and G_s is the real part of the source admittance. The ratio R_n/G_s is an indicator of how dependent the system noise figure is on departures from optimum conditions. The two-port noise parameters for a MOSFET transistor are developed in [7] as,

$$B_{opt} = -\omega C_{gs}\left(1-\alpha|c|\sqrt{\frac{\delta}{5\xi}}\right) \tag{2.20}$$

$$G_{opt} = \alpha\omega C_{gs}\sqrt{\frac{\delta}{5\xi}\left(1-|c|^2\right)} \tag{2.21}$$

$$F_{\min} \approx 1+\frac{2}{\sqrt{5}}\cdot\frac{f}{f_T}\sqrt{\xi\delta\left(1-|c|^2\right)} \tag{2.22}$$

$$R_n = \frac{\xi}{\alpha}\cdot\frac{1}{g_m} \tag{2.23}$$

In the above four equations, $\alpha = g_m/g_{d0}$ which is typically unity for long channel devices, c is the cross-correlation coefficient between drain-noise and gate-noise, ξ is the scaling factor (a.k.a. drain-noise coefficient) which is dependent on channel length (roughly $2/3 < \xi < 2.5$), $\delta = 2\xi$ as given in [7], and g_{d0} is the drain output conductance under zero drain bias. As mentioned, α is unity for long channel devices but decreases as channel length decreases. The cross-correlation coefficient (c) theoretically assumes

the value of $-j0.395$. [7] states that c is very difficult to measure in reality, but published measurements fall within a factor of 2 of the value given.

F_{min} is the approximate minimum noise figure possible for a given MOSFET device. Figure 2.9 plots F_{min} versus frequency for a short-channel MOSFET device with transit frequency, f_T = 62 GHz. This f_T is the maximum transit frequency for the TSMC 0.18μm CMOS process. Also in Figure 2.9, the following assumptions were made in order to account for the short-channel noise effects: $\xi = 2.5$ and $\delta = 5$.

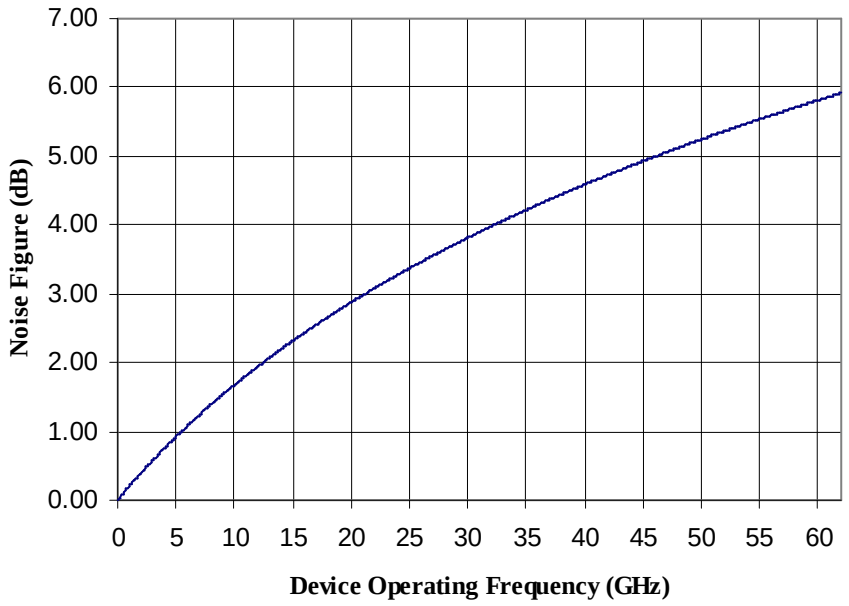

Figure 2.10 Approximate minimum noise figure for a short-channel MOSFET device as given by 3.23 ($\xi = 2.5$, $\delta = 5$, and $f_T = 62$ GHz)

2.2.7 Linearity

The most common narrow-band amplifier linearity parameters are input referred third harmonic intercept point (IIP_3) and the 1dB compression point ($1dBc$). For typical narrow-bandwidth LNAs, input referred third harmonic intercept point (IIP_3) is usually

used as a measure of the system's linearity. In an IR-UWB system which does not use a carrier frequency, the third harmonic of the carrier frequency is meaningless and therefore IIP_3 will not be calculated in this thesis. But in an MB-OFDM UWB system which does use a carrier signal with band centered frequency, a measurement of IIP_3 and 1*dBc* would be a valuable metrics to the system designer.

In this thesis, the 1*dBc* for the LNA designed herein is simulated at a particular in-band frequency. This is done mainly to demonstrate that the LNA has an adequate linear dynamic range capable of handling anticipated UWB signal inputs.

In reality, an amplifier can only handle a practical amount of input power before saturation of the device occurs. Saturation can be caused by several factors, but an amplifier with MOS devices usually saturates because one of the transistors in the circuit enters the triode region of operation due to excessively high input signals. Figure 2.10 shows an example response of an amplifier to a power sweep of the input signal. In this figure, there are two response lines shown: fundamental and third-order inter-modulation. As the input power increases, notice that as the power of the input signal increases, the output responses become "compressed". The point at which the fundamental response compresses by 1*dB* in the output is called the 1*dB* compression point (1*dBc*).

The third-order inter-modulation response is produced when two signals near in frequency are applied to the input of an amplifier that is not perfectly linear. The non-linear terms of the amplifier cause the two signals to "mix" together producing a signal output at either the sum or difference of the two frequencies.

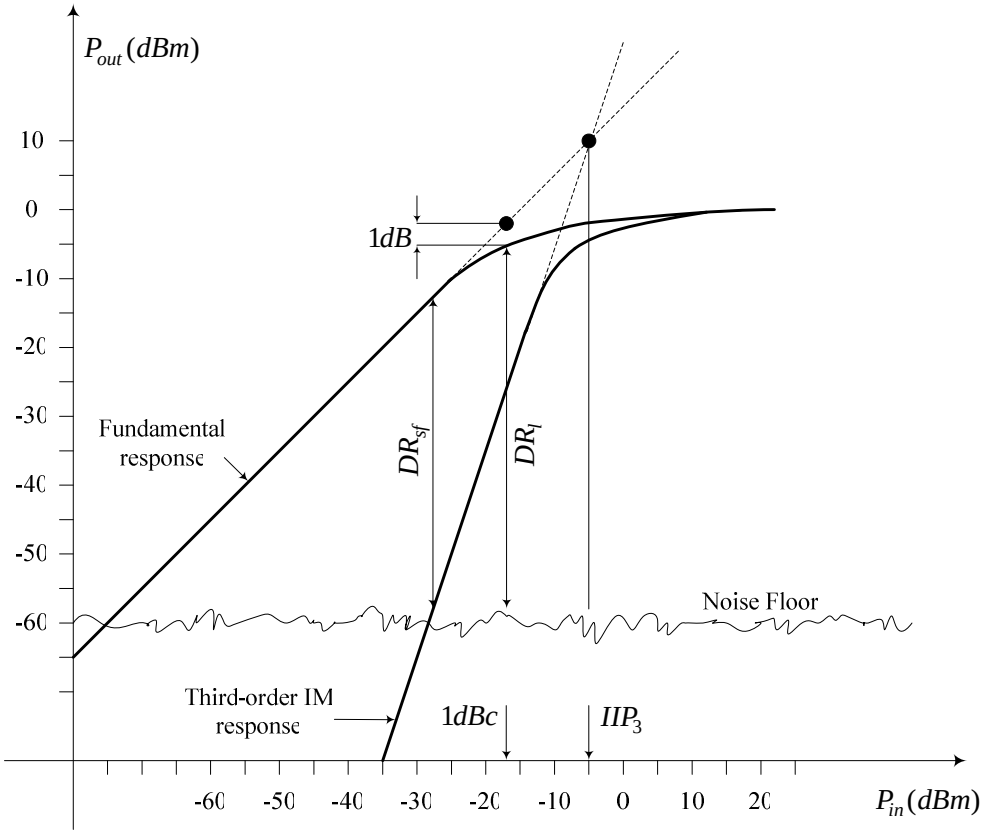

Figure 2.10 Illustration of linear dynamic range (DR_l) and spurious free dynamic range (DR_{sf})

There are two dynamic ranges which are associated with either the IIP3 or the 1dBc of a given amplifier. In Figure 2.10, DR_{sf} and DR_l as indicated represent the output dynamic ranges corresponding to the IIP_3 and 1dBc, respectively. One end of the dynamic range metric is bound by the power level of the noise, and the other by either IIP_3 or 1dBc. Any signal below the noise floor is considered undetectable, and therefore the noise floor is sometimes referred to as the minimum detectable signal level. The spurious free dynamic range (DR_{sf}), is the output power range from the point at which the third-order response become detectable to the power level of the

fundamental response. The linear dynamic range (DR_l), is the output power range between the minimum detectable signal level and the output referred 1*dBc*.

Unlike most narrow-bandwidth systems, linearity is generally not a source of major concern in UWB systems primarily because of the FCC restrictions binding the transmitted power level to below -41.3*dBm/MHz*. Since powerful signals are not allowed to be transmitted, the importance of the linearity characterizing parameters for the amplifiers can usually be ignored provided the amplifier is at least marginally linear.

2.2.8 Stability

Stability may be the most important property of any system. If the system is not stable, then it may be prone to uncontrollable oscillations which can internally damage the system. And depending on the system application, it could be hazardous to system operators. In the case of an LNA however, un-stability can cause internal circuitry damage and ensure that the amplifier will not work.

The Rollett stability factor, denoted by k, is given by the following expression,

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}||S_{21}|} \text{ where } \Delta = S_{11}S_{22} - S_{12}S_{21} \tag{2.23}$$

An amplifier is unconditionally stable if $k > 1$.

CHAPTER 3

LOW NOISE AMPLIFIERS

The low noise amplifier (LNA) is typically the first block in a wireless receiver. The main function of the LNA is to provide enough signal gain so as to minimize the effect subsequent stages while contributing a minimum amount of noise to the signal (see equation (2.18)). In addition to this, an LNA should be sufficiently linear to handle anticipated large input signals and must also present a specific real input impedance over the desired band of operation to the source antenna (typically 50Ω).

In section 3.1, desired characteristics of an LNA are presented which is then followed in the next section with a discussion about LNA topologies that can achieve a real input impedance over a reasonably sized band of operation.

3.1 Characteristics of the LNA

The basic block diagram of a typical LNA employing wideband impedance matching networks is shown in Figure 3.1, which consists of three blocks, namely, an input matching network (IMN), an amplifier, and an output matching network (OMN). Although the structure shown in Figure 3.1 has been the most popular of late and has shown the most success recently, there have been other structures proposed for implementing a wideband LNA. Other structures include distributed amplifiers and noise canceling techniques.

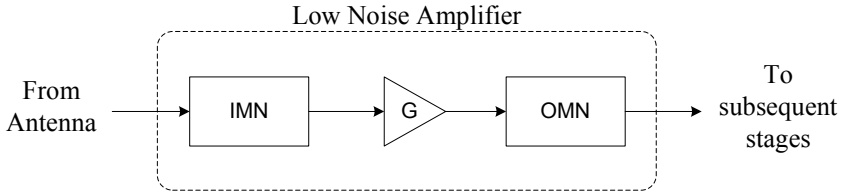

Figure 3.1 Functional block diagram of a LNA

The LNA must exhibit several distinguishing features or characteristics which makes it unique when compared to other types of amplifiers. As Figure 3.1 suggests, minimal reflections between presequent and subsequent stages must be realized by employing appropriate matching networks. Ideally, the matching network should match the impedances between stages for maximum power transfer as well as matching to realize minimum noise figure. However, this is seldom achieved with any technology, but specifically with MOSFETs this is next to impossible [7]. Therefore, the matching networks must first match impedances and then other compromises or considerations within the circuit can be made to reduce noise figure. A typical rule of thumb to ensure that a good power match has been made is when input and output reflection coefficients (S_{11} and S_{22} for a two-port network, respectively) are below -10dB.

Also, the LNA must have high reverse isolation. A high reverse isolation (S_{12} in a two-port network) ensures that signals caused by spurious outputs from subsequent stages which propagate to the input of the LNA can be deemed negligible. Reverse isolation, although very important, is usually dealt with when considering the LNA architecture. An architecture which is obviously susceptible to reverse isolation at any frequency should not be chosen if possible.

The LNA must also be acceptably linear, i.e. the linear dynamic range (DR_l) spans the intended input signal amplitude space. As previously mentioned, for UWB applications, the maximum output power allowed is -41dBm which does not place a very tough requirement on the linearity of an UWB LNA. The proposed LNA should only expect to see signals with power less than -41dBm at the input.

In addition, performing satisfactorily in the area of input and output matching and reverse isolation, the LNA must do so while consuming minimal power, having adequate gain, and a minimal noise figure.

3.2 Basic Topologies

As previously mentioned, presenting a real (resistive) impedance to the driving source and loading element is a critical requirement. This is the case because LNAs are usually driven by antennas with a real 50Ω characteristic impedance in the desired band of operation. In order to provide an optimum power match with the source antenna, the input impedance of the LNA must be very close to purely resistive with a value close to 50Ω. However, because the input of the LNA is connected to a capacitive node, providing good impedance matching to the source without degrading the noise performance is very difficult [7]. There are four basic LNA topologies which employed to realize a real input impedance.

3.2.1 Resistive Termination

The resistive termination method is the most rudimentary and strait forward in comparison. The desired input impedance (R_d) is simply placed as shown in Figure 3.2.

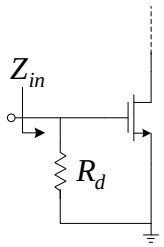

Figure 3.2 Resistive termination topology

This connection ensures that $Z_{in} \approx R_d$ at frequencies much lower than the transit frequency (f_T). This occurs because R_d is lower than the input impedance of the transistor, and will therefore dominate in the parallel combination of the two.

One of the main drawbacks associated with the resistive termination method is that the termination resistor, R_d, adds a significant amount of thermal noise to the signal as well as attenuates the input signal by a factor of 2 before the transistor. Thus, because of these two effects, the noise figure of resistively terminated LNA is significantly degraded and unacceptable for an LNA. According to [7], the lower bound on noise factor for this topology is given by,

$$F \geq 2 + \frac{4\xi}{\alpha} \cdot \frac{1}{g_m R_d} \tag{3.1}$$

Equation (3.1) is a very low estimate and is typically only accurate at low frequencies because induced gate noise has been ignored altogether in the derivation. With this topology, noise figures in excess of $11dB$ have been reported in an 800MHz CMOS amplifier [7].

Another drawback is that the parallel combination of R_d and the input impedance of the transistor is directly tied to the frequency of operation. This

immediately suggests that the resistive termination is not a good broadband matching candidate.

3.2.2 $1/g_m$ Termination

The $1/g_m$ termination simply uses the input impedance of a common-gate stage to present the real impedance. The conceptual topology is shown in Figure 3.3.

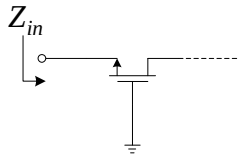

Figure 3.3 $1/g_m$ Termination topology

A more detailed analysis of the input impedance of a common-gate stage is shown in section 4.2.1, but basically the input impedance of the common-gate is determined by $1/g_m$ of the transistor. This architecture is very simple, and can easily achieve the correct input impedance matching. Furthermore, this topology also appears to be a good candidate for wideband impedance matching because the transconductance (g_m) of a MOSFET transistor is at least a weak function of frequency.

In the common-gate configuration, the noise figure is solely dependent on the noise sources from within the transistor. Ignoring induced gate noise, the noise factor of the common-gate configuration is given by,

$$F = 1 + \frac{\xi}{\alpha} \cdot \frac{1}{g_m R_S} \tag{3.2}$$

where R_S is the source resistance feeding the common-gate circuit. When designing the common-gate shown in Figure 3.4 for optimal power match, $1/g_m = R_S$ and (3.2) becomes,

$$F \geq 1 + \frac{\xi}{\alpha} \tag{3.3}$$

Equation (3.4) expresses noise factor, *F*, as a lower bound because induced gate noise current is not included. In (3.2) and (3.3), ξ is the drain noise coefficient, and $\alpha = g_m / g_{d0}$. For long-channel devices, ξ = 2/3 and α = 1 which implies a lower bound noise figure of 2.22 *dB*, which is expected to be significantly higher for short channel lengths. The inequality in (3.3) does not consider induced gate noise and is therefore a very low estimate for a lower bound of noise factor.

The common-gate topology offers a promising method for wideband impedance matching but suffers from an unavoidably high noise figure for short channel devices. However, when put into perspective, the high noise figure is still considerably less than the resistively terminated topology and the Shunt-Series Feedback topology.

3.2.3 Shunt-Series Feedback

The Shunt-Series feedback topology is shown in Figure 3.4 and is capable of providing a real input impedance.

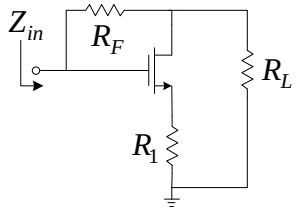

Figure 3.4 Shunt-Series feedback topology

This LNA topology outperforms the resistive terminated topology in terms of noise figure, but its noise figure still exceeds the F_{min} of the MOSFET device. Even though this topology does not realize the minimum possible noise figure, the wide-bandwidth

characteristics combined with an acceptable noise figure have made it a suitable choice for wideband LNAs.

CHAPTER 4

PROPOSED UWB LNA

This chapter will present the proposed LNA and some of the design issues associated with it. In the first section, the philosophy behind the choice of architecture will be presented. In the second, third, and fourth sections, specific details about the different stages of the LNA will be discussed. Finally, in the fifth section, the simulations of the entire completed LNA will be presented. And lastly, in section six a comparison is made between the performances of the LNA designed in this thesis with other UWB CMOS LNAs.

4.1 Proposed Architecture

Being the first block encountered in a wireless receiver, the LNA deals with extremely small analog signals that must be amplified with minimum noise degradation so that subsequent stages can perform additional signal processing on the signal. Also, the most promising implementation strategy which delivers the lowest cost and smallest sized product solution to electronic circuits and systems is combining digital and analog functions onto one die forming a complete system-on-chip (SOC). However, much of the hardship associated with SOCs is that the digital signal components produce large amounts of switching noise which detrimentally affect the sensitive analog circuitry located on the same chip especially the LNA. Much of the hoopla surrounding UWB communication circuitry is that the UWB system will enjoy the same SOC advantages as Bluetooth and Zigbee have. In order to accomplish this, the analog circuitry must be

robust against the switching noise caused by the digital circuitry. The proposed LNA utilizes a differential architecture to that end. The differential architecture rejects a significant amount of noise caused by the digital switching because such noise would be regarded as common-mode.

In addition to analog circuit's sensitivity to noise, another major issue to be concerned with for SOC implementation is size. The wideband characteristics of an LNA are largely determined by its broadband matching network. In a UWB LNA design, achieving flat gain is more important than obtaining a high maximum-gain. Thus, it is necessary to fix the LNA gain over the frequency range of interest through frequency compensated matching techniques. For narrow bandwidth LNA, the input or output matching network is usually realized with micro strip lines or simple passive elements. Broadband matching, however, is extremely challenging to realize over a wide frequency range such as UWB. There are several possible topologies such as p, T and L structure for the broadband matching network using passive elements [17]. In these structures, however, it is necessary to increase the order of the filter in order to broaden the bandwidth with small ripple and small loss. Increasing the order of the filter engenders a large chip size due to the large number of passive components needed. For this reason, the proposed LNA utilizes active components to perform the wideband impedance matching.

In choosing active matching, a fundamental trade-off was made between noise figure and size. Passive matching networks do not degrade the noise performance of the system nearly as much as active matching. However, as shown and verified by this

thesis, the active matching networks can still provide a suitable noise figure for an UWB LNA.

The proposed UWB LNA functions as the block diagram shown in Figure 3.1. However, both input and output matching networks are active circuits instead of passive. The overall simplified schematic proposed is shown in Figure 4.1

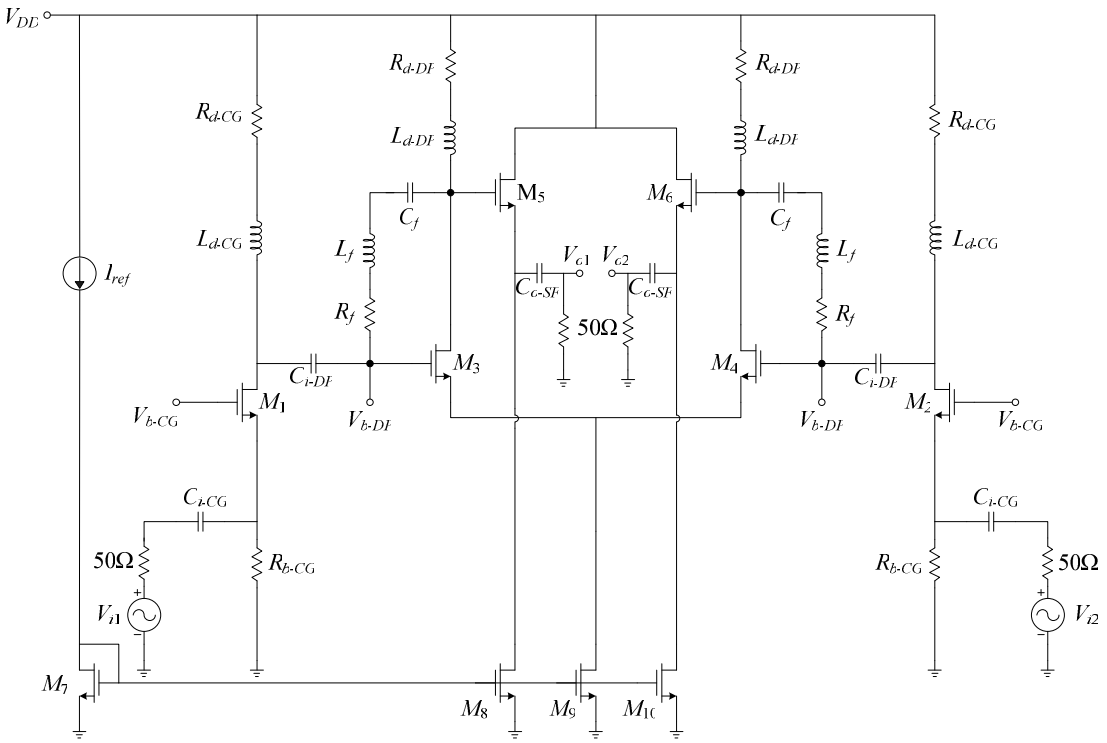

Figure 4.1 Schematic of the Proposed UWB LNA

One of the difficulties with Ultra-wideband design comes from the realizability of “true” inductance. In planar fabrication process, such as CMOS, in order to make an inductor a spiral trace pattern from a metal layer must be formed to provide self inductance. Therefore, making inductors in CMOS is difficult, and making good inductors is even harder. When it comes to designing UWB circuits in CMOS, one

does not actually have inductors in the “box” of devices and elements of which to choose from. What a designer actually has at hand is a spiral inductor, which can be modeled by ideal R, L, and C components as shown in Figure 4.2.

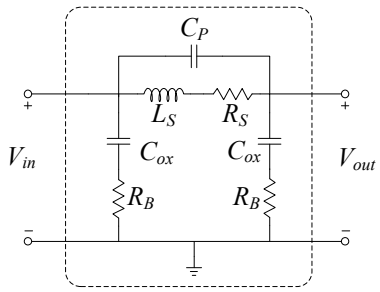

Figure 4.2 Component model of a spiral inductor [18]

In Figure, L_S represents the actual self-inductance realized by the spiral patterning and R_S is the series resistance in traces. The model also contains oxide capacitances (C_{ox}), bulk resistances (R_B), and inter-wire (inter-trace) capacitance (C_P). Ideally, the impedance of the spiral inductor would be $Z = jwL_S$. However, because of C_{ox} and C_P, parasitic capacitances involved with the spiral inductor overcome the inductance effect, and the impedance actually starts decreasing with frequency [18]. C_P and C_{ox} become shorts at high frequencies.

Figure 4.3 shows the magnitude of impedance versus frequency of an ideal 7.5*nH* inductor and actual impedance realized by an attempted 7.5*nH* realized in a spiral inductor from the TSMC 0.18μm technology. As can be seen from the table in Appendix A, this is the actual spiral inductor used in the feedback path of the differential core (L_f).

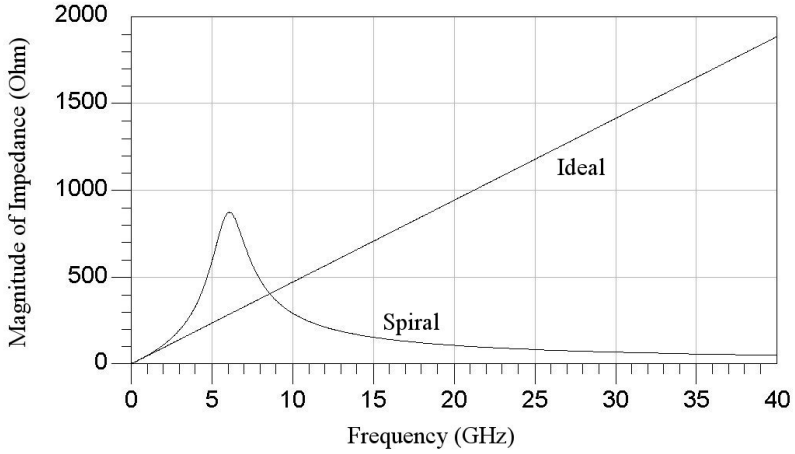

Figure 4.3 Magnitude of impedance of a 7.5*nH* spiral inductor versus frequency

4.2 Input Active Matching Stage

The common-gate input stage (as shown in Figure 4.3) was designed to perform two very important functions. First, the common-gate stage must have an input impedance of about 50Ω in order to satisfactorily minimize reflections between the source and the common-gate stage. Second, in order to realize a reasonably low noise figure for the entire LNA, the common-gate stage must provide sufficient gain so as to minimize the effect of the noise contributions from the downstream differential pair and source follower stages. Simulations showed that a gain of at least 10*dB* across the entire band in the common-gate stage as configured in Figure 4.3 must be realized in order to keep the noise figure of the entire LNA at or below about 5.5*dB*. The common-gate stage exhibits a shunt-peaking load inductor to enhance the wideband properties.

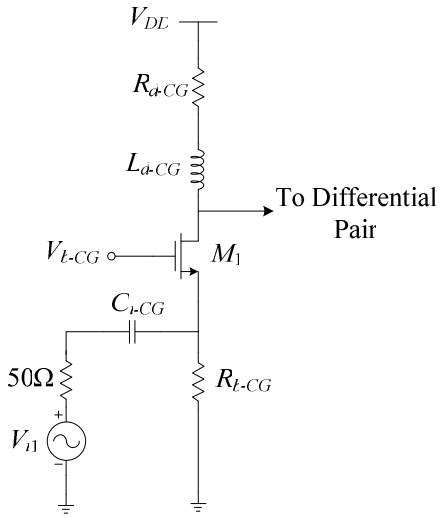

Figure 4.4 Schematic of the input active matching stage

4.2.1 Input Impedance of Common-gate stage

To calculate the input impedance of the common-gate stage, consider the small-signal model shown in Figure 4.4. In (4.1), $R_{i\text{-}CG}$ is calculated ignoring g_{mb}. This is fairly accurate because the body and source are tied together in the actual situation shown in Figure 4.4. Even though g_{mb} helps the gain of the common-gate stage, the noise sources generated as a direct result of g_{mb} noticeably degrade the noise figure while the small additional gain achieved does not compensate for the noise added.

The small-signal model shown in Figure 4.5, $Z_L = (R_{d-CG} + sL_{d-CG}) \| Z_{i-DP}$, represents the entire load seen by the transistor, including the effects of the differential pair input impedance. For calculation purposes, a test voltage (v_t) was applied at the node where the test current (i_t) is labeled in Figure 4.5. In this figure, C_{gs} represents the gate-source capacitance of transistor M_1.

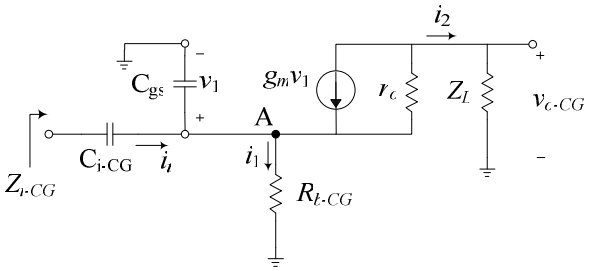

Figure 4.5 Small-signal model of the common-gate input stage for input impedance calculation

Performing KCL at node A and re-arranging gives,

$$i_t = v_1\left[\frac{1}{Z_{Cgs}} + \frac{1}{r_{o1}} + \frac{1}{R_{b-CG}} + g_{m1}\right] - \frac{v_{o-CG}}{r_{o1}}. \tag{4.1}$$

Performing KCL at the output node and re-arranging gives,

$$v_o = \frac{v_1\left(\frac{1}{r_{o1}} + g_{m1}\right)}{\frac{1}{r_{o1}} + \frac{1}{Z_L}}. \tag{4.2}$$

Substituting (4.1) into (4.2) and performing algebraic reduction gives,

$$\frac{v_1}{i_t} = \frac{r_{o1} + Z_L}{\frac{r_{o1} + Z_L}{\left[sC_{gs} + \frac{1}{R_{b-CG}} + g_{m1}\right]} + 1 - g_{m1}Z_L}. \tag{4.3}$$

The impedance $Z_{Cgs} = 1/(sC_{gs})$. Now, including the effect of $C_{i\text{-}CG}$, the input impedance of the common-gate stage can be expressed as,

$$Z_{i-CG} = \frac{v_1}{i_t} + \frac{1}{sC_{i-CG}} = \frac{r_{o1} + Z_L}{\left(r_{o1} + Z_L\right)\left[sC_{gs} + \frac{1}{R_{b-CG}} + g_{m1}\right] + 1 - g_{m1}Z_L} + \frac{1}{sC_{i-CG}}.$$

(4.4)

For simplification purposes, let $r_{o1} \rightarrow \infty$ and (4.4) becomes,

$$Z_{i-CG} = \frac{1}{\left[sC_{gs} + \frac{1}{R_{b-CG}} + g_{m1} \right]} + \frac{1}{sC_{i-CG}}. \tag{4.5}$$

Notice how letting $r_{o1} \rightarrow \infty$ removes the dependency of the loaded input impedance of the common-gate stage from the effects of Z_L. Since $C_{i\text{-}CG}$ is really large in comparison to C_{gs}, the second term in (4.5) can be ignored in the UWB frequency range of operation. Now, the input impedance of the common gate stage becomes,

$$Z_{i-CG} = \frac{1}{\left[sC_{gs} + \frac{1}{R_{b-CG}} + g_{m1} \right]}. \tag{4.6}$$

Notice, if $C_{gs} = 0$, and $1/R_{b\text{-}CG} \rightarrow 0$, we have the same situation as described in section 3.2.2 of this thesis.

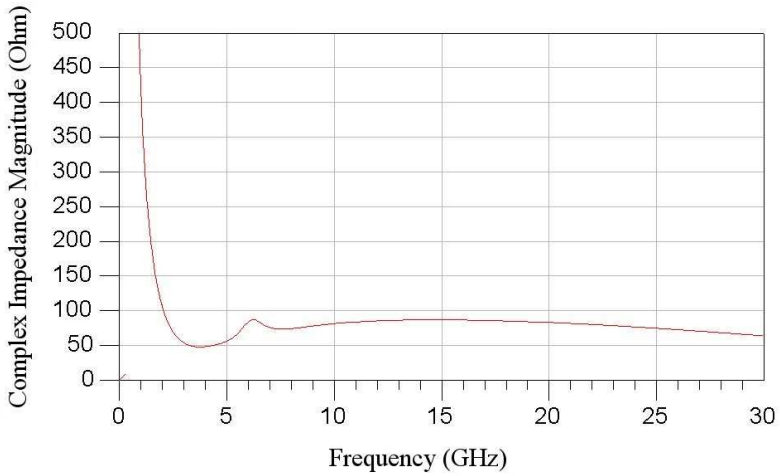

Figure 4.6 Simulated input impedance of common-gate stage

Figure 4.6 shows the simulated input impedance of the common-gate stage using the component values given in Appendix A. Notice from the figure, that around the bandwidth of operation, the impedance magnitude looking into the common-gate stage is approximately 50Ω. However, notice at 6GHz a sudden rise in input impedance occurs. This occurs but was not predicted by (A.15) because of the assumption that $r_{o1} \rightarrow \infty$. With r_{o1} assuming finite values, the input impedance of the common-gate stage is more accurately described by (4.6) which varies proportionally to Z_L and thus adding dependency of $Z_{i\text{-}CG}$ onto $Z_{i\text{-}DP}$. Therefore, the spike around 6GHz $Z_{i\text{-}DP}$ (simulated in Figure 4.8) directly causes the spike at approximately 6GHz in $Z_{i\text{-}CG}$.

4.2.2 Gain Analysis of Common-gate stage

In the model shown in Figure 4.7, $Z_L = (R_{d-CG} + sL_{d-CG}) \| Z_{i-DP}$, which represents the entire load seen by the common-gate stage. $Z_{i\text{-}DP}$ represents the total input impedance of the differential pair stage. The body transconductance (g_{mb}) was ignored because in the common-gate stage the body directly tied to the source terminal, and therefore $v_{sb} = 0$ at all times.

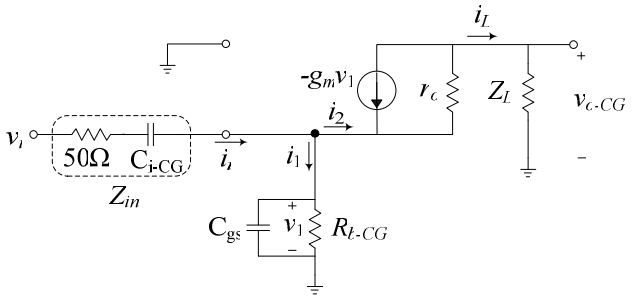

Figure 4.7 Small-signal equivalent model for the common-gate stage

Observing Figure 4.7 immediately suggests,

$$i_i = \frac{v_i - v_1}{Z_{in}} \text{ where } Z_{in} = 50\Omega + \frac{1}{sC_{i-CG}} \tag{4.7}$$

$$i_2 = \frac{v_{o-CG}}{Z_L} \tag{4.8}$$

$$i_1 = \frac{v_1}{Z_{Cgs} \| R_{b-CG}} \tag{4.9}$$

In (4.9), $Z_{Cgs} = 1/(sC_{gs})$ and it represents the impedance seen between the gate and source terminals of M_1 in this section. Using Kirchoff's current law (KCL) at the node directly above $R_{b\text{-}CG}$ we get,

$$i_2 = \frac{v_1 - v_{o-CG}}{r_{o1}} + g_{m1} v_1 \ . \tag{4.10}$$

Substituting (4.8) into (4.10) and solving for v_1 gives,

$$v_1 = \frac{v_{o-CG} r_{o1}}{(1 + g_{m1} r_{o1})(Z_L \| r_{o1})}. \tag{4.11}$$

Now, substituting (4.8), (4.9), and (4.11) into (4.1) for i_2, i_1 and v_1, respectively, gives,

$$\frac{v_{o-CG}}{Z_L} + \frac{v_{o-CG} r_{o1}}{(1 + g_m r_{o1})(Z_L \| r_{o1})(Z_{Cgs} \| R_{b-CG})} = \frac{v_i}{Z_{in}} - \frac{v_{o-CG} r_{o1}}{(1 + g_m r_{o1})(Z_L \| r_{o1})(Z_{Cgs} \| R_{b-CG}) Z_{in}} \tag{4.12}$$

Re-arranging (4.12),

$$v_{o-CG} \left[\frac{1}{Z_L} + \frac{r_{o1}}{(1 + g_{m1} r_{o1})(Z_L \| r_{o1})(Z_{Cgs} \| R_{b-CG})} + \frac{r_{o1}}{(1 + g_{m1} r_{o1})(Z_L \| r_{o1}) Z_{in}} \right] = \frac{v_i}{Z_{in}}. \tag{4.13}$$

Solving for $v_{o\text{-}CG}/v_i$ and performing algebraic simplification gives a small-signal voltage gain of,

$$A_{v-CG} = \frac{v_{o-CG}}{v_i} = \frac{(1+g_{m1}r_{o1})(Z_L \| r_{o1})(Z_{Cgs} \| R_{b-CG})Z_L}{Z_L r_{o1}(Z_{in}+R_{b-CG}) + Z_{in}(Z_{Cgs} \| R_{b-CG})(1+g_{m1}r_{o1})(Z_L \| r_{o1})}. \tag{4.14}$$

The result for small-signal gain of the common-gate stage is fairly complete in (4.14); however, in order to gain some simplifications need to be made. For starters, letting $r_{o1} \rightarrow \infty$ gives,

$$A_{v-CG} = \frac{g_{m1}Z_L(Z_{Cgs} \| R_{b-CG})}{Z_{in}+R_{b-CG}+Z_{in}(Z_{Cgs} \| R_{b-CG})g_{m1}}. \tag{4.15}$$

Also, at really high frequencies (UWB range of operation) Zin $\approx$ 50Ω, this occurs because $C_{i\text{-}CG}$ is very large in comparison to C_{gs}.

As shown in (4.15), $A_{v\text{-}CG}$ depends heavily on Z_L which is dependent on $Z_{i\text{-}DP}$. Z_L depends strongly on $Z_{i\text{-}DP}$ because $Z_{i\text{-}DP}$ is comparable to $Z_{d\text{-}CG} = R_{d\text{-}CG} + L_{d\text{-}CG}$ in value. Therefore, obtaining a flat gain response across the entire band of operation becomes exceedingly difficult because of the complex loading profile of $Z_{i\text{-}DP}$. Figure shows the simulated loaded input impedance of the differential pair (loaded with the source-follower stage) when the components assume the values tabularized in Appendix A.

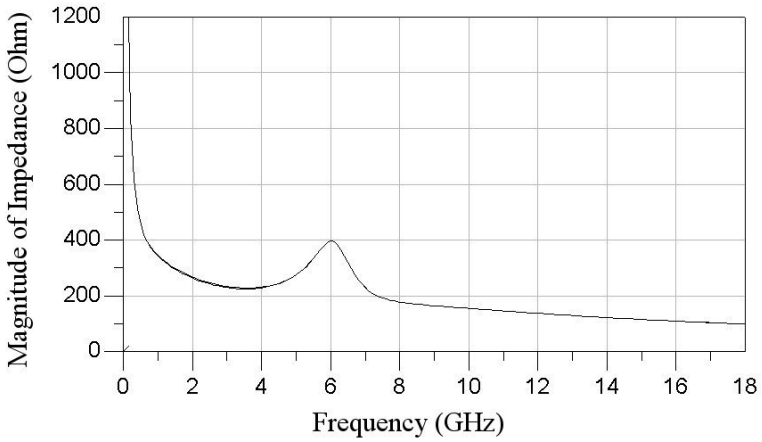

Figure 4.8 Loaded input impedance of differential stage

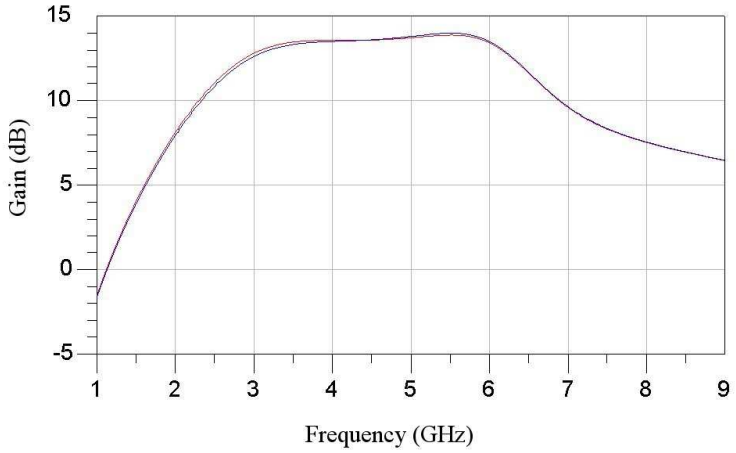

Figure 4.9 Gain versus frequency through loaded common-gate stage

4.3 Output Active Matching Stage

The common-drain (source-follower) output stage's primary purpose is to provide adequate matching with the loading 50Ω terminal. However, the gain of a source follower is always less than unity [6]. Therefore, it is very important that in addition to matching, the source follower stage must also realize a gain as close to unity

as possible. Accomplishing both of these feats optimally is not possible, and a trade off between gain and output impedance must be made. Of course, providing acceptable matching with the 50Ω trumps optimal gain, since without acceptable matching gain would be sacrificed anyway. As can be seen from Figure, the gain achieved was approximately -6*dB* through the source-follower. In order to accomplish the broadband matching, the gain of the source-follower had to be significantly sacrificed.

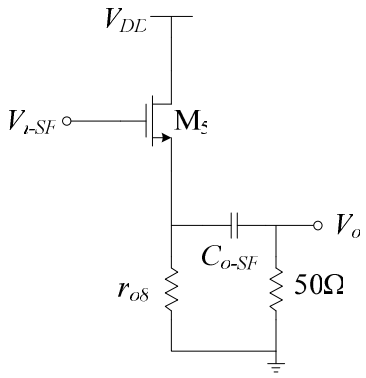

Figure 4.10 Schematic of the output active matching stage

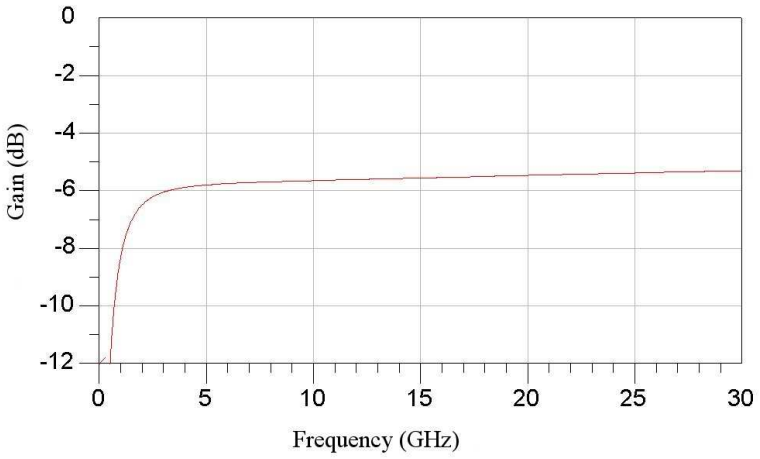

Figure 4.11 Gain versus frequency of the loaded source-follower stage

4.3.1 Output Impedance of Source-follower stage

The test situation for calculating the output impedance of the source follower is shown in Figure 4.12. For calculating output impedance, short the gate of transistor M_5 and remove the 50Ω load from Figure 4.10 and the test situation shown in Figure 4.12 results.

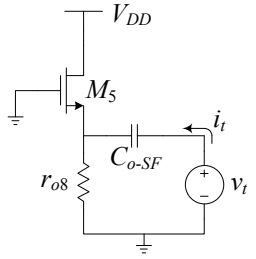

Figure 4.12 Test situation for calculating the output impedance of the source-follower stage

The reduced and re-arranged small-signal model for Figure 4.12 is shown Figure 4.13 where $Z_\Delta = Z_{Cgs} \| r_{o5} \| r_{o8}$, $Z_{Cgs} = 1/(sC_{gs})$ of transistor M_5, r_{o8} is the output impedance of transistor M_8, and $Z_{Co\text{-}SF} = 1/(sC_{o\text{-}SF})$.

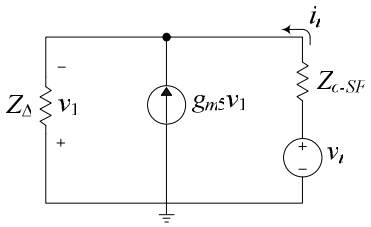

Figure 4.13 Reduced small-signal model for calculating output impedance of the source-follower stage

Performing KCL at the top node in Figure 4.13 gives,

$$i_t + g_{m5} v_1 + \frac{v_1}{Z_\Delta} = 0 \,. \tag{4.16}$$

Performing KVL around the outermost loop of the small-signal model gives,

$$v_1 = -v_t + i_t Z_{Co-SF}\,. \tag{4.17}$$

Substituting (4.17) into (4.16) and re-arranging we get,

$$i_t\left[1 + g_{m5}Z_{Co-SF} + \frac{Z_{Co-SF}}{Z_\Delta}\right] = v_t\left[g_{m5} + \frac{1}{Z_\Delta}\right]. \tag{4.18}$$

Solving for v_t / i_t, and simplifying (4.18) becomes,

$$Z_{o-SF} = \frac{v_t}{i_t} = \frac{Z_\Delta + g_{m5}Z_{Co-SF}Z_\Delta + Z_{Co-SF}}{1 + g_{m5}Z_\Delta} \quad . \tag{4.19}$$

Since $C_{o\text{-}SF}$ is large, assuming frequencies in the gigahertz range implies that $Z_{Co\text{-}SF} \rightarrow 0$. Then (4.19) simplifies to,

$$Z_{o-SF} = \frac{Z_\Delta}{1 + g_{m5}Z_\Delta}\,. \tag{4.20}$$

Now, at frequencies great enough to neglect $Z_{Co\text{-}SF}$ but low enough to keep Z_{Cgs} high so that $g_{m5}Z_\Delta >> 1$, then,

$$Z_{o-SF} \approx \frac{1}{g_{m5}}\,. \tag{4.21}$$

From (4.21), it can be observed that the value of the output impedance is roughly independent of frequency around the UWB range of operation. Therefore, an output match can be realized by specifying $1/g_{m5} \approx 50\Omega$.

4.3.2 Input Impedance of Source-follower stage

To calculate the loaded input impedance of the source-follower stage ($Z_{i\text{-}SF}$), consider the small-signal model of the circuit shown in Figure 4.10.

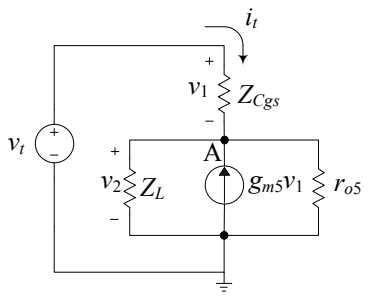

Figure 4.14 Small-signal model of the source-follower for input impedance calculation purposes

The small-signal model is shown in Figure 4.14 with,

$$Z_L = r_{o9} \left\| \left(50\Omega + \frac{1}{sC_{o-SF}} \right) \right. . \tag{4.22}$$

Performing KCL at node A gives,

$$i_t = \frac{v_2}{Z_L} - g_{m5}\left(v_t - v_2\right) + \frac{v_2}{r_{o5}} . \tag{4.23}$$

From observing the small-signal model with KVL in mind we can see that,

$$v_2 = v_t - i_t Z_{Cgs} \text{ where } Z_{Cgs} = \frac{1}{sC_{gs}} . \tag{4.24}$$

Substituting (4.24) into (4.23) and performing some algebraic manipulations we get,

$$i_t \left[1 + \frac{Z_{Cgs}}{Z_L} + g_{m5} Z_{Cgs} + \frac{Z_{Cgs}}{r_{o5}} \right] = v_t \left[\frac{1}{Z_L} + \frac{1}{r_{o5}} \right] . \tag{4.25}$$

Re-arranging (4.25) gives,

$$Z_{i-SF} = \frac{v_t}{i_t} = \left[\frac{Z_{Cgs} + g_{m5} Z_{Cgs} r_{o5} Z_L + r_{o5} Z_{Cgs} + r_{o5} Z_L}{r_{o5} Z_L} \right] \left(Z_L \| r_{o5} \right) . \tag{4.26}$$

Consider the case when $r_{o5} \to \infty$. Equation (4.26) becomes,

$$Z_{i-SF} = g_{m5} Z_{Cgs} Z_L + Z_{Cgs} + Z_L . \tag{4.27}$$

Assuming $r_{o9} << 50\Omega$ and at high frequencies $1/(sC_{o\text{-}SF}) \rightarrow 0$ because $C_{o\text{-}SF}$ is large, then $Z_L \approx 50\Omega$. And since $Z_{Cgs} = 1/(sC_{gs})$, (4.27) can also be expressed as,

$$Z_{i-SF} = \left[\frac{g_{m5}}{sC_{gs}} + 1 \right] Z_L + \frac{1}{sC_{gs}} . \tag{4.28}$$

Further increasing frequency so that $1/(sC_{gs}) \rightarrow 0$, then $Z_{i\text{-}SF} \rightarrow 50\Omega$. However, as verified by simulations (Figure 4.15), this situation does not occur until the frequency becomes greater than about 50GHz. Therefore, (4.28) with $Z_L \approx 50\Omega$ is a good approximation for the input impedance of the source follower output stage within the UWB operating band.

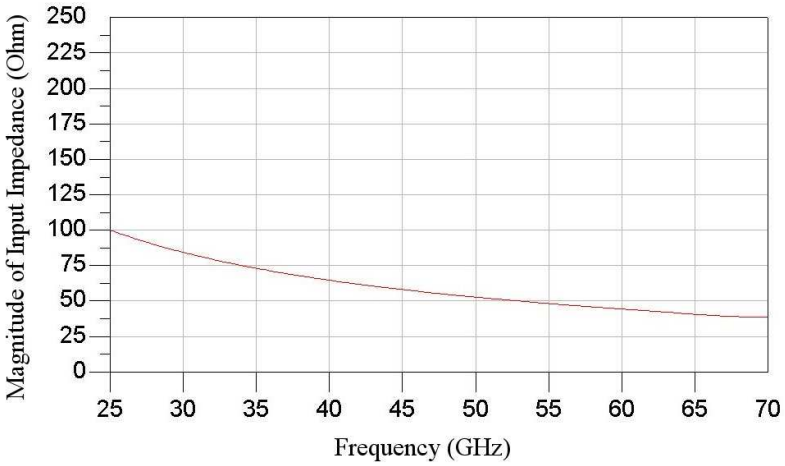

Figure 4.15 Loaded input impedance of the source-follower at very high frequencies

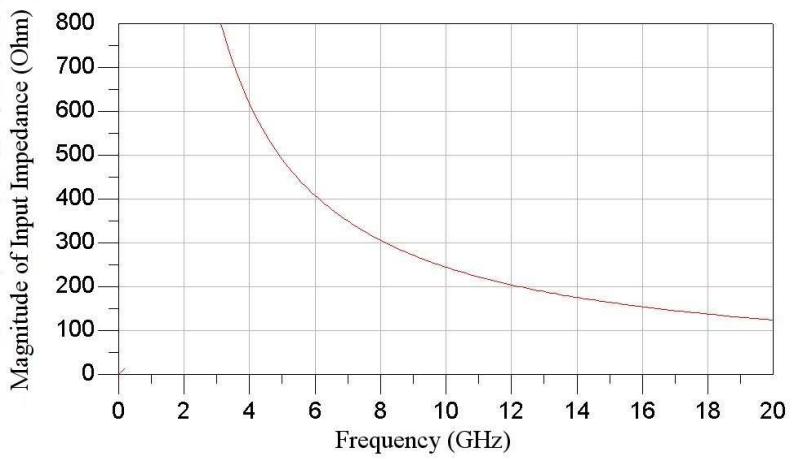

Figure 4.16 Loaded input impedance of the source-follower in the UWB frequency range of operation

In fact, since $Z_L \approx 50\Omega$ in the UWB band of operation, the input impedance as expressed in (4.28) looks like a simple capacitance. The input impedance of the source follower for frequencies in the UWB range is shown in Figure 4.16. Modeling the input source follower impedance with a simple capacitance reveals the $Z_{i\text{-}SF} \approx 65fF$. For both Figures 4.15 and 4.16, the source follower shown in Figure 4.10 with component values as indicated in Appendix A was simulated.

4.4 Differential Gain Stage

Feedback was utilized to desensitize gain from bias dependent parameters such as g_m [6]. This is very important for sensitive analog circuits, especially analog circuits that will reside in a mixed-signal environment. As mentioned before, in the mixed-signal environment the digital switching causes rapid variations in the power supply. The effect of these variations on analog bias networks is very difficult to minimize, and therefore the power supply variations significantly distort the sensitive analog circuitry,

even to the point of malfunction. Therefore, employing feedback in the core of the LNA (the differential pair) decreases the dependency of the differential pair gain upon g_m significantly increases the chances of the LNA performing properly in a SOC. As can be seen from (4.34), when Z_f becomes smaller, the differential-mode gain becomes less dependent on g_m as opposed to when $Z_f \rightarrow \infty$.

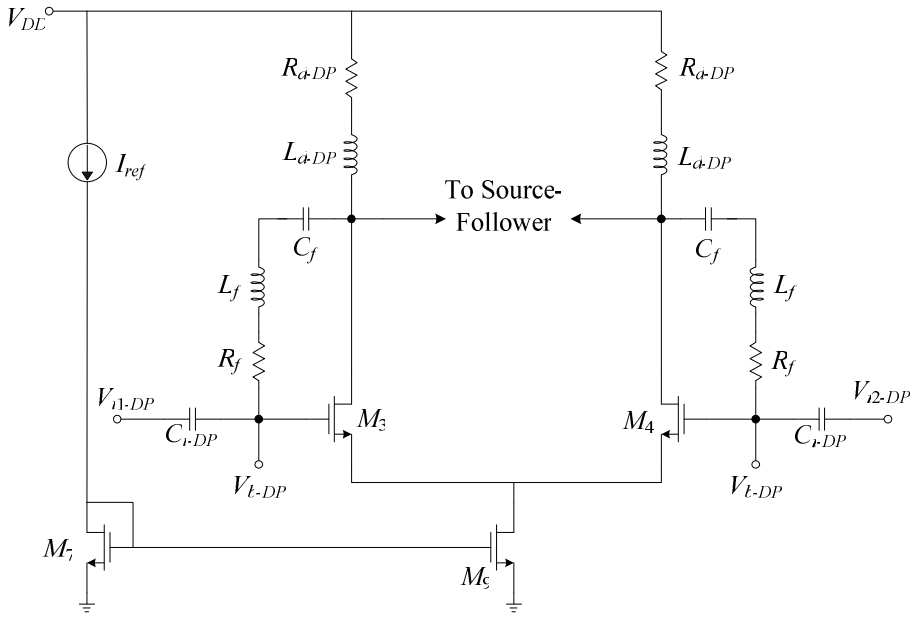

Figure 4.17 Differential Gain Stage

The differential-mode gain of the differential stage is shown in Figure 4.18 with the component values as shown in Appendix A. Notice how the gain of the differential core was not designed to be perfectly flat in the band of operation. This was done because of the difficulties associated with obtaining a smooth gain response in the common-gate stage. Therefore, the intentional design of non-flatness in the differential offsets the non-flatness seen in the gain of the common-gate stage.

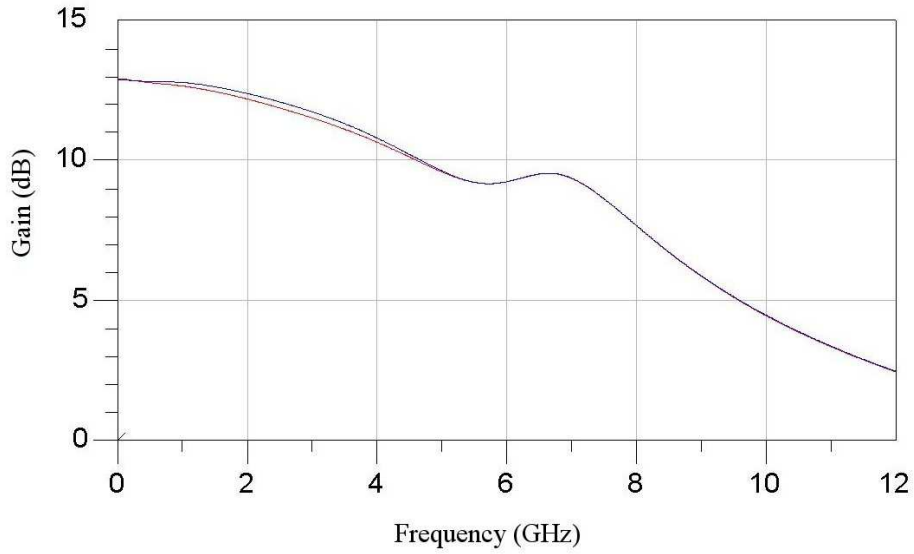

Figure 4.18 Loaded gain through differential core

4.4.1 Differential mode gain analysis

In order to perform the differential gain analysis of the differential pair, consider Figure 4.17. The differential mode half circuit is shown in Figure 4.19.

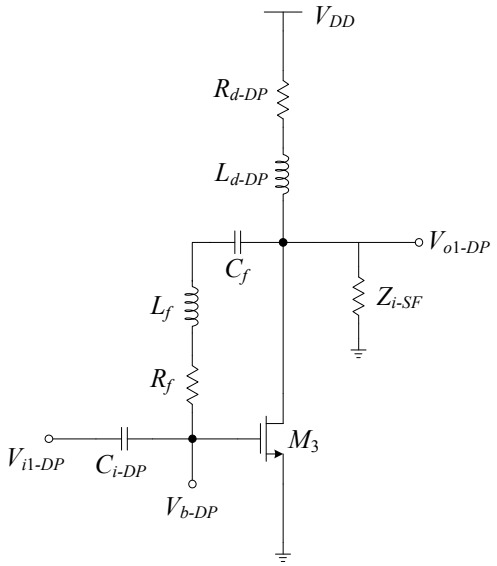

Figure 4.19 Differential-mode half circuit

The small-signal model of the differential mode half circuit is shown in Figure 4.20.

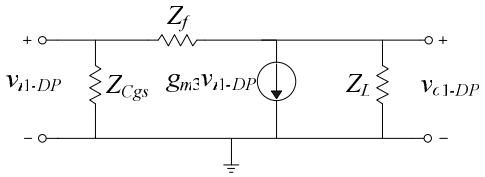

Figure 4.20 Small-signal model of the differential-mode half circuit

In the small-signal model of Figure 4.20,

$$Z_L = \left(R_{d-DP} + sL_{d-DP}\right)\left\|\left(Z_{i-SF}\right) \approx \left(R_{d-DP} + sL_{d-DP}\right)\right\|65\,fF \tag{4.29}$$

$$Z_f = R_f + sL_f + \frac{1}{sC_f} \tag{4.30}$$

$$Z_{Cgs} = \frac{1}{sC_{gs}} \tag{4.31}$$

The C_{gs} in (4.31) is the gate-source capacitance of transistor M_3.

Evaluating KCL at the output node of the small-signal model differential half-mode circuit gives,

$$\frac{v_{i1-DP} - v_{o1-DP}}{Z_f} - g_{m3}v_{i1-DP} - \frac{v_{o1-DP}}{\left(r_{o3}\left\|Z_L\right.\right)} = 0\,. \tag{4.32}$$

Re-arranging (4.32) we get,

$$v_{o1-DP}\left[\frac{1}{Z_f} + \frac{1}{r_{o3}\left\|Z_L\right.}\right] = v_{i1-DP}\left[\frac{1}{Z_f} - g_{m3}\right]. \tag{4.33}$$

Solving for small-signal differential mode voltage gain and re-arranging gives,

$$A_{v-DP} = \frac{v_{o1-DP}}{v_{i1-DP}} = \left[\frac{1 - g_{m3}Z_f}{Z_f}\right]\left(Z_f\left\|r_{o3}\right\|Z_L\right). \tag{4.34}$$

Notice from equation (4.34) that if $Z_f \rightarrow \infty$, then the output gain increases and approaches the small-signal voltage gain expression for a normal common-source stage with no feedback.

4.5 Overall System Simulations and Performance

4.5.1 Input and Output Matching

As seen in Figure 4.21, the input and output reflection coefficients (S_{11} and S_{22}) remain below -10*dB* in the band of 3-12GHz. Therefore, validating (4.6) and (4.21), and establishing a good method for wideband impedance matching. Also, from the Smith Chart plot in Figure 4.22, the complex input impedance of the common-gate stage and output impedance of the source-follower stage have capacitance components as accurately predicted by (4.6) and (4.21), respectively.

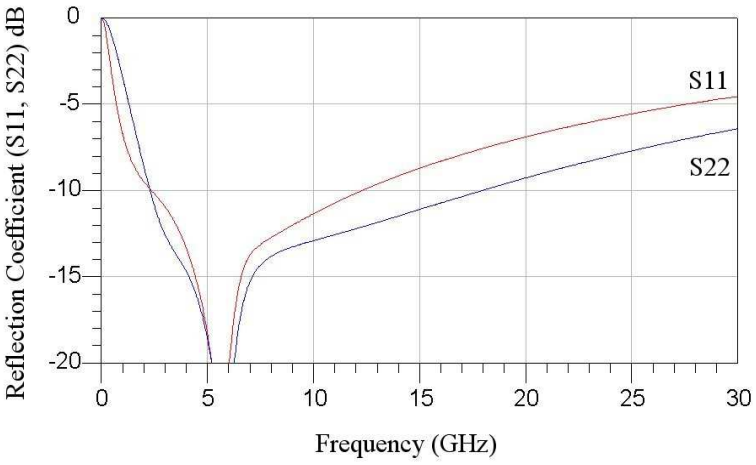

Figure 4.21 Input and output reflection coefficients (S_{11} and S_{22})

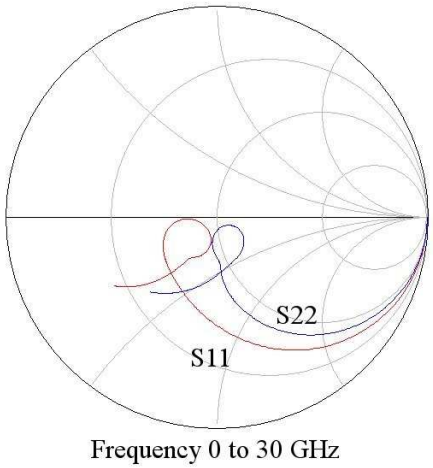

Figure 4.22 Smith Chart plot of input and output reflection coefficients

4.5.2 Gain

The complete LNA achieved a gain flatness of $\pm 0.2dB$ over the band from 3.1-6.2GHz. The overall gain of the LNA, including the -6*dB* attenuation from the source-follower stage, is 16.4*dB*. Figure 4.23 shows the gain versus frequency of the complete schematic shown in Figure 4.1 with the component values assuming those given in Appendix A.

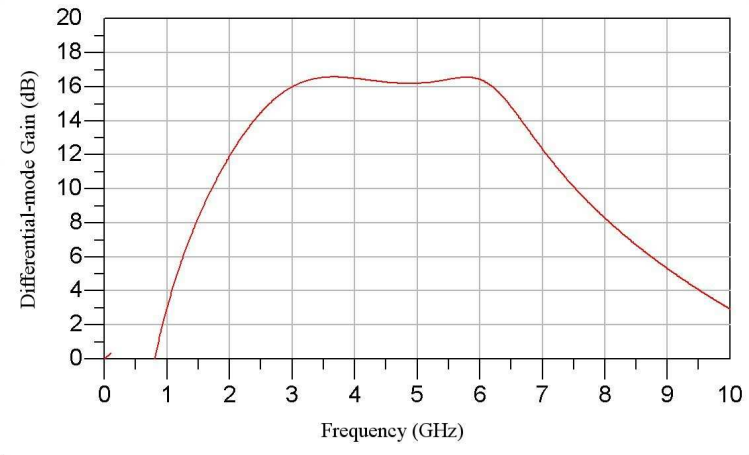

Figure 4.23 Differential-mode gain versus frequency

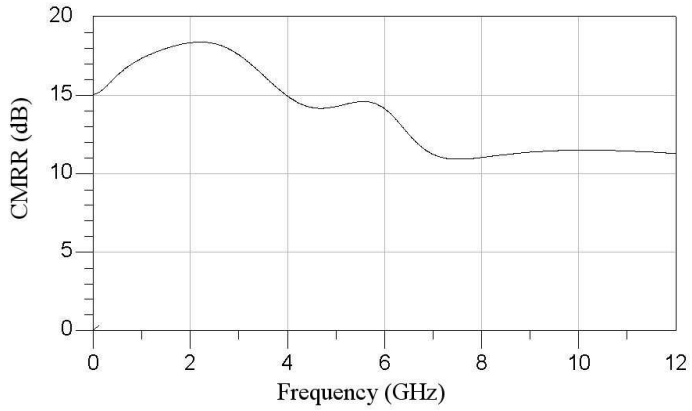

Figure 4.24 Common-mode rejection ratio

The common-mode rejection ratio (CMRR) is given by the following,

$$CMRR = \frac{A_{v-differential-\mathrm{mode}}}{A_{v-common-\mathrm{mode}}}. \tag{4.35}$$

The simulated CMRR is shown in Figure 4.24. From Figure 4.24, it can be seen that common-mode signals, such as voltage supply variations caused by switching of nearby digital signals, will be attenuated by approximately 14*dB* with reference to the desired differential-mode signals. In mixed-signals environments, the 14*dB* attenuation of common-mode signals can dramatically increase the performance of the LNA when compared to single ended counterparts such as [1, 2, 3, 4, 5, 19, 20, 21].

4.5.3 Noise Figure

Not including any losses associated with a pre-select filter, the budget link in the MB-OFDM proposal for IEEE 802.15.3a standard [22] specifies that an overall noise figure for the RF receiver chain should be less than 4.9*dB*. Therefore, since an adequate gain of 16.4*dB* was achieved, a noise figure for the LNA of less than 4*dB* should be adequate as well. For example, consider a subsequent stage after the LNA

with a noise figure of 10*dB*. Using equation (2.18), the cumulative noise figure and the input of this LNA would be approximately 4.3*dB*, which is still less than the needed 4.9*dB*.

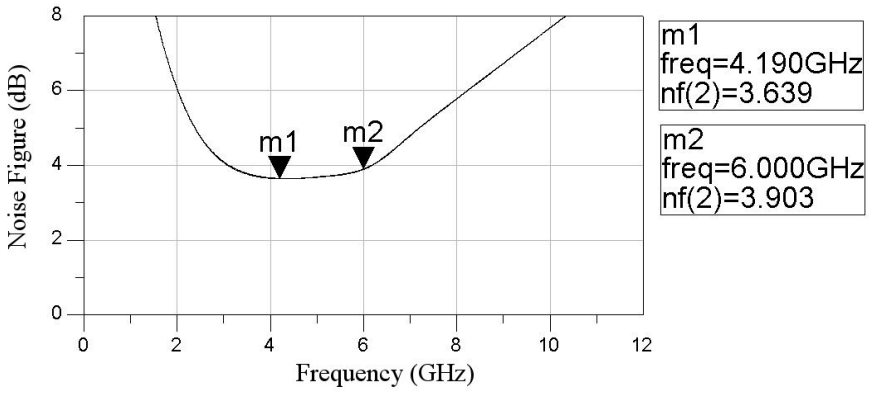

Figure 4.25 Single-ended noise figure

As can be seen from Figure 4.25, the noise figure varies from 3.64–3.9*dB* over 3–6GHz. The noise figure simulated is the single-ended noise figure and no differential-mode noise theory was employed such as in [23]. Therefore, the actual differential-mode noise figure is expected to be slightly better than that shown in Figure 4.25.

4.5.4 Stability

The differential-mode parameters were used in conjunction with equation (2.23), for simulating the stability factor, *k*. Figure shows the simulated k versus frequency. After the S-Parameter simulation, *k* was determined using the following equation,

$$k = \frac{1-\left|S_{d2d1}\right|^2-\left|S_{d2d2}\right|^2+\left|S_{d1d1}S_{d2d2}-S_{d1d2}S_{d2d1}\right|^2}{2\left|S_{d1d2}\right|\left|S_{d2d1}\right|}. \qquad (4.36)$$

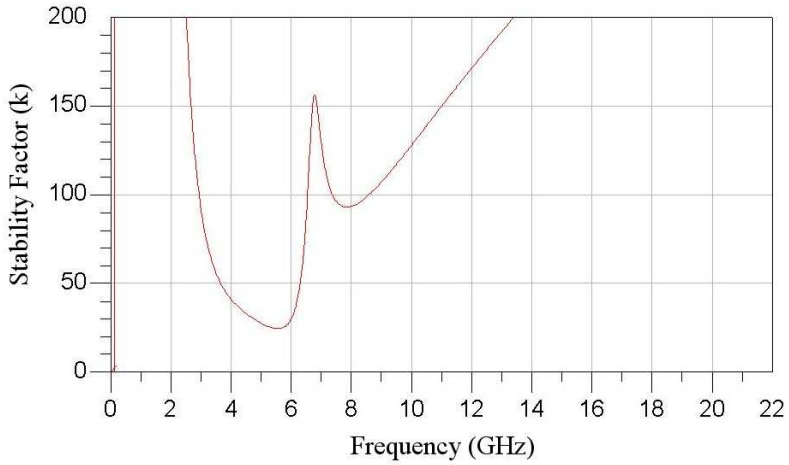

Figure 4.26 Stability Factor (*k*)

As can be seen from Figure 4.26, the stability factor of the LNA is greater than unity. Therefore the feedback in the differential core did not cause instability.

4.5.5 Reverse Isolation

Reverse Isolation (S_{d1d2}) should be well below -20*dB* so that unwanted signal transfer from the subsequent stage back through the LNA does not occur. Unwanted signals propagating back through the LNA could cause significant distortion. As shown in Figure 4.27, the differential-mode reverse isolation obtained was less than -50*dB* across the entire band of operation. This low reverse isolation was realized because the active output matching stage (source-follower) does not easily allow signals to propagate from the source terminal of the transistor to the gate terminal.

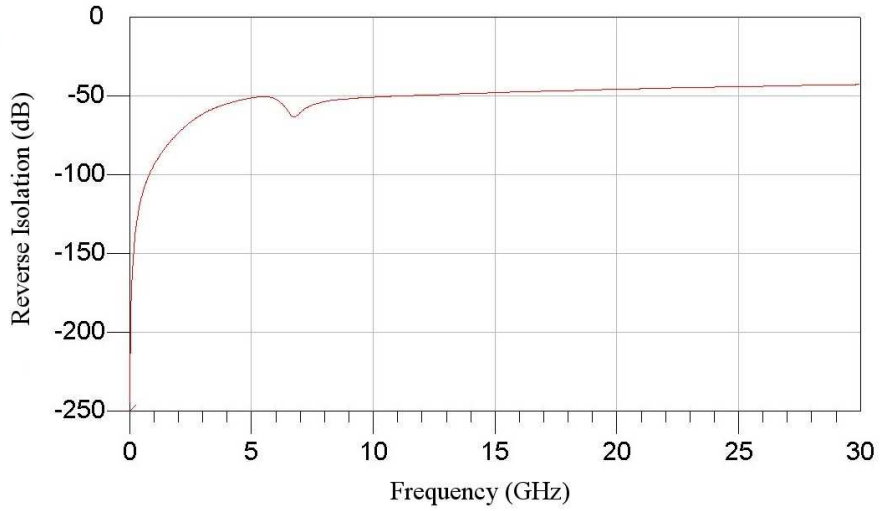

Figure 4.27 Reverse Isolation (S_{d1d2})

4.5.6 Linearity

As mentioned in section 2.2.8, the 1*dBc* referred to the input must be at least greater than -41.3dBm to successfully handle UWB signals without significant distortion. As can be seen from Figure 4.28, the LNA achieved a 1*dBc* of -24*dBm*. This is sufficient for an UWB LNA. Also, for the reasons discussed in section 2.2.8, 3rd order intercept point was not simulated.

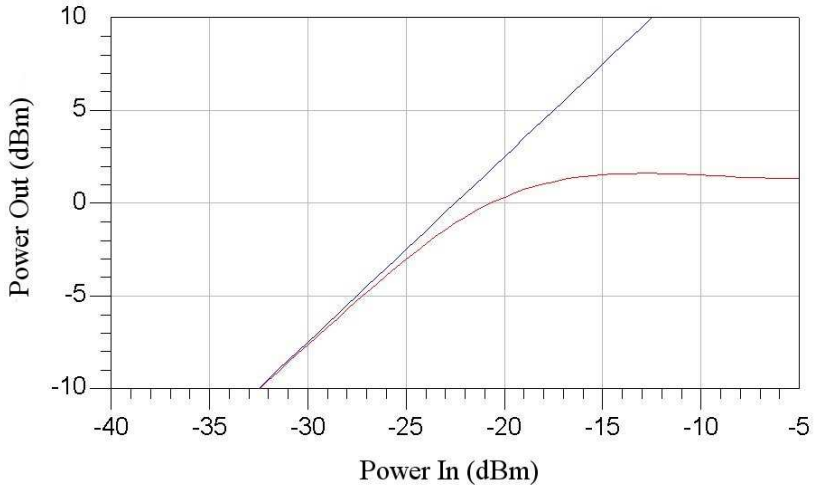

Figure 4.28 Input power sweep illustrating 1*dBc*

4.6 Performance Comparison with Recent UWB Low noise Amplifiers

The performance of the LNA designed in this thesis falls just about in the middle of the pack when compared to the most recently published CMOS UWB LNAs. However, as discussed before, several design considerations were made to make this LNA more suitable for a mixed-signal environment or SOC (e.g. Active matching and a differential architecture). The LNA designed in this thesis is, to the author's knowledge, the only differential UWB LNA capable of 3-6GHz operation (lower UWB band, see section 2.1.6). Also, the LNA in [5], employs active input matching.

The power consumption values given in Table 4.1 for the LNAs in [1], [3], and [20] do not include the power consumption of an output buffer stage that will be necessary for proper operation of these LNAs. Therefore, when listing this thesis's LNA, the output buffer stage (source-follower) power consumption was ignored for an

accurate comparison. The LNA in this thesis consumed 18mW power without the source-follower and 28.3mW including it. The other LNAs listed in Table 4.1 do not require and output buffer stage.

Table 4.1 Performance comparison with recent UWB low noise amplifiers

Ref.	Tech. (CMOS)	BW (GHz)	Gain (dB)	Power (mW)	Max. NF (dB)	Min. NF (dB)
[1]	0.18 um	2.3 – 9.2	9.3	9.0	9.0	4.0
[2]	0.18 um	3.0 – 7.0	15.3	21.0	1.9	1.4
[3]	0.18 um	2.0 – 4.6	9.8	16.2	5.2	2.3
[4]	0.18 um	3.0 – 6.0	24.0	51.0	2.9	2.7
[5]	0.18 um	3.1 – 4.8	16.5	21.0	4.3	4.0
[19]	0.18 um	3.0 – 6.0	16.0	59.4	6.7	4.7
[20]	0.18 um	2.0 – 9.0	13.5	25.2	7.4	2.6
[21]	0.13 um	2.0 – 5.2	16.0	38.0	5.7	4.7
This Thesis	0.18 um	3.0 – 6.2	16.4	18.0	3.9	3.7

The noise figures listed in Table 4.1 for the LNAs in [1], [3], [19], [20], and [21] are actual measured values from the fabricated circuit. The others, including this work, are simulated values.

As seen by equation (2.18), gain and noise figure of the LNA are the two most important parameters affecting the overall noise figure and consequently sensitivity of the analog-front end. Therefore, Figure 4.29 plots the gain/noise figure space of the LNAs compared in Table 4.1. Figure 4.29 gives a graphical illustration of how this LNA compares in terms of important performance parameters. Caution should be used when comparing measured data with simulated results since the simulations are only best estimates. Nonetheless, Figure 4.29 gives an approximate overview how the LNA designed in this thesis should perform in comparison to others. Also, keep in mind that Figure 4.29 does not highlight the advantage of a differential architecture or active

matching when compared to the other LNAs, but merely shows that the LNA designed herein adequately performs.

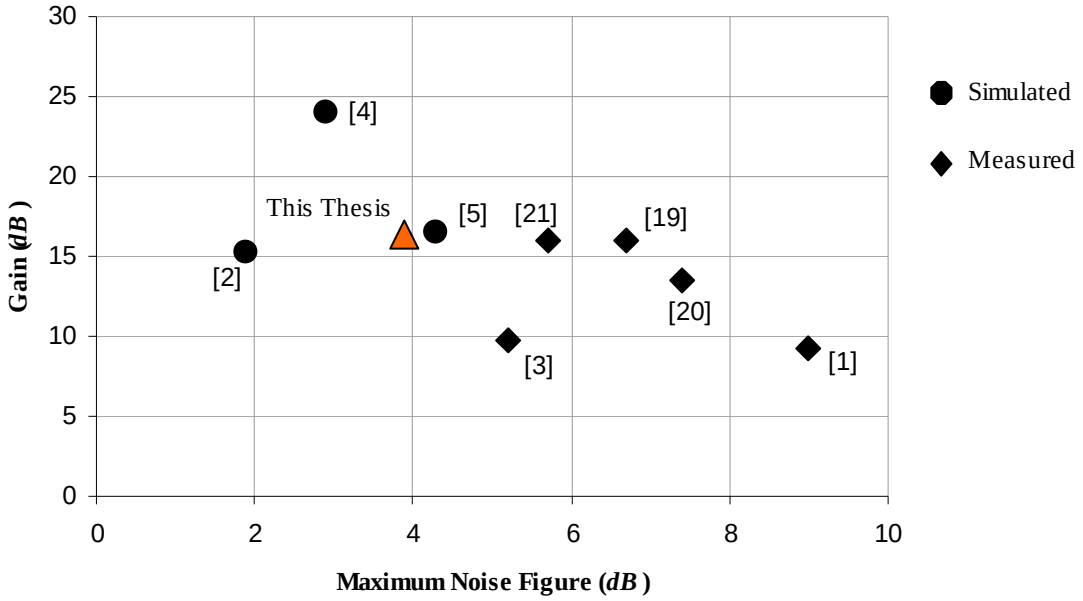

Figure 4.29 Graphical illustration comparing recently published LNAs and this work

CHAPTER 5

CONCLUSION

In this thesis a differential low noise amplifier with active matching was designed and simulated using the TSMC 0.18μm CMOS technology. As seen in Figure 4.29, the performance of this thesis' LNA is comparable to those who have gone before it. However, because of the differential architecture, this LNA will perform much better in a mixed-signal environment, such as a SOC implementation of a UWB communication or RADAR system. One of the major drawbacks associated with the differential architecture is that it consumes very valuable real-estate. To combat this drawback, active impedance matching networks were used to realize a smaller overall amplifier size. This proved successful, with the additional active components not significantly degrading the noise figure. The final simulations reveal a noise figure ranging from 3.6-3.9*dB*. The amplifier operates over 3.1-6.2GHz with a flat gain of 16.4*dB* and a ±0.2*dB* ripple. The LNA presented herein can work adequately in the lower band of the divided UWB spectrum.

The method of using active matching networks, however, proved to work excellent over an ultra-wideband while still providing a reasonable noise figure for a UWB amplifier. Viewing just the single-ended parameters, S_{11} was kept below -10*dBm* over 3-12GHz and S_{22} was kept below -10*dBm* over 3-17GHz.

For future work, an LNA that was designed to operate over the entire UWB spectrum is desirable. And the method and philosophy of using active matching proved

to be a very successful method for realizing excellent impedance matches over that bandwidth. However, the real limiting factor from preventing the LNA designed herein reaching a bandwidth of the entire UWB spectrum was the parasitic capacitances associated with the spiral inductors. Since relatively large inductance values were needed (7.5*nH*), the Cox in Figure 4.2 relegated the entire inductor useless above about 6GHz. It appears as if gain is significantly sacrificed by using much smaller loading inductors and a much smaller feedback inductor (less than 3*nH*), then the architecture presented herein might have sufficient bandwidth.

APPENDIX A

COMPONENT VALUES

The table in appendix A contains a list of all of the values of the components shown in Figure 4.1. The component values included in this table are the exact values that obtained the simulation results shown in this thesis. Note that the CMOS technology used was TSMC 0.18μm. Therefore, the dimension listed in this table for the transistors is the width of the transistor and the lengths are fixed at 0.18μm. Also, as mentioned before, the TSMC 0.18μm inductors are far from ideal. Therefore, the inductance listed in this table represents the inductance value attempted to be realized by the spiral inductors offered by the TSMC 0.18μm technology.

Table A.1 Tabularized list of component values

Component Name	Schematic Value
M_1	100 μm
M_2	100 μm
M_3	50 μm
M_4	50 μm
M_5	65 μm
M_6	65 μm
M_7	40 μm
M_8	30 μm
M_9	60 μm
M_{10}	30 μm
$C_{i\text{-}CG}$	4.5 pF
$C_{i\text{-}DP}$	0.99 pF
$C_{o\text{-}SF}$	1.98 pF
C_f	110 fF
$L_{d\text{-}CG}$	6.5 nH
L_f	7.5 nH
$L_{d\text{-}DP}$	5 nH
$R_{b\text{-}CG}$	300 Ω
$R_{d\text{-}CG}$	30 Ω
R_f	900 Ω
$R_{d\text{-}DP}$	280 Ω

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BIOGRAPHICAL INFORMATION

Timothy Bryan Merkin was born on April 6, 1981 in San Antonio, Texas. He graduated from Texas A&M University-Kingsville Summa Cum Laude with a Bachelor of Science in Electrical Engineering in the fall of 2003. During his undergraduate program, he held elected positions of president of Tau Beta Pi (TBP) national engineering honor society and recording secretary of Etta Kappa Nu (HKN) national electrical engineering honor society. Also during his undergraduate career, he was appointed by the chairman of the electrical engineering department at (TAMUK) to a student advisory board serving the curriculum committee of the department. He also competed on the rodeo team while at TAMUK for three years and qualified in the bull riding for the National Intercollegiate Rodeo Association (NIRA) play-off rodeo between the Grand Canyon, Southwest, and Southern regions for two years in a row. He enrolled in the Masters of Science program in the Electrical Engineering department at the University of Texas at Arlington in the fall of 2004.