

ANALYSIS AND CHARACTERIZATION OF THERMAL EFFECTS IN
ANALOG CIRCUITS

by

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DEDICATED TO MY FAMILY

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ABSTRACT

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Dielectrically Isolated Bipolar Junction Transistors (DIBJTs) are used in industry for high speed and high power applications. These devices suffer from thermal heating and are subjected to change in their characteristics. This thesis explores the thermal effects involving the self heating and inter-device heating (thermal coupling) at the device as well as at the circuit level.

Systematic analysis of individual device heating characteristics in a particular Current feedback operational amplifier (CFOA) design is carried out, using the VBIC (Vertical Bipolar Inter-company) model in the the Cadence SpectreS simulator. A diagnostic and design procedure is established for circuit designers to determine the possible causes of the thermal tail and to eliminate the problem. To consider the inter-

device heating effects, a BJT symbol including adjacent device heating in the VBIC model is developed at the schematic capture level.

Different test structures are developed, and fabricated using National Semiconductor process to study dependence of inter-device heating of DIBJTs on various layout factors. An innovative method for the inter-device heating measurement is developed using IC-CAP / HPIB interfaced evaluation system.

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CHAPTER 1

INTRODUCTION

Extensive research has been done to study the self heating of BJTs (Bipolar Junction Transistors). Positive feedback between collector current, I_c and the base emitter voltage (V_{be}), in BJT results in the dissipation of power. This is the self heating of the BJT. If this thermal feedback is ignored, it can cause increase in the self heating of the transistor and the device can burn out. The dependence of the self-heating effect of the BJT on the base-emitter voltage and collector current has been developed [1]. Self heating of the BJT increases the temperature of the device above the ambient temperature. In the case of integrated circuits this localized power dissipation within different devices can cause chip temperature gradients and variations which strongly affect the performance of the overall circuit. The deviation in performance from the ideal case is important; particularly in cases where very high accuracy is required or where large power dissipation occurs on the chip. The effect of thermal feedback on various integrated circuits like operational amplifiers, voltage regulators and voltage references has been proved by Fukahori and Gray [2]

With the invention of advanced process technologies the device size is being scaled down and density of transistors on a given chip area is increasing rapidly. The thermal runaway issue becomes more important and complex as the density of the

devices on a chip and the operational speed of the ICs increase. In analog circuits the heat dissipation is continuous and operating characteristics of the devices are sensitive to temperature changes. Hence more accurate thermal analysis is required to study the thermal feedback phenomenon at the device level as well as at the circuit level.

With scaling of transistor geometries the current densities and thermal spreading resistance increase. As the density of the devices on a chip increases another thermal issue called ‘inter-device thermal coupling’ comes into the picture. For devices with high power densities and small separation distances, there can be a direct coupling between temperature rise in these devices and the temperature of neighboring devices. Thus the device with high power density heats up neighboring device in addition to its own self heating. This thermal coupling or inter-device heating depends on layout as well as operating conditions of the power device and the adjacent device. These factors do vary on a larger scale in circuits containing a large number of devices and can affect the performance of the overall circuit. Fukahori and Gray [2] showed that thermal coupling can profoundly affect the gain characteristics of an operational amplifier.

The temperature rise in a chip is basically because of the three different heat transfer mechanisms; a) Chip to package and package to an ambient thermal impedance b) Self heating in a device due to power dissipation and c) Thermal coupling between the neighboring devices. As mentioned previously the last two effects have greater impact on analog circuits and are the concentration of this thesis work. Thus, to model the thermal effects in analog circuits, it is necessary to study thermal modeling of discrete devices as well as IC chips. In addition to this it is necessary to model the

thermal coupling or inter-device heating phenomenon and implement the improved thermal model at the device level to include the self heating as well as the inter-device heating effects.

One way to consider the thermal effect of BJTs in analog circuits is to use simulators which provide access to model equations and modify the model equations [3, 4]. But in this approach it is necessary to change the model equations each time the layout and operating conditions of the devices change. It becomes tedious for circuits containing a large number of devices. Another approach to consider thermal effects is to use a coupled electro-thermal simulation [5]. This approach needs a large amount of change in source code of simulator or entirely new simulator design to solve the three dimensional heat equations.

Advanced process technologies have made it easier to fabricate a transistor using a trench isolation technique. Trench isolation is used to form isolation regions suitable for very fine features. In this isolation technique a very narrow and relatively deep trench is etched around the device to be isolated. The trench is filled with an insulating material like SiO_2 . Thus the device is surrounded on five sides by SiO_2 , which is a poor conductor of heat. Since the maximum heat flow occurs only through the interconnecting conductors, and the five sides offer high resistance to heat flow, these devices are affected the most from thermal heating. Hence these devices are used for studying the thermal effects.

National Semiconductor Corporation has developed a dielectrically isolated complementary bipolar process, VIP10. It is one of the members of National's VIP

(Vertically Integrated PNP) family of complementary bipolar processes. This VIP10 process is used for design of high speed, high performance analog circuits. Transistors in this process are used to design High-frequency Operational Amplifiers [6]. The schematic cross-section of a dielectrically isolated BJT (DIBJT) is shown in Figure 1.1. As seen from the cross-section, the insulating oxide, SiO_2 in this case, surrounds the transistor and restricts the heat flow in all directions except the top surface. Because of the thermal isolation it is necessary to study the thermal behavior of these particular transistors. It is also necessary to study the impact of thermal characteristics on the performance of circuits containing these devices.

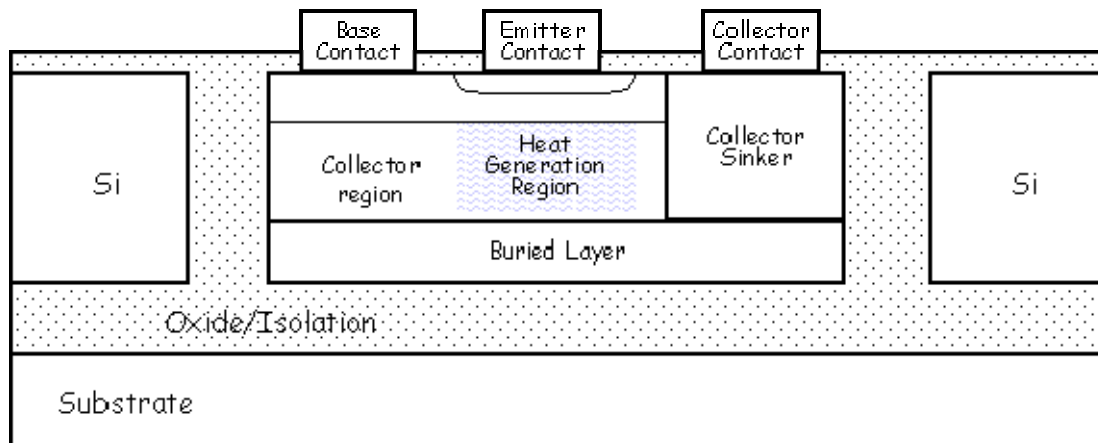


Figure 1.1 Schematic cross-section of a DIBJT [Dielectrically Isolated Bipolar Junction Transistor]. The Emitter, Base and Collector (including sinker and buried layer) regions are isolated within the dielectric (SiO_2) box. For forward-active operation, the heat generation region is primarily confined to the portion of the collector-base depletion region under the emitter [6]

The thermal analysis of DIBJT devices (using VIP10 process) and their impact on the performance variation of circuits like the Current Feedback Operational

Amplifier (CFOA) containing these devices is the main focus of this thesis work. Various methods have been developed to characterize and measure the thermal resistance of the DIBJTs using VIP10 process [7]. This thesis is the continuation of the research work in the same area. Here the thermal effects have been considered at circuit level to find the main factors affecting the inter-device heating. Test structures are developed to study the effect of these factors at the device level. An innovative measurement technique is developed to measure the device temperature using IC-CAP / HP1B evaluation system. The inter-device heating effect has been studied for various layout and operating conditions of the device. Thermal analysis has been carried out to study the effect of change in circuit temperature as well as device temperature on gain-error and input offset voltage for the current feedback operational amplifier (CFOA). Profound study of these specifications of CFOA has been done to propose a possible relation between device level and circuit level thermal effects.

The VBIC model for the BJT is an improvement over the Gummel-Poon model since the VBIC model considers the thermal effects more accurately. Self heating effects are well simulated using the existing VBIC model, and it is used for simulation purposes in this work. Also attempts have been made to modify the VBIC model externally to consider the inter-device heating phenomenon.

CHAPTER 2

DIELECTRICALLY ISOLATED BIPOLAR JUNCTION TRANSISTOR (DIBJT)

Dielectrically Isolated Bipolar Junction Transistors (DIBJTs) developed by National Semiconductor Corporation using the VIP10 process are used for the thermal study. Thermal properties of a device depend on its geometry and boundary conditions. It is necessary to develop accurate techniques to characterize the thermal resistance depending on the geometry of the device. Hence it is essential to study the structure of the DIBJT. This chapter describes the structure of a DIBJT, various thermal definitions and the five element resistance model developed from the geometry consideration of these particular DIBJTs.

2.1 Structure of DIBJT

Simplified schematic cross section of a Dielectrically Isolated Bipolar Junction Transistor is shown in figure 2.1. The National Semiconductor VIP10 process is a complementary bipolar process implementing NPN and PNP BJTs. VIP10 transistor cross section is shown in fig.2.2.

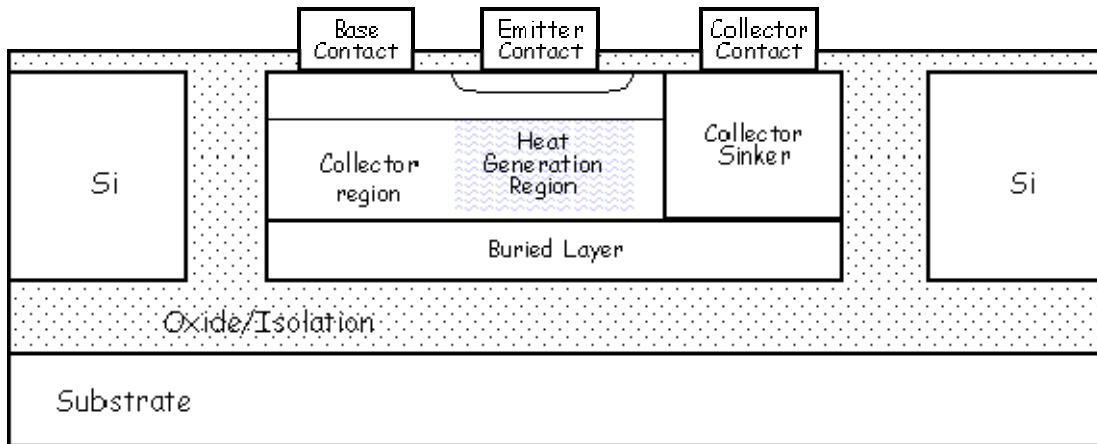


Figure 2.1 Schematic cross-section of a DIBJT [Dielectrically Isolated Bipolar Junction Transistor]. The Emitter, Base and Collector (including sinker and buried layer) regions are isolated within the dielectric (SiO_2) box. For forward-active operation, the heat generation region is primarily confined to the portion of the collector-base depletion region under the emitter [6]

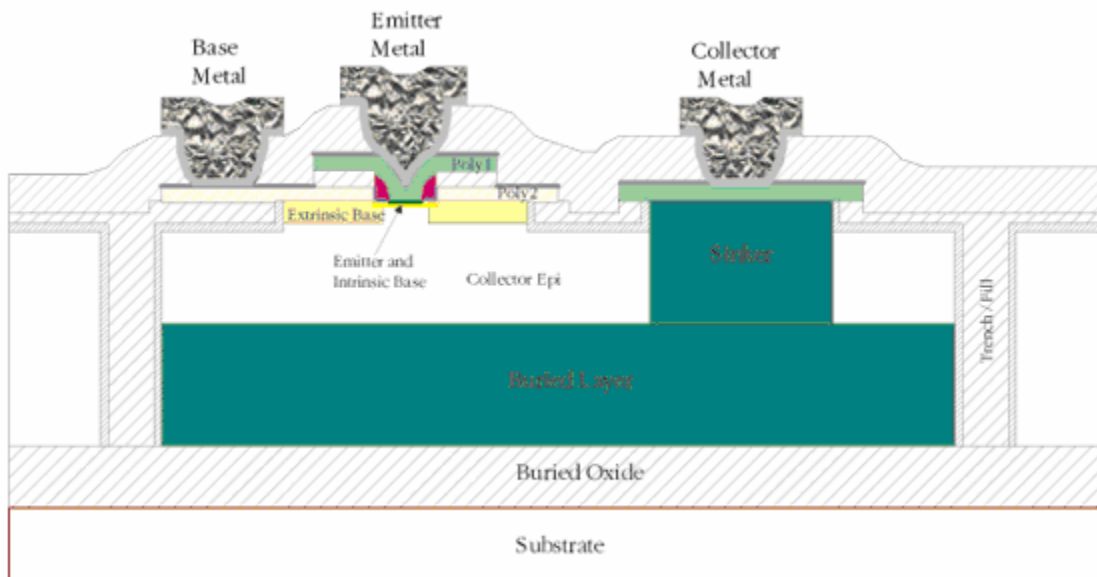


Figure 2.2 VIP10 Transistor Cross-section [8]

The active area is Silicon-On-Insulator (SOI) which is fabricated using the bonded wafer technique. This produces a buried oxide layer which isolates the bottom

of the epitaxial tubs, which are usually the collectors of bipolar transistors. P and N type buried layers are followed by epitaxial growth. Trenches are anisotropically etched into the silicon and filled to form the isolation sidewalls. Consequently the VIP10 transistor collectors are fully dielectrically isolated (DI) and have no P-N junction between the collectors and substrate or well. This reduces the parasitic collector-substrate capacitance [8]. The main transistor parameters for these DIBJTs using the VIP10 process are listed in table 2.1.

Table 2.1 VIP10 transistor parameters [8]

NPN f_t	9 GHz
PNP f_t	8GHz
NPN β	100
PNP β	50
NPN V_a	120
PNP V_a	40
C_{js}	0.005 pF
Emitter Width	1 μ m
Maximum Supply Voltage	12 V

Complementary DIBJTs using the VIP10 process has the following advantages over other existing BJT processes [8]:

1. The collector-substrate capacitance in a DIBJT is less than that in a junction isolated BJT and hence has an increased amplifier frequency response.

2. The presence of oxide isolation obviates leakage currents otherwise found in junction isolated (JI) transistors.
3. The trench isolation eliminates large sidewall base collector junction capacitance.
4. The DIBJTs drastically reduces the area required for isolation.
5. The complementary process enables class AB output stages with very low quiescent current and high output drive in analog circuits.
6. The DIBJTs offers low collector resistance and reduced quasi-saturation effects.
7. Unlike MOSFET devices, DIBJTs combine low distortion, low power dissipation and frequency stability.

Because of the above listed advantages, designs using complementary bipolar transistors, offer the best combination of features required in high speed amplifiers: wide bandwidth, low power consumption, low supply voltages, large output swing, high output current and low distortion.

But the main drawback of the DIBJTs in this process is that they suffer from thermal issues since the trenches surrounding the device are filled with SiO_2 which is a poor conductor of heat. Hence it is necessary to consider the different thermal effects affecting the performance of these particular transistors. Also it is essential to model and characterize the effect of thermal properties on the overall performance of designs using these devices. The basic thermal definitions and the analogy between thermal and electrical networks are discussed in the next section.

2.2 Thermal Definitions

Self heating is the main cause for the heating of the BJT. Thermal coupling or inter-device heating also plays an important role in high density ICs.

2.2.1 Self Heating:

Self heating is defined as the rise in the junction temperature of an emitter, which is caused by the transistor's own power dissipation. The heat generated elevates the temperature within the structure apart from the heating caused by the ambient temperature.

2.2.2 Thermal Coupling or Inter-device Heating:

Inter-device heating is defined as the increase in the temperature of the device caused by power dissipation in neighboring devices. Among all other factors, the inter-device heating depends most on the number of neighboring devices, spacing between the devices and the power dissipation of the adjacent devices.

Heat generation and dissipation in a transistor depends upon two main parameters: a) The resistance of the material to heat flow and b) the amount of heat stored in the material. These are the two main parameters which should be characterized accurately.

2.2.3 Thermal Resistance:

Thermal resistance is defined as the difference in temperature between two closed isothermal surfaces divided by the total heat flow between them.

Mathematically thermal resistance for a device can be expressed as

$$R_{th} = \frac{T_j - T_a}{P} \quad (2.1)$$

Where,

T_j is the junction temperature

T_a is the ambient temperature and

P is total heat flow rate.

R_{th} is expressed in units of °K / Watt.

A complete heat flux network is necessary to study the three dimensional conduction of heat from a device's hot core to its outer surface. The heat flux network depends on the geometry of the body. Thermal resistance is specific to the heat flux network. Hence any change in the geometry of the device changes its thermal resistance. Electro-thermal simulations for the DIBJTs using the VIP10 process have been carried out to characterize the thermal resistance of these devices [9].

2.2.4 Thermal resistivity:

Thermal resistivity is defined as the ratio of the thermal gradient to the heat flux density for one dimensional heat conduction. It is the property of the material indicating the resistance of the material to thermal conduction. It has units of $\text{KW}^{-1}\text{cm}^{-1}$ and mathematically it can be expressed as

$$r = \frac{\frac{T_1 - T_2}{x}}{q} \quad (2.2)$$

where,

T_1 and T_2 are the temperatures of the two isothermal surfaces,

x is thickness of the material separating the two isotherms, and

q is the heat flux per unit area.

2.2.5 Thermal Capacitance:

Thermal capacitance, C_{th} , is a measure of how much heat energy can be stored and dissipated in a device. It is expressed in the units of J/K and in rectangular structure given as

$$C_{th} = \rho_s \times C_s \times w \times l \times d \quad (2.3)$$

Where,

ρ_s is specific weight of the substance (kg/m^3),

C_s is specific heat capacity of the substance ($\text{Jkg}^{-1}\text{K}^{-1}$), and

w, l and d are width, length and thickness of the substance respectively in m.

2.3 Thermal and Electrical analogy

From the above discussed thermal definitions, it is clear that the temperature rise ΔT [$^{\circ}\text{K}$], is given by the product of the power dissipated, P [W] and the thermal impedance, Z_{th} [$^{\circ}\text{K} / \text{W}$] as

$$\Delta T = Z_{th} * P \quad (2.4)$$

In the VBIC model thermal effects are modeled by implementing an additional thermal network as shown in fig 2.3. This thermal network models the interaction between electrical characteristics and thermal effects.

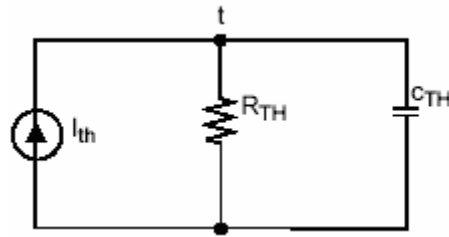


Figure 2.3 Additional Thermal Network in VBIC Model [10]

The above thermal sub-circuit with $I_{th} = P * 1 \text{ A/W}$ and $Z_{th} = Z_{th} * 1 \text{ Ohm W/}^\circ\text{K}$ couples the instantaneous power dissipation in the device to the thermal network. Thus from equation (2.4) the voltage level of the temperature node t (called the dt node in the VBIC syntax) is numerically equal to the local temperature rise $^\circ\text{K}$, which is used to calculate the instantaneous electrical characteristics of the BJT. The voltage at the temperature node can be written as

$$V_t = R_{th} * I \tag{2.5}$$

$$R_{th} = R_{th} * 1 \text{ Ohm W/}^\circ\text{K}$$

Comparing equations (2.4) and (2.5), it is clear that the temperature rise in the thermal network is equivalent to the voltage rise in electrical networks. Similarly the heat flow, thermal resistance and thermal capacitance have their equivalent terms in an electrical network. Table 2.2 summarizes this analogy between thermal and electrical networks.

Table 2.2 Thermal-Electrical Analogy

Thermal		Electrical	
Temperature	T in °K	Voltage	U in V
Heat flow	P in W	Current	I in A
Thermal resistance	R_{th} in °k/W	Resistance	R in V/A
Thermal capacitance	C_{th} in J/K	Capacitance	C in Coul / V

2.4 Five Element Thermal Resistance (R_{th}) Model for DIBJT

The total thermal resistance of the DIBJT shown in fig. 2.1 can be represented by a thermal network of five resistances as shown in fig.2.4. Each of these five resistances represent the thermal resistance of the particular part of the device and depends upon the geometry and the material in that region. Extensive analysis of different parts of this particular DIBJT has been carried out resulting in exact modeling of the thermal resistances and development of the five element resistance model as shown in fig2.4. This five element thermal resistance (R_{th}) model has been used as a basis for the research work in this thesis.

The overall thermal model with the inclusion of thermal resistance due to interconnects is shown in fig.2.5. This thermal model undergoes some changes while considering the inter-device heating. The following sections describe the changes in this model to accommodate the thermal coupling or inter-device heating.

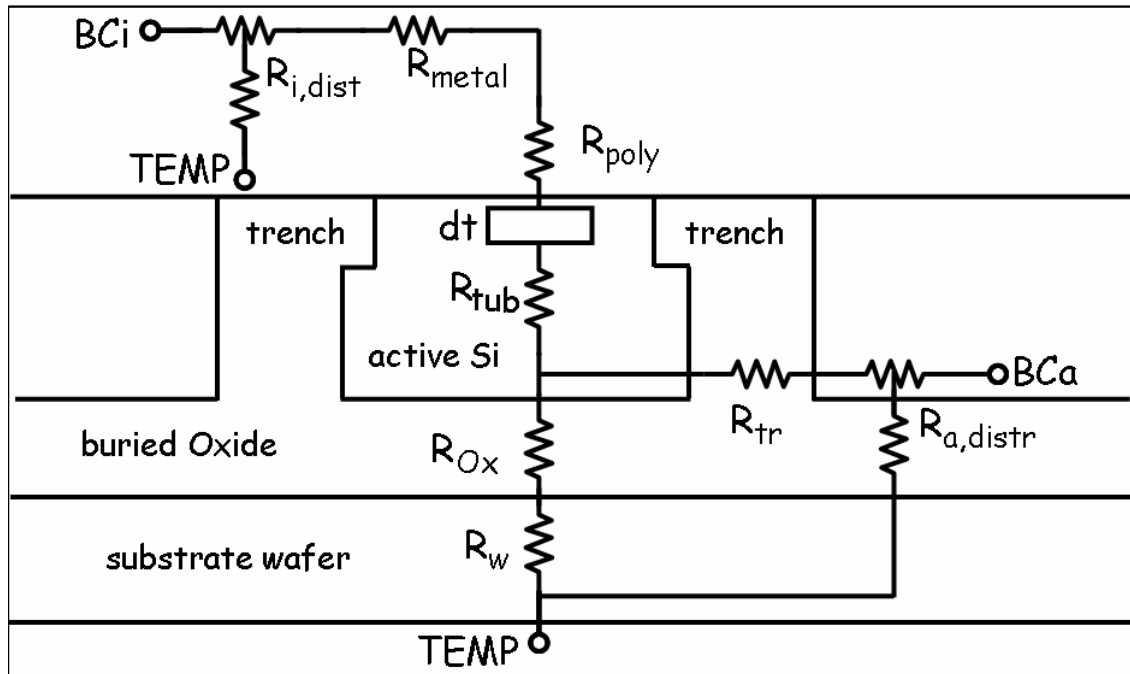


Figure.2.5 Overall Thermal Resistance (R_{th}) model for DIBJT [6]

2.5 Thermal model for inter-device heating or thermal coupling for DIBJT

The thermal network shown in fig2.5 can be used to model the self heating effect in a DIBJT. To accommodate change in thermal resistance due to thermal coupling or inter-device heating, this thermal network needs to be modified. As can be seen from figure 2.4, in case of thermal coupling, the wafer resistance R_w , oxide resistance R_{ox} and tub resistance R_{tub} , will still remain the same. The perimeter resistance R_{per} and distributed resistance R_{dist} are the resistances which need to be

modeled again. The values of these resistances depend upon various factors like the number of adjacent devices, amount of epitaxial coverage with trenches etc. Also it is essential to add the thermal resistance networks due to the shared interconnect and spacing between the adjacent devices. Device spacing, number of devices, shared interconnect etc. are not constant, but do vary with different designs and layout schemes. Hence it is necessary to model these resistances accurately. Fig.2.6 demonstrates the thermal network for two adjacent devices.

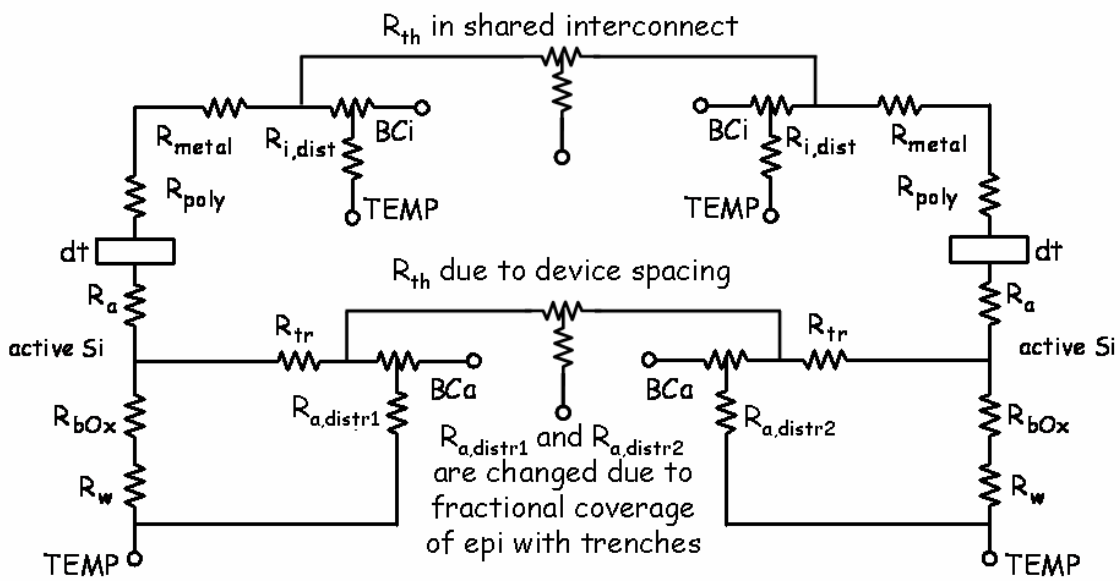


Figure 2.6 Modeling of Thermal Coupling between Two Adjacent Devices [6]

2.6 Voltage controlled voltage source (VCVS) representation for inter-device heating or thermal coupling

As mentioned in section 2.2 the VBIC model uses the thermal network shown in fig.2.3 to model the thermal effects due to self heating. The voltage at the 't' node in fig.2.3 represents the temperature increase above ambient temperature. It is commonly referred as 'dt' node in Spectre simulator. This is explained in detail in chapter 3. To account for the additional rise in temperature due to thermal coupling, it is necessary to modify thermal network at the circuit level. This effect can be modeled by using a modified thermal network at the 'dt' node and voltage controlled voltage sources as explained with the following example.

Consider a single transistor Q_i . The intrinsic VBIC model, used for modeling the self heating of this transistor in the absence of any other adjacent devices is shown in fig.2.7. $R_{th}Q_i$ and $C_{th}Q_i$ are the default R_{th} and C_{th} values for Q_i in the VBIC model.

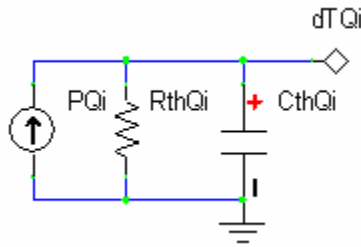


Figure 2.7 Intrinsic VBIC Model for Transistor Q_i

Now consider a case when this transistor is surrounded by four other adjacent transistors Q_j , Q_k , Q_m and Q_n . The rise in temperature due to inter-device heating

among all these five transistors can be modeled by the “Extrinsic VBIC Thermal Model” [PC] shown in fig.2.8.

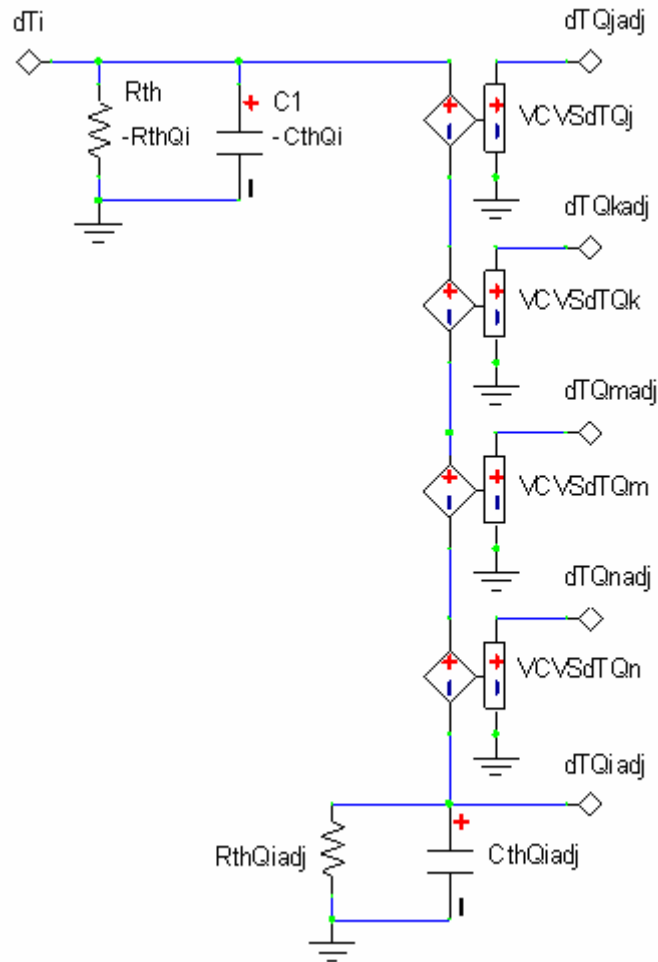


Figure 2.8 Extrinsic VBIC Thermal Model for Inter-Device Heating

In the above model the $R_{thQiadj}$ and $C_{thQiadj}$ are the respective R_{th} , C_{th} of device Q_i in the presence of the devices Q_j , Q_k , Q_m , and Q_n . R_{thQi} and C_{thQi} are the values of R_{th} and C_{th} that are in the Q_i default VBIC model. The inter-device heating effect is represented by the voltage controlled voltage sources (VCVS). The $VCVSdTQ_j$

has a gain of a_{ij} , where a_{ij} is the coupling coefficient for heating in device i due to dissipation in device j . The same is the case for the other transistors with the substitution of k , m , and n for j . There will also be a delay or phase shift associated with the gain of the VCVS. In practice, the node dtQ_i in fig.2.8 will connect to dT_i in fig.2.7. Similarly the nodes dTQ_{iadj} , etc. will connect to their counterparts on adjacent devices. The resistance, $-R_{thQ_{iadj}}$ and capacitance, $-C_{thQ_{iadj}}$ are added at the dT_i node to compensate for the default R_{th} and C_{th} values in VBIC model for the transistor Q_i .

From the above discussion it is clear that to implement the “External VBIC Thermal Model” it is necessary to characterize the thermal coupling coefficients. To determine the values of thermal coupling, it is necessary to develop test structures with different layouts and measure the device temperature rise caused by thermal coupling. Chapter 6 describes the different test structures developed for temperature measurement and different measurement techniques for the same.

With the above background of self heating and thermal coupling, the next chapter will concentrate on different computer aided design (CAD) tools and techniques for modeling the VBIC temperature effects.

CHAPTER 3

CAD TOOLS & SIMULATION TECHNIQUES FOR MODELING TEMPERATURE EFFECTS

The previous chapters described the structure of a DIBJT and the various thermal effects which need to be considered. This chapter focuses more on simulating self heating and different techniques for the same.

The first section talks about the widely used VBIC model and its advantages over the Gummel-Poon model. The second section gives an idea about different simulators available for simulating self heating effect. Use of the VBIC model in SpectreS simulator within the cadence is presented in the third section. The last section illustrates the meaning of the different temperature related terms in the SpectreS simulator.

3.1 Vertical Bipolar Inter Company (VBIC) Model

As mentioned in the previous chapter, the VBIC model has the advantage of incorporating the self heating effect which the Gummel-Poon model lacks. Hence it is widely used in simulators for simulating self heating. Fig.3.1 shows the equivalent circuit for the VBIC model. As can be seen it has an external thermal network and an excess phase network. The voltage at the 't' node denotes the rise in temperature above the ambient temperature. The self heating effect is mainly modeled by the thermal

resistance, R_{th} , and thermal capacitance, C_{th} . The self heating effect can be turned off by substituting $R_{th} = 0$ and $C_{th} = 0$.

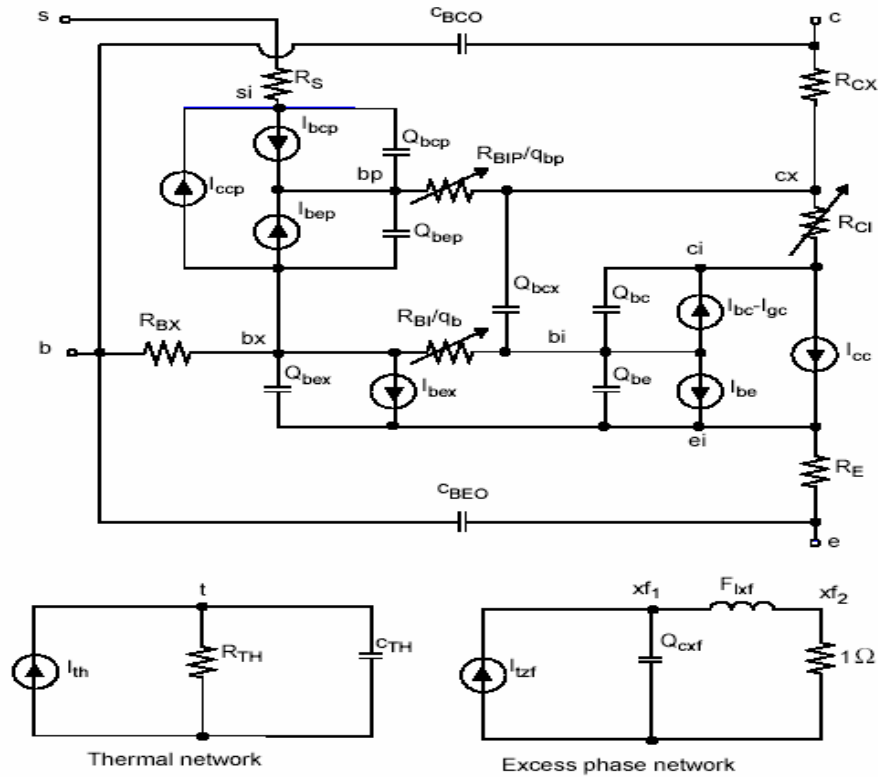


Figure 3.1 Equivalent Circuit VBIC Model [10]

In addition to modeling the self heating effect, the VBIC model has following advantages over the Gummel-Poon model:

1. Improved early effect modeling, g_0
2. Quasi-saturation modeling
3. Parasitic substrate transistor modeling

4. Parasitic fixed oxide capacitance modeling
5. Avalanche multiplication modeling
6. Improved temperature dependence modeling
7. Decoupling of base and collector currents.

Because of the above mentioned advantages and improved temperature modeling, the VBIC model has been used here for analysis and simulation purposes.

3.2 Different CAD tools supporting VBIC model

The most widely used simulator tools are Hspice, Spectre, SpectreS and ADS. Among these Hspice and ADS have limitations on using the VBIC model for simulating thermal effects [12]. Following are the limitations of using Hspice and ADS with VBIC model:

1. Hspice does not support PNP devices with 'dt' node. Thermal effects are not scaled with "Area" and "M" (multiplier factor) terms.
2. ADS does not have any temperature nodes and hence is unable to simulate thermal coupling effects.

Unlike Hspice and ADS, Spectre and SpectreS support both NPN and PNP devices with the VBIC model. Also in Spectre and SpectreS the thermal effects are scaled with "Area" and "M" terms [6]. Because of this, SpectreS is used in Cadence to simulate the thermal effects with the VBIC model.

3.3 Use of VBIC model in Cadence SepctreS simulator

In a simulator, it is essential to implement an explicit external thermal node for BJT to 1) Observe the temperature of each device and 2) Implement the thermal

coupling effect by the addition of voltage controlled voltage sources (VCVS) connecting the external nodes of the adjacent devices.

Considering the above facts a 6-terminal transistor symbol has been created for SpectreS simulations [11]. Fig.3.2 shows the same symbol.

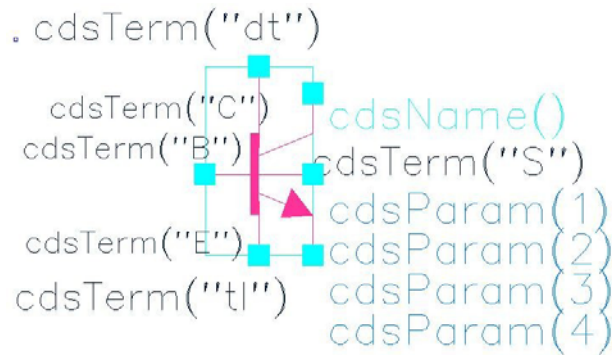


Figure 3.2 The VBIC 6 Terminal Transistor Symbol for the SpectreS Simulator [11]

In the above symbol for the BJT the B, C, E and S nodes represent the base, collector, emitter and substrate terminals as in the case of a normal BJT symbol. The added 'tl' node is the local temperature node and the 'dt' node is the temperature rise above the local temperature caused by the thermal power dissipated by the device. The voltage at the 'dt' node indicates the rise in temperature of the device above the ambient (local) temperature. 1 Volt at the 'dt' node represents a 1 degree rise in temperature of the device above the ambient temperature.

The 'tl' node in the symbol is not necessary and can be removed from the symbol while doing the simulations for self heating. So the BJT symbol will have only five nodes, B, C, E, S and dt. This modified symbol has been used here throughout for the thermal simulations in SpectreS using Cadence.

In the VBIC mode the self heating is modeled by the model parameters RTH, CTH and SELFT. The self heating effect can be simulated by setting RTH and CTH equal to the thermal resistance and thermal capacitance of the device and SELFT is set equal to one. Similarly the design can be simulated without self heating by either setting RTH and CTH equal to zero or SELFT equal to zero.

This means that every time the self heating condition is changed it is necessary to make changes to these model parameters. To avoid the task of accessing the model files while changing the simulation condition from self heating to no self heating or vice versa, the following procedure was used for the thermal simulations:

1. In the model file assign the model parameters RTH, CTH and SELFT as
$$\text{RTH} = \text{rthx} * (\text{Value of thermal resistance for the device})$$
$$\text{CTH} = \text{cthx} * (\text{Value of thermal capacitance for the device})$$
$$\text{SELFT} = \text{selfx} * 1$$
2. In the analog design environment edit the values of rthx and cthx equal to 1.
3. To simulate the self heating, the value of selfx is edited as equal to 1 in analog design environment.
4. Simulations with no self heating can be done by either editing the values of rthx and cthx equal to zero or by assigning selfx equal to zero in the analog design environment.
5. Any variable name can be used instead of rthx, cthx and selfx and can be edited respectively in the analog design environment. For simplicity these

variable names are used here throughout unless and until mentioned otherwise.

With the above basic knowledge of simulating the self heating effect in SpectreS, next section explains the different temperature related terms in Cadence SpectreS simulator.

3.4 Different temperature related terms

Various temperature related terms are used in the Cadence SpectreS simulator. These are mainly TREF, tnom, temp and T. TREF is a SPICE term and is mentioned in the VBIC model file. T, tnom and temp are the terms observed in the analog design environment. To know the exact significance of these terms, simulations were carried out with a current feedback operational amplifier (CFOA) with a circuit configuration as shown in fig.3.3. The simulations were carried out with and without self heating on and varying the above mentioned terms in sequence. Table 3.1 summarizes the simulation results with selftx = 0 and TREF = 25.

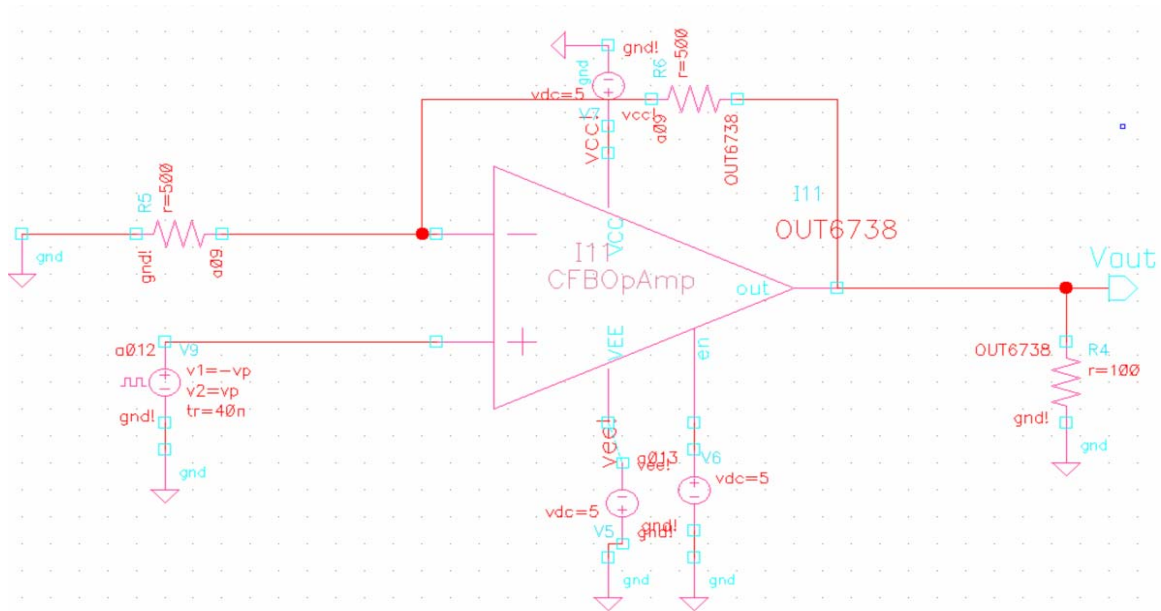


Figure 3.3 Schematic of CFOA used to verify different temperature related parameters in SpectreS

Table 3.1 Simulation results for CFOA with selftx = 0 and TREF = 25

Temp	Tnom	Vout
27	27	3.56946
27	25	3.56946
27	50	3.56946
25	27	3.56798
50	27	3.58935

From the above simulation results it is clear that changing 'tnom' with const 'temp' does not have any affect on the output voltage (Vout), proving that 'tnom' gets overwritten by 'TREF'. The output voltage changes with a change in 'temp' with constant 'tnom' and 'TREF' which means that 'temp' represents the overall circuit temperature. By changing the value of 'temp' it was observed during the simulation that

in analog design environment, 'T' takes the value of the 'temp' proving, 'T' also represents the overall circuit temperature.

Similar simulations were carried out with selftx = 1 and TREF = 25 and these are tabulated in table 3.2. These results also support the conclusions drawn from the selftx =0 simulations.

Table 3.2 Simulation results for CFOA with selftx = 1 and TREF = 25

Temp	Tnom	Vout
27	27	3.59324
27	25	3.59324
27	50	3.59324
25	27	3.59167
50	27	3.61277

The above conclusions can be summarized as follows:

1. 'TREF' is the temperature at which all the model parameters are calculated.
2. 'temp' is the circuit temperature, meaning the temperature at which the overall simulation is carried out, and is available in the analog design environment for editing.
3. 'T' is same as 'temp' and can be seen at the top of analog design environment while the simulation is running.
4. 'tnom' is available for editing in the analog design environment and gets overwritten by the value of 'TREF'.

5. If 'TREF' is mentioned in the model file, editing 'tnom' in the analog design environment has no effect.

With this background of the CAD tools and simulation techniques used for modeling temperature effects, the next chapter presents the use of these simulation techniques. Thermal characterization of complex circuits such as the current feedback operational amplifier (CFOA) is demonstrated.

CHAPTER 4

THERMAL CHARACTERIZATION OF CURRENT FEEDBACK OPERATIONAL AMPLIFIER (CFOA)

Current feedback operational amplifiers (CFOA) have higher slew rate, lower input referred noise, better differential gain and phase performance than the Voltage Feedback Operational Amplifiers (VFOA). Because of these advantages, the CFOA is being used mainly for automatic gain control and video signal processing applications. National Semiconductor has developed a current feedback architecture using an advanced complimentary bipolar process to meet a variety of industrial requirements. One of National's CFOA architectures has been used for the thermal study in this research work and is the main focus of this chapter. The first section describes the general topology of the CFOA. The motivation for the thermal study of the CFOA is presented in section two. The third section presents the thermal behavior of the devices constituting the particular CFOA. The last section gives an idea about the dependence of the thermal effects on different layout factors and the possible representation of these factors at the design or circuit level.

4.1 General Current Feedback Operational Amplifier (CFOA) topology

The general schematic of a typical modern complementary bipolar high speed current feedback operational amplifier (CFOA) is shown in fig.4.1. The basic architecture consists of a unity gain input buffer, a current mirror gain stage, and a unity gain output buffer.

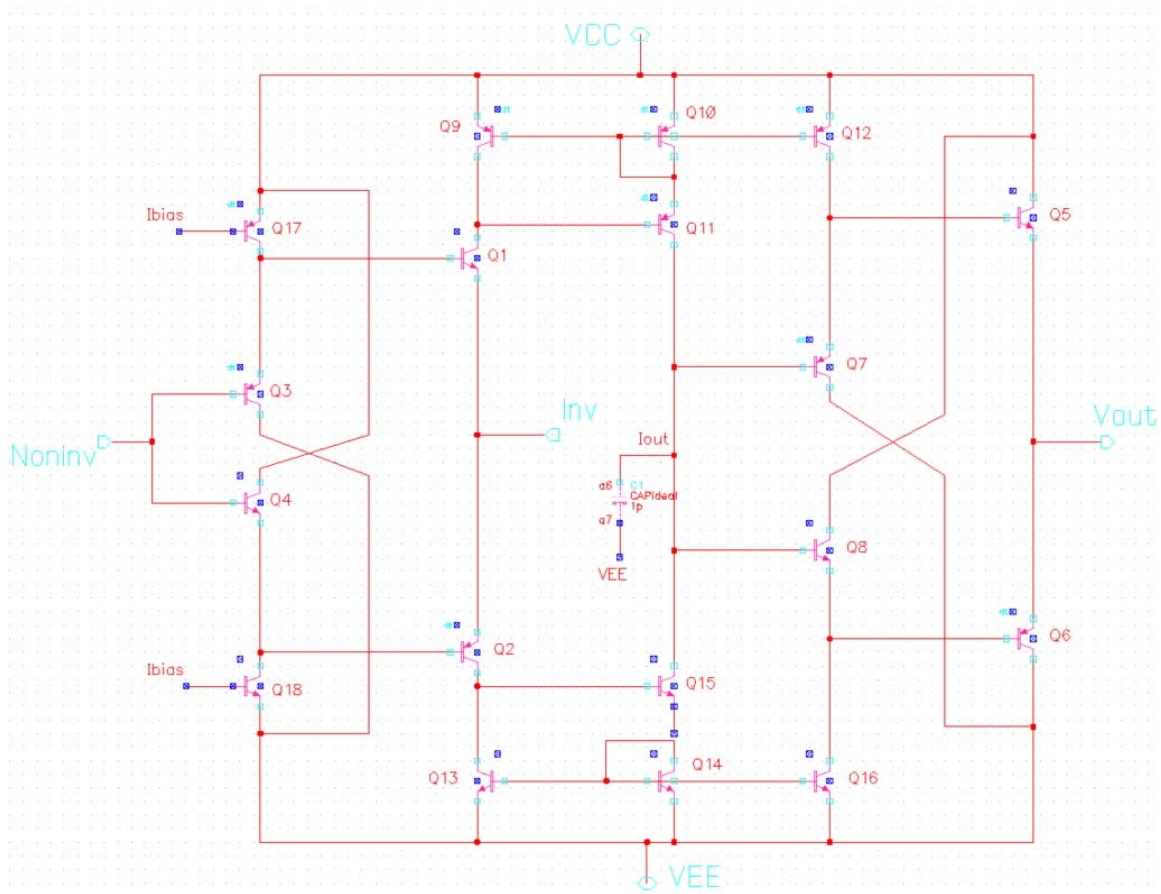


Figure 4.1 General Schematic of typical high speed complementary bipolar CFOA [13]

Complementary emitter followers Q1-Q4 form the input buffer. Collector currents of transistors Q1 and Q2 are turned around and summed through Wilson current mirrors formed by Q9-Q11 and Q13-Q15 respectively. This signal current injected into the high impedance node sets the open loop gain of the amplifier. The output buffer is formed by Q5-Q8. This output buffer provides nearly unity voltage gain and isolates the high impedance current summing node from the amplifier node. The single gain stage architecture provides high bandwidth at the expense of open loop transimpedance. The loss of dc accuracy is usually acceptable in high-speed applications in which these amplifiers are used [13].

Almost all complementary bipolar high-speed CFOAs are a variation of the basic architecture described above and employ some variations to meet different design specifications as well as characteristics of the fabrication process. The particular CFOA used here for the thermal study has architecture similar to the one shown in fig.4.1 with some specific variations to meet fabrication process characteristics. Since this CFOA is actually used by National Semiconductor, its exact architecture is not shown here. However the schematic in fig.4.1 is a functional equivalent for the same and will be used henceforth. Thermal analysis is carried out for all devices in the original CFOA design, but will be discussed here for Q1 to Q18 as mentioned in fig.4.1.

4.2 Need for the thermal study of CFOA

The devices used in this CFOA are dielectrically isolated BJTs (DIBJT). As discussed in previous chapters, these are the devices which are most affected by thermal

effects. So this is a good design to study how the device level thermal effects affect the overall circuit performance when they are used as the building block for the circuit. The primary study of this particular CFOA showed that the percentage output error varies with time for an initial period of a few microseconds. When simulated this CFOA with self heating ON for all the devices, it showed a time varying thermal offset shown in figure 4.2. The thermal offset is same as the time dependent gain error and is defined as

$$TO = \text{Thermal Offset (\%)} = (dV(t) - dV(\text{settled value})) \times 100 \quad (4.1)$$

where,

$$dV = \frac{V_{out} - A \times V_{in}}{A \times V_{in}} \quad t \text{ is the time since the switching transition and } A \text{ is the closed}$$

loop gain of the amplifier.

From figure 4.2 it can be observed that the thermal offset immediately after switching is 0.5% with a time-constant of 2.09 microseconds. The time constant is consistent with the, $R_{th} \times C_{th}$ product, thermal characteristic time of the devices.

The measurement data taken for the same CFOA is shown in figure 4.3. It shows the measured data for the thermal offset vs time for a V_{in} transition from -1V to +1V

[14].

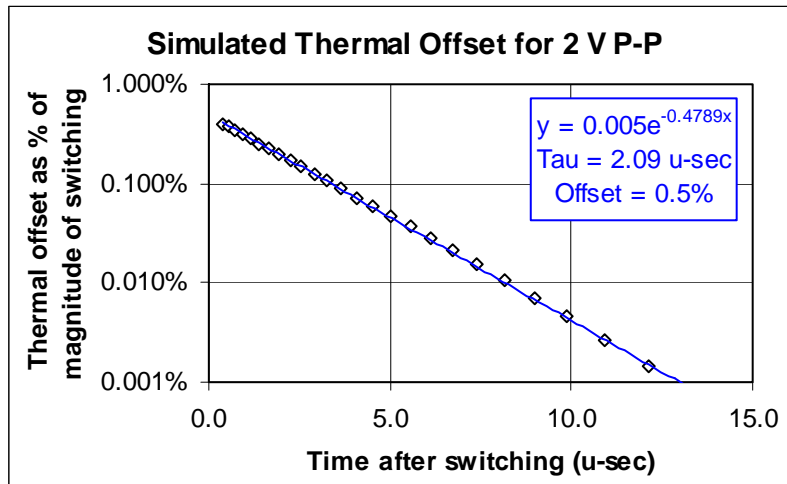


Figure 4.2 Simulation plot of log of TO vs. time for CFOA [14]

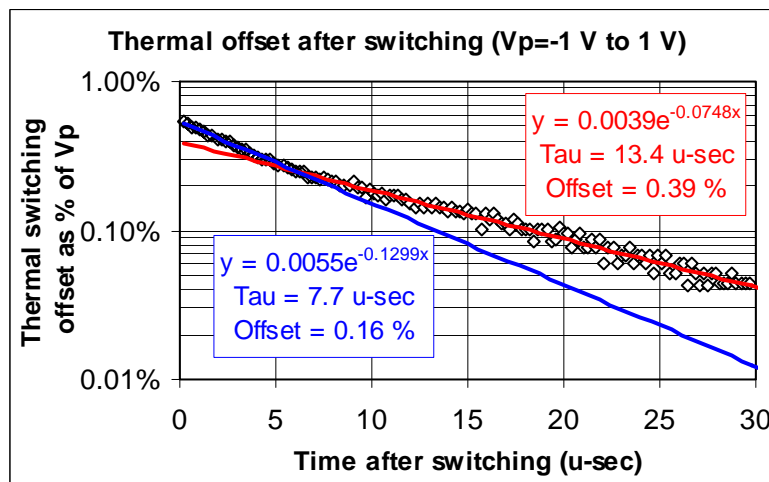


Figure 4.3 Measured TO data for the CFOA on a 2V P-P (-1 to +1) transition [14]

Comparing fig.4.3 with fig. 4.2 it is clear that the simulation and the measured data have approximately the same initial offset error of 0.5%. But the measured data shows two significant time constants, a short time constant of 7.7 microseconds with initial offset of 0.16% and a longer time constant of 13.4 microseconds with a 0.39%

initial offset. This complex time constant response is the main motivation for the detailed thermal characterization of the CFOA. Following are the some of the initial hypothesis made to accommodate the complex time constant:

1. The difference in the time constant is because of the different thermal response of the devices forming various stages of the CFOA.
2. Considering the layout it can be predicted that the short time constant may be because of the devices on the non-inverting terminal and the longer time constant may be because of the devices forming the inverting input, high impedance node and the output buffer.
3. The thermal response of the device, surrounded by the adjacent devices, may be different from that of an isolated device.
4. A different time response of the heat flow from the tub than that through the trench oxide.
5. Also the absence of the complex time constant response in the simulation results gives some idea about the ineffectiveness of the existing VBIC model to consider additional complex thermal heating effects like thermal coupling, other than self heating and hence needs to be improved or modified.

To prove the above hypothesis, it is necessary to study the thermal behavior of the CFOA in depth. The thermal study needs to be done for all the devices constituting the CFOA to figure out how the device level thermal effects exactly affect the circuit performance. This study needs to be done in a systematic manner so as to analyze the

contribution of each stage in the design, towards the overall thermal time constant. It is also essential to study the layout of the particular CFOA to know the position of each device in the layout, to observe the dependence of device position in a layout, on its thermal response. The next section presents the thermal response of all the devices in the CFOA using the cadence SpectreS simulator.

4.3 Thermal response of the devices constituting the CFOA

To study the effect of each device on the thermal response of a CFOA it is necessary to know the power dissipation and temperature rise above the ambient temperature for all devices. This section describes the simulations carried out to obtain this data with self heating on. The initial analytical observations drawn from this data are mentioned at the end of this section. As mentioned in section 4.1, figure 4.1 is used to represent the particular CFOA and to analyze results stagewise the transistors were named as shown in fig.4.4 where the following nomenclature mentioned in 4.3.1 is used to differentiate various stages of the CFOA.

4.3.1 Nomenclature used for CFOA

Basically the CFOA is divided into five main branches each called a stick. The leftmost non-inverting branch is called stick0 and the rightmost branch is denoted as stick4 or the output stick. To differentiate among all the devices on these particular sticks, the transistors on these are named as follows:

NPN and PNP on stick0 (Non-inverting input) is denoted as normal NPN and PNP

NPN and PNP on stick1 (Inverting input) is denoted as I_NPN and I_PNP

NPN and PNP on stick2 is denoted as 2_NPN and 2_PNP

NPN and PNP on stick3 is denoted as 3_NPN and 3_PNP

NPN and PNP on stick4 or output stick is denoted as Out_NPN and Out_PNP

This convention is used throughout the CFOA analysis and is demonstrated in figure 4.4.

4.3.2 Thermal Simulations

The VBIC model was used to simulate the self heating effects in the Cadence SpectreS simulator. A 2V peak to peak square wave input with rise and fall times of 40 nsec. and a pulse width of 50 μ sec with a 50% duty cycle was used for the simulation as shown in figure 4.5. The CFOA was simulated with 'self' turned on for all the devices.

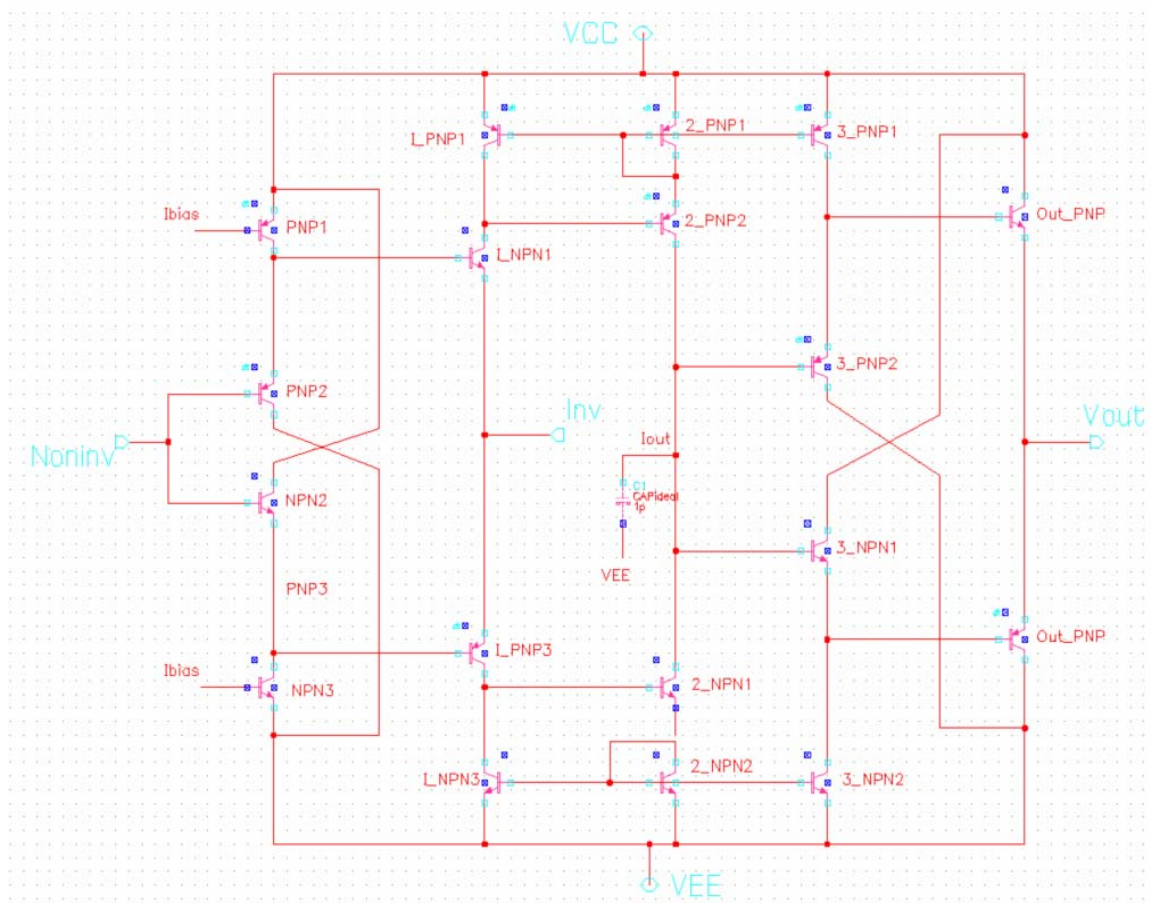


Figure 4.4 General Schematic of CFOA Showing the nomenclature used for devices on different sticks

As mentioned in previous chapters the voltage at 'dt' of the device represents the increase in temperature above ambient temperature for the particular device. In this design 'dt' nodes of all the transistors were available, since the 6 terminal transistor symbol described in chapter 3 was used. The 'dt' nodes were labeled the same as the transistor names. The transient response of the voltage (which is equivalent to a rise in temperature) at these 'dt' nodes for NPN and PNP devices is shown in fig.4.6 and 4.8 respectively. The bar graph showing the temperature rise of each device during the

positive half cycle and the negative half cycle for the NPN and PNP devices is shown in fig.4.7 and 4.8 respectively.

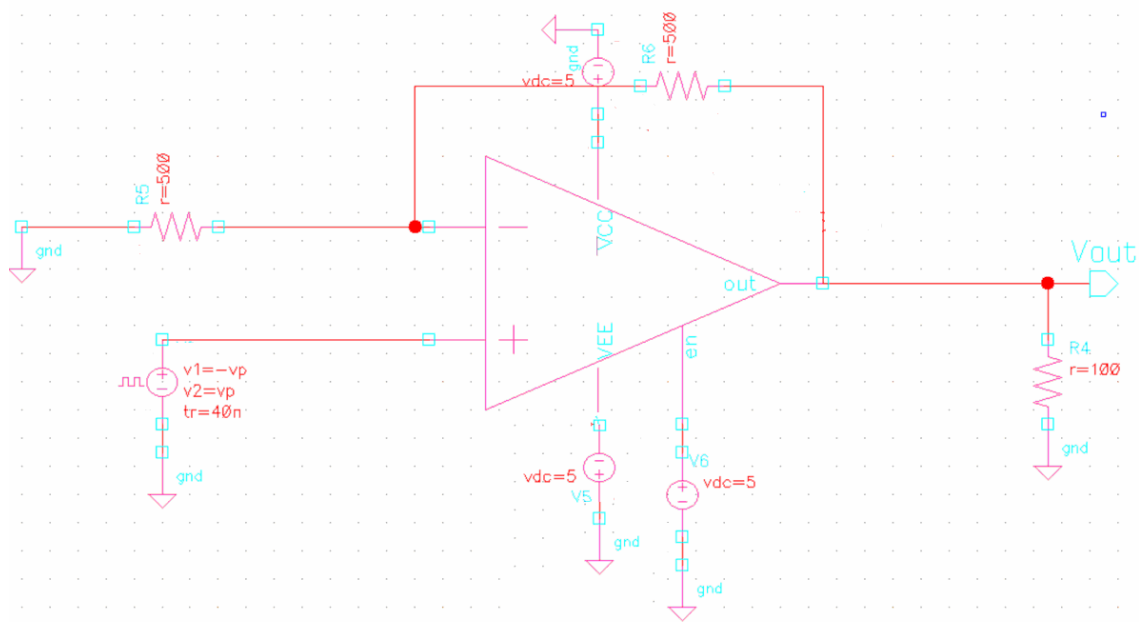


Figure 4.5 Simulation set up for thermal analysis of CFOA

As can be seen from fig. 4.6 and 4.7 each device in the CFOA heats up in a distinct way because of its self heating and exhibits a different thermal response than any of the other devices. Also the thermal response for a particular device differs for the positive half cycle and negative half cycle.

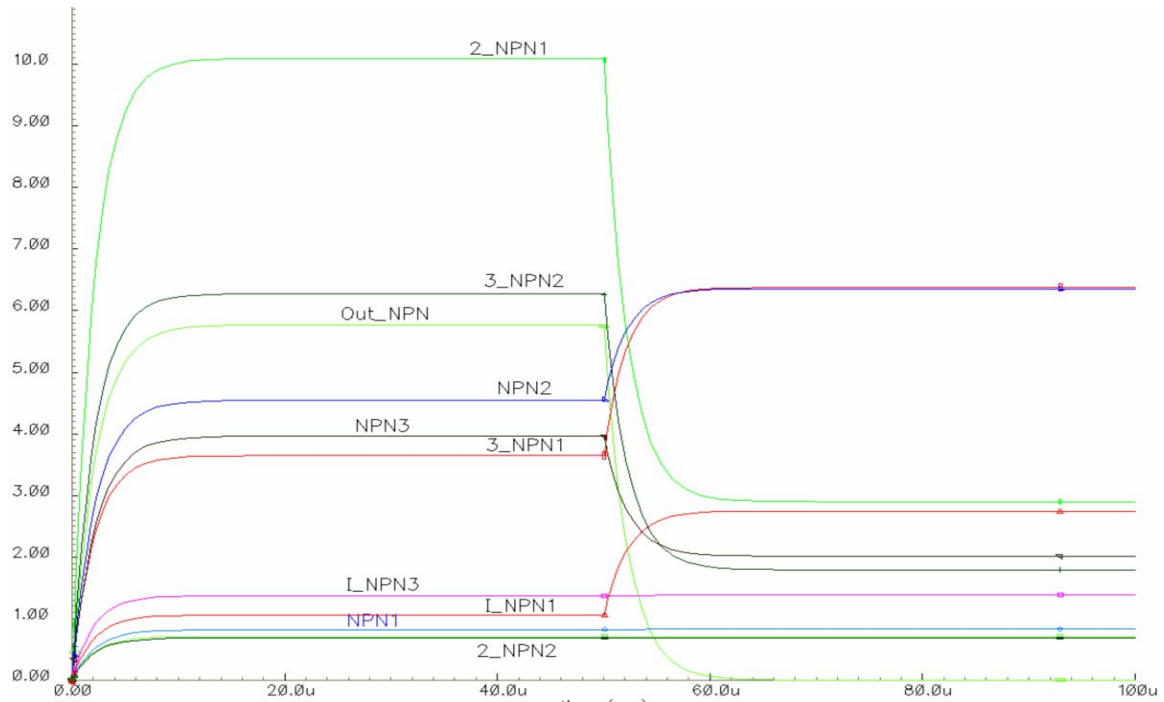


Figure 4.6 Transient response of the voltages at 'dt' nodes of all NPN devices in CFOA with 'self' on for all devices

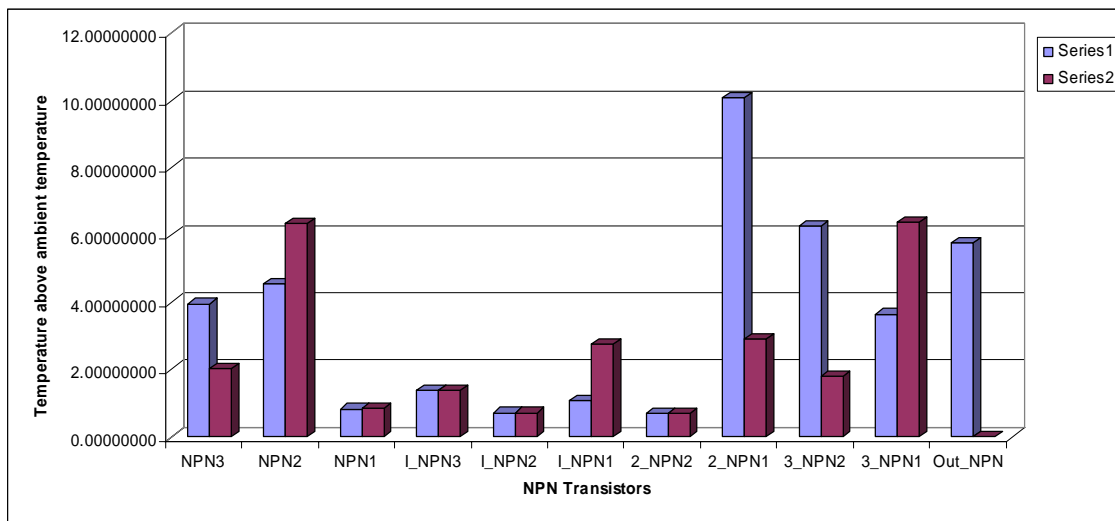


Figure 4.7 Final temperatures at 'dt' nodes of all NPN devices in CFOA with 'self' on for all devices

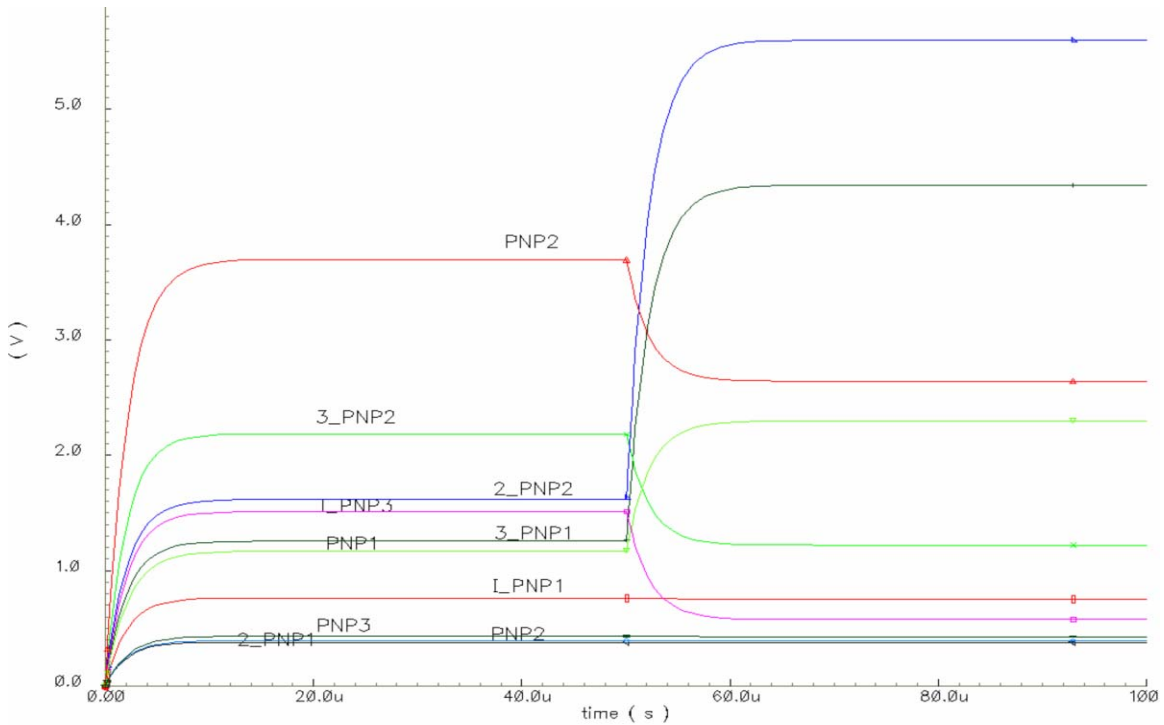


Figure 4.8 Transient response of the voltages at 'dt' nodes of all PNP devices in CFOA with 'selft' on for all devices

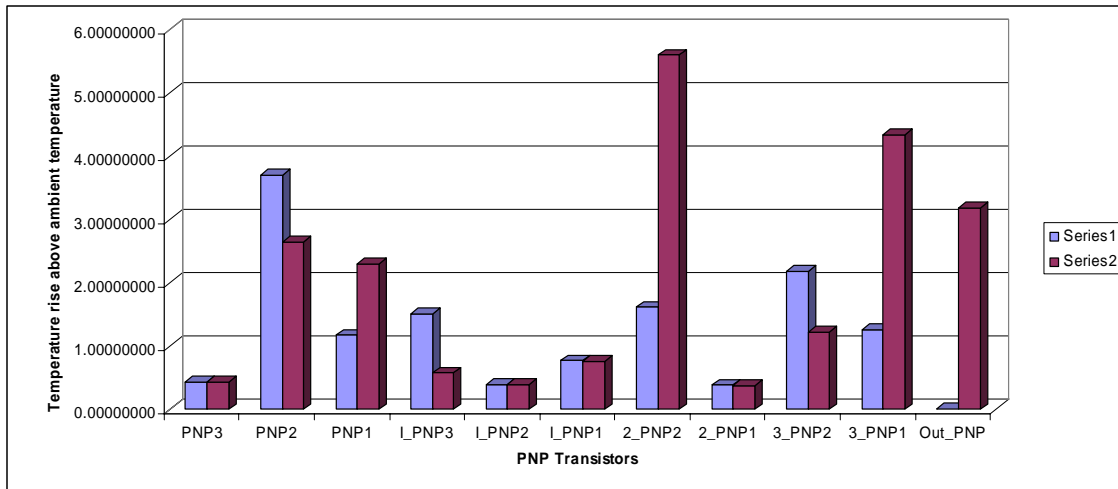


Figure 4.9 Final temperature at 'dt' nodes of all PNP devices in CFOA with 'selft' on for all devices

From the analysis of different graphs shown in figures 4.6 to 4.9 along with the CFOA design study, the following primary results were obtained:

1. The maximum temperature rise was observed on transistors 2_PNP2 and 2_NPN1. These are the transistors on the high impedance stick and carry almost twice the current than that in the inverting terminal.
2. Transistors NPN2 and PNP2 have significant rise in temperature and the difference between the rise in temperature during the positive and negative half cycles of the input is less than the other transistors in the CFOA. This confirms that these transistors do not cool down as fast the other transistors.
3. The CFOA output is a class AB stage. The output NPN transistor carries all the current during the positive half cycle and the PNP during the negative half cycle. Since the power dissipation and hence the self heating is directly proportional to the current, the same trend can be observed in the temperature rise of these devices during the positive and negative half cycle of the input.
4. Even though the output stage carries the maximum current, the temperature rise in the output devices were not observed to be the highest among all devices. The main reason for it is that each output transistor has 10 transistors in parallel. In other words, the area of each output device is 10 times the area of single device. Since the thermal resistance scales inversely to the area of device, the temperature rise for these devices is less than other devices in the CFOA.

From the above discussion, it can be concluded that the transistors on the non-inverting terminal, NPN2 and PNP2 and transistors on the high impedance stick, 2_PNP2 & 2_NPN1 are the ones, which heat up significantly and can be the primary cause of the complex time constant and offset error.

4.4 Layout study of the CFOA

As mentioned in section 4.2, the complex time constant response of the CFOA might result from the thermal delay caused by different stages of the CFOA. To study the exact cause for this thermal delay, it is necessary to know the way all the devices are laid out in the CFOA. This section talks about the overall layout study of the CFOA. As mentioned before due to proprietary concerns the layout is not shown here.

A detailed layout study of the CFOA shows that the devices on the non-inverting terminal are laid close to each other. The NPN devices on stick1 to stick3 are contiguous as compared to any other NPN devices in the CFOA. The output devices are far away from the input stick and separated from each other. This particular layout style might be the reason for the complex time constant. The shorter time constant may be caused by the devices on non-inverting input terminal. Since the devices on stick1 to stick3 are separated from each other by a minimum spacing (2 um) available for this technology, these devices which could experience thermal coupling in addition to self heating, and contribute towards the longer time constant. Also as observed from the thermal simulations in section 4.3.2, the 2_NPN1, NPN device on stick2, heats up the most. This device was surrounded by three neighboring devices with a minimum spacing of 2 um between shared walls. The geometry of these particular devices on

layout is represented in fig. 4.10. This structure was the motivation for the design of the test structure for studying the thermal coupling and will be explained in more detail in chapter 6.

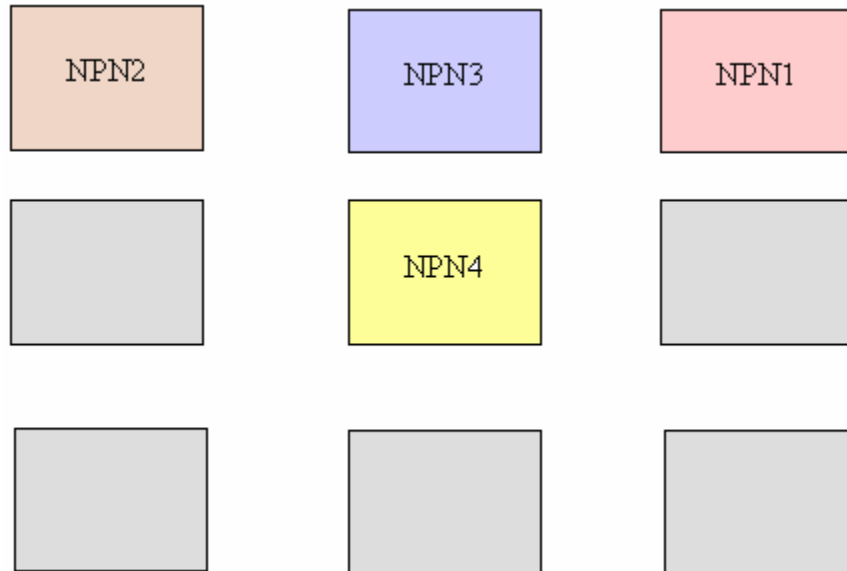


Figure 4.10 Part of Layout representation for the devices on stick1, 2 & 3

Also it can be observed from fig.4.10 that the device is not square in shape, having the same dimensions for all the sidewalls. Rather it is rectangular with two small sidewalls and two larger sidewalls. Since heat flow is directly proportional to the area of the surface, the heat flow through all the sidewalls is not the same. As the heat flow varies with the device sidewalls, thermal coupling must also vary with the sidewalls as well as the spacing between two adjacent devices. The maximum thermal coupling will be for the devices with minimum spacing.

Thus the layout study gives an insight into the geometry of the devices and the different possible ways to lay out the design. It also gives an idea about the possible causes for the complex time constant. In addition to all these points this layout served as the main motivation to develop test structures for the study of the thermal coupling between adjacent devices.

As mentioned above, layout dependant factors like thermal coupling contributes towards the overall circuit performance and varies with variation in the layout. The existing VBIC model for the BJT does not have any model parameter to model these effects. Hence it is essential to make changes in the model file or develop circuit level modifications to accommodate these effects. The second approach is easier than the first, since with the first one different model files will have to be used as the layout changes. The circuit level change involving modification of the existing VBIC model, as mentioned in chapter 2, will be easier and needs to be verified with this particular CFOA design.

With this understanding of thermal simulations along with the layout study of the CFOA, the next chapter explains in-depth characterization of off-set error and gain error for this particular CFOA.

CHAPTER 5

THERMAL CHARACTERIZATION OF OFFSET AND GAIN ERROR FOR CFOA

As observed in chapter 4, measurement results for the particular CFOA under study showed a variation in the thermal offset with switching time. This thermal offset basically involves time dependent gain error change. At first sight the main reason for gain error comes from unbalanced components resulting in input offset voltage. It is essential to study the change in time dependent gain error as well as the change in input offset voltage with self heating. Also, in-depth analysis needs to be done to know the contribution of each device. This enables design and layout engineers to implement modifications in order to overcome these errors. Comprehensive analysis of these errors for the CFOA was carried out in this research work and is presented in this chapter. The first and second section of the chapter presents the thermal characterization of the input offset voltage of CFOA. Time dependent gain error analysis is described in the last section of the CFOA.

5.1 Input offset voltage (V_{io}) variation with temperature

5.1.1 Input offset voltage (V_{io})

The differential input voltage that exists between two input terminals of an operational amplifier without any external inputs applied is called the ‘input offset voltage’ and is denoted by V_{io} . In other words, the input offset voltage is the amount of the input voltage that should be applied between two input terminals in order to force the output voltage to zero.

5.1.2 Thermal Voltage Drift

The most serious variation in the value of V_{io} is due to the change in temperature. The average rate of change of input offset voltage per unit change in temperature is called ‘thermal voltage drift’ and is denoted by dV_{io} / dT . As mentioned in chapter 3, circuit temperature is denoted by ‘temp’ in the SpectreS simulator. Hence thermal voltage drift will be denoted as $dV_{io} / dtemp$.

Thermal voltage drift is not a constant value. It is not uniform over a specified operating temperature range. Furthermore, the value of the input offset voltage may increase or decrease with increasing temperature. Since the input offset voltage is one of the possible contributors to gain error, it is important to study the behavior of the thermal voltage drift.

5.2 Different Circuit Configurations for input offset voltage simulations

To study the thermal voltage drift of the CFOA under study, it is connected in closed loop with a gain of 101 as shown in fig.5.1. In this particular configuration, it is made sure that the resistors used in the non-inverting and inverting terminals have same ratio in order to eliminate errors arising due to resistance difference.

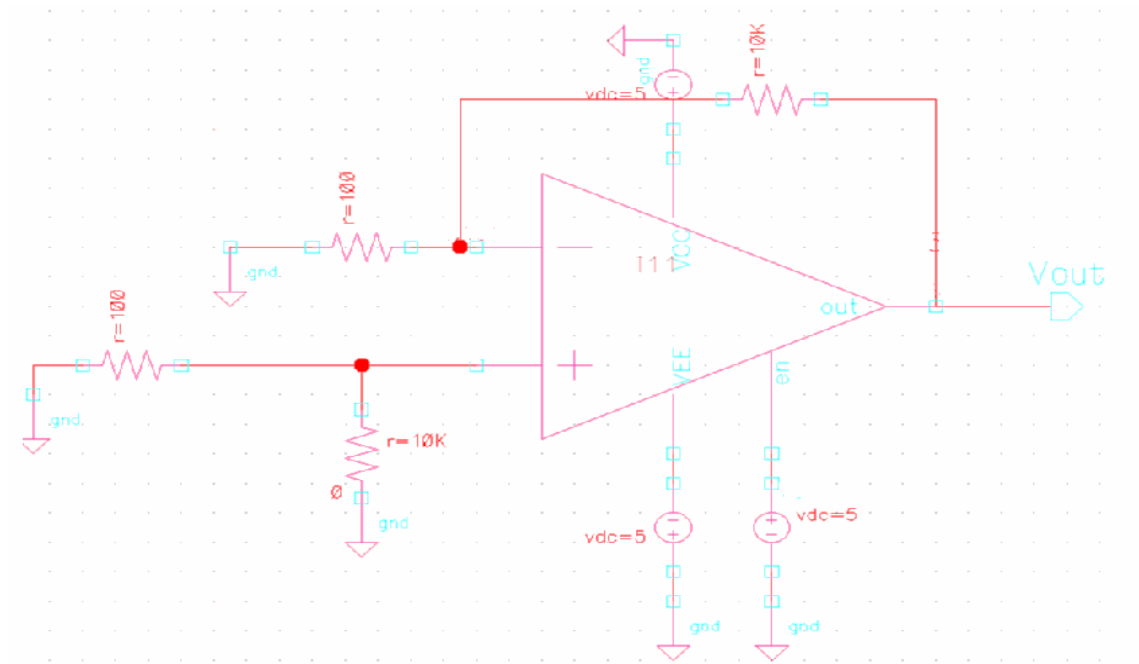


Figure 5.1 Closed loop CFOA configuration for Vio simulations

The above schematic was simulated with selft ON as well as OFF for all the devices over a circuit temperature range of 25⁰ C to 40⁰ C. Input offset voltage was calculated for each temperature as (Vout / 101). Table 5.1 lists the values of input offset voltages at different circuit temperatures.

Table 5.1 Input offset voltage values with selft = 0 and selft = 1 for the schematic shown in fig.5.1

Circuit Temperature	selft = 0	selft = 1
Temp	Vio	Vio
25	0.00089	0.00242
27	0.00086	0.00241
29	0.00084	0.00239
31	0.00081	0.00238
33	0.00079	0.00236
35	0.00077	0.00234
37	0.00074	0.00232
39	0.00072	0.00231
40	0.00071	0.00230

A graph showing the variation of the input offset voltage with overall circuit temperature is plotted in figure 5.2.

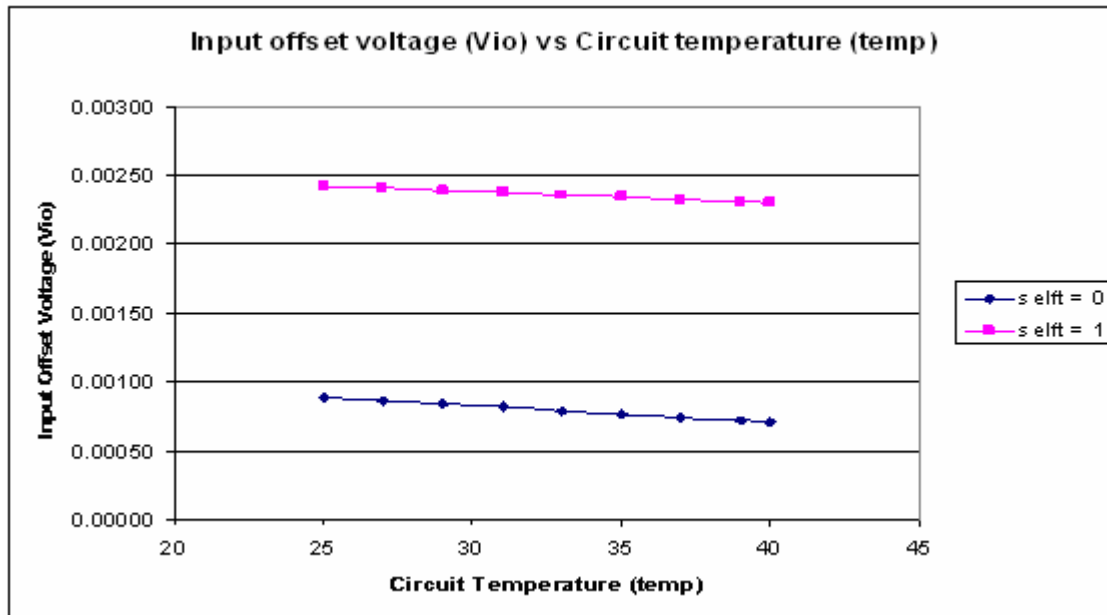


Figure 5.2 Input offset voltage (Vio) with variation in the circuit temperature for selft = 0 and selft = 1

It was observed from the plot of fig.5.2 that the input offset voltage varies with circuit temperature. It can also be seen that self heating changes the value of the input offset voltage from its value when all the devices are turned OFF with self heating. This analysis clearly showed that thermal voltage drift not only depends upon the circuit temperature but is also a function of device temperature.

It was observed that offset voltage changes with change in the resistor values in the inverting and non-inverting terminals, even when the ratio is maintained same. Thus this method of finding the offset voltage does not prove to be the accurate one. Also, since the thermal offset analysis and measurements done before were with resistances of $500\ \Omega$ in the feedback as well as in inverting input terminal, the offset voltage analysis should be done with these values of resistors. Hence to improvise the offset voltage results the schematic shown in fig.5.3 was used for simulation purposes. In this method of finding the input offset voltage, the input voltage is inserted in the non-inverting terminal and varied to make the output voltage equal to zero. With this DC input voltage in the non-inverting input, the voltages at both input nodes denoted by V_p and V_n were noted down. The voltage difference ($V_p - V_n$) between these input nodes is the input offset voltage.

As observed in the previous analysis, the thermal drift voltage depends on the device temperature. To study the contribution of each device temperature variation to the input offset voltage change, self heating was turned ON for all devices except a particular device. This can be obtained by globally turning selft ON for all devices and

turning it OFF for a particular device while carrying out the input offset voltage simulations.

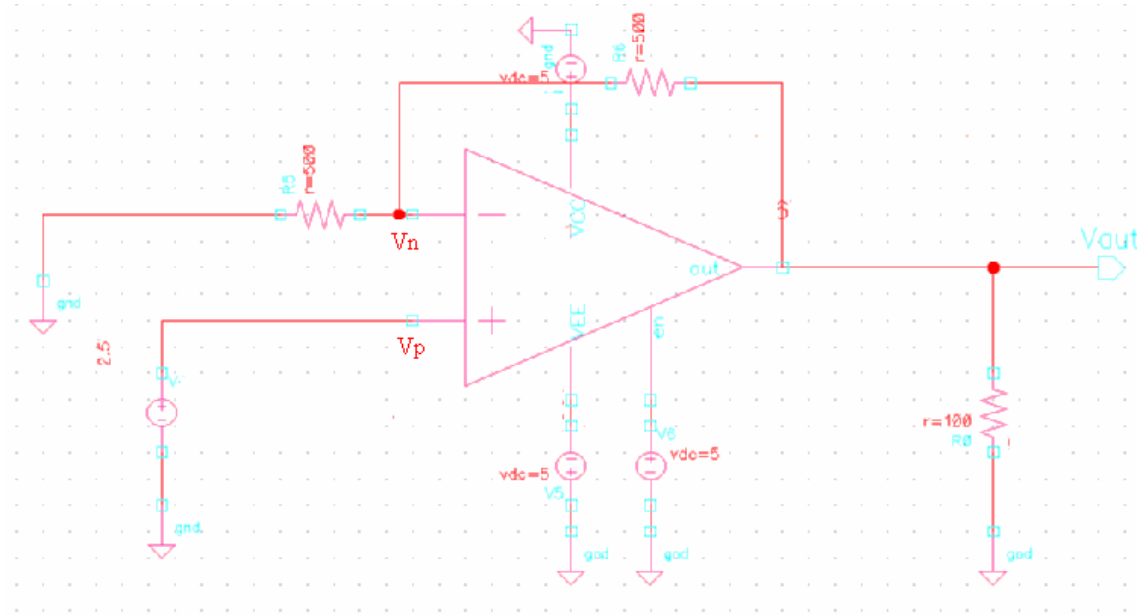


Figure 5.3 Simulation set up for input offset voltage measurements with DC source in non-inverting input

In the first case, for which all transistors are turned ON with self heating, voltage values at the V_p , V_n nodes are -0.00129 V , 0.00068 V respectively. The input offset voltage, which is a difference between the two node voltages is -0.00197 V . The input offset voltage in this case shows the offset voltage contributed by all the devices.

In the second case only one particular device selft was turned OFF. In this case the voltages at the V_p and V_n nodes were observed and the input offset voltage was calculated as the difference between these voltages for all the devices. Table 5.2 and 5.3 list the input offset voltage values with a particular device selft turned OFF at one time. Assuming the superposition for overall input offset voltage, the difference between the

input offset values in the first case and the second case (ΔV_{io}) gives the contribution of the particular device towards the offset voltage due to self heating. The value of ΔV_{io} (Input offset voltage error) is also included in table 5.2 and 5.3 for each device.

Table 5.2 Input offset voltage with a particular NPN device self turned OFF for the circuit configuration shown in fig.5.3

Transistor	Vp	Vn	Vio	ΔV_{io}
NPN3	-0.00167	0.00068	-0.00235	0.00038
NPN2	0.00250	0.00070	0.00180	-0.00378
I_NPN3	0.00029	0.00208	-0.00180	-0.00018
I_NPN1	0.00007	0.00068	-0.00061	-0.00136
2_NPN2	-0.00206	0.00000	-0.00206	0.00009
2_NPN1	-0.00132	0.00066	-0.00198	0.00001
3_NPN2	-0.00140	0.00059	-0.00199	0.00001
3_NPN1	-0.00129	0.00069	-0.00197	0.00000
Out_NPN	-0.00129	0.00068	-0.00197	0.00000

It can be seen that the input offset voltage V_{io} and input offset voltage error ΔV_{io} changes are very small. Hence simulations for the same need to be carried out with high accuracy.

Table 5.3 Input offset voltage with a particular PNP device self turned OFF for the circuit configuration shown in fig.5.3

Transistor	Vp	Vn	Vio	ΔV_{io}
PNP2	-0.00367	0.00069	-0.00436	0.00239
PNP1	-0.00105	0.00068	-0.00173	-0.00024
I_PNP3	-0.00206	0.00067	-0.00273	0.00076
I_PNP1	-0.00219	-0.00012	-0.00208	0.00010
2_PNP2	-0.00181	0.00078	-0.00259	0.00061
2_PNP1	-0.00086	0.00106	-0.00193	-0.00005
3_PNP2	-0.00131	0.00067	-0.00198	0.00000
3_PNP1	-0.00123	0.00074	-0.00197	-0.00001
Out_PNP	-0.00129	0.00068	-0.00197	0.00000

Careful analysis of the figure 5.3 indicates that at the amplifier input terminals, node V_p and V_n , there will be an input differential signal, since the non-inverting terminal is not grounded. In addition to the input offset voltage this small input differential signal will be amplified by the amplifier's closed loop gain. Hence the output is equal to the closed loop gain times the summation of input offset voltage and small differential input signal. Hence the results obtained for the input offset voltage with this circuit configuration are not accurate.

To overcome the problem of small input differential voltage observed with the circuit configuration of figure 5.3 an improved circuit as shown in fig.5.4 is used. In this arrangement the input voltage source forcing the output to zero is placed in the inverting terminal with the non-inverting terminal grounded. With this arrangement, the non-inverting terminal is grounded and since the inverting input terminal is at virtual ground the problem of additional input differential input signal gets resolved.

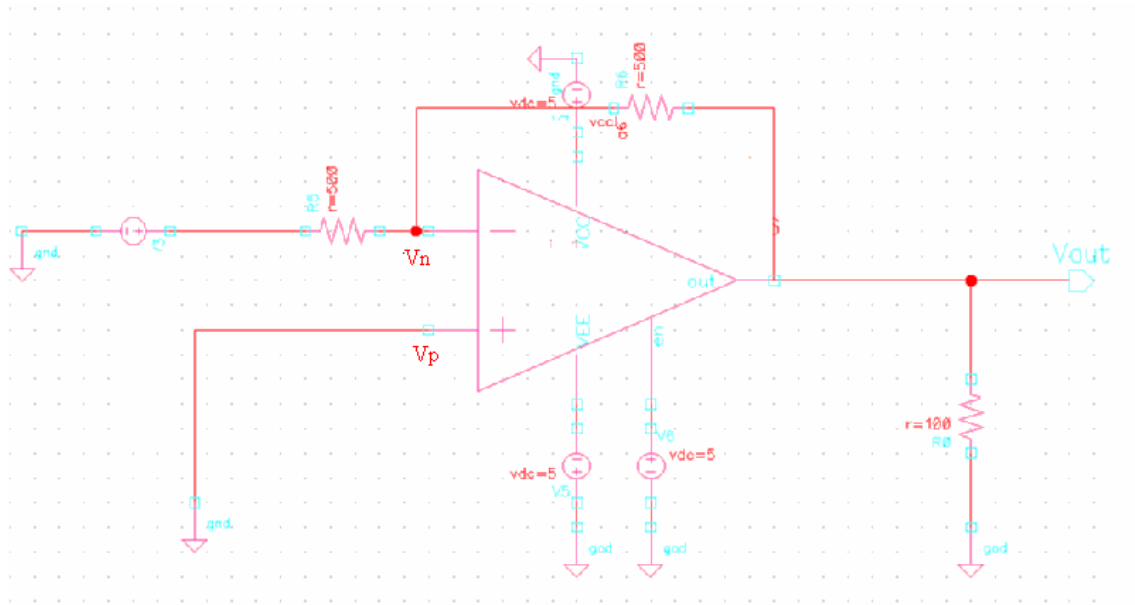


Figure 5.4 Simulation set up for input offset voltage measurements with DC source in inverting input

With this configuration, the input offset voltages are found for two cases; first with all devices selft turned ON and the second with all devices selft turned OFF. The input offset results for these two cases are tabulated in table 5.4. In this circuit configuration, since the non-inverting terminal is grounded, the input offset voltage is equal to the voltage at the Vn node with the opposite polarity. From table 5.4 it is confirmed that the offset voltage varies with variation in device temperature or self heating.

Table 5.4 Input offset voltage values with all devices turned ON and OFF.

Selft for all devices	Vio
ON	-0.00197
OFF	-0.00052

As mentioned before, the simulations for determining input offset voltage with a particular device selft turned OFF were carried out for this configuration too. The results showing the input offset voltages in this case are listed in table 5.5 and table 5.6. Also the input offset error values for each device are included in both these tables.

Table 5.5 Input offset voltage with a particular NPN device selft turned OFF for the circuit configuration shown in fig.5.4

Transistor	Vn	Vio	ΔVio
NPN3	0.00235	-0.00235	-0.00038
NPN2	-0.00180	0.00180	0.00377
I_NPN3	0.00180	-0.00180	0.00017
I_NPN1	0.00061	-0.00061	0.00136
2_NPN2	0.00206	-0.00206	-0.00008
2_NPN1	0.00198	-0.00198	-0.00001
3_NPN2	0.00198	-0.00198	-0.00001
3_NPN1	0.00197	-0.00197	0.00000
Out_NPN	0.00197	-0.00197	0.00000

Table 5.6 Input offset voltage with a particular PNP device selft turned OFF for the circuit configuration shown in fig.5.4

Transistor	Vn	Vio	ΔVio
PNP2	0.00435	-0.00435	-0.00238
PNP1	0.00173	-0.00173	0.00024
I_PNP3	0.00273	-0.00273	-0.00076
I_PNP1	0.00207	-0.00207	-0.00010
2_PNP2	0.00196	-0.00196	0.00002
2_PNP1	0.00192	-0.00192	0.00005
3_PNP2	0.00197	-0.00197	0.00000
3_PNP1	0.00196	-0.00196	0.00001

For readability purpose all the decimal figures are not included here in all the tables. But when compared accurately, the results obtained with configuration in fig 5.3 are higher than those obtained with configuration in fig.5.4, as expected.

Input offset voltage error ΔV_{io} , is also included in tables 5.5, 5.6. A plot showing the input offset voltage error ΔV_{io} contributed by individual device is drawn in fig.5.5 and fig.5.6 for NPN as well as PNP devices.

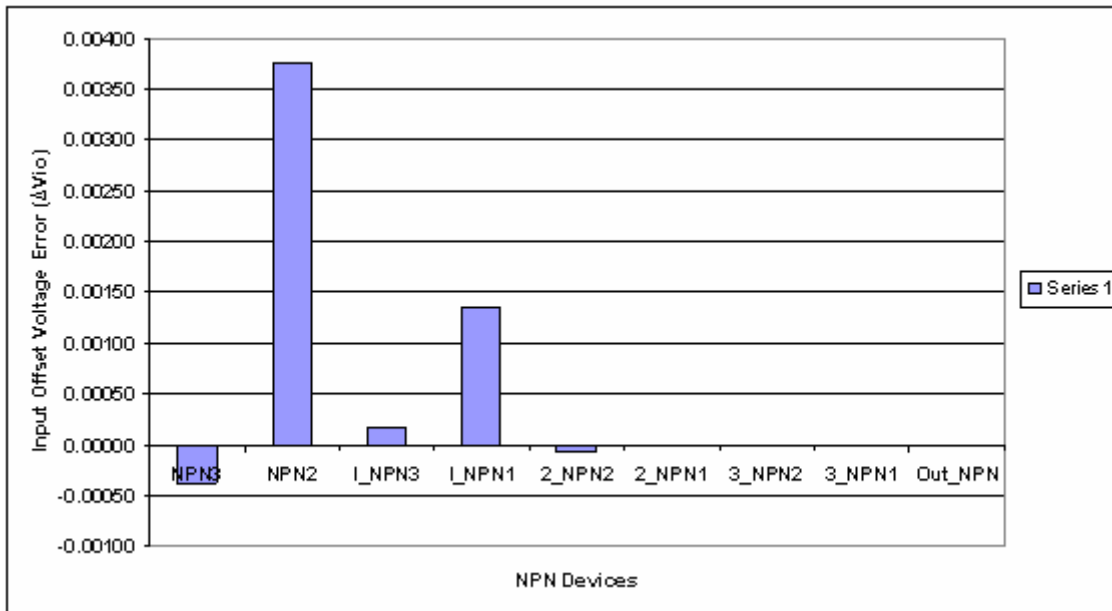


Figure 5.5 Input Offset Voltage Error contribution by individual NPN device for the circuit configuration in fig.5.4

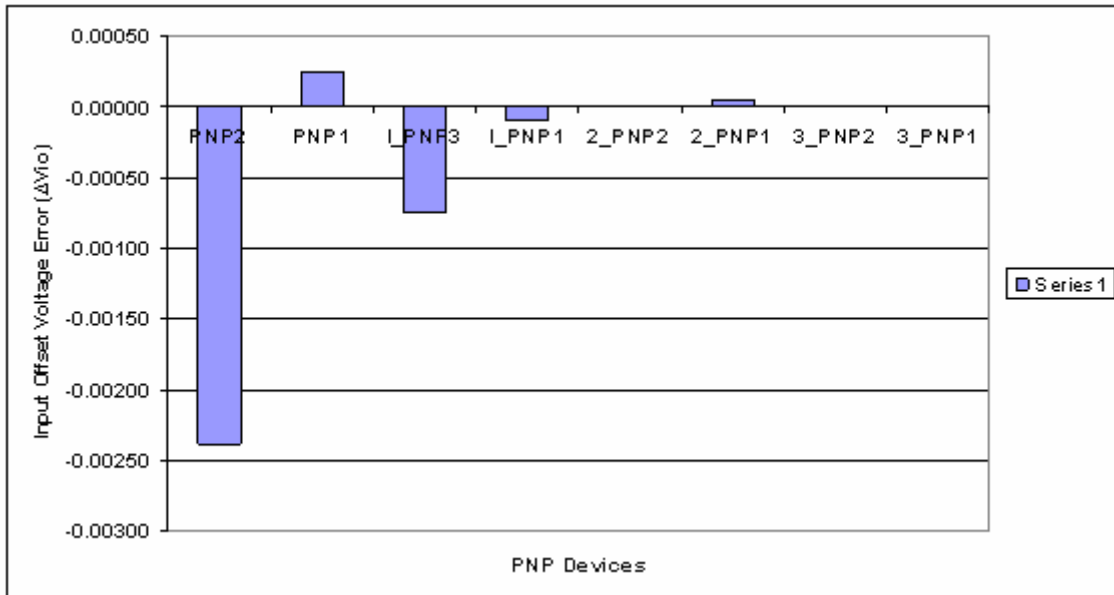


Figure 5.6 Input Offset Voltage Error contribution by individual PNP device for the circuit configuration in fig.5.4

Analysis of plots in fig.5.5 & fig. 5.6 along with the CFOA general schematic, fig. 4.4 and its test configuration in fig.5.4 shows that:

1. The input offset voltage error is mainly caused by the NPN2 and PNP2 devices.
2. These are the input devices on the non-inverting terminal. Since the non-inverting terminal is not in the feedback loop, these devices contribute the most to the input offset voltage error.
3. If the non-inverting terminal is connected in closed loop, similar results will be obtained with the input devices on the inverting terminal.

4. The input offset voltage error caused by the devices on stick2 to stick5 (output stick) is very small as compared to that caused by the input devices.

To verify statement no.1, the same circuit was simulated by turning self heating ON only for NPN2 & PNP2, with all other devices self turned OFF. The input offset voltage obtained with this simulation was observed to be -1.94 mV which is 98.48 % of the total input offset voltage (-1.97 mV) when all devices have self heating ON. This means that the two input devices NPN2 and PNP2 contribute 98.48 % of total input offset voltage due to self heating.

Turning only these two particular transistors self heating OFF results in input offset voltage of -0.59mV, close to the -0.52 mV, which is the value of input offset voltage with all the transistors self heating turned OFF. This shows that, turning self heating OFF for only NPN2 and PNP2 devices, almost eliminates the overall input offset voltage variation due to device self heating.

Reducing the self heating of NPN2 and PNP2, reduces the thermal tail of the overall input offset voltage. Hence reducing thermal resistance for these two input devices should result in the overall reduction of input offset voltage caused by device heating. Since the thermal resistance scales inversely with the area of the device, the emitter area of these two devices was increased by increasing the multiplication factor by 2. Simulations were carried out with self heating on for all other devices except these two. In this case the input offset voltage was reduced to -0.42 mV, demonstrating the effect of the area factor on the thermal tail of the input offset voltage.

From the design point of view increasing area might not be the best way, since this might cause a change in the multiplication factor of other devices too so as to maintain the desired specifications. Another way to decrease the thermal resistance for these particular devices is to increase the tub area (double in this case) of the enclosed in trench. This approach serves the purpose of reducing the input offset voltage without any other design changes.

5.3 Thermal characterization of Time Dependent Gain Error of CFOA

As observed in chapter 4, the output voltage of a CFOA varies with switching time. From the thermal simulations of the CFOA, it is seen that the device temperature also varies with the time. Both the output voltage and the device temperature settle down to a constant value after a few microseconds. Systematic thermal characterization of time dependent gain error change for a CFOA is a challenging area of study. Here the time dependent gain error analysis is done with the overall change in circuit temperature as well as with the change in device temperature. Time dependent gain error is different from the normal gain error term used for amplifiers which is equal to the reciprocal of return difference. Here analysis is carried out for time dependent gain error and for simplicity purposes it is referred as gain error.

The circuit configuration used for gain error analysis is shown in figure 5.7. A square wave input voltage of 4 V p-p, rise and fall time of 40 nsec and pulse width of 50 μ sec with 50 % duty cycle was used for transient simulations.

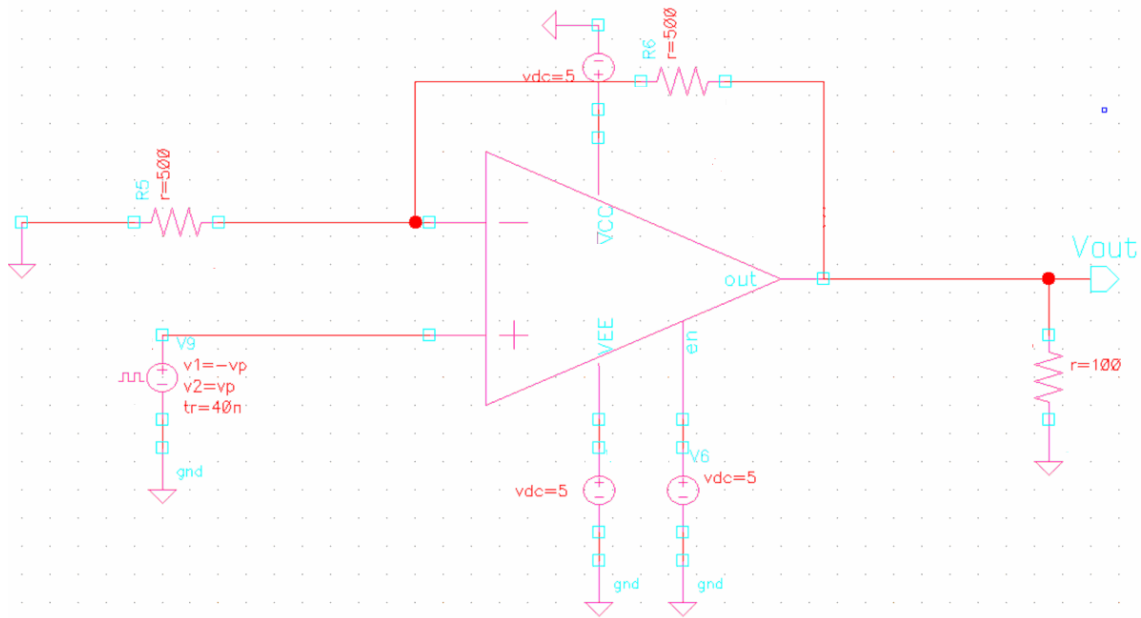


Figure 5.7 Simulation set up for thermal analysis of CFOA

5.3.1 Gain change of the CFOA with circuit temperature ($dA/dtemp$)

To observe the effect of the overall circuit temperature variation on the gain of CFOA, the schematic shown in fig.5.7 was simulated with self heating on for all the devices for a circuit temperature range of 25⁰ C to 40⁰ C. The circuit temperature was changed by changing the value of ‘temp’ in the analog design environment. The final (settled) values of the output voltages for the first positive and negative half cycle were noted. It was observed that the final output voltage values during the positive and negative half cycle of the input differs. The final voltage during the positive half cycle is denoted as Vout (+) and during negative half cycle as Vout (-). Analysis is mentioned for first positive half cycle. Corresponding to these settled values of voltages, gain

values during positive half cycle A(+) and negative half cycle A(-) were calculated for different circuit temperatures and plotted against the circuit temperature as shown in figure 5.8.and figure 5.9.

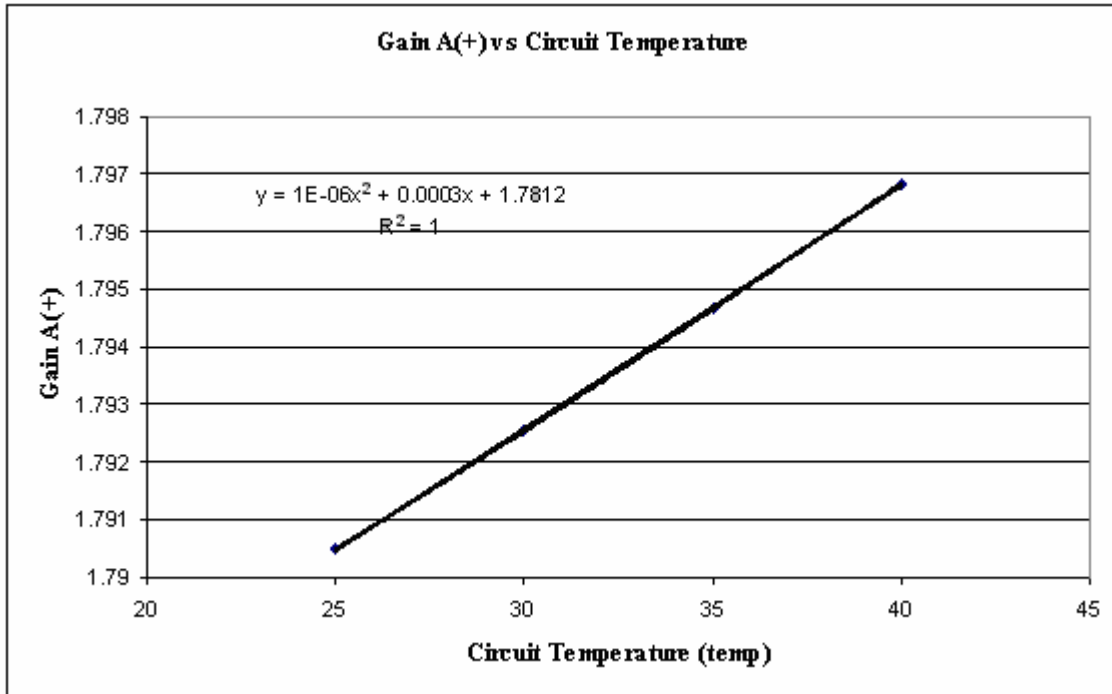


Figure 5.8 Variation of CFOA gain during positive half cycle A(+) with overall circuit temperature when all the devices are with self heating turned on

From fig.5.8 it can be seen that the gain A(+) as a function of circuit temperature can be expressed as

$$A(+)= -1E - 6 \times (temp)^2 - 0.0003 \times (temp) + 1.7812 \quad (5.1)$$

The value of gain at any circuit temperature in the range of 25⁰ C to 40⁰ C can be obtained by using equation 5.1 The gain change due to change in circuit temperature can be obtained by evaluating $dA(+)/dtemp$ at that particular temperature as explained below:

Differentiating equation 5.1 with respect to circuit temperature gives

$$\frac{dA(+)}{dtemp} = 2E - 6 \times (temp) - 0.0003 \quad (5.2)$$

Substituting temp = 27 in the above equation gives the value of $dA(+)/dtemp$ at 25⁰ C and was found to be 0.035 %.

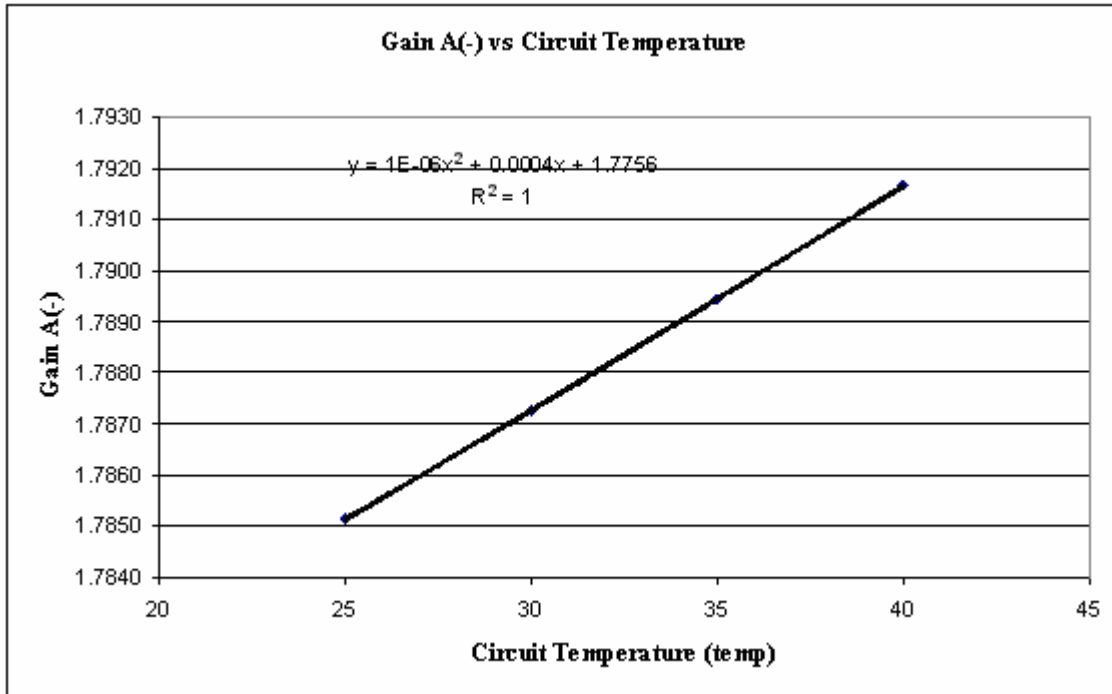


Figure 5.9 Variation of CFOA gain during negative half cycle A(-) with overall circuit temperature when all the devices are with self heating turned on

Similarly analysis for the negative half cycle at 27⁰ C gives $dA(-)/dtemp$ value as 0.045 %.

Hence the overall change in gain of the CFOA due to change in circuit temperature when all the devices selft turned on is 0.035% for the positive half cycle and 0.045 % for negative half cycle.

5.3.2 Device temperature change with Circuit temperature ($dT / dtemp$)

The initial hypothesis for the gain change with overall circuit temperature change is the delayed time response of self heating of each device in the CFOA. The self heating response results in a variation of the operating characteristics of the device. It is necessary to study the change in device temperature with overall circuit temperature change in order to have the rough estimate of device temperature change. Though the change is very small it can be of importance in some industry applications.

In order to study the device temperature change for each device, the CFOA circuit configuration shown in fig.5.7 was simulated with only one device with self heating turned on over a circuit temperature range of 25⁰ C to 40⁰ C. The final settled value of device temperature in positive half cycle is $T_i(+)$ and $T_i(-)$ in the negative half cycle (where i denotes the name of particular transistor). Both these values were noted for each circuit temperature case. A graph showing the variation of device temperature with overall circuit temperature during the positive half cycle for a particular device, NPN2 is shown in fig.5.10. Similar plots were obtained for all the devices constituting the CFOA.

It was observed that the change in device temperature is not constant over the entire range of circuit temperatures. The trend of device temperature change varies from device to device and hence not predictable. It is worthwhile to mention here that the device temperature change with circuit temperature during the positive half cycle differs from that during the negative half cycle. Hence the change in device temperature at a

particular circuit temperature can be best obtained by calculating the slope $dTi/dtemp$ during positive as well as negative half cycle at that temperature.

For convenience, data for all the cases have not been shown here but the similar analysis applies for calculating data for all the devices in both positive and negative half cycle of input voltage.

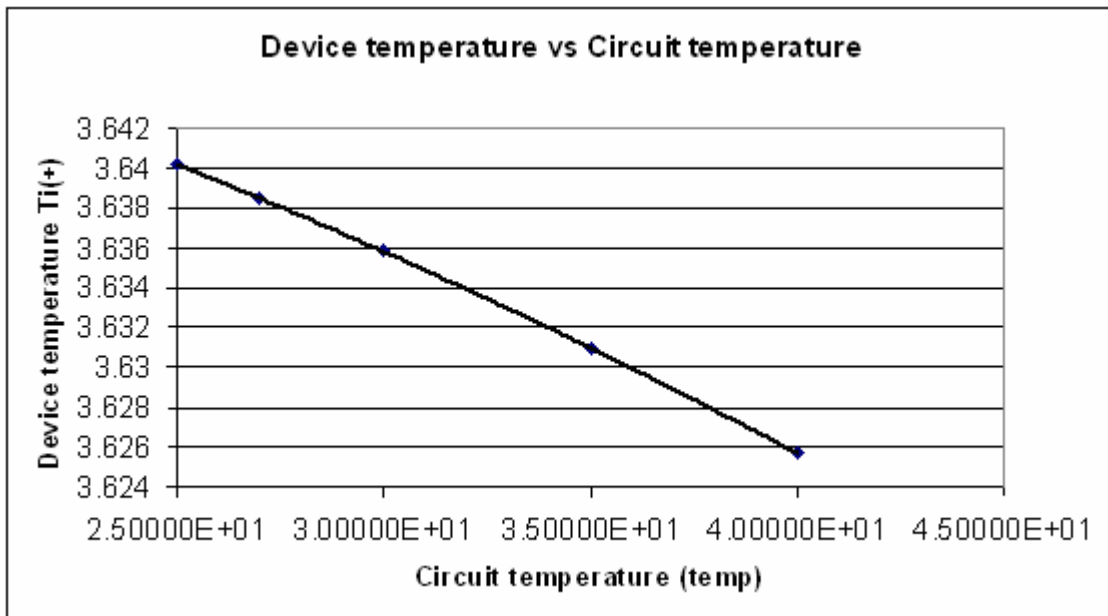


Figure 5.10 Temperature variation of NPN2 device with circuit temperature when only NPN2 is turned on with self heating

The device temperature of NPN2 in figure 5.10 as a function of circuit temperature can be expressed as

$$T(+)= -9.10062E - 6 \times (temp)^2 - 3.7872E - 04 \times (temp) + 3.65538 \quad (5.3)$$

and the change in device temperature with circuit temperature $dTi / dtemp$ can be obtained by differentiating above equation with respect to temp. For NPN2 this can be expressed as

$$\frac{dT_i(+)}{dtemp} = 2 \times (-9.10062E - 6) \times (temp) - 3.7872E - 4 \quad (5.4)$$

The value of $dT_i (+) / dtemp$ for the NPN2 device, at a circuit temperature of 27^0 C was calculated by substituting $temp = 27$ in equation 5.4. and found to be -0.00087. Similar procedure was followed to find $dT_i(+)/dtemp$ and $dT(-)/dtemp$ for all NPN and PNP devices of the CFOA, at a circuit temperature of 27^0 C. These values for the NPN and PNP devices are tabulated in tables 5.7 and 5.8.

Table 5.7 $dT/dtemp$ at 27^0 C for NPN devices

Transistor	$dT (+) / dtemp$	$dT (-) / dtemp$
NPN2	-0.000870	0.001991
NPN3	0.003719	0.002956
1_NPN1	0.004789	0.010102
1_NPN3	0.000570	0.000153
2_NPN1	0.023610	-0.000504
2_NPN2	0.000259	0.000018
3_NPN1	0.001569	0.019980
3_NPN2	0.014903	0.000423
Out_NPN	-0.001555	0.000001

Table 5.8 $dT/dtemp$ at 27^0 C for PNP devices

Transistor	$dT (+) / dtemp$	$dT (-) / dtemp$
PNP1	0.00178	0.00217
PNP2	0.00085	-0.00046
I_PNP1	-0.00021	0.00059
I_PNP3	0.00471	0.00243
2_PNP1	-0.00016	0.00028
2_PNP2	-0.00052	0.01543
3_PNP1	0.00016	0.01215
3_PNP2	0.00451	0.00089

Plots showing the change in device temperature with circuit temperature are shown in figures 5.11 and 5.12.

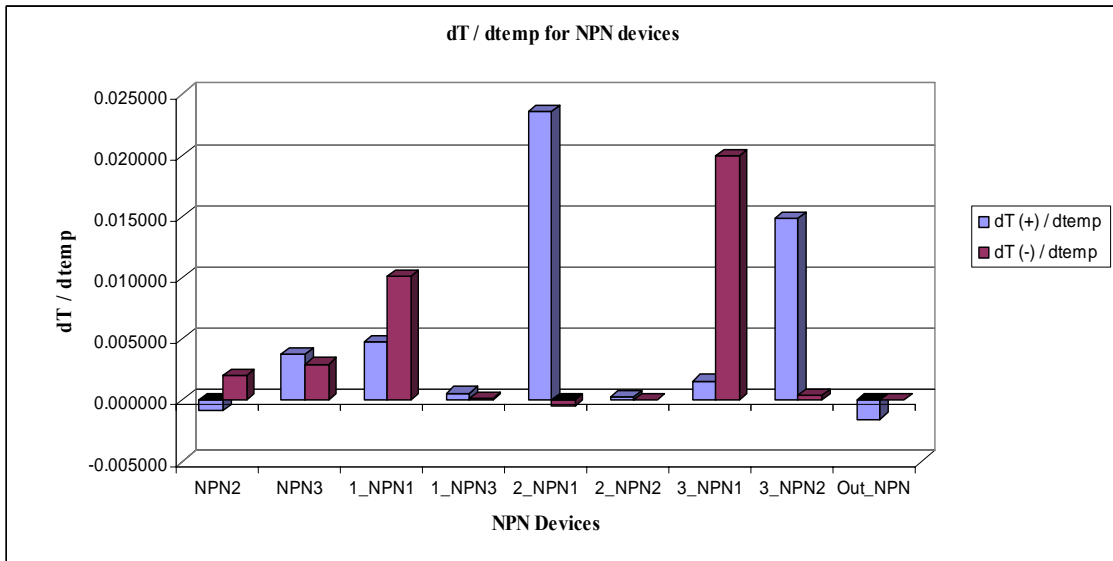


Figure 5.11 $dT / dtemp$ values for NPN devices during the positive and negative half cycle of input voltage

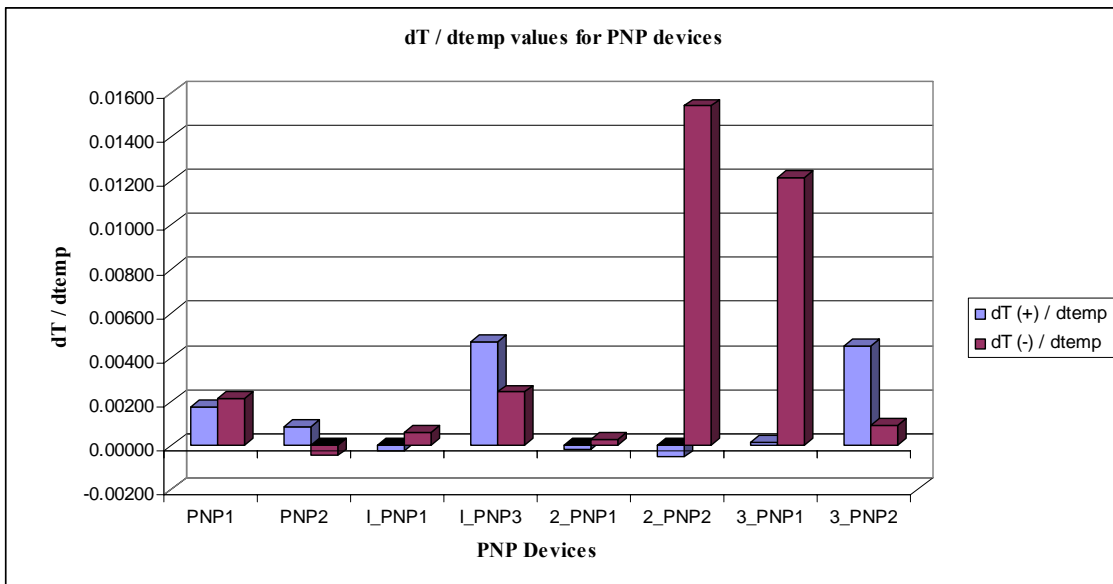


Figure 5.12 $dT / dtemp$ values for PNP devices during the positive and negative half cycle of input voltage

Close observation of figures 5.11 and 5.12 shows that

1. The maximum change in the device temperature due to a change in circuit temperature for NPN devices was observed during the positive half cycle of input voltage.
2. The maximum change in the device temperature due to a change in circuit temperature for PNP devices was observed during the negative half cycle of input voltage.
3. The maximum $(dT(+)/dtemp)$ of the NPN devices is for 2_NPN1 which is one of the NPN devices on high impedance stick driving output stage.
4. The maximum $(dT(-)/dtemp)$ of the PNP devices is for 2_PNP2 which is one of the PNP devices on high impedance stick driving output stage.
5. The thermal analysis in chapter 4 showed that, with all the transistors with self heating turned on, the 2_NPN1 and 2_PNP2 are the devices with the maximum temperature rise during the positive and negative half cycles respectively.

5.3.3 Gain change with device temperature variation (dA/dTi)

As observed previously both the gain of CFOA and device temperatures, are functions of time and circuit temperature. In previous sections we discussed the variations of CFOA gain and device temperature with change in overall circuit temperature. In an attempt to co-relate the gain error change to the effects caused by thermal variations, the time dependent gain error contributed by each device temperature rise was studied.

To study the gain error contributed by each device as its own temperature varies, dA/dT_i , the set up shown in fig.5.7 is simulated with selft on only for a particular device. The time dependent output voltage and device temperature values were exported from cadence to MS excel for data analysis. The gain error was calculated as

$$dA = \frac{V_{out}(t) - V_{out}(Final)}{V_{in}} \quad (5.5)$$

and Gain error due to variation of particular device temperature

$$\frac{dA}{dT_i} = \frac{dA}{\text{Change In Temperature Rise Of the Device}} \quad (5.6)$$

Using equation (5.6), the dA/dT_i values for all the devices during both positive and negative half cycle were calculated. Table 5.9 and 5.10 lists these values expressed in percentages, for NPN and PNP devices respectively. The plots showing the percentage variation of $dA(+)/dT_i$ and $dA(-)/dT_i$ for both NPN and PNP devices in the CFOA are shown in fig.5.13 and 5.14 respectively.

Table 5.9 Percentage Gain error due to variation of device temperature, for NPN devices.

Transistor	% $dA(+)/dT_i$	% $dA(-)/dT_i$
NPN2	-0.121065708	0.099281716
NPN3	0.02544877	-0.020713914
1_NPN1	0.098485363	-0.119018929
1_NPN3	-0.000196909	0.007982375
2_NPN1	0.000104104	-0.011314547
2_NPN2	0.019087229	0.025167906
3_NPN1	-0.000359648	-0.05714897
3_NPN2	0.003596475	0.025999672
Out NPN	-0.045394583	0

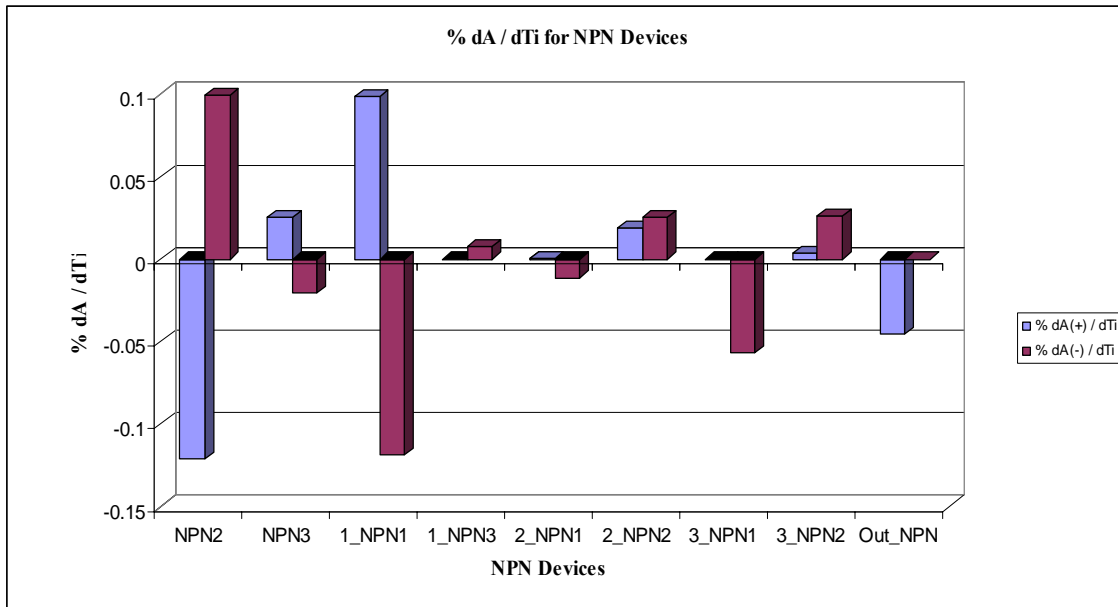


Figure 5.13 Percentage Gain error due to variation of device temperature (NPNs), during positive and negative half cycle of input voltage

Table 5.10 Percentage Gain error due to variation of device temperature, for PNP devices.

Transistor	% dA(+) / dTi	% dA(-) / dTi
PNP1	0.022658011	-0.023803784
PNP2	-0.116678718	0.117256938
1_PNP1	-0.010466231	0.03796283
1_PNP3	0.133764574	-0.102395226
2_PNP1	-0.028202305	-0.036512341
2_PNP2	0.003760657	-0.000618508
3_PNP1	-0.005099819	-0.000775896
3_PNP2	0.056273194	0.000652918

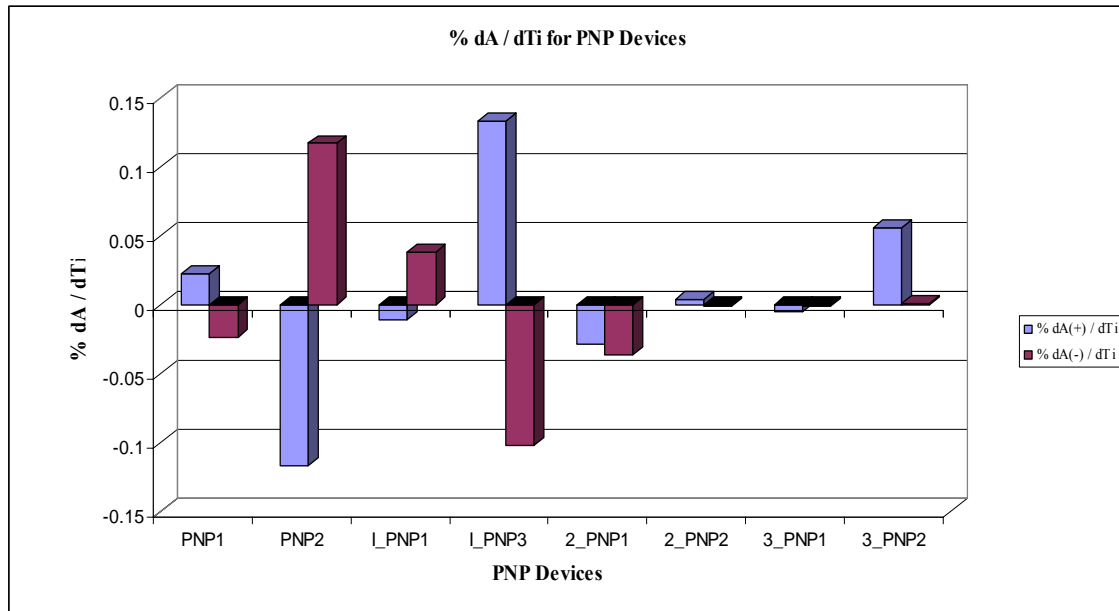


Figure 5.14 Percentage Gain error due to variation of device temperature (PNPs), during positive and negative half cycle of input voltage

From plots of figures 5.13 and 5.14 it is clear that the gain error change due to variation in device temperature is significant for NPN2, PNP2, 1_NPN1 and 1_PNP1. These are the devices on the non-inverting and inverting input terminals respectively. Gain error caused by the devices on stick2 to stick5 is negligible as compared to that caused by devices on the input sticks. So the input devices are those which contribute the most to gain error. These are the same devices which caused maximum input offset voltage change as was proved by thermal characterization of the input offset voltage.

CHAPTER 6

INTER-DEVICE HEATING MEASUREMENT

In addition to self heating, inter-device heating is also an important phenomenon in high density chips. In order to model the inter-device heating effect using the extrinsic VBIC model as in chapter 2, it is necessary to have real time measurement data for the thermal coupling amongst the adjacent devices. The first section of this chapter lists the different test structures designed to study thermal coupling. The second section presents the apparent temperature measurement configuration. The third section gives details about the hardware and software tools used for the measurement and describes the measurement procedure. Results of the measurements are discussed in the last section of the chapter.

6.1 Test Structures for Thermal Coupling Measurements

Each of the VCVS in the extrinsic VBIC model of figure 2.8 has a gain equal to the coupling coefficient for heating between two adjacent devices. Hence to incorporate this model in simulators like Spectre or SpectreS, it is essential to have measured data for thermal coupling. The thermal coupling or inter-device heating depends on the a) number of adjacent devices b) spacing between the devices c) nature of shared wall and d) operating conditions of the adjacent devices. To consider the effect of all these parameters on thermal coupling of DIBJTs various test structures were developed using the National Semiconductor VIP10 process. These test structures were named as

UTA184, UTA185, UTA189 and UTA190 and are explained in detail here. UTA204 and UTA205 are the modified versions of UTA184.

6.1.1 UTA184 and UTA189 test structures:

The UTA 184 test structure is mainly designed to study the effect of spacing on the inter-device heating for NPN devices. Figure 6.1 shows one of the three setups laid in this structure. As can be seen from this schematic, it consists of four parallel connected transistors and a single transistor.

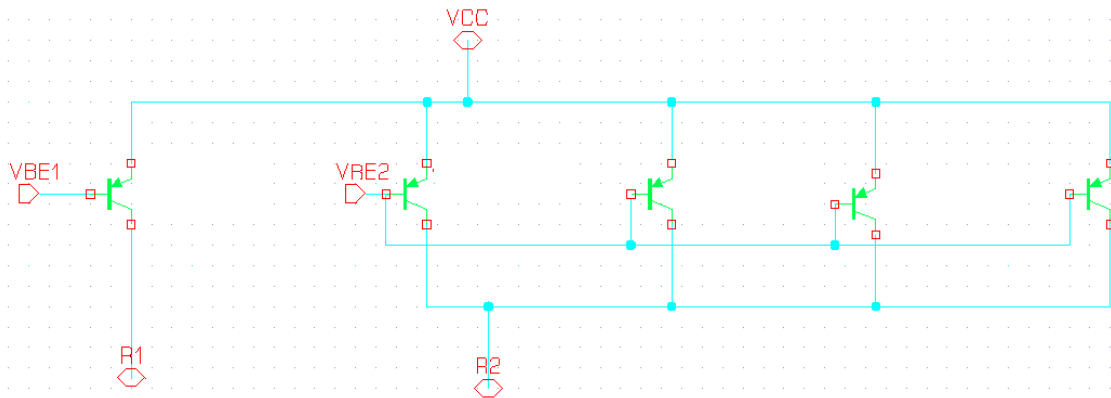


Figure 6.1 Part of UTA184 Schematic

The emitters of all the transistors are connected together. The base, collector and emitter are made available for external connections. Figure 6.2 shows the pin out diagram for the final layout for the UTA184 test structure. It can be seen from the layout that it has three main set-ups. Each set-up has the central device (single transistor) surrounded by four outer devices (parallel connected transistors). The only difference among the three set-ups is the spacing between the devices. The minimum device spacing available in the VIP10 process is 2 μm . The first set-up has 2 μm

spacing and is 5 μm and 11 μm for second and third set-ups respectively. The test structure was put into a DIP14 package by National Semiconductor.

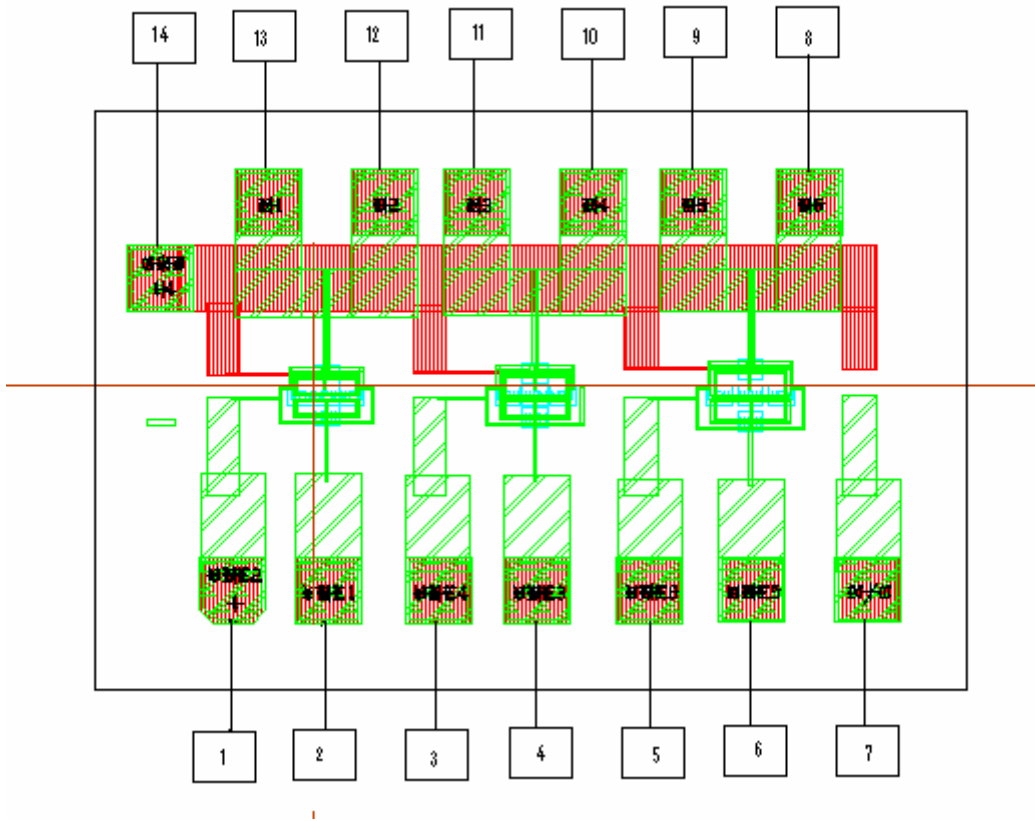


Figure 6.2 Pin out with final layout for UTA184

UTA189 is designed for PNP devices on the same basis as of UTA184. In case of UTA 189, it has device spacing of 2 μm and 5 μm for two set-ups. In addition to this, an isolated NPN and PNP device are also laid out on the same structure as shown in the layout of UTA 189 in figure 6.3.

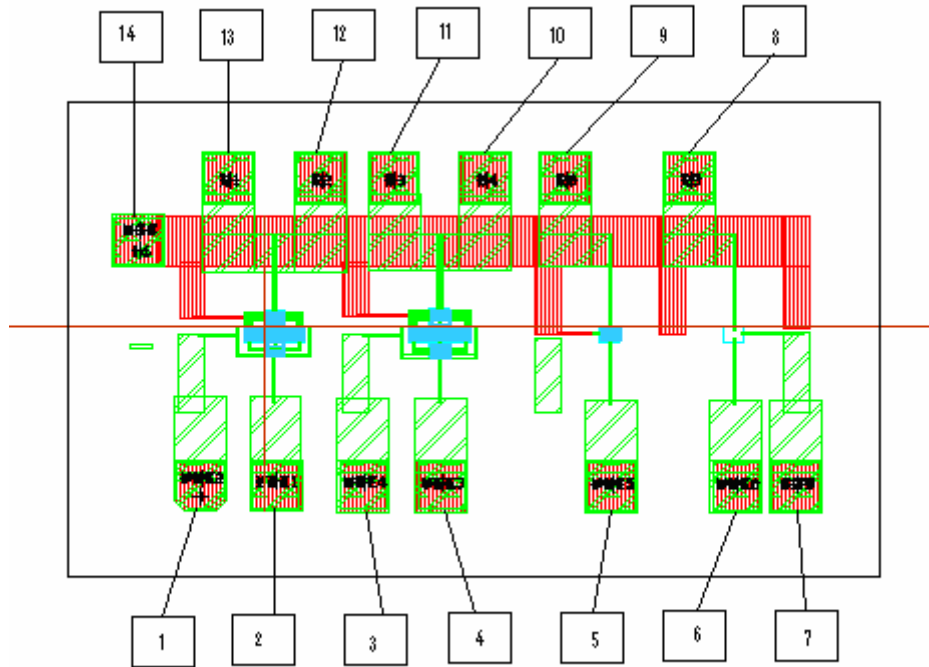


Figure 6.3 Pin out with final layout for UTA189

6.1.2 UTA185 and UTA190 test structures:

UTA185 is designed basically to study the effect of adjacent devices on inter-device heating for the NPN device. UTA 190 is designed with PNP devices. The number of adjacent devices varies from one to three. The spacing between the devices used in all the cases for these structures is $2\ \mu\text{m}$. As in case of UTA 184 and 189 here also the emitters of all the devices are shorted together. The bases, collectors and emitters of central as well as outer devices are made available for external connections. Figure 6.4 and 6.5 shows the pin out diagrams with layouts for UTA 185 & UTA 190 respectively. Both these structures were fabricated by National Semiconductor in DIP 14 package.

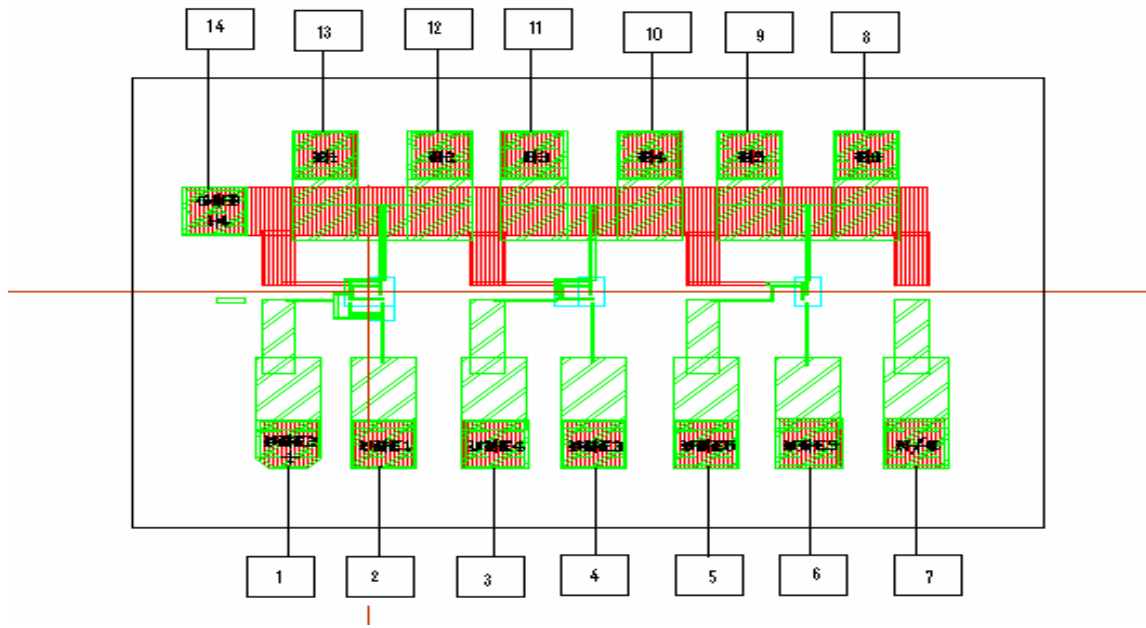


Figure 6.4 Pin out with final layout for UTA185

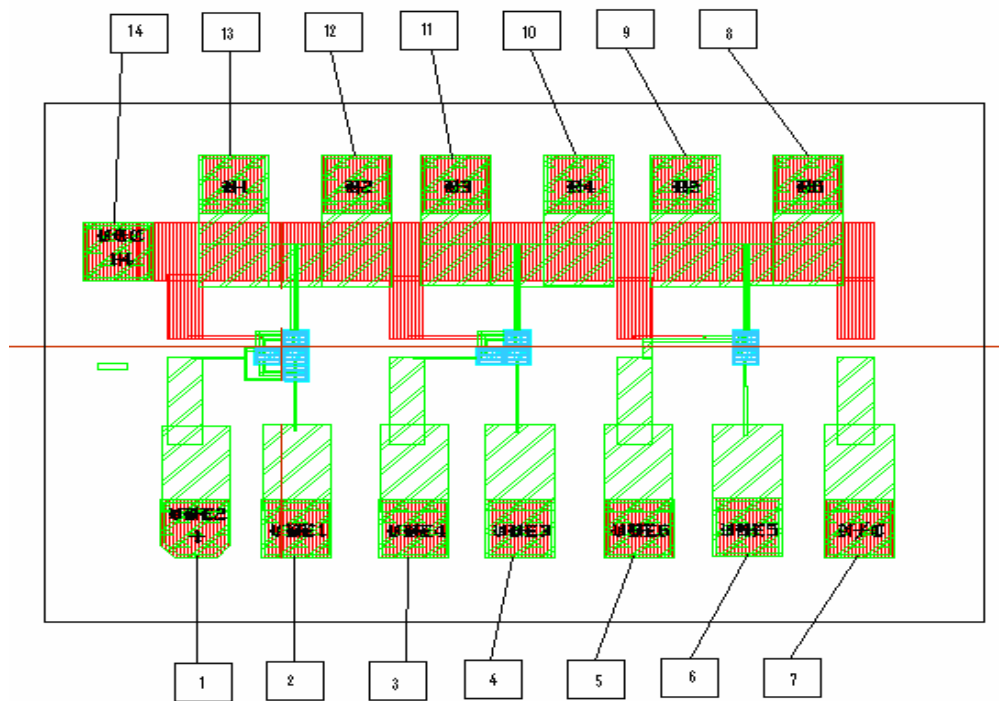


Figure 6.5 Pin out with final layout for UTA190

6.1.3 UTA 204 & UTA 205 test structures:

As can be observed in all the layouts, the emitters of the central device and outer devices are connected together at a single pad connection. To avoid ground currents flowing in the emitters, it is necessary to provide separate pads for the emitters of the outer devices and the central device. This modification was implemented in the UTA 204 and UTA205 test structures. UTA204 and UTA205 consist of part of UTA184 design with separate pads for the emitters of the central device and outer devices. In both the designs the central device is surrounded by four outer devices with a minimum spacing of 2 μm . In addition to this set up isolated NPN and PNP transistors are also laid out on the same chips. The layout diagram for both these test structures is shown in appendix A.

6.2 Configuration for Apparent temperature measurement of BJT

The temperature of a device can be evaluated from its forward Gummel voltage and current data. The forward Gummel arrangement for a BJT is shown in figure 6.6.

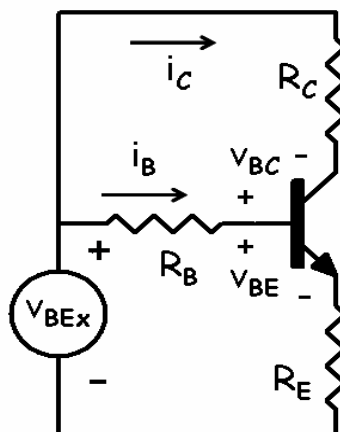


Figure 6.6 Forward Gummel configuration for an intrinsic transistor with its internal resistances

In forward Gummel set up, the base and emitter of the BJT are shorted together and kept at constant D.C. voltage. The base emitter voltage is varied linearly. The ideal plot for the base and collector current vs base emitter voltage in this configuration is shown in figure 6.7. Base current I_b and collector current I_c are plotted on log scale. At low V_{be} voltages the base current is more than the collector current due to recombination taking place in base-emitter junction. At high voltages the collector current is higher due to the high level injection. The maximum value of β occurs in the V_{be} range between these two limits. The base and collector current values in this V_{be} range can be used for the temperature measurement of the particular BJT. The temperature of a device can be evaluated from the forward Gummel data using equation 6.1.

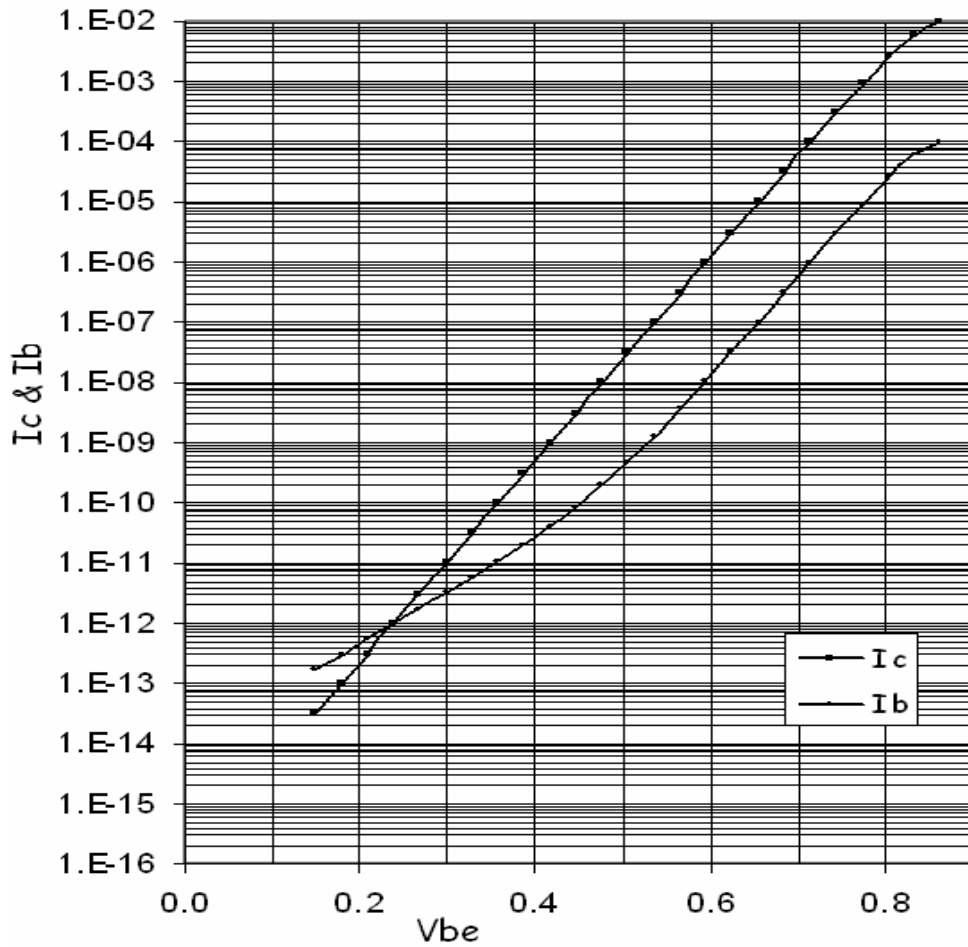


Figure 6.7 Ideal forward Gummel plot

For maximum β range, temperature of device can be evaluated as

$$T \approx \frac{q \times d[Vbe]}{N \times K \times d[\ln(Ic)]} \quad (6.1)$$

In the above equation except for V_{be} and I_c all other quantities are constant. Hence for temperature calculation it is necessary to measure the variation in I_c with V_{be} in the maximum β range. Since the temperature calculation involves derivative over the range of V_{be} , the minimum value of the temperature in this range can be taken as the

apparent temperature of the device. The apparent temperatures of the devices were measured using the forward Gummel setup.

The test structures used for thermal coupling measurement had the central device surrounded by the outer devices. To measure the thermal coupling or inter-device heating, it is necessary to measure the change in temperature of the central device with the variation in the power on the outer devices. Figure 6.8 shows the configuration used for the thermal coupling measurement.

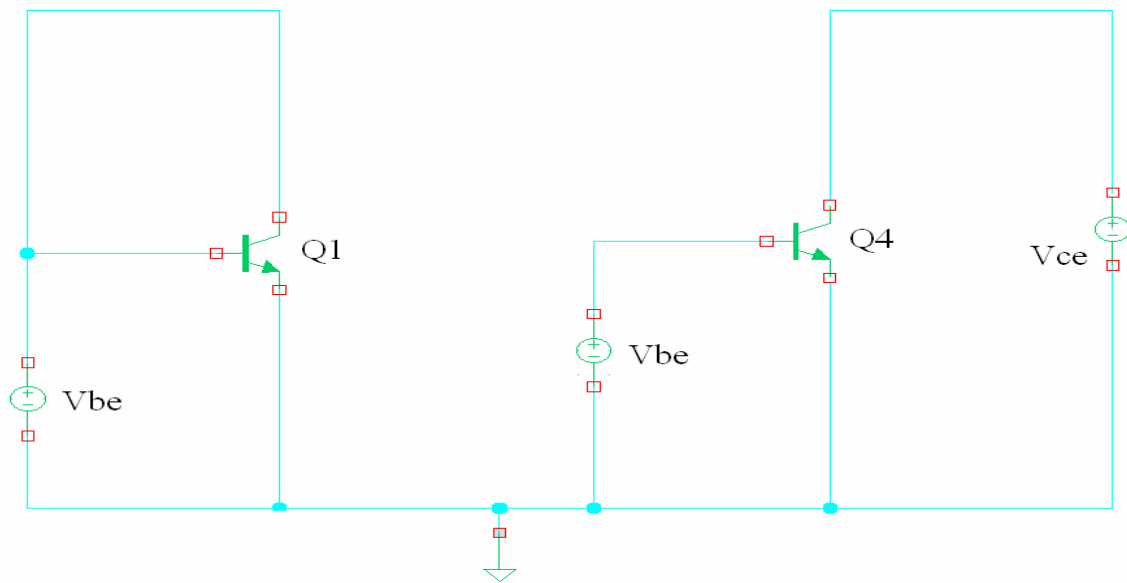


Figure 6.8 Configuration for thermal coupling measurement

In the figure 6.8 transistor Q represents the central device and Q4 represents parallel connected four outer devices. The central device is connected in the forward Gummel set up for temperature as explained before. The outer devices are excited with a constant Vbe. The power on the outer devices can be increased by increasing the Vce gradually within the device specifications. With changing Vce on the outer devices,

collector current and hence power on the outer devices will change. The power on these devices can be computed as

$$P = (V_{be} \times I_b) + (V_{ce} \times I_c) \quad (6.2)$$

With this varying power on the outer devices the apparent temperature of the central device can be obtained from its forward Gummel data. A graph of power vs temperature can then be plotted giving a display of the heating of the central device due to power on the outer devices. The slope of the graph gives the thermal coupling between the central device and the outer devices. The actual measurement set up and measurement procedure using HP 4142B Modular DC Source/Monitor [15] and IC-CAP interfaced evaluation system is explained in later sections of the chapter. The next section describes about the hardware and software tools used for the measurements.

6.3 IC-CAP / HP IB interfaced Evaluation system

The forward Gummel data is required for computing the apparent temperature of the central device. Voltage and current data for the outer devices is used to calculate the power on these devices. This data was obtained by using IC-CAP / HP IB interface system. This system consists of a HP 4142B DC Source/Monitor unit interfaced with IC-CAP software. The source and monitoring units of the HP 4142B can be controlled through IC-CAP. These tools are explained in detail next.

6.3.1 HP 4142B Modular DC Source/Monitor:

HP 4142B is a high performance DC parameter measurement instrument which has the facility of sourcing as well as monitoring both the voltage and the current. It has overall four SMUs (Source and Monitoring Units) and one GNDU (Ground Unit).

These SMUs are denoted as SMU1, SMU2, SMU4 and SMU6 on the HP4142 B front panel. Out of these four SMUs, SMU1 and SMU2 are medium power SMUs. SMU4 and SMU6 are high power SMUs. The medium power SMUs (SMU1 and SMU2) can force and measure voltages up to 100 V and currents up to 100 mA (independent of polarity). Power up to 2 W can be supplied by these SMUs. The high power SMUs can force and measure voltages up to 200 V and currents up to 1A. They can supply power up to 14 W. The Ground unit (GNDU) is a 0 V constant source that provides a measurement ground reference and can sink current up to 1.6 A. Table 6.1 lists the main features of the HP 4142B.

Table 6.1 Features of HP 4142B.

	Current	Voltage
Measurement Range	0 to 10 A	0 to 200 V
Resolution	20 fA	4 μ V
Speed for measure/force	4 ms	4 ms
Accuracy	0.2 %	0.05 %

A 14 pin zero insertion force (ZIF) socket was soldered on PCB (Printed Circuit Board) in which the 14 pin test structure packages fit. Connections were taken out from each pin. All the four SMUs as well as the GNDU connections are brought from the HP 4142B front panel to a socket board using quadraxial cables. For all the SMUs the force and guard wires are shorted together and connected to the GNDU terminal. For the GNDU, all the force, sense and guard connections are shorted together. The sense

terminal of all the SMUs and GNDU were made available for connection on the PCB (Printed Circuit Board) using BNC cables with alligator clips.

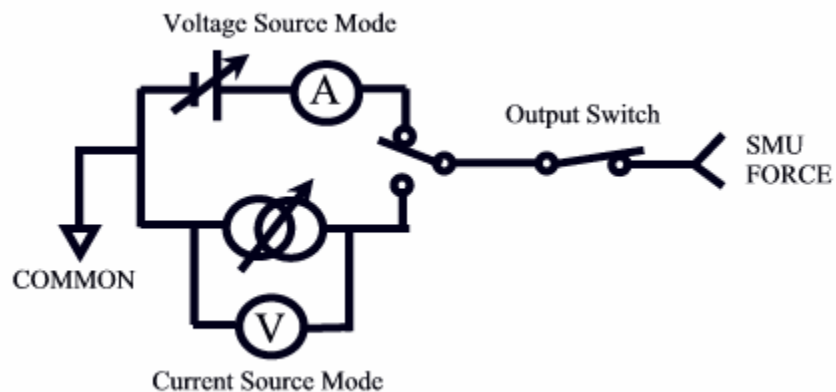


Figure 6.9 Simplified SMU (Source/Monitoring Unit) Circuit Diagram [15]

Each of these SMUs can be used either as a voltage or current source as shown by the simplified connection of one of the units in figure 6.9. SMUs can be controlled by using a computer connected through the interfacing card. The IC-CAP tool was used to control the SMUs of the HP 4142B. The HP 4142B calibrates itself when it is first turned on. After the self calibration it can be added in the instrument list from IC-CAP and can be used for controlled measurements through IC-CAP.

6.3.2 IC-CAP tool:

The HP 4142B was interfaced with a computer and was controlled with the IC-CAP tool. IC-CAP was mainly used for a) controlling all the four SMUs and GNDU units b) setting the devices in different configurations, c) evaluating different transforms and d) data analysis using graphs.

The HP 4142B was connected through the interfacing card to the computer and was added in the instrument list of the IC-CAP. The SMUs and GNDU can be connected to different pins of the package depending upon the appropriate configuration. The same configuration can be set up in the “Device Under Test (DUT)” set up. The voltage, current and the compliance limits for each SMU can be mentioned along-with the particular mode for which the SMU will be used. The compliance limits help to make sure that the DUT is not damaged by exceeding current or voltage. After specifying the compliance limits and the modes for all the SMUs measurement can be carried out using the measure command.

IC-CAP can be effectively used for analyzing the data resulting from the measurements. Different transforms can be written using mathematical operations and can be plotted on graphs. Various options are available for data analysis as well as for graphical presentation. Apparent temperature plots were obtained by writing the transform for it as in equation 6.1 with the variable values replaced by the measured values obtained during the measurement process. This reduces the time for calculating the value of the apparent temperature each time after measurement. In addition to the graphical representation same data is also available in tabular formats for analysis. Data and graphical analysis was used to for the thermal coupling measurement.

6.4 Measurement set-up and procedure for thermal coupling measurement

This section explains the actual measurement set up used for the thermal coupling measurement with the HP 4142B / IC-CAP interface. The measurement setup and procedure is described in this section.

6.4.1 Measurement set up for thermal coupling measurements:

A fourteen pin ZIF socket was soldered to the PCB board on which the 14 pin package fits. The SMUs were connected to various pin connections of the ZIF socket. The arrangement showing the connections of SMUs and GNDU of HP 4142B to the transistor connections is shown in figure 6.10.

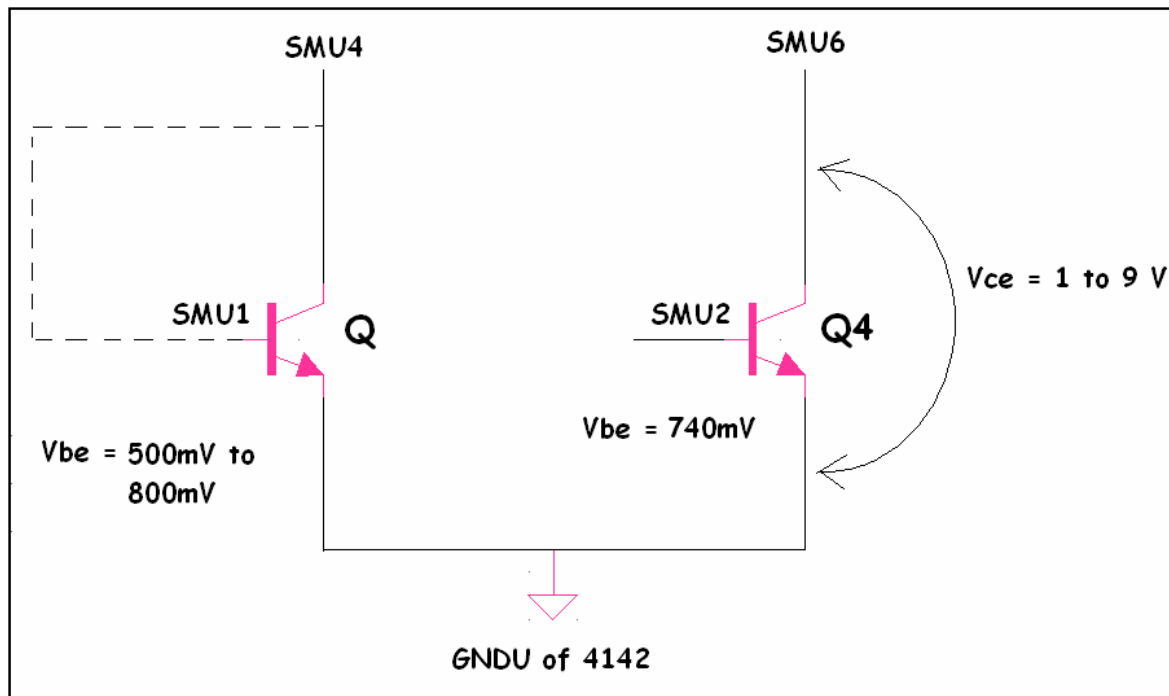


Figure 6.10 Measurement set up showing the connections of SMUs and GNDU

The emitters were held at zero potential by connecting them together to the GNDU. The base of Q4 was kept constant at 740 mV using SMU2 and the power on Q4

was varied by varying V_{ce} from 1 V to 9 V using SMU6. The central device, Q, was connected in the forward Gummel arrangement by holding SMU1 and SMU4 at the same potential. This was achieved by using the synchronous command in IC-CAP. The base emitter voltage of the central device was varied in the range of 500 mV to 800 mV by varying the voltages on SMU1 & SMU4 simultaneously. The base and collector currents of Q4 were measured using the SMU2 and SMU6.

6.4.2 Measurement Procedure:

The following steps describe the general procedure for the measurement of thermal coupling:

1. Log-in to the computer and start ICCAP.
2. Switch on HP 4142B. Wait until the self calibration of the HP 4142B is finished. Completion of self calibration is indicated by the “0” on display.
3. Add HP 4142B in hardware list of IC-CAP and configure its Source/Monitor units.
4. Create a new DUT set up and specify the SMU connections as shown in figure 6.10. Mention the appropriate voltage/current to be applied on each SMU and also make sure that the compliance on each SMU is well within the specifications of the device.
5. To start with, keep the integration time, hold time and set up time with their default values. Also the voltage step (ΔV_{be}) for V_{be} sweep of central transistor can be taken arbitrarily.
6. Write the appropriate transform for temperature in transform window.

7. Connect the alligator clips to the appropriate connections on the PCB.
8. Turn off the light in the measurement room to minimize photo-generation and close the door to avoid noise.
9. After the set-up is ready, measure the set-up using the “Measure” command of IC-CAP.
10. Upon finishing the measurement check the forward Gummel plot of the central device as well as the output characteristics of the outer devices to make sure that the devices are working correctly.
11. Noise in the measurement can be removed by robust connections, setting longer integral time and increasing the hold and set up times.
12. Carry out the measurements until the noise is overcome in the measurement.
13. Execute the temperature transform and plot the temperature against the V_{be} of the central device.
14. Noise can be seen in the temperature plot since it is evaluated using a derivative. Noise can be reduced by using optimized values of set up time, ΔV_{be} .
15. Carry out the measurements until the noise is minimized. The same optimized values of the hold time, set up time and ΔV_{be} should be used throughout the measurements.
16. The minimum value of the temperature obtained from the execution of the transform over the range of V_{be} can be taken as the apparent temperature of the central device.

17. Note down the base, collector currents and voltages of the outer devices for the particular set of the measurements. Power on the outer devices can be calculated by using equation 6.2.
18. Increase the power on the outer devices by increasing the collector voltage, and measure the apparent temperature of the central device.
19. Note the measurement values of the all the quantities mentioned above for each reading and tabulate them in an excel file for further data analysis.
20. Carry out the same procedure on each chip at least thrice as the results might vary due to aging effects.
21. After finishing the measurement, disconnect the alligator clips from the PCB board, turn off the ICCAP section and the HP 4142B and remove the chip from the socket.

The above procedure was followed for the thermal coupling measurement. The results of the measurement are discussed in the next section.

6.5 Measurement Results & Discussion

Thermal coupling measurements were carried out on UTA184 which consisted of a central device surrounded by four adjacent devices with a minimum spacing of 2 μm . All the set-ups on other test structures were checked for their functionality. This section presents the measurement results.

6.5.1 Measurement results with forward Gummel configuration:

To start with, measurements with forward Gummel configuration as shown in figure 6.6 were carried out for the central device as well as for the outer devices. The measurements were carried out independently. Figure 6.11 shows the measured forward Gummel plot for the central device.

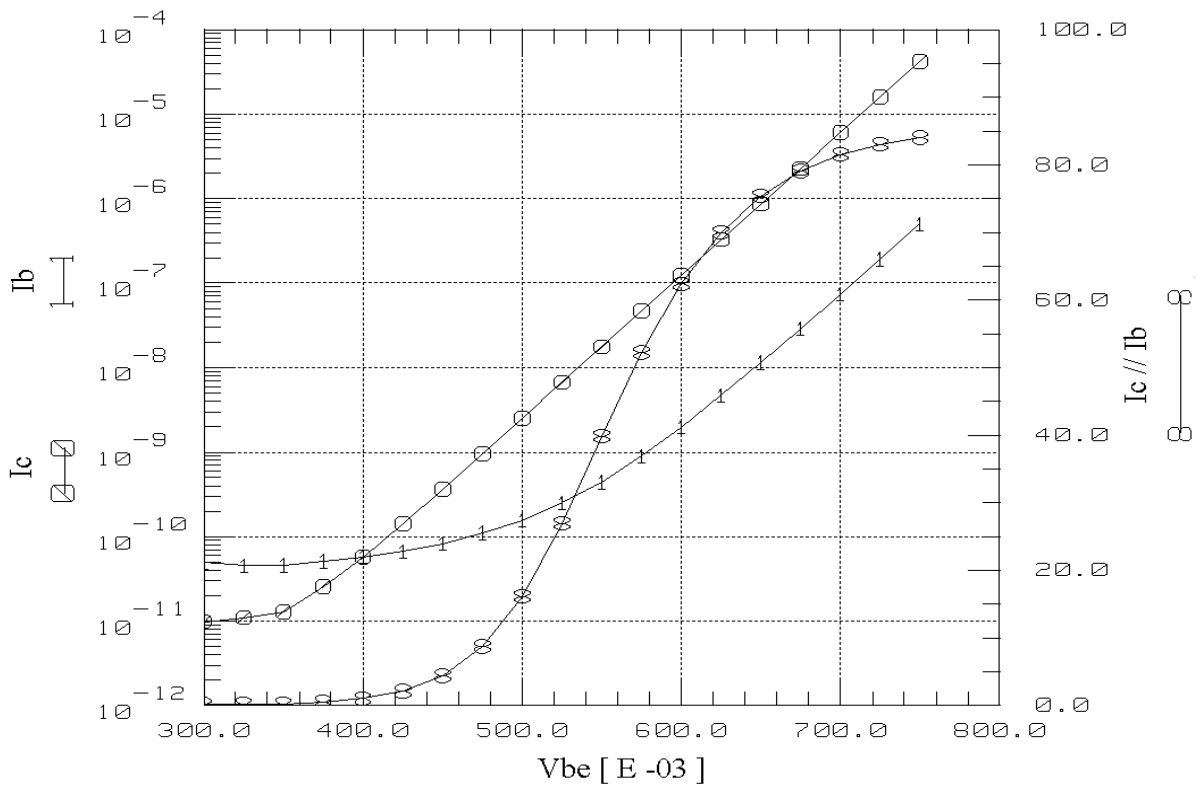


Figure 6.11 Measured forward Gummel plot for the central device

The graph shows, at small V_{be} , base current dominates the collector current due to recombination. I_c , I_b data at low V_{be} contains noise and hence the lower limit for the measurement was set to be 300 mV. At higher values the base as well as collector current increases due to high level injection. Since the base current exceeds the

compliance limits on the SMU, the maximum limit on V_{be} was set at 750 mV. Therefore the range of V_{be} used for forward Gummel measurement was 300 mV to 750 mV. The maximum value of β varies among the chips among was observed to be in the range of 70 to 89.

Similar measurements were carried out with outer devices in forward Gummel configuration. Figure 6.12 shows the forward Gummel plot for the outer devices. As mentioned previously the outer devices consist of four parallel connected transistors. The functionality of the central device as well as the outer devices was verified by taking the ratio of the currents in the outer devices and the central device. It was confirmed that the current ratio is 4 which is equivalent to area ratio for the central and outer devices.

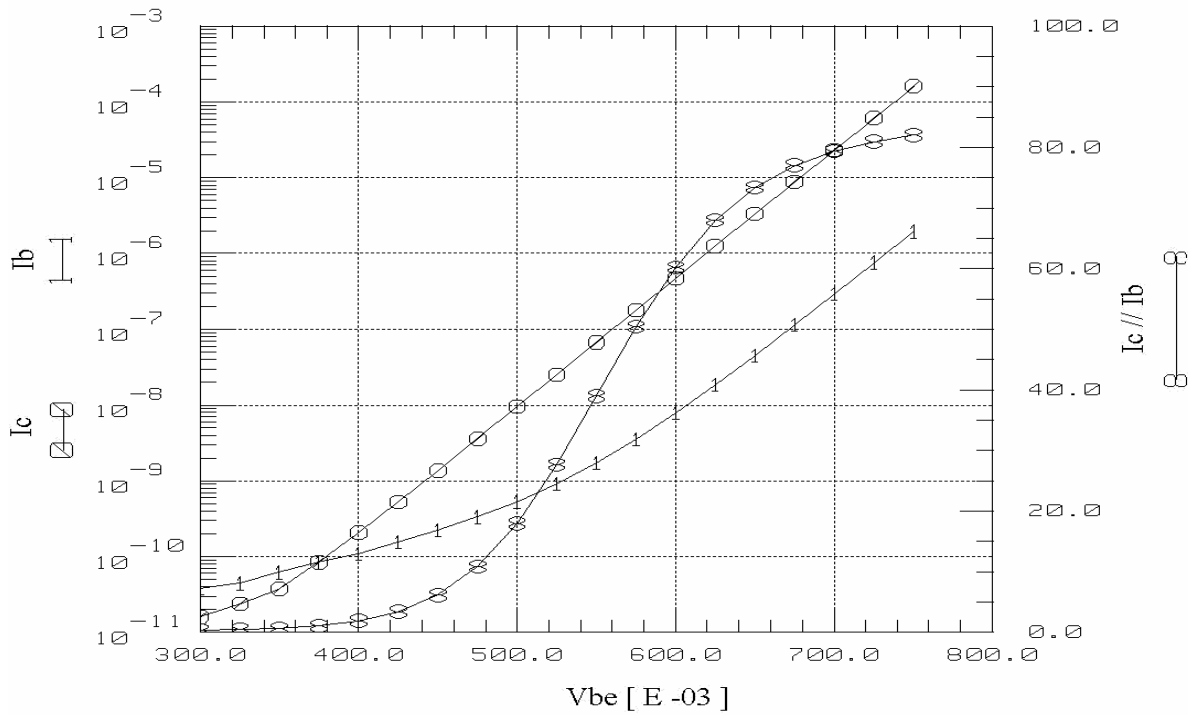


Figure 6.12 Measured forward Gummel plot for the outer devices

6.5.2 Measurement results for inter-device heating:

After checking the proper working of all the devices, the configuration as shown in figure 6.10 was used for thermal coupling or inter-device heating measurement. The outer devices were powered up at with constant V_{be} and V_{ce} . The temperature on the central device was evaluated using equation 6.1. The power on the outer devices was increased by increasing the V_{ce} and the temperature of the central device was plotted against the V_{be} of the central device in each case. Forward Gummel measurements were carried out on the central as well as outer devices to make sure that the devices were not burned out due to excessive current or voltage. Figure 6.13 shows the plot of temperature of the central device vs the base emitter voltage for a constant power on the outer devices.

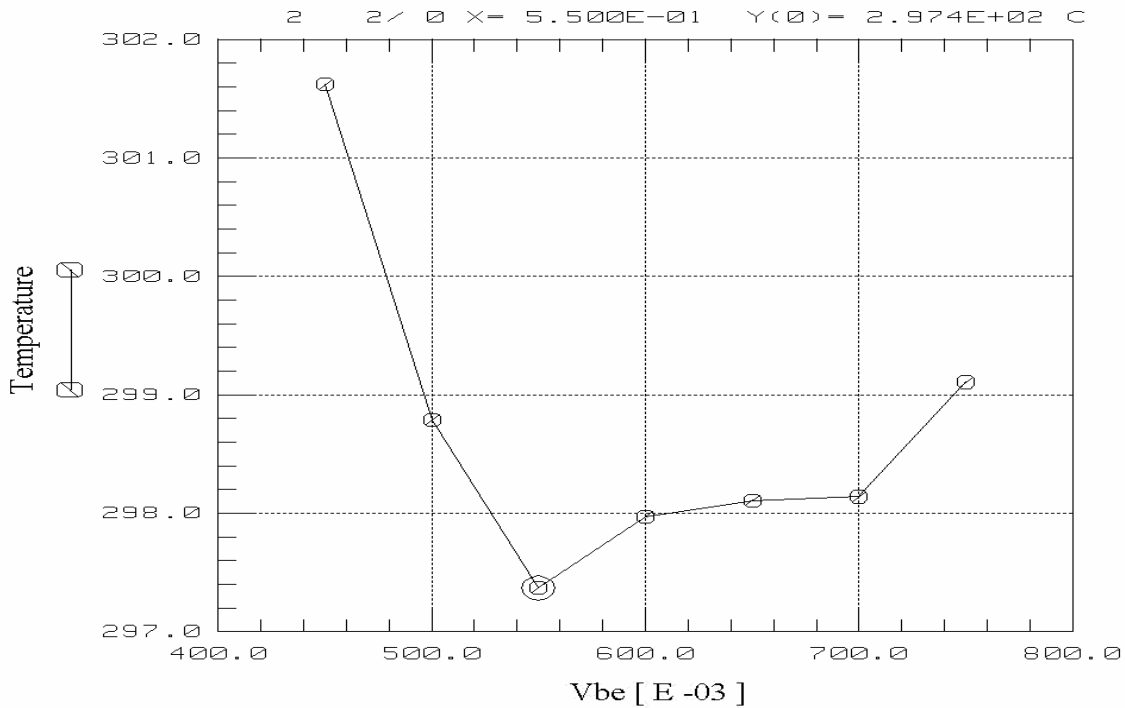


Figure 6.13 Temperature of the central device with constant power on the outer devices

The temperature of the device over the range of V_{be} was evaluated using derivatives. The noise in the temperature data was eliminated by varying the hold time, set up time and voltage steps for V_{be} . Hold time of 100 mSec, set up time of 300 mSec along with a voltage step of 50 mV gave good measurement results. As derivative scheme was used for evaluating temperature the minimum value of the temperature can be taken as the apparent temperature of the device. In case of the measurement results shown in figure 6.13 the apparent temperature of the central device was observed to be 297.4 °K. The I_c , I_b values of the outer devices were noted for the same measurement to calculate the power. The same sets of measurements were carried out by varying V_{ce} of the outer devices from 0 V to 9 V. For each case the apparent temperature of the central device was observed and the power on the outer devices was calculated. Table 6.2 lists the variation of temperature of the central device with power on the outer devices for a particular measurement set.

Table 6.2 Variation of apparent temperature of the central device with power

Power on the Outer devices in uW	Apparent Temperature of the Central device in 0K
111.1938	297.5923
223.7953	297.585
338.1975	297.596
454.1997	297.5887
572.0005	297.6002
690.999	297.6426
811.5931	297.6227
934.5768	297.6375
1058.4472	297.6634

A plot showing the change in apparent temperature of the central device with increasing power on the outer devices was plotted as shown in figure 6.14 for this particular set of measurements.

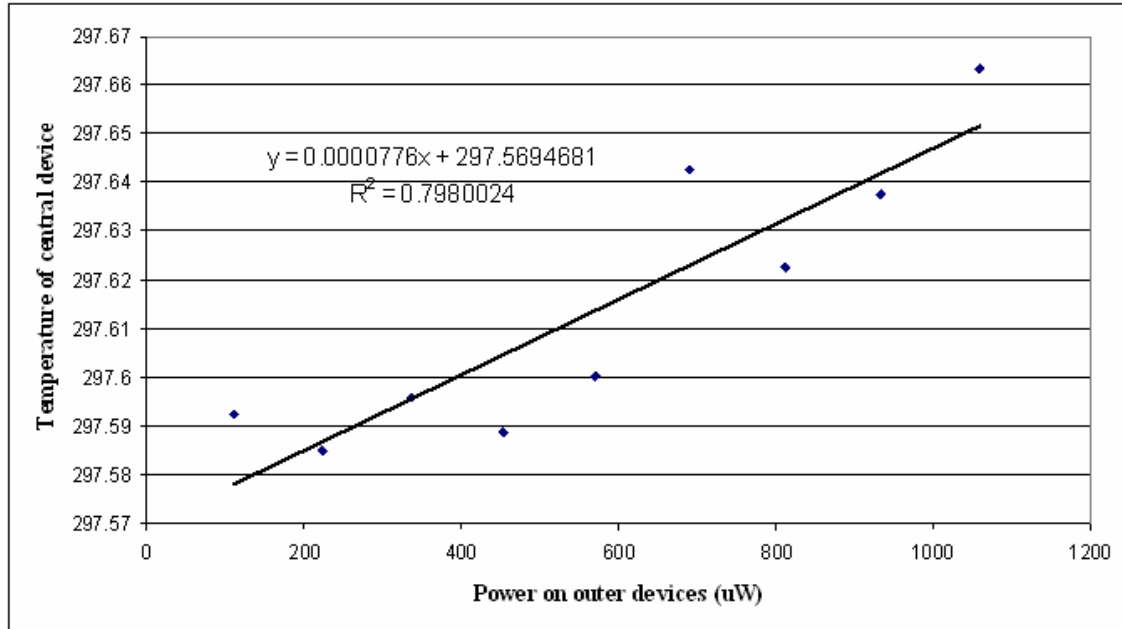


Figure 6.14 Apparent temperature variation of the central device with increasing power on outer devices

As can be seen from the figure 6.14 the trend line fitting the data points has a slope of $77.6 \text{ }^{\circ}\text{K/W}$. This slope indicates the thermal coupling among the central device and the outer devices. It can be interpreted from this slope that the temperature of the central device increases by $77.6 \text{ }^{\circ}\text{K}$ per watt of power on the outer devices when it is surrounded by four devices with a minimum spacing of $2 \text{ }\mu\text{m}$.

Similar data analysis was carried out on different chips, and the plots similar to one in figure 6.15 were plotted for each case. Apparent temperature of the central device was observed to increase in the range of $66 \text{ }^{\circ}\text{K}$ to $100 \text{ }^{\circ}\text{K}$ per watt of power on the

outer devices. The thermal resistance due to self heating for these particular devices is approximately $1000 \text{ }^{\circ}\text{K/W}$. So from the measurement results it can be concluded that the heating of these devices due to thermal coupling is about 6.6 % to 10 % of that due to self heating when surrounded by four devices with minimum spacing.

CHAPTER 7

CONCLUSION AND FUTURE WORK

Two major thermal effects in analog circuits including self heating and inter-device heating or thermal coupling are presented. The extrinsic VBIC model for the BJT is proposed to describe the thermal coupling effects at the schematic level. Various methods to simulate the self heating effects using Cadence SpectreS simulator are described.

Extensive thermal study of a particular current feedback operational amplifier (CFOA) was carried out. Systematic analysis of individual device heating characteristics in the CFOA was carried out using the VBIC model. The study involved finding the hot-spot in the CFOA. The CFOA layout was studied in detail to locate the hot-spot in the layout and dependence of the thermal effects on various layout factors.

Exhaustive research, involving detailed thermal characterization of time dependent gain error and input offset voltage error was carried out. The thermal characterization of the CFOA established a diagnostic and design procedure for circuit designers to determine the possible causes of the thermal tail at the circuit level.

Dependence of inter-device heating on layout was studied in depth. Different test structures were designed and fabricated using the National Semiconductors VIP 10 process, to study this dependence.

An innovative method for inter-device heating measurement is developed using IC-CAP / HP1B interfaced evaluation system. Real time thermal coupling measurements, showing increase in device temperature due to the power on the adjacent devices was carried out successfully. The measurement results demonstrate the presence of thermal coupling or inter-device heating for closely spaced devices.

The research can be further continued by carrying out the inter-device heating measurements for different spacing and with a different number of adjacent devices for all other set-ups on the remaining UTA test structures including the UTA204 and UTA205 test structures.

Systematic thermal characterization of input offset voltage and time dependent gain error for various configurations of CFOA as well as VFOA will be an interesting research area to work on.

APPENDIX A

LAYOUTS FOR EAGLE 19

To avoid ground loop currents involving the emitters of the central device and outer devices, separate pad connections were provided in Eagle 19 designs. UTA204 and UTA205 are the test structures designed for Eagle 19 run. The layout diagrams for both the designs are shown in figure A.1 and A.2.

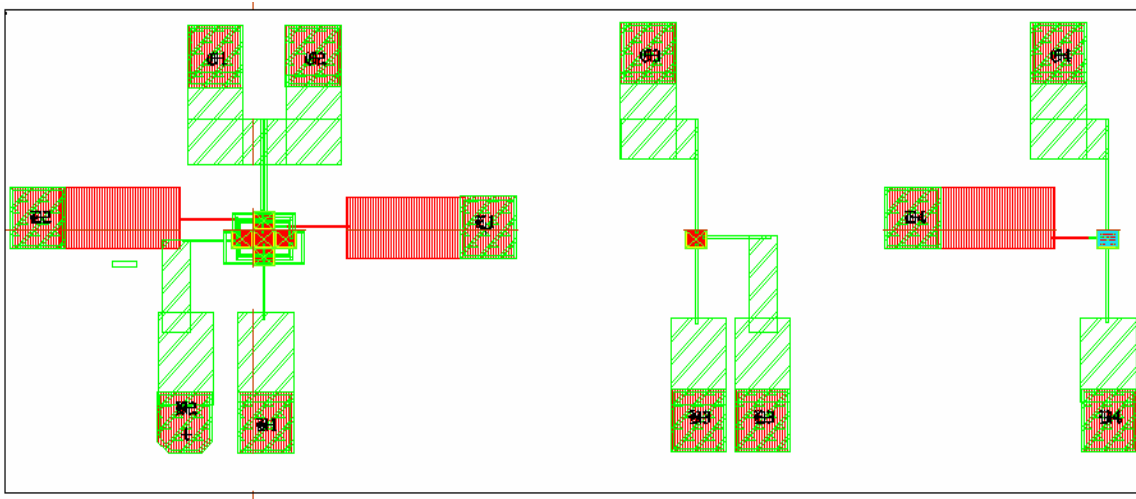


Figure A.1 Layout diagram for UTA 204

The main difference between these two designs is that in UTA 205 additional dummy devices adjacent to surrounding devices were laid out. The main purpose behind the additional dummy devices was to restrict the heat flow from the central device by the presence of these dummy devices. Isolated NPN and PNP devices were also laid out on the same chips to compare the increase in temperature of the device due to self heating and due to inter-device heating.

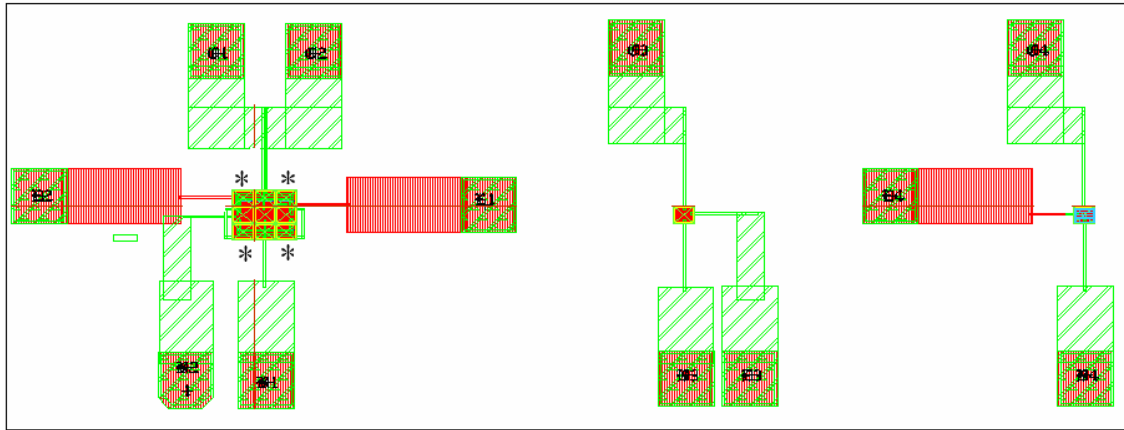


Figure A.2 Layout diagram for UTA205

In the figure A.2, the '*' indicate the positioning of the four additional dummy devices.

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BIOGRAPHICAL INFORMATION

Born in Miraj, State of Maharashtra, India, the author received his Bachelor of Engineering degree in Electrical Engineering from Walchand College Of Engineering, Sangli, Shivaji University, India, in 2001. He worked with Bajaj Auto Ltd., India for one year. The author commenced his graduate studies in Electrical Engineering department at The University of Texas at Arlington in Fall 2003 to achieve expertise in the field of VLSI design and Microelectronics circuits. During his graduate studies the he worked as Graduate Research Assistant in Analog IC Research group under the guidance of Dr. Ronald Carter, Dr. Alan Davis & Dr. Howard Russell. He has worked on characterizing thermal effects at device as well as circuit level, in co-ordination with National Semiconductor. His research interests concentrate on design, simulation, layouts and testing for the development of analog and digital integrated circuits.