

MEMS PACKAGING: FLUXLESS SOLDERING  
AND RELIABILITY  
ASSESSMENT

by

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Presented to the Faculty of the Graduate School of  
The University of Texas at Arlington in Partial Fulfillment  
of the Requirements  
for the Degree of

MASTER OF SCIENCE IN MECHANICAL ENGINEERING

THE UNIVERSITY OF TEXAS AT ARLINGTON

August 2006

## ACKNOWLEDGEMENTS

With this degree, I feel one step closer to my goal. I wish to begin by thanking my Mom, Dad and my Brothers.

I would like to thank Dr. Dereje Agonafer & Dr. Woo Ho LEE for their constant support and encouragement shown. I am indebted to Dr. Dan Popa for his support and belief in my ability. I would also like to thank Dr. Jeongsik Sin for his encouragement. I also want to thank ARRI for believing in me let me work on the research projects.

I cannot undermine the role played by Manoj Mittal, Abiodun fasoro Rakesh Murthy, Manoj Mittal, Mike Deeds and all my ARRI colleagues for my success in the BMC project and subsequently in my thesis research.

Finally I wish to thank all my friends from UTA and in India.

July 31, 2006

ABSTRACT  
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Publication No. \_\_\_\_\_

Amit Patil, MS

THE UNIVERSITY OF TEXAS AT ARLINGTON 2006

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All the optical MEMS devices are gaining popularity in the applications like telecom, medical, avionics and military. Majority of devices carry a MEMS chip, which is fabricated by deep reactive ion etching (DRIE) of silicon on insulator (SOI). The chip carries micro machined structures like optical mirrors, actuators and Sensors. All these structures are prone to failures due to stiction. For some applications these devices are suppose to have long shelf of 25-30 years. Hence it is essential to put this delicate device into strong package capable of properly protecting these devices from moisture and deleterious effects from the external environment. The package housing should be hermetic and no organic substance should be involved while packaging.

This thesis presents process development and reliability assessment of the fluxless packaging of the MEMS devices. This packaging consists of metallized Kovar package with side wall of same material and circular holes for the optical fiber interconnect between the microstructures on the chip and the macro-environment. The back of the MEMS chip and the soldering part of the optical fiber is metallized. A thin solder perform is placed between the chip and the metallized package to attach the chip and a circular solder perform is used to attach the fiber to the metal substrate. The soldering process is fluxless hence organic free.

Selection of soldering environment and solders is studied. Different process parameters are evaluated to achieve the fluxless soldering. Once the bonding between the die and the package and the fiber and the package are achieved the joining is to be assessed with different reliability tests like die shear test, fiber pull test, impact and vibration test.

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# **CHAPTER 1**

## **INTRODUCTION**

### **1.1 MEMS**

Micro Electro Mechanical System (MEMS) is the integration of Mechanical elements, sensors, actuators, and electronics on a common Semiconductor substrate through the utilization of micro fabrication technology.

The electronics are fabricated using conventional integrated circuit (IC) process sequences (e.g., CMOS, Bipolar, or BICMOS processes), the micromechanical components are fabricated using compatible "micromachining" processes that selectively etch away parts of the semiconductor wafer or add new structural layers to form the mechanical and electromechanical devices.

MEMS will revolutionize nearly every product category by bringing together semiconductor-based microelectronics with micromachining technology, thereby, making possible the realization of complete systems-on-a-chip. Although the vast majority of today's MEMS products are best categorized as components or subsystems, the emphasis in MEMS technology is on the systems aspect. True Microsystems may be a few years away, but their development and evolution rely on the success of today's components, especially as these components are integrated to perform functions of ever increasing complexity. Even though the performance of MEMS devices is expected to be superior to macro scale components and systems, the price is expected to be much

Lower [1]. Now is the actual boom time for this field which promises to make fully assembled systems that can do what large scale systems cannot do as affordably as MEMS. Things behave substantially different in micro domain. Forces related to volume, like weight and inertia, tend to decrease in significance. Forces related to the surface area, such as friction and electrostatics tend to be large. Forces like surface tension that depend upon an edge become enormous [2]. MEMS devices are currently fabricated, integrated with controlling microelectronics on a single chip.

Using the fabrication techniques and materials of microelectronics as bases, MEMS processes construct both mechanical and electrical components. MEMS are not about any one single fabrication or limited to a few materials. It is a fabrication approach that conveys the advantage of miniaturization, multiple components, and microelectronics to the design and construction of integrated electromechanical systems. Regardless of what type of micromachining processes are used all MEMS fabrication share the following key characteristics:

1) Miniaturization: Structures that are relatively small and light in weight lead to devices that have relatively high resonating frequencies. These high resonant frequencies, in turn, mean higher operating frequencies and bandwidth for sensors and actuators. Thermal time constants-the rates at which structures absorb and release heat are short for smaller, less massive structures. But miniaturization is not the principal driving force for MEMS that it is for microelectronic devices such as IC's. Because MEMS devices are by definition interacting with some aspect of the physical world such as pressure, inertia, fluids flow, light etc. There is a size below which further

smallness is detrimental to the device and system operation. The minimum size usually varies between one to two orders of magnitude larger than the smallest microelectronic device [2]

2) Multiplicity: It makes it possible to fabricate a million components easily and quickly in one fabrication process. Such economics of costs and scale are critical for reducing unit costs. Equally important advantage of multiplicity is the additional flexibility in the design of massively parallel and interconnected systems.

3) Microelectronics: These integrated into the MEMS devices provide the latter with greater intelligence and allow closed loop feedback systems, localized signal conditioning, and control, for example control of parallel actuator arrays becomes possible with integrated circuitry.

4) Active surfaces: Devices are attached to a surface so that there is a fixed topology. The devices are coupled primarily to the dynamics of the medium they are manipulating, leading to a movement in the degree of global as well as local coordinate systems.

Like many other emerging technologies with significant future potential, MEMS is subject to an increasing level of excitement and publicity. As it matures and end markets develop, end users will be faced with the difficult choice between MEMS and conventional methods. For applications that can benefit from existing commercial MEMS products, the answer relies on the ability to meet required specifications and pricing. In practice a MEMS solution becomes attractive if it allows a new function, provides cost reduction, realizes a performance enhancement, or all of these. Size

reduction can play an important role but is seldom sufficient as the sole reason unless it becomes enabling itself, i.e. the size reduction is an important aspect of the final product.

One of the significant challenges facing MEMS is the requirement that they be reliable or more reliable than the conventional solution that they replace.

## **1.2. Applications of MEMS**

MEMS devices can be used as miniature sensors, controllers or actuators. They have become increasingly dominant in every aspect of commercial marketplace as the technologies for micro fabrication continue to be developed. MEMS find applications in various fields. But so far, very few commercial applications exist. Some that are present in the commercial market are inertial sensors like accelerometers, gyroscopes, inkjet printers, video projection systems, gas and chemical sensors, and biomedical devices like muscle stimulation, blood monitors, etc [3] Vast amount of research can help MEMS find place in the following field Table 1.1 [2].



Table 1.1 Application Areas of MEMS devices (sensors)

Area	Application
Automotive	Pressure sensors, flow sensor, accelerometer gyroscopes
Aerospace industry	Active flight control surfaces, Temperature sensors, chemical sensors, Micro satellites
Telecommunication	RF switches, variable optical amplifier, tunable lasers, inductors
Information technology	Video projectors, Ink jet print heads, displays, Data Storage
Consumers products	Social Robots, fitness gear using hydraulics, washers with water level controls in washing machines, smart toys
Healthcare and biomedical	Disposable blood pressure transducer (DPT), intrauterine pressure sensor, angioplasty pressure sensor, micro nozzle injection systems microfluidic systems, hearing aids, DNA testing (gene probes)

### 1.3 MEMS Fabrication

Majority of the technology that supports MEMS research is borrowed from the microelectronics industry; so the field takes advantage of four decades of broad, research into the properties of silicon, thin film deposition, photolithography, and related technologies. Thus MEMS research holds out the promise of batch fabrication of miniaturized machines that can be easily integrated with electronics.

There are a number of basic techniques that can be used to pattern thin films that have been deposited on a silicon wafer, and to shape the wafer itself, to form a set of basic microstructures (bulk silicon micromachining). The techniques for depositing and patterning thin films can be used to produce quite complex microstructures on the surface of silicon wafer (surface silicon micromachining). Electrochemical etching techniques are being investigated to extend the set of basic silicon micromachining techniques. Silicon bonding techniques can also be utilized to extend the structures produced by silicon micromachining techniques into multilayer structures.

### **1.3.1 Bulk Micro machining**

Bulk Micromachining makes micromechanical devices by etching deeply into the silicon wafer Bulk micromachining is the oldest process for the production of MEMS, and it was developed in the 1960s [5]. Areas of single crystal silicon that have first been exposed through a photolithographic mask are removed by alkaline chemicals. Etching produces concave, pyramidal or other faceted holes, depending on which face of the crystal is exposed to the chemicals [6]. There are several ways to etch the silicon wafer. Anisotropic etching uses etchants like KOH that etch different crystallographic directions at different rates. Certain crystallographic planes etch extremely slowly, and are called stop planes. Anisotropic etching usually produces Vee grooves, pyramids, and channels into the surface of the silicon wafer. Isotropic etching etches all directions in the silicon wafer with nearly the same rate, and produces rounded depressions on the surface of the wafer that usually resemble hemispheres and

cylinders. Deep Reactive Ion Etching, RIE or DRIE, uses plasma to etch straight walled structures on the wafer.

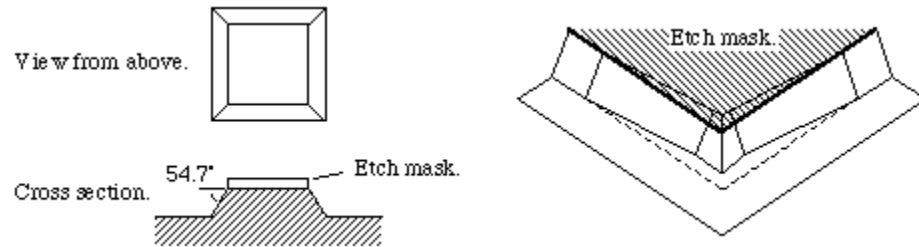


Figure 1.1 Wet Etching of Silicon

### 1.3.2 Surface Micro Machining

The limitations of bulk micromachining have been overcome by surface micromachining [7]. The anisotropic wet etching and concentration dependent etching techniques are generally called bulk silicon micromachining techniques. This is because the microstructures are formed by etching away the bulk of the silicon wafer to achieve the desired result. Surface micromachining techniques build up the structure in layers of thin films on the surface of the silicon wafer (or any other suitable substrate).

This process involves films of two different materials, a structural material (commonly a polysilicon) and a sacrificial material (oxide). These are deposited and dry etched in sequence. Finally the sacrificial material is wet etched away to release the structure. The more layers, the more complex the structure, and the more difficult it becomes to fabricate [8].

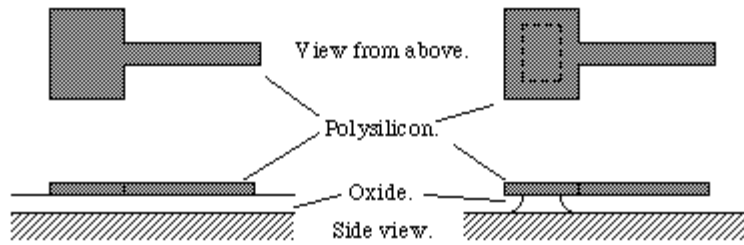


Figure 1.2 Surface Micromachined cantilever beam

A surface micromachined cantilever beam is shown in figure 1.2. A sacrificial layer of oxide is deposited on the surface of the wafer. A layer of polysilicon is then deposited, and patterned using RIE techniques to a beam with an anchor pad. The wafer is then wet etched to remove the oxide layer under the beam, freeing it (fig 1.2). The anchor pad has been under etched, however the wafer was removed from the etch bath before all the oxide was removed from under the pad leaving the beam attached to the wafer.

A variety of different chambers can be fabricated on the surface of silicon wafers using surface micromachining techniques. In figure 1.3, the chamber is defined by a volume of sacrificial oxide. A layer of polysilicon is then deposited over the surface of the wafer. A window is dry etched (RIE) through the polysilicon, and the wafer is then immersed in a wet etch that removes the oxide, leaving a windowed chamber.



Figure 1.3 Different chamber fabrication by surface micromachining and RIE

Surface micromachining can potentially produce quite complicated structures; such as microengineered tweezers, and gear trains.

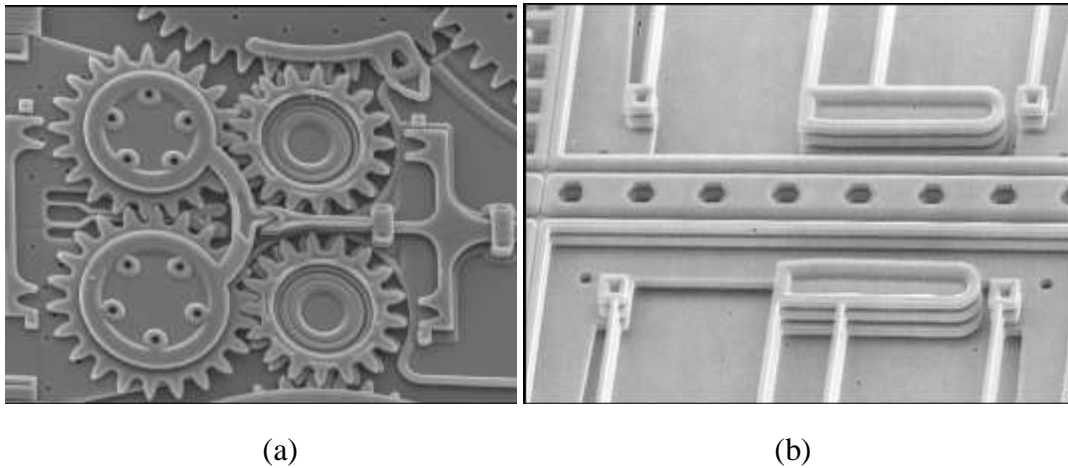


Figure 1.4 Structured made by surface micromachining (a) meshing gears on a movable platform, (b) laminated support springs (Sandia National laboratories)

### 1.3.3 LIGA

LIGA is a German acronym that stands for (Lithographie, Galvanoformung, Abformung) lithography, electroplating, and molding. LIGA was developed to produce high aspect ratio structures. LIGA offers some unique properties that makes it an interesting technology. LIGA enables the construction of structures with the thickness of bulk micromachining with a degree of design freedom similar to surface micromachined devices. This technology offers structures several hundred microns thick, with a minimum feature size of only a few microns. It is capable of creating very finely defined microstructures of up to 15-500 $\mu$ m high [8].

In the process as originally developed, a special kind of photolithography using X-rays (X-ray lithography) is used to produce patterns in very thick layers of photoresist[9]. The X-rays from a synchrotron source are shone through a special mask onto a thick photoresist layer (sensitive to X-rays) which covers a conductive substrate . This resist is then developed.

The pattern formed is then electroplated with metal. The metal structures produced can be the final product; however it is common to produce a metal mould. This mould can then be filled with a suitable material, such as a plastic, to produce the finished product in that material.

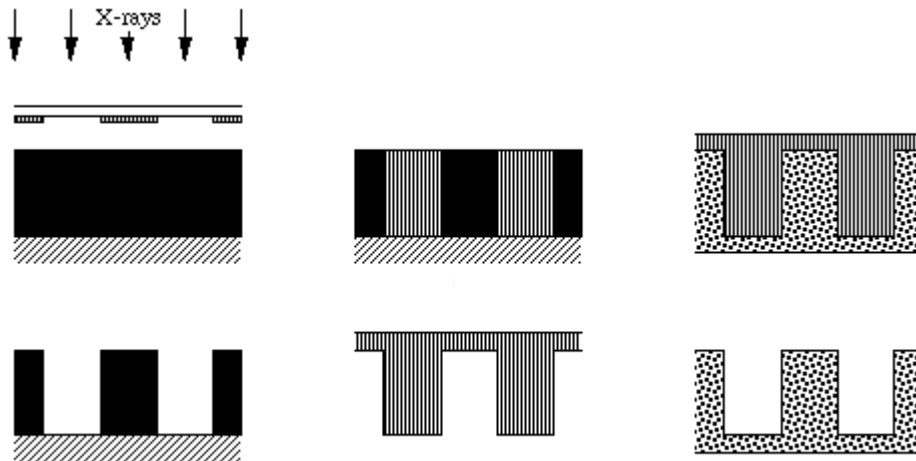


Figure 1.5 LIGA Process Flow

As the synchrotron source makes LIGA expensive, alternatives are being developed. These include high voltage electron beam lithography which can be used to produce structures of the order of 100 $\mu$ m high, and excimer lasers capable of producing structures of up to several hundred microns high [10]

Electroplating is not limited to use with the LIGA process, but may be combined with other processes and more conventional photolithography to produce microstructures.

#### **1.4 MEMS Packaging**

A MEMS device generally requires an extra fabrication process where the device wafer is bonded to a second wafer which effectively encapsulates the MEMS structure. This method leaves the device free to move within a vacuum or an inert gas atmosphere. These bonds are typically hermetic and therefore prevent moisture contamination and subsequent failure of the microstructure. Once protected in this way, devices are considered robust. They can then be assembled into a wide variety of package options including SOIC, PLCC, SiP or *MicroLeadFrame*® (MLF®) which can all be adapted to meet the height requirement of the capped device [11].

MEMS packages can contain many electrical and mechanical components. To be useful to the outside world these components need interconnections. Alone, MEMS die is cut from a wafer is extremely fragile and must be protected from mechanical damage and hostile environments. To function, electrical circuits need to be supplied with electrical energy, which is consumed and transformed into mechanical and thermal (heat) energy. Because the system operates best within a limited temperature range, packaging must offer an adequate means for removal of heat.

The package serves to integrate all of the components required for a system application in a manner that minimizes size, cost, mass and complexity. The package provides the interface between the components and the overall system.

The different core functionality of package can be mechanical support, protection from environment and electrical connections. Due to different moving parts in the MEMS it is very mechanical in nature because of which the requirement to support and protect the device from thermal and mechanical shock, vibration, high acceleration, particles, and other physical damage during storage and operation of the part becomes very important [12].

The mechanical stress induced on the device depends on the application. For example, device used in automobile would experience lesser vibration and heat compared to use in an aircrafts or avionics based applications. The device used in telecommunication would handle much lower stress levels compared to the earlier. There is a vast difference between space and terrestrial applications.

The coefficient of thermal expansion (CTE) of the package should be almost equal the CTE of silicon to get better reliability, because thermal shock or thermal cycling test may cause die cracking and delamination if the materials are unmatched or if the silicon is subject to tensile stress. Other important parameters are thermal resistance of the carrier, the material's electrical properties, and its chemical properties, or resistance to corrosion [3].

After the MEMS device is supported package or carrier, wire bonding and other electrical connections are made, this assembly should be protected from possible



scratches, particulates, and different physical damages. This can be achieved by adding walls and a cover to the base or by encapsulating the assembly in plastic or other material. As the electrical connections to the package are usually made through the walls, the walls are generally made from glass or ceramic. The glass or ceramic can also be used to provide electrical insulation of the leads as they exit through a conducting package wall [13].

One of the functionalities of the MEMS devices includes measuring something in the immediate surrounding environment. Such devices can be used as biological ‘sniffers’ to chemical sensors that measure concentrations of certain types of liquids. This gives us an idea that the traditional hermetic packaging used for protecting microelectronic devices may not apply to all MEMS devices. These devices might be directly mounted to a printed circuit board (PCB) or a hybrid-like ceramic substrate and have nothing but a ‘housing’ to protect it from mechanical damage such as dropping or damage from the operator’s thumb.

Taking into consideration all the above issues and problems for MEMS packaging it is important to study and compare the well matured packaging technology used in packaging of microelectronics to MEMS packaging. In the following section we discuss about the same.

For fabrication of MEMS we use manufacturing processes tools similar to that used in microelectronics area. Majority of these tools are directly used and few are modified to achieve the requirements of MEMS [14].

As MEMS packaging follows the rules of IC packaging it is important to understand packaging of microelectronics.

The structure of packaging can be classified as different levels of packaging with level 0 as the IC itself. At level 1 the chip is extracted from the wafer and assembled into the carrier. Multiple number of these carries are assembled on to the board with interconnects representing level 2. An array of these boards assembled on the mother board represent level 3 and the whole system represent s level 4 [3].

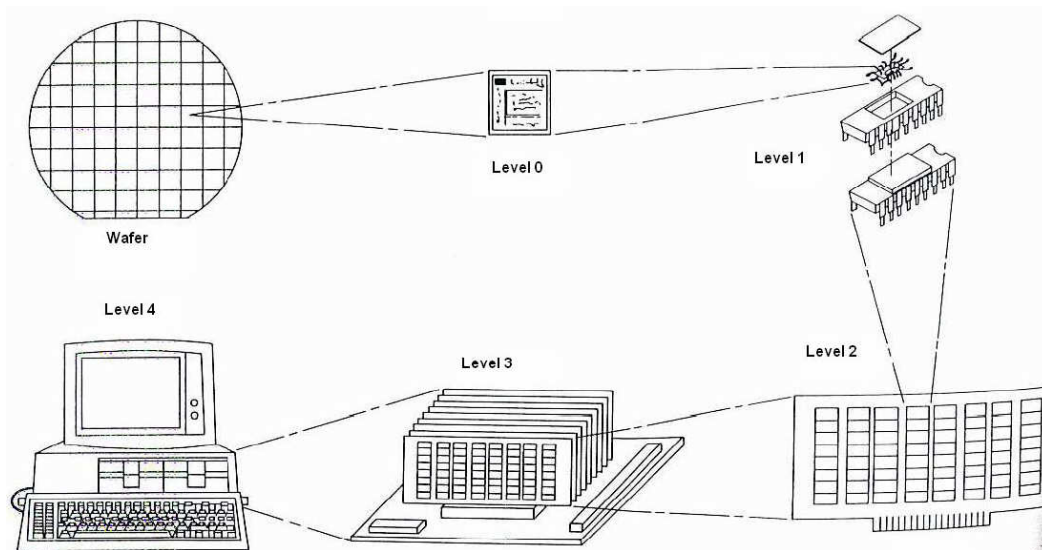


Figure 1.6 Different levels of Packaging

All these packaging levels are performing some function in their respective places. One of the most important being provision of electrical connections for transfer of power and signals interaction between the chip and the outside world. Second with the package should provide mechanical support to the chip for further processing handling and performance. Third the package must provide protection from moisture, dust, and any gases that would deteriorate the performance of the chip. Fourth function

would include dissipation of heat produced by the chip to prevent degradation of performance and reduction in operational lifetime. To fulfill all these functions the package puts constraints on the chip. These constraints lead to degradation in electrical performance, increase in effective size and weight of the chip, this induces the burden of testing and brings in reliability issues. The package adds to the cost, that often exceeds that of the chip itself. Therefore packaging is a critical balance between the availability of desired functions and lowering of constraints with cost effectiveness [3].

#### **1.4.1 MEMS vs. IC Packaging**

There are differences between MEMS and IC packaging techniques. Unlike the IC die packaging, MEMS dice need to interface with the environment for sensing, interconnections and actuation. MEMS packaging is application specific and the package allows the physical interface of the MEMS device to the environment. In the case of fluid mass flow control sensor, the medium flows into and out of the package. This type of packaging is referred to as media compatible packaging. There would be different challenges for harsh environment MEMS application packaging. Table 1.2 shows the comparison of MEMS packaging and IC packaging referring to some of the processes used [15].

Packaging of MEMS devices is more complex as they serve to protect from the environment, while somewhat in contradiction, enabling interaction with that environment in order to measure or affect the desired physical or chemical parameters. Difference between the two is shown in the fig 1.7 & fig 1.8 [16].

Table 1.2 Comparisons between IC and MEMS packaging [15]

Sr.No	Process	IC packaging	MEMS packaging
1	Dicing	✓	✓
2	Die Bonding	✓	✓
3	Wafer Bonding		✓
4	Wire Bonding	✓	✓
5	Pre-molding		✓
6	Post molding	✓	
7	Hermetic	✓	✓
8	Capping	✓	✓
9	Testing	✓	✓
10	Stiction	✓	✓
11	Reliability	✓	✓
12	Standard	✓	✓
13	Cost	✓	✓

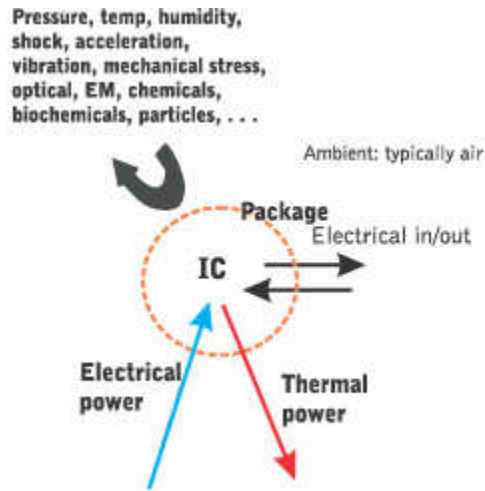


Fig 1.7 IC Package Functionalities

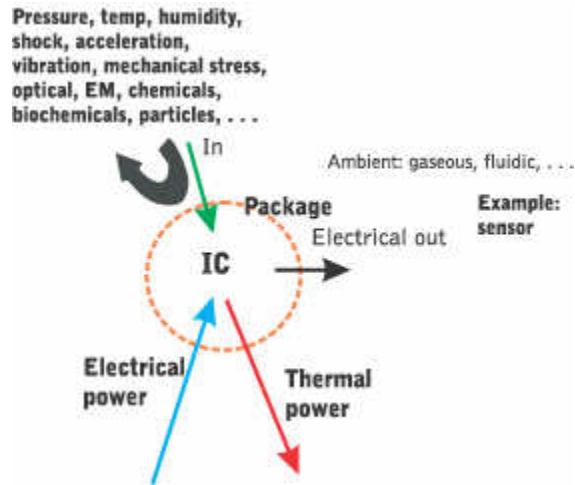


Figure 1.8 MEMS Package Functionalities

The goal of IC packaging is to provide physical support and an electrical interface to the chip and to isolate it physically from adverse effects of its environment. MEMS devices, on the other hand, often are interfaced intimately with their

environment and are less generic in nature. Consequently, MEMS packaging must address different and more diverse needs than IC packaging [16].

1) MEMS do not obey scaling laws as ICs do: although some devices have been scaling down, MEMS are dealing with energy as input or output, and therefore scaling does not result in the same advantages as for ICs.

2) There is a larger variety of basic building blocks in MEMS: sensors and actuators can be composed of pyroelectric, resistive, thermoelectric, magnetic, acoustic, chemical, optical elements.

3) There is often no dominant 'mainstream' process sequence for a particular building block.

4) The packaging functionalities are inherently broader. IC packages have to accommodate ever-denser electrical I/Os and increasing levels of electrical power and thermal dissipation. Ambient parameters, such as moisture or pressure, are treated as non-desirable noise signals to be totally isolated from the IC by the package. In MEMS packaging, the electrical I/O is typically unidirectional and less dense. The electrical and thermal power handling is less demanding, but at least one of the non-electrical influences becomes a desired input [17].

#### **1.4.2 Packaging issues and challenges**

Packaging (including reliability) has been and continues to be a major challenge. Packaging cost is about 50 to 90% of the total cost of the MEMS product [18].

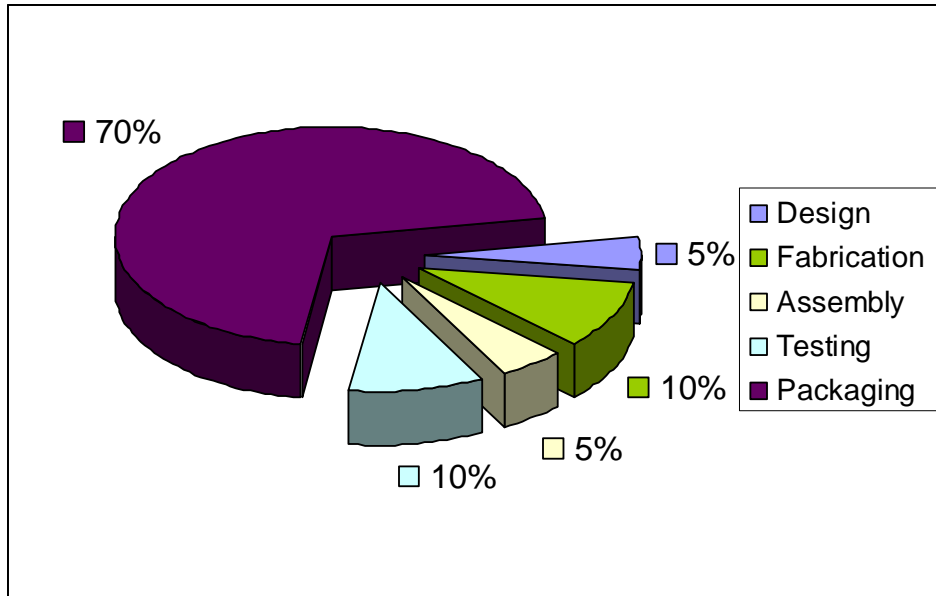


Figure 1.9 Percentage cost involved in different processes of MEMS

For MEMS packaging task like assembly, packaging and testing make a major area of whole process.

MEMS packaging is developing area and faces challenges as listed below

1) Environment-: MEMS devices need to operate in diverse environments such as under automobile hoods, intense vibrations, in salt water, strong acids or other chemicals, alkaline or organic solutions. The package while performing detection or actuation must be able to withstand the environments.

2) Reliability of the MEMS die due stress induced by packaging parameters: The package is a part of the complete system and should be designed as the MEMS chip is designed, with specific and many times custom package. It is necessary for the chip, package and environment to function together and must be compatible with each other.

This determines which materials and what design considerations and limitations become

important. One of the major challenges is the issue of material properties. The properties of materials depend on how they are used, processed, the heat treatments to which the materials are subjected. One positive point is that the defect density decreases with the size for materials and MEMS devices are so small that the chance of a killer defect occurring in a device is reduced [12].

3) Packaging of MEMS dice is application specific and hence desired process steps vary significantly. It is important to classify MEMS dice from the packaging requirements and develop the packaging standards and related knowledge base.

4) Stiction: Typically the polysilicon features are supported by silicon dioxide, which is used as a sacrificial layer [12]. The challenge in this is when the etching should be done to release the features. Complementary to this is the issue of stiction. The risk of stiction occurs during the release and after the release. Stiction occurs from the capillary action of the evaporating rinse solution in the crevices between structural elements like cantilevers and the substrate.

5) Stress: One source of stress results from the die attach materials at the interface between the MEMS die and the package substrate. When polysilicon is deposited a great deal of stress is produced in the films. This stress can be annealed out at a temperature of around 1000°C.

6) Dicing: the challenge is in dicing of the wafer into the individual dice. It is typically done with a diamond saw a few mils thick. This requires the coolant to flow over the surface of the very sensitive dice along with silicon and diamond particles. These



particles combined with the coolant can contaminate the devices and get into the crevices of the features causing the device to fail.

7) Penetration of Moisture: dicing: the challenge is in dicing of the wafer into the individual dice. It is typically done with a diamond saw a few mils thick. This requires the coolant to flow over the surface of the very sensitive dice along with silicon and diamond particles. These particles combined with the coolant can contaminate the devices and get into the crevices of the features causing the device [12].

8) Outgassing: when epoxies are used as in the case of plastic encapsulation, the die attach compounds outgas as they cure. These water and organic vapors redeposit on the features, in crevices and on bond pads [12].

### **1.4.3 Types of MEMS packages**

Every MEMS device would typically need a new package design to get the best of its performance. One can generally group these packages; this section will talk about different types of packages.

#### **Plastic Packages**

Plastic packages have been widely used by the electronics industry for many years and for almost every application because of their low manufacturing cost. High reliability applications are an exception because serious reliability questions have been raised. Plastic packages are not hermetic, and hermetic seals are generally required for high reliability applications. The packages are also susceptible to cracking in humid environments during temperature cycling of the surface mount assembly of the package

to the mother-board. Plastic packaging for space applications may gain acceptability as time goes on [19].

### Thin-Film Multilayer Packages

Within the broad subject of thin-film multilayer packages, two general technologies are used. One uses sheets of polyimide laminated together in a way similar to that used for the LTCC packages described above, except a final firing is not required. Each individual sheet is typically 25  $\mu\text{m}$  and is processed separately using thin-film metal processing. The second technique also uses polyimide, but each layer is spun onto and baked on the carrier or substrate to form 1- to 20  $\mu\text{m}$ -thick layers. In this method, via holes are either wet etched or reactive ion etched (RIE). The polyimide for both methods has a relative permittivity of 2.8 to 3.2. Since the permittivity is low and the layers are thin, the same characteristic impedance lines can be fabricated with less line-to-line coupling; therefore, closer spacing of lines is possible. In addition, the low permittivity results in low line capacitance and therefore faster circuits [19].

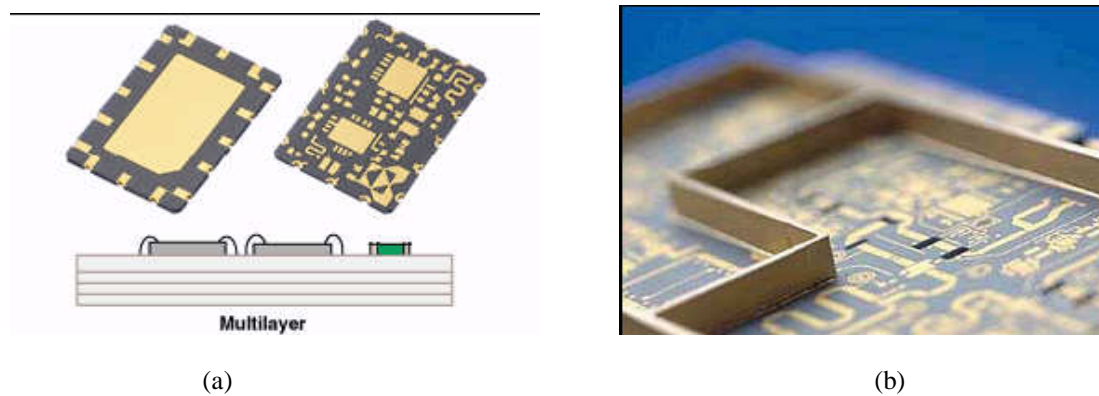


Figure 1.10 Multilayer packages a) multilayer packages, b) LTCC package

## Ceramic Packages

These packages have several features that make them suitable for MEMS. They provide low weight, are easily mass produced and can be low in cost. They can be made hermetic and can more easily integrate signal distribution lines and feed-through. The multilayer ceramic packages could reduce the size and the cost of the device. These types of packages are generally referred to as co-fired multilayer ceramic packages. Ceramics have dielectric constants from 4 to 10000, thermal expansion coefficients matching silicon  $30 \times 10^{-7}/^{\circ}\text{C}$  or copper  $170 \times 10^{-7}/^{\circ}\text{C}$  and thermal conductivities from one of the best insulators to better than aluminum metal  $220 \text{ W/m}^{\circ}\text{K}$ . Dimensional stability as measured by shrinkage control has been achieved at better than  $\pm 0.1\%$  of nominal shrinkage, allowing as many as 30 to 50 layers of ceramic to be metallized. Ceramic packages can be found in a variety of forms, such as DIP's, chip carriers, flat packs, and pin grid arrays [19].

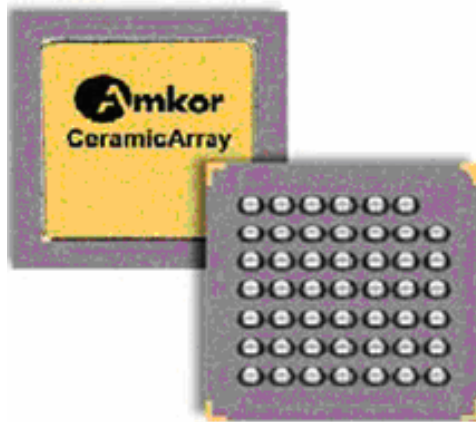


Figure 1.11 Ball grid array ceramic package (courtesy Amkor technology)

## Metal Packages

Metal packages are often used for microwave multichip modules and hybrid circuits because they provide excellent thermal dissipation and excellent electromagnetic shielding. They can have a large internal volume while still maintaining mechanical reliability. The package can use either an integrated base or sidewalls with a lid or it can have a separate base, sidewalls, and lid. Inside the package, ceramic substrates or chip carriers are required for use with the feed-throughs.

The selection of the proper metal can be critical. CuW (10/90), Silvar™ (a Ni-Fe alloy), CuMo (15/85), and CuW (15/85) all have good thermal conductivity and a higher CTE than silicon, which makes them good choices. Kovar, a Fe-Ni-Co alloy commonly. All of the above materials, in addition to Alloy-46, may be used for the sidewalls and lid. Cu, Ag, or Au plating of the packages is commonly done[19].

Before final assembly, a bake is usually performed to drive out any trapped gas or moisture. This reduces the onset of corrosion-related failures. During assembly, the highest temperature curing epoxies or solders should be used first and subsequent processing temperatures should decrease until the final lid seal is done at the lowest temperature to avoid later steps damaging earlier steps. Au-Sn is a commonly used solder that works well when the two materials to be bonded have similar CTEs. Au-Sn solder joints of materials with a large CTE mismatch are susceptible to fatigue failures after temperature cycling. The AuSn intermetallics that form tend to be brittle and can accommodate only low amounts of stress.

Welding (using lasers to locally heat the joint between the two parts without raising the temperature of the entire part) is a commonly used alternative to solders. Regardless of the seal technology, no voids or misalignments can be tolerated since they can compromise the package hermeticity. Hermeticity can also be affected by the feedthroughs that are required in metal packages. These feedthroughs are generally made of glass or ceramic and each method (glass seal or aluminum feedthrough) has its weakness. Glass can crack during handling and thermal cycling. The conductor exiting through the ceramic feedthrough may not seal properly due to metallurgical reasons. Generally, these failures are due to processing problems as the ceramic must be metallized so that the conductor (generally metal) may be soldered (or brazed) to it. The metallization process must allow for complete wetting of the conducting pin to the ceramic. Incomplete wetting can show up as a failure during thermal cycle testing [19].

#### **1.4.4 MOEMS Packaging**

Microoptoelectromechanical systems (MOEMS), which are MEMS integrated with photonics, share the traditional challenges of MEMS with the additional issues of optical interconnects and of optical surface contamination. Traditionally, switching in the telecommunication industry is performed electrically, even in optical networks. MOEMS offers significant savings in power, cost, and volume. More importantly, it eliminates problems the electrical switch or router and allows wavelength division multiplexing (WDM) to reach its full performance potential. For all optical networks, MOEMS is expected to have a huge impact on the telecommunications market. The optical component market, in general, is projected to grow anywhere from 35% to 50%

per year in coming years [20]. MOEMS is well positioned to impact the existing market as well as the expanding market. Most MOEMS applications place additional emphasis on hermetic packaging due to potential contamination of the optical surfaces. The proliferation of hermetic optical packaging needs has resulted in a library of standard packages and numerous sources for custom package fabrication [12].

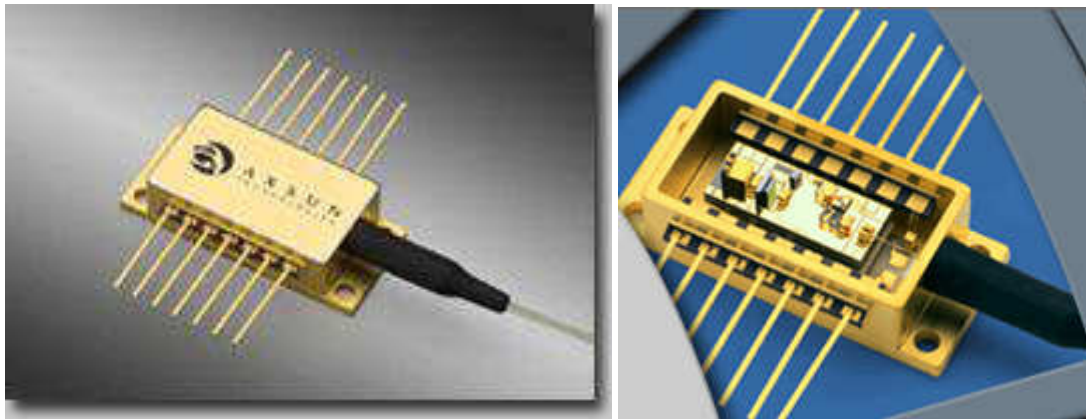


Figure 1.12 MOEMS Package By Axsun Technologies

### 1.5 Motivation

This section provides the motivation of thesis. The IC market has transformed because of IC packaging. The IC industry had a boom when low cost and reliable packaging was available. Similarly MEMS packaging will have same effect on commercialization of MEMS. IC industry has benefited a lot from research involved in the IC packaging reliability. Every MEMS device is unique in nature and would require unique packaging process also with different controlled processes parameters.

The goal of this research was to develop a packaging process for devices having longer shelf life. With major concentration on die attach process and fibers attach

process development without use of any organic substance like flux while soldering. The die and fiber both are attached to the metal package with fiber crossing the boundary of the package. After the attachment being done the solder bond should be tested for reliability. Different reliability test that should be done for the reliability assessment of the process are 1) Die shear test 2) Fiber pull test 3) Vibration test 4) Thermal cycling 5) Mechanical drop or impact test. 6) Hermeticity test.

### **1.6 Approach**

For packaging of the devices having longer shelf life it is important that the package should be hermetic so package material selected was kovar. The package is then electroplated with Nickel and Gold layers respectively. For the MEMS die the MEMS structure were made on chrome and gold backed silicon wafer. Solder selection to do the die attach was also important because after the die is bonded to the package optical fiber is also soldered to the package. So the first solder (i.e the die attach solder) should have much higher melting point than the later. The first solder was selected as 80Au/20Sn (melting point 280°C) and the later to be pure Indium (melting point 157°C). During handling of components of the packaging care was taken that all parts are free of contaminants. All of them are wet etched with Isopropyl alcohol while the indium was followed by etching in 10% HCL.

#### **Contribution**

- The primary contribution of this thesis is the attachment of the die to the metallized Kovar substrate followed by interconnects between the MEMS die

and the macro environment with the attachment of the metallized optical fiber to the carrier.

- Secondly for destructive testing of these joints fixtures were developed.
- Finally the both the joints were tested with destructive testing.



## CHAPTER 2

### SOLDERS AND SOLDERING & RELIABILITY TEST

#### 2.1 Die attach

The process of mounting a semiconductor or MEMS dies/chip on a package or a substrate is called die attach. The way the chip is bonded defines the die attach process - epoxy, soft solder, eutectic and flip chip are the most widely used techniques. Die can vary in size from less than  $0.5 \times 0.5 \text{ mm}^2$  to greater than  $50 \times 50 \text{ mm}^2$ , the choice of attachment depends on the size, substrate material (e.g. ceramic, polymer, glass metal) device requirements and operating environment [21].

The requirements of a die attach material depends on the application, but may include:

- Good mechanical strength
- Process temperature that will not affect the die function
- Absorption of stress from thermal expansion mismatch between the die and substrate
- Joint fatigue resistance - mechanical and thermal
- Electrical/thermal conduction or isolation

- Chemical inertness with low outgassing
- Reworkable
- Ability to automate process

Die attach is an established process which has been evolving over the several years. Initial applications usually employed eutectic bonding or soldering on ceramics or metal substrates. Due to the development of non-hermetic packaging, high volume production and larger die, adhesives have become the predominant attachment medium. These materials are still evolving to meet the requirements for faster manufacturing systems and more severe component requirements.

The Die attach process can be classified in following types.

### **2.1.1 Adhesive process or Adhesive attach**

A typical adhesive joining process requires working temperatures up to 250° C, in addition to increased pressure. The three adhesive types listed above - ICA, ACA and NCA-are used in flip chip applications with increased frequency [21].

ICA (isotropic conductive adhesive) describes a polymer filled with conductive particles. With flip chip processes it is applied to the bond pads and to create the contact between bumps and substrate.

NCA (non-conductive adhesive) is a non-conductive polymer. The adhesive is applied to the substrate across the entire surface under the component. A flip chip die is bonded to the substrate under pressure and heat, pressing the bumps onto the substrate.

The adhesive ensures that the mechanical and electrical contact is maintained long term.

ACA (anisotropic conductive adhesive) is a polymer with enclosed conductive particles (e.g. Ni). The adhesive is also applied across the entire surface. As a result of the pressure applied during bonding, the conducting connections in the adhesive form a connection between bumps and bond pads on the substrate.

Above processes are generally applicable to electronic packaging and can also be applicable for MEMS applications.

Following are some benefits and limitations of adhesive attach.

Benefits:

- Ease of automation
- Low curing temperatures
- Reduced die stresses
- Low cost
- Wide range of die sizes
- Special plated surfaces are not required
- Rework is possible

Limitations:

- Outgassing

- Contamination/bleed
- Voiding (in some cases)
- Inferior thermal/electrical conductivity
- Dimensional changes during processing and service life
- Harsh environment sensitivity

Typical adhesive die materials:

- Epoxy thermo set resins
- Acrylic thermoplastic resins
- Silicone resins

### **2.1.2 Soldering die attach**

Soldering is mainly used on high power devices because of its good thermal/electrical conductivity and ability to absorb stresses due to expansion mismatch [21].

Benefits:

- Good electrical/thermal conductivity
- Good CTE (coefficient of thermal expansion) absorbing capabilities
- 'Clean'

- Rework is possible

Limitations:

- Requires wettable metallized surfaces on the die/substrate
- Usually requires processing temperatures  $>200^{\circ}\text{C}$
- Needs flux or an inert gas atmosphere
- Thermal fatigue resistance of some alloys

Typical solder die attach materials

63Pb-37Sn( $183^{\circ}\text{C}$ )

95Pb-5Sn( $310^{\circ}\text{C}$ )

Pb-In-Ag( $310\text{-}314^{\circ}\text{C}$ )

65Sn-25Ag-10Sb( $233^{\circ}\text{C}$ )

Values in brackets indicate melting temperature

### **2.1.3 Glass die attach**

The glass is introduced to the joint as a paste/frit, then heated (to  $350\text{-}450^{\circ}\text{C}$ , for instance) until it softens to form a low viscosity liquid that will wet the die and substrate. Silver particles can be added to the glass ( $\sim 80\% \text{Ag}$ ) to enhance the thermal and electrical conductivity of the material [21].

Benefits:

- Relatively insensitive to metallization

- Low void content
- Good thermal/electrical conductivity
- Limited stress relaxation
- Low contamination
- High process/operating temperature resistance

Limitations:

- High processing temperature
- Processing is conducted in an oxidizing atmosphere (oxidation of other plated systems)

Typical glass die attach materials

Lead borate based glass - 80% Ag

#### **2.1.4 Eutectic die attach**

A eutectic bond is formed by heating two (or more) materials (e.g. Au and Sn) in a joint such that they diffuse together to form an alloy composition (e.g. a 80Au-20Sn eutectic) that melts at a lower temperature than the base materials (e.g. a 80Au-20Sn eutectic melts at 278°C). The eutectic bond can be produced by heating the die then scrubbing it against a gold foil/metallization or by introducing a eutectic foil (e.g. Au-Sn) into the joint [22-23].

Benefits:

- Good thermal conductivity
- Electrically conducting
- Good fatigue/creep resistance
- Low contamination
- 'High' process/operating temperature capability

Limitations:

- High stresses on Si chip due to CTE mismatch on larger dies
- Relatively high processing temperatures
- Die back metallization may be required
- If bare die are used, a scrubbing action is required to break down surface silica film
- Rework is difficult.

Typical eutectic die attach materials

- Au97-Si3(363°C)
- Au88-Sn12 (350°C)
- Au80-Sn20 (280°C)
- Pb63-35Sn-1.8Sb (230°C)

Values in the brackets indicate eutectic temperature.

The process described above requires application of heat and working in protective gas.

In addition, it often requires scrubbing motion and/or pressure.

For our die attach being for MOEMS based application for packaging of which the die is attached to the substrate first followed by fiber attachment. So there is a requirement of step soldering for which the first solder material or alloy should have should have much higher melting point than the second solder. Also the melting temperature of the solder should be such that it does not affect the die.

The substrate is made of Kovar material as it has CTE close to that of silicon. For attaching the die on this metal there is a requirement of metallization on the surfaces of both, the die and the substrate. The metallization consist coating of gold on both surfaces with barrier metal beneath. The gold layer is much thicker so it becomes important to use gold bearing solders for soldering.

## **2.2 Gold Bearing Solders**

Gold bearing solders are all gold rich alloys of eutectic composition and have melting points between 278 and 363°C. Some of the most common gold bearing solder alloys is listed in the table below [24].

Gold bearing solders.

- Au80-20Sn (280°C)
- Au75-25Sb (356°C)
- Au88-12Ge (361°C)
- Au97-3Si (363°C)



Gold bearing solders have the advantage of being suitable for joining to gold-metallized components. Three of the above mentioned solders are widely used in electronic industry as high temperature solders for attaching devices on the packages and building hermetic enclosures for sensitive and optical devices.

These solders are considered as hard solders. They bear high thermal conductivity and are free from thermal fatigue because of high strength which results in elastic deformation rather than plastic deformation. As they lack plastic deformation, bonding with hard solders produces high stresses on the die. But if the bonding layers are void free the stress developed is less than the strength of the die. Hence the die will not crack. Where as if large voids exist in the bonding layer near to the edges of the die, which will induce high localized stress thus increasing the probability of, die cracking. Hard solders are preferred as the bonding media for highly reliable devices provided that good bonding can be achieved.

All these solders can be used for our application. Au-Si and Au-Ge have almost similar characteristics as solders compared to Au-Sn .Some reasons for using Au-Sn for the die attach. Au-Sn has lower melting point compared to Au-Si thus Au-Sn reduces the processing temperature in comparison with Au-Si. Further more Au-Sn eutectic alloy has higher thermal conductivity 0.57 w/cm-K compared with 0.27 w/cm-K of Au-Si. Also die bonded with Au-Sn will develop less stress from thermal expansion mismatch between the die and the substrate. Thus reducing the chances of die cracking which often experienced with Au-Si [24].

The above discussion leads to the selection of Au-Sn as a die attach media. So the die attach we do becomes eutectic die attach mentioned earlier.

### **2.2.1 About Au-Sn alloy**

80Au-20Sn eutectic solder is hard and moderately brittle. It has these properties as its constituent phases are two gold-tin intermetallic compounds, namely, AuSn ( $\delta$ ) and Au<sub>5</sub>Sn. Though difficult but this solder can be hot rolled to foils and stamped from it[24].

The alloy provides excellent wetting characteristics, great joint strength, superior resistance to corrosion, and superior thermal conductivity, making it the material of choice in many applications. Some major attributes of this alloy are listed below.

- Excellent wettability
- High joint strength, tensile strength is 275 MPa (40,000 lbs./sq. inch)
- Yield strength 31.5 psi x 10<sup>3</sup>
- Excellent resistance to corrosion
- High Thermal Conductivity 0.57 w/cm°C@85°C
- TCE (Temperature Coefficient of Expansion) matches many of the materials used in high reliability applications, viz., silicon, GaAs, GaP, InP, alumina ceramic, Kovar, Cu, CuW and alloy 42 viz., 16ppm/°C@20°C
- High surface tension, zero wetting angle
- Flux less soldering, the original flux-free reflow alloy
- Suitable for “step soldering” applications

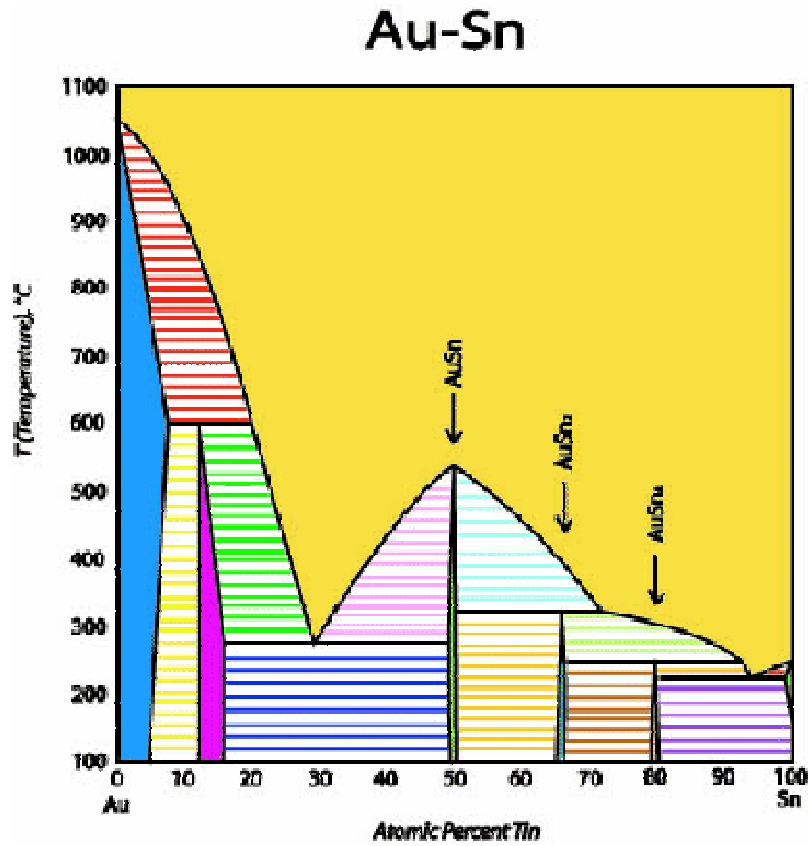


Fig 2.1 Phase diagram for Au-Sn Solder alloy

### 2.2.2 Process parameters for eutectic die attach

Gold-tin is generally used when joining gold-bearing surfaces, such as gold plating, sputtered gold films, Pt-Au, Ni-Au and Pd-Au thick film metallization. Because of the high surface tension and zero wetting angles Au-Sn does not flow easily on a horizontal surface, although it has excellent wettability, pressure is required to ensure good, void free, reflow.

Eutectic die attach should be performed in a dry nitrogen atmosphere to avoid the formation of oxides. A suitable nitrogen environment can be achieved by directing a

200 liter per hour flow through a nozzle onto the surface to which the die will be attached. Forming gas composed of 95% nitrogen, and 5% hydrogen will reduce organic contaminants on the substrate surface and may be substituted for dry nitrogen. The supply of gas has to be from a high purity monitored line and the oxygen content of the gas must remain below 20ppm. Thus, an oxygen monitor is highly desirable to ensure complete compliance to this level [25].

As mentioned earlier the dice have gold back metallization to facilitate achieving good eutectic die attach. To achieve a good die attach by placing a eutectic perform on desired location and appropriate pressure should be applied at the die interface to ensure good void-free spread of the solder, but with no agitation or ultrasonic assistance, as the eutectic is at a true 80/20[23].

This is not the case with, for example, the 98%Au-2%Si alloy used in silicon die-attach, as the true eutectic is at 3.1%Si. In this case, thermosonic power is required to scrub the die to diffuse the Si from the chip into the solder so that it reflows when that alloy percentage is reached. The scrubbing action here also ensures that the eutectic appears around the periphery of the die, visibly ensuring that the eutectic composition has been reached [24].

To ensure proper die attach following care should be taken

### **1) Using gold alloy pre forms**

The alloy elements and the percentage content in a preform will determine the melting temperature of the preform. Different alloys are available to meet particular

electrical specifications or assembly requirements. The working temperature should be well above the perform melting point so that full wetting can be assured. For this preform the recommended working temperature is  $310^{\circ}\text{C} \pm 5$  degrees [26].

All preforms should be stored in a dry nitrogen atmosphere to prolong their life by keeping them free of contaminants & oxidation. Contaminated preforms can only be spotted during the die attachment process. A bad preform shows signs of a blackish, dull tint. Sample preforms should be tested before the die is scrubbed into the preform.

#### Testing the perform

Place several preforms on a carrier. Use dry nitrogen or forming gas  $\text{N}_2\text{H}_2$  (95% / 5% respectively) to flow evenly over the hot plate at a rate of 200 liters per hour. Place the carrier onto the hot plate and watch the preforms start to melt (5 to 10 seconds) and spread out the preforms with a tweezer [23].

Good Preforms: Will appear shiny and smooth and will flow smoothly over the carrier surface.

Bad preforms: Will appear dull and wrinkled.

Bad preforms should be either discarded or cleaned. Buying preforms in small quantities and different lots assists in eliminating problems.

#### Preform Size

Care should be taken in choosing preforms of proper dimensions. Oversized preforms can increase costs and reduce die attach quality due to floating effect. Floating occurs when the preform is too large and results in poor thermal contact caused by the

chip floating on a bubble of melted preform. It is best to order preforms that are slightly smaller than the chip being used and/or allow plenty space for excess preform material to flow. The recommended thickness for preforms is .001 inch [23].

## 2) **Die attach Procedure**

- Set preform in position where die is to rest.
- Place die on same carrier to preheat.
- Place carrier on hot plate with some pressure on the die.
- Wait for preform to melt.
- Remove carrier from hot plate and cool on metal

## 3) **Some Die attach issues**

The Back of the Chip Wets 50% or Less

Reasons can be

- The back of the chip is contaminated.
- The preforms are contaminated or oxidized.
- There is not enough pressure.
- The process is performed in a non-clean environment.
- Oxides are forming due to insufficient or improper flow of dry nitrogen or forming gas.

The Preform Does Not Wet Properly

- The preform is contaminated or oxidized.
- There is no forming gas or there is an incorrect mixture.

- The substrate or carrier is contaminated.

### **2.3 Solder selection for optical fiber attach & fiber metallization**

Devices used for telecommunications or military application usually require operation for 20-25 years in field with potentially humid, corrosive, and mechanically turbulent environments. Long-term reliability in such harsh operating conditions requires hermetic sealing of the optoelectronic devices inside the metal housing. The optical signals are transferred to and from the housing by an optical fiber. For optoelectronic package, the optical fiber should have proper alignment to achieve good coupling efficiency by a joint. This operation followed by the feed through joint where the fiber enters the package is sealed hermetically.

There are two ways to make this solder joint hermetic.

- 1) Solder glass and 2) Metal solder or Solder alloys.

The joint with solder glass can be hermetic if the bond achieved is ideal. As the glass seal requires ideal surface conditions and uniform surface flow during the process which is difficult to obtain thus making it difficult to use it for fiber packaging. Also, solder glass has poor mechanical shock and impact properties, and possesses relatively low chemical resistance. The solder glass has higher liquidous temperature ( $>350^{\circ}\text{C}$ ) which makes to implement because the package usually contains other optical parts, such as die attach, optical components, which are soldered below  $350^{\circ}\text{C}$ . The solder joints inside the package will melt when the solder glass is reflowed. All the above mentioned issues make, the solder glass seal technique is not suitable in fiber attach for packaging.

Compared to the glass solder, the metal solder sealing technique has proved good hermeticity and long-term reliability.

The advantages of metal solders over glass solders are

- Lower melting temperature below 300°C, which will not melt solder joint inside the package.
- Good resistance to chemicals.
- Good mechanical shock and impact properties.

However, there is a need for careful selection of the solder and housing materials to overcome problems, like CTE mismatch induced stress, Au dissolution issue.

Before the solder sealing process, the fiber end inside the optoelectronic package should be aligned with laser or other optical parts to achieve low coupling loss, then bonded (by laser welding or soldering) to the substrate.

### **2.3.1 Optical fiber Metallization**

The optical fiber, i.e silica ( $\text{SiO}_2$ ), can't be directly soldered with metal housing. Hence metallization of optical fiber required for the purpose of wetting and solder ability.

Some important requirement for the optical fiber metallization is:

- Metal to silica adhesion.
- Metal solderability / wetting.
- Fiber strength is not degraded much.
- Fiber fatigue.



It is difficult get a metal coating that will suffice all the above requirements. But the most commonly used materials for coatings are Ni and Au. Metals with oxygen affinity show good adhesion to silica fiber. Hence nickel is generally used as first layer to be coated on the silica fiber and gold above the nickel [27].

The gold coating provides

- Coating for to prevent from oxidation.
- Gold does not oxidize easily so has minimum surface oxides thus helping fluxless soldering for sealing.
- Resistance to corrosion
- Protection from environmental moisture
- Solderability

The metallization sequence of Nickel and Gold is as shown in figure below

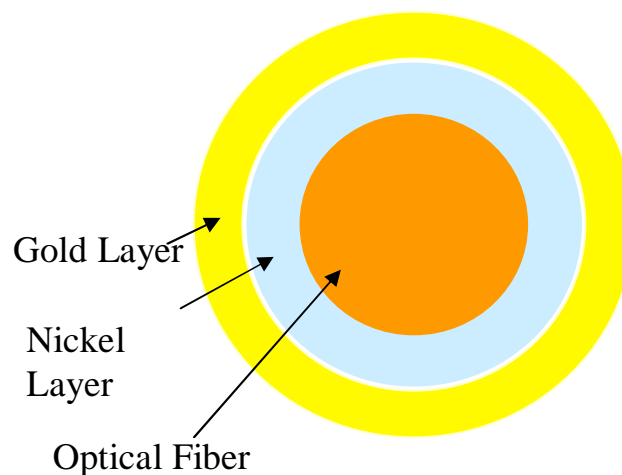


Figure 2.2 Metallization sequence on optical fiber

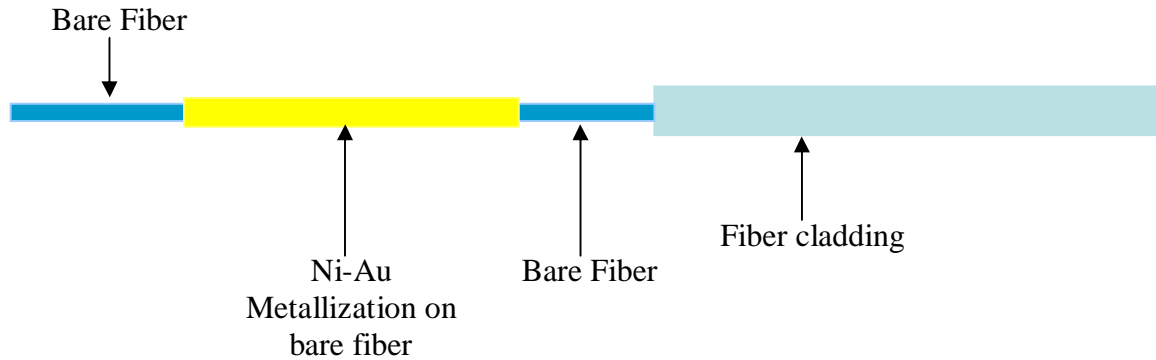


Figure 2.3 Side view of metallized fiber

#### 2.4 Solder Selection for Fiber attach

As mentioned earlier gold coatings are used extensively on photonic packages due to the reliability requirements. These coatings provides good corrosion resistance, excellent conductivity and optimal conditions for fluxless assembly, but the dissolution of gold into solder joints can cause solder joint embrittlement in the tin-based alloys which is generally used in electronics industry[28] . At normal reflow temperatures, the tin/lead alloy can dissolve gold films at a rate of 1mm/second. Once the gold content of the solder joint exceeds ~ 5 weight %,  $AuSn_4$  crystals form within the solder. The  $AuSn_4$  phase embrittles the solder joint, thus often resulting in a premature failure. This is particularly common in cases of extreme temperature cycling. The use of extremely thin Au metallizations (<1mm) has been investigated to minimize the Au available to the Sn/Pb solder joint. But, plating thicknesses in this range tend to be very porous, resulting in an extremely short shelf life of substrates and poor wetting to the underlying

(nickel) surface. Alternatively, increasing the amount of Sn in the solder alloy allows the absorption of a greater percentage of Au before the precipitation of the brittle  $\text{AuSn}_4$  occurs. Due to this dilution effect, the tin/silver eutectic alloy is sometimes considered for solder processes on gold films. However, to achieve the benefits of this approach the maximum thickness of the Au plating would still have to be so thin that the shelf life and solderability issues noted above would still be a significant problem [29].

Indium-based solders (indium/lead, indium/silver and indium/lead/silver) are a good alternative to tin-based solders when soldering to gold films. It has been demonstrated that a  $6\mu\text{m}$  thick gold film can withstand molten 50In/50Pb @  $250^\circ\text{C}$  for 15 minutes<sup>4</sup>. Gold will dissolve into indium/lead systems, a layer of  $\text{AuIn}_2$  forms at the joint interface. This layer acts as a barrier to further dissolution of the gold film. Further, the  $\text{AuIn}_2$  intermetallic that does form remains ductile, allowing for an effective solder joint with good fatigue life. While these indium alloys have favorable mechanical properties when used to make joints on gold films, wetting and corrosion resistance can be challenging when compared to tin or gold/tin alloys. In fluxless applications, the indium-based solder must be chemically etched to remove surface oxides. In addition, even with surface oxides removed, the use of ultrasonic energy may be required to promote good wetting [29].

Corrosion of indium systems within a hermetically sealed package is generally not an issue, provided there are no halides present. Indium alloy joints exposed to ambient conditions should be conformal coated to prevent corrosion. The corrosion

resistance of indium systems improves steadily as the indium content decreases, with compositions containing < 25 wt.% indium having very good corrosion resistance [29].

Some optical packages require optical windows to be incorporated into the package design. Putting an optical window into a Kovar package while maintaining hermeticity can be a challenging process. CTE induced stresses incurred during assembly and subsequent temperature cycling can put substantial stresses on this portion of the assembly. High tensile strength alloys such as gold/tin will transfer stress to the window which it, depending on the type of glass, typically cannot withstand, resulting in cracks and loss of hermeticity.

The use of pure indium and high indium content alloys as the solder or sealing material creates a glass to metal bond that offers a high degree of ductility while ensuring a hermetic joint. With very low tensile strengths (Pure indium @ 2.5ksi, 97In3Ag @ 5.5ksi), indium solder layers can deform to absorb any CTE stresses within the solder layer.

Whether using pure indium or an indium alloy, the solder preform should be pre-etched to remove surface oxides. This will improve wetting and flow characteristics in fluxless processes. In some cases, alternative metallizations may be considered for the bonding surfaces. Films of nickel are commonly used as the barrier layer with a top adhesion/protective layer of gold. Some nickel is dissolved into the solder joint during reflow. In cases where the nickel layer is too thin or porous solder adhesion can be compromised. Platinum has been investigated and is a very good alternative barrier layer for use with indium or indium alloy solders. At reflow temperatures the rate of

diffusion of platinum is very slow. The platinum that does go into solution remains at the joint interface and most likely acts as a barrier to further diffusion [29].

With the above discussion we can consider pure indium as one of the solders for fluxless soldering of metallized optical fiber to the metallized Kovar package or housing.

## **2.5 Package Housing material selection**

The coefficient of thermal expansion or contraction (CTE) of package material may induce stresses in both the fiber and the solder. Low expansion materials (Invar, C.T.E. = 1.4 ppm/°C) result in elevated tensile radial and tangential stresses in the glass and in the solder (both on its inner and outer boundaries) because of the big mismatch of C.T.E. So Invar is not suitable for the housing. On the other hand, high expansion materials, such as aluminum (CTE = 25ppm/°C), result in high compressive stresses and therefore should also be avoided. However, materials of moderate expansion, such as Kovar (C.T.E. = 5.86 ppm/°C), lead to moderate relatively low stresses in both the fiber and solder. Most popular material used in optoelectronic packaging is Kovar because of the lower stress induced to fiber in soldering process. The package is nickel-gold plated. The thickness of Ni is usually 0.5– 4  $\mu\text{m}$ , Au is 0.5 – 2  $\mu\text{m}$ , depends on different requirement [30].

## **2.6 Reliability testing**

Reliability is a critical issue in any product development. The products using MEMS technology is no exception. The central issue of reliability is that no matter how sophisticated a product is designed and manufactured, it becomes useless if it fails to

deliver the designed performance during the expected lifetime. Reliability of MEMS devices is critical as failure of these products can be catastrophic and devastating. Reliability is also recognized by the engineering community and industrial sectors as a major hurdle to commercialization of MEMS. So when all the soldering processes are complete it is important to test it for following test.

### **2.6.1 Die Shear test**

Die Shear Testing is the process of determining the strength of adhesion of a semiconductor die to the package's die attach substrate (such as the die pad of a lead frame or the cavity of a hermetic package), by subjecting the die to a stress that's parallel to the plane of die attach substrate, resulting in a shearing stress between: 1) the die-die attach material interface; and 2) the die attach material-substrate interface [31]. The general purpose of die shear testing is to assess the over-all quality of the die attach process, including the integrity of the materials and the capabilities of the processes used in mounting the die to the package substrate.

### **2.6.2 Hermeticity test**

Hermeticity testing is a failure analysis technique used to detect ambient atmosphere leakage paths into the cavity of a hermetic package. Leakage here refers to the free movement of moisture and gases to and from the package cavity through openings that an otherwise perfect hermetic seal wouldn't have. The amount of leakage determines the magnitude of the hermeticity failure of the package.

Hermeticity testing has two major categories: fine leak testing and gross leak testing. Fine leak testing checks for package damage or defects that result in very small leakage. While the, gross leak testing checks for large package damage or defects that result in gross package leakage.

The methods used to conduct fine leak and gross leak testing are very different from each other. As such, one can not substitute for the other nor can either stand alone. In fact, a unit that passes gross leak testing may fail fine leak testing while a unit that passes fine leak testing can fail gross leak testing. Thus, hermeticity testing can not be considered complete unless both fine leak and gross leak testing have been done [31].

### **2.6.3 Shock and vibration testing**

#### **1) Shock Test**

The Mechanical Shock Test is a test performed to determine the ability of MEMS devices to withstand moderately severe shocks resulting from suddenly applied forces or abrupt changes in motion encountered during mishandling, improper transportation, or field operation. Shocks of this type can cause devices to degrade in performance, or to even get damaged permanently. Shock pulses that are repetitive can also cause damage that is similar to those caused by extreme vibration.. Mechanical shock testing requires an apparatus that is capable of providing shock pulses of 500 to 30,000 g (peak), with the pulse width or duration ranging from 0.1 to 1 millisecond, to the body of the device package [31].

## **2) Vibration testing**

Vibration Tests are tests performed to determine the effects of mechanical vibration within a specified frequency range on semiconductor devices. There are two military standards that are widely used for this purpose: 1) the Vibration Fatigue Test, and 2) the Variable Frequency Vibration Test. Both vibration tests are similar in many aspects, although they are intended to uncover different types of vibration-related failures.

### **2.6.4 Thermal or temperature cycling test**

Temperature Cycle Testing or simply temperature cycling, determines the ability of parts to resist extremely low and extremely high temperatures, as well as their ability to withstand cyclical exposures to these temperature extremes. A mechanical failure resulting from cyclical thermo mechanical loading is known as a fatigue failure, so temperature cycling primarily accelerates fatigue failures. Thermal Shock Testing closely resembles TCT and also accelerates fatigue failures. TCT consists of subjecting the parts to the specified low (or high) temperature then subjecting the same units to the specified high (or low) temperature for a specified number of cycles using an equipment known as a Temperature Cycle Chamber[31].



## **CHAPTER 3**

### **SOLDERING EXPERIMENTS**

Equipments and Supplies needed for die attach experiments.

- 1) Hot plate with max temp up to 380°C.
- 2) Force Gage to apply pressure on the die.  
(Maximum capacity 5Kg, Resolution 25g)
- 3) Dice (Diced from wafer of thickness 500µm)  
(With 200Å Chrome and 2000Å Gold)
- 4) Kovar Plates (Drawing in the appendix)  
(Cut to 2 inch sizes from available strip)

To do the die attachment for the shear test the KOVAR package is to be replaced by a flat KOVAR plate. The package is electroplated with 50µinch of Nickel followed by 50µinch of Gold. The kovar plates were electroplated using the available setup.

#### **3.1 Electroplating Kovar Plates**

Equipments and supplies required

- 1) 3 plastic tanks and 3 Lids ( For degreasing, Nickel and Gold solution)
- 2) 3 300 W Heater
- 3) 3 thermostat
- 4) 2 Nickel Anodes with anode bandage

- 5) 2 gold Anodes(Stainless)
- 6) Nickel and gold crystals, Brightener, Distilled water

The electroplating procedure involves following Steps

- 1) Solution Preparation
  - i. Degreaser Solution

Degreaser solution is prepared by mixing 12 Oz of degreaser powder to 3 gal distilled water.

- ii. Nickel Brightener solution

Nickel solution is prepared by one pack of Nickel crystal to 1.5 gal of water.

- iii. Gold Solution

Solution is supplied by the vendor and is to be used as supplied and not to be diluted.

- 2) Surface preparation

The metal to be electroplated should have good surface finish. The component to be plated should be buffed and polished to get high quality surface finish.

- 3) Degreasing

The metal to be electroplated should be cleaned for any kind of grease on the surface. During degreasing the degreaser solution should be kept between 140°F to 200°F with the immersion of the component in the solution for 5 minutes. Immersion cleaning is followed by rinsing in distilled spray.

#### 4) Water Break Test

The water break test gives you an idea if there is oil or dirt on the metal surface. If the water beads up on the surface there is a residue of oil or dirt if its clean water covers up the surface.

#### 5) Calculating surface area current for plating

The plating time for both nickel and gold plating is determined by the surface area to be plated. For nickel the current should be 1 amp/16 sq” with voltage to be 2-4 volts approx. Similarly for gold plating the current is 0.003-.007 amps/Sq” and voltage being 2-4 volts approx.

#### 6) Tank Makeup

The tanks should place on a safe environment. The heater and the sample to be plated should be completely immersed in plating solution. The temperature sensor of the thermostat should be immersed in the solution too making sure that we obtain required temperature of the plating solution. The anodes for nickel plating are covered with a bandage while anodes for gold plating are immersed in the solution as is. The plating solution temperature for Nickel is 110°F and that for the gold is 140°F.

Following figure illustrates the plating tank arrangement

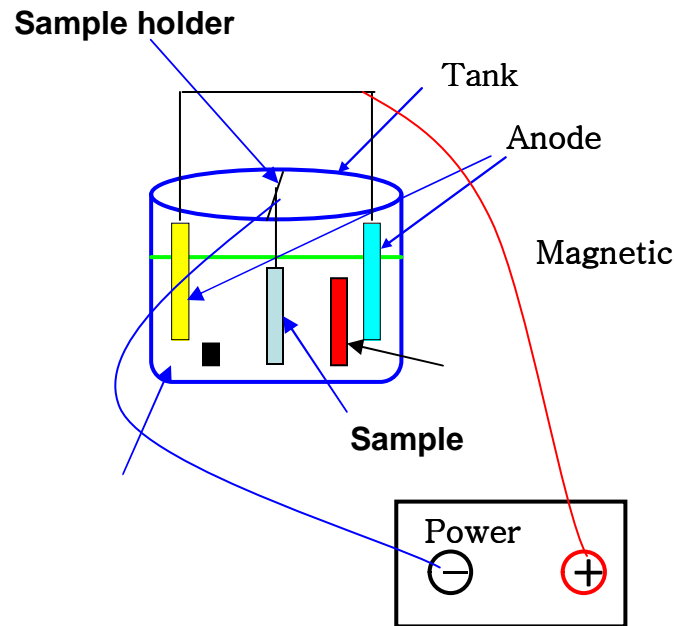


Figure 3.1 Arrangement of the plating tank with all the accessories

### 3.2 Die Attach Procedure & process parameters

The kovar plates electroplated earlier will be used for die attach. The kovar plates substitute for the real package. For the die attachment we need to ensure that all the parts are clean and dirt and grease free. The Die attach process could be listed with following steps.

#### 1) Cleaning of the Parts

The gold plated Kovar plates and the Solder Preforms are cleaned by immersing them in IPA for 10 minutes. The gold plated side of the die is cleaned by wiping the surface with no lint cloth dipped in IPA. All the parts are dried by blowing nitrogen on them and store them in contamination free environment. Earlier this wet chemistry cleaning was followed by argon based plasma cleaning but was further eliminated.

#### 2) Set up arrangement for performing die attach process.

The die attach process can be carried in clean room environment. Once the components are cleaned perform is sandwiched between the die and the plate substrate and kept on the hot plate.

### 3) Reflow process

As earlier mentioned in the solder selection chapter, the Au-Sn solder the melting point is  $280^{\circ}\text{C}$  and to get better soldering it should be heated to a temperature of  $30\text{-}40^{\circ}\text{C}$  above the melting point.

Once the plate, perform and the die are assembled and the required amount of force is applied by touching the tip of the force gage on the die as shown in the fig below.

For reflowing considering some heat losses the hot plate temperature is set to  $360^{\circ}\text{C}$ . Once the temperature reaches  $320^{\circ}\text{C}$  the solder is allowed to reflow between  $320^{\circ}\text{C}$ -  $340^{\circ}\text{C}$  for 2 – 4 minutes as suggested by the vendor reflow profile.

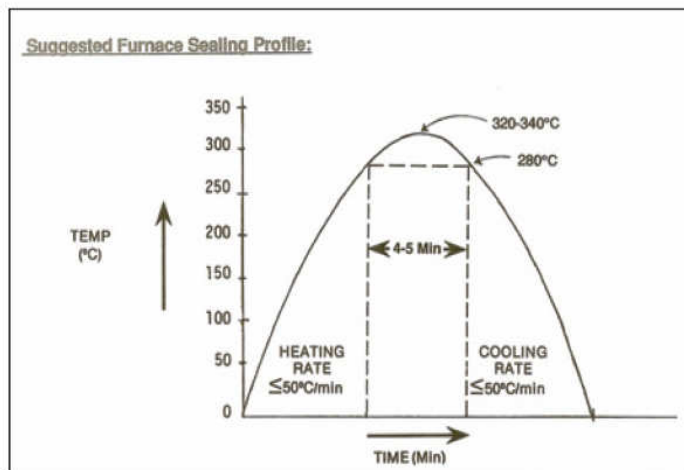


Figure 3.2 Reflow profile 80Au20Sn solder alloy

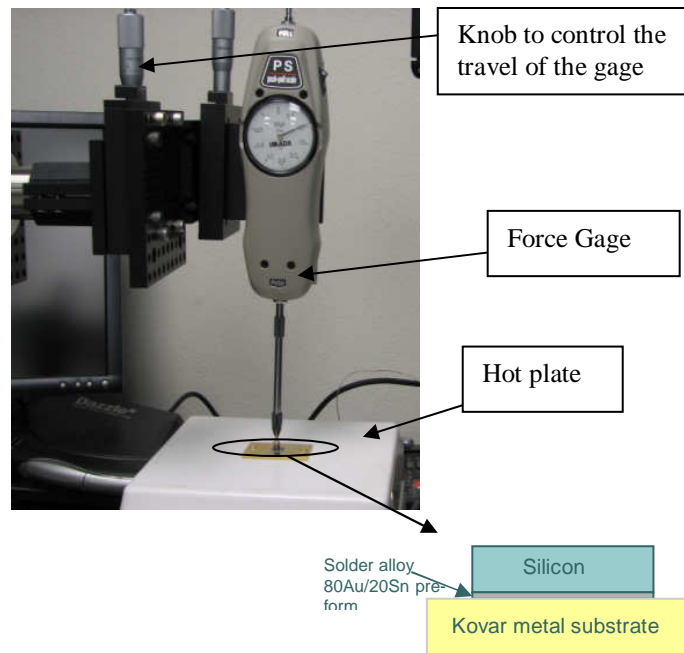


Figure 3.3 Die attachment setup with details of substrate to die assembly

### 3.2.1 Die attach experiments.

For die attachment there few experiments were conducted to understand and practice the process. Initially the die and the pre-form size was 12 mm × 12 mm followed by 10 mm × 10 mm die and 9 mm × 9 mm pre-form further die size was reduced to 6mmx6mm. The size was reduced to understand shear failure of the die attach.

The reflow can be distinguished with three stages with the hot plate

#### 1) Heating stage

Here the ramp rate should be kept close to 1-2°C per sec allows gradual evaporations of volatiles and prevents defects like solder beading.

#### 2) Reflow stage

A minimum peak temperature of 30°C-50°C above the melting point of solder is required to form a quality solder joint and achieve acceptable wetting due to formation of inter-metallic layers. A ramp rate of 2.5°C-3.5°C for solidus to peak temperature is recommended.

### 3) Cooling Stage

This stage refers to temperature range from peak temperature to approximately 50°C below the liquidus temperature where the cooling rate has negligible effect. A rapid cooling rate of <4°C is desired to form fine grain structure. Slow cooling may form a large grain structure, which generally shows lower fatigue resistance. With excessive rate >4°C both the die and the substrate may be stressed due to CTE mismatch.

Following the above procedures and stages few experiments were carried out using a hot plate and a separate kovar plate with a thermocouple attached was kept on the hot plate to measure the temperature during the process. Various experiments were carried out with similar re-flow profiles. As suggested by the vendor. Following graph shows reflows for 6 of the final samples.

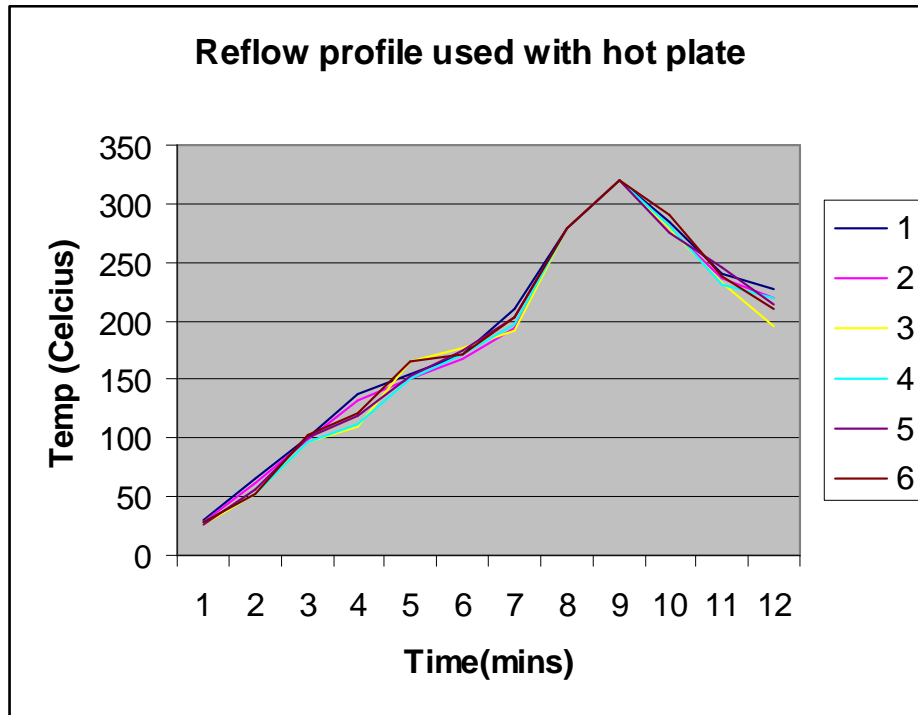


Figure 3.4 Measured reflow profile during Die attach

The ramp up rate of the process is dependent on the capacity of the hot plate.

Once the temperature of 30-40°C above the liquidus temperature is reached the kovar plate is taken off the hot plate and kept on aluminum block at room temperature and let it cool and temperature was recorded till about 50°C below the liquidus temperature.

Following picture shows die attached to metal substrate after reflow.



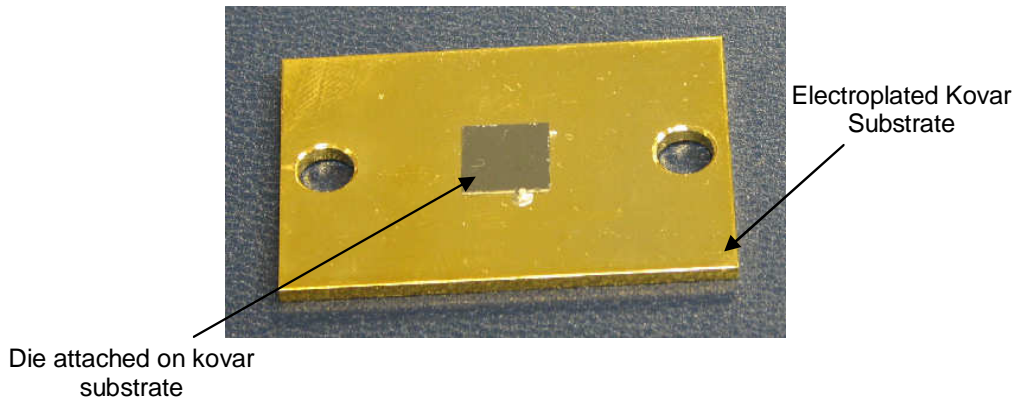


Figure 3.5 Die attached to a metal substrate after reflow

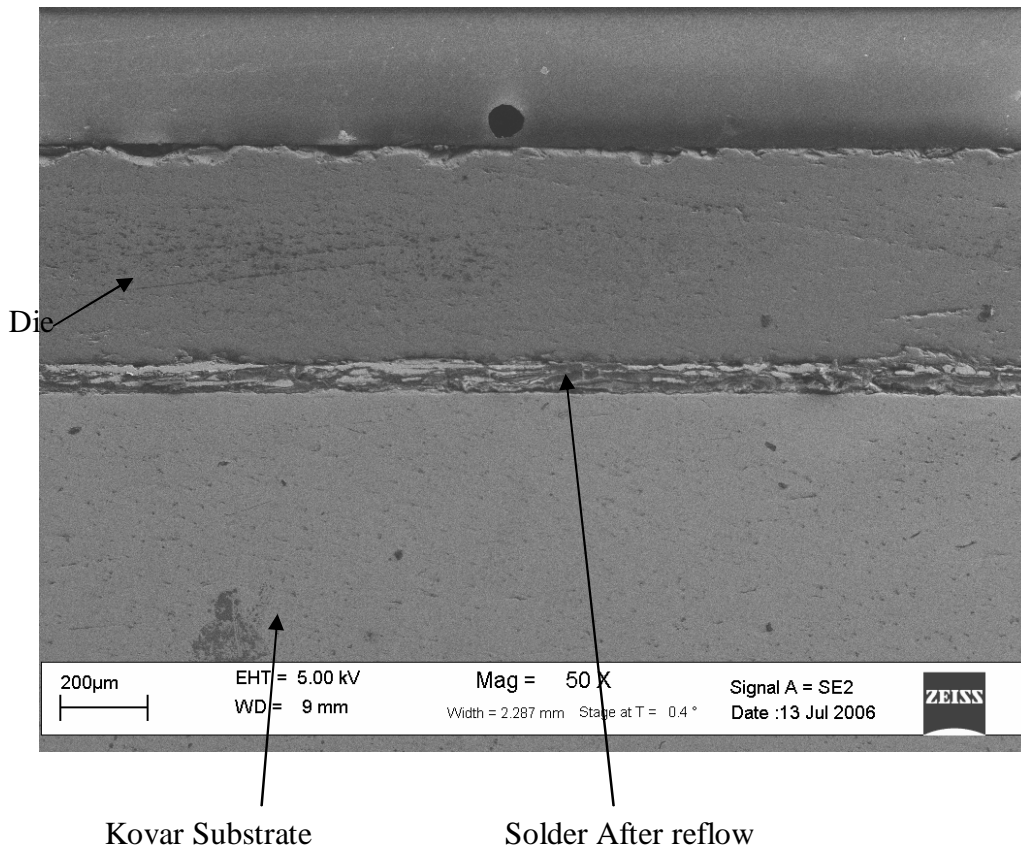


Figure 3.6 SEM image of the die attach

### **3.3 Fiber attach experiments**

#### **Cleaning**

For all these experiments the indium was cleaned by immersing the Indium in 10% HCL for 10 minutes and followed by rinsing in water and later with followed with Iso Propyl Alcohol (IPA) cleaning. After cleaning the indium was stored in a 4'' wafer carrier.

The packages and the optical fibers were also cleaned with IPA for 10 minutes immersion. After cleaning the packages black paint is put on the packages and then baked on the hot plate at 125°C for 30minutes. All the packages were stored in 4'' wafer carrier.

#### **Experimental Set up**

Equipments required for fiber attach Experiments

- 1) Indium ( Cleaned as mentioned above)
- 2) Dummy packager with black paint to avoid reflection from the package.
- 3) Optical Fiber gold coated on the soldering area
- 4) Gas enclosure
- 5) Ready supply of nitrogen.
- 6) Laser (available 30 w power)
- 7) Oxygen Sensor

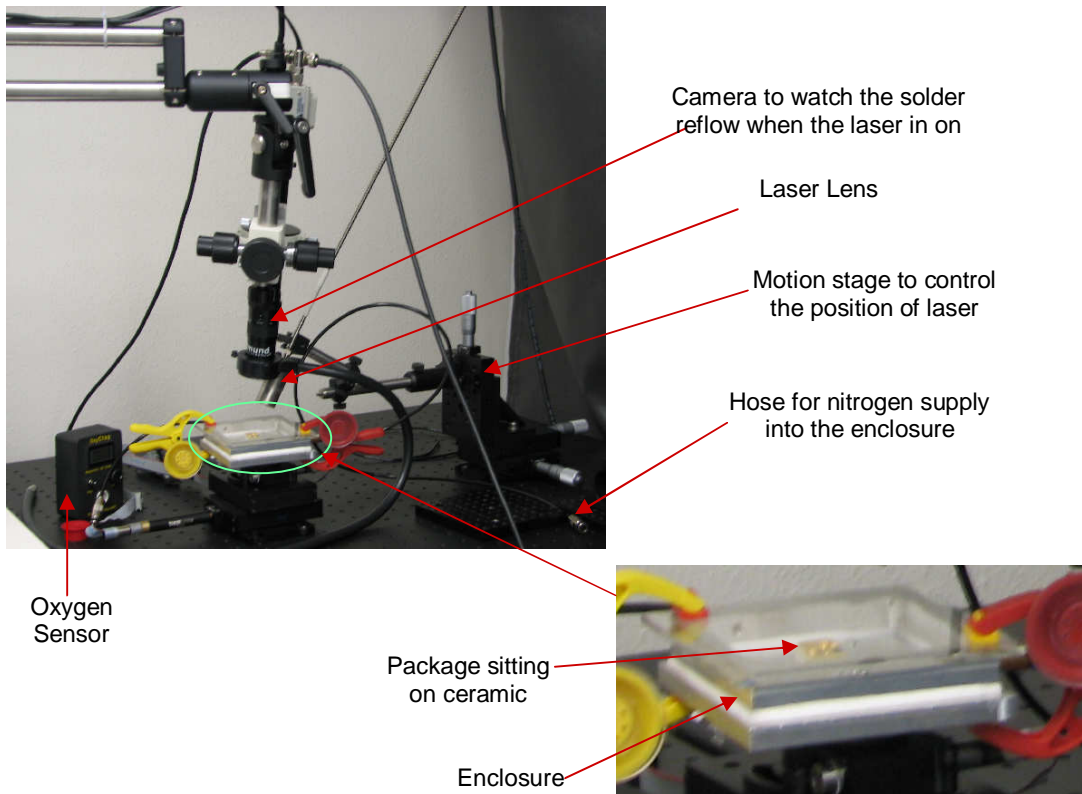


Fig 3.7 Experimental set up for fiber attachment

During the fiber attach experiments the ceramic is kept inside bottom metal plate and the package is then mounted on the ceramic (avoids heat dissipation to the bottom plate) and the fiber is inserted in the hole of the package followed by 6mm indium perform onto the top hole of the package.

After indium is set in the hole the glass enclosure is mounted on the bottom plate clamped diagonally to ensuring that it is almost air tight. After that the aiming beam is targeted at the black paint. The laser power is set 20w and the Nitrogen supply is turned on and respective oxygen level is recorded by the oxygen sensor. When the oxygen level goes close to 200 ppm the laser is turned on and kept on till the solder melts and spreads through out the hole which is viewed through over the package.

Few experiments were initially done to understand the process and practice it. Some experiments process parameters were recorded. The following table gives the details of parameters such as power of laser and time required for the Indium solder to melt. All the packages were stored in the desiccators box after the fiber attachment is done.

Table 3.1 Parameters for Fiber attach experiments

Sr.No	Power (W)	Heating Duration
1	20	3min 15 sec
2	20	48 sec
3	20	1 min 15 sec
4	20	1 min 50 sec
5	20	1 min
6	20	55 sec
7	20	55 sec
8	20	1 min 06 sec
9	20	1 min 20 sec
10	20	1 min 25 sec
11	20	2 mins
12	20	2 min 15 sec
13	20	2 min 25 sec
14	20	2 min 25 sec

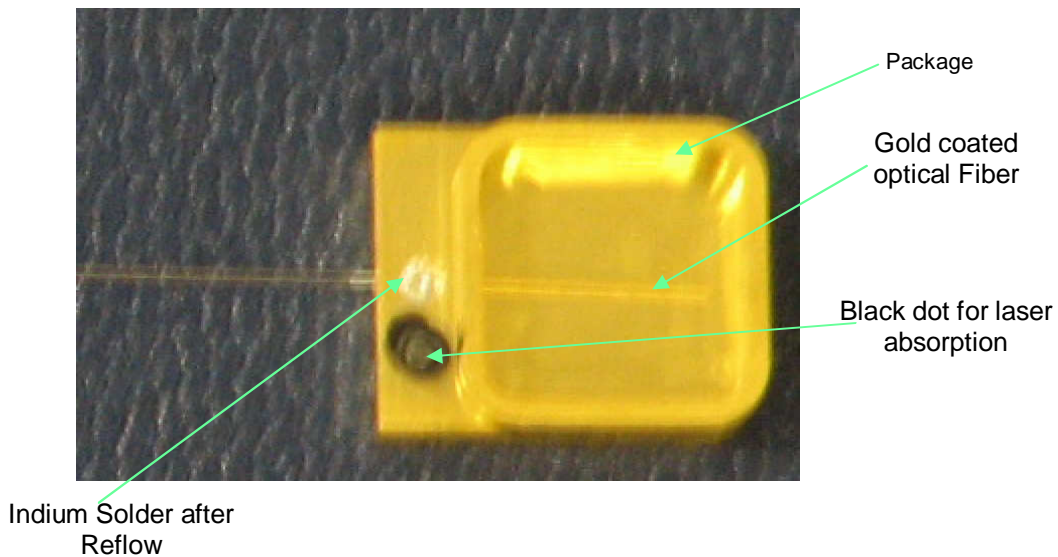
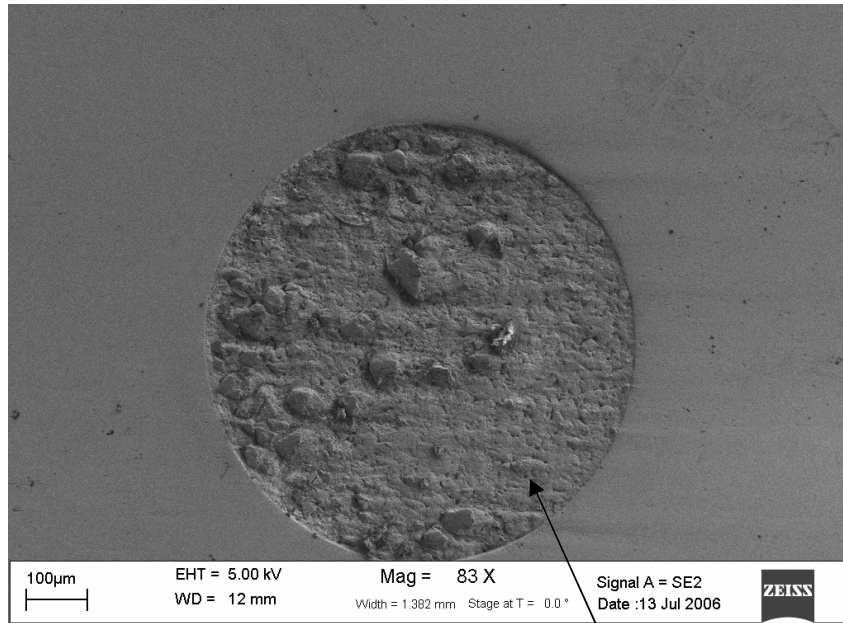


Figure 3.8 Indium after reflow for fiber attach



Indium after reflow

Figure 3.9 SEM of the fiber attach with indium

## **CHAPTER 4**

### **RELIABILITY TESTING AND TEST METHODS**

Reliability is defined as the probability that a device or a system will perform the required functions under stated conditions for a stated period of time. In many cases, the measure of time may be more appropriately expressed as the number of cycles, revolutions, or operations. A failure is said to have occurred when a device or a system no longer performs the required functions under the stated conditions within the stated period of time.

The requirements for reliability of a product can be differentiated with mechanical behavior and electrical characteristics of the overall system.

The failures can be categorized as

- (1) Catastrophic failures includes the total destruction of device and making it completely in operable.
- (2) Degradation failure includes the operation of the device outside its specified range of operation.

Failure modes refer to observable adverse effects as broken structures or cracked surfaces during field operation or during manufacturing. The failure modes also include degradation of directly measurable parameters exceeding the prescribed operational limits of the device. Thus a failure mode guided by description in terms of electrical quantities such as voltage current and power or mechanical operating conditions.

Failure mechanisms are the processes directly causing the observable failure mode. Generally, there is more than one level of mechanisms, starting from one mechanism leading to another, eventually causing the observable failure mode. Understanding the failure modes and mechanisms under different operational environments is a crucial part of addressing the issue of reliability, since mitigation strategies could be developed throughout the development and fabrication processes, and life cycle operation to ensure reliable operation of the device.

In Recent days MEMS devices are used in products or systems that require reliable operation over extended periods of time or have longer shelf life. One critical element in many MEMS applications is chip-to-substrate bonding. The substrate could metal, ceramic or PWB. For these long-term operation and storage reliability needs to be understood. MEMS packages are likely to have a large number of bond layers because of multiple interfaces inside the package. The bond layers in MEMS devices must often maintain precise chip alignment in addition to withstanding loading from the macro-environment and loading within the package. A primary indicator of failure in a chip-to-substrate bonded system is de-lamination between the chip and the material used to bond the chip to the substrate.

The bonding process has its importance in MEMS packaging, the earlier work on these process and process reliability assessment is limited. The focus of our work is reliability assessment and testing of chip to metal substrate bond using solder alloys and soldering without the use of organic materials such as flux also reliability assessment of

optical fiber attachment to a metal substrate using flux-less soldering for optical MEMS applications (MOEMS).

#### 4.1 Die Shear testing

The purpose of die shear testing is to evaluate the bond integrity between chip and the metal substrate by comparing to the shear strength of the bond.

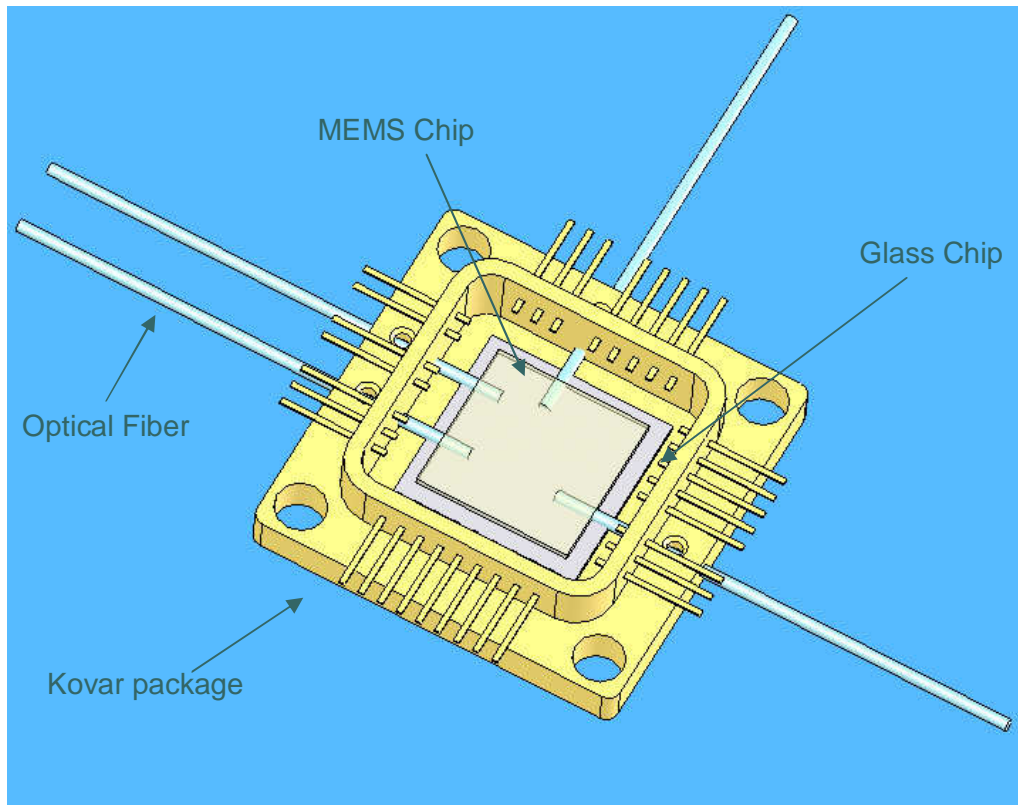


Figure 4.1 Schematic of a Package assembly with Die and glass chip attach

As mentioned in the earlier section different types of solders were considered and we selected 80Au/20Sn. The S&A chip is made of silicon and the substrate is made of kovar metal. The chip and the substrate have gold metallization on the surface



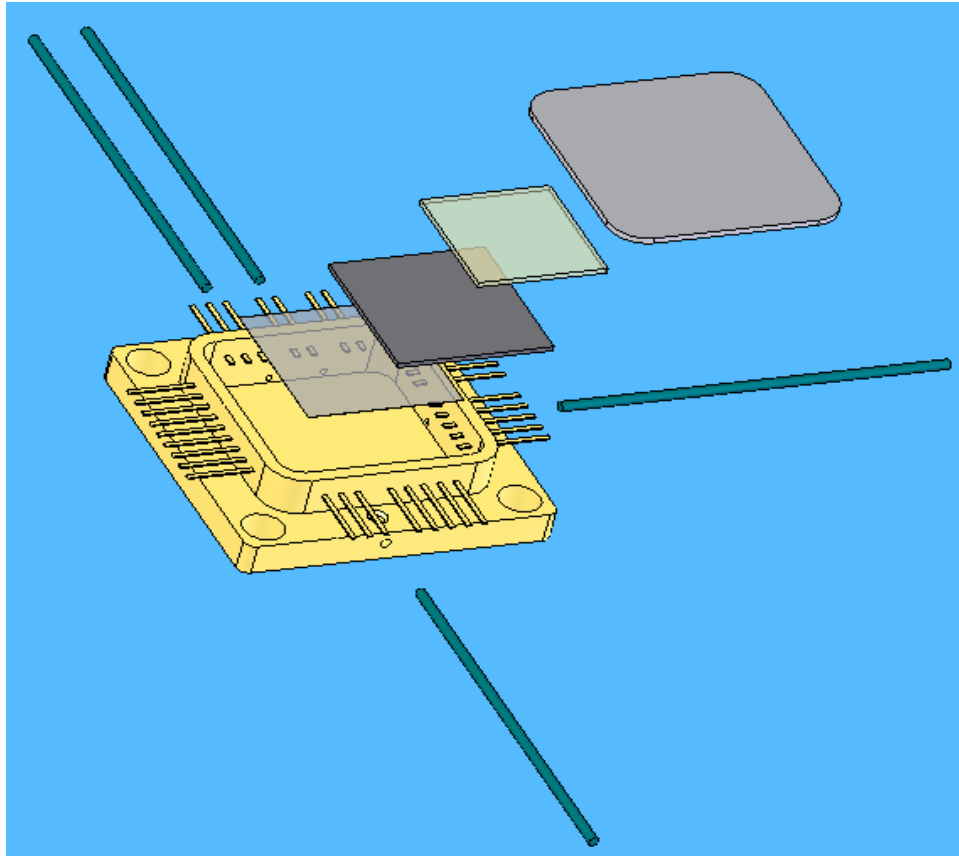
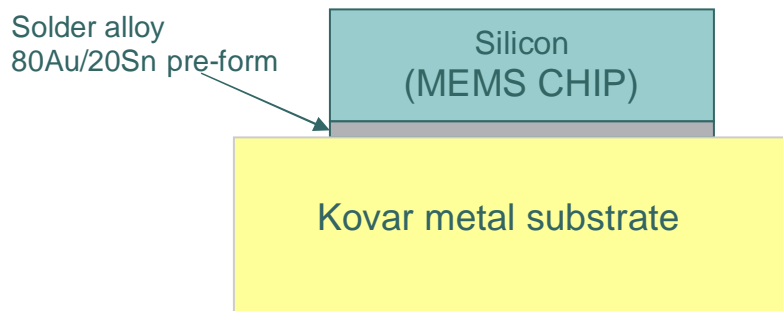


Figure 4.2 Exploded view of the assembly



The MEMS chip is 500  $\mu\text{m}$  thick and the solder pre-form is 25  $\mu\text{m}$  thick. For die shear testing the kovar package is replaced dummy gold coated kovar plate 0.1in thick.

### 4.1.1 Fixture for Shear testing

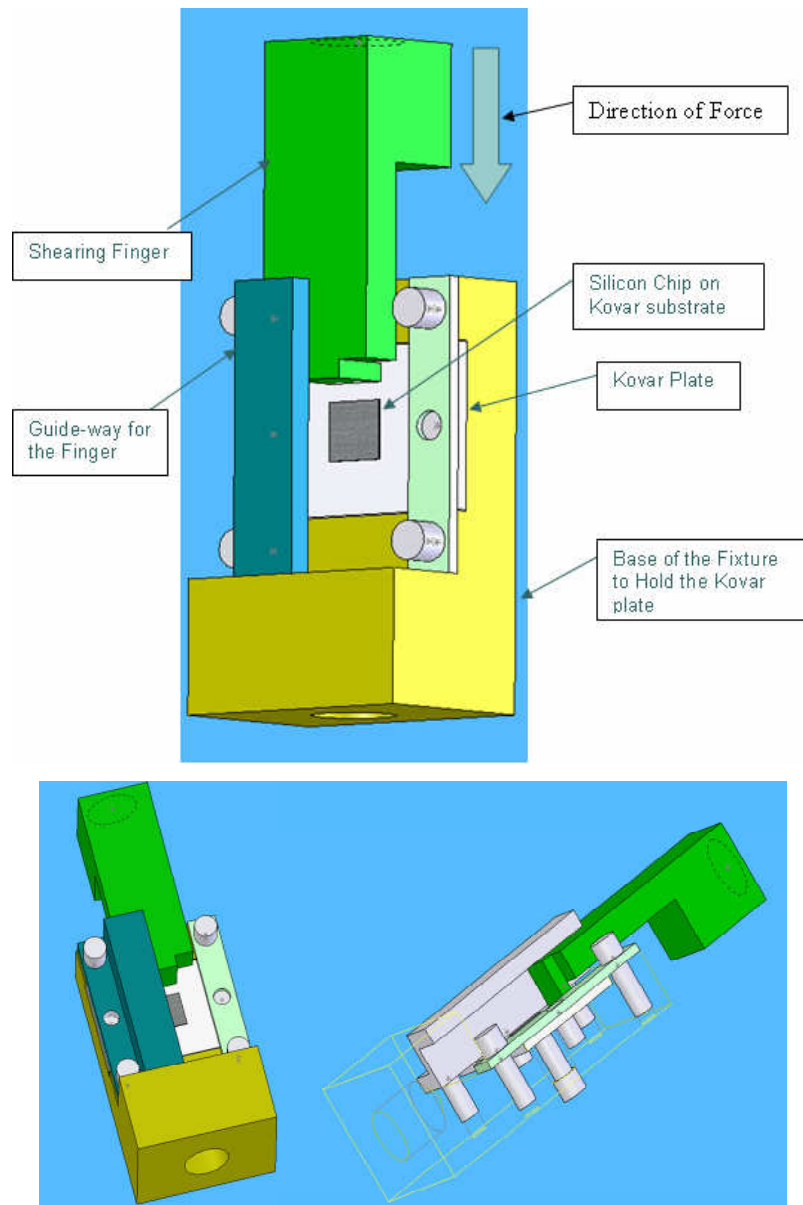


Figure 4.3 Schematic of a Fixture assembly showing different views

### 4.1.2 Test procedure

During die shear testing it is important that a pure shear force is applied to the bond between the MEMS chip and the kovar substrate. So it becomes important that the

face of the shearing tool is exactly perpendicular to the edge of the silicon die. Thus shearing tool cannot have out of plane motion and it should follow a fixed path. The guideway was redundant design so was eliminated during the testing. The base side of the fixture had a well of depth equal to the thickness of the kovar plate. So when the force is applied the motion of the plate is restricted in the well. To avoid the out of plane motion of the plate it was held by steel plate bolted to base side of the fixture. The movement of the tip of the shearing tool and the top of the kovar plate (i.e the bottom of the silicon chip) are in same plane following care was taken.

- 1) The center of the shearing tool and tip of the tool are in same plane.
- 2) The center of the base side and top of the well for kovar plate are in same plane ensuring the top of plate in same plane.
- 3) All the centers are matched to the center of the micro tester thus all the movement of the fixture in one plane.

After the fixture is assembled with the kovar plate (with die attach) on Instron micro tester the test is conducted using displacement control from the software of the micro tester. Once the shearing finger is brought almost in touch with the die the displacement on the actuator side of the tester is set to zero. Then maximum displacement is set to 3mm and the maximum loading condition to 490N and if any of the limit exceeds the test stops. With different control modes the mode that was set was the displacement control. The displacement rate was set to 0.10mm/sec and with displacement the corresponding force was recorded.

## **4.2 Military standard**

The entire tests are in compliance with the military standard MIL-STD 883F. For the die shear test the method adopted is 2019.7 for die shear strength.

According to this standard

### 1) Purpose

The general purpose of die shear testing is to assess the over-all quality of the die attach process, including the integrity of the materials and the capabilities of the processes used in mounting the die (and other elements, if any) to the package substrate. Mil-Std-883 Method 2019 is the most widely-used industry standard for performing

### 2) Apparatus

1) A mechanism that applies the correct load to the die with an accuracy of +/- 5% of full scale or 50 g, whichever tolerance is greater.

2) A die contact tool which makes the actual contact with the full length of the die edge to apply the force uniformly from one end of the edge to the other.

3) Provisions to ensure that the die contact tool is perpendicular to the die attach plane.

4) provisions to ensure that the fixture holding the die may be rotated with respect to the contact tool so that the die edge and contact tool may always be aligned in parallel to each other; and

5) A binocular microscope (10X min magnification) and lighting system to facilitate the observation of the die and contact tool while the test is being performed.

The force applied to the die during die shear testing must be sufficient to shear the die from its mounting or twice the lower specification limit for the die shear strength,

whichever occurs first. The direction of the applied force must be perpendicular to the die edge and parallel to the die attach or substrate plane. After the initial contact has been made and the application of force starts, the relative position of the tool must not change vertically, i.e., it must be prevented from contacting either the die attach material or the substrate.

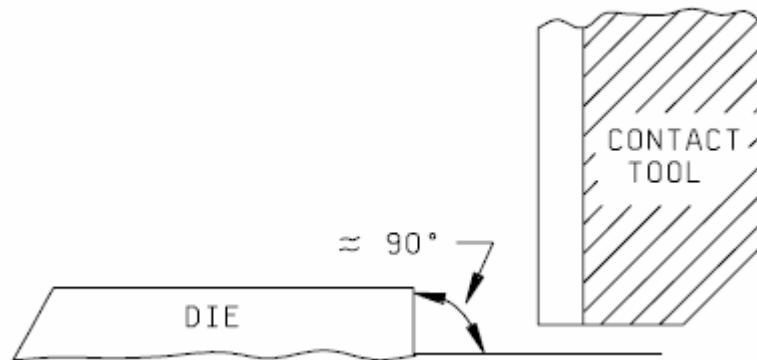


Figure 4.4 Angle between die and the shearing tool

#### Failure criteria

Failures from die shear testing include:

- 1) Failure to meet the specified die shear strength requirements.
- 2) A separation that occurs at less than 1.25X the minimum die shear strength and evidence of less than 50% adhesion of the die attach material.

3) A separation that occurs at less than 2X the minimum die shear strength and evidence of less than 10% adhesion of the die attach material.

The mode of separation must also be classified into and recorded as any of the following:

- 1) Shearing of the die itself with silicon remaining;
- 2) Separation of the die from the die attach material; and
- 3) Separation of both the die and die attach material from the package substrate.

### 4.3 Testing Set up

Before the testing was done some finite element analysis was done using Ansys workbench (Details in the appendix)

The fixture for die shear testing went through several design changes. The fixture shown above was the last. With each design few test were done as there were some unexpected results. All the tests with these fixtures were carried out on Instron micro tester.

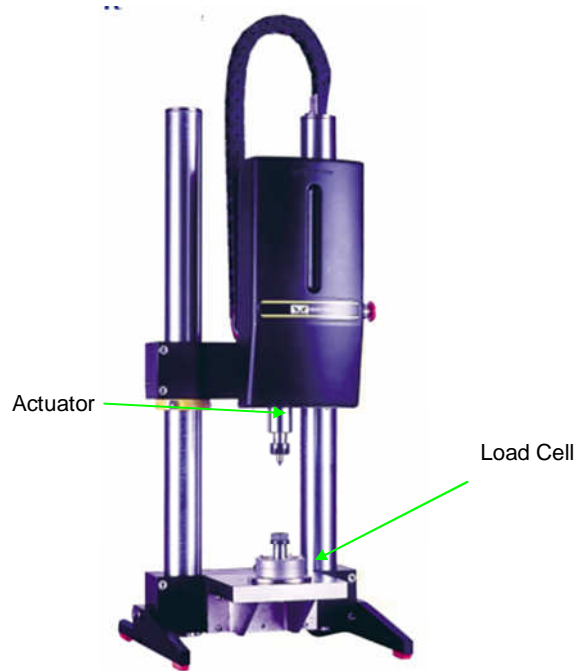


Figure 4.5 Instron Micro tester used for Die Shear testing

Following are some of the results of the tests conducted. With the first fixture design the tip of the shearing finger were movable. Offering ease of assembly of the fixture during

the mounting on the machine. Details of the fixture when assembled are show in the following picture.

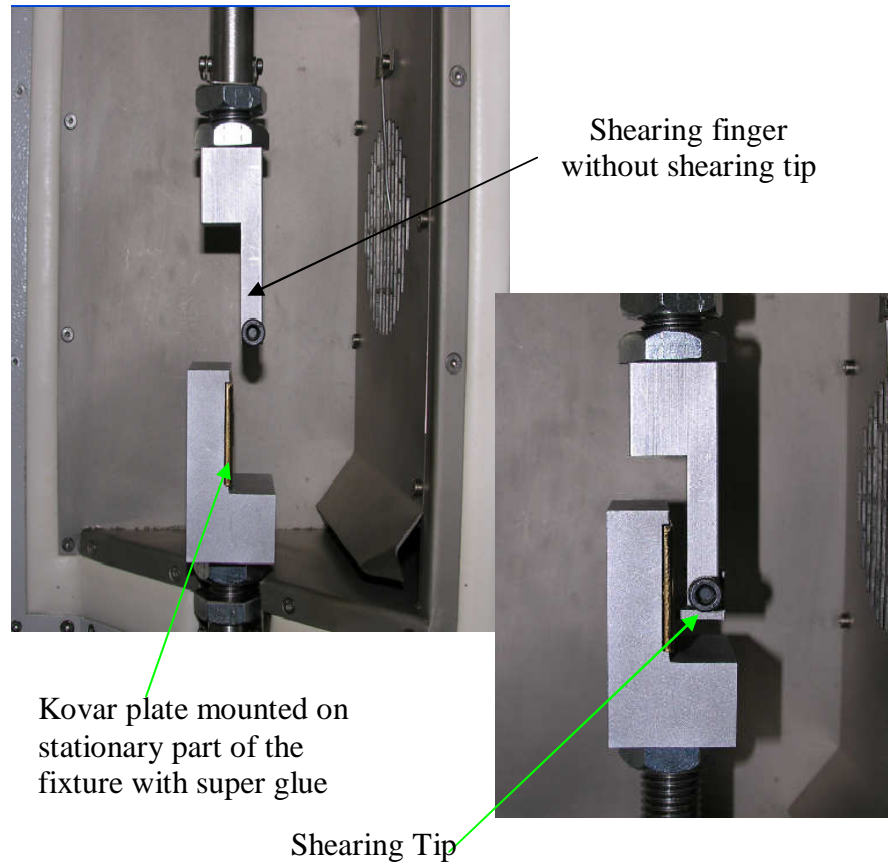


Figure 4.6 Initial designs of the fixture used for die shear testing

The problem with this design was that the when kovar plate was attached to the stationary side of the fixture with the glue was a possibility that the glue would interact with the shear strength also the possibility of the tip of the shearing finger would create some moment. Other Issue with this fixture was shear tool started slipping and breaking



the die because of lower die thickness and some tolerances. Also the tool would apply force inadequately (some times it would grip and sometimes lose the grip).

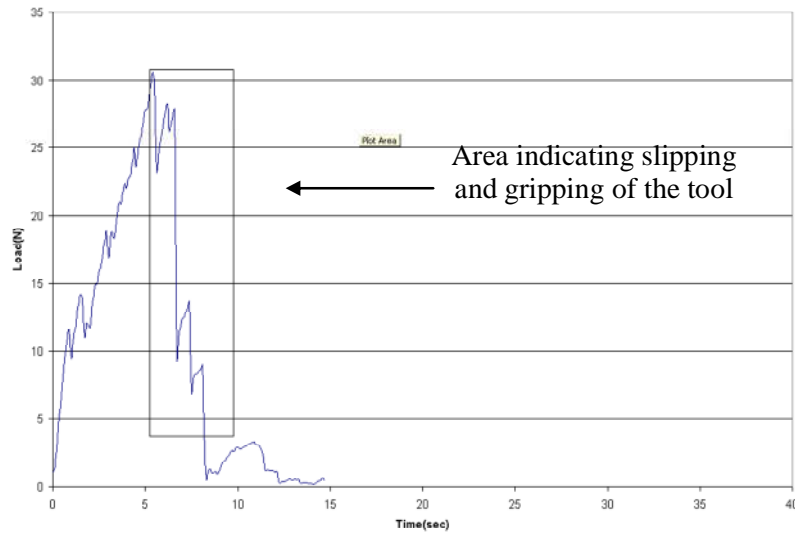


Figure 4.7 Load showing the fixture not holding adequate loading due to die thickness

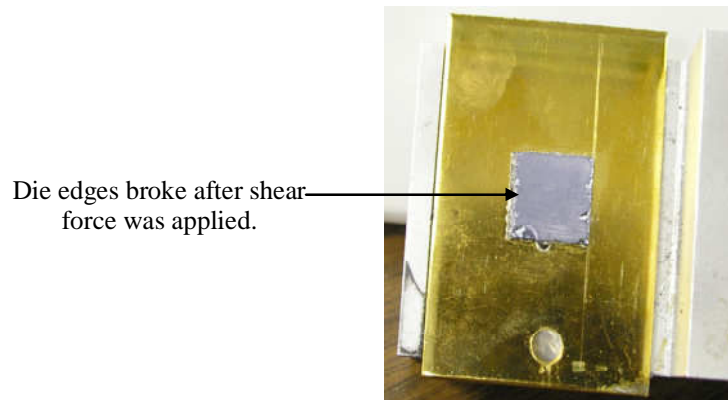


Figure 4.8 Cracked edges of the die with initial test of the fixture

As a result of which some fixture changes had to be made. The changes included permanent shear finger tip and a restrain plate on the kovar to avoid using superglue and

the top of the kovar plate and centers of both the sides of the fixture were kept in same line.

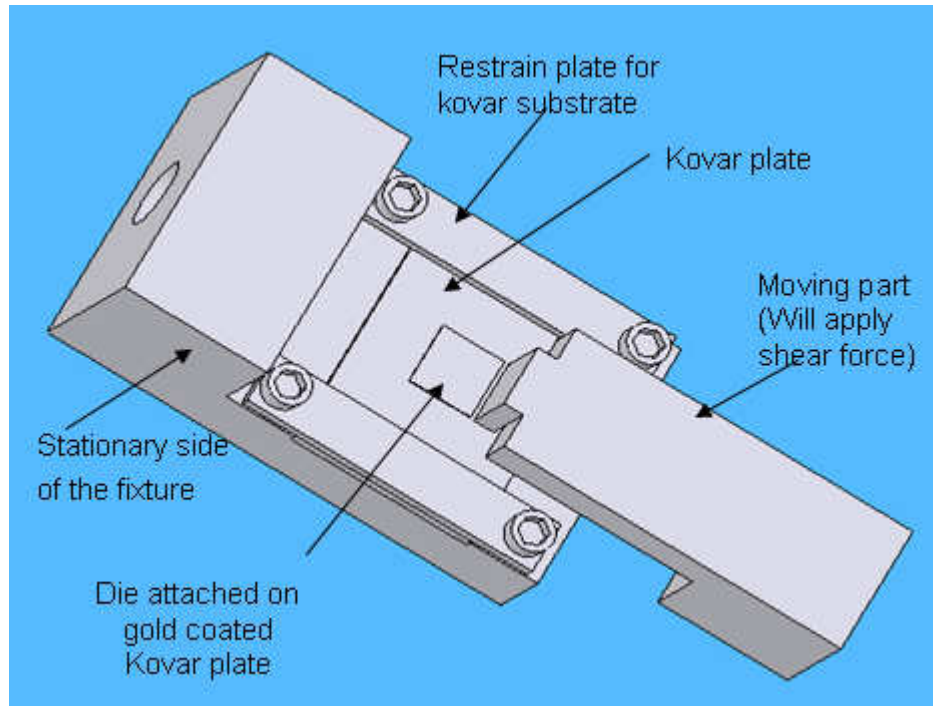


Figure 4.9 Changes made to the fixture to with no adjusting shear finger tip

With this fixture similar kind of problem was observed the as the earlier fixture. Like slipping of the tool on the die surface and uneven contact on the edge of the die making the die to crack at lower force than expected.

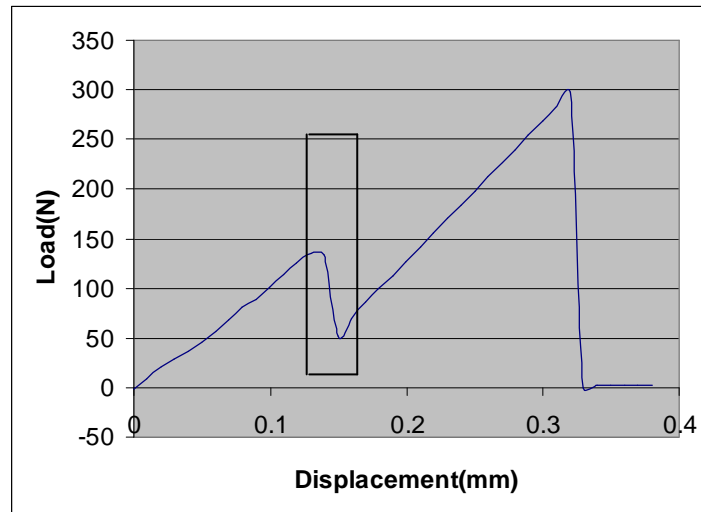


Figure 4.10 Uneven load distribution and die cracking at 300 N

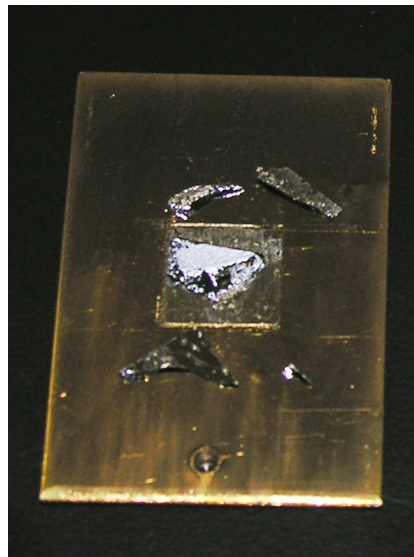


Figure 4.11 Die breaking after the load was applied with new Fixture design

One of the reasons for that the die would crack and the difficulty to apply the shear force on the die because of lower die thickness an aluminum piece extension was attached to the die to get a standoff for the shearing finger.

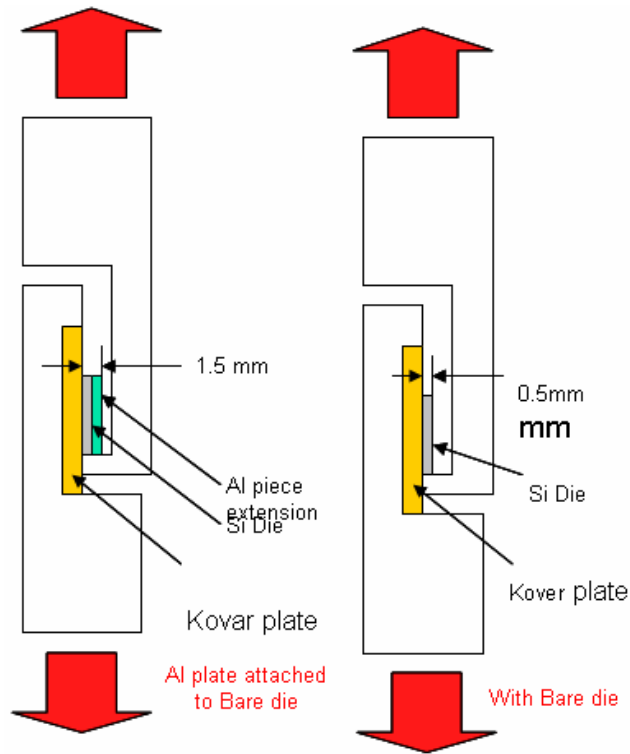


Figure 4.12 Arrange of extension attached to the die with superglue

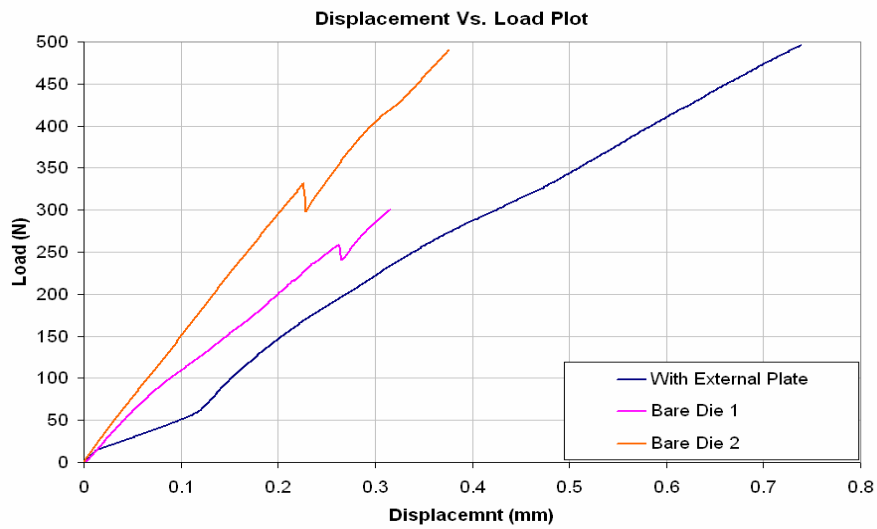


Figure 4.13 Comparison with bare die and plate extension

With this change we got an idea that the die can with stand higher load as the joint with super glue did not fail. So there was the need that the die edge and the tip of the

shearing finger are in complete contact with each other and perpendicular to each other. Later design changes were the last changes. The final fixture design changes are described earlier.

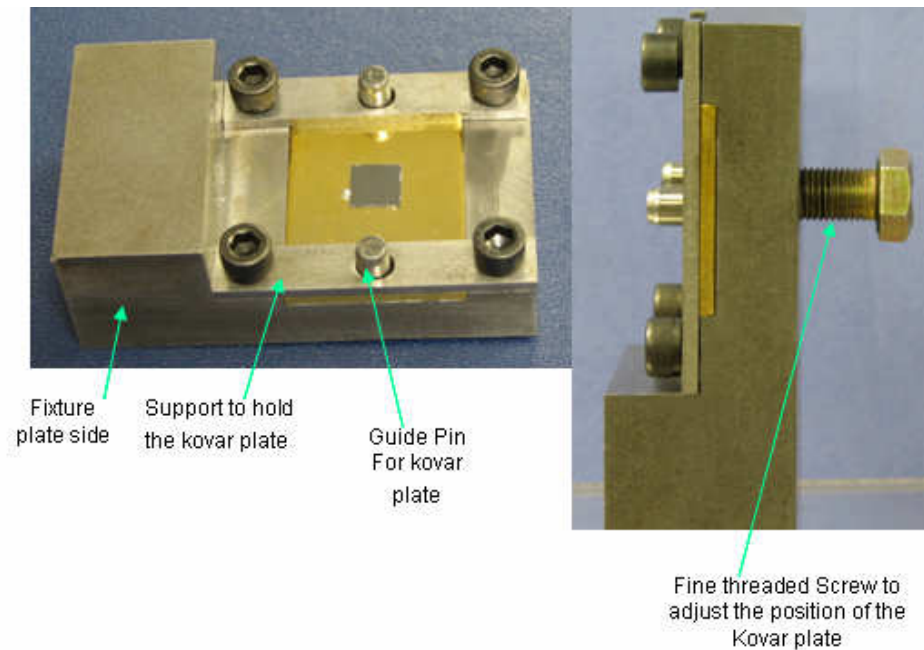


Figure 4.14 Die attached Plate assembled on the fixture

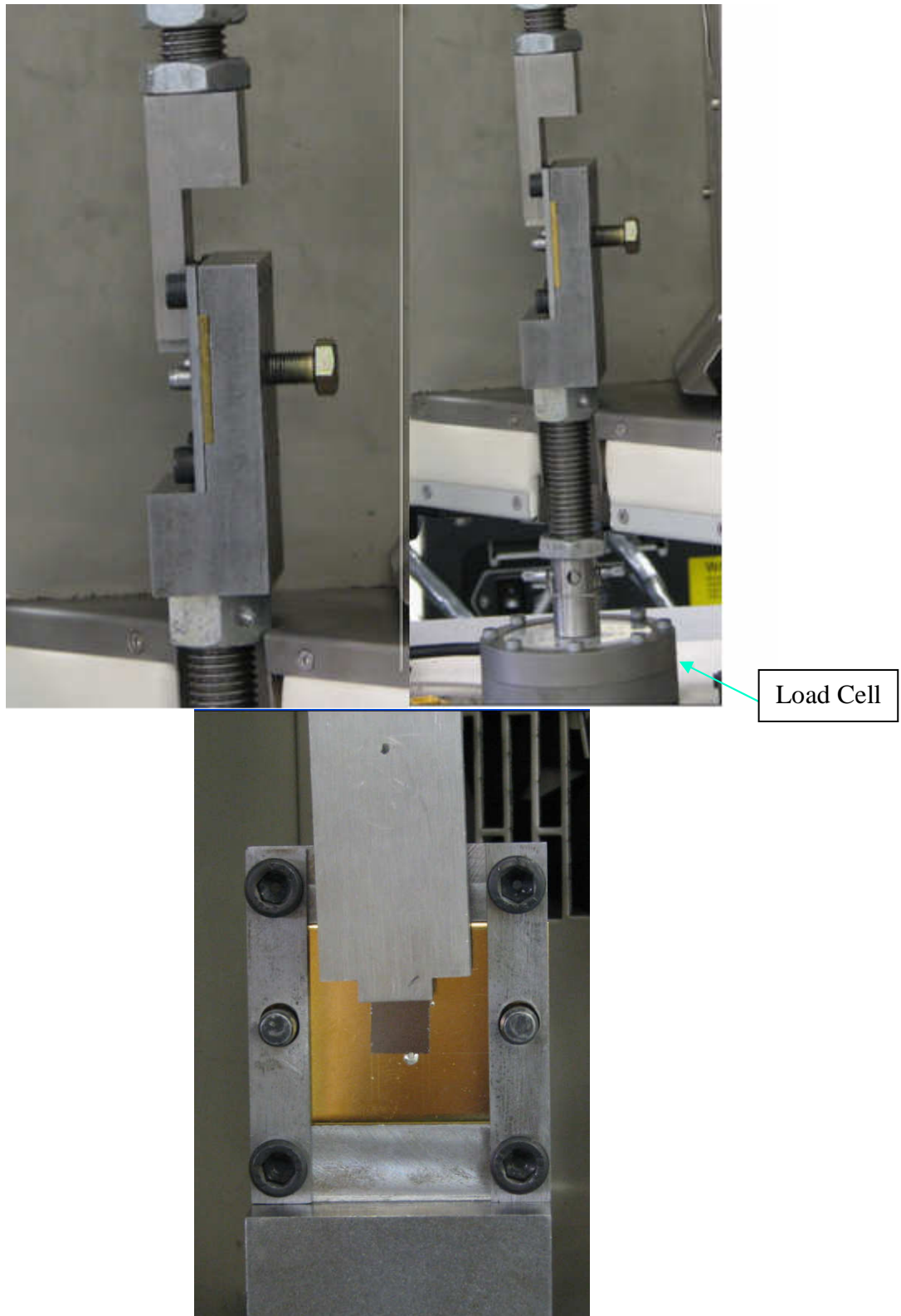


Figure 4.15 Fixture assembled on the micro tester with latest fixture design

## 4.4 Results

For these the load on the machine was applied in compression. Following results will indicate the compressive load applied on the dice.

### Test one

Load applied on the die during the die attach process 0.5 kgf

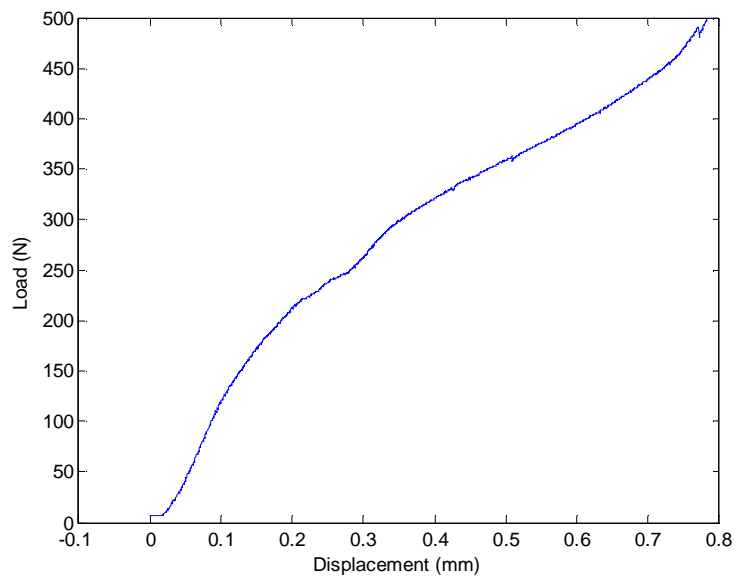


Figure 4.16 compressive Load against displacement test one

As shown in the die to substrate joint did not fail with 500 N. As result one more test was run where the load used for die attach was 1.5N with other parameters being same.

### Test two

Again for the test two the joint did not fail but the edges of the silicon were cracked. As the silicon was cracked we attached a extension on the die to get a stand off as done earlier to understand if the die would crack with the similar amount of force. The extension piece attached was Small metal piece.

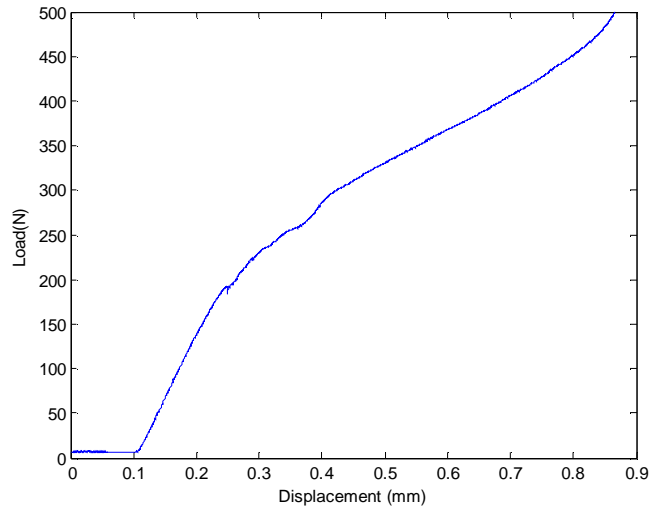


Figure 4.17 Compressive load against Displacement for test two

Again the die with extension attached on it did not fail with 500N load. We implied that the solder joint area is too large. Giving it higher shear strength. Further the die size was reduced to 6mmx6mm keeping the perform size to 9mmx9mm. With this die also the joint did not fail. So there is need to reduce the area further and test the joint

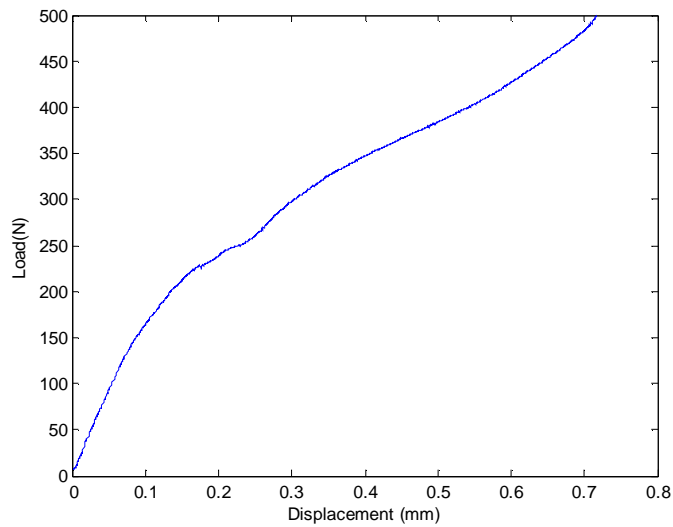


Figure 4.18 Compressive Load against Displacement with Aluminum extension



Further the die size was reduced to 6mmx6mm and was tested for shear loading. This die also did not fail with 500N load.

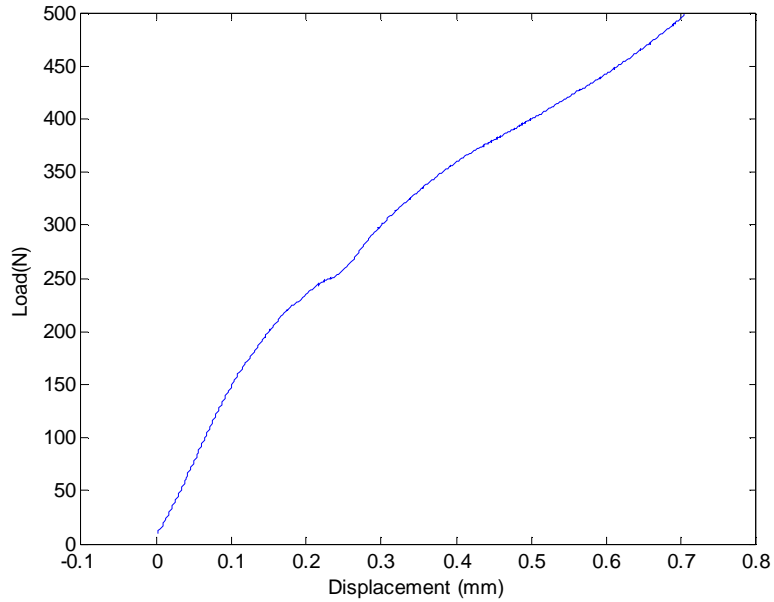


Figure 4.19 Compressive load VS Displacement for 6mm die

#### 4.5 Fiber Pull Testing

The purpose of fiber pull test is to evaluate the bond integrity between the fiber and the kovar package by determining the strength of the bond in tensile loading. The fiber is bonded to the package using 99.99% indium as a solder.

#### 4.5.1 Test set up and Testing

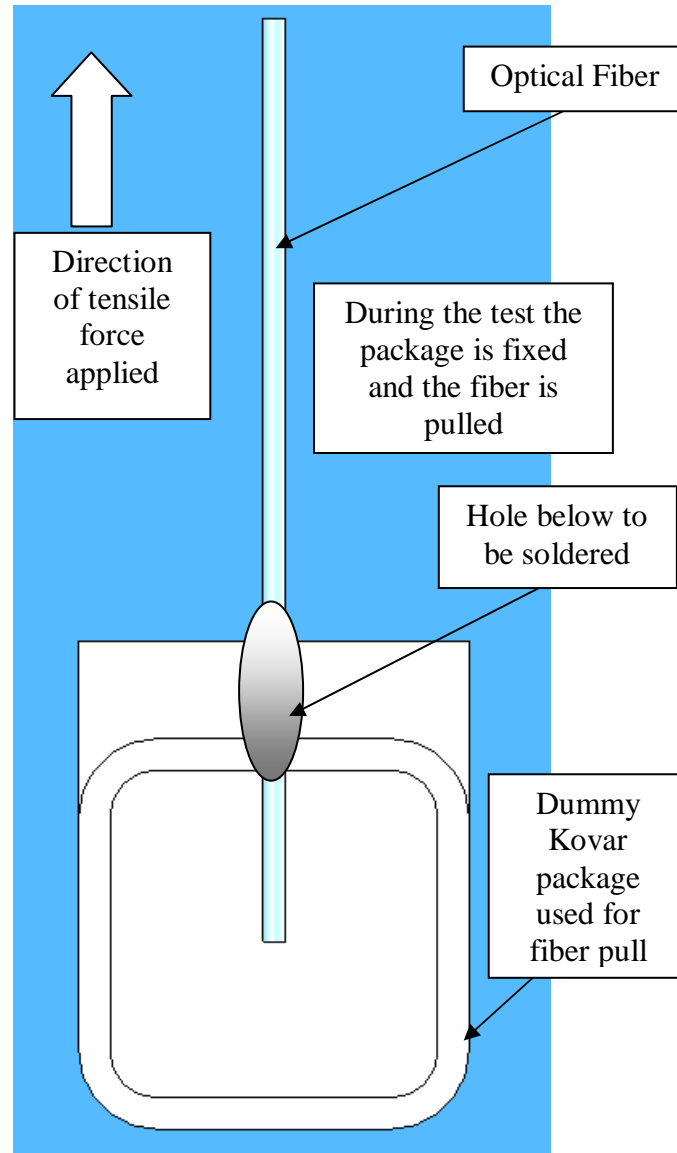


Figure 4.20 The arrangement of optical fiber pull test

This test was also done on the Instron micro tester used for die shear earlier. In displacement control mode with the displacement rate of 0.01mm/sec. For the first test the package with fiber attached was directly mounted on the stationary side of the tester

with the help of self centering grip. The fiber was gripped at the other end also with self centering grip with two rubber pads to avoid slipping of the fiber from the grip.

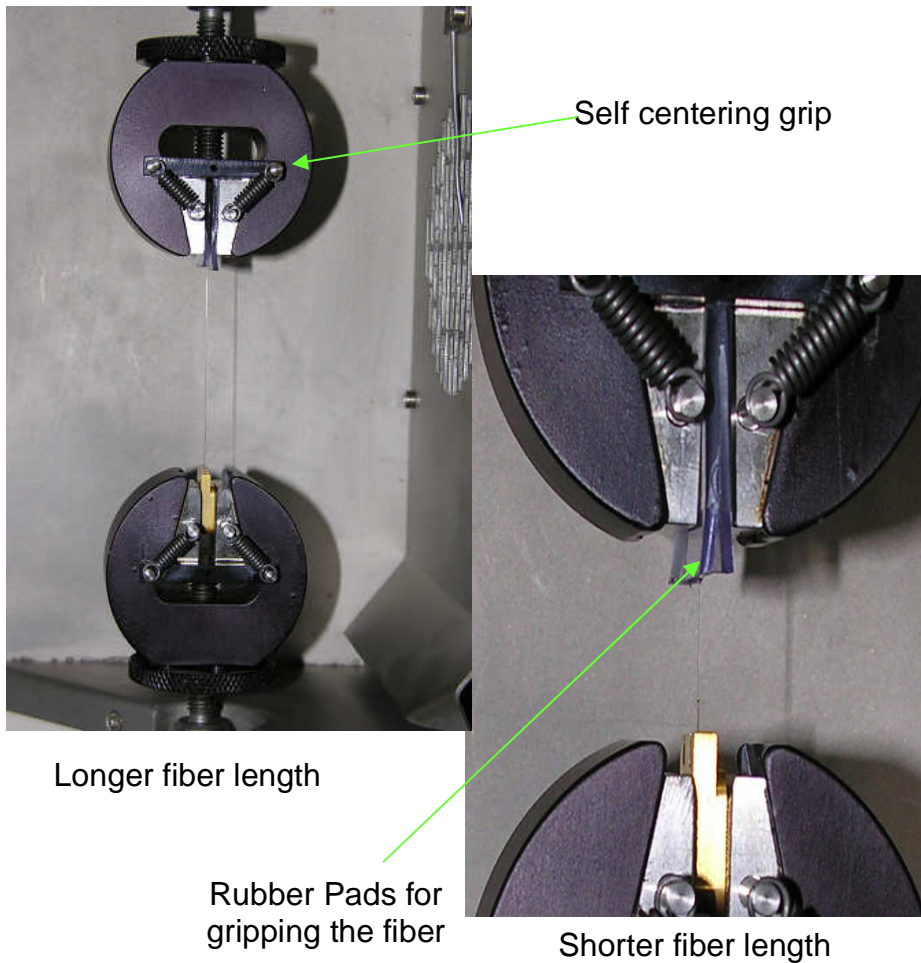
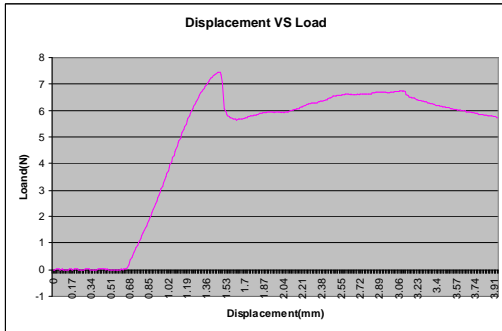


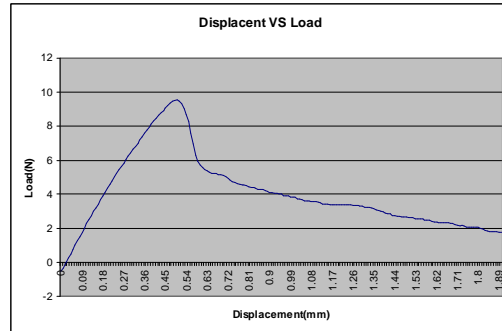
Figure 4.21 Assembly of fiber attached package on the instron micro tester

For the first test sample the fiber was attached to the package using flux and for the second test sample the fiber attach was done in inert environment with no flux.

For fiber attached with flux shows the joint failed at 7.5 N but at initial stage of the test slippage of the fiber. As there was slippage during the first test the fiber length was shortened the graph shows that the joint failed close to 9 N.



(With Flux)



(shorter length)

Figure 4.22 Load V/S Displacement fiber attached with flux & after fiber length Shortening

As there was a slippage issue with the rubber pads to grip the fiber at the moving end the idea of using the rubber pads was discarded. Alternative to that was to use a capillary tube having inner diameter slightly greater than the diameter of the fiber but the available capillary tube had an inner diameter close to the fiber core. So to insert the free end of the fiber into the capillary tube fiber was stripped using the fiber stripper and the capillary tube was inserted into the fiber.

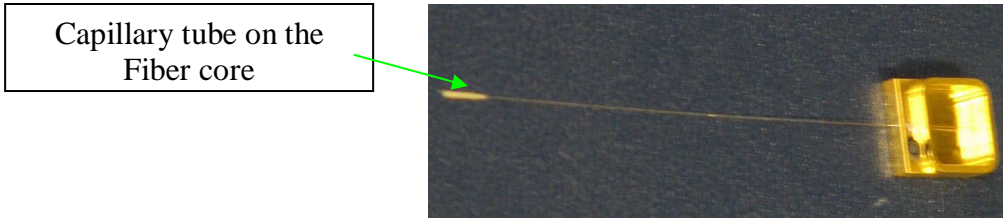


Figure 4.23 Fiber attached to the package and the optical fiber with capillary tube

The capillary tube helps in holding the fiber without damaging it and avoids the breaking of fiber because of the compressive force by the grip. The capillary tube provides a cushion and grip for the fiber. While mounting the package on the grip a shim of 0.16 in was inserted between the package and the grip towards the bottom side of the package. The purpose of the shim was to align the center of the hole (Provided for fiber insertion) to the center of the actuator or the center of the tester.

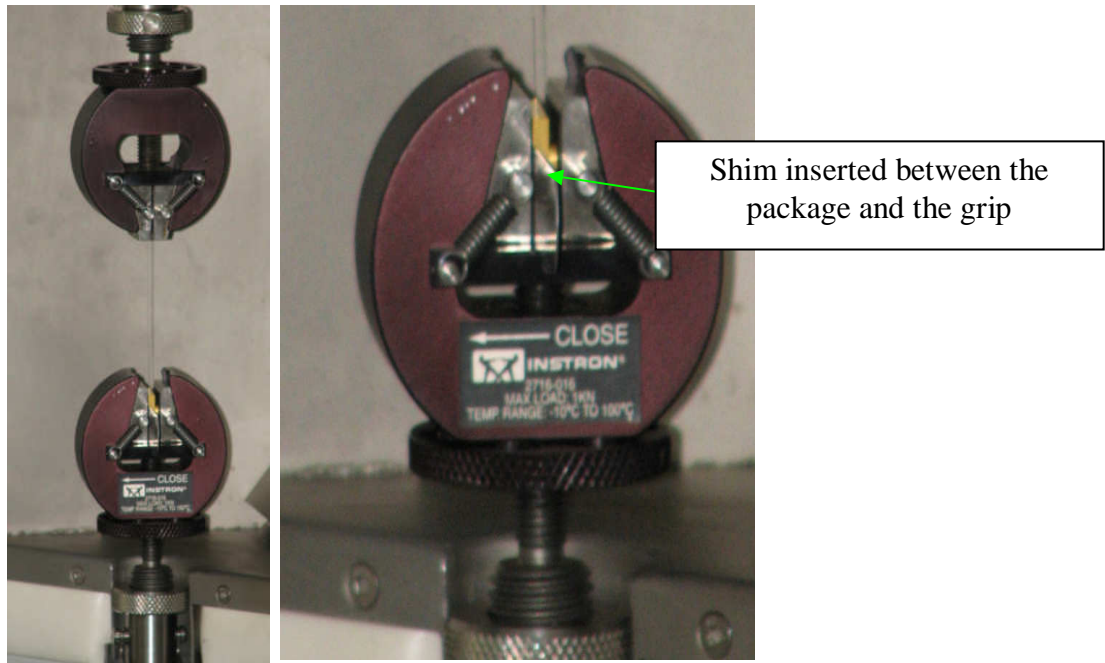


Figure 4.24 The fiber test set up with changes showing the magnified image of the adjustment made for centering the hole on the package

## 4.5.2 FEA Analysis

Some FEA analysis was done to understand the failure pattern of indium following picture explains the simulation results using Cosmos the fem tool in solidworks. For this simulation a load of 7.5N is applied at the inner surface of the indium. As yield strength of indium is 2.14 Mpa the indium will fail around 2.14 Mpa and the maximum stress induced is 10.95 Mpa.

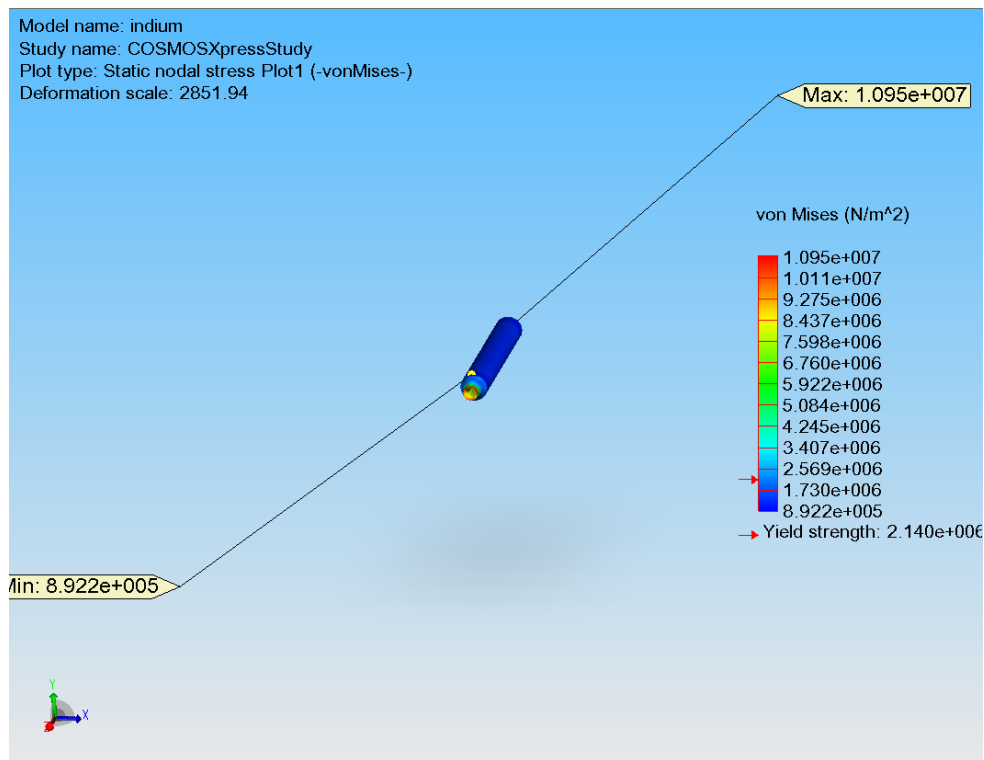


Figure 4.25 FEM results on pure Indium (Material properties as supplied Indium Corporation)

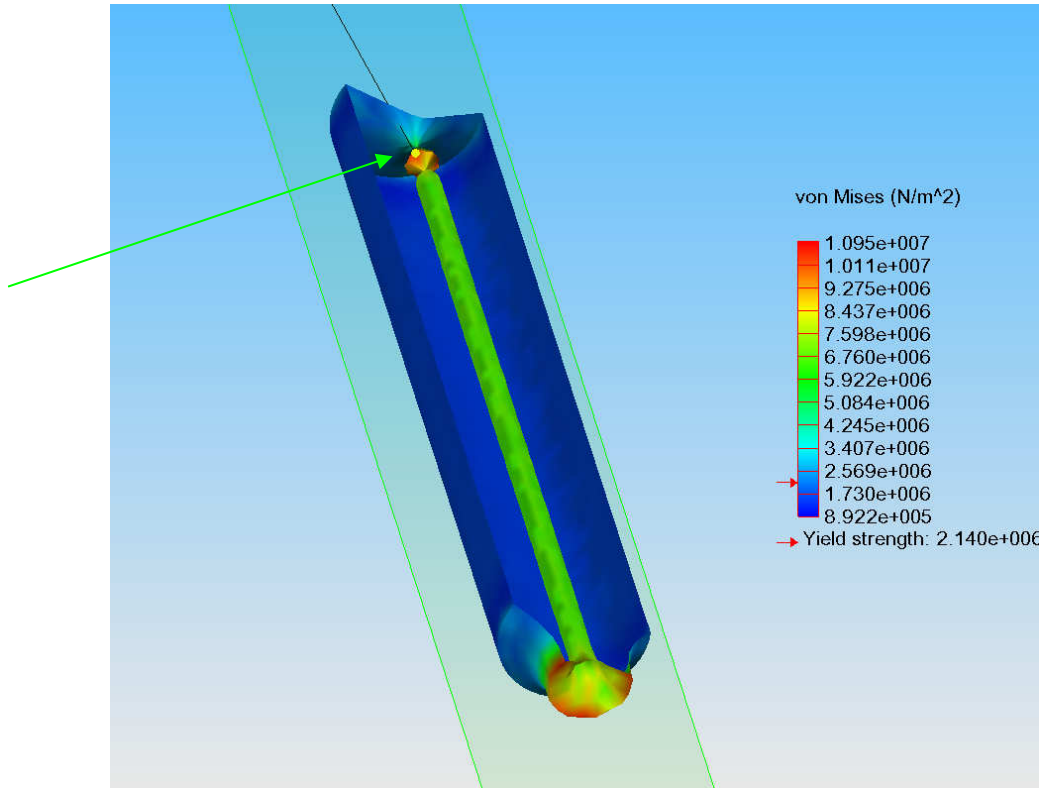


Figure 4.26 Sectional view of Indium indicating maximum stress induced

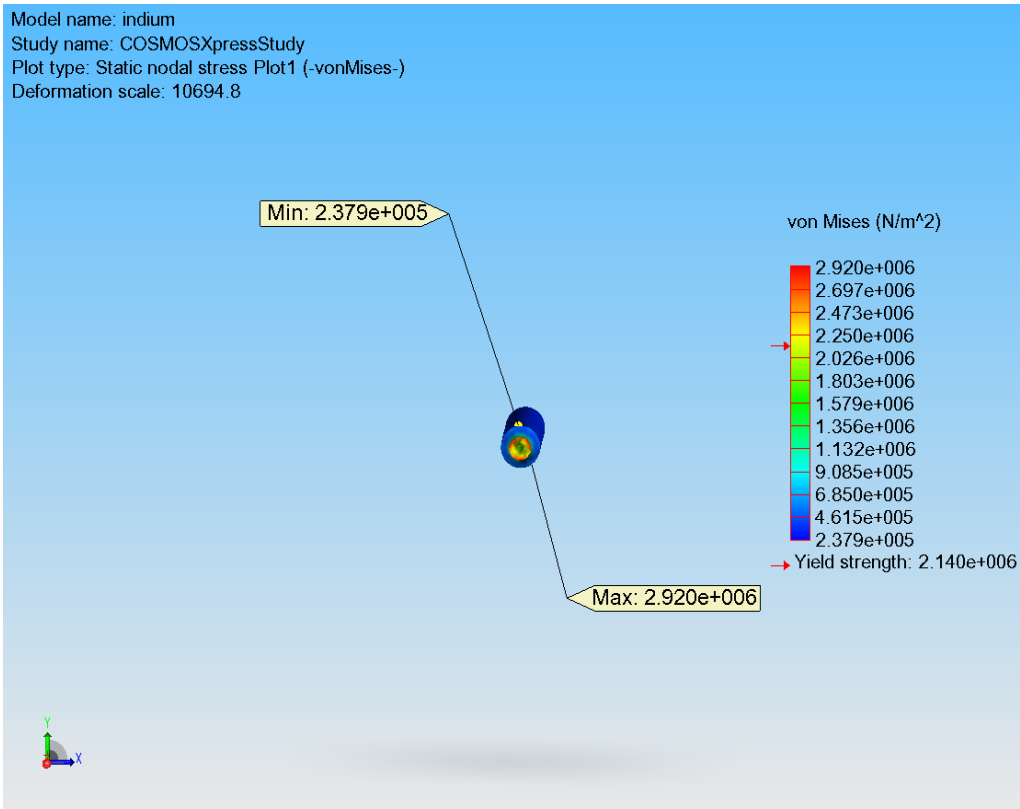


Figure 4.27 Simulation with 2N force showing deformation of Indium



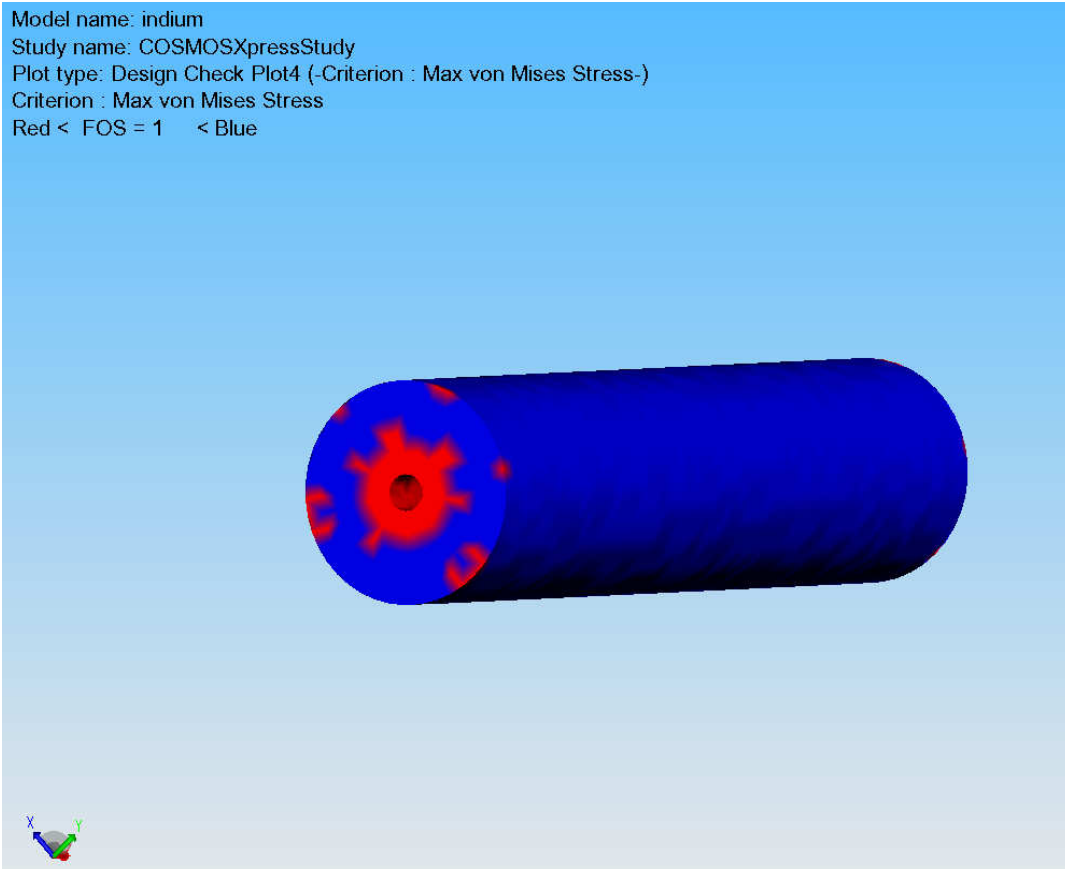


Figure 4.28 Maximum stress induced on the Indium

### 4.5.3 Results

Using the above test setup several fiber pull test were carried out the results are presented in the following the graph. Assuming that the displacement to be same for all the tests.

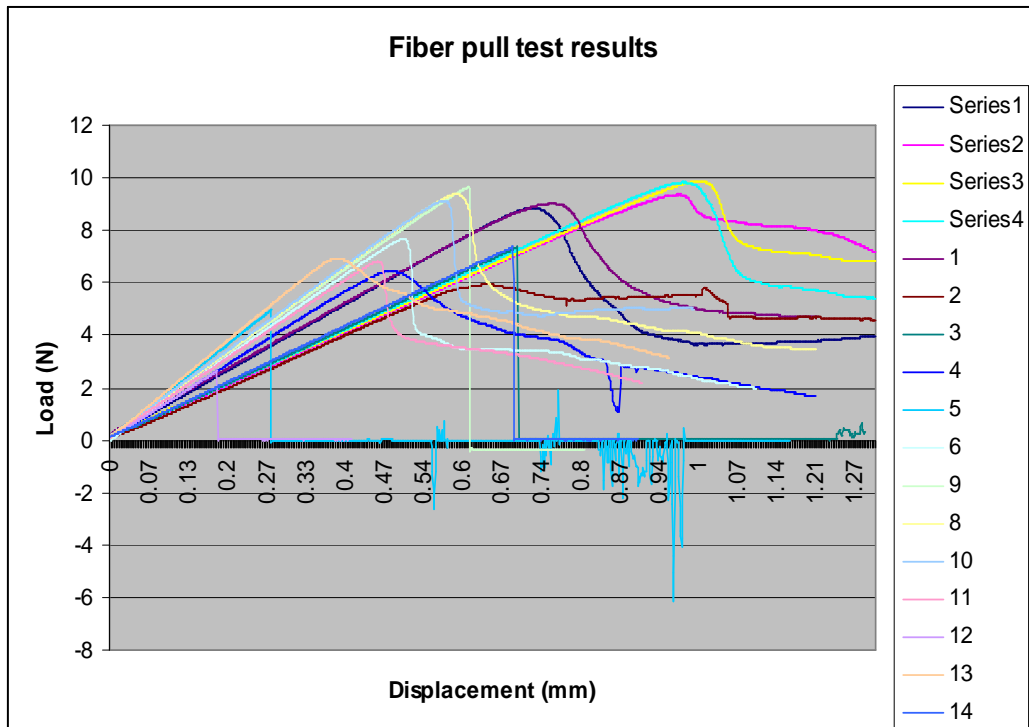


Figure 4.29 Load vs. displacement plot for last 18 fibers attach

All the tests show that the indium deformed in the almost similar manner. Majority of the joints failed between 8-10N forces. Some failed between 6 -8N force. Few fibers broke before the joint failed. Reasons for earlier failure could be mishandling of the fiber or improper mounting during the test.

Comparing the FEM results to the experimental results shows that the indium after reflow increases its strength compared to pure indium. This happens because after reflow the Gold-Indium intermetallics are formed. Which may be harder than the pure indium thus increasing the strength of the solder joint.

## **CHAPTER 5**

### **CONCLUSION & FUTURE WORK**

There is plenty of enthusiastic and exciting research going on in the field of MEMS to be used for various applications. The fabrication techniques are matured enough to make chips for every possible application but for MEMS to popularize and get into every possible application it's important that the MEMS packaging solutions and technology should be matured. Each MEMS device interacts in a unique manner with its environment which becomes a hurdle to develop a common and standard package for all the MEMS devices. As there is no standard process and specialty packaging tools it becomes difficult to commercially implement new MEMS devices. One of the possible solutions to this could be developing standard interconnect design that would give a tool which can be implemented in the Microsystems design that will facilitate the packaging process.

#### **Conclusion**

This thesis addresses the need to attach a MEMS chip to a metallized substrate and also an optical fiber interconnects between the chip and the external environment with attachment of the fiber to the carrier. All these soldering attachments were to be done with fluxless soldering with different controlled parameters. The experimental results showed that the cleaning of all the parts involved in soldering, affected the

attachments. So the cleaning procedures were set for all the soldering experiments. For indium based soldering reducing gas (Nitrogen) environment was used to avoid oxidation of solder during the soldering process. With the cleaning procedures and inert environment the die attach and fiber attach were achieved with fluxless soldering.

As the fluxless soldering was established there was a need to assess the reliability of the process developed. Different reliability tests were used to do so. Die shear test to evaluate the bond strength between the metallized carrier and the metallized MEMS chip.

The results showed that the bond survived required strength. Similarly for the fiber attached with fluxless soldering it is necessary to evaluate the bonding strength with a fiber pull test. Results showed that the bond formed had sufficient strength but after the fiber is attached the fiber would have handling issues.

### **Future work**

This work can be continued with testing of these solder bonding with further reliability destructive test like Vibration test, shock or impact test and thermal cycling test and fine leak test. Thermal cycling especially for indium based soldering as indium is soft material and has lower melting point. This may deform the indium with temperature change thus displacing the fiber in the hole.

Further and alternative approach for packaging can be adopted by achieving a hermetic wafer level chip to chip between the MEMS chip and a top chip over it. Top

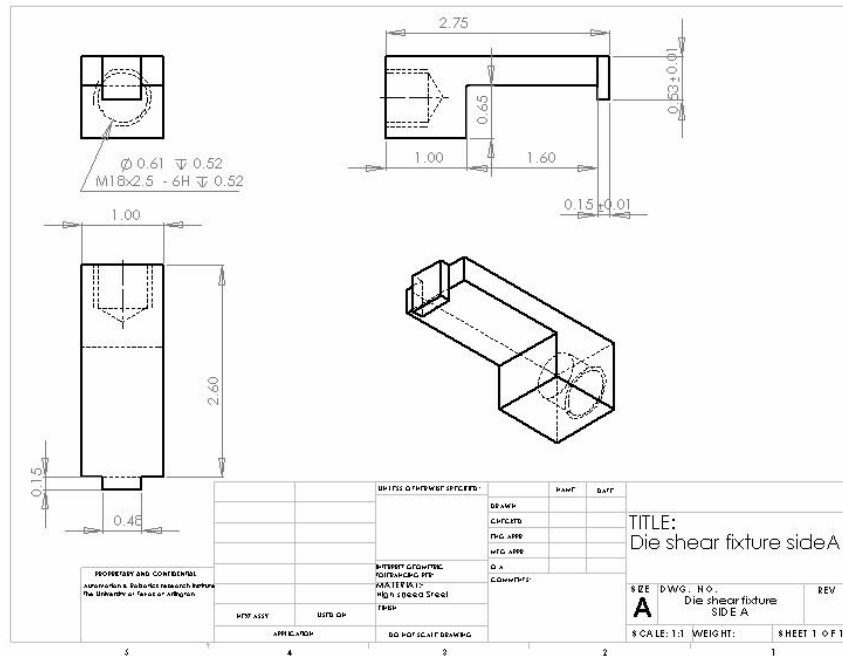
chip can be made out of silicon or glass. If the hermetic bond is achieved for the same, it may make the further packaging easier.

**APPENDIX A**  
**DRAWINGS FOR THE FIXTURE PARTS**









3) Shearing finger of the fixture for die shear



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