VISCOPLASTIC FINITE-ELEMENT SIMULATION TO PREDICT THE SOLDER JOINT FATIGUE LIFE OF DIFFERENT FLASH MEMORY DIE STACKING ARCHITECTURES

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ABSTRACT

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This thesis focuses on the viscoplastic finite-element simulation to predict the solder joint fatigue life of different die stacking architectures for flash memory products. Four different stacked package architectures were evaluated as follows: pyramid, rotated, and spacer stacking, while interconnection (solder joint) was held constant. Number of dies for all four stacking configurations were varied from three, five and seven. To keep the package height constant, the die and die attach thickness were varied and the resulting effects on the stresses were investigated. A quarter and half symmetry model of stacked flash package are generated using ANSYS APDL script. The life cycle

of the resulting packages were simulated under accelerated temperature cycling conditions (-40C to +125C, 15min ramps/15min dwells).

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

Figure

LIST OF TABLES

CHAPTER 1

INTRODUCTION

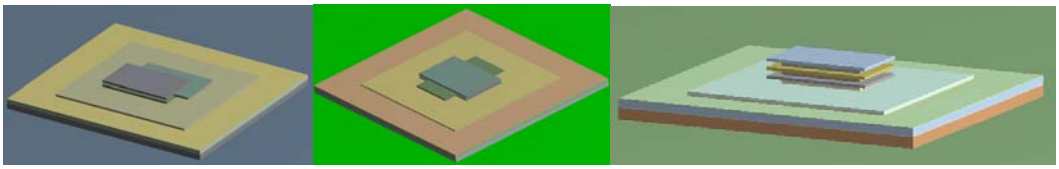
1.1 3D PACKAGE

Most future electronics applications will require increased reliability and performance as well as lower cost. In order to meet this general demand, new three-dimensional (3D)packaging technologies are now emerging where multiple ICs are stacked on a single substrate. The advantages of 3D packaging are an increase in the silicon packing efficiency and, through a reduction in the parasitic impedances, an increase in the bandwidth, reduction of signal time delay and reduction of system power consumption, allowing an increase in the system speed and clock rate.

1.1.1 Types of 3D package

The primary formats for stacked die packaging are 2-,3-,and 4-wire bonded stacks, although stacks of 5,6 and more are in development for low volume production. Stacked dies are typically configured in a pyramid or same size dies with spacers. Currently, dies as thin as 100µm are in production, with 50µm thick die in development. The dies are typically mounted to a substrate, which is bumped to create either a chip scale package (CSP) or ball grid array (BGA) as the final package.

There are various ways of die stacking which includes pyramid, same-size dies with spacer die, rotational and staggered stack.

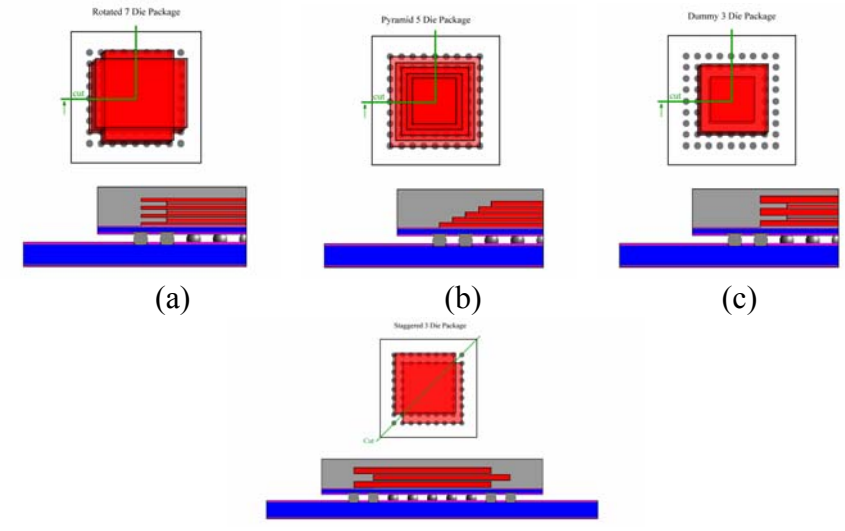


(a) (b) (c)

Figure 1.1 Die stacking configurations (a) Staggered Stack; (b) Rotated Stack; (c) Spacer-Die Stack

For the thermal analysis study, 4-Die stack package with four different die configurations were considered. The three stack configurations considered are: staggered, rotated and stacked die with die spacer in between. Figure 1.1 (a), (b), (c), and (d) show the four different die stacking configurations for thermal analysis.

Figures 1.2 (a), (b), (c) and (d) are showing the basic structure of four different die stack architecture (stack, pyramid and rotated) of the package for structural analysis.



(a) (b) (c)

(d)

Figure 1.2 Basic structure of (a) Rotate 3 Dies; (b) Pyramid 3 Dies; (c) Spacer 3 Dies;(d) Stagger 3 Dies

The original stacked die configuration placed a smaller die on the top of the larger die to create a "pyramid stack". To improve the assembly yield, it is recommended that the bottom die be at least 0.5 mm larger than the top die to ensure that the combination of the die attach placement error and die attach epoxy bleed-out do not impact wire bond ball and loop formation on the bottom die. The two dies can be wire bonded in a single pass process to achieve optimum productivity.

The second stacked die package configuration is the same-size die package. In this package an interposer or spacer die, typically made of silicon to match the coefficient of thermal expansion of the die, is placed on top of the bottom die to provide clearance for the wire bond loops that were made to the bottom die. The thickness of the interposer combined with the bond line thickness provides the clearance for the loops that have been bonded on the bottom die. As a guideline, the combined interposer and bond line thickness should be at least 50μm greater than the maximum specified loop height of the wire bonds on the bottom die.

1.1.2 How many could dies be stacked?

From a technical point of view, just how many dies can be stacked depends on the thickness of the final package and the thickness of each layer within the package. These include the substrate, die, spacers (if required), and BGA ball diameter. Substrate thickness is in turn influenced by the number of chip I/Os, which determines the number of substrate layers necessary. BGA ball diameter follows BGA ball pitch. In the past, 1.4 mm was the standard for stacked-chip packages in these applications. As Figure 1.3 shows, now demand is shifting to 1.2- and 1.0-mm high packages, and even

0.8 mm is a possibility. It is currently possible to build three- and four-die stacks in 1.4-mm packages.

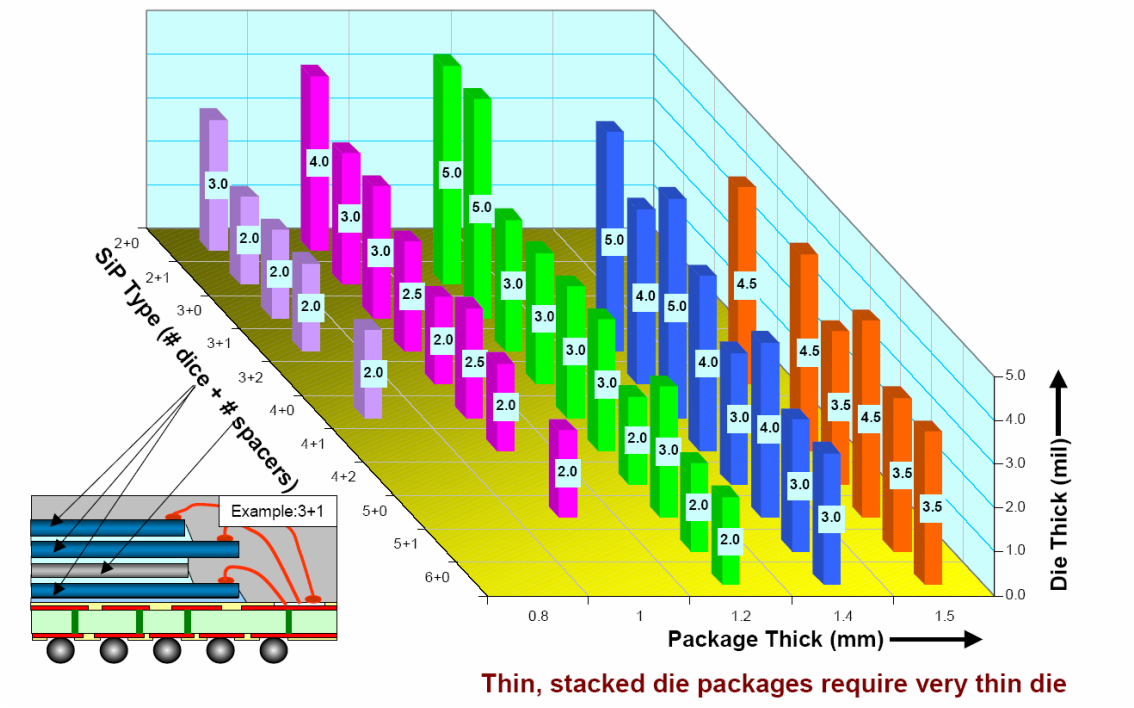


Figure 1.3 Die Thickness Trends [ChipPac Inc.]

1.2 Reliability

The integrity of solder joints is a major reliability concern in modern microelectronic packages. Temperature fluctuations caused by either power transients or environmental changes, along with the resulting thermal expansion mismatch between the various package materials, results in time and temperature dependent creep deformation of solder. This deformation accumulates with repeated cycling and ultimately causes solder joint cracking and interconnect failure. To minimize

development costs and maximize reliability performance, advanced analysis is a necessity during the design and development phase of a microelectronic package. This requires the utilization of a life prediction methodology that is based on the damage mechanisms experienced in a field operation environment.

The solder structures accommodate the bulk of the plastic strain that is generated during accelerated temperature cycling due to the thermal expansion mismatch between the various materials that encompass the stacked die package. Since plastic strain is a dominant parameter that influences low-cycle fatigue, it was used as a basis for evaluation of solder joint structural integrity. The paper discusses the analysis methodologies as implemented in finite element simulation software tool and the corresponding results for the solder joint fatigue life. Simulated accelerated temperature cycling is performed to obtain the plastic work due to thermal expansion mismatch between the various materials. Accumulated plastic strains were incorporated to predict the fatigue life. The model incorporates time dependent and time independent plasticity (i.e. creep) for the solder materials. Solder joint fatigue life are calculated for four different die stacking configurations and compared for design of an optimum stacking architecture.

1.3 Finite Element Method and Solder fatigue life prediction model

Several finite element based analysis methodologies have been proposed which predict solder joint fatigue life. Of all these methodologies, Darveaux's seems to be the most popular due to the ease in its implementation. Darveaux's methodology links laboratory measurements of low-cycle fatigue crack initiation and crack growth rates to

the inelastic work of the solder. It is a strain energy based approach, where the work term consists of time-dependent creep and time-independent plasticity. This inelastic behavior is captured in ANSYS using Anand's constitutive model. The modeling methodology utilizes finite element analysis to calculate the viscoplastic strain energy density accumulated per cycle during thermal or power cycling. The strain energy density is then utilized with crack growth data to calculate the number of cycles to initiate a crack, and the number of cycles for the crack to propagate across a solder joints diameter. Darveaux's methodology has been previously presented in the successful analyses of various electronic assemblies from multiple industry sources. In many of these sources, reliability test data that validates the accuracy of Darveaux's methodology is presented within +/-2X, which is considered state of the art for this type of complex physical analysis. This energy based model is used in this study to predict the solder joint life of the Stacked CSP.

CHAPTER 2

LITERATURE REVIEW

2.1 Reliability

Reliability is defined as the probability that a component or assembly will be operational for the expected period of use [Tummala 2001]. When microelectronic packages are subjected to actual field use, failures in the product are typically seen at the system level. However, the cause of the failure are always observed at the component level which is due to thermal, mechanical, electrical, or a combination of these failure modes and mechanisms. To assess the reliability and qualify a product within a reasonable amount of time in a well-controlled environment, accelerated tests can be performed. In these accelerated tests, they are performed to obtain reliability data in a much shorter period of time, and an acceleration factor is used to convert the time-to-failure under accelerated test conditions to the actual time-to-failure under normal usage conditions [Tummala 2001]. A commonly accepted thermal cycling profile for microelectronics is by JEDEC (JESD22-A104-B), test condition J and thermal soak 4, which thermal cycles the package between -45 C° and 125 C° with fifteen minute dwells [JEDEC 2000]

To supplement the empirical data obtained from performing accelerated tests, virtual reliability modeling can also be used for stress and strain analysis to aid the design engineer to determine the failure modes such as interfacial delamination, solder

joint fatigue, and die cracking. To assess the reliability of the system, numerical models can be developed to take into account the actual geometry details. To obtain a model that attempts to replicate the performance of the system, material modeling of each component is critical.

2.2 Constitutive Relations

In general, a change in temperature causes the mechanical properties and performance of materials to change. Some properties and performance, such as elastic modulus and strength decrease with increasing temperature. Others, such as ductility, increase with increasing temperature. Therefore, in the material modeling of the various materials in the package, constitutive relations that predict strain as a function of stress, temperature, and time should be taken into consideration.

Since solder is used to assemble the copper pad to the next-level interconnection, the material has the tendency to creep at room temperature. This is because the absolute temperature is greater than one half of the absolute melting temperature. The ratio between the absolute temperature and absolute melting temperature is defined as the homologous temperature in an absolute temperature scale. For instance, 63Sn/37Pb solder at room temperature ($20\,C^{\circ}$) has a homologous temperature of 0.64. Taking this into consideration, the material modeling of solder should include inelastic strains that constitute rate-independent plasticity along with rate-dependent deformation behavior either in an explicit creep equation or combine the inelastic strains into a unified viscoplastic model [Anand, 1985, McDowell 1994].

2.2.1 Time-dependent Plasticity

Time-dependent plasticity, otherwise known as creep, is a rate dependent nonlinearity that occurs in materials whose absolute temperature is greater than one half the absolute melting temperatures. Creep can be broken down into three stages which are Primary, Secondary and Tertiary as shown in Figure 2.1

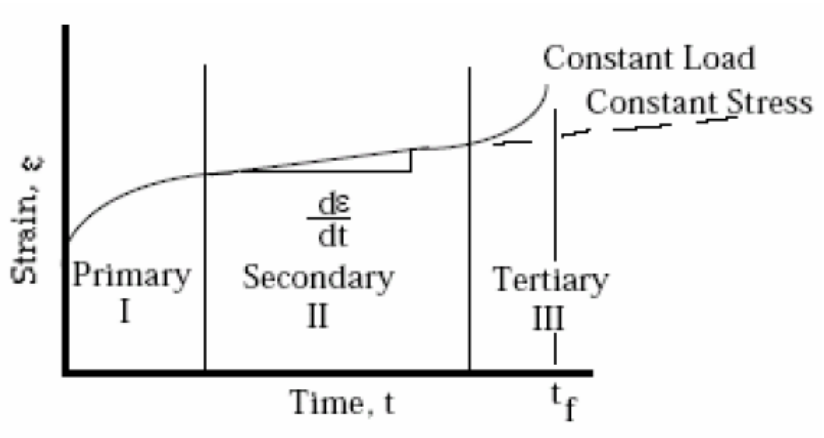


Figure 2.1 Strain time curve for a creep test

In the primary region, it is characterized by transient creep with decreasing strain rate due to creep resistance of the material to deformation. In the secondary region, the deformation due to creep is at a steady-state and competing mechanism of strain hardening and recovery may be present. In the tertiary region, the creep strain rate begins to increase and necking occurs under constant load.

The steady state creep stain rate for eutectic and near-eutectic solder alloys can be characterized by a Arrhenious-type rate model (also known as Norton creep law) which includes the effect of temperature in the model of Equation 2-2 such that:

$$\dot{\varepsilon}_c = A\sigma^n e^{-(Q/R_g T)} \tag{2-1}$$

where $\dot{\varepsilon}_c$ is the steady state creep strain rate, σ is the current stress, *A* and *n* are experimentally determined material constants, *Q* is the activation energy for creep, R_g is the universal gas constant, and *T* is the temperature of the solder in Kelvin.

At higher stresses the power law equation breaks down. Therefore, the strain rate is not dependent on the stress to the power, *n* [Darveaux 1992]. The power law breakdown region can be subsequently described by the Garafalo relation:

$$\dot{\gamma}_s = C_1 \frac{G}{T}\left[\sinh\left(\alpha \frac{\tau}{G}\right)\right]^n \bullet \exp\left(\frac{-Q}{kT}\right) \qquad (2\text{-}2)$$

where $\dot{\gamma}_s$ is the steady state shear strain rate, C_1,*n*, and α are experimentally determined material dependent constants, *Q* is the material activation energy for creep, τ is the shear stress, *G* is the shear modulus, *T* is the absolute temperature, and *k* is the Boltzmann's constant.

2.2.2 Unified Viscoplasticity Model (Anand's Model)

Viscoplasticity is defined as unifying plasticity and creep via a set of flow and evolutionary equations where a constraint equation is used to reserve volume in the plastic region[ANSYS 1994]. A viscoplastic model which can be incorporated into commercially available software packages is proposed by Anand. This model comprises of single scalar internal state variable "s", called the deformation resistance, to measure the isotropic resistance offered by the solder to the plastic flow. In this model, it assumes no explicit yield condition and no loading/unloading criterion used. Instead, it assumes that plastic flow occurs at all non-zero stress values. Therefore, Anand's model characterized the inelastic strains with an Arrhenius term for the temperature

dependency and the stress and strain rate dependency of the Garafalo form. The constitutive equation is the flow equation as prescribed in Equation 2-3

$$\dot{\varepsilon}_p = Ae^{(-Q/RT)}\left[\sinh\left(\xi\frac{\sigma}{s}\right)\right]^{1/m} \tag{2-3}$$

where $\dot{\varepsilon}_p$ is the inelastic strain rate, A is a pre-exponential factor, Q is the activation energy, R is the universal gas constant, T is the current absolute temperature, ξ is a multiplier of stress, σ is the current tensile stress, m is the strain rate sensitivity, and s is the internal state variable (deformation resistance) and the evolution equation is:

$$s^* = \hat{s}\left[\frac{\dot{\varepsilon}_p}{A}e^{(Q/RT)}\right]^n \tag{2-4}$$

where $\hat{s}$ is a coefficient for deformation resistance saturation value, and n is the strain rate sensitivity for s saturation.

Anand's model has been shown to provide reasonable results when compared to a combination of plasticity and creep model [Tunga et al, 2002]. To model the material behavior of solder, nine material constants are needed which are: $A, Q, \xi, m, h_0, \hat{s}, n, a,$ plus the initial value of the deformation resistance, s_0.

2.2.3 Fatigue Life Prediction Models

The following section outlines the fatigue-life prediction models used to evaluate the thermo-mechanical reliability of the compliant interconnect and solder material. Fatigue life models are used to determine the number of cycles that a package can endure before failing. There are two approaches: high cycle fatigue (HCF) and low

cycle fatigue (LCF). In HCF, it is based off of stress reversals which are in the elastic regime and have not exceeded the yield point. As for LCF, it is based on strain reversals where plastic deformation dominates.

In microelectronic packaging, *due to the multi-axial loading that is incurred during thermal excursions*, *the reliability of compliant interconnect technology is considered to fail under low cycle fatigue where failure is predominately due to plastic strains*. To understand the fatigue life of the components in the package, fatigue models have been constructed which fall into the following categories:

- Inelastic strain amplitude (Coffin-Manson-type)
- Stress based
- Strain-energy density-based(Darveaux's methodology)
- Creep strain based
- Damage-mechanics-based

In this work, fatigue life based on of strain-energy density (Darveaux's methodology) will be utilized for characterizing the fatigue life of the compliant interconnect and solder.

2.2.3.1 Strain-energy density based prediction models

Energy based fatigue life prediction model was used in this paper, as it is the most widely used model available for Pb-Sn solder. The combined probabilistic and optimization study deals with scalar parameters and can be incorporated in any failure model, especially for the case of lead free solder where the use of energy based model is still under consideration. ANSYS APDL script was used for incorporating energy based

fatigue life model to predict solders joint fatigue life. The element interface thickness utilized in all models discussed herein was 0.0254 mm (1mil).

The layer of elements having maximum plastic work density is included in the calculation of the weighted average plastic work density, W_{ave}

$$\Delta W_{ave} = \frac{\sum_{i=1}^{Element} \Delta W_i \times V_i}{\sum_{i=1}^{Elements} V_i} \tag{2-5}$$

where W_i designates the plastic work density in the i^{th} element and V_i is the volume of that element.

A thermal cycle to crack initiation "No" is given by:

$$N_o = K_1 \Delta W_{ave}^{K_2} \tag{2-6}$$

Crack propagation rate per thermal cycle "da/dN"

$$\frac{da}{dN} = K_3 \Delta W_{ave}^{K_4} \tag{2-7}$$

where W_{ave} is the element volumetric average of the stabilized change in plastic work within the controlled eutectic solder element thickness. K_1, K_2, K_3, and K_4 are crack growth constants, which depend on geometry, loading, and the finite element analysis method. Crack growth correlation constants K_1, K_2, K_3, and K_4 are respectively 56300 cycles/psi, 1.62, 3.34e-07, 1.04.

The characteristic solder joint fatigue life "α" (number of cycles to 63.2% probability of failure) can be calculated by summing the cycles to crack initiation with

the number of cycles it takes for the crack to propagate across the entire solder joint pad diameter “a”. α is given by:

$$\alpha = N_o + \frac{a}{\frac{da}{dN}} \tag{2-8}$$

Using this equation to assess the 63.2% failure probability lifetime is based on the assumption that the solder joint fatigue life follows an exponential distribution.

2.3 Summary

Package models are created using Ansys APDL. Work energy by thermal cycles, are utilized for reliability. In order to evaluate solder ball life of package, Darveaux's prediction models have been chosen, linking experimental data and based strain energy.

CHAPTER 3

OBJECTIVES AND APPROACH

3.1 Gaps in previous work

Previous thermal analysis study on various die stacking architectures, which are commonly, employed in semiconductor flash products shows that thermal issues are not dominant for stacked die configuration (at least in current power levels). This leads to this current study to investigate the effect of thermo-mechanical stresses. As there are existence of multiple die and other material with different CTEs, thermo-mechanical loading and its effect on reliability needs to be studied for optimum die configuration.

3.2 Objectives

This study focuses on viscoplastic finite-element simulation to predict the solder joint fatigue life of different die stacking architectures for flash memory applications. Four different stacked package architectures were evaluated as follows: pyramid stack, rotated stack, and stacking with spacers, staggered die stacking; while interconnection architecture (solder joint) was held constant. Die stacking number for four different stacking configurations were varied from three, five and seven keeping the package height constant.

3.3 Approach

A quarter symmetry and half symmetry model of stacked flash package are generated using ANSYS as a finite element solver. Models are simulated under

accelerated temperature cycling conditions (-40C to +125^{o}C, 15min ramps/15min dwells). Fatigue life and plastic strain accumulation results are presented in the paper. Results show that significant differences in plastic strain accumulation and fatigue life differences for different geometrical die configuration. Effects of different package reliability package reliability parameters like die size, die and die attach thickness are were varied and the effects of stresses due to that were discussed in this work.

CHAPTER 4

FATIGUE MODEL DESCRIPTION

4.1 Package and Test PCB Description

9x9mm^2 (depopulated 5x5 in the middle) plastic CSP module on a 1-layer PWB is adopted in the model of study. SMD pads are used for the package and NSMD pads are used on the PWB. Four different stacked package architectures evaluated were pyramid stack, rotated stack, stagger stack, and stacking with spacers. 3-die, 5-die and 7-die configurations were chosen for the four different architectures. The dimensions are given in Table 4.1 below:

Table 4.1 Package Dimension (every package)

Parameter	**Dimension(mm)**
PCB	13.5 x 13.5 x 0.754
Substrate	9 x 9 x 0.252
mold compound	1.2
Solder pitch	0.8
Solder ball diameter	0.33

The dimensions of the other parameters for spacer, rotated, staggered, and pyramid die configurations are given in table 4.2, 4.3, 4.4, and 4.5.

Table 4.2 Dimensions for Spacer Die configuration

Parameter (mm)	3-Die	5-Die	7-Die
Die-Size	4.8x4.8		
Spacer Size	3.2x3.2		
Die Thickness	0.2	0.12	0.0857
Spacer Thickness	0.08	0.04	0.0107
Paste thickness	0.0201	0.0150	0.0120

Table 4.3 Dimensions for Rotated Die configuration

Parameter (mm)	**3-Die**	**5-Die**	**7-Die**
Die-Size	6.4x4.8	6.4x4.8	6.4x4.8
Die Thickness	0.25	0.15	0.107
Paste Thickness	0.025	0.016	0.0114

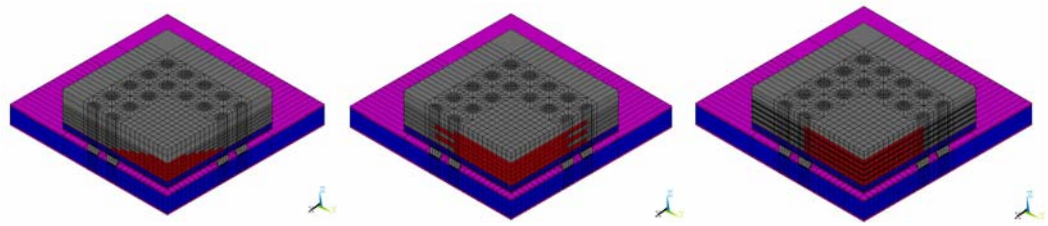
Table 4.4 Dimensions for Staggered Die configuration

Parameter (mm)	**3-Die**	**5-Die**	**7-Die**
Die-Size	5.6x5.6	5.6x5.6	5.6x5.6
Die Thickness	0.2	0.12	0.084
Paste Thickness	0.02	0.015	0.012

Table 4.5 Dimensions for Pyramid Die configuration

Parameter (mm)	**3-Die**		**5-Die**		**7-Die**	
Die-Size	**Bottom**	**Top**	**Bottom**	**Top**	**Bottom**	**Top**
	6.4x4.8	**3.2x1.6**	**6.4x4.8**	**3.2x1.6**	**6.4x5.6**	**1.6x 0.8**
Die Thickness	0.2		0.1230		0.095	
Paste Thickness	0.025		0.154		0.012	

Studies have been done by changing the die cross-section to square and rectangular configuration with same package dimension for spacer and pyramid die stacking.



(a) (b) (c)

Figure 4.1 Finite Element Quarter Models for three different die configuration: (a) Stacked 5 Die; (b) Pyramid 5 Die; (c) Rotated 5 Die

Figure 4.1 shows the quarter symmetry finite element model for three different die stacking configuration: die stacking with spacers; pyramid stacking and rotated stacking.

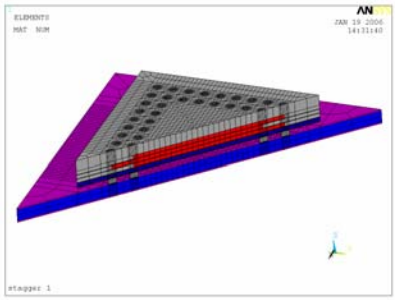


Figure 4.2 Finite Element Half Model for staggered 3 Die configuration

Figure 4.2 shows the diagonal symmetry finite element model for staggered die configuration.

4.2 Material Properties

Accuracy of the FE model depends on the accuracy of the materials properties and proper meshing. Linear and non-linear, elastic and plastic, time and temperature independent and dependent material properties were incorporated in the finite element model as displayed in table 4.5. Thermo-mechanical properties used are Young's Modulus, co-efficient of thermal expansion (CTE) and Poisson's ratio.

The solder material was modeled with modified Anand's rate-dependent plasticity model. Anand's constitutive model incorporates viscoplasticity, a time-dependent plasticity phenomenon, where the development of plastic strains is dependent on the rate of loading. Darveaux has presented solder constitutive relations based on Anand's model for rate dependent plasticity. Linear orthotropic material properties were used for the printed wire board and the BT (Bismaleimide Triazine) laminate substrate.

Linear and non-linear, elastic and plastic, time and temperature independent and dependent material properties were incorporated in the FE models. Solder ball materials are meshed with Visco107 and all other package materials are meshed using the SOLID185 elements. To get stable results mesh sensitivity was done on the model. Since the simulation time highly dependent on the number of elements and nodes mesh sensitivity was done to compromise between the solving time and stable data. By changing the model nodes, the plastic work accumulation and the solder joint fatigue life changes within the range of 5%.

Table 4.6 Material properties for various package materials used in the finite element analysis

Component (Material)	**Elastic Moduli(Mpa)**	**Shear Moduli (Mpa)**	**CTE (1/K)**	**Poisson Ratio (No Units)**
Ball (63Sn37Pb)	75482-152T	-	$24.5e^{-6}$	0.35
Chip (Silicon)	162716	-	$-5.88x10^{-6}+6.2610-8T$ $-1.610-10xT^{2}+1.510-13T^{3}$	0.28
Conductor (Copper)	128932	-	$13.8x10^{-6}+9.44x10^{-9}T$	0.34
Epoxy Film (Proprietary)	2230-5.27T	-	$41x10^{-6}$<Tg,288K $110x10^{-6}$>/= Tg,288K	0.35
Mold Cap (Mold)	15513	-	$15.0x10^{-6}$	0.25
PCB Core (FR4)	7294-37T(XY 12204-16T(Z)	12600-16.7T(XY) 500-7.3T(YZ & XZ)	$16.0x10^{-6}$(XY) $84.0x10^{-6}$(Z)	0.39(XZ & YZ) 0.11(XY)
PCB Mask (Dry Film)	4137	-	$30.0x10^{-6}$	0.40
Substrate Core (BT)	24132	-	$13.0X10^{-6}$(XY) $35.0X10^{-6}$	0.30
Substrate Mask (Dry Film)	4137	-	$30.0X10^{-6}$	0.4 0

4.3 Solution and Postprocessing

For evaluating the component reliability, a 60 minute thermal cycle, ranging from -40 to 125^{o}C and consisting of 15-minute ramps and 15-minute dwell was used. Figure 4.3 below shows the thermal cycles used for the simulations. Nonlinear, diagonal, quarter, global models were used with ANSYS finite element solver.

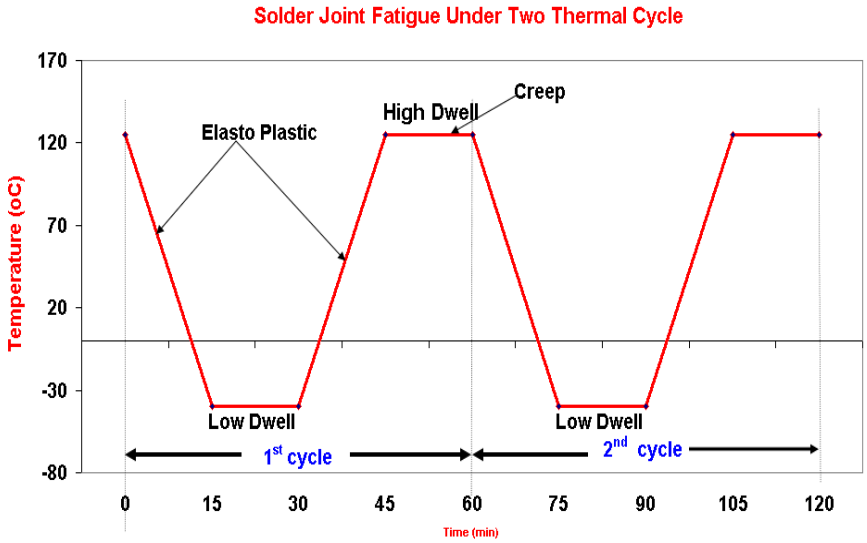


Figure 4.3 Thermal Cycle Profile used for Analysis

CHAPTER 5

THERMAL & MECHANICAL RESULTS

A total of twelve package quarter models were created to evaluate corresponding solder joint fatigue effects using four different die configurations for four different types of package geometry. Die stack geometries for different die configuration also varied to see the parametric effect on plastic deformation of the solder joint under accelerated thermal cyclic condition.

5.1 Thermal & Mechanical Result

Accelerated thermal cycling was performed on the modeled CSP using finite element analysis. Temperature variation was from -40 to 125^{o}C with 15 minutes ramps and 15 minutes dwells (one hour cycle). ANSYS APDL code was used to obtain the stress strain relationship and post processing information. Quarter symmetry model is used for the FE simulation. To stabilize the plastic work the number of cycles were varied from two to five cycles. Computer used for running the simulations was a Intel duel core 3GHz processor with 4GB DDR2 RAM. Simulation time varied from two to four hours. After successive thermal load cycles, maximum plastic work/volume information were documented along with the stress strain information for solder ball. Figure 6 below shows the accumulated plastic work in the solder joints from the finite element analysis.

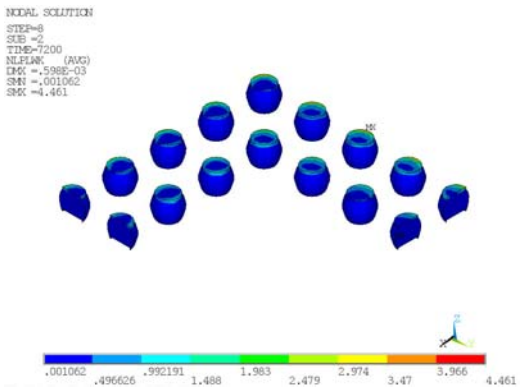


Figure 5.1 Accumulated plastic work in the solder

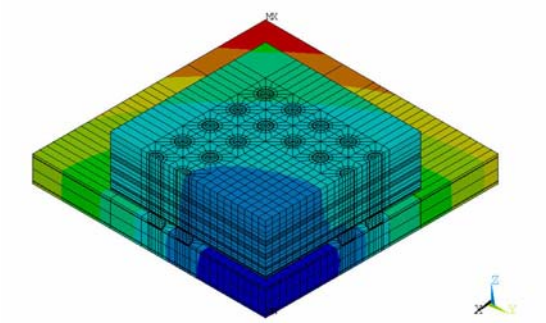


Figure 5.2 Vertical displacement due to thermal cycling

Figure 5.2 shows the vertical displacement due to thermal cycling. Vertical displacement varies with different die stacking.

Table 5.1, 5.2 and 5.3 indicate the detailed simulation results. Fatigue life calculated for substrate and PWB solder joint and also the plastic work accumulated in the solder joint. Number of nodes/elements and simulation time also added to these tables below.

Table 5.1 Result summary for the stack package with spacer die

Data Description	Spacer–Die configuration 4.80x 4.80mm^2			Spacer–Die configuration 6.40 x 4.80 mm^2		
	3-Die	5-Die	7-Die	3-Die	5-Die	7-Die
Ball/Substrate Solder Joint						
Delta Plastic Work/Cycle (MPa)	19.39	23.32	33.36	34.02	38.66	60.64
Characteristic Life (cycles)	1460	1199	821	804	703	440
Ball/PCB Solder Joint						
Delta Plastic Work/Cycle (MPa)	8.37	9.16	12.29	12.27	13.01	19.85
Characteristic Life (cycles)	3650	3305	2392	2396	2247	1424
Model Size and Run Time Info.						
Total Model Nodes	40723	55075	69427	40723	55075	69427
Total Model Elements	35928	49668	63408	35928	49668	63408
CPU Run Time (Hrs)	2.49	1.71	2.65	2.54	1.79	2.77

Table 5.2 Result summary for the stack package with pyramid die configuration

Data Description	Pyramid (Square-Die configuration)			Pyramid (Rectangular-Die configuration)		
	3-Die	5-Die	7-Die	3-Die	5-Die	7-Die
Ball/Substrate Solder Joint						
Delta Plastic Work/Cycle (MPa)	33.84	31.12	47.60	56.24	55.47	65.47
Characteristic Life (cycles)	809	883	566	476	483	407
Ball/PCB Solder Joint						
Delta Plastic Work/Cycle (MPa)	11.53	11.43	12.93	19.36	18.40	17.94
Characteristic Life (cycles)	2563	2589	2262	1463	1544	1587
Model Size and Run Time Info.						
Total Model Nodes	33547	40723	47899	33547	40723	47899
Total Model Elements	29058	35928	42798	29058	35928	42798
CPU Run Time (Hrs)	0.60	1.01	1.38	0.60	0.96	1.38

Table 5.3 Result summary for the stack package with rotational die configuration

Data Description	Rotated–Die configuration		
	3-Die	5-Die	7-Die
Ball/Substrate Solder Joint			
Delta Plastic Work/Cycle (MPa)	33.84	45.33	47.93
Characteristic Life (cycles)	809.14	595.89	562.28
Ball/PCB Solder Joint			
Delta Plastic Work/Cycle (MPa)	11.53	15.03	15.52
Characteristic Life (cycles)	2563.71	1921.50	1855.70
Model Size and Run Time Info.			
Total Model Nodes	33547	40723	47899
Total Model Elements	29058	35928	42798
CPU Run Time (Hrs)	0.60	1.00	1.01

Table 5.4 Result summary for the stack package with staggered die configuration

Data Description	Staggered–Die configuration		
	3-Die	5-Die	7-Die
Ball/Substrate Solder Joint			
Delta Plastic Work/Cycle (MPa)	88.15	85.95	83.82
Characteristic Life (cycles)	299.83	307.70	315.73
Ball/PCB Solder Joint			
Delta Plastic Work/Cycle (MPa)	38.93	41.26	41.53
Characteristic Life (cycles)	698.41	657.29	652.87
Model Size and Run Time Info.			
Total Model Nodes	59754	69614	79474
Total Model Elements	51560	61128	70696
CPU Run Time (Hrs)	5.71	6.23	6.64

Table 5.4 shows not much difference in characteristic life for staggered die configuration.

Certainly it is seen from the table 5.1, through 5.4 that plastic work increases with die counts, which indicates risk for a solder joint reliability.

Further studies have been done for the spacer-die architecture by changing the die size and die thickness. Table 5.5 shows simulation result for three die stack with spacer die by changing the die size (real estate).

Table 5.5 Result summary for different size die stack with spacer die

Data Description	Spacer–Die configuration				
	4.8x 4.0 mm^2	5.6 x 4.8 mm^2	5.6 x 5.6 mm^2	6.4 x 4.8 mm^2	6.4 x 6.4 mm^2
	3-Die	3-Die	3-Die	3-Die	3-Die
Ball/Substrate Solder Joint					
Delta Plastic Work/Cycle (MPa)	19.39	30.30	33.98	34.02	50.59
Characteristic Life (cycles)	1460	909	805	804	532
Ball/PCB Solder Joint					
Delta Plastic Work/Cycle (MPa)	8.37	9.12	10.01	12.27	17.81
Characteristic Life (cycles)	3650	3319	2995	2396	1600

Larger die area with same die thickness increases the plastic work for same die stacking with spacer. Table 5.6 shows simulation result for three stacked spacer die by changing the die thickness of the square size die.

Table 5.6 Result summary for different die thickness die for die stack with spacer die.

Data Description	Spacer–Die configuration 4.80x 4.80mm^2		
	3-Die	3-Die	3-Die

Table 5.6 - continued

Die thickness	0.2	0.15	0.10
Spacer Thickness	0.08	0.05	0.05
Paste thickness	0.025	0.025	0.025
Total mold thickness	1.2	1.2	1.2
Ball/Substrate Solder Joint			
Delta Plastic Work/Cycle (MPa)	19.39	27.99	31.84
Characteristic Life (cycles)	1460	988	863
Ball/PCB Solder Joint			
Delta Plastic Work/Cycle (MPa)	8.37	11.00	10.53
Characteristic Life (cycles)	3650	2699	2833

Plastic strain accumulation and the worst solder joint location vary with various die stacking configurations. Die stresses in various die stacking configuration also varies and the worst case found with the pyramid 7die stacking. This means that die stacking in stack packages surely has an effect on solder joint reliability and on ball architecture.

Die size (cross-section) has an impact on solder joint plastic work and the fatigue life. Increasing the die size reduces the joint life of the package with same mold height and the cross-section. Die thinning also impacts the fatigue life and reduced it with thinner die.

5.2 Analysis

Following figures will be showing us why thinner die reduce fatigue life.

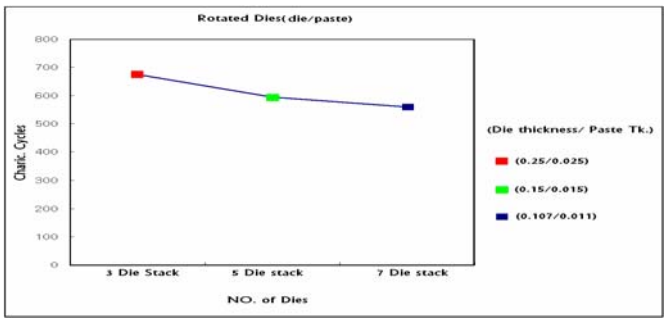


Figure 5.3 Characteristic life for the number of die in Rotated Package in limit package size

Figure 5.3 shows that the die thickness should be reduced for putting in limit package. What if, however, are die thicknesses remained?

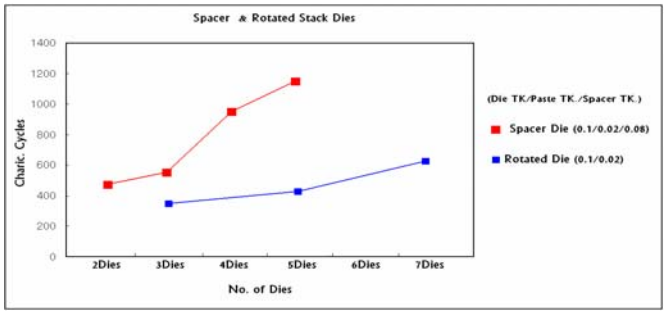


Figure 5.4 Characteristic life for the number of die in Rotated package using the same die thickness

Figure 5.4 shows higher rate of die material in package increase cycles of solder balls. Here is the reason spacer –die are relatively higher reliability than that of pyramid and rotated one. Then, next will be show how could Table 5.7 be explained, which used to same total volume of die.

Table 5.7 Result summary for each die thickness with spacer die

Data Description (mm)	**Spacer–Die configuration 4.80x 4.80mm^2**	
	Spacer Thickness	0.08
	Paste thickness	0.02
	Total mold thickness	1.2

Bottom die Thickness	Middle die Thickness	Top die Thickness	Characteristic life (cycles)
0.1	0.25	0.25	1560
0.15	0.225	0.225	1475
0.2	0.2	0.2	1460
0.225	0.225	0.15	1339
0.25	0.25	0.1	1277

Table 5.7 indicates that each location of die has different efficiency to fatigue life in the solder balls. In this case, top die thickness has priority over the others.

Table 5.8 Result summary for each die thickness with Rotated-die

Data Description (mm)	**Rotated–Die configuration 6.40 x 4.80 mm^2**	
	Paste thickness	0.025
	Total mold thickness	1.2

Bottom die Thickness	Middle die Thickness	Top die Thickness	Characteristic cycles)
0.1	0.325	0.325	549
0.15	0.3	0.3	598
0.25	0.25	0.25	676
0.3	0.3	0.15	700
0.325	0.325	0.1	688

In Rotated-Die configuration, Table 5.8, the effective location was changed downward. Both cases could be compatible with that 7die stacking has worst reliability, which has thinner dies in some location (z-direction). Besides, the different location of both could be explainable by the different rate of die material; spacer-die having more rate of the die materials because of spacer.

5.3 Conclusion

A finite element analysis based study for estimating accelerated temperature cycling solder joint characteristic fatigue life has been applied to predict the reliability performance of different stack die architecture on chip scale ball grid array package. The method uses the ANSYS finite element analysis tool along with Anand's viscoplastic constitutive law. Darveaux's crack growth rate model was applied to calculate solder joint characteristic life using simulated viscoplastic strain energy density results at the package substrate and printed circuit board solder joints. Twelve die configurations were evaluated. Also further study was done by changing the die size and die thickness of the spacer and pyramid-die package.

For enhanced solder joint performance, it is recommended to have smaller die size in stacked-die packages. While considering stacked die architecture, it was found that spacer-die architecture had better solder joint reliability performance than the other four die architectures. As solder joint dimensions become smaller and smaller in the future, and interface reactions and properties become more complex, more effort need be put on understanding the effect of multiple dies and its optimum architectural distribution considering the wire-bonding or other types of material and interconnection

issues. Experimental study needs to be combined with the computational simulation to optimize thermal and mechanical reliability of the future high density stack packages for flash memory application.

CHAPTER 6

REDUCING SOLVING TIME AND OVERCOMING CONVERGENCE PROBLEMS IN NONLINEAR ANALYSIS

6.1 Typical Nonlinear problems

Nonlinear behavior could be grouped into these principal categories:

- Geometric nonlinearity
- Material nonlinearity
- Changing status (including contact)
- Combination of (1) to (3)

6.1.1 Geometric nonlinearity

If a structure experiences large deformations, its changing geometric configuration can cause the structure to respond nonlinearly. An example would be the fishing rod shown in Figure 6.1: "A Fishing Rod Demonstrates Geometric Nonlinearity". Geometric nonlinearity is characterized by "large" displacements and/or rotations.

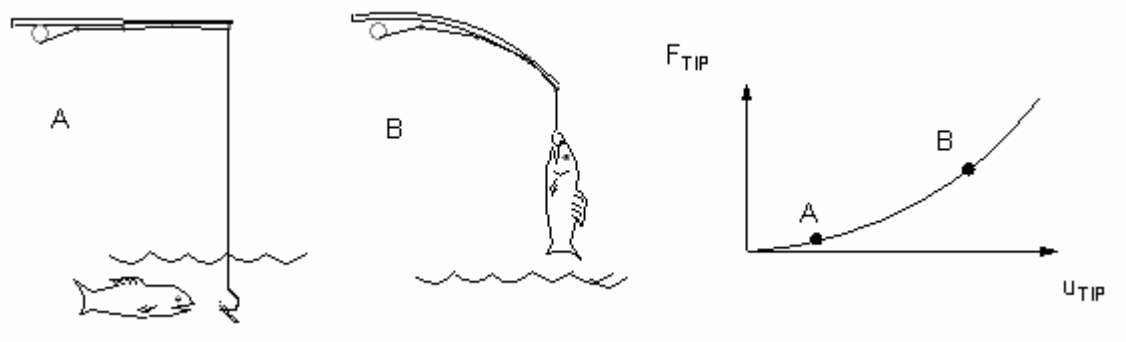


Figure 6.1 A Fishing Rod Demonstrates Geometric Nonlinearity

Small deflection and small strain analyses assume that displacements are small enough that the resulting stiffness changes are insignificant. In contrast, large strain analyses account for the stiffness changes that result from changes in an element's shape and orientation. In this thesis, large strain effects are activated by issuing NLGEOM command

6.1.2 Material nonlinearity

If a material displays nonlinear or rate-dependent stress-strain behavior, then the models must define the nonlinear material property relationships in terms of below data table.

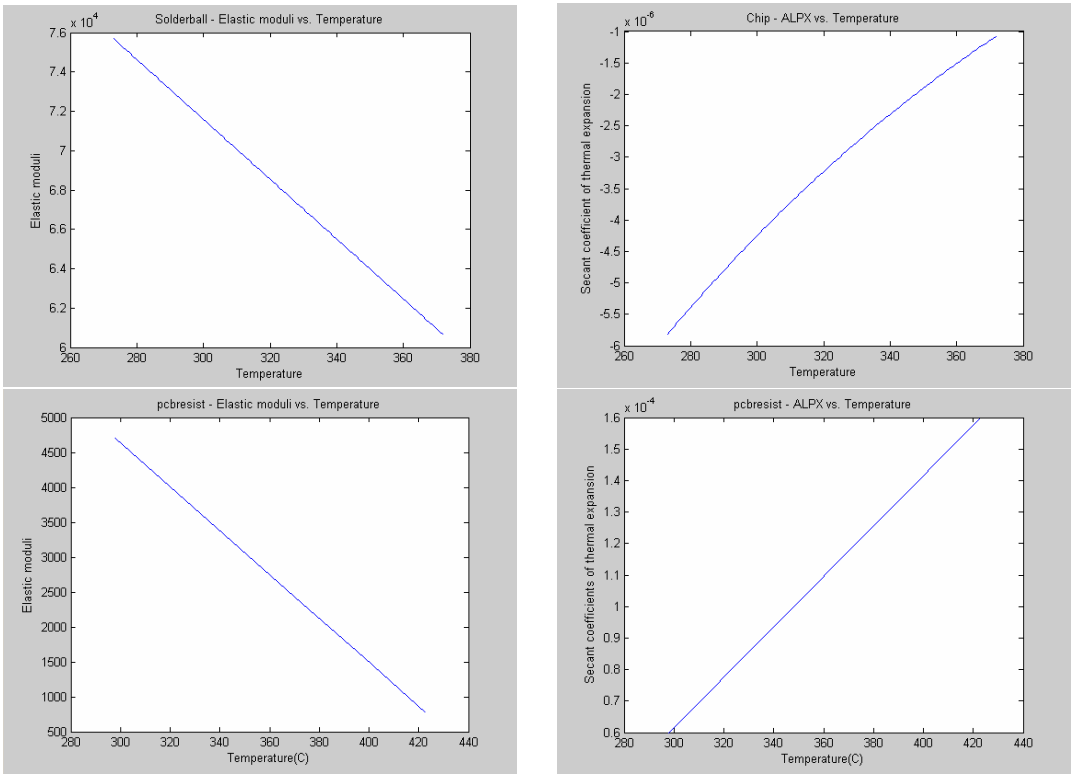


Figure 6.2 Applied Nonlinear material properties; Solderballs, Chip, PcbResist

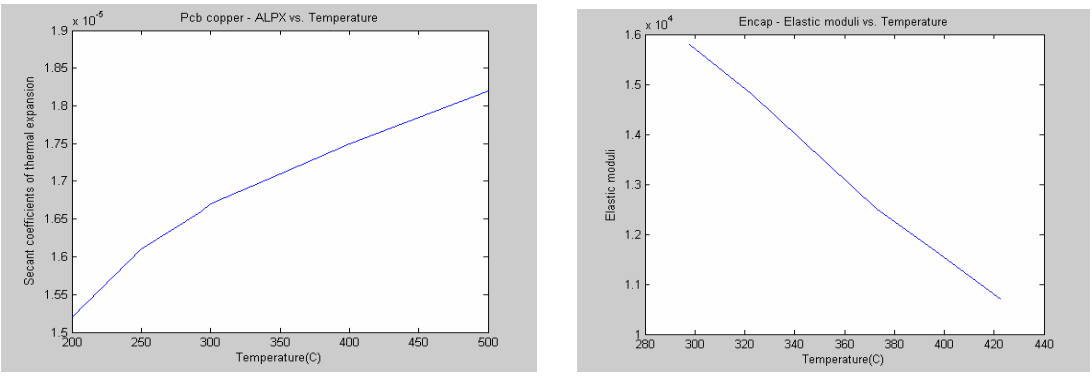


Figure 6.3 Applied Nonlinear material properties; Pcb Copper, Encap

The integrity of solder joints is a major reliability concern in modern microelectronic package. Several finite element based analysis methodologies have been proposed which predict solder joint fatigue life. Darveaux' fatigue model, which I choose for this thesis, deal with viscoplastic behavior.

6.1.2.1 Viscoplasticity

Viscoplasticity is a time-dependent plasticity phenomenon, where the development of the plastic strains are dependent on the rate of loading. The primary applications are high-temperature metal forming processes such as rolling and deep drawing, which involve large plastic strains and displacements with small elastic strains (see Figure 6.4: "Viscoplastic Behavior in a Rolling Operation"). The plastic strains are typically very large (for example, 50% or greater), requiring large strain theory [**NLGEOM**,ON].

Viscoplasticity is modeled with using Anand's model for material properties

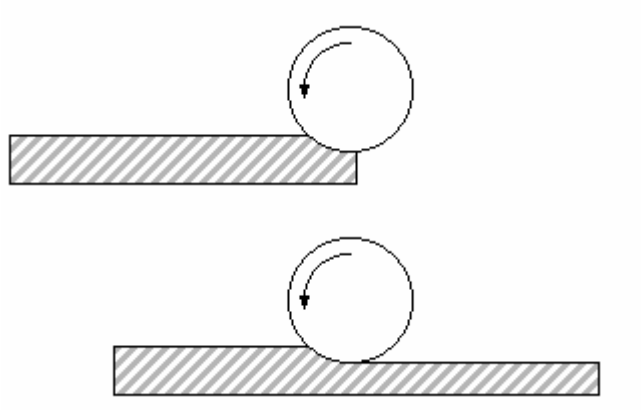


Figure 6.4 Viscoplastic Behavior in a Rolling Operation

Viscoplasticity is defined by unifying plasticity and creep via a set of flow and evolutionary equations. A constraint equation is used to preserve volume in the plastic region.

Table 6.1 Constants for Viscoplasticity equation

Initial value of deformation resistance	1800*(6.894e-3)	stress
Activation energy /universal gas constant	9400	Energy/volume
Pre-exponential factor	4.0e6	1 / time
Multiplier of stress	1.5	dimensionless
Strain rate sensitivity of stress	0.303	dimensionless
Hardening / softening constant	2.0e5*(6.89e-3)	stress
Coefficient for deformation resistance saturation value	2.0e3*(6.89e-3)	stress
Strain rate sensitivity of saturation value	0.07	dimensionless

Table 6.1 - continued

Strain rate sensitivity of hardening or softening	**1.3**	dimensionless

6.2 Solving nonlinear analysis in Ansys

This section describes basic information about nonlinear analyses and guideline of convergence problems that we may encounter in solving.

6.2.1 Basic Information about Nonlinear Analysis

ANSYS employs the "Newton-Raphson" approach to solve nonlinear problems. In this approach, the load is subdivided into a series of load increments. The load increments can be applied over several load steps. Figure 6.5: "Newton-Raphson Approach" illustrates the use of Newton-Raphson equilibrium iterations in a single DOF nonlinear analysis.

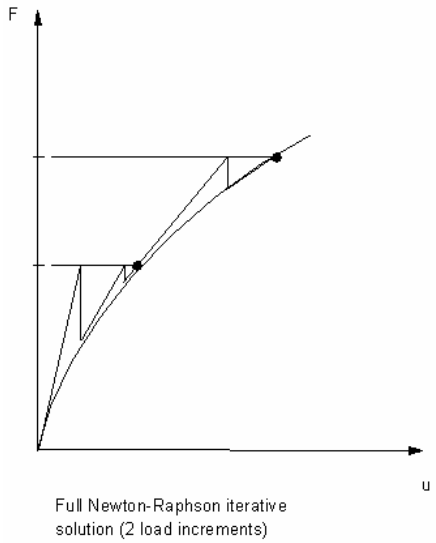


Figure 6.5 Newton-Raphson Approach

Before each solution, the Newton-Raphson method evaluates the out-of-balance load vector, which is the difference between the restoring forces (the loads corresponding to the element stresses) and the applied loads. The program then performs a linear solution, using the out-of-balance loads, and checks for convergence. If convergence criteria are not satisfied, the out-of-balance load vector is reevaluated, the stiffness matrix is updated, and a new solution is obtained. This iterative procedure continues until the problem converges.

A number of convergence-enhancement and recovery features, such as line search, automatic load stepping, and bisection, can be activated to help the problem to converge. If convergence cannot be achieved, then the program attempts to solve with a smaller load increment.

6.2.2 Mesh sensitivity and convergence problems

In fact, most simple models are recommended to use Ansys Default when solving. In this work, however, solving time is time consuming process. Figure 6.6 indicate that the number of each Substep has consistency of the result. Therefore, we can trade off the number of Susteps unless divergence problems happen in solving models.

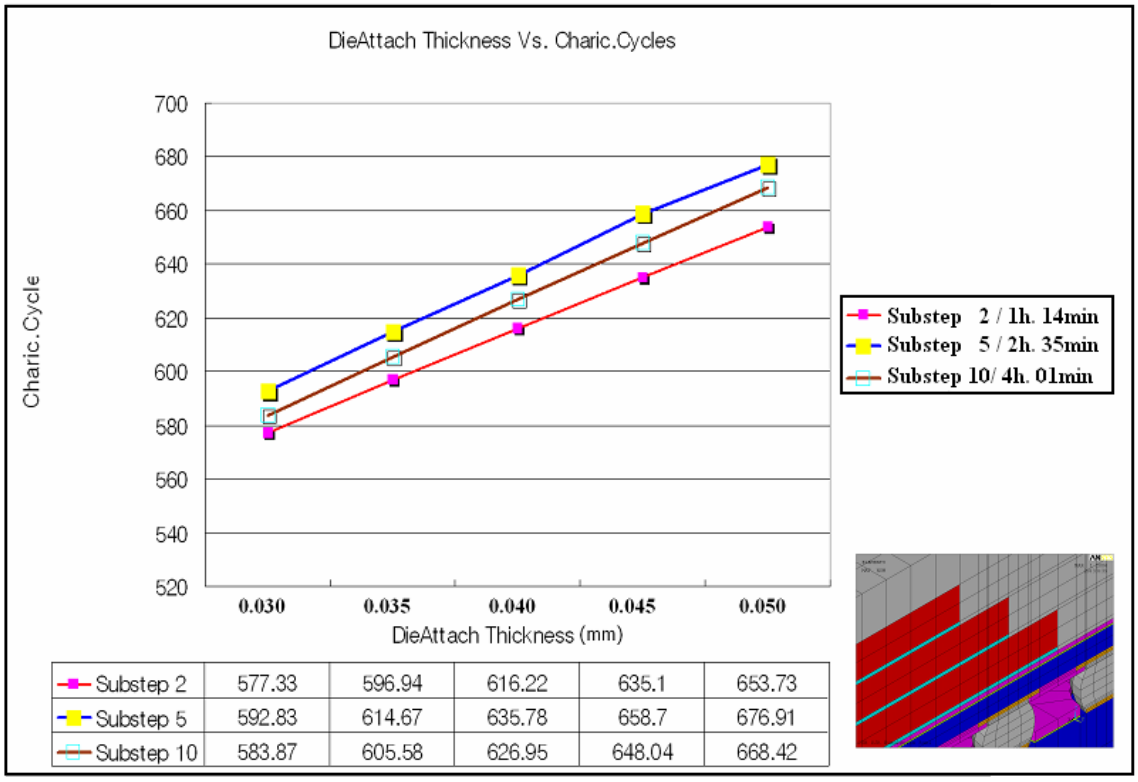


Figure 6.6 Dieattach thickness Vs. Fatigue lifes of solderballs

Some examples may be initially open contact surfaces causing rigid body motion, large load increments causing nonconvergence, material instabilities, or large deformations causing mesh distortion that result in element shape errors.

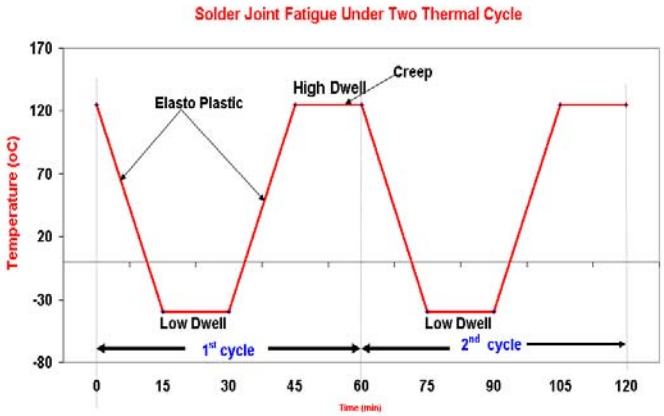
A convergence failure can also indicate a physical instability in the structure, or it can merely be the result of some numerical problem in the finite element model. The following sections will be the procedure that I used to encounter the divergence and deal with it in this work.

- Too large a plastic or creep strain increment
- Using selective Automatic Time Stepping

- Coarse mesh in Die material

As Solderballs are characterized by viscoplastic, some portions of the initial mesh can become highly distorted. Highly distorted elements can take on unacceptable shapes, providing inaccurate results. This can cause nonlinear solution to stop. When this happens, use the **ESCHECK** command to perform shape checking of deformed elements in the postprocessor (based on the current set of results in database). This deformed-shape checker will help you to identify the portions of your model that require different meshing, thereby allowing them to retain acceptable shapes. Using **ESCHECK** at different time points will help you to identify the load conditions that cause mesh deterioration.

We can use the least substeps number that result has consistency. In this work, there are two classified load categories: Figure 6.7 illustrate simulated thermal cycles are consist of ramp load time (linear increasing) and dwell load time




```
antype,static,new                          ! set solver and tollerance
eqslv,sparse,1.0E-04                       ! set analysis type
nlgeom,on                                  ! turn on large deflection and large strain deformation effects
nropt,auto,,off                            ! set newton-raphson solution options
outres,all,last                            ! write data to jobname.rst for last substep of each loadstep
tcyc=highdwel+lowramp+lowdwel+highramp     ! complete cycle
ntc=2                                      ! total no. of thermal cycles

rampstep=2                                 ! calc substeps for ramp loadsteps (1 substep/10 deg)
tref,hightemp                              ! apply uniform zero strain high temperature to all nodes
*do,m,1,ntc                                ! loop through total no. of thermal cycles

! ---- RAMP LOW/CYCLE 1 (LOAD STEP 1) ----

autots,off                                 ! turn off auto time stepping
nsubst,rampstep                            ! set substeps for this load step
bf,all,temp,lowtemp                        ! apply uniform temperature to all nodes
kbc,0                                      ! linearly ramp body force load temperatures from previous load step
time,lowramp+(m-1)*tcyc                    ! set time at end of load step
solve                                      ! solve load step

! ---- DWELL LOW/CYCLE 1 (LOAD STEP 2) ----

autots,on                                  ! turn on auto time stepping
nsubst,2,4,1                               ! set the size of first time step
bf,all,temp,lowtemp                        ! apply uniform temperature to all nodes
kbc,1                                      ! use applied body force load temperature for all substeps
time,lowramp+lowdwel+(m-1)*tcyc            ! set time at end of load step
solve                                      ! solve load step
.
..
...
....
```

Figure 6.7 Applied loading cycle in models and APDL postprocess script

In case of ramp time, **Load STEP 1**, viscoplastic strain is shown with comparatively small increment. Therefore, non-convergence problems didn't happen so that we could turn off **AUTOTS** command and define the minimum number of substeps which has shown result consistency. In Dwell time, however, the number of susteps is recommended to shift to the **Ansys Solver** and then just define Maximum number of substeps to be taken because of large deformation, especially in high dwell.

Sometimes, coarse mesh could affect convergence as well as result accuracy. Table 6.2 indicates that the difference between **Type 1** and **Type 3** are only 1% in results while solving time highly increased. Therefore, we could choose small element in die materials in limit of convergence.

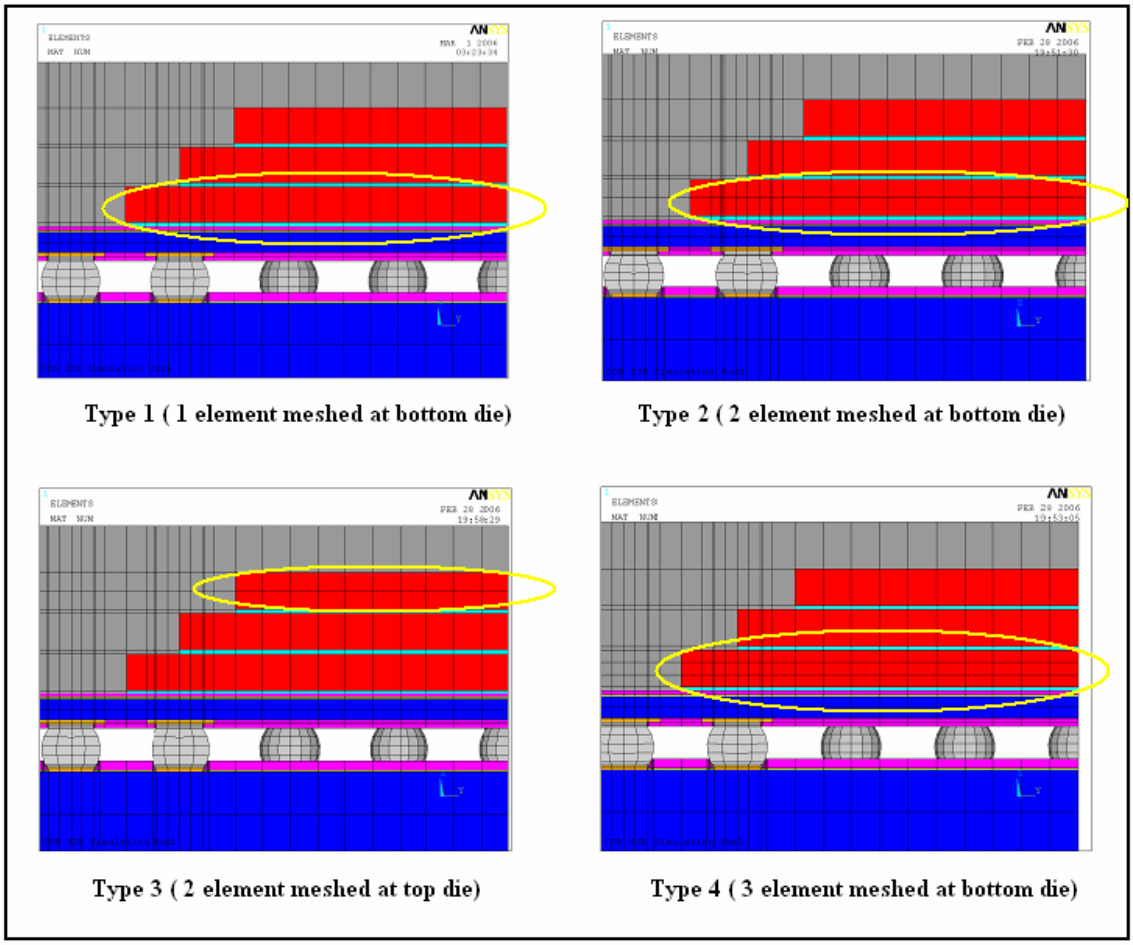


Figure 6.8 Mesh sensitivity

Table 6.2 Mesh sensitivity result

Pyramid 3dies	No. nodes	No. elements	Characteristic cycles	Solving Time
Type 1	28765	24478	561.52	1h.30m
Type 2	29959	25623	566.05	1h.44m
Type 3	29959	25623	560.93	1h. 44m
Type 4	31155	26768	567.05	1h. 58m

6.3 Summary

The accuracy of simulation results are connected with solving time. Convergence trouble also be parameters to affect final time to evaluate the results. In limit time, and memory, adapted mesh and proper convergence methods was shown up. From the result, mesh sensitivity are not affect and result of each substep size are consistent one another so that one element in z-direction are recommended for die and the minimum substep number in transient analysis could be chosen in limit of convergence.

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BIOGRAPHICAL INFORMATION

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