INVESTIGATION ON THE MECHANISM OF INTERFACE ELECTROMIGRATION(EM) IN COPPER(Cu) THIN FILMS

by

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ABSTRACT

INVESTIGATION ON THE MECHANISM OF INTERFACE ELECTROMIGRATION(EM) IN COPPER(Cu) THIN FILMS

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This study concerns the mechanism of the interface electromigration (EM) in copper (Cu) thin films. While EM in Cu is one of the most concerned reliability failure phenomena in Cu interconnects used microelectronic devices, its mechanism is not well understood yet. In order for better understanding of the EM mechanism, this study attempt to investigate the interface EM mechanism by examining the passivation effects on Cu EM using a cross-strip structure where Cu lines are cross-stripped with different passivation layers. From the observation of the marker polarity (hillocks and voids), the

interface EM mechanism is determined whether the passivation layer increases or decreases the interface EM of Cu.

A series of investigation finds that the surface/interface EM mechanism of Cu is different depending on both the passivation material and the thickness of passivation. Differing passivation materials and their thickness do induce change in the kinetics of the marker formation. In all cases, the results show that the mass transport along the metal passivation/Cu interfaces has slower EM rate than dielectric passivation/Cu interfaces. CoWP passivation provides interface with the slowest interface EM, and TaN passivation provides more stable interface with slower EM rate than Ta. In addition, Si_3N_4 passivation seems to provide interface with slower interface EM than SiO_2. On the other hand, when interface EM is compared to surface EM, it is found that the interface EM tends to be faster than the surface EM. This is somewhat unexpected result, but all systems inspected produced a consistent indication. It is found that the reason for higher rate of interface EM than the surface EM may be related to higher Z* at interface.

The results of this investigation may bear importance both for scientific and engineering aspects. This is the first study that shows direct evidence for active interface EM in Cu. While the interface EM and also surface EM needs further investigation in order to understand how they occur, especially the mechanism, the results suggest that engineering the interface may be critical for reliability improvement of Cu interconnects.

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CHAPTER 1

INTRODUCTION

1.1 Research Objetive

With a miniaturization of microelectronic devices, the reliability of interconnect is becoming more critical than ever [1-5]. For this reason, as well as to increase the circuit performance, copper (Cu) interconnect replaced the conventional interconnect materials based on aluminum (Al) and its alloy. The Cu interconnects offer higher electrical conductivity and thus effectively reduces the signal delay in the microelectronic devices [6-9]. In addition, with higher melting temperature, the Cu interconnects tend to show generally better reliability than the Al interconnects. However, the introduction of the Cu for Integrated Circuit (IC) created several new technical and theoretical challenges. One of these is the electromigration (EM) reliability [10,11]. The EM, the atomic diffusion under high current density, has been the major source of interconnect failure in IC [12-15]. It is expected that the EM reliability will be more critical problem in the future devices mainly because of increased current density.

In theory, the EM is a simple process, but failure induced by EM is a result of complex process. The failure is created by a local divergence of EM flux, which is linearly dependant on atomic mobility and EM force. The complexity stems from the fact that there are many possible EM path in Cu interconnects, namely the lattice, grain boundaries, interfaces, and surfaces. Furthermore, flux divergence varies with microstructure, making the understanding of failure mechanism exceedingly difficult. In Cu interconnects, it is believed that at least two EM mechanisms, grain boundary and surface/interface EM, are active in the temperature range of device used and accelerated reliability test [16-21].

Several published reports indicate that surface/interface EM may be the dominant mass transport mechanism leading to failure [13,17,20, 22-25], but there exists no direct evidence to support the interface EM and the role of surface/interface structure (material and thickness) on the interface EM is not well investigated.

It is true that, since the introduction of the Cu interconnects, the surface/interface EM in Cu interconnects has been extensively studied by many researchers. However, they all have been focused on the EM lifetime test, the result of which is affected greatly by various factors such as microstructure, processing and test structure [26-28]. Therefore, it is difficult to understand the interface EM behaviors in Cu and to determine what affects such behaviors. Hence, new investigative approach is necessary to isolate the interface (or surface) EM mechanism from other influential factors. For this reason, we developed a new methodology of investigating the interfacial EM in Cu thin film lines.

The study presents a new methodolo gy of investigating the surface/interface EM of Cu, and also presents the influences of interface materials on the interface EM mechanisms in Cu thin films studied by the developed methodology. The new method, so called cross-strip, utilizes, a strip of a second material patterned across a Cu line, thus creating an isolated area on the Cu surface. This method has been extensively used for studying alloying effect on aluminum (Al) EM [29-32]. In our tests, the cross-strip concept has been modified to investigate interface EM in Cu interconnects. Surface is the same condition but interface condition is different due to different passivation layers. The cross-strip creates the flux divergence of EM and allows to observe the nature of the divergence as it induce formation of hillocks and voids at the ends. In case of the passivating cross-strip we are using, the flux divergence is likely to be created by difference in interface EM rate. Although both grain boundary and interface EM are expected to occur [16-25], but their contribution to the marker formation (hillock and void) is far smaller than the interface EM.

With the developed investigative method, this study further aims to find: (1) the relative EM rate between surface and interface in Cu thin films, (2) difference in interface EM rate between two different passivation materials in Cu interconnects, and (3) the effects of temperature and current density on Cu EM. In order to accomplish these goals, this study examines: (1) different passivation materials, (2) different passivation thickness and length, (3) different test ambients, (4) different temperatures and current densities, and (5) different test configurations.

The interface materials chosen in our study includes tantalum (Ta), tantalum nitride (TaN), titanium nitride (TiN), chromium (Cr), cobalt tungsten phosphide (CoWP), silicon nitride (Si_3N_4), and silicon oxide (SiO_2) films. They are chosen because they are interface materials of practical importance. They are either being used or considered as interface material in real interconnects. Ta, TaN and TiN films are used as adhesion or diffusion barrier layer, Si_3N_4, and SiO_2 films are used as dielectric and passivation layer, and CoWP film is used as a passivation layer in microelectronic devices.

This dissertation organized as follows: Chapter 1 presents the background information of this study, where the basic theory of EM and EM in interconnect, as well as the various other factors affecting EM are reviewed. Chapter 2 presents the results of single passivation layer cross-strip test. Chapter 3 presents the temperature and current density effects on Cu EM. Chapter 4 turns its focus to the double passivation layer cross-strip and under-layer cross-strip tests to support single passivation layer cross-strip test. And interface EM rates between two different passivation materials will be compared. Finally, chapter 5 summarizes the main findings and offers suggestion for future research directions.

1.2 Background

1.2.1 Cu interconnects

In recent years, great progresses in interconnect technologies have been made, and Cu interconnects have been used to take place Al interconnects. The transition to

Cu as interconnect metal began with intensive research and development efforts in the early 1990's, which led to IBM's electroplated 0.22μm CMOS generation and Motorola's physical vapor deposited Cu product [33,34]. The transition to Cu interconnects have begun because that Cu offers many intrinsic advantages over conventional Al-based alloy interconnect, including higher electrical conductivity and higher mechanical strength. Cu is also expected to show better reliability because it has much lower grain boundary and lattice diffusivity than Al because of its higher melting temperature [35].

The current generation of Cu interconnects are generally manufactured using the dual-damascene method because Cu lacks the appropriate dry etch plasma chemistry needed to pattern the lines. In the damascene process, trenches and via holes are etched into the dielectric layer; then liners and Cu layers are deposited to fill in the pattern, followed by chemical-mechanical planarization (CMP). Similarly, Cu lines and vias can be formed simultaneously with a dual-damascene process flow. A simplified dual damascene process flow for Cu interconnect is illustrated schematically in Figure 1.1.

The advantages of damascene processing include patterning without metal etching and a three-dimensional network of interconnections called multilevel interconnection (MLI) is available for Cu damascene process to replace the Al interconnection network [36].

The use of the Cu interconnects has produced substantial enhancement in interconnect performance both in electrical and physical aspects. In case of Al interconnects, the interconnection network is two-dimensional planar configuration

because damascene and CMP process is not available, therefore, it becomes more and more unsuitable for high performance interconnection because of the following reasons: (a) lack of space to provide interconnections for all devices in a two-dimensional planar configuration, (b) interconnect RC delay, and (c) reliability for large current densities. Such benefits increase when the multilevel interconnection is considered. In multilevel interconnection, the metal interconnections are not confined in one plane, therefore, RC delay can be reduced due to the reduced interconnection length and the increased cross-sectional area of interconnects.

For this reason, according to the prediction of Semiconductor Industry Association (SIA) National Technology Roadmap for Semiconductors (NTRS), as many as eight to nine levels of metals in a multilevel interconnection scheme for high performance chips can be used [1,40]. In this concept, as shown in Figure 1.2, several levels of Cu interconnect can be employed.

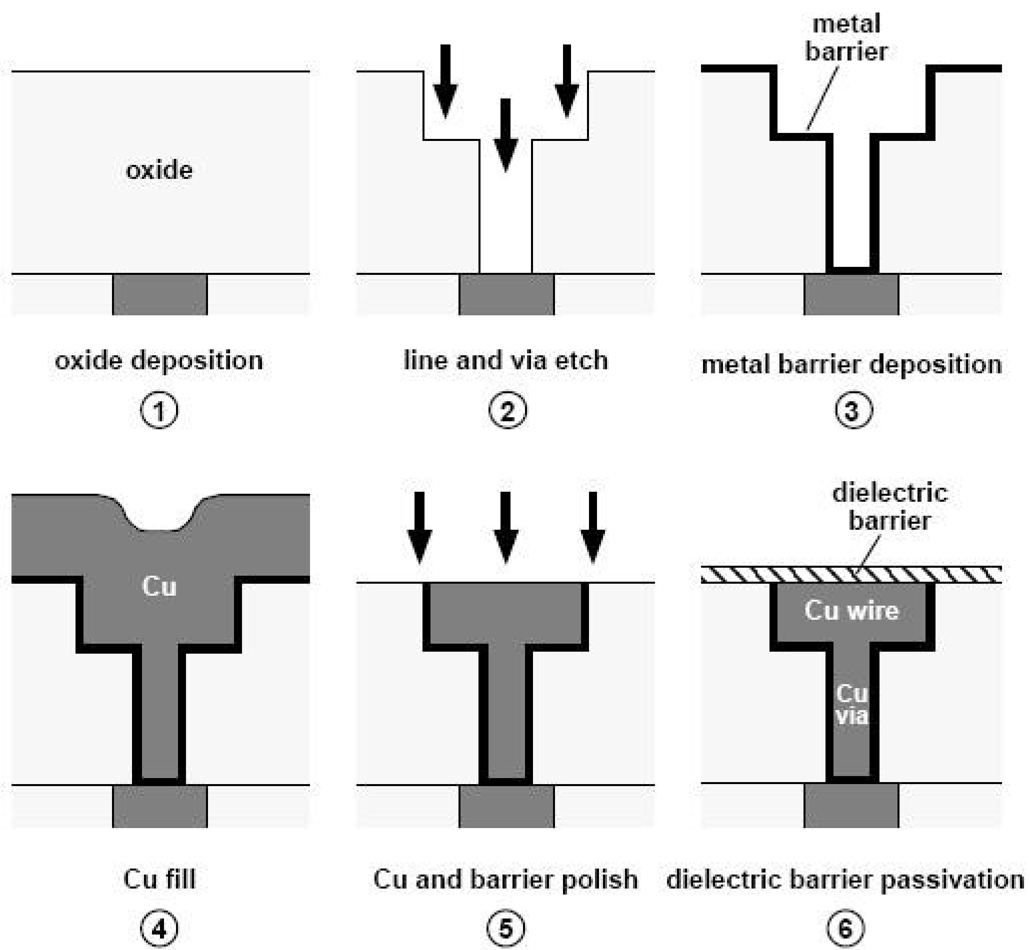
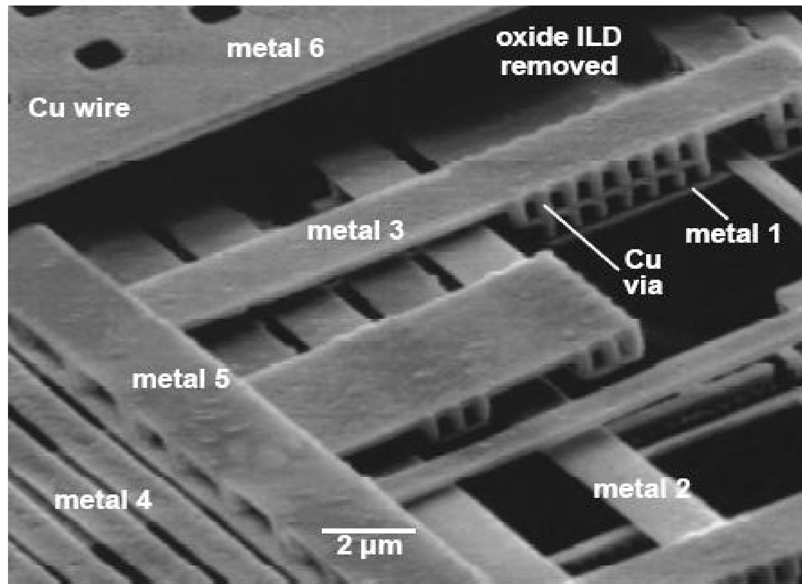
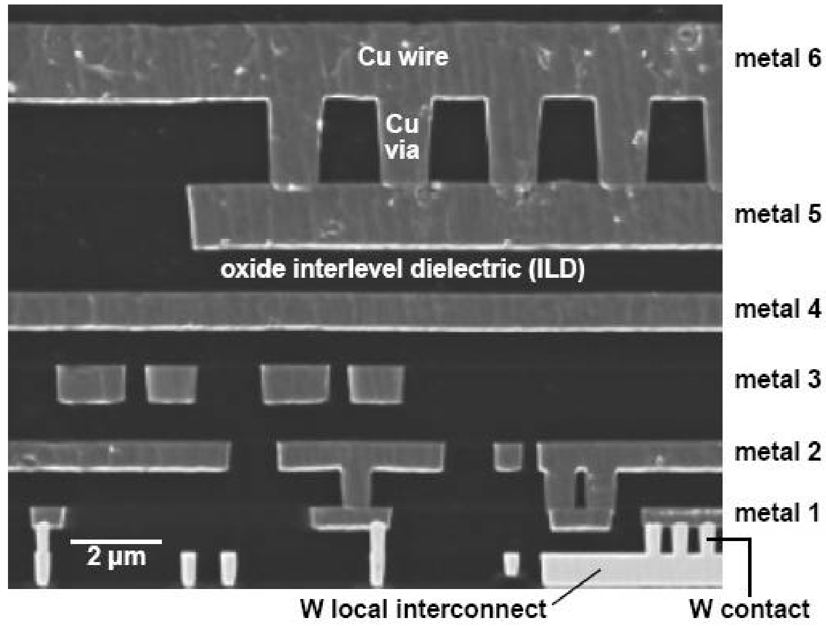


Figure 1.1 Simplified copper dual damascene process flow [37]



(a)



(b)

Figure 1.2 Multilevel interconnections; Demonstration by
(a) Motorola, and (b) IBM [37-39]

1.2.2 Reliability issues in Cu interconnects

The reliability of metal interconnect is a major concern for modern IC fabrication. With decreasing the device dimensions, the length of the interconnect increases while the interconnect line width decreases. These two factors lead to higher electrical resistance and higher current density in the metal interconnects [1-5]. For this reason, reliability problems such as EM become increasingly important to reliability problem in Ultra-large scale integrated (ULSI) circuits [10,11].

EM describes the development of structure damage caused by metal ion transport as a result of high-current stressing in thin metal film. As previously mentioned, Cu is expected to have high reliability in addition to low resistivity compared to Al-based metal interconnects. However, there still exists reliability issues in Cu interconnects, including the EM itself [10,11]. Many investigations suggest that the Cu interconnects is still prone to EM induced failures, although the resistance against EM failure is far better than the Al interconnects. Also, those studies suggest that the EM failure occurs in different mechanism from those in Al interconnects. Such difference is believed to related to the lack of passivation oxide in Cu. Unlike Al, Cu does not have a self-passivation layer. Exposed surfaces will continue to oxidize, leading to poor barrier adhesion and high resistance. Also, the lack of self-passivating oxide demands the use of artificial passivation materials (such as Ta and SiN), and such interfaces are not necessarily resistant against EM [12,13,17-20]. With continuing miniaturization of the Cu interconnect dimension, the question as to the extent of the interface EM has intensified and, in fact, has created significant concerns.

1.3 Review of electromigration (EM) mechanism

EM in interconnects has been studied the late 1960's when it was first observed in wide Al-based interconnects [41]. As one of the main IC failure mechanisms, EM performance will continue to be one of the main issues in integrated circuit reliability for a relatively long time. Modern microelectronic devices use either Al or Cu thin films as interconnection materials, both of which are susceptible to physical failure by EM. Although the signal current itself is small, due to the sub-micron scale of the interconnects, current density is sufficient to induce EM. A small amount of EM in the interconnect can result in catastrophic circuit failure by void formation or hillock formation. Therefore, it is of great importance to accurately assess the effect of EM on interconnect reliability.

1.3.1 Mechanism of electromigration (EM)

The EM refers the phenomena of atomic transportation in a conductor under the influence of high electrical current density. High current density provides driving force to atoms migrate to the direction of electron flow. The driving force for EM consist of the two forces acting on metal atoms [12, 42-46]. The first is the interaction of the applied electric field and the metal ions. This electrostatic force contains the interaction of the ion with valence Z and applied field as well as any electrostatic shielding from the surrounding electrons. This contribution is often referred to as the "direct" force. The direct force can be written as

$$F_D = Z(1-k)e\vec{E}$$

$$= Z_D * e\vec{E}, \qquad (1.1)$$

where k describes the electrostatic shielding and $Z_D *$ is the effective charge caused by the electrostatic force $F_D *$, $Z_D * = Z(1-k)$. The second contribution to the total force, F, arises from the momentum transferred to the ions from the electrons. This contribution is often referred to as the " electron wind" force.

The simple theoretical description of the wind force can be seen from the following discussion. In a given conductor, the number of collision per unit time between the electrons and diffusion ions, $n_{collision}$, is approximately given by

$$n_{collision} = n_e v_e \boldsymbol{s}_e \qquad (1.2)$$

where n_e is the number density of electrons, v_e is the average electron velocity, and $\boldsymbol{s}_e$ is the cross section for scattering between an electron and a diffusio n ion. In the scattering process, the electron transfers all of the momentum it gained since its previous collision. The average momentum transferred per collision is given by

$$\Delta p = e\vec{E}\frac{l_e}{v_e} \qquad (1.3)$$

where e is the charge of an electron, E is the electric field and l_e is the mean free path of the electrons. The product of these two equations is the wind force

$$\vec{F}_{wd} = -n_e \boldsymbol{s}_e |e| \vec{E} l_e \qquad (1.4)$$

As defined in eq.(1.4) the wind force is directly proportional to the electric field applied to the metal. It is traditional to define an effective charge of the metal ions

$$F_{wind} = Z_{wd} * e\vec{E} \qquad (1.5)$$

where Z_w is the valence of the diffusion ion.

The total force, F, is simply the sum of these two components.

$$\vec{F} = \vec{F}_D + \vec{F}_{wd} \tag{1.6}$$

$$= (Z_D * + Z_{wd} *) e\vec{E}$$

$$= Z * e\vec{E} \tag{1.7}$$

where $Z*$ is the effective charge number for the migrating metal ions describe in this system. Z* can be either positive or negative depending on the direction along which migrating ions diffuse. Depending on which of the force is stronger, metal atoms toward the cathode or anode end of the conductor. However, for a good conductors Z* is found to be in the range of ~ -10, indicating that the direct force is small compared to the wind force. It is generally believed that the contribution of the direct force is reduced substantially by screening effects by free electrons. Therefore, electron "wind" force is dominant and metal atoms migrate in the same direction as the electron flow [12,42-47].

Under the given driving force, the metal atoms move with rate controlled by the diffusivity. The atomic EM flux can then be obtained through the relation J=μF, where μ is the atomic mobility. The atomic mobility is related to the atomic diffusion coefficient, D, by the Nernst-Einstein equation, $\boldsymbol{n} = nD/kT$, where n is the mass density of the metal, k is the Boltzman's constant and T is the absolute temperature [48]. By substituting the applied electric field with the product of the current density, j, and the metal resistivity, ρ, the following equation is derived.

$$J_e = n(D/kT)Z * e\mathbf{r}j$$

$$= nv_e \tag{1.8}$$

where, J_e, is the atomic flux due to EM and V_e is the drift velocity due to EM. Drift velocity is a product of the mobility (D/kT) times EM driving force (F):

$$v = (D/kT)F \tag{1.9}$$

Hence, the drift velocity due to the EM force is give by

$$v = \frac{De\mathbf{r}jZ*}{kT} \tag{1.10}$$

The atomic diffusion coefficient D is a function of temperature in Arrhenius equation as follows [49]:

$$D = D_O \exp(-\frac{E_a}{kT}) \tag{1.11}$$

where D_O is a proportionality constant (m^2/sec), Ea is the activation energy (eV) associated with the diffusion mechanism (or path). At fixed temperature, the value of D is different for different diffusion paths.

Since the dependence of $\mathbf{r}$ on T is nearly linear, v/j follows Arrheniuns behavior. Therefore, the EM flux becomes

$$J = \frac{n}{kT} D_O e^{-Q/kT} e\mathbf{r}jZ* \tag{1.12}$$

It can be seen that EM flux is determined by temperature in addition to electric current applied.

1.3.2 EM in interconnects

The interconnects of modern semiconductor are highly dense and intricate networks containing millions of line segments terminating with vias and contacts. As the interconnect dimension becomes smaller, they become more susceptible to EM induced failures due to increase in current densities and surface/interface fraction. EM itself in interconnects can occurs through several different diffusion paths. These paths include diffusion through the bulk, grain boundaries, interfaces, and surfaces. The effective diffusivity can be written as the sum of the diffusivities associated with different paths. The following equation shows the effective diffusivity written as the sum of the bulk, grain boundary, interface, and surface [17,50,51].

$$D_{eff} = D_b + \sum_j^n D_{gb,j} (\frac{\boldsymbol{d}_{gb,j}}{d}) + D_i [2\boldsymbol{d}_i (\frac{1}{w} + \frac{1}{h})] + D_s (\frac{2}{w} + \frac{1}{h}) \qquad (1.13)$$

where the subscript b, gb, i, s refer to the bulk, grain boundary, interface, and surface, respectively; D_{eff} is the effective diffusivity, $\boldsymbol{d}$ is the width of the grain boundary, w is the width and h is the height of the interconnect.

With several mechanisms contribute to EM mechanism, the activation energy (Ea) for EM failure in interconnects can be a function of temperature since a particular diffusion mechanism dominated a temperature range. The bulk diffusion term can be ignored because the temperatures of practical importance are too low for the bulk diffusion to be significant compared to others. Thus, the most important diffusion mechanisms to be considered for Cu interconnects are the grain boundary diffusion and

interface diffusion [17,50,51]. In that case, the drift velocity of Cu ions under EM can be expressed as

$$v_d = D_{eff} Z^*_s \, e\rho j / kT \tag{1.14}$$

where Z^*_s is a coefficient based on momentum transfer from electrons to copper atoms. In case of Cu interconnects, various studies suggest that the bulk and grain diffusion plays insignificant role, and thus eq.(1.13) reduces to

$$D_{eff} = D_i [2\delta_i (\frac{1}{w} + \frac{1}{h})] \tag{1.15}$$

where D_i is the interfacial diffusion.

Another important consideration of EM in interconnects is the presence of the stress-induced back flow, namely the 'Blech' effect [52,53]. If the particular metal line of interest is embedded in a stiff dielectric material like SiO_2 the back flow force is created which opposed to the EM force. This force arises as atoms are depleted from the cathode and accumulated at the anode. The accumulation and depletion of mass in confined space creates the stress. In places where mass is accumulated, compressive stress is induced. In the opposite case, tensile stress is developed. In interconnects, these two places are closely spaced, resulting in a steep stress gradient. This stress gradient counteracts the EM force and reduces the net atomic flux, as illustrated in Figure 1.3.

In this configuration, $\Delta\sigma$ is the local gradient in the hydrostatic stress in Cu and its maximum value is a function of the surrounding structure. For stiff surroundings, $\Delta\sigma$ can reach a higher value than for a more compliant structure.

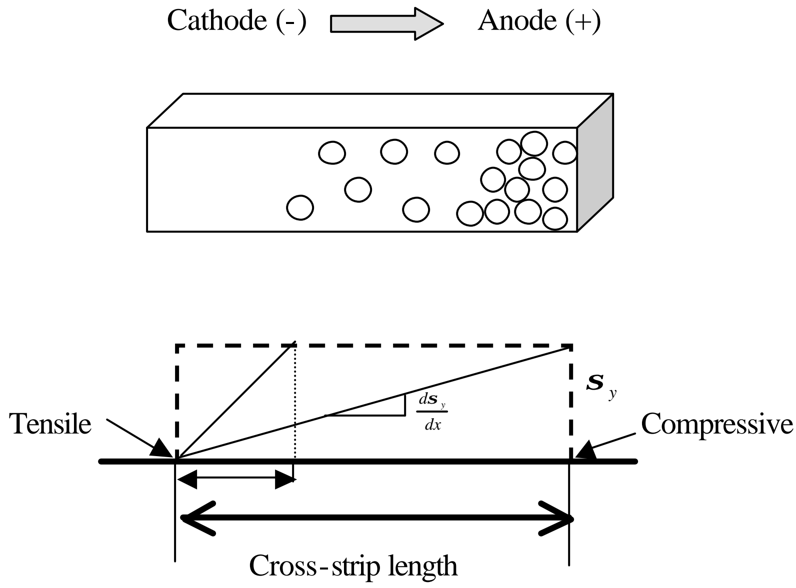


Figure 1.3 The schematic diagram illustrating net atomic flux and stress gradient

The net atomic flux in an interconnect due to the combined effects of the EM force and the stress gradient can be expressed as [52-58]:

$$J_{net} = nv_d = n(v_e - v_b)$$

$$= n(D/kT)(z^* e\rho j - \Delta\sigma\Omega_a / L) \qquad (1.16)$$

where v_e is atomic migration due to EM, v_b is atomic back flow due to and EM-induced stress gradient, v_d is the net drift velocity, $\Delta\sigma$ is the stress gradient, Ω_a is the atomic volume, and L is the line length.

The back-stress affect can improve the EM resistance of metal lines if the product of the current density j, and line length, L, is equal to or less than a threshold value, Γ. If the current density is held constant then there arises a critical length, L_c,

below which there will be no net EM flux. The threshold value and the critical length are expressed as

$$\Gamma = jL_c = \Delta\sigma\Omega_a / Z^* e\rho \tag{1.17}$$

1.4 EM failure in interconnects

1.4.1 EM lifetime testing

The most common method for evaluating the EM reliability is a lifetime measurement under accelerated conditions (high temperature and high current density). EM performance is characterized by the mean time-to-failure (MTTF or t50), that is the time at which 50% of the test sample has failed cumulatively, and σ that is the dispersion of time-to-failure distribution.

In 1969, Black conducted a series of accelerated testing designed to evaluate the temperature and current density dependence of the time to failure [55,56]. MTTF is defined as the 50 % point of the time to failure distribution.

$$MTTF = t50 = Aj^{-n} \exp\left(\frac{E_A}{kT}\right) \tag{1.18}$$

where t50 corresponds to the cumulative probability P=50%, A is technology-dependent and structure-dependent pre-exponential factor and is dependent on the material and conductor geometry, j is the current density (A/cm^2), n is the current density exponent, where n varies between 1 and 2 depending on the mode of failure (during void formation or void growth). E_A is the activation energy of the EM associated with the diffusion mechanism, k is Boltmann's constant and T is the absolute temperature. The

MTTF and σ are obtained from the log-normal curve that is the best fit for EM time-to-failure. High MTTF and low σ are desired for good EM performance. The chief benefit of lifetime test is the ability to test large numbers of specimens at the same time. However, it would be difficult to determining the mechanisms of EM failure solely using this method.

The main purpose of the EM lifetime testing is to determine the activation energy and current dependence of the failure rate for given interconnect structure. Such testing is necessary because the prediction of the interconnect reliability under use condition needs to be conducted for any given set of interconnects produced. In addition, the testing is conducted to identify the weak part of interconnects that needs to be improved for better reliability. The latter part is especially important for interconnect development because EM failure rate is affected greatly by many factors in interconnects and the reduction of the potential failure site can be achieved by EM testing. Many factors contributing to the EM failure rate, and such factors are related to site for flux divergence. Such places include locations with a change in current density and direction, interface between different materials, defects such as grain triple points, conductive and non-conductive contaminants, dopant precipitate and segregation, grain size variations, and so on.

1.4.2 Various factors affecting Cu EM

EM failure rate is profoundly influenced by a number of factors. In thin film conductors, EM-induced flux divergence can be caused by inhomogeneity in local

structure and temperature because the variation of micro-structural parameters of thin film causes a non-uniform distribution of atomic flow rate. The magnitude of the atomic flux divergences depends on the degree of the structural and thermal inhomogeneities in the metallic thin films. The structural imperfections include point defects, dislocations, grain boundaries and triple points. The factors which influence the EM of Cu interconnects can be classified into those which impact Cu fine structures, such as Cu grain size, degree of crystal orientation, etc., and those relating to the condition of the interface between Cu and passivation layer.

1.4.2.1 Grain size and line width

Since atoms are more loosely bounded at the grain boundaries than in the lattice, atoms migrate along grain boundaries more easily than through the lattice. Ideally, therefore, the EM failure rate should depend on the grain size (d) of metallic thin film. Such a dependence is well documented in case of Al interconnects, however, the dependence is found to be less pronounced in Cu interconnects. It is probably because the interface EM is most dominant in Cu interconnects.

Ideally, the grain size and linewidth affects the EM failure rate (if everything else equal) because it affects the flux divergence. In case of Al interconnects, the dependence is found to be very pronounced and shows slower failure rate both at wide and narrow lines. In case of wider lines, since the line contains many grains, the flux along the line is more uniform. With the reduction in degree of flux divergence, EM failure rate is reduced [57]. On the other hand, when the linewidth is extremely narrow,

the line structure becomes bamboo-like. In such a case, the EM can not proceed continuously through the grain boundary network but involve lattice or other diffusion paths. This leads to higher EM failure lifetime.

Various studies have investigated the EM failure rate dependence of the Cu interconnects on the grain size and the linewidth and revealed that the dependence is less pronounced than those found in Al interconnects. It appears that the less strong dependence seen in Cu interconnects originates from two sources. The first is the fact that the study of the width dependence (or size dependence) involves several unknown line structure factors. The Cu interconnects are made by damascene process, so that the microstructure developed in different trench widths is not the same. With such a limitation, it is extremely difficult to determine how EM rate (or the failure mechanism) changes with width and grain size. The second problem is related to the intrinsic properties of Cu interconnects, that is that the EM in Cu interconnects occurs also through interface. As the interface EM should affect the resulting EM failure data, the width or grain size dependence is straightforward but requires complex analysis to extract the contribution of each EM components to the lifetime. However, a few studies do indicate that the grain structure may influence the EM failure because the failure rate appears to vary with the texture.

1.4.2.2 Texture

A few studies find that EM lifetime varies significantly with textures in Cu interconnects. For example, it is found that CVD Cu with (111) texture show much

longer lifetime than CVD Cu with (200) texture [24,59]. The varying EM failure rate with the texture is attributed to the possibility that the tighter tilting distributions of grains in (111) textured interconnects create slower atomic diffusion. However, whether such results can be related to grain structure effect or not is not clear yet because it is possible that interface EM still affects the result.

There are two ways to view the experimental results. The first is to relate the results to grain structure effect. In highly textured films, large portions of the grain boundaries are low-angle, where the atomic arrangement is relatively ordered and the grain boundaries are more uniform. Such microstructure reduces the grain boundary diffusion (and also the flux divergence) and thus reduces the failure rate. In randomly oriented grains, flux divergence is more likely to occur at the grain boundary junctions.

The second possibility is that the texture induces the formation of low diffusivity interfaces. It is known that self-EM on the low-miller index faces of Cu should be dominated by the wind force and it varies with surface orientation; -26e, -24e, and –22e for self-EM on Cu(100), Cu(110), Cu(111) respectively [60]. Furthermore, it is also known that the activation energy for surface diffusion differs with surface orientation, activation of (111) surface being much lower than on (100) or (110) surfaces [24,59]. As a result, different texture impart influence on the EM failure rate not by differing grain boundary EM rate but by differing interface EM rate.

1.4.2.3 Passivation layer

It is generally agreed that the surface/interface diffusion is the most active in Cu. Therefore, the passivation layer that creates interface with Cu is expected to play an important role in determining the EM reliability of Cu interconnects [26,27]. Various studies have reported that EM failure rate is affected significantly by the passivation material, thickness of passivation layer, interface condition of passivation/metal interconnects, stress condition, etc. While these studies show consistent results indicating that the interface EM is the most active EM mechanism in the Cu interconnects, they fail to show how interface EM is affected by interface condition. An important question to answer is what interface would provide better interface against EM failure, and such question is still not answered. With the complexity of EM mechanism in Cu interconnects, finding the answer is extremely difficult and requires lengthy and complex analysis. Due to this difficulty, the question is still remained unanswered in the interconnect community although the answer is increasingly important.

Complexity of EM failure analysis in Cu interconnects can be seen from following example. N. G. Ainslie et al. report that the EM failure rate is reduced by passivating the Cu interconnects [26,27]. Superficially, this result can be attributed to the suppression of surface diffusion that may provide faster diffusion path than the interface. However, it is not simple as what appears to be because the EM may be affected by the "Blech Effect". As shown in equation (2.7), the EM induced stress-gradient counteracts the EM driving force, resulting in reduced mass flux. When Cu is

not passivated, the surface is not constrained and the Cu is allowed to expand and contract. This makes the stress build-up to be small, if there is any. On the other hand, when the Cu is encapsulated with rigid dielectric materials, the free expansion and contraction is less allowed and much higher stress gradient can be resulted. Therefore, EM flux under confined condition would show much longer EM lifetime even if the interface EM were faster than the surface EM.

From above discussions, it is clear that the mechanism of EM in Cu interconnects is not well understood. Even the question as to the degree of surface EM compared to interface EM is not well answered in the field. Furthermore, it is not known which interface would provide best interface for EM reliability. Such uncertainty of the mechanism makes the design and development of interface materials in microelectronics and demands elaborate investigation on the fundamental aspects of interface EM mechanism. Also clear is the fact that the conventional EM testing method is not likely to work for the desired purpose. The EM lifetime is a result of complex process with numerous influential factors involved. With such a method, it is nearly impossible to isolate one mechanism from other. This formed basis of our efforts in developing the "cross-strip" method.

1.5 Cross-strip test

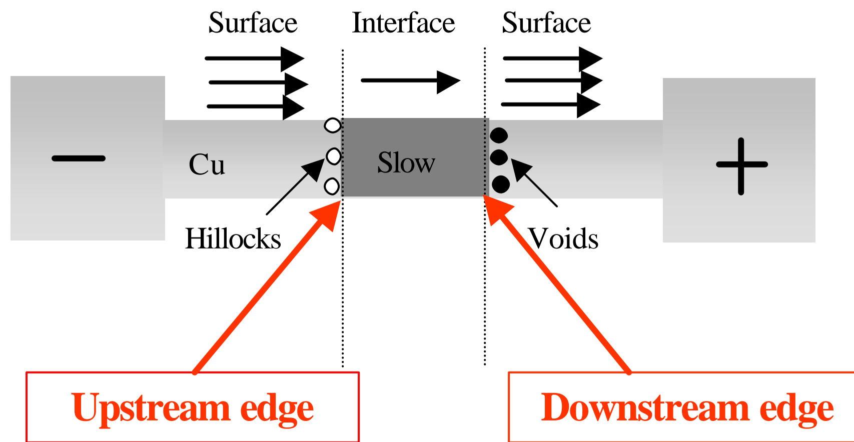
The concept of the cross strip test is simple and initially was introduced by Howard and Ross, which was further developed by others [29-32]. The cross-strip method was initially used to study the solute effect on EM mechanism, but the cross-

strip test we developed here aims to test interface EM in reference to surface EM. As shown in Figure 1.4 a cross strip configuration consists of a Cu conductor line and a cross strip of passivation layer. During the EM test, electrical current passes through the Cu surface, passivation/Cu cross-strip, then Cu surface region again.

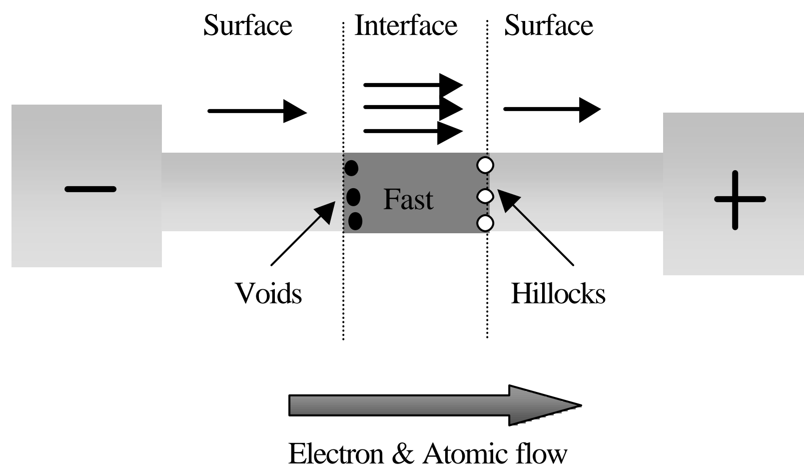
The passivation creates an artificial interface. Since all micro-structural features are the same between the cross-stripped passivation and unpassivated Cu surface except for the possibility of having different mechanical constraints, any markers formed by EM should indicate the relative difference between surface and interface EM rate.

The marker forms because the variation of surface/interface chemistry or other parameters over a film causes a non-uniform distribution of atomic flow rate. Therefore, non-zero atomic flux divergence exists at the places where the number of atoms flowing into the area is not equal to the number of atoms flowing out of that area per unit time. With the non-zero atomic flux divergence, there will be either a mass depletion (divergence>0) or accumulation (divergence<0), leading to formation of voids and hillocks.

The polarity of the markers and their amount, hillocks and voids, provides evidence for interface EM. If the passivation suppresses the EM, the EM rate is slower in the cross-strip region. In this case incoming flux is larger than outgoing flux at the upstream edge of cross-strip, resulting the formation of hillocks at the upstream (with respect to electron flow) edge and voids at the down stream edge of cross-strip. On the other hand, if passivation results in the faster EM rate in the interface than surface, hillock and void would with a reverse polarity.



(a)



(b)

Figure 1.4 The schematic diagram of cross-stripe sample configuration; (a) Surface EM > Interface EM, (b) Surface EM < Interface EM

CHAPTER 2

STUDY OF INTERFACE AND SURFACE ELECTROMIGRATION (EM) USING SINGLE CORSS-STRIP CONFIGURATION

2.1 Introduction

As discussed in chapter 1, one of the main debates on EM mechanism lies on the question whether interface (or surface) EM play a role in Cu interconnects [13,17,20, 22-25]. Also debated is the choice of the interface materials that retards EM rate, if the interface is active part of EM path, because it will guide microelectronic industries to enhance the reliability of Cu interconnects. However, answers to such questions have not been provided in any previous studies. Our study aims to provide answers to those questions by characterizing of interface EM characteristics using cross-strip method. We create an artificial interface with different passivation layers, and the interface EM characteristics under different interface conditions are examined. Our experiments consist of the cross-strip configuration having various interface materials and compare the characteristics of interface in reference to the surface EM. Results from this study reveal that interface EM does exist and its extent varies with cross-strip materials, thickness, length, test ambient, and so on. Furthermore, it is found that the rate of interface EM is faster the surface EM in Cu interconnects. This chapter presents evidence supporting these findings and discusses their importance.

2.2 Experiments

2.2.1 Single cross-strip sample configuration

The sample configuration used in this study is based on the single cross strip structure. As shown in Fig.2.1, the single cross-strip configuration involves a base Cu line having local area covered with the passivating layers. Under this configuration, the markers should form as a result of the flux difference between the interface EM and surface EM. Therefore, this configuration enables us to determine whether a particular interface offers faster or slower EM path than the Cu surface. The test line is consisting of 3 parallel lines connected in series. Typically, the width of these lines is 20um, while their thickness is varied from 0.1 to 1.3um. One test pattern contains 8 individual cross-strip area. Their lengths are 20, 40, 60, 80, 10, 160, 200 and 300um. The variation in the strip length is introduced to examine the presence of the Blech effect. As discussed in Chapter 1.3.2, the EM driving force is affected by EM induced back-flow. If the back flow driving force exists, the kinetics of marker formation would vary with the length (or width and thickness) of the cross-strip. The 8 different lengths of cross-strip patterns are introduced to investigate such an effect.

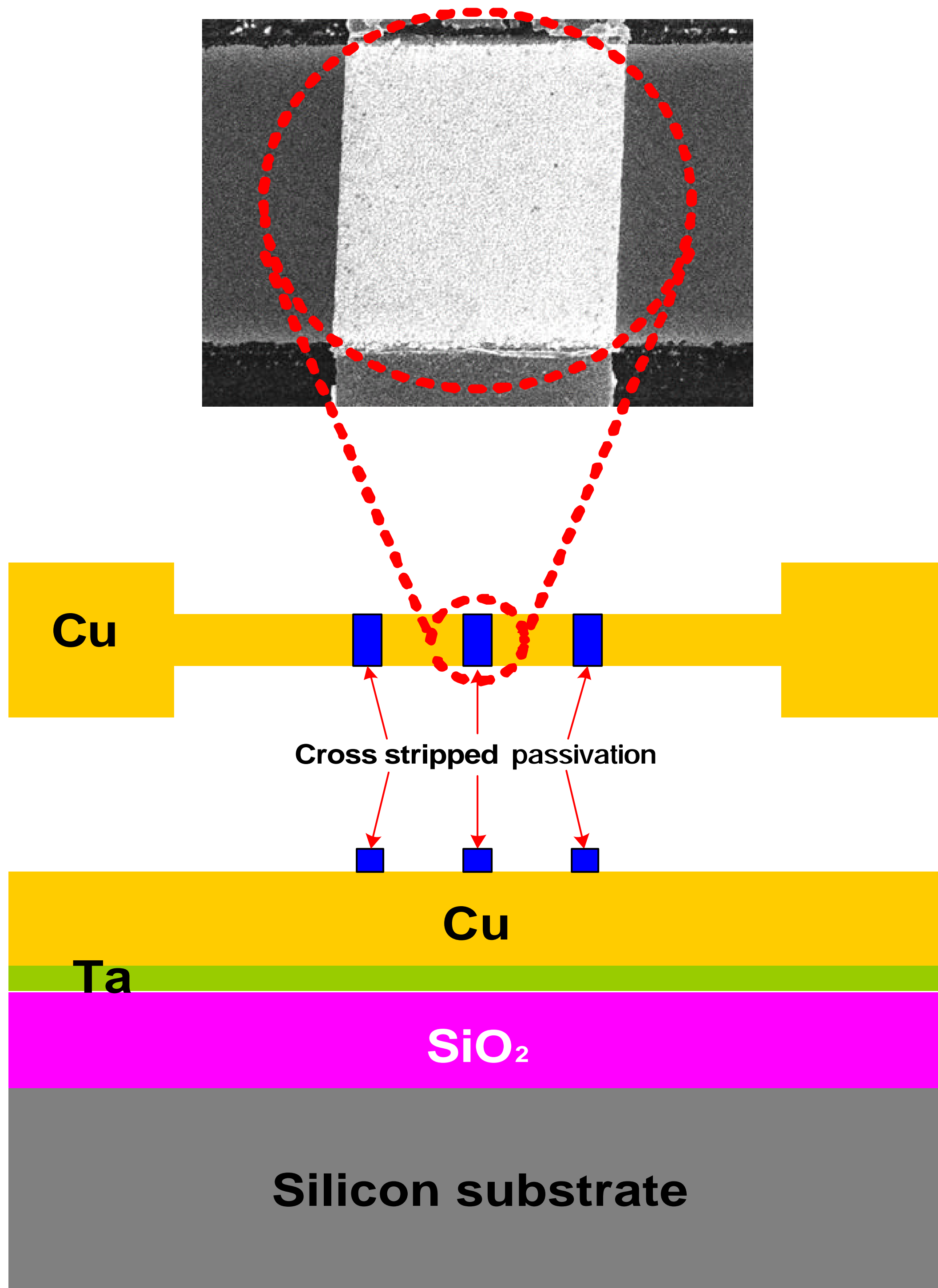


Figure 2.1 A schematic diagram of sample configuration

2.2.2 Sample preparation

The samples needed for the single cross-strip testing are prepared in 3 steps: film preparation, line patterning, and cross-strip layer deposition. The Cu films used in this study are prepared either by using sputtering or electroplating. In this process, Si wafer is oxidized to form the 0.1um thick thermal SiO_2 layer. The formation of SiO_2 is needed to prevent Si from diffusion to Cu lines. Some wafers are coated with 15nm thick Ta layer after SiO_2 formation to enhance the adhesion of Cu to the substrate. The During line patterning, Ta layer is also removed except for the area underneath Cu lines. In this way, adhesion of the Cu line to Si substrate is enhanced while preventing the short-circuit among test lines.

The test lines are patterned using a standard lithography technique. It involves photo-resist application, exposure to pattern mask, developing and finally an etching. The etching of Cu films is done by using wet chemical etching method, and the etching solution used is a 1:1:2 solution of acetic acid (CH_3COOH): hydro-peroxide (H_2O_2): de-ionized water (H_2O) and 1:1:2 solution of hydrofluoric acid (HF): nitric acid (HNO_3): de-ionized water (H_2O) respectively.

The final step of the sample preparation is the creation of the cross-strip layer. For patterning of the cross-strip over layer, a similar photolithography technique as the one for the test line patterning is used, but the method employed is the lift-off process. In this process, the test line is coated with photoresist, which is then exposed to pattern mask. The area of the photoresist removed during developing process is the area where cross-strip layer is planned to be deposited. After deposition of the targeted overlayer

(passivation material), the wafer is immersed in solvent to remove the photo-resist. Examples of the final test samples produced in these procedures are shown in figure 2.2. Figure 2.2 (b) show the magnified view of the cross-strip regions on the Cu line tested. Tantalum (Ta), tantalum nitride (TaN), titanium nitride (TiN), chromium (Cr), silicon nitride (Si_3N_4), silicon oxide (SiO_2), Cuprous oxide (Cu_2O), and cobalt tungsten phosphide (CoWP) films are used as the passivation layers. Except for Cu_2O and CoWP, all the passivating layers are deposited using sputtering method. The Cu_2O and CoWP layers are formed by electrochemical methods to achieve desired film quality and following sections detail the preparation methods.

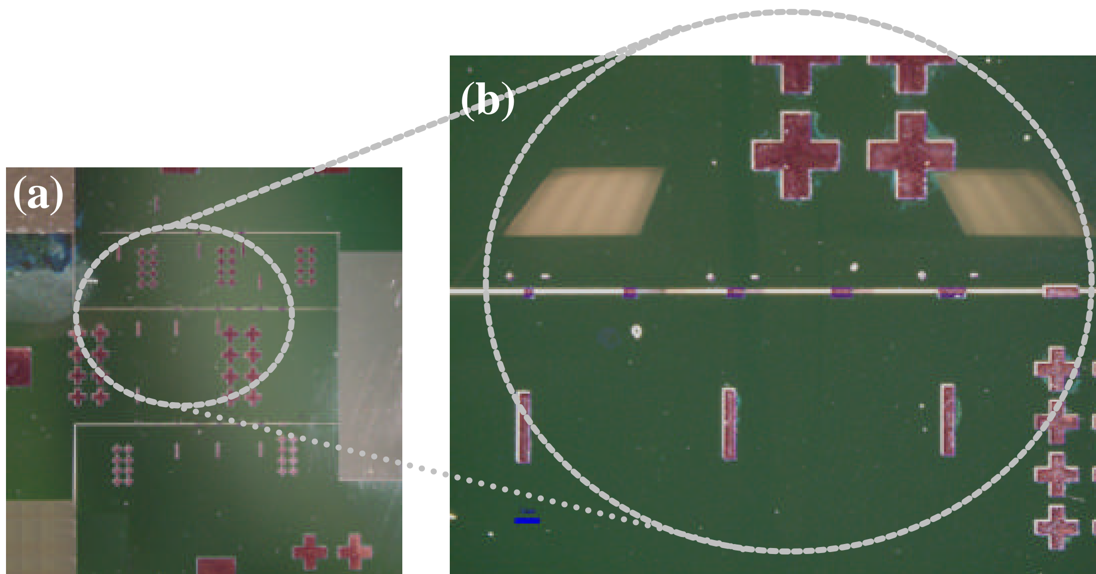


Figure 2.2 Optical microscope images of sample configuration

2.2.2.1 Cuprous oxide (Cu_2O) cross-strip deposition

Cuprous oxide (Cu_2O) cross-strip layer is grown on Cu line by the cathodic reduction of copper (II) lactate solution. The schematic diagram of electrodeposition cell is shown in figure 2.3.

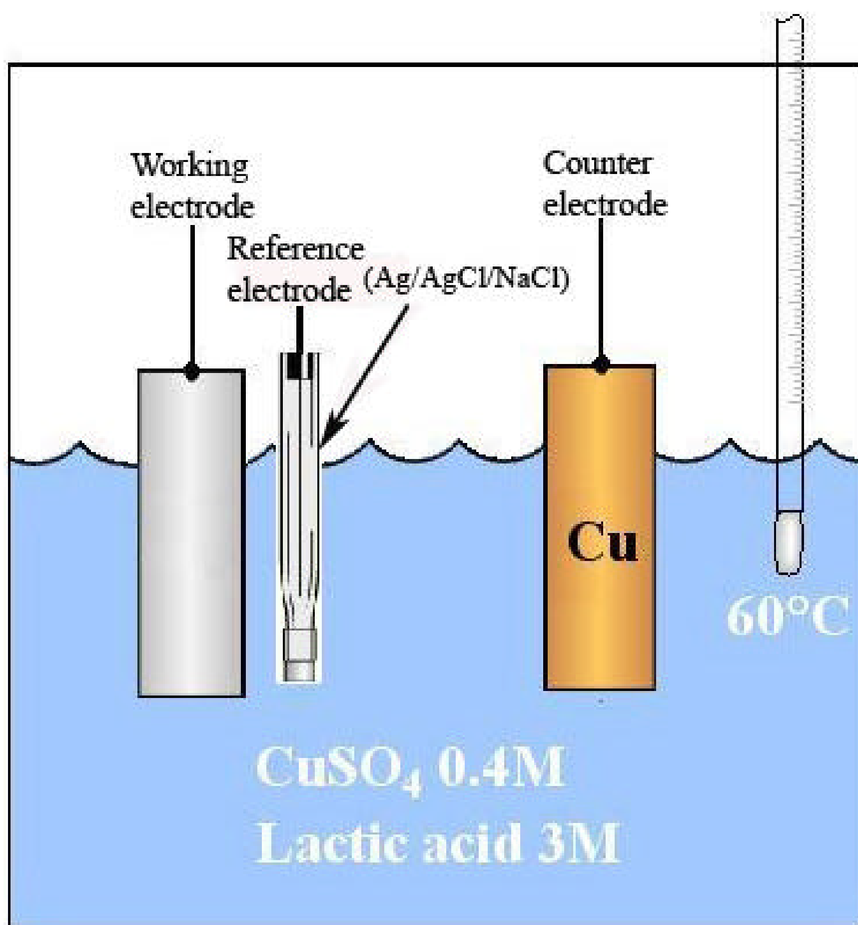


Figure 2.3 The schematic diagram of the electro-deposition cell

The electrolyte consists of 0.4 M cupric sulfate (Fisher Scientific) and 3 M lactic acid (Aldrich). The pH of the bath is adjusted around 9 by the addition of sodium hydroxide [61,62]. The bath temperature is kept at 60°C and applied potential is – 0.4 V (vs SCE). The working electrode, which is used as cathode, is Cu line patterned sample. The anode is a rectangular piece of Cu. The reference electrode was a saturated calomel electrode (SCE). Electrodeposition of cuprous oxide film is carried out in a potentiostatic mode.

2.2.2.2 Cobalt tungsten phosphide cross-strip deposition

Cobalt tungsten phosphide (CoWP) cross-strip layer is grown on Cu line by electroplating deposition method. The plating bath conditions are showed in Table 2.1.

Table 2.1 Bath composition and operating conditions [63]

	CoWP bath (Mol/L)
$CoCl_2 \cdot 6H_2O$	0.1
$NaH_2PO_2 \cdot H_2O$ $Na_3C_6H_5O_7 \cdot H_2O$	0.2 0.3
$Na_2WO_4 \cdot 2H_2O$	0.03
$(CH_3)_2NH \cdot BH_3$	0.02
pH	9.5
pH adjusting agent	KOH

The solution for electroplating CoWP films comprises a source of tungsten ions such as sodium or ammonium tungstate, or phosphotungstic acid; a source of cobalt ions such as cobalt chloride or cobalt sulfate; and complexing agents, reducing agents, surfactants and chemicals used to adjust the pH of the bath solution. As reducing agent, hypophosphate and Dimethyl Amine Borane (DMAB) is used. The pH of this solution can be adjusted by the amount of potassium hydroxide (KOH) added to the bath. The CoWP films used in this study are deposited at the constant current of 1mA and room temperature.

It is known that the amount of cobalt, phosphorous and tungsten in the CoWP films is highly dependent on the applied current density and the pH of the electroplating bath solution [64]. For example, cobalt tungsten phosphide films with less than 1 atomic percent tungsten forms if the pH is less than 6. Increasing the pH of the electroplating bath above 7 result in an increase in the amount of tungsten in the film above 1 atomic percent. In order to check the composition of the film produced in our method, the EDS (Energy Dispersive Spectroscopy) analysis is conducted and the result is shown figure 2.4. It can be seen that Cobalt (Co), tungsten (W), and phosphorous (P) are present in the film. Both Cu and Si peaks come from under layer of Cu line and Si substrate. The EDS analysis shows that the film contains a small amount of W along with residual amount of P.

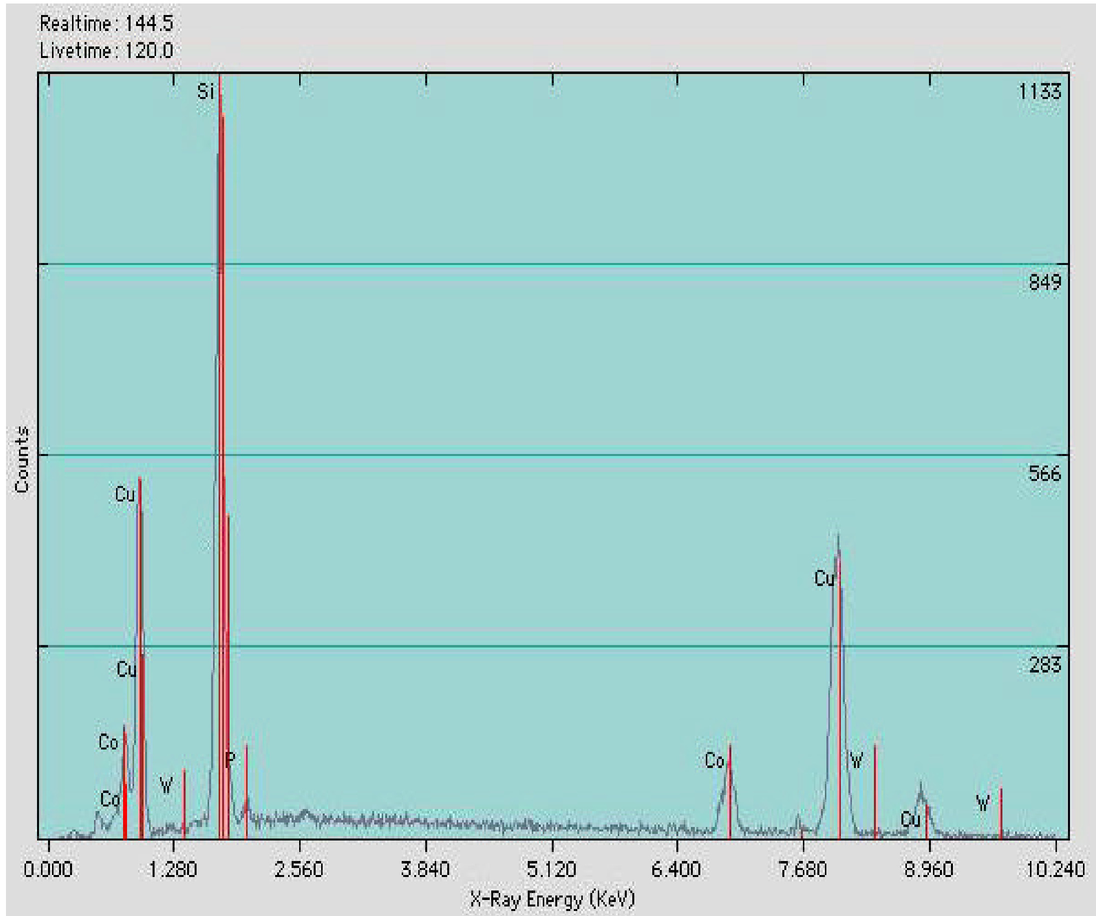


Figure 2.4 The EDS spectra of CoWP on Cu line on Si substrate

2.2.3 Test procedure

Prior to EM testing, all the samples are inspected under SEM to make sure that the testing samples are free of defects at as-prepared condition. The samples are then EM tested in a tube furnace while flowing the forming gas (10%H_2/90%N_2) or argon gas (99.9999%) in order to prevent oxidation of the Cu during testing. A schematic of EM test apparatus is shown in figure 2.5. A sample is placed at a place of the target test temperature and EM tested under a constant current condition. The EM tests is

performed at stress condition of 1~2 MA/cm^2 current density and 170~320℃ ambient temperature.

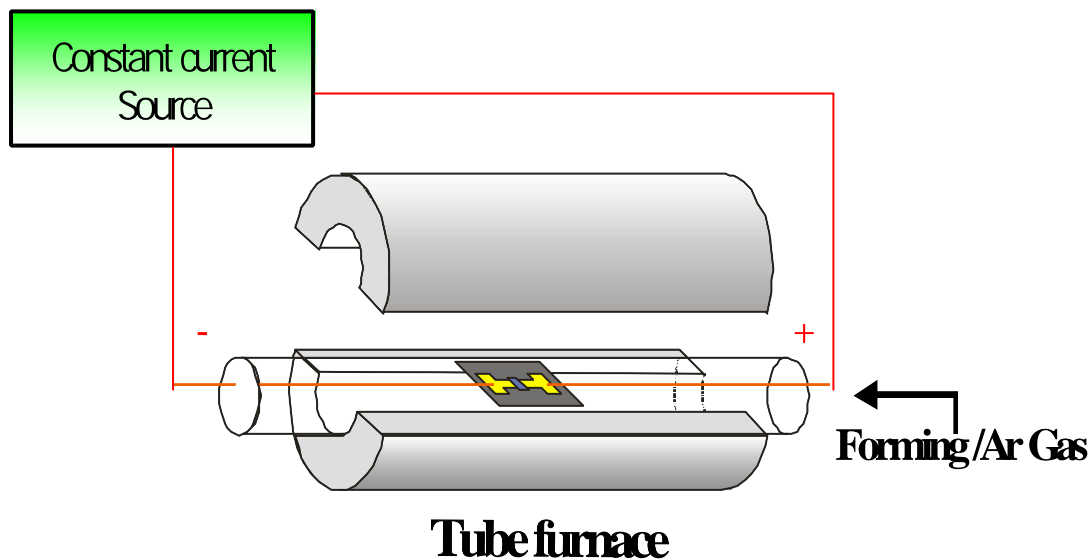


Figure 2.5 A schematic diagram of EM test apparatus

2.2.4 Joule heating

One of important aspects of the EM testing in our configuration is the level of the joule heating because joule heating can offset the temperature from the target test temperature and can cause erroneous results [6,65]. For this reason, the level of joule heating is characterized prior to EM testing. The amount of joule heating present in the sample can be estimated by measuring resistance change as a function of current density. The change in the temperature is reflected in the resistance because the resistance

changes with temperature in proportional to α, the coefficient of thermal resistance of the test structure:

$$R = R_O(1 + \alpha \Delta T) \quad (2.1)$$

The joule heating characterization indicates that the average sample temperature increases to a moderate degree and varies with the thickness of the Cu film. In case of electroplated Cu, which is 1.3um thick, the increase in the line temperature is measured to be 17°C at j=1.0MA/cm^2. On the other hand, sputtered Cu (0.1um thick) shows below 1°C increase at j=1.5MA/cm^2. Figure 2.6 shows the measured values of resistance changes for electroplated Cu line (1.3um) as a function of applying current. In can be seen that the joule heating is minimum in most cases, and therefore it is concluded that the effect can be ignored.

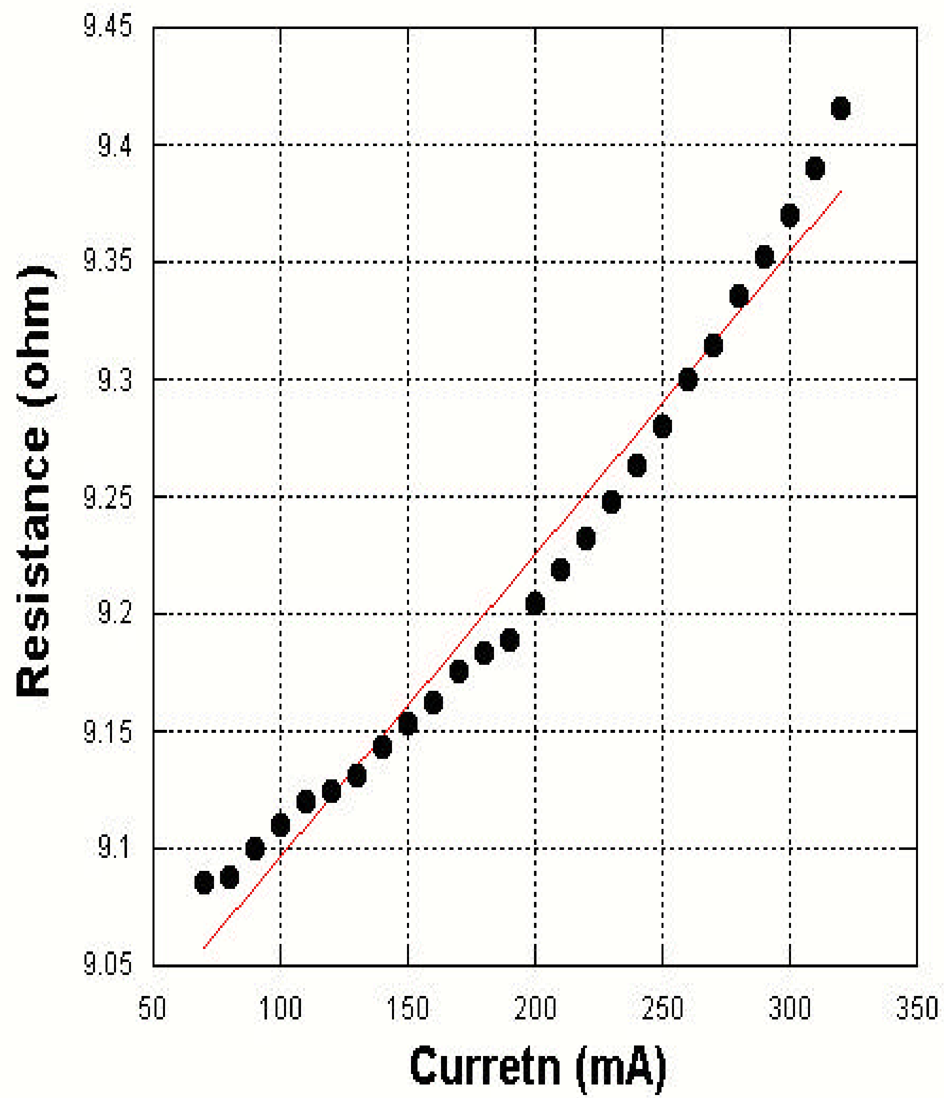


Figure 2.6 Measured values of resistance change for electroplated Cu line

2.3 Results

There are a large number of variables tested with the single cross-strip configuration, and the variables include cross-strip materials, their thickness, test ambient and current density. While some variations exist in detail, all the results show a certain level of consistencies. In order for better understanding of the results we gained in our study, following statements can be provided as a summary:

a) Our experiments present clear evidence that the interface and surface EM is active in Cu. This conclusion is drawn from the observation that the markers (void and pair) do form within reasonable time frame of EM.

b) Regardless of the interface materials, it appears that the EM rate in interface is faster than the free surface EM. This is determined from the observations of the marker formation (void and hillock pair). In all materials tested, the markers form with polarity indicating that the interface EM rate is faster than the surface EM.

c) Our results suggest that Blech effects also play a role in the interface (or surface EM mechanism). It is general trend that the marker formation is more pronounced as the width of the cross-strip increases.

Following sections summaries all the experimental results that lead to these conditions.

2.3.1 Influence of interface materials

2.3.1.1 Tantalum (Ta) cross-strip

Sputtered Cu samples with 30nm Ta over layer cross-strip were EM tested under forming gas ambient. Figure 2.7 is a SEM image of the EM markers taken after 45 hours EM test at T=270°C and j=1.5MA/cm^2. In these images, voids appear as dark contrast due to the lower secondary electron intensity. It can be seen that multiple voids are formed at the upstream edge of the cross-strip while hillocks are formed at the downstream edge of the electron flow.

The markers observed in this experiment are clearly due to the presence of the cross-strip. When other areas of the test line are inspected, there is no apparent evidence of markers forming by EM. Further more, even when the voids or hillocks are found, there are sporadic and not having systematic pair formation. In order to make confirmation that the marker formation seen under SEM is physically correct, the Energy Dispersive Spectroscopy (EDS) is used to determine the amount of Cu in the void and hillock area. Figure 2.8 shows the EDS spectra of void and hillock on the Cu line on Si substrate after 45 hours test; (a) Cu line without void and hillock, (b) void, and (c) hillock, respectively. When EDS spectra of Cu is compared in these areas, there is an intensity variation with the location. It can be seen that the peak intensity is weak in the voiding area and it is strong in the hillock area.

Additional experiment is conducted to further the confirmation. Figure 2.9 shows the cross-sectional view of the voiding area after 24 hour testing at 270°C. These

micrographs are taken after cross-sectioning the local area of interests using focused ion beam (FIB) and titled the sample 54° to expose the cross-sectional area.

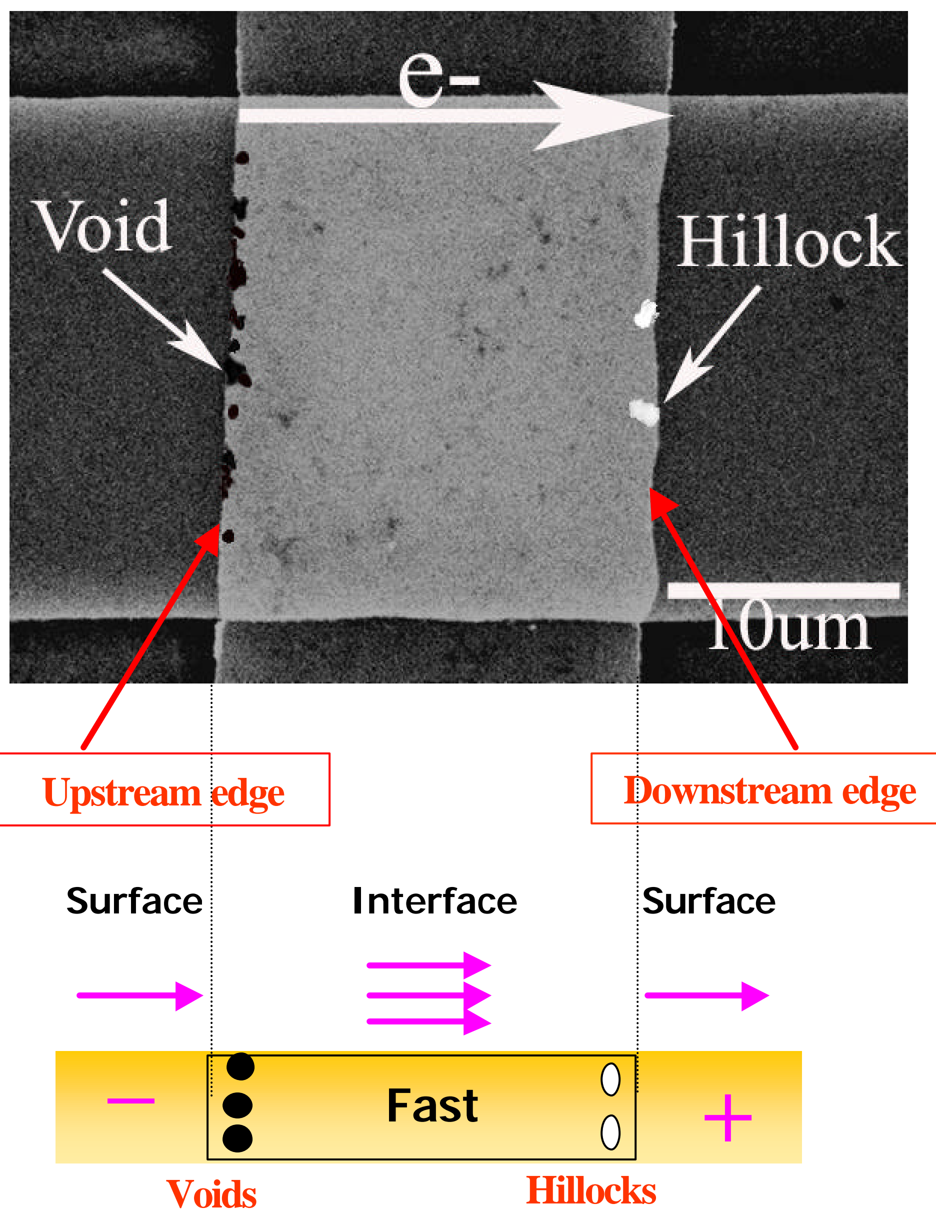


Figure 2.7 The SEM image of Ta cross-strip after 45 hours EM test at 270°C, 1.5MA/cm$^{2;}$ under forming gas ambient

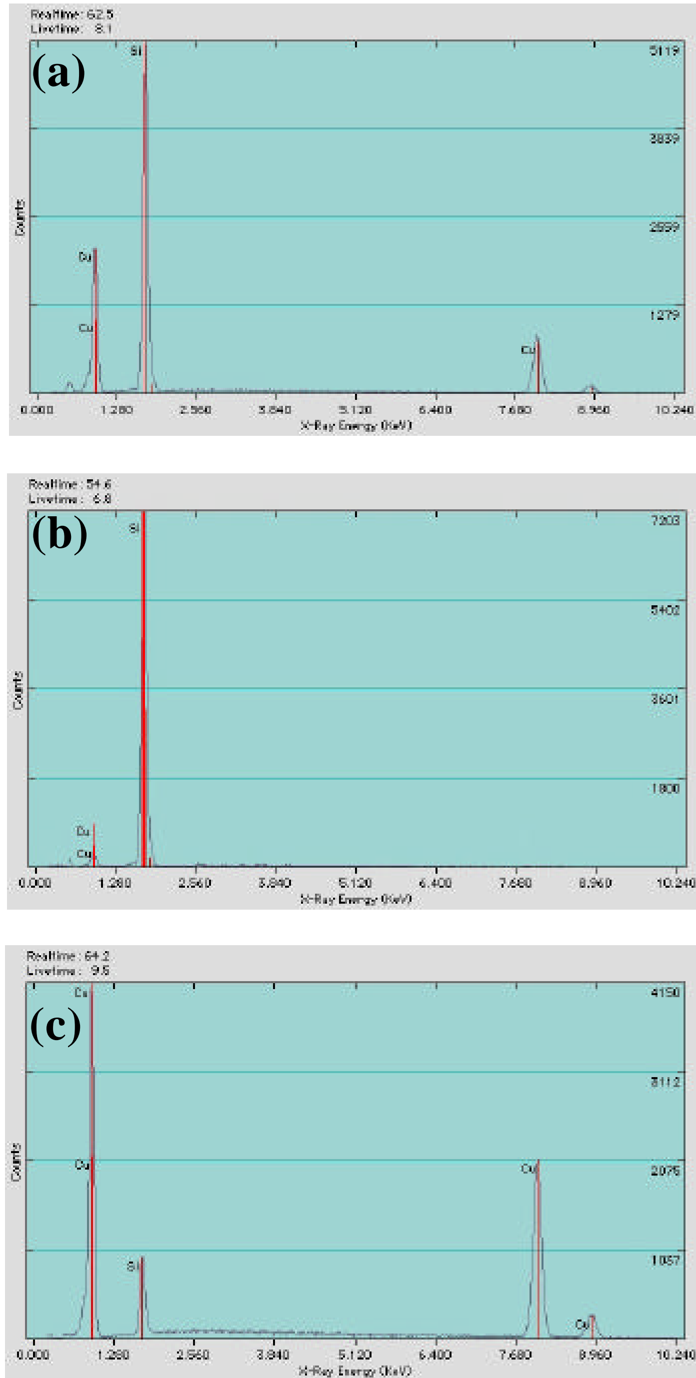
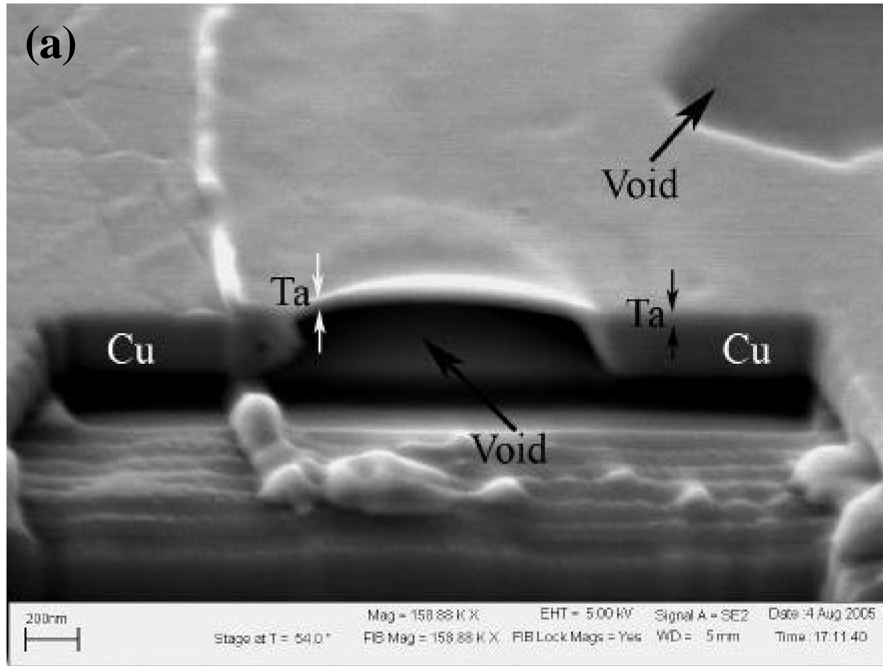


Figure 2.8 The EDS spectra of (a) Cu line, (b) void, and (c) hillock after 45 hours EM test.

It can be seen that the voids at the upstream edge of the strip has a shape suggesting that they are nucleated at the interface between the Ta and Cu line and grow toward the underlying SiO_2 layer. A region of metal accumulation is also shown in figure 2.9 (b). Again, the hillocks appear to form at interface between Ta and Cu. The voids seen under Ta cross-strip in figure 2.9 (a) after 24 hours EM tested were grown too much excessive to allow investigation of the evolution. For this reason, SEM characterization of the sample tested for 8 hours is inspected, and the result is shown in figure 2.10. As marked as an arrow, the voids are not as intense as the ones in 24 hours sample but the presence of voids can be seen. These micrographs present evidences that void formation occurs at the interface between cross-strip/Cu interface and spread through the Cu film. A cross sectional view of another sample presented in figure 2.11 confirms that Cu is removed from the interface between Ta cross-strip and Cu. The polarity of the marker formation found in this experiment indicates that interface EM is very active in Cu thin films. With the given configuration, it is not possible whether the both interface and the surface is active path because the configuration allows us to observe only the flux difference between interface and surface EM. It is possible that one path is inactive and the other is active. However, it is that both are active but one path is more active than the other. The result also suggests that, between the two EM mechanisms, the interface EM is more active than the surface EM. Since Cu EM occurs in the direction of electron flow, the marker polarity indicates that the EM rate is faster at the cross-striped area than the rest of the Cu line.



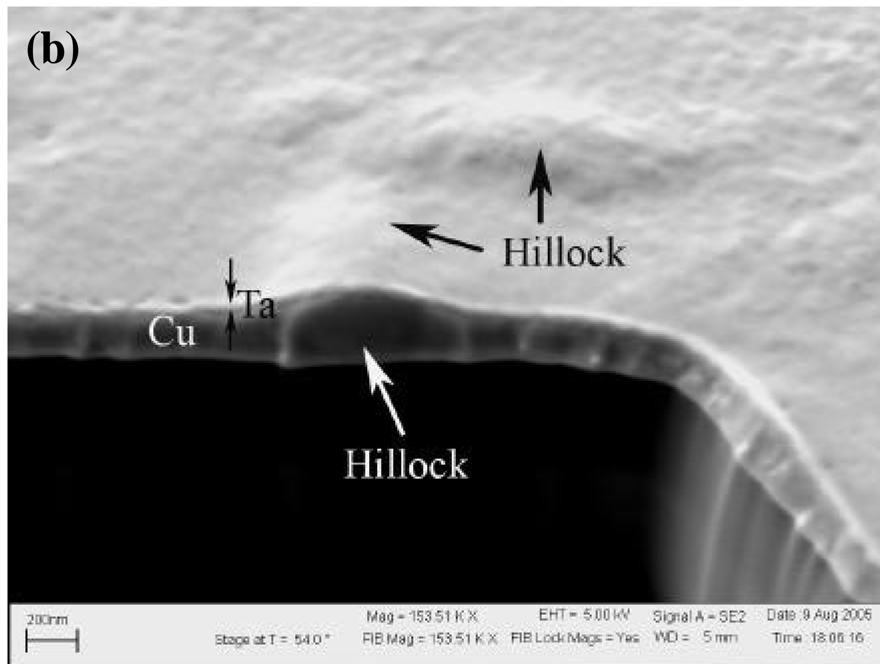


Figure 2.9 The FIB images of Ta after 24 hours EM tested at 270°C, 1.5MA/cm^2 under forming gas ambient; (a) void, and (b) hillock

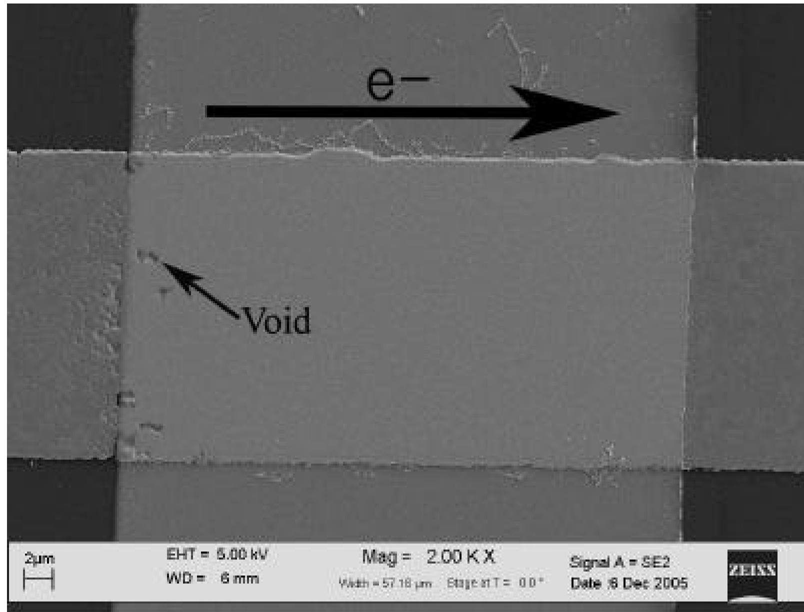


Figure 2.10 The SEM image of Ta cross-strip after 8 hours EM test at 270°C, 1.5MA/cm^2 under forming gas ambient

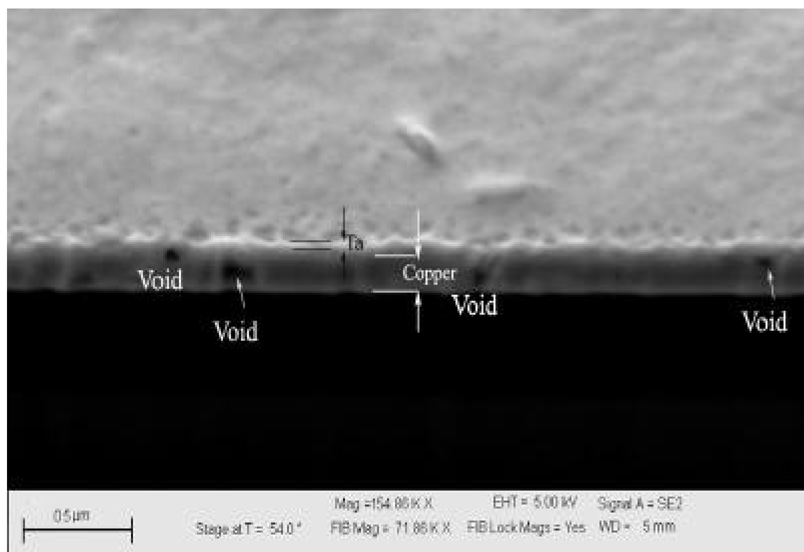


Figure 2.11 The FIB image of Ta cross-strip after 8 hours EM test at 270°C, 1.5MA/cm^2 under forming gas ambient

2.3.1.2 Silicon nitride (Si_3N_4) cross-strip

In case when the sputtered Cu samples 30nm Si_3N_4 cross-strip passivtion is EM tested under forming gas ambient, the markers are also formed with the same polarity as in the case of Ta. SEM micrograph shown in figure 2.12 presents an example of such results. It is seen that multiple voids are formed and aligned at the upstream edge while hillocks are formed at the downstream edge of the cross-strip. Similar to the case of Ta, this result indicates that Si_3N_4 provides easier EM path than the free Cu surface.

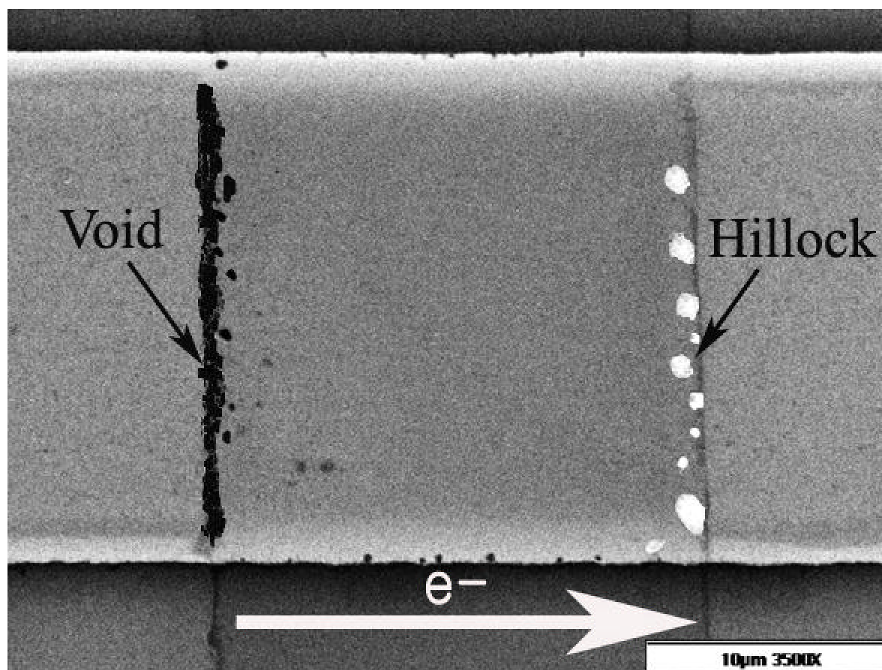


Figure 2.12 The SEM image of Si_3N_4 cross-strip after 45 hours EM test at 270°C, 1.5MA/cm^2 under forming gas ambient

While the marker polarity is similar to the case of Ta, it is noted that the extent of the marker formation seems significantly increased with Si_3N_4 passivation under similar EM testing conditions (current density, temperature, EM time, and cross-strip width). Although qualitative, this result may indicate that the interface EM with Si_3N_4 passivation may be faster than the interface EM with Ta. In fact, this indication is consistent with the several previous studies because those studies finds that dielectric/Cu interface such as Si_3N_4/Cu interface provides faster EM path than Ta/Cu interface [66-70]. Typically, Ta has better adhesion ability to Cu than Si_3N_4, and therefore, Ta/Cu interface may form more ideal interface than Si_3N_4. Studies on the interfacial diffusion activation energy also support this view, that is, that the stronger adhesion suppresses the interfacial EM because they find that the diffusion activation energy depends highly on bonding nature of the interfaces [67-71].

2.3.1.3 Tantalum nitride (TaN) cross-strip

EM test results of TaN cross-strip are shown in figure 2.13. The same polarity of marker formation, voids and hillocks, is also seen in samples with TaN cross-strip samples. Voids are formed at the upstream edge and hillocks are formed at the downstream edge of the cross-strip. Similar to other interfaces, this indicates that the TaN/Cu interface provides the faster EM paths than Cu surface. However, a minor difference is noted. It is found that void and hillock formation with TaN passivation is not confined within a strip area but extended to outside the strip.

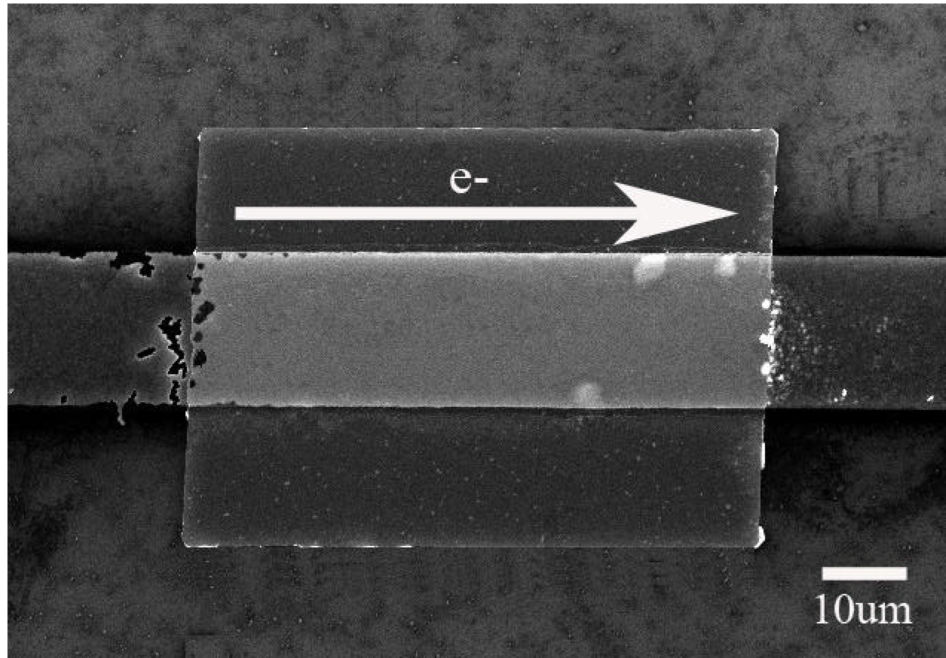


Figure 2.13 The SEM image of TaN cross-strip after 45 hours EM test at 270°C, 1.5MA/cm^{2} under forming gas ambient

2.3.1.4 Titanium nitride (TiN) cross-strip

EM test results of 30nm thick TiN passivation after 45 hours EM test are shown in figure 2.14. Similar to other interface materials, voids are found to form within the cross-strip area of the upstream edge and hillocks form on the downstream edge, indicating that the EM rate of Cu is higher in TiN/Cu interface than in the Cu surface. However, void formation is less extensive and more dispersed than the cases of Si_3N_4 and Ta.

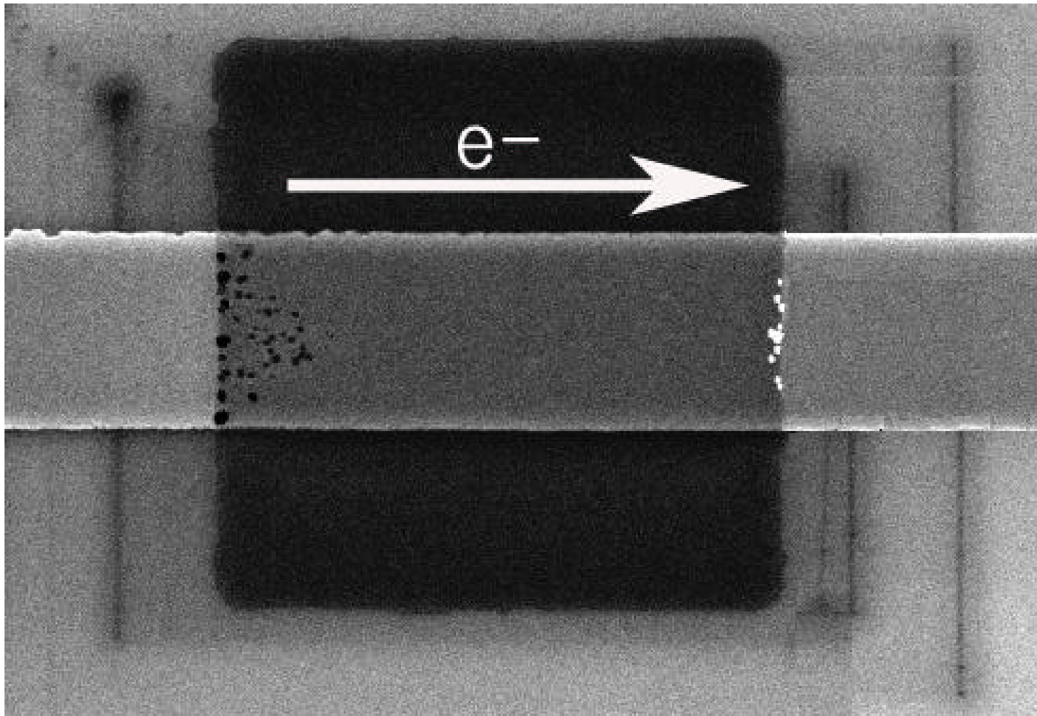


Figure 2.14 The SEM image of TiN cross-strip after 45 hours EM test at 270°C, 1.5MA/cm^2 under forming gas ambient

2.3.1.5 Chromium (Cr) cross-strip

Figure 2.15 shows marker formation for a cross-strip of Cr after 24 hours EM test. In general, polarity of marker formation is the same as those in the other single cross-stripped passivation results. Voids form at the upstream edge and hillocks form at the downstream edge of cross-strip. This result indicates that EM rate along Cr/Cu interface is higher than along free surface of Cu. However, unlike Si_3N_4 and Ta passivation, void formation is not concentrated along the upstream edge of cross-strip but is more dispersed. Such a dispersed marker formation may be a result of the active diffusion. When the diffusion rate is low, the voids and hillocks should form without

possibility being diffused away from the flux divergence points. If the diffusion rate is high, diffusion would disperse vacancies and excessive atoms before nucleating voids and hillocks, resulting in the dispersed formation of the markers.

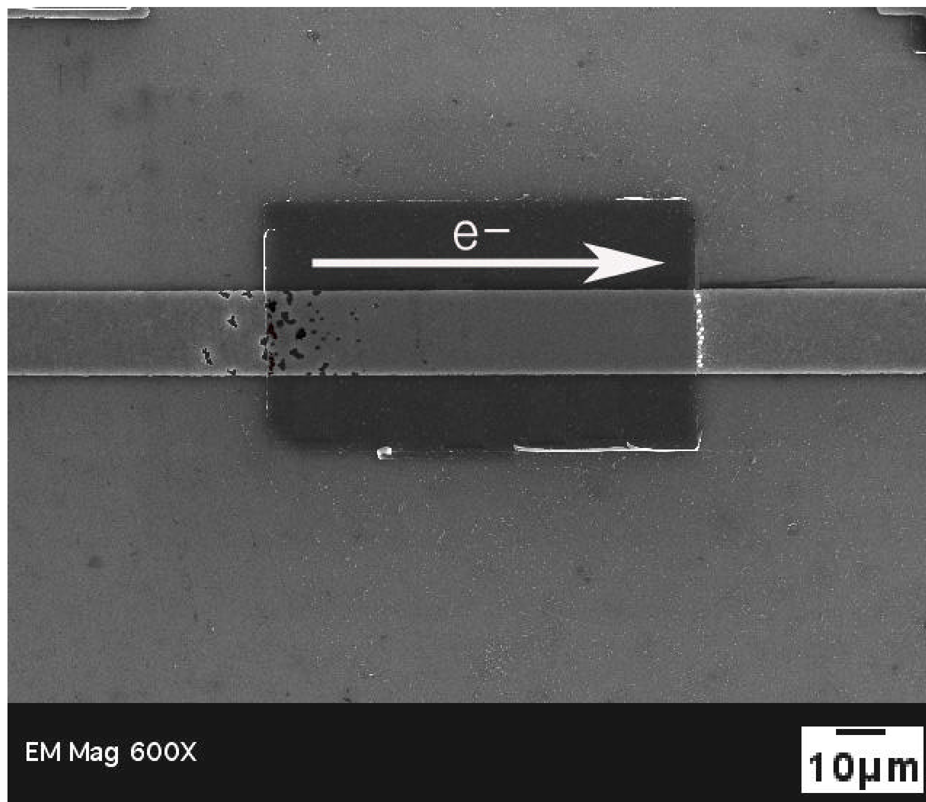


Figure 2.15 The SEM image of Cr cross-strip after 24 hours EM test at 270°C, 1.5MA/cm^2 under forming gas ambient

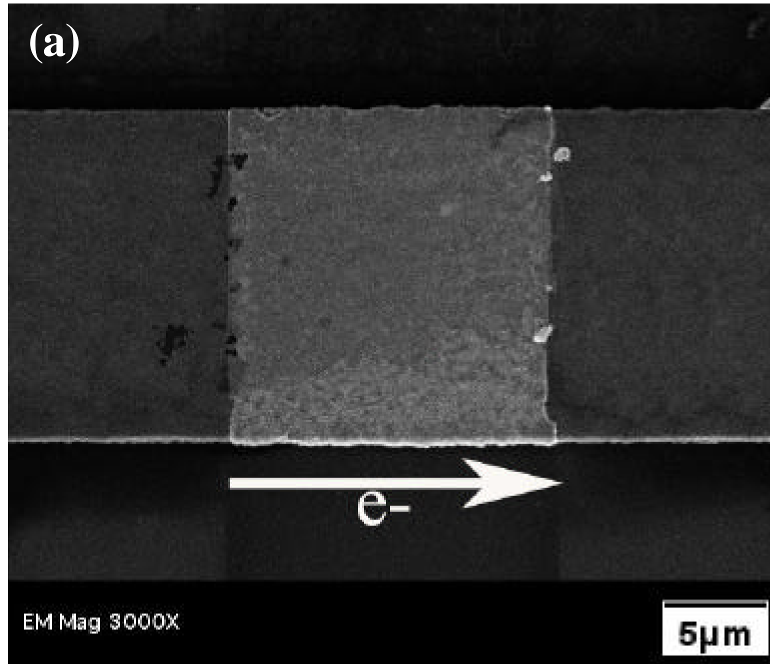
Such a view may be suffered by the observation that the area of marker formation is not confined to but extended to the outside the cross-stripped area. This is similar to the case of TaN passivation EM.

It is important to rote here that the current configuration measures the EM rate difference not diffusion rate difference. It is true that the diffusion and EM is

interrelated. However, it should be noted that the EM rate is not only affected by diffusion rate but also affected by the effective valance of the EM driving force. In case when the interface is with high diffusion rate and the effective valence, the marker formation should be extensive and also dispersed. On the other hand, when the interface is with high effective valence but the diffusion rate is slow, the markers should form in a confined space. We believe that the Cr belongs to the former case and TaN belongs to the latter case.

2.3.1.6 Cobalt tungsten phosphide (CoWP) cross-strip

In our study, the interface created by CoWP is also tested. The main reason for including this interface is because CoWP is currently being considered as one of capping materials for Cu interconnects. Recently, CoWP metal cap is considered as a potential material that can replace the dielectric cap. With metallic capping layer, it is possible to increase the conductivity of the Cu interconnects, and this reduce the RC. It is also argued that the CoWP capping layer would improve the Cu EM performance. In fact, surface coating of Cu interconnects by electroless CoWP is found to significantly improve EM lifetime by providing protection against interface diffusion of Cu [67,70-79]. Our single cross-strip EM test with CoWP passivation reveals that the fundamental EM behavior with CoWP is similar to other passivation materials. Figure 2.16 shows the marker formation after 45 hours EM test under forming gas ambient; (a) for 20um, and (b) 80um cross-strip lengths, respectively.



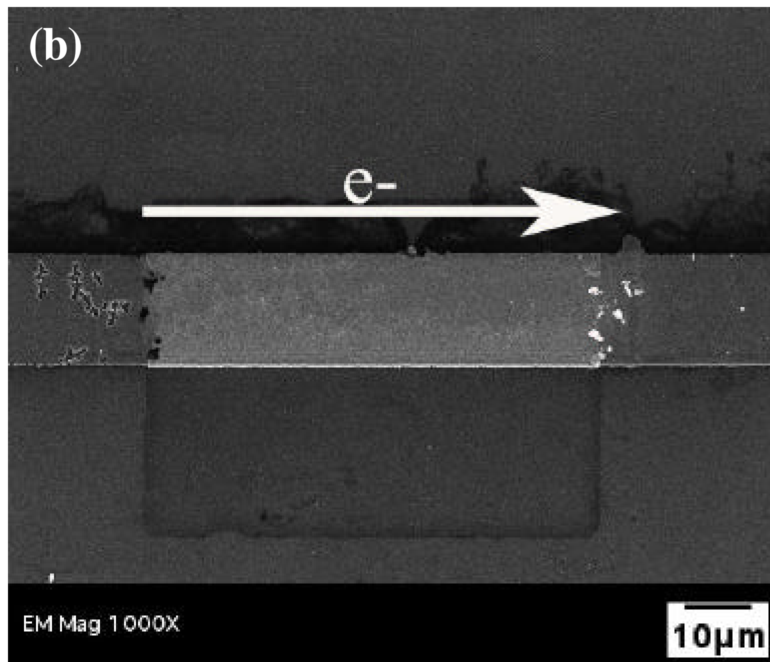


Figure 2.16 The SEM images of CoWP cross-strip after 45 hours EM test at 270°C, 1.5MA/cm^2 under forming gas ambient; (a)20um, and (b) 80um cross-strip lengths, respectively.

Note that voids form at the upstream edge and hillocks form at the downstream edge of cross-strip. This indicates that the CoWP passivtion also creates an interface where EM is faster than in surface. However, the location of void and hillock formation is slightly different from Ta cross-strip samples; some voids and hillocks form away from the cross-strip. With the given result, it is difficult to conclude whether CoWP would be a good interface material or not. However, within the given resolution of our experiment, it can be conclude that the CoWP passivation would provide similar interface similar to other metallic materials like Ta and TiN.

2.3.2 Blech effect and Interface EM

The results of the single cross-strip indicate that the interface EM is active in interfaces created by all passivation materials tested in our study. Although such a conclusion is clearly supported by many observations, it is not clear how interface EM proceeds in the given configuration. As discussed in the background, one of the most significant aspects of EM is the presence of EM induced backflow, namely Blech effect. The Blech effect is a result of EM interacting with vacancy creation and destruction process in a confined space [52,53]. The passivation could produce effect of confining the test line used in our study and may influence the EM rate. In this regards, the EM rate can be affected by a) varying thickness of the passivation layer (in a given length of the strip) and b) varying length of the passivation layer (in a given thickness of the strip).

Our study finds that the interface EM rate is affected greatly by the Blech effect. When the kinetics of marker formation is compared with varying thickness of the

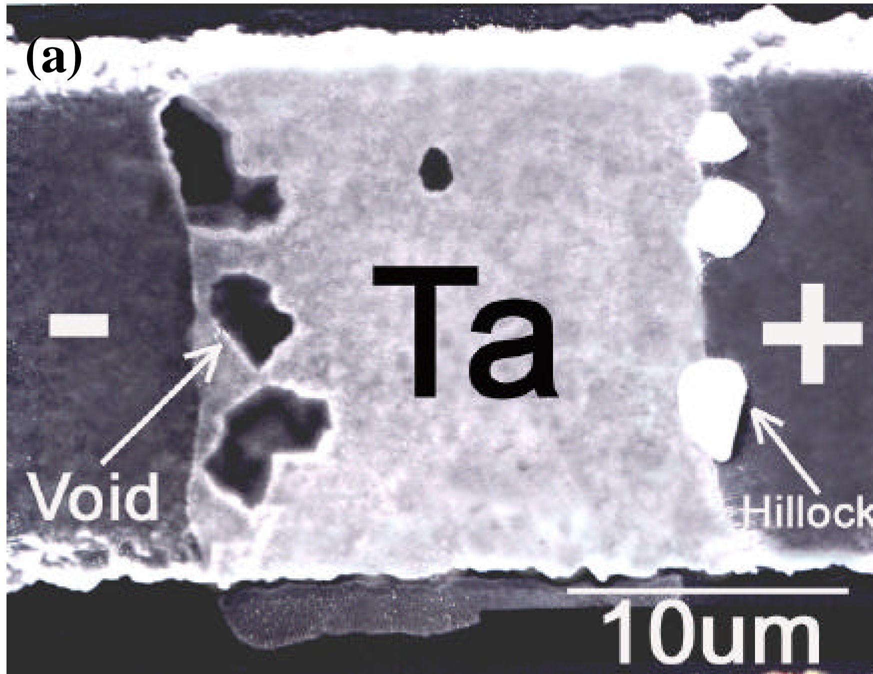
passivation layer, it is found that the EM rate increases with decreasing the thickness of the cross-strip layer. Similarly, the EM rate decreases with decreasing the cross-strip length. Both results are consistent with the conventional EM theories and following sections detail our observations.

2.3.2.1 Effect of the passivation layer thickness

It is our consistent observation that the thicker passivation suppresses the marker formation. For this study, we use electroplated Cu as base Cu line and Ta as the passivation material. Figure 2.17 shows the variation of void formation with varying thickness of Ta cross-strips after EM testing of samples under similar testing conditions. It can be seen that the polarity of the marker formation is the same regardless of the thickness, but the marker formation is significantly less in lines with thicker Ta layer (60nm). In thicker passivation, voids are faintly visible and hillocks are almost invisible.

2.3.2.2 Cross-strip length effect on Cu EM

The study on the length effect also supports the presence of the Blech effect. In this study, the effect of cross-strip length on marker formation (void and hillock formation) is investigated using structures based on the basic structures but with varying cross-strip length. Structures with cross-strip lengths of 20, 40, 60, 80, 100, 120, 160, and 300 *um* were used. All of the structures are based on a 20 *um* wide test structure. Figure 2.18 shows the basic layout of the test structure with Si_3N_4 as passivation layer.



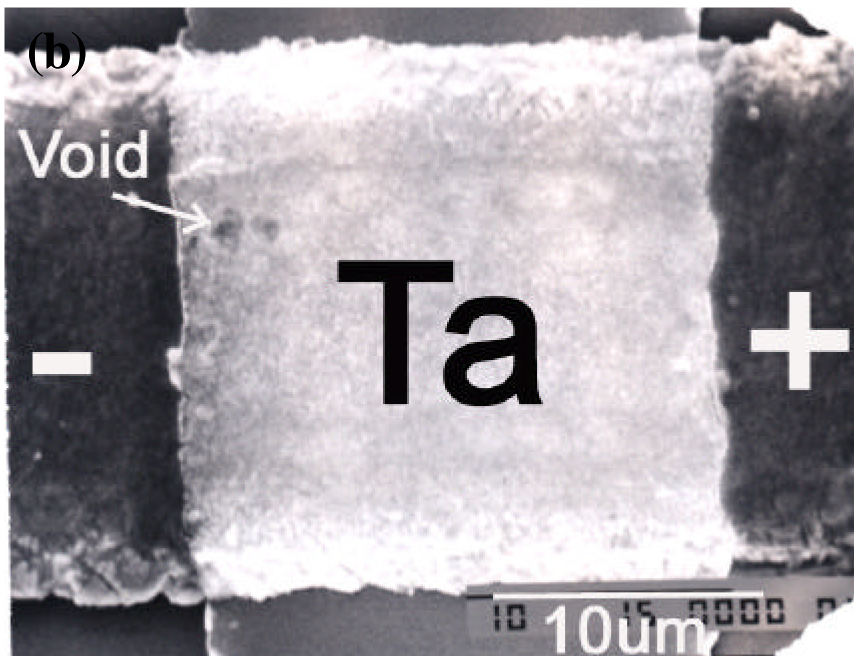


Figure 2.17 SEM images of Ta cross-strip tested at 270°C, 1.0MA/cm^2; (a) 30nm after 44 hours test, and (b) 60nm after 48 hours test.

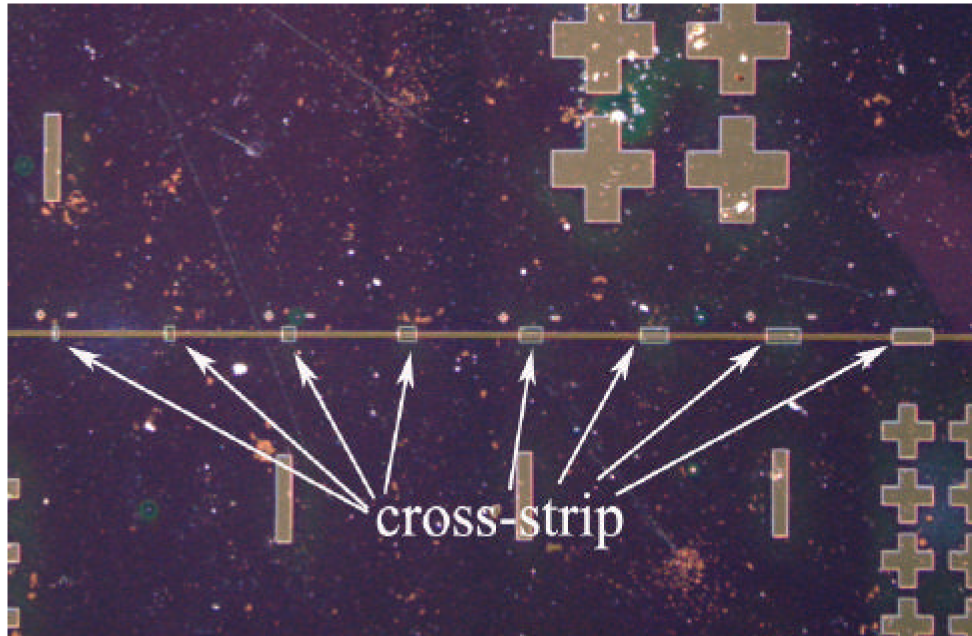


Figure 2.18 The basic layout of test structure; different cross-strip lengths

A series of SEM micrographs shown in figure 2.19 shows the length effect. Figure 2.19 shows the marker formation after 36 hrs at 270°C and 1.5 MA/cm² in Cu lines with 30nm thick Ta cross strips of different length. As can be seen in SEM images, as cross-strip length increases, the magnitude of void and hillock formations increases. Note that void and hillock formation is almost completely suppressed in 20um length strip, while markers are clearly visible in longer strips. Since the backflow force inversely scales with the strip length, the kinetics of marker formation is likely to be reduced in shorter strips. The micrographs shown in these figures support such a mechanism.

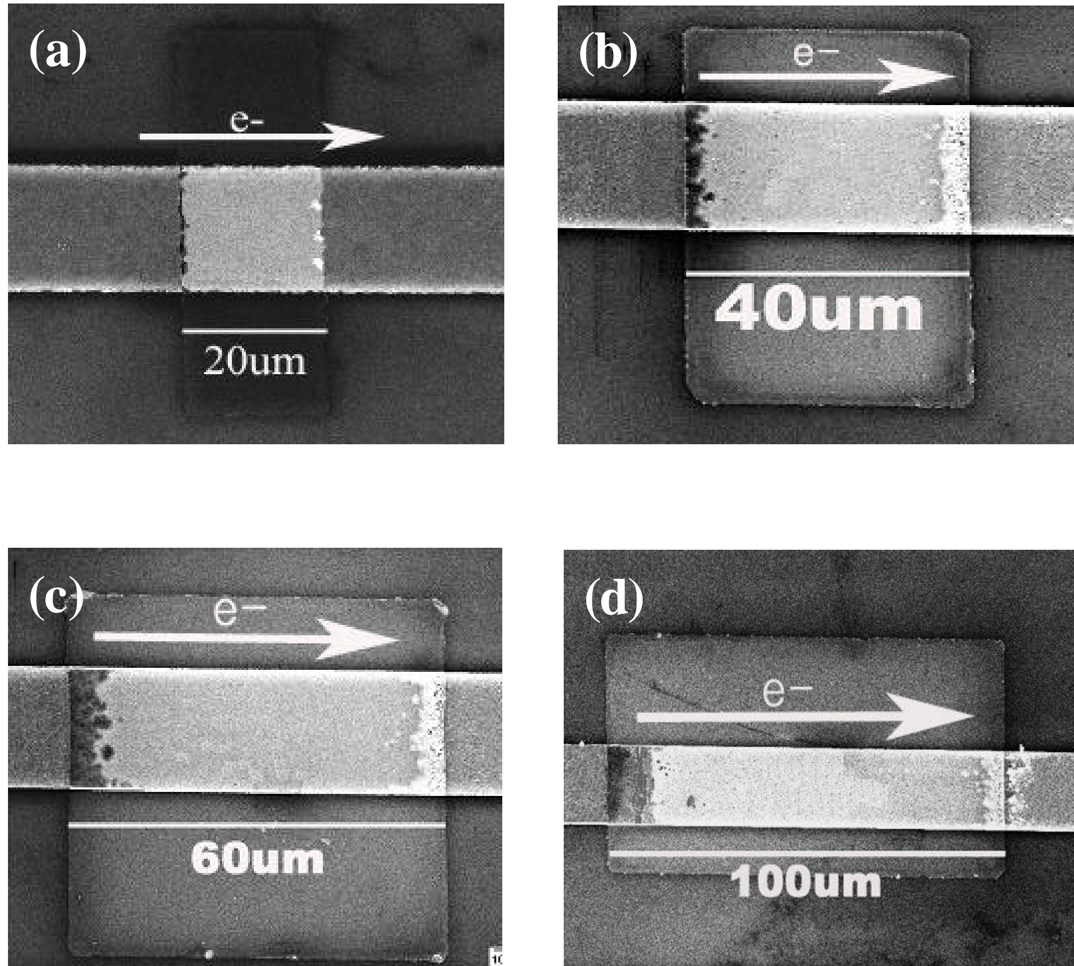


Figure 2.19 The SEM images of Si_3N_4 cross-strip tested at 270°C, 1.0MA/cm^2; (a) 20um, (b) 40um, (c) 60um, and (d) 100um after 36 hours test.

2.4 Discussion

2.4.1 Surface and microstructure of the test pattern

The testing with cross-strip configuration reveals that the method itself is very useful in studying the interface and surface EM mechanism. In particular, since the micro-structural feature of the stripped and unstripped area is the same, the resulting

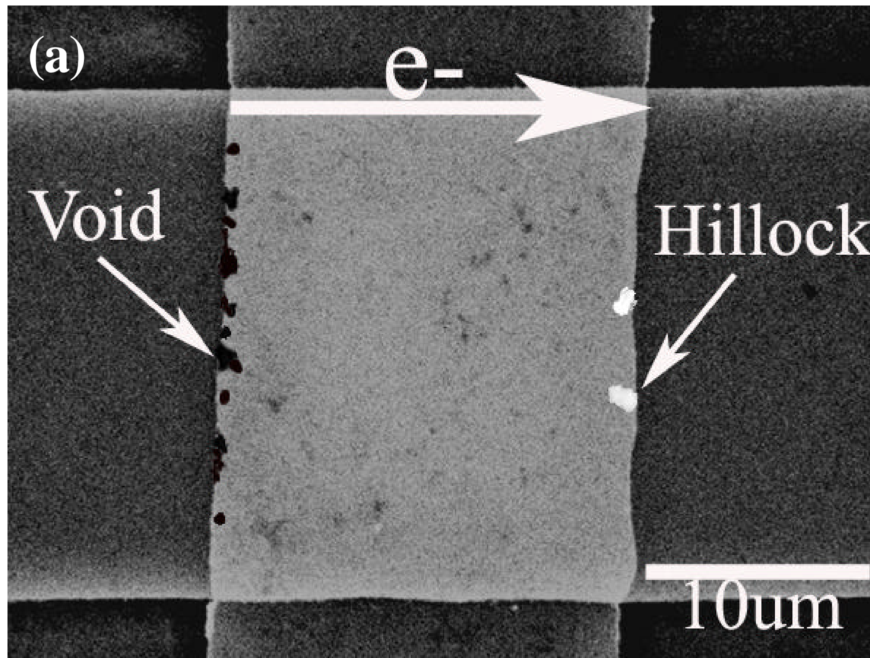
marker formation is direct evidence supporting the active EM along the surface and interface. What is surprising, though, is the fact that the marker polarity does seem to indicate that the surface EM rate is far smaller than the interface EM rate. Regardless of passivation materials tested, the results show consistency that the markers form with the polarity indicating that surface EM is slower than the interface EM. This is somewhat unexpected result because it is common belief that surface diffusion is faster than the interface diffusion. Since EM kinetics is governed primarily by the diffusion [12-21], it is natural to assume that the surface EM would show slower kinetics than the interface EM. Among many possibilities, the first to suspect is some type of artifacts in our test method. For this reason, we carry out additional tests and try to confirm that the results we have reflect the true physics.

There are several possible sources that may cause the EM rate either at surface or at interface. The first may be related to the testing environment. In our testing, forming gas is used to prevent the oxidation of Cu surface. Containing H_2, the forming may passivate the Cu surface and thus reduce surface diffusion rate [80]. The second possibility is that the surface may be covered with a thin layer of Cu oxide. With Cu oxide on Cu surface, the tested surface EM may not be true surface EM but may be interface EM between Cu/Cu oxide. Thirdly, difference in the film stress condition may result in the interface EM to be faster than the surface EM. Consideration on the stress condition may be necessary to validate our result. Finally, it may be possible that the grain structure underneath the stripped area and free surface is changed. If the grains in free surface evolve in such a manner to produce highly textured grains while the

stripped area does not, the surface EM kinetics may be substantially reduced compared to otherwise [24,57,59]. It is a remote possibility because the microstructure of Cu is stabilized before patterning of the test line s, but needs to investigate for confirmation. We examined these possibilities as detailed below.

2.4.1.1 Ta cross-strip under Ar ambient

In order to examine the possibility that H_2 passivation of Cu surface reduces the surface EM, the samples with Ta cross-strip are tested under two different ambient and the results are compared. The first ambient is the forming gas and the second ambient is argon (Ar) gas. This test is needed because it is known that Cu surface saturated with hydrogen shows slower diffusion kinetics because hydrogen interacts strongly with defects and lowering defect concentration in Cu surface [80]. Strong passivation by hydrogen may suppresses the surface diffusion to an extent to reduce the EM rate lower than a normal interface. Such an effect may reverse the polarity of the markers. Figure 2.20 shows the void and hillock formation at the Ta cross-strip after 48 hours EM test under Ar gas ambient.



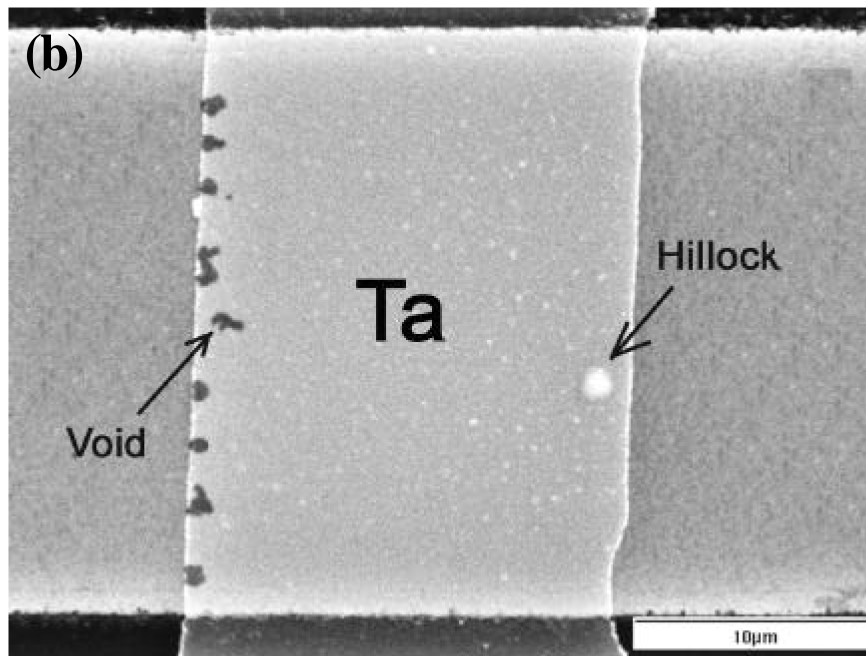


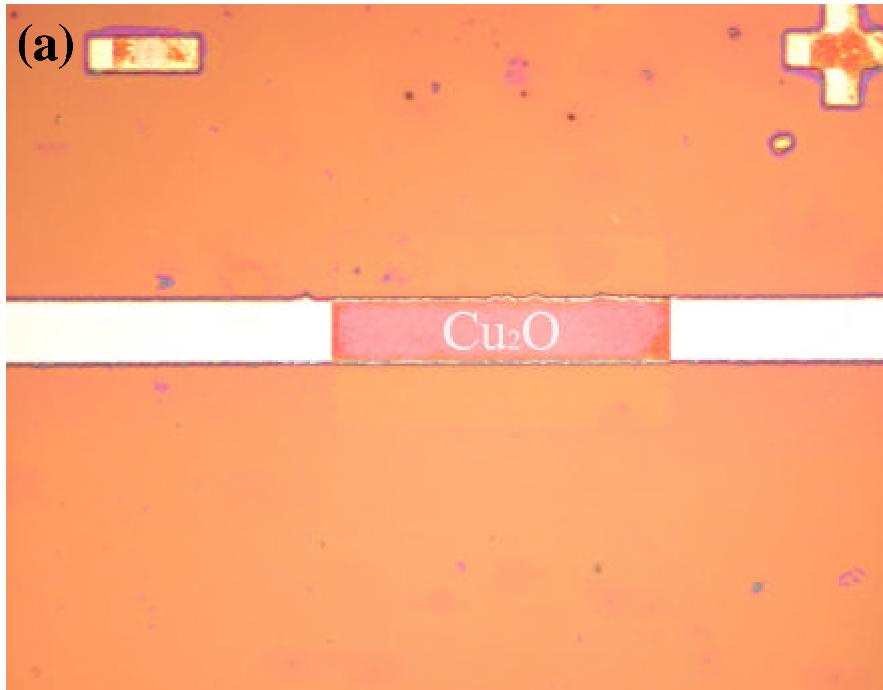
Figure 2.20 The SEM images of Ta cross-strip tested at 270°C, 1.5MA/cm^2 (a) forming gas and (b) Ar gas ambient

When the result is compare to SEM micrographs shown in (figure 2.20), it is seen that the marker polarity is not changed from the testing under forming gas environment. The voids form at the upstream edge and hillocks form at the downstream edge of cross-strip. We cannot detect a significant difference between the two results under different ambient. However, void and hillock formations within Ta cross-strip for Ar gas ambient seem to be retarded. This result is consistent with previous reports that hydrogen slows diffusion kinetics of a Cu surface [80].

However, the results clearly indicate that hydrogen passivation is not sufficient to make surface EM to be slower than the interface EM.

2.4.1.2 Cu_2O cross-strip test

Another possibility of the Cu surface chemistry affecting EM rate is the oxidation. During sample preparation processes, the Cu surface is exposed to ambient. It is possible that the Cu surface is slightly oxidized during such an exposure and remained during EM testing. For this, EM test patterns with Cu_2O cross-strip are made in our study and make them to be subjected to EM testing under forming gas environment. Figure 2.21 shows the optical microscope images of Cu_2O cross-strip; (a) before test, and (b) after 24 hours test at $270^{O}C$, $1.5MA/cm^2$ under forming gas ambient. It can be seen that cross-stripped Cu_2O layer was reduced by hydrogen contained forming gas after 24 hours EM test at $270^{o}C$.



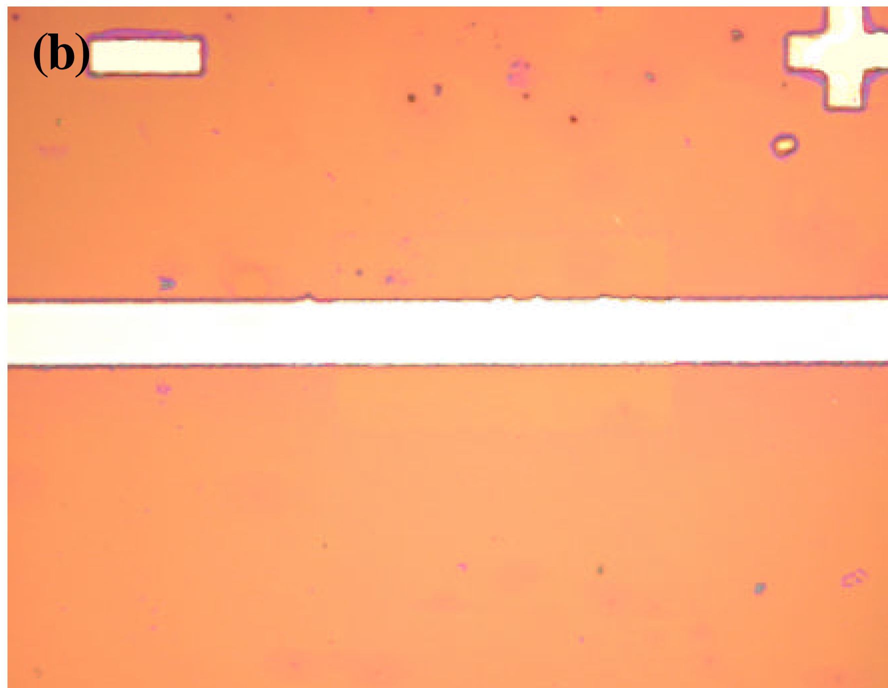


Figure 2.21 The optical microscope images of Cu_2O cross-strip; (a) before test, and (b) after 24 hours EM tested at (b) 270°C, $1.5MA/cm^2$ under forming gas ambient.

This result indicates that the Cu oxide, even if it is present before EM testing, would be removed from the Cu surface during EM testing and does not affect EM rate at Cu surface.

2.4.1.3 Consideration on film stress

As is well known in the field of diffusion, the diffusion rate is affected greatly by stress. Difference in stress state in the passivated and unpassivated line may produce effect such that the surface EM rate is reduced below interface EM rate. In this regard, it is necessary to consider how diffusion rate is affected by stress and what type of stress should develop in the test structure used in this study.

The atomic and vacancy diffusivity are function of stress largely because the vacancy concentration and the lattice density are function of stress. Atomic diffusivity and vacancy diffusivity are related [81]:

$$D_a = D_v \frac{C_v}{C_a} \tag{2.2}$$

where D_a and D_v are the atomic and vacancy diffusivities respectively; C_a and C_v are the atomic and vacancy concentration respectively. It has been shown that equation 2.3 represents an approximate analysis of the stress evolution.

$$D = D_{0s} \exp(\frac{\Omega \sigma}{k_B T}) \tag{2.3}$$

where D and D_{0s} are the values of diffusivity with and without stress, Ω is atomic volume, and σ is the hydrostatic stress of the metal conductor under test. The value of D scales with temperature such that

$$D_{os} = D_O \exp(-\frac{E_a}{k_B T}) \quad (2.4)$$

where E_a is the activation energy for diffusion and both D_o and E_a depend on the materials and on the diffusion path in a given material.

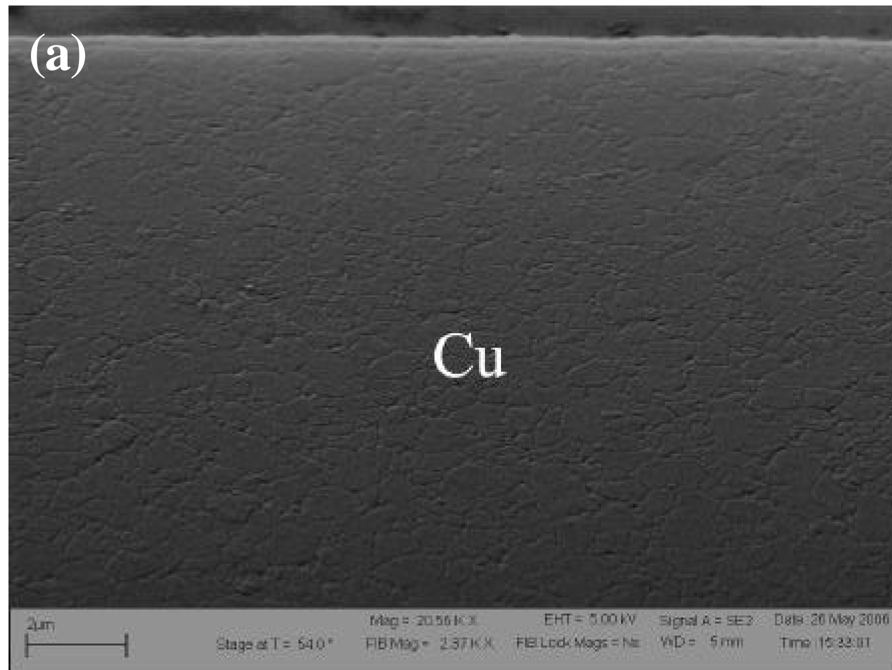
The relation predicts a higher diffusivity for thin film under tensile stress and lower diffusivity under compressive stress [81-83]. Therefore, when everything else is the same, EM rate in the area under tensile stress is higher than the area under compressive stress. However, this cannot explain the result of this study. Since the passivating materials are with lower thermal expansion than the Cu, the area with passivation layer is likely to be under compressive stress. In such a case, the interface EM rate should be suppressed and may produce markers with the opposite polarity to what is seen here. Furthermore, if any stress exists in the test line due to thermal mismatch, it should be quickly relaxed during EM testing. Therefore, it is unlikely that the stress is the factor causing the result of slower surface EM rate.

2.4.1.4 Comparison of grain structure

The microstructure of Cu can also be an important factor in determining the Cu transport mechanism [63]. Variations of the local microstructure of Cu can change diffusivity of Cu. In particular, if the passivated and unpassivated area develops different grain texture, the surface EM rate may be sufficiently changed to make it to be slower than the interface EM rate. This is very unlikely because a) the grain structure of the test line is stabilized prior to pattern production and b) studies on Cu surface

diffusion using a single crystal Cu indicates that the surface diffusion is still sizable in any orientation. Such belief is found to be correct in our study.

After EM test for Ta cross-strip sample, Ta cross-strip layer is removed by focused ion beam (FIB). Figure 2.22 shows SEM images of microstructure of Cu after EM test; (a) microstructure of Cu at free surface region (outside of cross-strip) and (b) microstructure of Cu at cross-strip region after removing Ta cross-strip, respectively. The grain structures between the two areas are not much difference, as expected. Therefore, it is concluded that the observation of slow surface EM rate than the interface EM must have a generic origin.



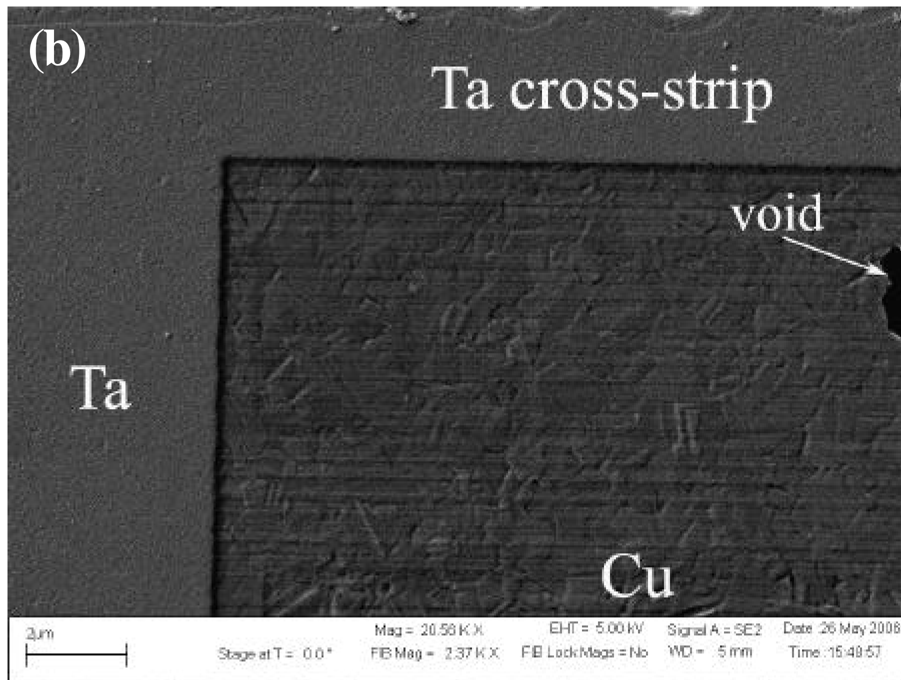


Figure 2.22 The microstructure of Cu after EM test; (a) free Cu surface region, and (b) cross-strip region

2.4.2 Mechanism of the marker formation

Our cross-strip test shows the marker formation. This result presents undisputable evidence for active interface/surface EM in Cu interconnects. The presence of cross-strip layer changes the EM mechanism from that in surface, producing flux divergence sufficient to create the voids and hillocks. The void and hillock formations occur whenever there is an imbalance of Cu fluxes at the interface between cross-strip and Cu surface. The flux divergence is given as [69] ;

$$-\frac{\partial n}{\partial t} = \frac{J_{out} - J_{in}}{\Delta x} \tag{2.5}$$

where J_{in} and J_{out} represent the Cu flux entering and leaving at that location. When the flux divergence is positive, namely, i.e. more atoms flowing out than moving in, mass depletion occurs by collecting vacancies. When the vacancy concentration exceeds the critical concentration, nucleation of void becomes possible. On the other hand, when the flux divergence is negative, vacancies are destroyed by accumulation of atoms, resulting in the formation of hillocks formation.

In a cross-strip configuration, the flux divergence is created by the EM flux difference between the interface and surface, that is

$$-\frac{\partial n}{\partial t} = \frac{J_{\text{int}} - J_{s}}{\Delta x} \tag{2.6}$$

where J_{int} and J_s represent the EM flux of interface and surface, respectively. From the marker formation polarity, it is concluded that the J_{int} is greater than J_s. This promotes the formation of voids at the down stream edge and hillocks at the upstream edge of the cross-strip. As discussed above, the slower EM rate in surface than in interface is

somewhat unexpected result but is believed to have a generic origin. This finding deserves further discussion and is discussed further in later sections. At the present moment, there is another mechanism that needs some attention, that is that the change in the location of the marker. It is found that the markers sometimes form within the cross-strip area but sometimes outside of the strip area.

In an ideal case, the markers should form at the boundaries between the strip and free surface but within the cross-strip area because they are the points of maximum flux divergence. However, the fact that the markers often form outside of the strip means that there is a mechanism promoting marker formation outside of the cross-strip. It is our belief that interplay between the vacancy accumulation/depletion and diffusion is responsible such variations. From the nucleation point of view, the interface is less favored place because it is the confined space with low surface energy than the free surface. For hillocks, physical confinement should certainly suppress their formation, making free surface more favorable. For voids, a similar mechanism should be in operation. Voiding is a process of creating free surface. Making additional free surface should be easier in free surface than in a place where surface is passivated. For these reasons, the nucleation prefers the formation of markers outside of the cross-strip. However, in order to form markers at outside of the cross-strip, it requires diffusion. Unless marker formation within the stripped area is sufficiently suppressed to allow diffusion of vacancies or excess atoms to outside of the cross-strip, markers wouldn't form at those places. It is therefore, conceivable that the location of the marker formation is determined by the relative rate of EM and the diffusion. When the flux

divergence is greater than the rate of diffusion that disperses the divergence, the markers forms within the cross-strip. Opposite happens when the divergence is less, so that the depletion and accumulation is compensated by diffusional flux.

2.4.3. Mechanism of thickness and length dependence

Except for an unexpected result of slower surface EM rate than the interface EM rate, every aspect of EM mechanism observed in our study follows the conventional understanding of EM. The most notable example is the EM rate dependence on the thickness and length of the passivation layer. These results can be understood within the frame of the Blech effect.

As discussed in section 1.3.2, two counteracting forces are working together for EM in a confined space and they are EM force and the backflow force. The backflow force arises because EM produces stress gradient. An atomic flux divergence causes a change in the atomic density. In a place where mass is accumulated, compressive stress is induced, while the tensile stress is resulted in the opposite case [52,53]. This stress gradient counteracts the EM force and reduces the net atomic flux, as illustrated in Fig.1.3.

The net atomic flux in an interconnect due to the combined effects of the EM force and the stress gradient can be expressed as

$$J_{Total} = \frac{CD}{kT}(Z^{*}e\rho j - \Omega\nabla\sigma) \quad (2.7)$$

where C is the concentration of the migrating species, D is the diffusivity, k is Boltzman's constant, T is the absolute temperature, Z^{*} is the effective charge of the metal ion, e is the charge of electron, ? is the electrical resistivity of metal, j is the current density, Ω is the atomic volume, and $\nabla\sigma$ is the local gradient in the hydrostatic stress. Equation 2.7 represents the forward atomic flux due to the EM driving force and the backward driving force resulting from EM-induced stress gradients. This gradient can only occur if compressive stress builds up as a result of an EM flux divergence [52-54, 84-88]. Equation 2.7 indicates that the influence of the backflow increases with decreasing the length of test strip. For a given material sets, where the yield stress should be the same regardless of the strip length. Therefore, the gradient becomes more significant in short segment, making net flux to be smaller. This effect is well demonstrated by Blech [52,53]. A similar situation arises for our cross-strip configuration after Cu atoms have moved to the downstream edge of cross-strip. At the upstream edge of cross-strip, tensile stresses is created as a result of the depletion of Cu atoms. On the contrary, as Cu atoms are accumulated at the downstream of cross-strip, compressive stress develops, thus creating a stress gradient from upstream edge to downstream edge. This stress gradient acts in opposition to the EM force. This makes the extent of marker formation inversely scales with the cross-strip length. The explanation for the thickness effect is straightforward. Thicker passivation layer would have higher yield strength.

For given length of the cross-strip, therefore, the stress gradient in lines with thicker passivation would be subjected to lower EM rate.

2.4.4 Consideration on surface EM and interface EM

The most striking and important result found in this study is the fact that the surface EM rate is found to be slower than the interface EM rate. The reason why this result is counter-intuitive is simply because the diffusion on Cu surface is known to be far faster than in interface. However, this result may not be entirely new because a few previous studies find such indications. Gladkikh et al. report that the thin Ta over-layer passivation degraded the EM performance of Cu interconnects. They postulate that the mechanism may be related to the lack of damage healing process with Ta passivation [16,20,89,90]. Nevertheless, they contribute the lack of healing effect with passivation to lower interfacial mobility of Cu. It should be noted that EM lifetime testing cannot correctly identify the underlying EM mechanism because factors affecting lifetime is not simple. For example, reported values of lifetime activation energy of Cu interconnects are not consistent but vary considerable even in the interconnects with similar geometry and material make-up. Such a wide variation in data and sensitivity of EM lifetime on various factors of interconnects often leads to erroneous conclusion on the true nature of the EM mechanism even though the observation might be correct.

On the other hand, the cross-strip configuration is less prone to such variations and offer much more decisive evidence for the mechanism in operation. Therefore, it is clear that the surface EM rate is slower than the interface EM rate. The question is the

mechanism, and the mechanism may be found from the consideration on the EM force itself. As can be seen in atomic flux equation (equation 2.13 and 2.19), the EM mass flow is determined by two terms, atomic EM force and mobility. The EM force is dictated by Z*rj while the mobility is dictated by the diffusivity. When EM in given geometry of the cross-strip is considered, the EM force must be dictated by Z* (since current density is the same throughout the test pattern). Therefore, the reason for the interface EM is faster than surface EM must be found from either higher D or higher effective valence (Z^*) of at interface. Ordinarily these two parameters $(D$ and $Z^*)$ cannot be measured independently. However, we believe that the responsible mechanism may lie on the Z* difference, although D difference cannot be completely ruled out.

It is general belief that surface diffusivity is far higher than the interface diffusivity. With lack of data on the interface and surface diffusivity, it is rather difficult to find any substantiating evidence to support that the interface diffusivity is higher than the surface in case of Cu. One possible way that the surface diffusion is slower than the interface diffusion is when the diffusion of Cu is affected greatly by the surrounding bond network numbers. It is known that diffusion of atoms can be affected by environmental bonding condition under certain circumstances. If the mechanism of the periphery diffusion is extended to interface diffusion mechanism, it is possible to argue that the interface diffusion may be faster than surface in Cu. It is known that diffusion of atoms along island edges (periphery diffusion) is much more effective than diffusion of atoms on the flat surface [91-97]. Atoms can be trapped at the kink sites, but once

released, they travel relatively fast along the straight segments of the island edges. Consequently, the diffusion coefficient of atoms moving along the periphery depends on the detailed structure of the island edges. The schematic drawing of atoms flowing by periphery (or step edge) diffusion is shown in figure 3.25. The calculations [98-103] show that diffusion along the [104] step has a barrier of about 0.25eV, which is even smaller than the barrier energy for adatom diffusion on the flat (0.40eV).

If similar mechanism works in the interface diffusion, it is possible that the interface diffusivity is indeed higher than the surface diffusivity. However, it is not certain whether such an extension yields valid pictures for the interface diffusion. It is true that the interface is with more bonds than the surface is, and thus it is possible that the interface diffusivity becomes higher. However, the observations on surface diffusion and interface diffusion, although they are limited, do indicate otherwise. More plausible mechanism is the case when the Z* of interface is far higher than Z* of surface.

The origin of Z* is the momentum exchange between electrons and metal ions during electron scattering process. Electrons flow through a metal film and collide with metal atoms. This collision produces electron momentum transfer to metal atoms and this momentum transfer produces a driving force on the metal atoms in the direction of electron flow as described in section 2.2.1. Z* is the parameter that measures the strength of the momentum exchange effect.

Consideration on the Z* indicates that its value at interface can be higher than at surface. In theory, the Z* consists of two terms. The first term is the electron wind force that is proportional to the momentum transfer rate, while the second term is the electro-

static force. These forces are acting against each other because electrons push atoms to the direction of electron whereas the electrostatic force drags atoms in the opposite direction. For metals, the electron wind force is most dominating and therefore EM occurs in the direction of electron flow. When the wind force is considered, it is assumed to be term representing the momentum transfer of electrons to a lattice defect as electrons are scattered by the defect. Then, The wind force can be assumed to be proportional to the density of free electrons and the ionic volume. The ionic volume is the mean free path of a free electron, l, times the electron collision cross section, Ω, of the activated ion in the saddle point. Then, the wind force term Z_w* can be expressed by:

$$Z_w* = N_e l\Omega * \qquad (2.8)$$

or

$$Z_w* = Z_{el}(\frac{1}{2}\frac{\boldsymbol{r}_d Nm}{\boldsymbol{r}N_d|m*|}), \qquad (2.9)$$

where N is the free electrons density , N_d is the vacancy density, $\boldsymbol{r}$ is electrical resistivity, $\boldsymbol{r}_d$ is the contribution of the defects to the resistivity, and $m/m*$ is the usual effective mass ratio of the electrons.

The effective charge number z_w* of surface and grain boundary in Cu is estimated by C.-K. Hu et al. by fitting the published values of diffusivity and activation energy for diffusion [17]. Using values from calculated from known values of $\boldsymbol{d}_s D_s E_s$ and $\boldsymbol{d}_{GB} D_{GB} E_{GB}$, they fit their drift data to extract Z*. $\boldsymbol{d}_s$ and $\boldsymbol{d}_{GB}$ are width of surface

and grain boundary, D_s and D_{GB} are diffusivity at surface and grain boundary, E_s and E_{GB} are activation energies at surface and grain boundary. In their study, it is found that the values of Z^* are higher at grain boundary than at interface. Their result is consistent with a theoretical prediction that the electron wind force decreases as an atom moves from the bulk to a grain boundary and to a surface [17,105]. Since the structure of the interface must between the surface and the grain boundary, it is plausible to assume that the Z* follows the similar trend, that is that the Z* of interface is greater than the surface.

2.5 Summary

The effects of passivation layer on Cu EM are investigated using single passivation layer cross-strip test. The cross-strip configuration allows the characterization of the interface EM in reference to the surface EM. Using the cross-strip configuration, various types of interfaces are investigated and their EM characteristics are compared.

The results clearly indicate that (1) interface EM is indeed active EM mechanism in Cu thin films, and (2) interface EM in Cu is intrinsically faster than surface EM, at least within materials tested here, regardless of the metallization methods, passivation thickness, or gas ambients. Various considerations and characterizations on the samples and test conditions indicate that the results of the faster interface EM have a generic origin. While many possible mechanisms are explored, it is

believed that the faster interface EM rate is more related to higher Z* at interface than at surface.

CHAPTER 3

TEMPERATURE AND CURRENT DENSITY EFFECTS ON COPPER (Cu) ELECTROM MIGRATION (EM)

3.1 Introduction

As explored in Chapter 2, the investigation on the interface EM mechanism in Cu thin films yields several interesting facts. The study reveals that a) interface EM is certainly active in Cu thin films and that b) the interface EM rate is found to be faster than the surface EM. While these two facts are extensively discussed in Chapter 2, they deserve more attention. Most notably, the finding of the faster interface EM requires additional studies to understand the reason. Although such investigation demands various types of new investigation, it is felt that more detailed analysis on the marker formation mechanism may yield indications that may be helpful in providing insights to the questions. In particular, the location where markers form seems bear critical importance in gaining such insights.

As shown in the results of the Chapter 2, the marker location are not fixed but tend to vary with type of passivation material and cross-strip length. Although phenomenological understanding behind such a change is discussed in Chapter 2, it needs to be further explored to gain better understanding of the physics governing the

interface EM and surface EM. For this reason, we carry out additional experiments that target to gain more information on how marker formation location is determined and, in conjunction with the understanding made in chapter 2, attempt to extract the nature of EM driving force in interface and surface. The additional experiments that are carried out is the identical EM testing but with variation of the testing temperature and current. Efforts are made to identify whether markers form and to connect the results to fundamental EM theories. From this analysis, it is found that the reason for higher rate of interface EM than the surface EM may be related to higher Z* at interface. The result is consistent with speculations made in the Chapter 2.

3.2 Experiments

Two types of passivation materials are used in this study and they are Si_3N_4 and Ta. These samples are made following the same procedures as the others. The thickness of the passivation layers kept at 30nm and several lengths of the cross-strips are patterned on the identical test line. These samples are tested as a function of temperature, ranging from 170 to 320°C. Also, they are test at different current densities, 1.0, 1.5, and 2.0MA/cm^2. After EM testing, the markers are characterized with specific attention to their location.

3.3 Results

This study finds that the marker location varies systematically with length, temperature, and current densities. In case of the hillock, the variation is not easy to

notice because hillock formation is not as substantial as the void formation. The suppression of hillock formation is understandable because its formation requires the deformation of the passivation layer, which requires additional time and energy. With the given limitation, we focus on the characterization of the void marker. The void is much easier to form and to identify. Therefore, the presentation of results and the subsequent discussion are made mainly using the void as the main marker.

3.3.1 Influence of Test Temperature on Marker Location

Figure 3.1 shows the marker formation with variation in test temperatures. In this case, the cross-strip material is 30nm thick Ta and the current density is kept at 1.0MA/cm². The temperature here varies from 170 to 320°C.

In case of the EM test conducted at lowest test temperature, 170°C, only a faint trace of the void and hillock are found even after excessively long duration of EM stressing. This is understandable result because the diffusivity of Cu should be significantly lower at such a temperature. As temperature increases, as expected, the marker formation becomes more pronounced. Note that the polarity of the markers is not affected by the testing temperature. However, one interesting result is that the location of the marker seems to change with testing temperature. It appears that the void nucleation tend to occur outside of the cross-strip area at lower temperatures but shift toward inside of the cross-strip at higher temperatures. The formation of the voids within the passivation layer is clearly visible in lines tested at 270 and 320°C. Testing

with other types of interface materials do show similar trend. Additionally, there is a variation on marker location within the given test structure.

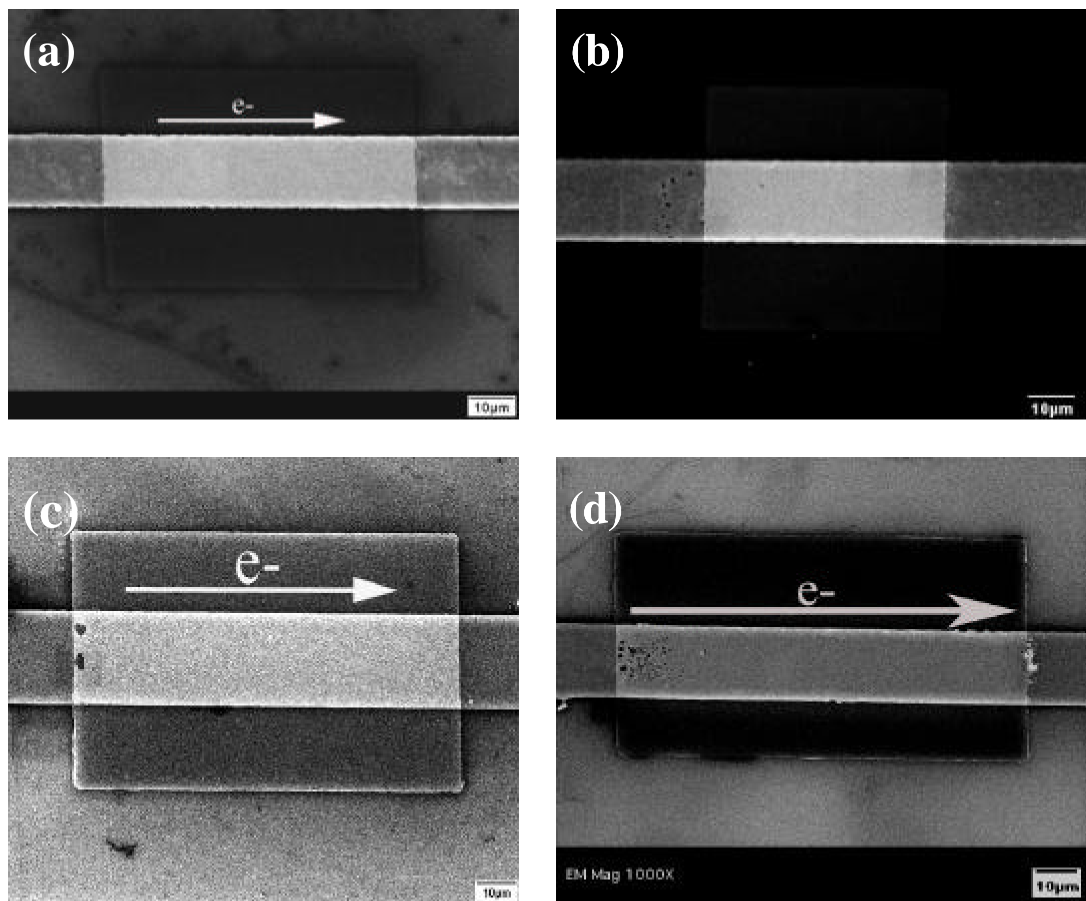


Figure 3.1 SEM images of Ta cross-strips at different EM test temperatures and $1MA/cm^2$ of current density; (a) 170°C, 115 hours test, (b) 220°C, 115 hours test, (c) 270°C, 48 hours test and, (d) 320°C, 24hours test

Since several different lengths of cross-strips are tested, it is possible to observe how the location changes with the length. The result is similar to what is explained in Chapter 2.3.2.2, that is that the marker formation within the cross-strip is more favored in longer strip while outside of the strip is favored in short strip pattern.

3.3.2 Influence of Current density on Marker Location

It is found that the location of the marker formation is also influence greatly by the current density. Figure 3.2 shows the supporting evidence of such a change. These figures show the markers formed at two different current densities at 220°C. Figure 3.2 (a) and (b) are SEM micrographs of a Ta cross-strip tested under j=1MA/cm^2 for 55 and 110 hours, (c) and (d) are the Ta cross-strips tested under j=2MA/cm^2 for 55 and 110 hours.

It can be seen that the location of marker formation is shifted. Voids initially form outside the upstream edge of cross-strip at j=1MA/cm^2. As the test progressed, voids became larger and denser, followed by the nucleation of new voids within the upstream edge of cross-strip. On the contrary, for samples tested at 2MA/cm^2, voids begin to form within cross-strip. With continuing EM, new voids begin to form at outside of the cross-strip. However, in so far as nucleation sites are concern, it is a general trend that the voids favors the area outside of the cross-strip at lower current density and favors inside of the cross-strip at higher current density.

Similar to the case of temperature dependence study, the nucleation site for voids is systematically varied with the cross-strip length. At a given current density, outside of the cross-strip is more favored in lines with shorter strip length while inside is favored with longer strip width.

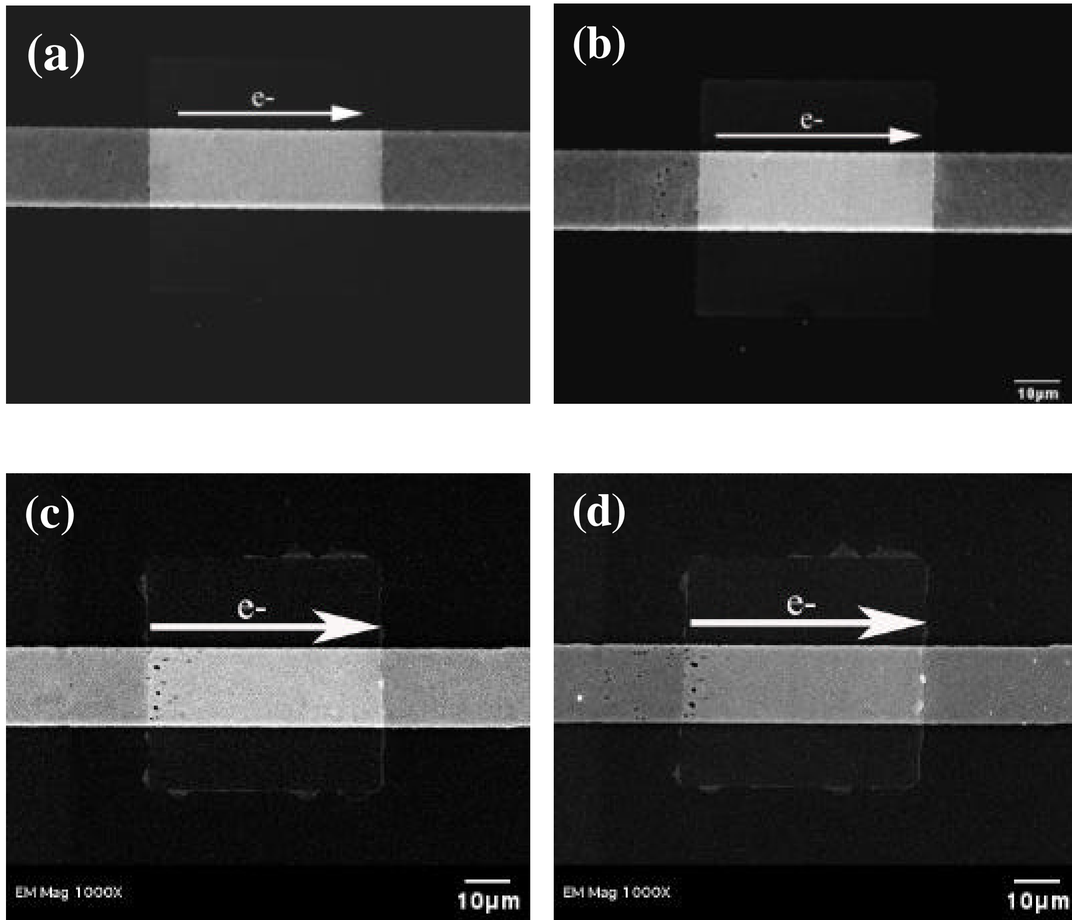


Figure 3.2 SEM images of cross-strip of different current density at 220°C; (a) Ta, 1MA/cm^2, 55hours test, (b) Ta, 110hours test, (c) Ta, 2MA/cm^2, 55hours test, and (d) 110hour test

3.4 Discussion

It is observed that the marker formation changes systematically with temperature, current density and the strip length. Ideally, such shift shouldn't occur because the marker formation is a result of the flux divergence created by two EM fluxes (surface and interface) and thus the inside of the cross-strip near to the upstream edge is the most

favored place for the voiding. In practice, however, it is changing and should near important physics relevant to interface and surface EM mechanism.

As discussed in the Chapter 2, the marker formation is not only affected by the flux divergence site but also affected by the nucleation process [69]. The site of maximum flux divergence is not necessarily the favored place for voiding because it is located underneath the passivation layer where physical confinement exists. In order for voiding to occur, the vacancy concentration should exceed the critical concentration. The critical vacancy concentration is determined by the energy of creating new surface, which is likely to be different depending on locations. As seen in previous chapter, the voids always nucleate at the interface or surface. With such nucleation process, it is likely that the critical vacancy for voiding inside of cross-strip area and outside area is not the same. The difference arises from the fact that the nucleation at interface requires the creation of new surface while the nucleation at free surface does not (voiding at free surface would require energy only enough to make the surface area larger). Therefore, it is plausible to conclude that the critical concentration for voiding is high at the interface and low at the free surface.

With low critical vacancy concentration for voiding at free surface, the area outside of the cross-strip is energetically favored place for void nucleation. On the other hand, inside of the cross-strip area is favored for void nucleation in terms of flux divergence. We believe that these two competing factors are responsible for the shift of void nucleation site. In case when the flux divergence generated in given time is sufficient to produce vacancy accumulation exceeding the critical concentration, voids

nucleate inside of the cross-strip. On the other hand, flux divergence is not sufficient such that the vacancy concentration does not reach the critical, then the vacancy has a time to diffuse away toward outside of the cross-strip. Since outside area is with lower critical vacancy concentration, voids can nucleate and grow in the area outside of the cross-strip. This mechanism explains why the location of void nucleation changes with the cross-strip length. This is the simplest case to examine the mechanism since EM condition is identical for all lengths. With the Blech effect, the flux divergence at the longer segment is higher, making it easier to reach the critical vacancy concentration at inside of the cross-strip area. When the strip length becomes shorter, the flux divergence becomes less and thus the nucleation favors the free surface located outside of the cross-strip area [52,53].

The application of the developed mechanism to the temperature dependency and current dependency provide further insights as to the nature of the EM mechanism at surface and interface. The first case to examine is the temperature dependence of the void location. In order for marker to favor the outside of the cross-strip area at lower temperature, the flux divergence (flux difference) must decrease with temperature. If it is assumed that the difference in the critical vacancy concentration between the interface and surface is not affected too much with temperature, the only possible way that the flux divergence decreases with temperature is the case when the diffusion activation energy for surface and interface is not the same. As shown in Fig.3.3, when the activation energy for EM flux is the same for both interface and surface, there

should be no change in the flux divergence in reference to the diffusion kinetics (because D also scales with temperature by the same amount).

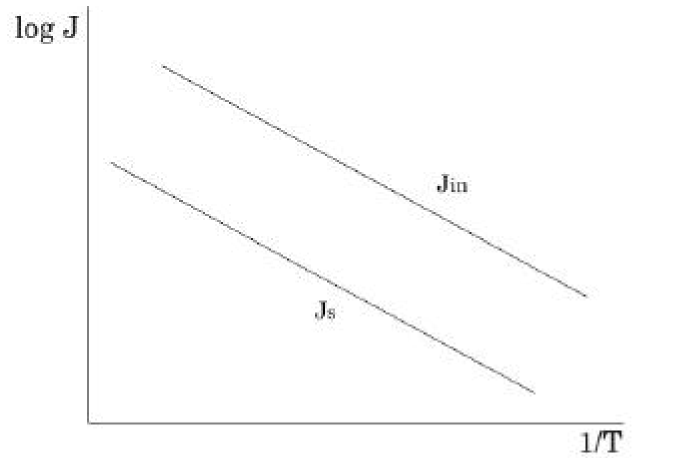


Figure 3.3 Temperature dependence on EM flux
(when $\Delta J_{in} = \Delta J_s$)

Therefore, in order to account for the experimentally observed case, the interface EM flux and surface EM flux must scale differently with temperature, as shown in Fig.3.4.

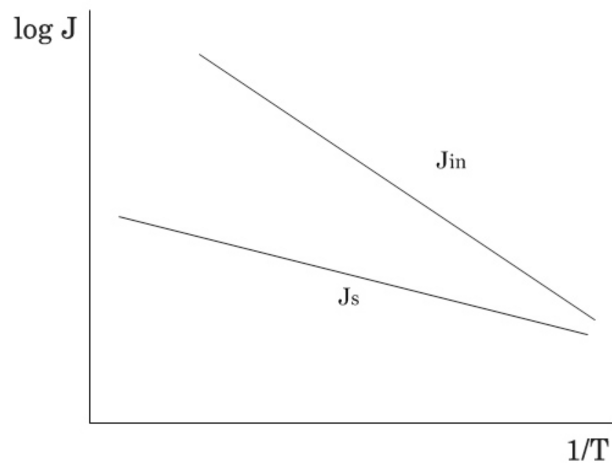


Figure 3.4 Temperature dependence on EM flux
(when $\Delta J_{in} > \Delta J_s$)

Because the EM flux is determined by

$$J = \frac{DC}{kT} Z^* e\mathbf{r}j \tag{3.1}$$

where D is the predominant term affecting the flux J, the diagram shown in Fig.3.4 indicates that the activation energy for diffusion at interface is higher than that at the surface ($E_{a(\text{interface})} > E_{a(surface)}$). The atomic diffusion coefficient D is a function of temperature in Arrhenius equation as follows [17,43,50,51]:

$$D = D_O \exp(-\frac{E_a}{kT}) \tag{3.2}$$

It is generally accepted fact that the diffusivity of atomic species with higher activation energy is lower, eq.3.2 must lead to $D_i < D_s$.

This result, that is $D_i < D_s$, is consistent with many previous findings and general physics of diffusion. The result further indicates that Z* of interface must be much higher than Z* of surface. As seen in many results, the polarity of marker formation always indicates that the interface EM rate is higher than the surface EM rate.

It means that

$$\frac{D_i Z_i}{kT} je\mathbf{r} > \frac{D_s Z_s}{kT} je\mathbf{r} \tag{3.3}$$

Since $D_i < D_s$, the only way for equation 3.3 to work is when $Z_i >> Z_s$. As discussed in Chapter 2, this result is probably consistent with theoretical consideration on EM physics.

The current density dependence of the marker location can also support the conclusion that $Z_i > Z_s$. In order to shift the location of void nucleation from the outside to inside of the cross-strip area, the interface EM flux and surface EM flux should scale with current density in the manner displayed in Fig.3.5. At low current density, the EM flux divergence (flux difference) is small, so that void nucleation occurs at the outside of the cross-strip. With increasing current density, the flux divergence increases and thus voiding favors inside of the cross-strip. In order for this to work, following relation must be true: $D_i Z_i > D_s Z_s$. If $D_s > D_i$ as is found from the temperature dependency analysis, Z_i must be significantly greater than Z_s.

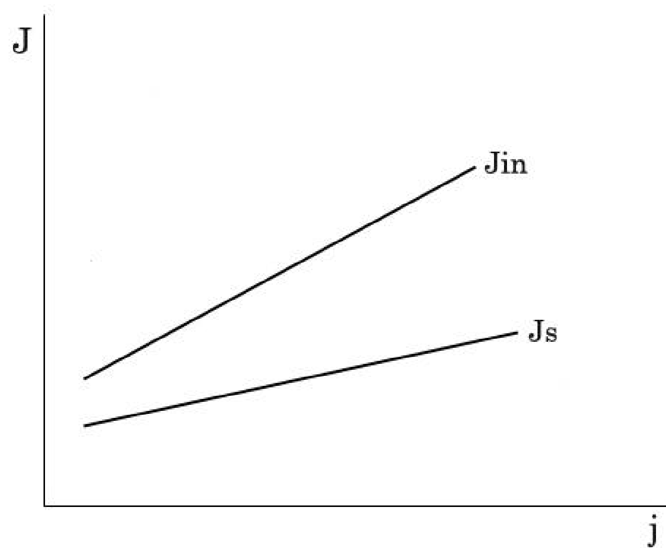


Figure 3.5 Current density dependence on EM flux (when $\Delta J_{in} > \Delta J_s$)

From the analysis of the temperature and current dependence of marker location, our study finds that the higher interface EM rate than the surface EM is probably due to higher effective charge valence (Z*) for EM at interface. It is true that the direct

evidence for such a finding is lacking. However, within the observations made in our study and plausible reasoning, we do believe that the conclusion bears correct physical fact.

3.5 Summary

The mechanism behind the change in the marker formation location is explored in this chapter. Experimentally, markers are found to form at different places depending on the EM test conditions and cross-strip length. General trend is that void nucleation prefers outside of the cross-strip area as

a) Temperature decreases

b) Current density decreases

c) Cross-strip length decreases.

Our analysis finds that such variation stems from the interplay between the flux divergence and the critical vacancy concentration for voiding. With lower vacancy concentration at free surface, we believe that the nucleation at outside of the cross-strip is favored with decreasing flux divergence. Further analysis on the temperature and current density dependence reveals that

a) Diffusion activation energy for interface is higher than that for surface, and

b) Diffusivity of Cu atoms at surface is higher than at interface, and

c) The effective charge valence for EM at interface is higher than the surface.

The finding of higher effective charge valence at interface is particularly important conclusion drawn from this study because it may explain why the interface EM rate is higher than the surface EM rate.

CHAPTER 4

STUDY OF RELATIVE ELECTROMIGRATION (EM) RATE USING DOUBLE PASSIVATION LAYER CROSS-STRIP AND UNDER LAYER CROSS-STRIP TEST

4.1 Introduction

The cross-strip test configuration with single passivation layer is proved to be extremely effective in studying the nature of interface EM in Cu thin films. Our study shows how interface EM occurs and how it is related to the surface EM mechanism. While the single passivation configuration is useful in studying the characteristics of interface EM, it is found that the configuration is rather ineffective in yielding direct comparison of EM rate variation with different passivation material. To a certain extent, the comparison can be made with the single passivation layer because the passivation layer producing an interface with higher interfacial EM rate produces more pronounced marker formation at identical EM testing condition. However, the comparison is ineffective because it takes two samples and, more importantly, prone to errors. Nevertheless, the comparative information on interfacial EM mechanism is critically needed both for engineering and scientific purposes. Engineering importance of such information is apparent. In microelectronics, enhancing EM reliability of Cu interconnects is of immense importance. For this reason, related industries are

experimenting with various types of interfacial materials yet lack of fundamental data on interface EM makes their efforts to be extremely challenging. The comparative understanding of the interfacial EM is also important for scientific purpose. As indicated, the mechanism of interface EM is least understood subject in the EM research field. It is not known how interfacial EM occurs and how the mechanism is changed by interface types.

We find that a simple extension of the single cross-strip configuration can provide an effective way of yielding needed information on the interfacial EM. This new configuration is shown in figures 4.1 and 4.2. As is shown, there are two different configurations that are equally effective in studying the interfacial EM difference and they are the double passivation and the under-strip configuration. The configuration of the double passivation is identical to the single passivation except that an additional layer is deposited on top of the entire line of the single cross-strip pattern. In this case, the marker formation is a result of EM rate difference between the interface formed by the first layer and the second layer. The under-strip configuration achieves the same purpose except that the flux divergence sites created by two different interfaces are located at the substrate side.

With these samples, a direct comparison of interface EM rate between two different passivation materials can be made by observing the polarity of the markers. Similar to the case of the single passivation configuration, the markers form because of the EM rate difference. In case when the interface EM rate in the central strip is faster than the surrounding interface, voids should form at the upstream edge and hillock form

at the downstream edge of the strip. The opposite polarity should occur when the difference in EM rate is reversed. With preparation and EM testing of one sample, the relative difference in interface EM rate of two interfaces can be made with these configurations. Furthermore, substantiation of any result can be made with a simple test. What is required is to make another sample with the same passivation materials but having reversed arrangement for the central strip and the surroundings. In this case, the polarity of the marker must be reversed.

We carry out a series of EM testing using the double passivation and the under-strip configurations with specific aims:

(1) To validate the findings made in the single cross-strip testing. The single cross-strip testing suggests that the interfacial EM rate differs with different passivation layers, Si_3N_4/Cu being the fastest and CoWP the slowest. However, such a finding is qualitative and needs more direct confirmation. Further, if such a finding is proven to be correct, it can be concluded that the interfacial and surface EM mechanism seen in the single cross-strip testing is free from experimental errors.

(2) To find the best interface materials for enhancing EM reliability. Undoubtedly, this part of work is motivated by the engineering needs.

Our experiments with the new configurations demonstrate that there is indeed a difference EM rate between the passivation materials, and the difference matches with the qualitative comparison made from the single cross-strip study. With this result, it is

also concluded that the nature of surface and interface EM observed in the single passivation test has an intrinsic origin EM.

4.2 Experiments

The configuration double cross-strip test is shown in figure 4.1. We capsulated all of the Cu surface with thin passivation film after cross-striped passivation.

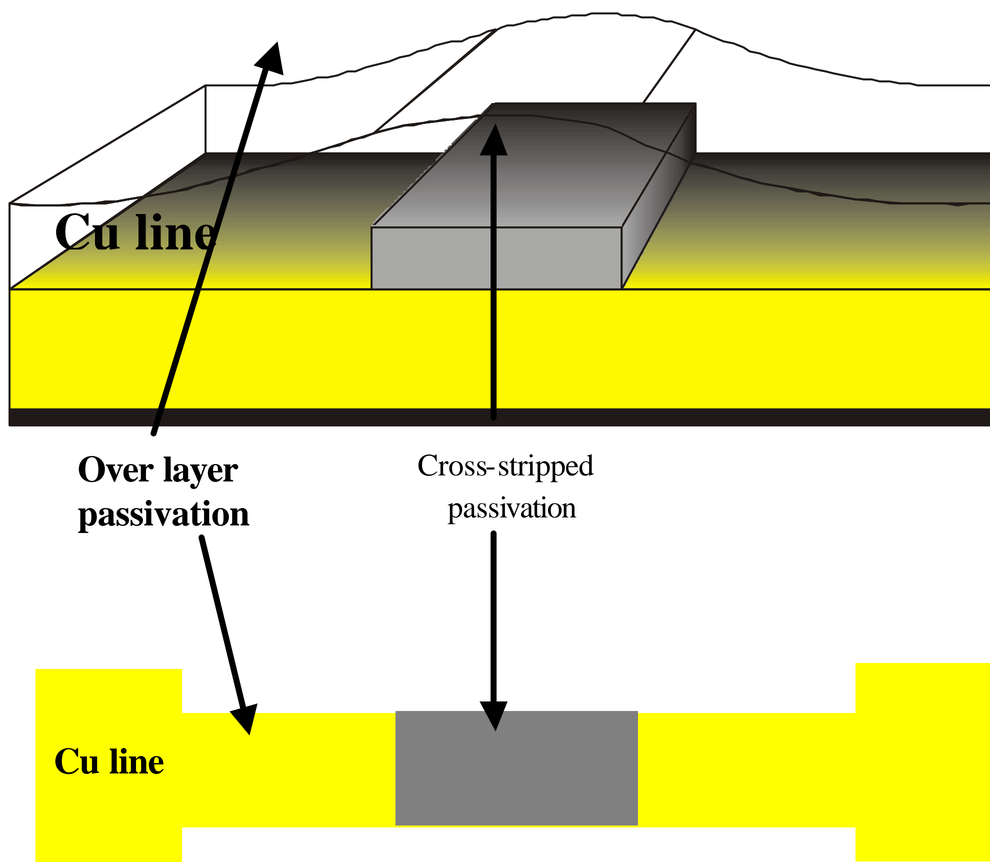


Figure 4.1 The configuration of double passivation layer cross-strip test

After creation the cross-strip of one passivation material on the Cu line (center strip), very thin layer of the second passivation material is deposited over the entire Cu line.

The schematic diagram of under layer cross-strip structure is shown in figure 4.2. The samples are prepared in the same manner as the double passivation layer cross-strip, but the sequence of layer deposition was changed. Prior to deposition of Cu film, very thin cross-strip pattern is deposited first and patterned on top of substrate that is coated with second material under study. Then, Cu line is patterned over the target area. By doing this, the surface of Cu line is not confined and free to deform. Therefore, interfacial EM rate study can be conducted without influence from stress effect.

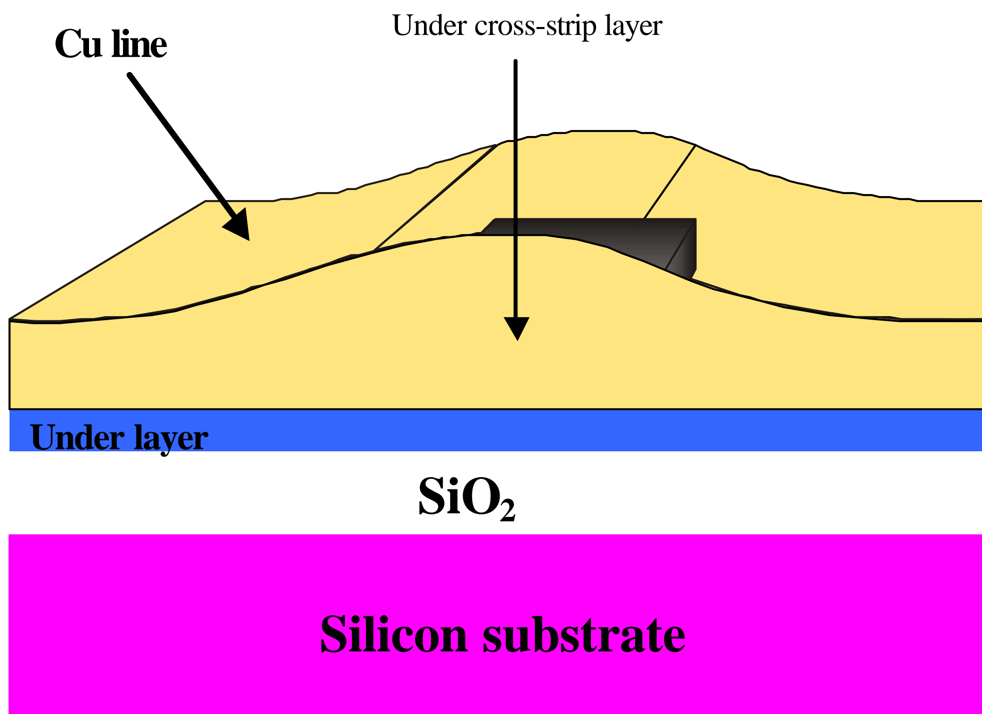


Figure 4.2 The configuration of under layer cross-strip test

4.3 Results

4.3.1 Double passivation layer cross-strip

4.3.1.1 Ta cross-strip with Si_3N_4 over passivation vs. Si_3N_4 cross-strip with Ta over passivation

In order to better understand the difference in the interface EM behavior between the two different passivation materials, Ta and Si_3N_4 layers are first examined. After depositing cross-strip of either Ta or Si_3N_4, very thin layer of the other material is deposited over the entire Cu line. In this case, we can create two different interfaces with Cu and direct comparison of EM behavior between Ta and Si_3N_4 with Cu interface is possible.

Figure 4.3 shows the SEM image of the marker formation in lines with Ta cross-striped area and Si_3N_4 film as over-passivation after a 100 hours EM test at 270°C under forming gas ambient. The cross-strip area is Ta/Cu interface and the area of outside cross-strip is Si_3N_4/Cu interface. It can be seen that hillocks form at the upstream edge and voids form at the downstream edge of cross-strip.

This result indicates that the EM rate at Ta/Cu interface is slower than at Si_3N_4/Cu interface, which is consistent with the findings made from the single cross-strip test (section 2.3.1.1 and 2.3.1.2). When the sequence of passivation material is revered, that is to use Si_3N_4 as cross-strip and Ta thin film as over layer, it is found that the marker polarity is revered. The result of this test is shown Figure 4.4 where SEM image of markers formed in the test line after 100 hours of EM testing at 270°C under forming gas ambient.

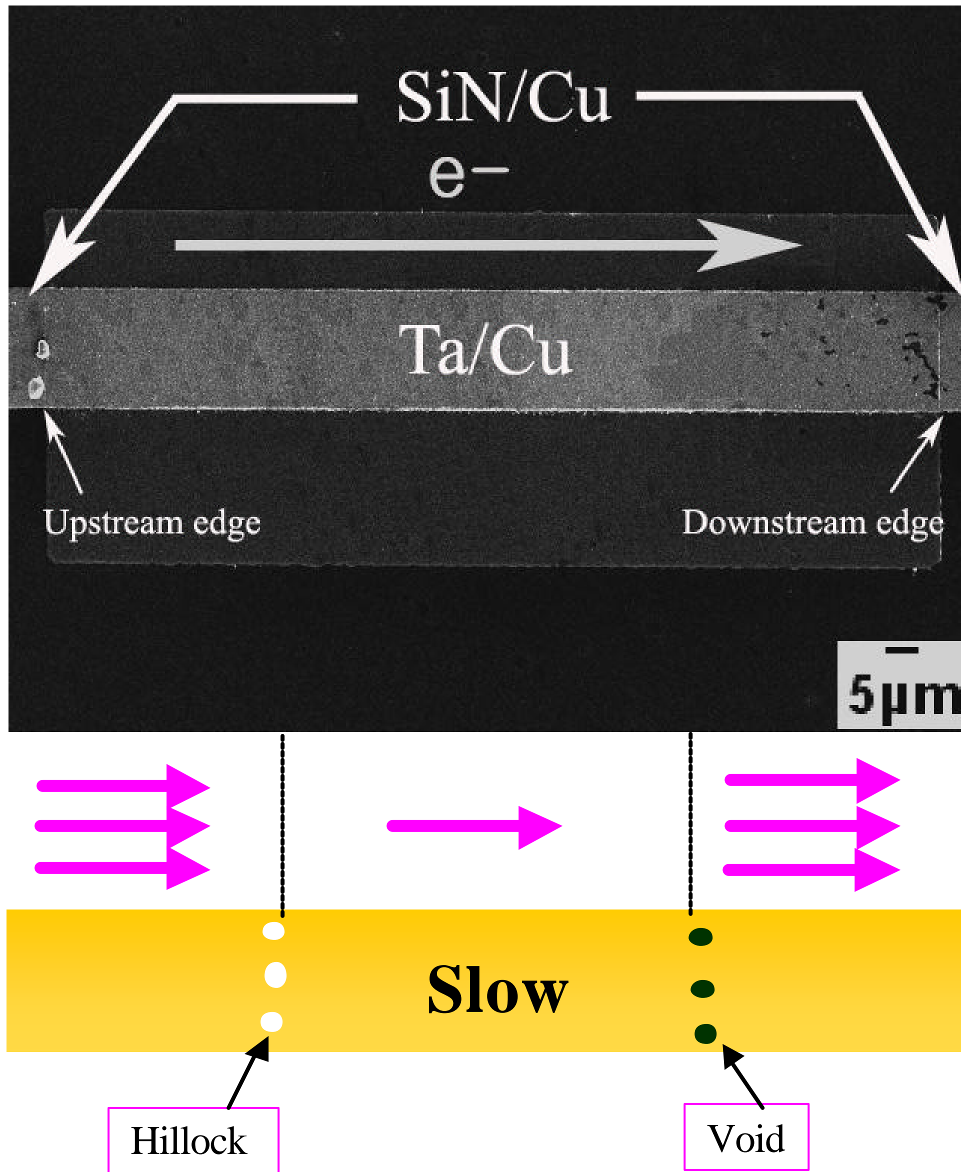


Figure 4.3 SEM image of Ta cross-strip with Si_3N_4 over passivation after 100 hours test at 270°C, 1.5MA/cm^2 under forming gas ambient

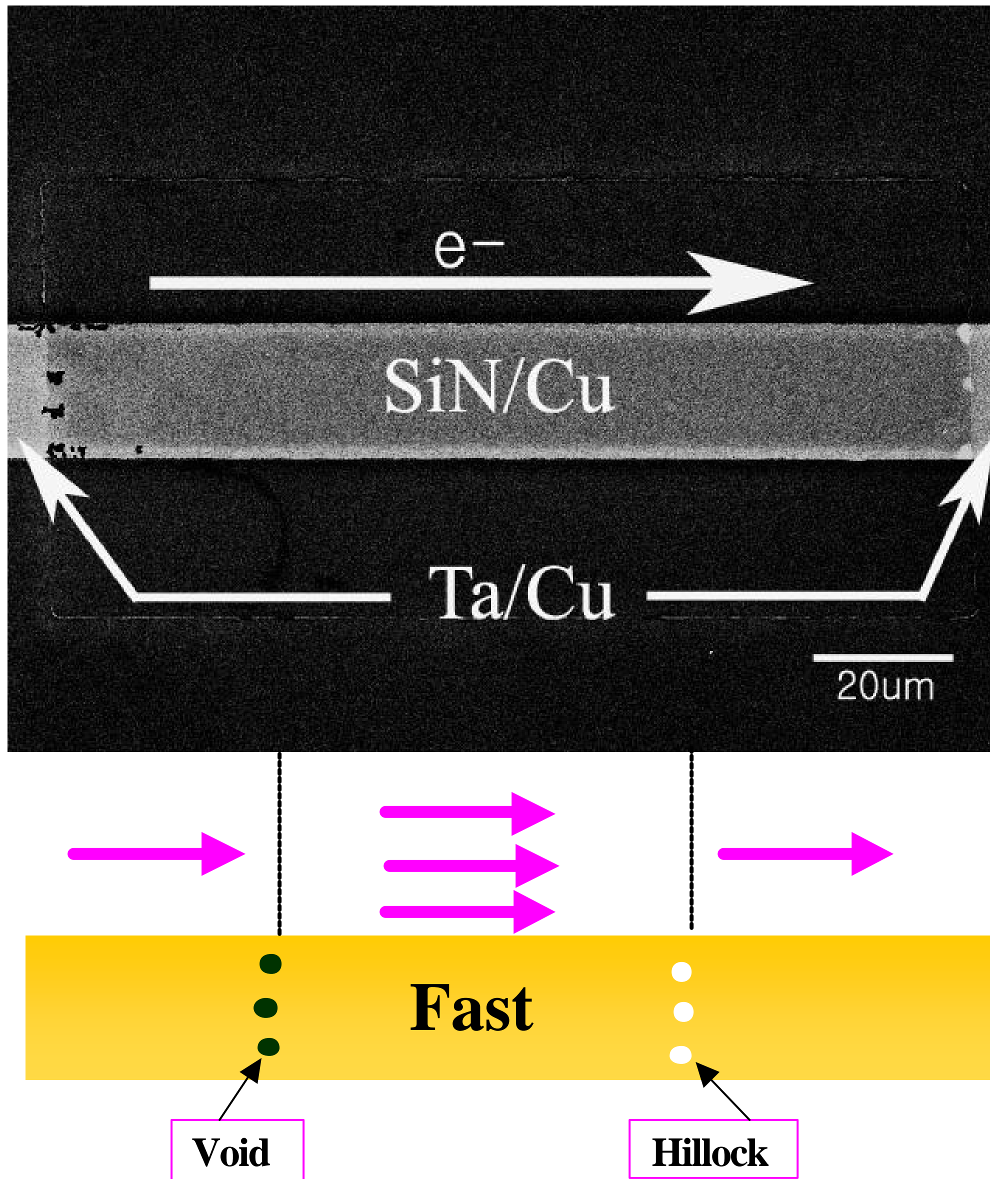


Figure 4.4 SEM image of Si_3N_4 cross-strip with Ta over passivation after 100 hours test at 270°C, 1.5MA/cm^2 under forming gas ambient

Note that hillocks form at the downstream edge and voids form at the upstream edge of the Si_3N_4 cross-strip, indicating that the Ta/Cu interface has a slower EM rate than Si_3N_4/Cu interface.

The change in marker polarity with changing passivation sequence confirms the relative EM rates seen in the single passivation cross-strip tests. These results provides clear evidence the interface EM rate of Ta is slower than that of Si_3N_4.

4.3.1.2 Ta cross-strip with CoWP over passivation vs. CoWP cross-strip with Ta over passivation

Figure 4.5 shows the SEM image of Ta cross-strip with CoWP over passivation after 100 hours EM test at 270°C under forming gas ambient. The cross-strip area is Ta/Cu interface and outside cross-strip is CoWP/Cu interface. Note that voids form at the upstream edge and hillocks form at the down stream edge of cross-strip. The marker polarity indicates CoWP passivation has slower EM rate than Ta passivation.

Figure 4.6 shows SEM image of Cu lines with CoWP cross-strips and a thin over layer of Ta after 100 hours of EM testing at 270°C under forming gas ambient. In this configuration, cross-strip area is CoWP/Cu interface and outside cross-strip is Ta/Cu interface. Notice that the polarity of markers is reveresed with changing passivation sequence. It means that interface EM rate of CoWP is slower than that of Ta.

The polarity of marker formation in this study is also consistent with the previous results.

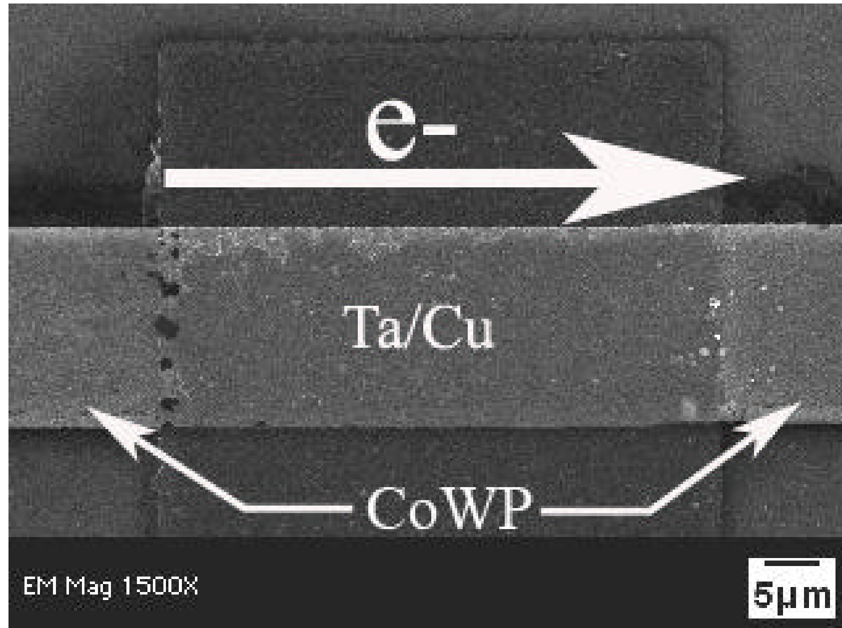


Figure 4.5 SEM image of Ta cross-strip with CoWP over passivation after 100 hours test at 270°C, 1.5MA/cm^{2} under forming gas ambient.

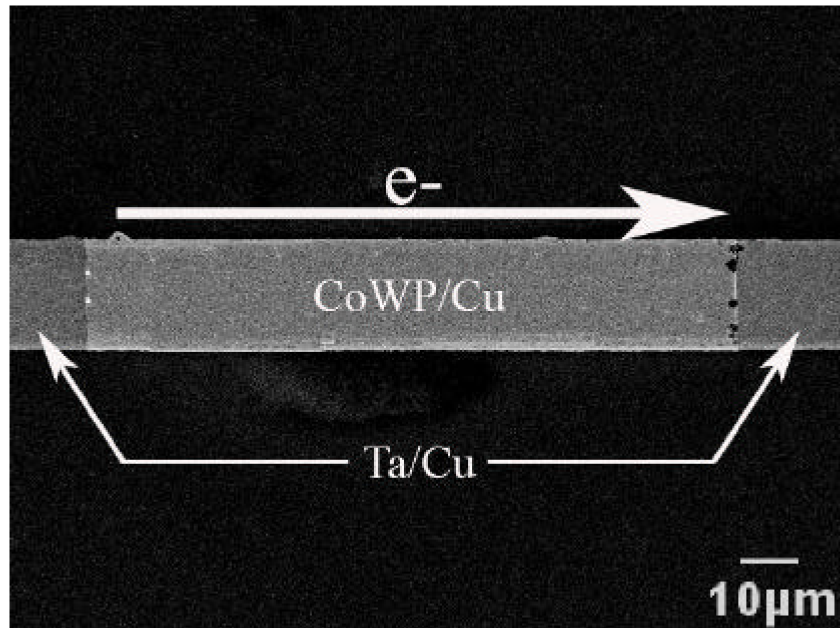


Figure 4.6 SEM image of CoWP cross-strip with Ta over passivation after 100 hours test at 270°C, 1.5MA/cm^{2} under forming gas ambient.

4.3.1.3 TaN cross-strip with CoWP over passivation

Figure 4.7 shows SEM image of Cu lines with TaN as a cross-strip and a thin over layer of CoWP after 48 hours of EM testing at 270°C, j=2MA/cm^{2} under forming gas ambient. In this case, voids form at the upstream edge and hillocks form at the down stream edge of cross-strip. This marker polarity indicates CoWP passivation has slower EM rate than TaN passivation.

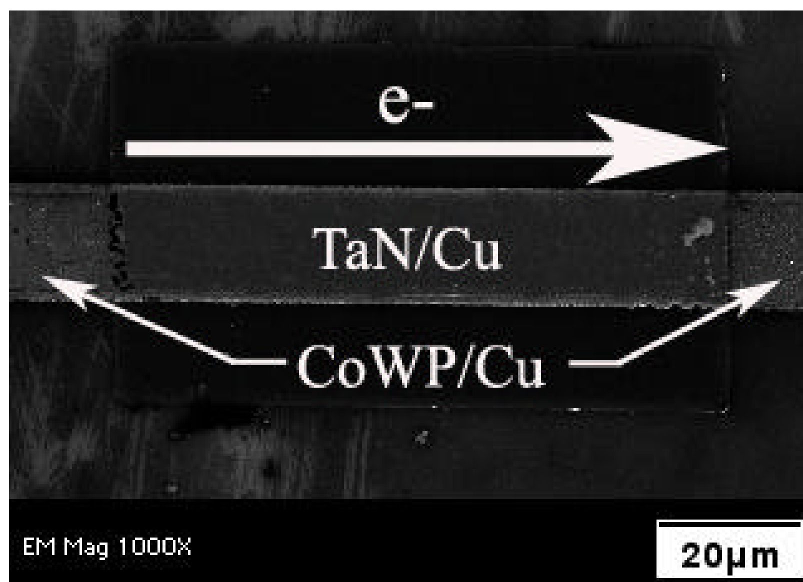


Figure 4.7 SEM image of TaN cross-strip with CoWP over passivation after 48 hours test at 270°C under forming gas ambient.

4.3.1.4 Ta cross-strip with TaN over passivation

Figure 4.8 shows the SEM image of Ta cross-strip with thin TaN film passivation after 100 hours EM test at 270°C, 2MA/cm^{2} under forming gas ambient. Note that voids form at the upstream edge and hillocks form at the downstream edge of

Ta cross-strip. The polarity of markers indicates that TaN passivation provides interface with slower EM rate than in Ta.

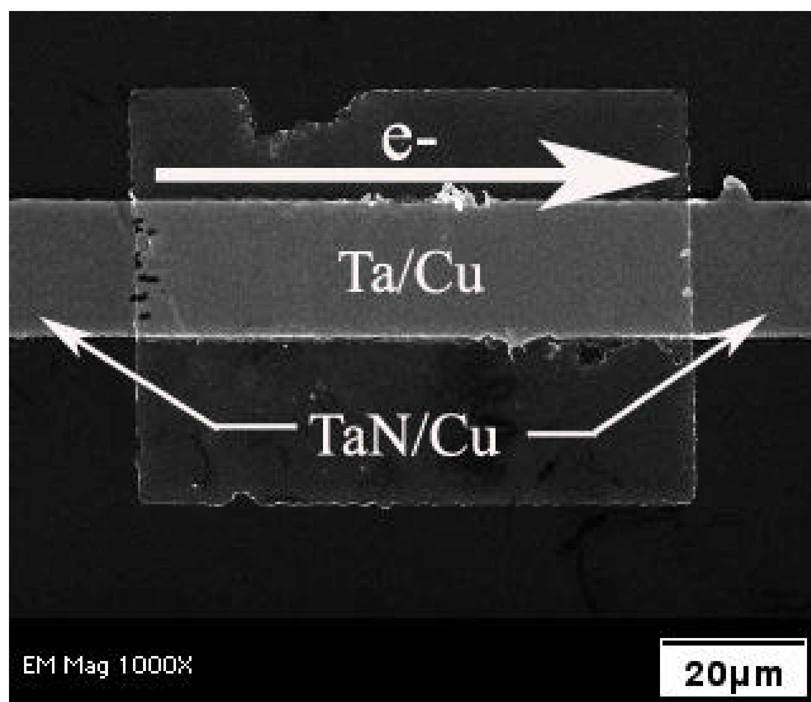


Figure 4.8 SEM image of Ta cross-strip with TaN over passivation after 100 hours test at 270°C, 1.5MA/cm^2 under forming gas ambient.

4.3.1.5 Cr cross-strip with Si_3N_4 over passivation

Figure 4.9 shows the SEM image of test lines with Cr as cross-strip and thin Si_3N_4 film as passivation after 100 hours EM test stressing at 270°C, and 1.5MA/cm^2 under forming gas ambient. The cross-strip area is Cr/Cu interface and outside the cross-strip is Si_3N_4/Cu interface. The polarity of markers indicate that Cu EM proceeds

with slower rate in the Cr cross-strip region than outside the cross-strip where Si_3N_4 creates an interface with Cu.

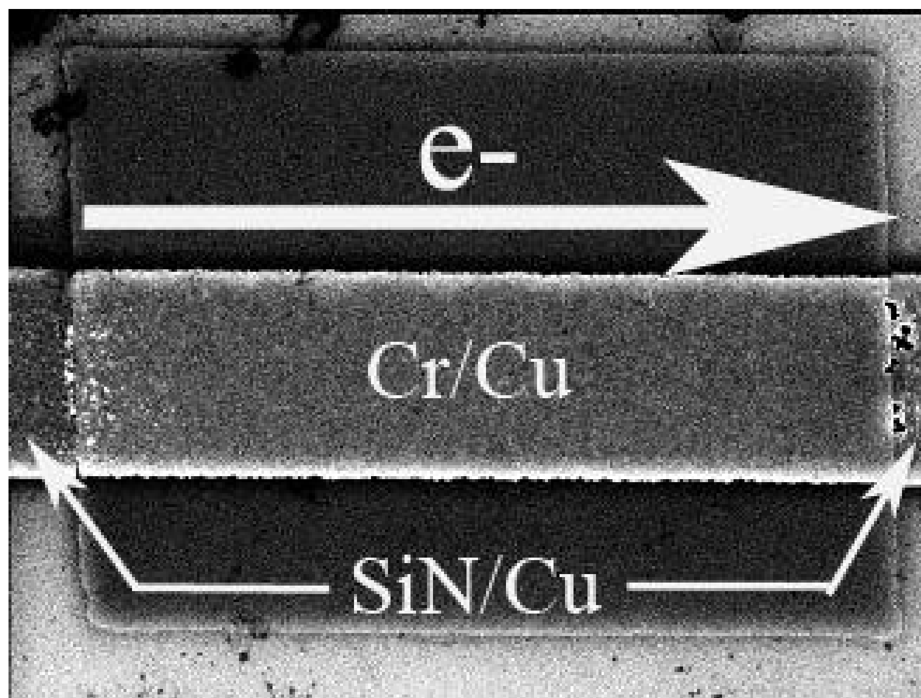


Figure 4.9 SEM image of Cr cross-strip with Si_3N_4 over passivation after 100 hours test at 270°C, 1.5MA/cm^2 under forming gas ambient.

4.3.2 Under layer cross-strip

It is possible that the double cross-strip configuration is subjected to influences from film stress because test pattern is entirely encapsulated. In order to carry out EM investigation without influence from such stress, the under-strip configuration is made. Nevertheless, the results obtained from the underlayer cross-strip matches very well with the double cross-strip, indicating that the stress impart minimal influence on the results obtained from the double passivation configuration.

4.3.2.1 Ta under layer cross-strip on Si_3N_4 vs.
Si_3N_4 under layer cross-strip on Ta

Figure 4.10 shows the SEM image of marker formation in test lines with Ta under cross-strip on the Si_3N_4 layer, and figure 4.11 shows the result of Si_3N_4 under cross-strip on the layer of Ta, after 100 hours EM test stressing at 270°C, and 1.0MA/cm^2 under forming gas ambient. Notice that the polarity of markers is identical to the same cases studied with double layer cross-strip configuration. In case of Ta under cross-strip on the Si_3N_4 layer, voids form at the downstream edge and hillocks form at the upstream edge of cross-strip for Ta under cross-strip on the Si_3N_4 layer. The polarity of void and hillock formations indicates Ta passivation has slower EM rate than Si_3N_4 passivation. The polarity reveres when the sequence is changed, that is Si_3N_4 becomes the under cross-strip: voids form at the upstream edge and hillocks form at the downstream edge of cross-strip shown in figure 4.11.

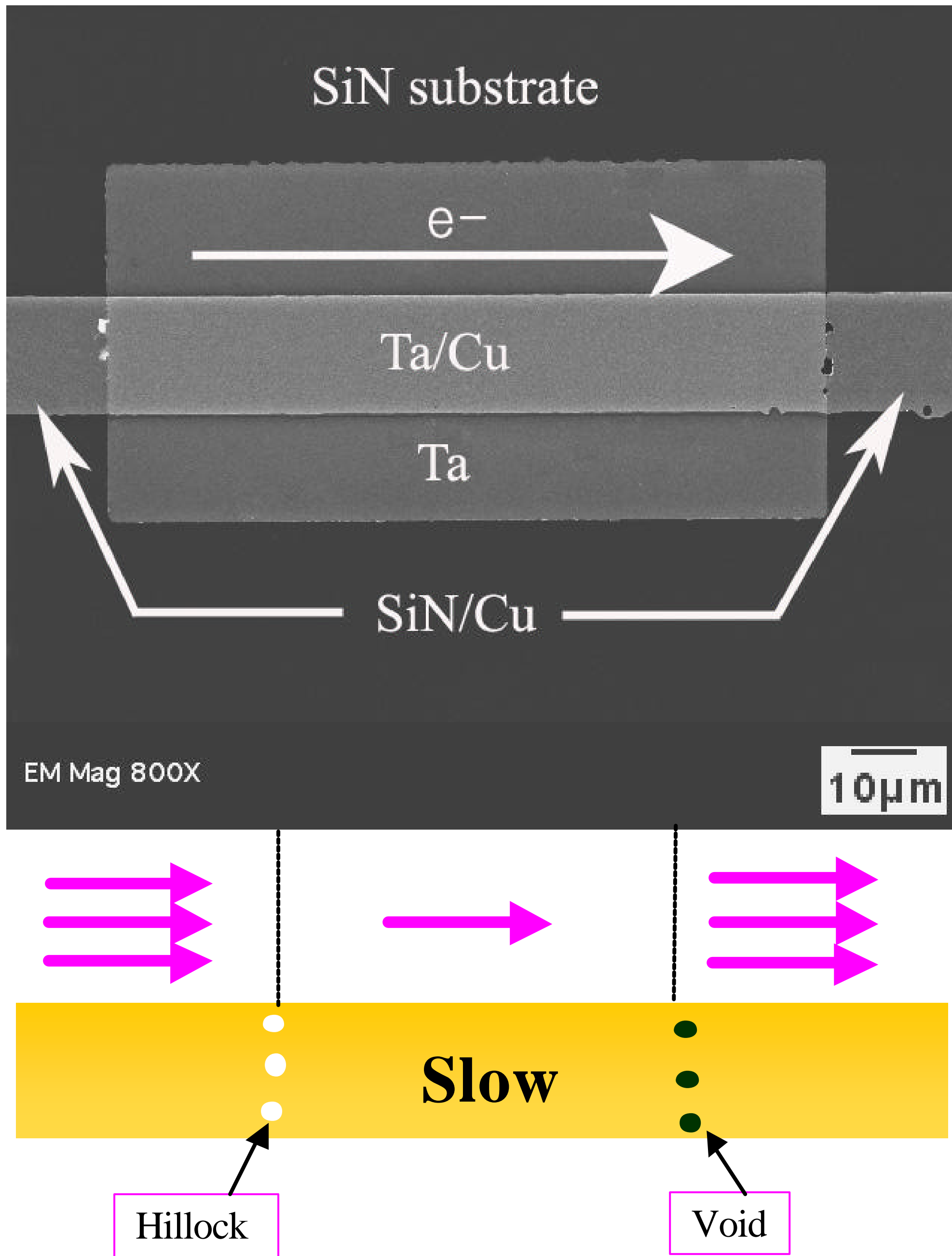


Figure 4.10 SEM image of Ta under cross-strip on Si_3N_4 after 100 hours test at 270°C, 1.0MA/cm^2 under forming gas ambient

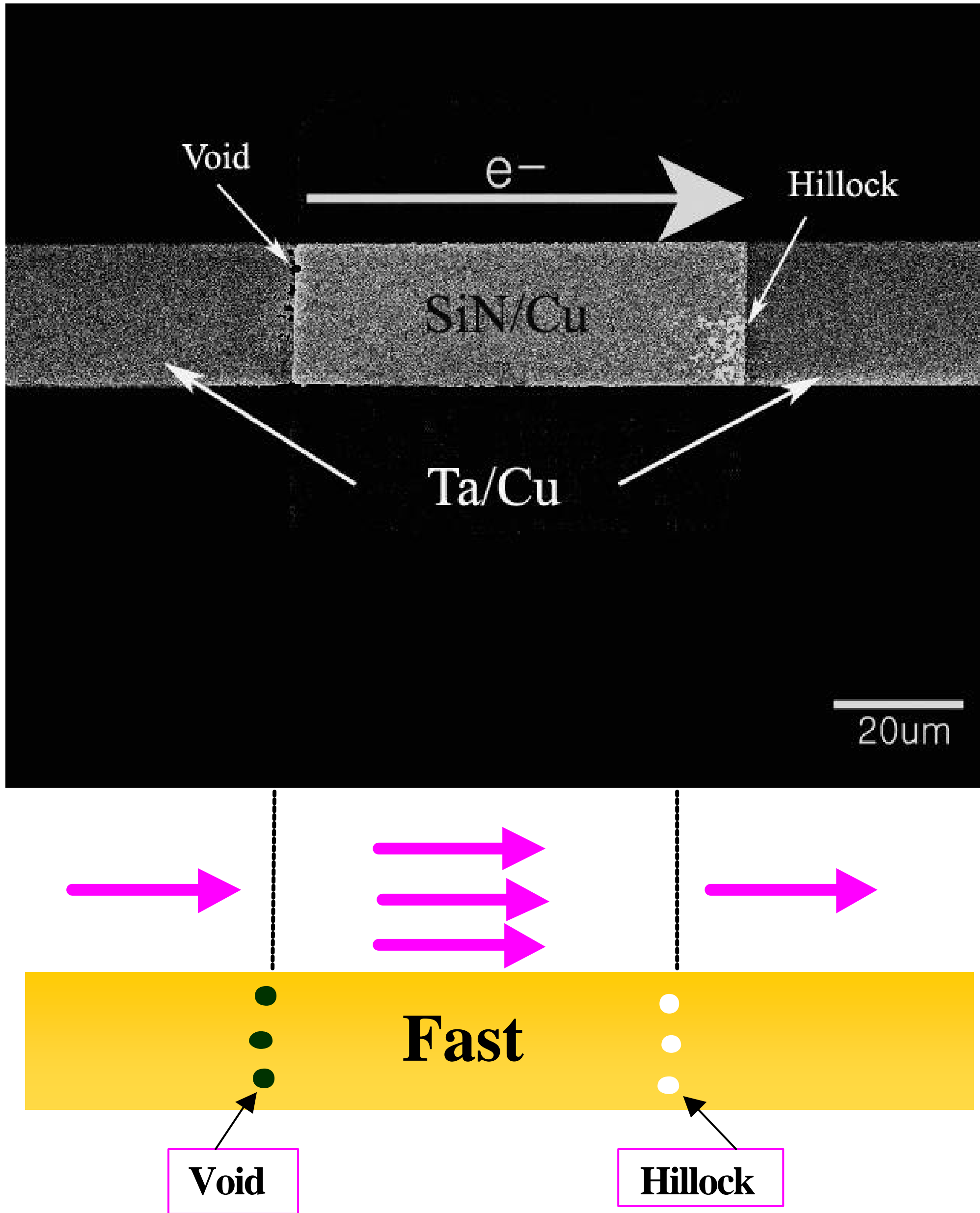


Figure 4.11 SEM image of Si_3N_4 under cross-strip on Ta after 100 hours test at 270°C, 1.0MA/cm^2 under forming gas ambient

4.3.2.2 Ta under layer cross-strip on SiO_2

Figure 4.12 shows SEM image of Cu lines with Ta under cross-strip on the layer of SiO_2 after 100 hours of EM testing at 270°C, 1.0MA/cm^2 under forming gas ambient. In this configuration, hillocks form at the upstream edge and voids form at the downstream edge of the Ta cross-strip, indicating that the Ta/Cu interface has a slower EM rate than SiO_2/Cu interface.

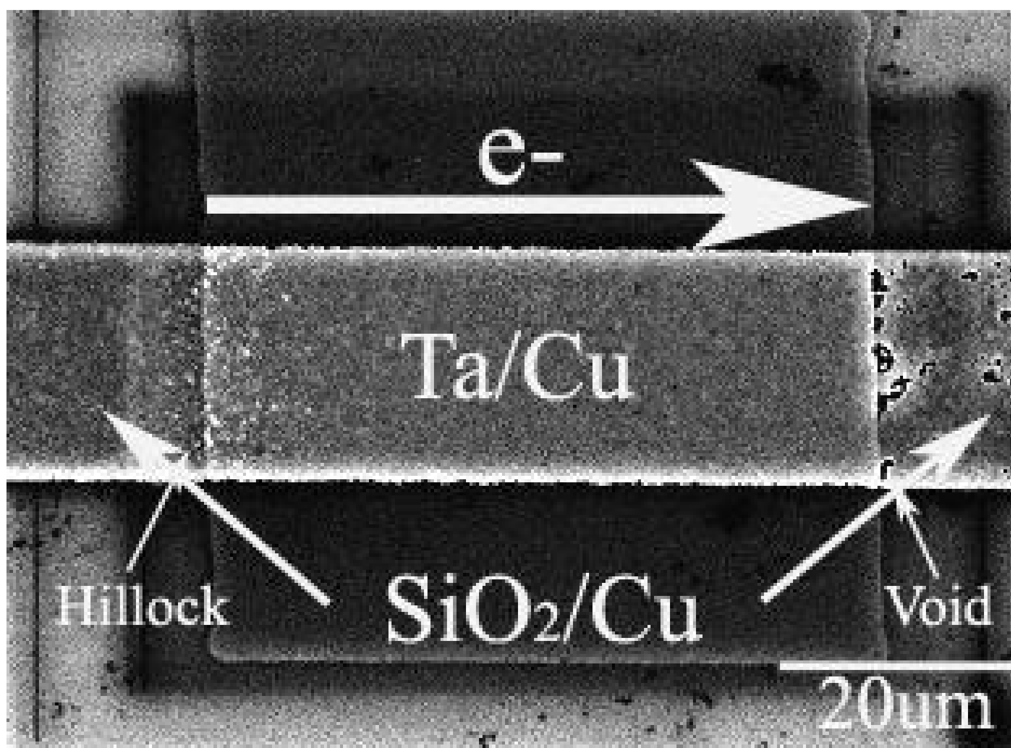


Figure 4.12 SEM image of Ta under cross-strip on SiO_2 after 100 hours test at 270°C, 1.0MA/cm^2 under forming gas ambient

4.3.2.3 Si_3N_4 under layer cross-strip on SiO_2

We also performed EM test on Si_3N_4 under cross-strip on the layer of SiO_2. Figure 4.13 shows the result of EM test for Si_3N_4 under cross-strip on the layer of SiO_2 after 122 hours of EM testing at 270°C, 1.0MA/cm^2 under forming gas ambient. In this experiment, SiO_2 layer was formed using conventional wet oxidation and Si_3N_4 layer was made using sputtering method. The cross-strip area is Si_3N_4/Cu interface and the area of outside cross-strip is SiO_2/Cu interface. It can be seen that voids form at the downstream edge of Si_3N_4 cross-strip while the hillocks are not found to form within EM test conditions used in our study.

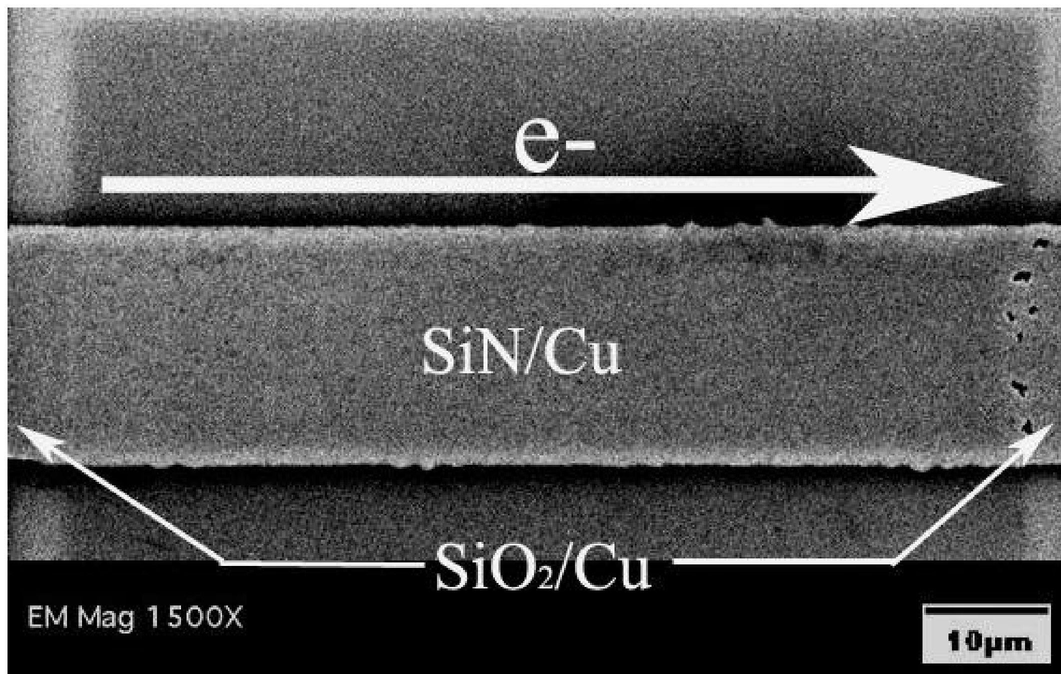


Figure 4.13 SEM image of Si_3N_4 under cross-strip on SiO_2 after 122 hours test at 270°C, 1.0MA/cm^2 under forming gas ambient

The polarity of void formation indicates Si_3N_4 interface has slower EM rate than SiO_2 interface even though it is known that thermal oxidation produces the highest quality of SiO_2.

4.4 Discussion

The EM failure is a complex phenomenon that requires a local divergence of EM flux. While diffusion processes along interface, grain boundaries, and other paths contribute to the overall mass transport, the EM studies in Cu line structures showed that mass transport is dominated by diffusion at interface. Interfacial diffusion refers to atom motion along the interfaces such as between the dielectric/metal (e.g. Si_3N_4/Cu, SiO_2/Cu) or the metal/metal (e.g. Ta/Cu, TaN/Cu, TiN/Cu, Cr/Cu, CoWP/Cu) [67,70-79].

The experiments in this chapter demonstrated that there was a difference interface EM rates between the passivation materials and the dielectric passivation/Cu interface is the weakest interface and the fastest EM path than metallic/Cu interface for Cu interconnect [67,70-79]. It can be assumed that this difference in EM characteristics can be explained by interface quality based on adhesion and suppression of interface diffusivity due to the work of adhesion [67-71]. Both the activation energy of interfacial diffusion and the work of adhesion for the cross-strip passivation material/Cu interfaces are related to bonding strength. Therefore, the interface bonding strength, significantly influencing the interface diffusivity and consequently the mass transport along interfaces, result in different interface EM rates. The weak bonding and the resulting

poor adhesion between Cu and the adjacent material, from which the interface is composed, are the reason for the dominating EM-induced mass transport along the dielectric/Cu interface. The metal-metal bonds have higher adhesion energy (above $40J/m^2$) than the metal-dielectric bonds ($10\sim20J/m^2$) [70-79]. In addition, the poor quality of the interface also can cause more pronounced diffuse scattering of the electron flux at dielectric/Cu interface compared to the metallic cross-strip passivations/Cu interfaces.

The activation energies for EM in Cu lines with dielectric, Ta/TaN and CoWP caps were found to be 0.9-1.0eV, 1.4ev, 1.9-2.4eV, respectively, suggesting that CoWP capping has slower EM rate in Cu interconnects [106]. In this case, the measured activation energy is in good agreement with our double passivation layer cross-strip and under layer cross-strip test results.

In addition, our cross-strip tests for dielectric passivation materials showed that Si_3N_4 passivation seemed to provide interface with slower interface EM than SiO_2. The metal lines passivated in a stiffer dielectric are more reliable than those passivated in a compliant material [107-109]. For a given amount of material transport, a larger stress gradient can be created under a stiffer constraint resulting in greater reduction in atomic flux.

4.5 Summary

The investigation of the interface EM behavior of two different interfaces in Cu is demonstrated in this chapter. Samples with different passivation sequence were

prepared for the purpose of studying the influence of passivation materials on the interface EM behavior. Summarizing all experimental data, Cu EM is dependent on the interface nature and bonding strength.

All the cases in our cross-strip tests, the mass transport along the metallic passivation/Cu interfaces has slower EM rate than the dielectric/Cu interfaces. CoWP passivation provides interface with the slowest interface EM and TaN passivation provides more stable interface with slower interface EM than Ta ($J_{CoWP/Cu} < J_{TaN/Cu} < J_{Ta/Cu}$). In addition, Si_3N_4 passivation seems to provide interface with slower interface EM than SiO_2.

CHAPTER 5

CONCLUSIONS AND RECOMMENDATIONS

5.1 Introduction

The effects of passivation layer on Cu EM were investigated. As a source for atomic flux divergence sites, cross-strip region was introduced into Cu line. Our experiments consisted of comparing the surface EM and interface EM, and also investigating the effects of different passivation layers.

The findings in this study have scientific and engineering implications. A scientific implication is contributed to finding the evidence of active interface EM in Cu and the mechanism of interface EM in Cu thin films. Engineering implication is contributed to finding the best passivation materials with the slowest interface EM.

Section 5.2 summarizes and discusses the significant findings of the results and based on these results, makes suggestions and recommendations that may be of use to those who conduct research on ultra thin Cu interconnects. Finally, section 5.3 suggests some directions for future research.

5.2 Significant Findings and Implications

5.2.1 Single passivation cross-strip test

The role of interface materials on the EM rate at the Cu surface/interface is investigated using simple cross-strip structure. The effect of passivation layer on Cu EM is found to be different from what was originally anticipated. Intuitively, surface has higher mass flow rate than interface, therefore, by adapting passivation layer, it was expected to improve the EM characteristics of Cu. However, the results indicate that the passivation/Cu interface is the most active EM path and EM appears faster at the cross-strip/Cu interface than the unpassivated Cu surface regardless of the metallization method, passivation material, or gas ambient.

The reason that the interface EM is faster than surface EM is unknown, but it is suspected that higher effective charge valence for EM at interface is responsible for faster interface EM than surface EM.

5.2.2 Double passivation and under layer cross-strip test

In our observations, all the cross-stripped passivation materials tested tend to create an interface where EM rate is faster than in surface. In addition, relative difference in EM kinetics and location of marker formation (voids and hillocks) seems to exist; there is the sensitivity of the EM mechanism to the passivation materials.

The investigation of the interface EM behavior of two different interfaces in Cu is demonstrated using double passivation layer cross-strip and under layer cross-strip methods. The metal/Cu interfaces provide the more stable interface where EM rate is

slower than in dielectric/Cu interfaces. CoWP passivation provided interface with the slowest interface EM, and TaN passivation provided more stable interface with slower interface EM than Ta ($J_{CoWP/Cu} < J_{TaN/Cu} < J_{Ta/Cu}$). In addition, Si_3N_4 passivation seemed to provide interface with slower interface EM than SiO_2.

Summarizing all experimental data, Cu EM was dependent on interface nature and bonding strength.

5.2.3 Implications

The results presented in this study clearly indicate that interface EM is the dominant transport mechanism in Cu, which is very sensitive to the nature of the interface. Therefore, it is necessary to choose the best passivation materials for lowest interface EM. Since Cu interface diffusion controls the mass flow, understanding of interface EM and identifying the dominant interface EM path in Cu interconnections are not only important for scientific interest but also it is a critical factor for improving Cu interconnect reliability. Therefore, there is a great interest in devising ways to verify, measure, and ultimately to control, EM along interface.

5.3 Further Research

The mechanism that faster interface EM than surface EM is not completely understood. Therefore, more research is required for verifying the results. The EM mass flow rate is affected by the atomic mobility and EM force linearly dependant on the diffusivity (D) and effective charge valence (Z_w*) for EM force. However, these two

parameters (D and Z_w*) cannot be independently measured. Therefore, one research area is the measurements of diffusivity (D) and electron scattering effect (Z_w*) at surface and interface.

Next research area is investigates the effects of more passivation materials on Cu EM and compare interface EM rates between the two different interfaces.

The EM tests in this study were performed on 20μm wide Cu lines, therefore, the other interesting research area can focus on EM testing on the ultra thin interconnects.

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