IMPACT OF VISCOELASTIC PROPERTIES OF LOW LOSS PRINTED CIRCUIT BOARDS (PCBs) ON RELIABILITY OF WCSP PACKAGES UNDER DROP TEST

by

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ABSTRACT

IMPACT OF VISCOELASTIC PROPERTIES OF LOW LOSS PRINTED CIRCUIT BOARDS (PCBs) ON RELIABILITY OF WCSP PACKAGES UNDER DROP TEST

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Reliability of electronic packages is a major concern as different failure modes are induced due to factors such as temperature loads, mechanical stresses, humidity, corrosion and so on. Finite element analysis (FEA) is often performed to assess reliability under different loading conditions such as thermal cycling, drop testing, power cycling and vibrational loads. Having accurate material property data is one of the key requirements to perform successful FEA study, and a significant amount of time and money is spent to perform accurate material characterizations. Lump modeling approach, where components are represented by a block and assigned effective properties, is commonly used to model printed circuit boards (PCBs) using their elastic properties. However, previous work done by Liu et. al. has shown that viscoelastic properties of PCBs have a direct influence on dynamic characteristics of PCBs under drop impact. In this paper, the viscoelastic properties of PCBs made of low loss materials are characterized and used in finite element analysis to study reliability of wafer level chip scale packages (WCSP) under drop testing conditions. The Wafer-level packaging is one of the advanced modern-day packaging techniques that is popular because it is lighter, smaller and less

expensive. Low loss materials are used for high frequency applications as they provide improved electrical performance and have low dielectric constant. Dynamic mechanical analysis (DMA) measurements are done on PCBs made of Megtron-6 6 (a type of low loss materials) for multiple frequencies and results are used to obtain a master curve for the complex modulus over a wide range of frequency. The master curve is used to obtain Prony series constants that are used in ANSYS Mechanical to perform reliability analysis under drop testing conditions. Using a JEDEC standard, an acceleration pulse of 1500G was applied for a duration of 0.5 ms. The FEA results are used to compare the two cases where PCBs are modeled with and without the inclusion of viscoelastic properties. Results from the FEA simulations are observed to compare deformation, normal strain, total acceleration of the package with and without viscoelastic properties.

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Chapter 1

INTRODUCTION

1.1 Electronic Packages

Integrated Circuits are microelectronic devices which integrates elements such as transistors, resistors, capacitors each with an assigned specific function into an electronic circuit. The primary functions of electronic packages are to power, protect and cool the microelectronic components and enable interconnection between these components and the circuit [1]. Electronic packaging is essential for the better performance and reliability of these microelectronic devices as it protects them from mechanical, thermal, and chemical damage [2]. Some of the major advantages of electronic packages are high speed signaling, accelerated heat dissipation from the device and providing a mechanical housing for the device [3]. According to Moore's law, the integrated circuits are getting smaller with time and the functionality is increasing. This makes it more complex to protect the package as interconnections increase with the increase in transistor density coming from the chip to substrate. The packages can be broadly classified as, [4]

- Through Hole Mount IC Packages
    - Dual in-line Package (DIP)
    - Pin Grid
- Surface Mount IC Packages
    - Quad Flat Package (QFP)
    - Thin small outline package (TSOP)
    - Small outline J-leaded package (SOJ)
    - Ball Grid Array (BGA)

• Chip Scale IC Packages

- Chip Scale Package (CSP)
- Wafer Level
- Stacked Die (2.5D & 3D Packages)

1.2 Wafer level Chip Scale Packages (WCSP packages)

With the increasing trend to use portable and wireless devices and the decrease in the commodity costs of these devices made it necessary to develop much smaller ICs (Integrated Circuit) and system level packages which are less expensive. These factors led to the development of Chip Scale Packages (CSP), Quad-Flat No-lead packages (QFN) and Wafer-level Chip Scale Packages. A chip scale package is defined as a package whose area does not exceed 1.5 times the area of IC it packages, and the perimeter of the package does not exceed 1.2 times the perimeter of chip [1]. Therefore, chip scale packages have advantages owing to their small size over other packages. The comparison in the areas of different packages over the years is shown in the figure 1.1.

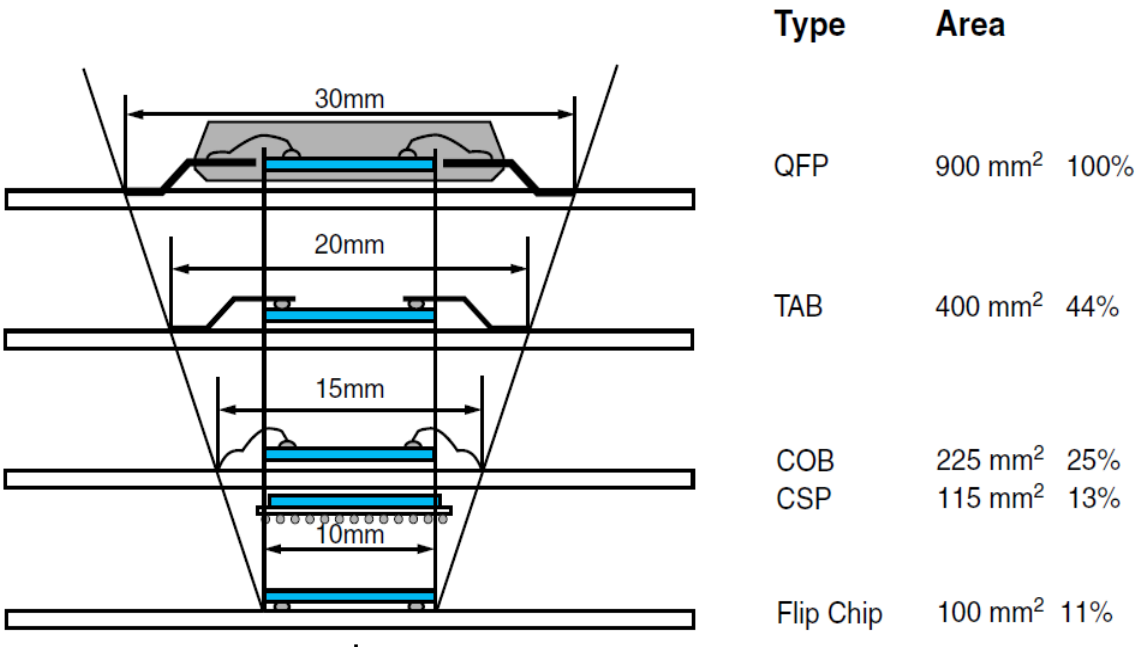

Figure 1.1: Reduction in the size with the evolution of new packages [1].

WCSP packages are the most trending chip scale packages as it uses true chip-scale packaging which is, the package is of the same size as the die. Wafer level chip scale packages are a combination of flip chip packages and chip scale packages, but as the name suggests IC packaging is done at the wafer level in the foundry. The packaging is done in two levels, wafers and singulation of wafers into ICs. Unlike the traditional process of assembling the package of individual unit after the slicing of wafer, the assembly is done at wafer level which saves time and makes it cost effective [5]. Since flip chip technology is used, there is no need for external packaging material to protect the chip [6]. A cross- section of a WCSP package can be seen in figure 1.2.

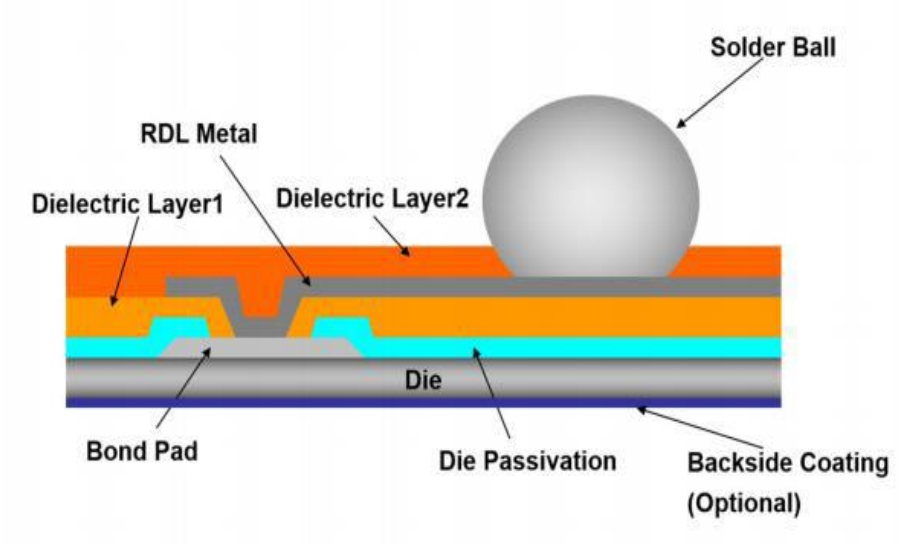

Figure 1.2: Cross-section of a WCSP package [5].

The bare die is processed to have solder balls attached directly to the device which eliminates the need for external casing and wiring. WCSP packages are widely known for its low cost and smallest size. The other advantages of a WCSP package include minimized die to PCB inductance and enhanced thermal conduction characteristics [6].

1.3 Board Level Reliability

The design for reliability is to check if the product functions appropriately and consistently, as reliability is one of the major concerns along with performance, cost, and size of the product. One approach is to, conduct tests on packages after it is designed, fabricated, and assembled. This is expensive and time consuming, hence it is preferable to design the systems packaging up-front for reliability. Board level reliability is an important aspect to ensure the reliability of the package by following certain standard protocols as the package must withstand temperature, shock, vibration while performing its functions [7].

Failure rate when plotted against time, a curve is obtained which is commonly known as “Bathtub curve”. This explains the phases of failures in the life of a product. Three phases are concluded from the curve: infant mortality, useful life and wear-out as seen in the figure 1.3. Infant mortality is the early life fails of the product which usually occurs due to the defects in the fabrication, process, and assembly. The second phase is the useful life of the product and it is almost constant as the poorly manufactured ones are eliminated in the first phase. The wear out phase mainly occurs due to the extensive use of the product for a designated period. The mechanical, electrical, and environmental effects start causing failures at a higher rate.

For example, temperature cycles can induce thermal as well as shear stresses in the solder joints. Shear stresses are induced by in plane thermal expansion due to CTE mismatch between component and the substrate. The external clamping forces and the internal thermomechanical forces causes the warpage of the substrate which induces out of plane tensile peeling forces [8]. Hence, the reliability of a product is to be ensured so that suitable measures are taken to minimize or postpone the failure of the product in wear-out phase [3]. Figure 1.3 shows the bathtub curve which represents the phases of failures in the life of a product.

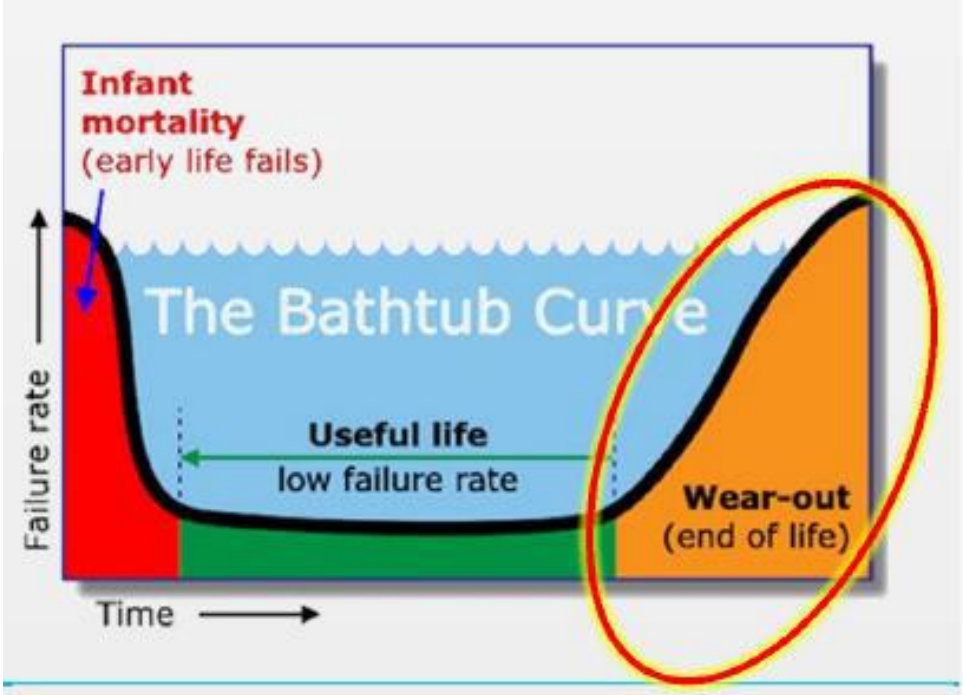

Figure 1.3: Bathtub curve [3].

Some environmental stress tests are conducted to estimate the reliability of the package, the marginalities experienced by the package or the initiations of the failure during the operational life. Few consortiums like Joint Electronic Device Engineering Council (JEDEC) and Institute for Printed Circuit (IPC) have adapted, standardized, and documented many of the reliability tests. As JEDEC standard for drop testing is used in this work, it is discussed in section 1.51.

1.4 Low Loss Materials

The laminate for the PCB is determined based on several factors like circuit fabrication, basic material properties, reliability and end-use performance needs like electrical performance [9]. The rapidly evolving technology in the field of communication and broadband involves high-frequency and high-speed applications. The traditional FR-

4 laminates no longer effectively perform in such applications. The concern for signal transmitting delay increases at high frequency applications and the effect from the signal loss becomes crucial. This resulted in the escalated demand for the use of low loss materials [10]. A picture of a Megtron-6 printed circuit board which is a kind of low loss material is shown in the figure 1.4.

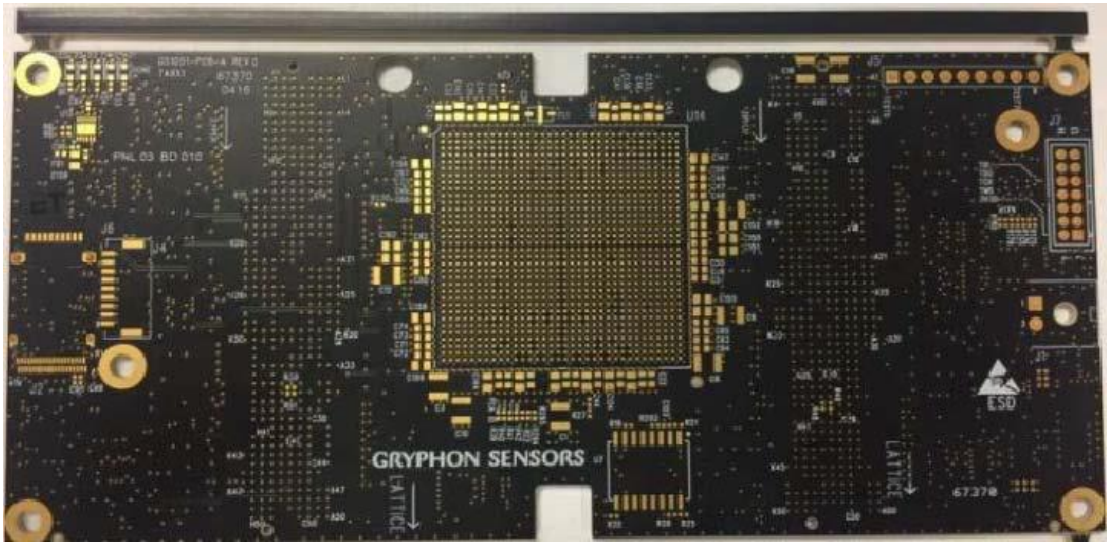

Figure 1.4: A Megtron-6 printed circuit board [2].

Low loss materials have a low dielectric constant which helps in faster transmission of signal and with negligible loss compared to conventional FR-4 materials. They are well-suited for humid environment as they have a low moisture absorption capacity. These materials have a low dissipation factor (Df) and a stable Df characteristic with frequency. They exhibit improved impedance control and better electrical performance in contrast with the traditional FR-4 laminates. Low loss materials or high frequency laminates are more consistent in a thermally dynamic environment as they have a better thermal management quality. They have a high glass transition temperature (Tg) and high

decomposition temperature (Td). Some of the applications of low loss materials is IC testers, high frequency measuring equipment, high speed network equipment. Hence, it is vital to explore the use of these materials to achieve superior performance in an electronic package [9].

1.5 Drop Testing of Electronic Packages

The modern technology is developing rapidly with the inventions of hand-held portable and wireless devices. More often, the goal is to have smaller devices with as many functions as possible [11]. With this increasing trend of using miniature sized devices, the vulnerability of these devices has also increased due to its augmented liability to be prone to drops or experience impact loading. Consequently, it is important to ensure the reliability of package due to mechanical stresses as much as thermal stresses. Due to the drop impact, the exterior of the package experiences a shock and in turn imparts stresses on the interior parts of the package. These mechanical stresses can cause the failure of solder joints which might further cause failure of the entire assembly as solder joints are the vital interconnections of the assembly in a package. The bending of PCB can be observed due to this impact loading. As the PCB bends or deforms after several drops, it may result in loss of contact with other components of the package which might lead to the failure of the entire package. Therefore, it is necessary to avoid this failure with design modifications or by using alternate materials [12].

Product level drop test can be expensive and time-consuming. It also depends on certain factors like design, gripping method etc. which makes it more complex. Hence it can be concluded that board drop level test is more realistic than product level drop test

and is also inexpensive. The factors like board design, construction, thickness, material, interconnect material, component size attribute to the reliability of the package. Since product level testing is a destructive testing, it cannot be further examined by implicating the modifications on the same product. Although, board level drop test also depends on various factors, it gives opportunities to improvement before building the complete product. The board level test considers the input forces acting on the board and does not include product casing. Therefore, the performance of two IC packages are comparable if same inputs and board design are considered [13].

The accuracy of the board level drop tests is decided by friction between the gliding rods and drop table, contact surface and environmental factors. To eliminate these discrepancies, Joint Electronics Device Engineering Council (JEDEC) has standardized the board level drop test in the report JESD22-B111 to evaluate the mechanical reliability by performing Board level drop test reliability on IC packages [14].

1.51 JEDEC condition for Board Level Drop Test (JESD22-B111)

The experimental setup consists of a drop table which has a base plate. The PCB assembly is mounted to the standoffs of the base plate. There is a rigid surface which acts as a strike surface and guide rods that helps in the navigation of drop table during impact. The PCB assembly is mounted to the standoffs using screws at all four corners to prevent its relative motion with the drop table. An accelerometer is mounted on the PCB assembly at or near the support location to characterize output acceleration response of the PCB assembly. The experiment is done with a horizontal orientation with the components facing down in the cause of PCB flexure as shown in the schematic of the experiment setup in figure 1.5.

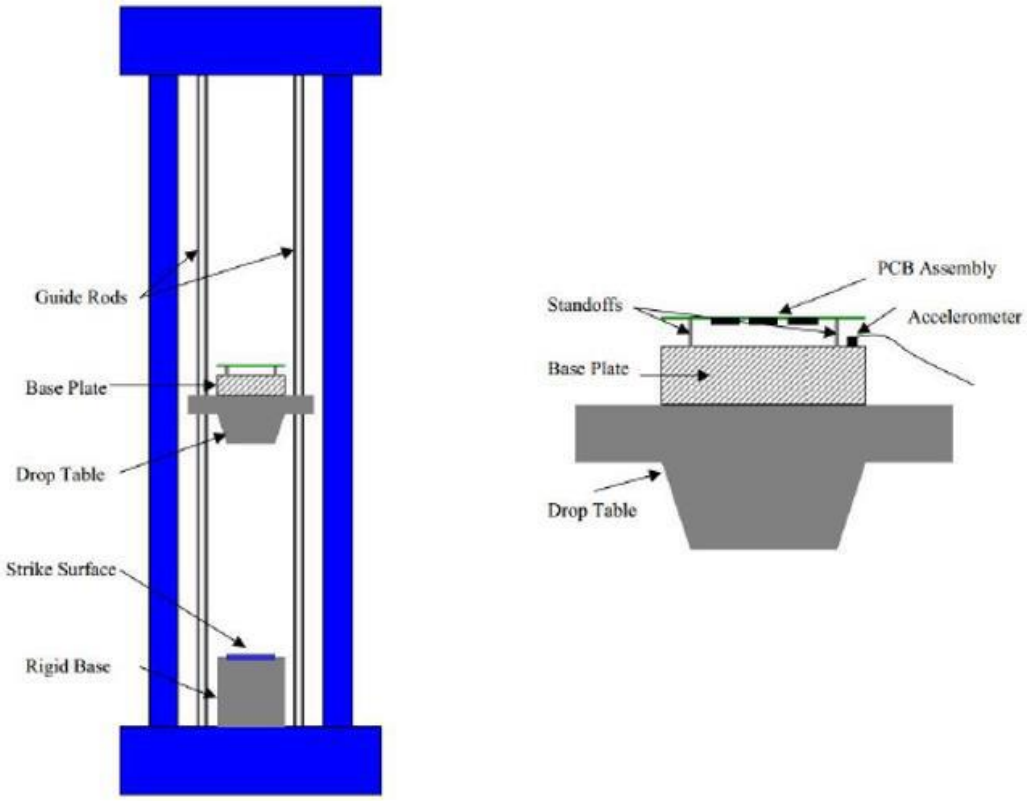

Figure 1.5: A schematic of JEDEC drop experimental setup [15].

Input half sine waves are generated into PCB board with the help of accelerometer for 0.5 ms duration, and drop height is adjusted to achieve 1500G of input acceleration as shown in the figure. Peak acceleration and pulse duration are not only a function of drop height but also strike surface [16] [15]. However, this equation does not include the strike surface effect. Figure 1.6 shows the acceleration load input for a drop test of the board at different instants of time.

$$A(t) = A_o \sin\left(\frac{\pi t}{t_w}\right)$$

$$\sqrt{2gH} = \frac{2A_o}{C}\frac{t_w}{\pi}$$

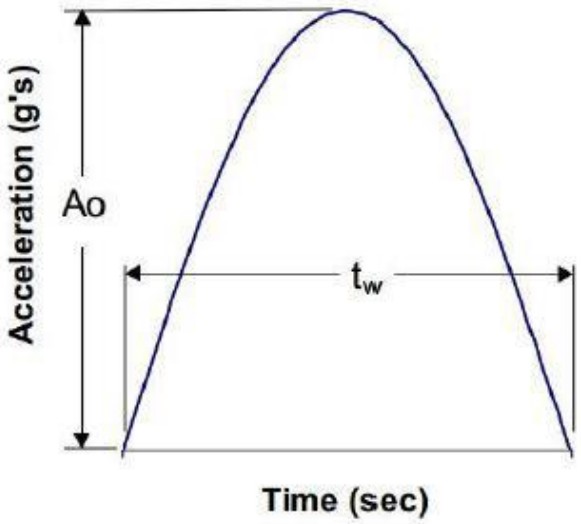

Figure 1.6: Acceleration load input for drop test [15].

Where H is the drop height and C is the re-bound co-efficient (1- no rebound, 2 – full rebound).

1.52 Input G method

The loading conditions for board level drop test in Finite Element Analysis can be assigned in different ways. The most widely used method of applying load conditions is Input G technique proposed by Luan and Tee [17]. Additionally, in these methods the drop table, fixture, contact surface, and friction of guiding rods are not simulated, however their effects are considered to generate impact pulse. So, input acceleration 1500G given to board-package assembly for the duration of 0.4ms under a drop height of 1.5m to simulate experimental input impact pulse. The simple experimental methodology of input G method reduces the computational time for same element mesh size of PCB and package in finite element modelling. The dynamic loads are applied on the bottom face

of the package in the direction as shown in the figure 1.7 as this side is most susceptible to failure.

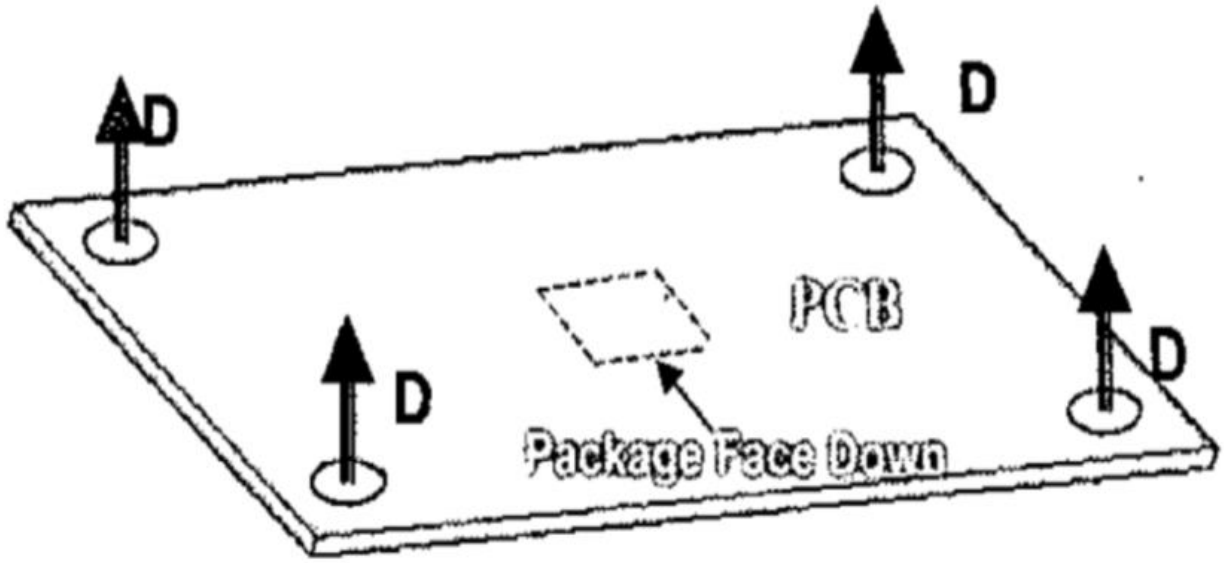

Figure 1.7: Schematic of experimental setup of Input G method [17].

Chapter 2

MOTIVATION AND OBJECTIVE

The work from Liu et.al. analytically proves that the viscoelastic properties of the PCB have direct influence on the dynamic characteristics under drop impact. This states that modeling the PCB as linear elastic in the computational analysis for the reliability of package is not completely accurate as viscoelastic properties might have an impact on the results. As the PCB is primarily made of macromolecules which are typical viscoelastic materials, it is realistic to model the PCB as viscoelastic for computational analysis [18]. Also, from the above sections, its known that low loss PCBs have a superior electric performance and capable of replacing the traditional FR-4 laminates in high frequency and high-speed network applications. This necessitates the need to check for the reliability of low loss PCBs to further validate their use. Due to multiple function integration on portable handheld devices, miniaturization of handheld devices has become a trend which increases its vulnerability under impact loading [19]. The microelectronic assemblies are subjected to shocks and vibration loads during manufacturing, transportation, and end use. Therefore, in this work, reliability of WCSP package is analyzed under drop impact when low loss PCBs are used.

The objective of the work is to model the PCBs in two different ways, one as orthotropic linear elastic and other as orthotropic linear viscoelastic. The drop test of WCSP packages is done for the two different cases of PCB modeling and computational results are compared. The attempt is made to conclude whether the inclusion of viscoelastic properties in modeling of low loss PCBs have an impact on the reliability of WCSP package under drop test.

Chapter 3

LITERATURE REVIEW

Fang Liu studied about the impact of viscoelasticity of PCB on its dynamic characteristics under drop impact. The work models the PCB as a plate and a beam and evaluates the impact of viscoelastic properties. It summarizes that when a PCB under drop impact is modeled as a plate or a beam, if the dynamic viscosity of the substrate increases, then their damping coefficients rise. Also, the deflection response becomes smaller and the acceleration could reduce faster during drop impact. The work concludes that the drop impact reliability can be increased by choosing a PCB material with greater material viscosity and also reducing the size of the PCB accordingly [18].

Kasireddy's thesis work has discussed about the impact of viscoelastic modeling of FR-4 PCBs in WCSP packages under drop test. The author compared the results of elastic FR-4 PCB model and viscoelastic FR-4 PCB model under impact loading. According to this work, the total deformation, normal stress, and peeling stresses are significantly higher in elastic model compared to viscoelastic model, thus indicating the importance of viscoelastic properties in PCB modeling [12].

Chaudhari has studied the reliability of BGA package under thermal cycling using different kinds of PCBs. Low loss materials like Megtron-6 series boards were used in this work in contrast with conventional FR-4 laminates and the results were compared. It was seen that the package with FR-4 laminates deformed more than the package with Megtron-6 boards. The work concluded that the Megtron-6 boards or high frequency laminates used in the work was more reliable and durable than FR-4 laminates in a BGA package under thermal cycling load [20] [2].

Pallapothu's thesis work explores the reliability of high frequency laminates over FR-4 PCBs in a BGA package when power cycling is done. Material characterization is done to obtain the material properties of Megtron-6 6 board, and it is used in the computational analysis. Transient thermal analysis and static structural analysis is done to evaluate reliability under power cycling. Total deformation, maximum accumulated plastic work per cycle and number of cycles to failure of Megtron-6 series boards and FR-4 laminates were compared. Most of the Megtron-6 series boards showed better performance and had less number of cycles to failure [21] [22].

Mundhe's work shows that Megtron-6 boards are better than FR-4 laminates in the reliability of BGA package under drop impact. Megtron-6 6 boards showed significantly superior reliability when total deformation, equivalent strain, and peeling stresses of the package were observed [23]. Denria et. al studied about the reliability of low loss materials when both power cycling and thermal cycling loads are applied. An octant symmetric BGA model was used for the computational analysis and Megtron-6 6 board had a 11.11% less total deformation and 49.74% more durability compared to the traditional FR-4 board [24].

Anaskure's work studied about the viscoelastic behavior of the FR-4 laminates over elastic modeling in thermal cycling of a WCSP package. The study includes material characterization of FR-4 PCBs using DMA to get the viscoelastic properties. According to this study, viscoelastic model took lower number of cycles to failure compared to orthotropic elastic model. This accentuates the inclusion of viscoelastic properties of PCB for more accurate results in the computational analysis [25] [26].

Chapter 4

MATERIALS AND METHODS

The material properties of the board are characterized, and they are used in the Finite Element Analysis of the model. It is decisive to characterize the board for their realistic material properties to have more accurate results in the analysis. Therefore, the coefficient of thermal expansion is measured by testing the board on a Thermomechanical Analyzer (TMA). The modulus of the board is characterized by testing it on a Dynamic Mechanical Analyzer (DMA).

4.1 Thermomechanical Analyzer (TMA)

4.1.1 Coefficient of Thermal Expansion (CTE)

The rate at which the material expands with the change in temperature is called co-efficient of thermal expansion. It can also be defined as the ratio of the fractional change in length of the sample to the change in its temperature. It is denoted by α (/°C).

$$\alpha = \frac{\epsilon}{\Delta T}$$

Where, ϵ = strain of the sample(mm/mm); ΔT= change in temperature (°C).

Thermomechanical Analyzer consists of a thermal chamber which heats the sample placed in a sample cylinder. A negligible load is applied on the sample to ensure proper contact with the probe throughout the test. A LVDT sensor is present in the equipment which detects the varying position of the probe with the expansion of the

sample [27] [28]. It consists of a thermocouple to record temperature data at any instant of time. Figure 4.1 shows the schematic of a TMA with the parts of the equipment labeled.

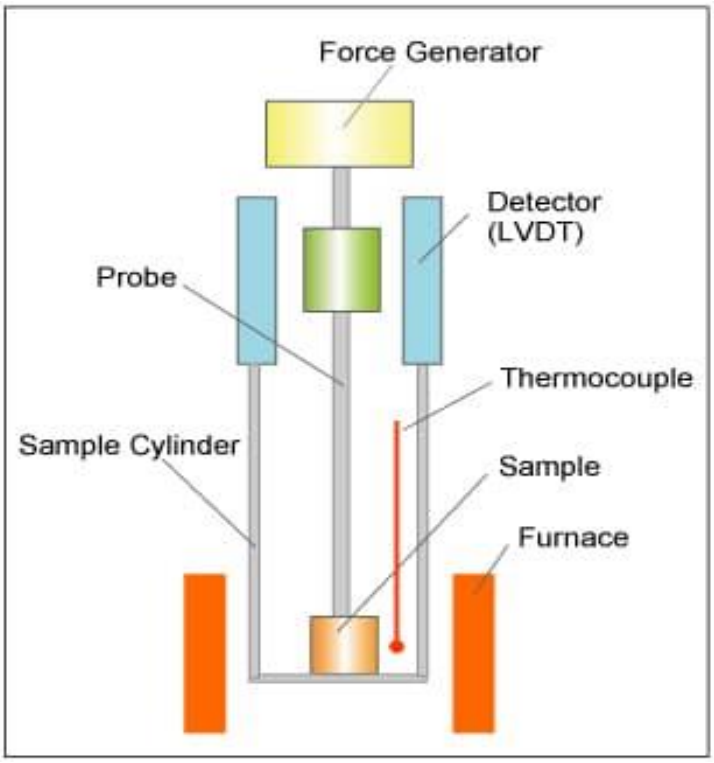

Figure 4.1: Schematic of a TMA [29].

The samples were cut to a dimension of 8 mm x 8 mm using a high-speed cutter and were thoroughly cleaned using ethanol. The tests were done for a temperature range of 25°C to 200°C at a ramp rate of 2°C/min. Both in-plane and out of plane CTEs were measured by changing the orientation of the sample in the sample cylinder [30]. Three tests were done for both in-plane and out of plane CTE with different samples and the average value was calculated. Figure 4.2 shows the Thermomechanical Analyzer used in this study.

Figure 4.2: Thermomechanical Analyzer used in this study.

The CTE values obtained from the TMA data are in the table below. The CTE values were classified into two different ranges based on the glass transition temperature as shown in Table 1.

Table 1: CTE values of Megtron-6 PCB obtained from TMA test.

Temperature	CTE (ppm/°C)		
	X	Y	Z
<Tg	14.8	14.8	53.9
>Tg	4.65	4.65	251.2

4.2 Dynamic Mechanical Analyzer (DMA)

4.2.1 Young's Modulus:

Young's Modulus or Tensile Modulus or Modulus of Elasticity is the measure of the stiffness of the PCB. It can also be defined as the ratio of stress to strain in a direction. The lesser the deformation, the stiffer the PCB in that direction. It is denoted by E (Pa). Complex modulus is compared to Young's modulus and is calculated as given by the following relation:

$$E^* = \sqrt{E'^2 + E''^2}$$

Where, E^*- Complex Modulus (Pa); E'- Storage Modulus (Pa); E''- Loss Modulus (Pa).

4.2.2 Storage Modulus

It is the measure of the stored energy and this represents the elastic part of the material. It is denoted by E''.

4.2.3 Loss Modulus

It is the measure of the energy dissipated as heat and it represents the viscoelastic part of the material. It is denoted by E'.

4.2.4 Glass transition temperature (Tg):

The temperature at which the polymer chains become more mobile and there is transition of the PCB substrate from a glassy rigid state to a rubbery deformable state. The original properties are regained once the PCB goes back to room temperature.

The glass transition temperature is not one exact temperature point for a material, the value varies with the test conducted to analyze the Tg. There are three ways to

deduce Tg from the DMA data on the software TA7000. Tg can be the drop in the storage modulus, the peak of loss modulus or the peak of the tanD data. The viscoelastic properties come into picture at temperatures greater than Tg. In this work, the glass transition temperature was deduced with respect to storage modulus to increase the possibility of getting viscoelastic data for a wider range of temperature.

DMA measures the mechanical properties of the material as a function of time, temperature, and frequency. The LVDT sensor detects the position of the sample as it deforms with respect to the sinusoidal load applied by the force generator. DMA measures the storage modulus, loss modulus and tanD as a function of time, temperature, and frequency [31]. Complex modulus and glass transition temperature is deduced from this data. Figure 4.3 shows the schematic of a Dynamic Mechanical Analyzer.

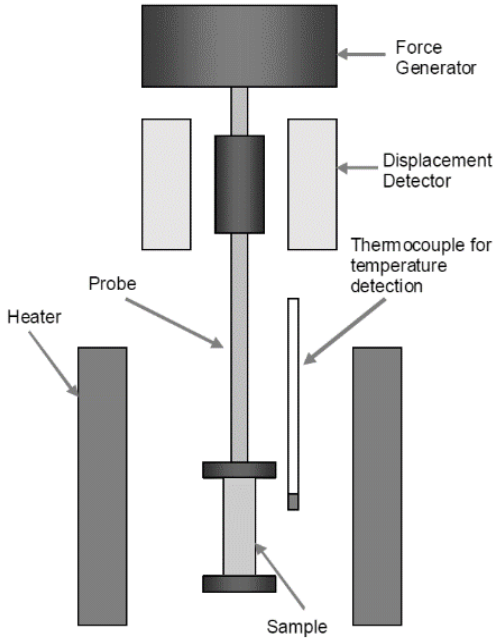

Figure 4.3: Schematic of a DMA [32].

The samples were cut to dimension of 50mm in length and 8mm in width with a high-speed cutter and cleaned thoroughly with ethanol to remove the dust particles. Owing to the hardness of Megtron-6 board, the bending attachment which uses dual-cantilever beam principle was used. The test was conducted for a temperature range of 25°C to 220°C at a ramp rate of 2°C/min. A maximum bending force of 2000mN was selected. Five different frequencies 0.5, 1, 2, 5 and 10 Hz were selected for the test in order to create master curve. The modulus of the Megtron-6 board was found to be 12.7 GPa and the glass transition temperature was measured to be 169.7°C from the DMA test. Figure 4.4 shows the Dynamic Mechanical Analyzer used in this study.

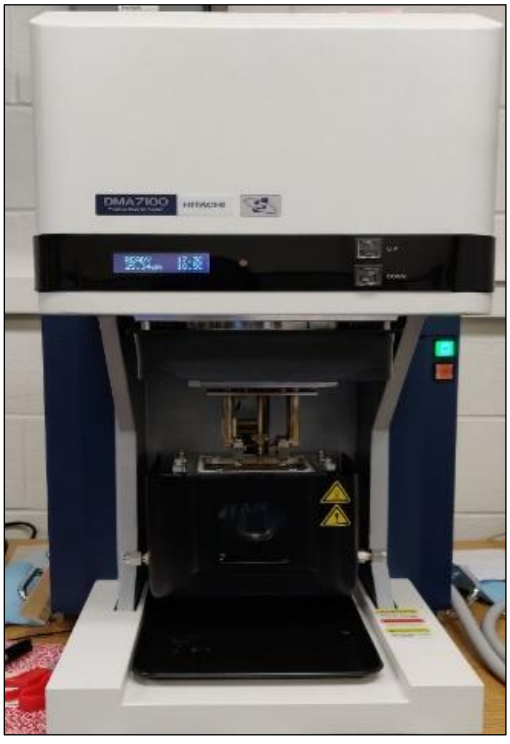

Figure 4.4: Dynamic Mechanical Analyzer used in the study.

4.3 Master Curve

The time-temperature superposition principle explains the relation between temperature and frequency dependency of the dynamic viscoelastic data. Using this principle, the temperature changes can be converted to frequency dependency of the viscoelastic properties at a given temperature. The modulus data obtained from the DMA test for several frequencies can be extrapolated to a wide range of frequencies at a given temperature by creating a master curve. This frequency dependency of viscoelastic properties can be shifted to a different reference temperature using WLF shift functions.

Williams-Landel-Ferry function or WLF shift functions for creating master curve is given by the following equation,

$$\log\big(a(T)\big) = \frac{C_1(T - T_R)}{C_2 + (T - T_R)}$$

Where, C_1 and C_2 are constants, T_R is the reference temperature [33]. The disadvantage of WLF shift function is, it holds good when the reference temperature is only several tens of degrees above the Tg and not for temperatures less than the Tg. In this work, master curve was created for every 10°C from 160°C to 200°C. TA7000 software has an inbuilt function to create master curve which uses WLF shift function and auto generates the constants C_1 and C_2. Figure 4.5 shows master curve created at 170°C for which C_1= 16 and C_2= 88 was used in the WLF function. The frequency ranges from 6.9E-08 to 1.5E+04 in the master curve shown in Figure 4.5.

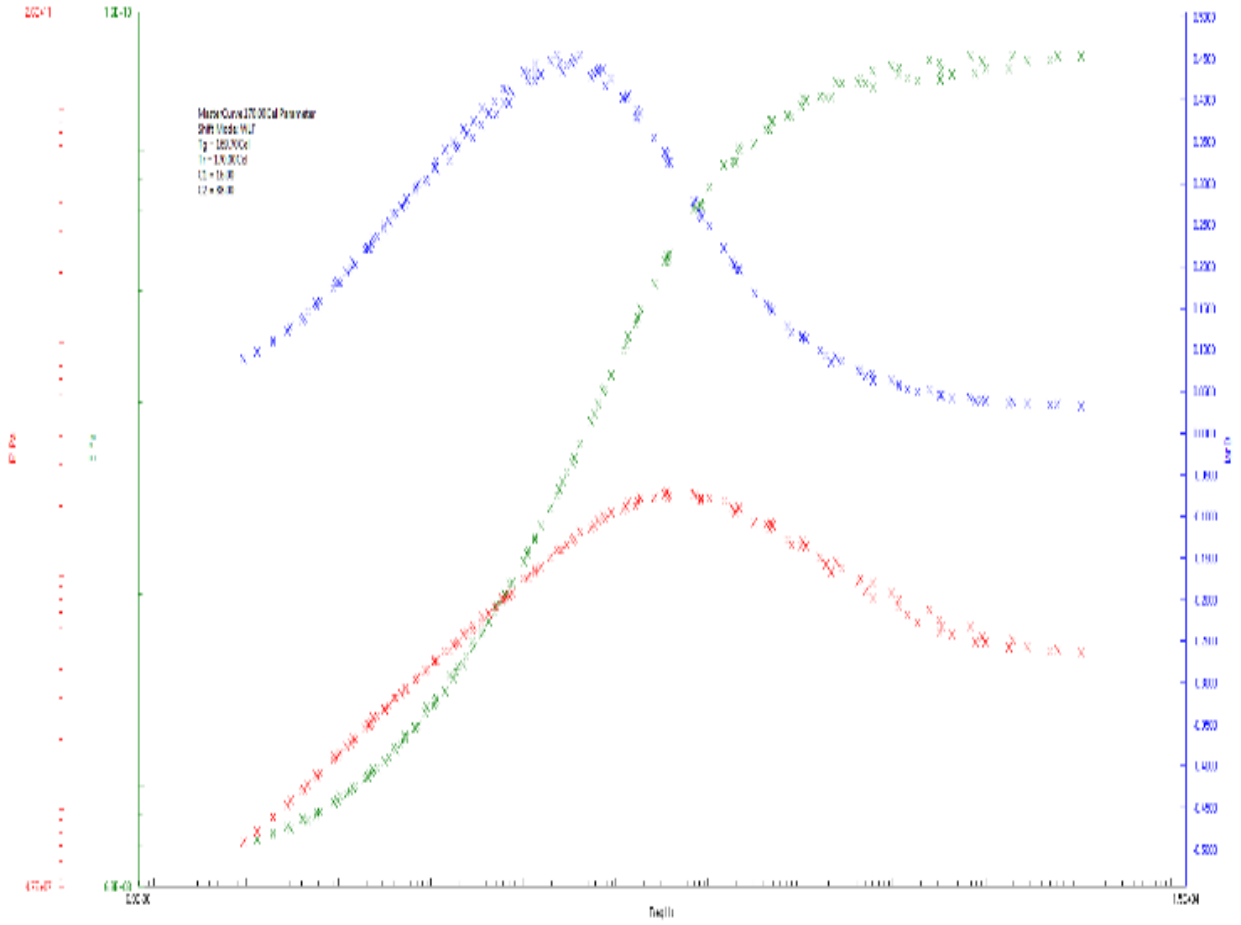

Figure 4.5: Matser curve of Megtron-6 PCB created at 170℃.

4.4 Prony Series Representation of Linear Viscoelasticity

The linear viscoelastic properties of a material can be represented by Prony Series. Maxwell model consists of linearly elastic hook springs and linearly ideal viscous Newtonian dampers connected in series. The total strain is the summation of strain in elastic and viscous elements [34]. In this work, Prony series representation given by generalized Maxwell model which consists of a spring and K Maxwell elements in parallel is used which is given by the equation,

$$E(t) = E_\infty + \sum_{k=1}^{K} E_k e^{-t/\tau_k}$$

Where, E_∞- modulus at equilibrium; E_k- relaxation moduli; τ_k- relaxation time [35]. E_k and τ_k are together called as Prony series constants. Prony series constants are used as the input for viscoelastic properties of a material in ANSYS Workbench.

The data from Master curve was imported to ORIGINPRO software. A non-linear curve fitting option was used to fit the data to the above equation in order to get the prony series constants. A R^2 value of 99.92 was achieved and the fit was 100% successful. The prony series constants calculated at different temperatures are given in the Table 2.

Table 2: Prony series constants at different temperatures.

	160°C	170°C	180°C	190°C	200°C
α1	0.0438	0.0234	0.0438	0.0234	0.0438
α2	0.0672	0.0327	0.0672	0.0327	0.0672
α3	0.1134	0.0701	0.1134	0.0700	0.1135
α4	0.1759	0.1191	0.1759	0.1190	0.1759
α5	0.1969	0.1929	0.1969	0.1927	0.1969
α6	0.1543	0.2182	0.1543	0.2181	0.1543
α7	0.0924	0.1463	0.0924	0.1463	0.0924
α8	0.0503	0.0758	0.0504	0.0759	0.0503
α9	0.0306	0.0414	0.0306	0.0415	0.0306
α10	0.0155	0.0201	0.0155	0.0202	0.0155
τ1	1.55E-02	2.01E-02	1.55E-02	2.02E-02	1.55E-02
τ2	7.59E-01	1.55E-03	1.67E-04	1.76E-06	6.31E-07

$\tau 3$	2.22E+01	1.09E-02	4.87E-03	1.23E-05	1.85E-05
$\tau 4$	1.31E+02	2.29E-01	2.87E-02	2.60E-04	1.09E-04
$\tau 5$	6.25E+02	1.36E+00	1.37E-01	1.54E-03	5.20E-04
$\tau 6$	2.62E+03	6.84E+00	5.74E-01	7.75E-03	2.17E-03
$\tau 7$	1.03E+04	3.30E+01	2.26E+00	3.74E-02	8.57E-03
$\tau 8$	4.46E+04	1.63E+02	9.78E+00	1.85E-01	3.71E-02
$\tau 9$	2.24E+05	9.21E+02	4.91E+01	1.04E+00	1.86E-01
$\tau 10$	1.30E+06	6.63E+03	2.86E+02	7.47E+00	1.08E+00

To validate the constants obtained from the OriginPro curve fitting, the modulus values were calculated using the prony series constants. The calculated modulus values were plotted together with measured modulus values from DMA test against frequency. A good match was observed between the measured modulus values and the calculated modulus values which validates the prony series constants obtained by fitting the master curve data on the prony series equation. Figure 4.6, 4.7, 4.8 shows the plot of calculated and measured storage modulus, loss modulus, complex modulus against frequency respectively.

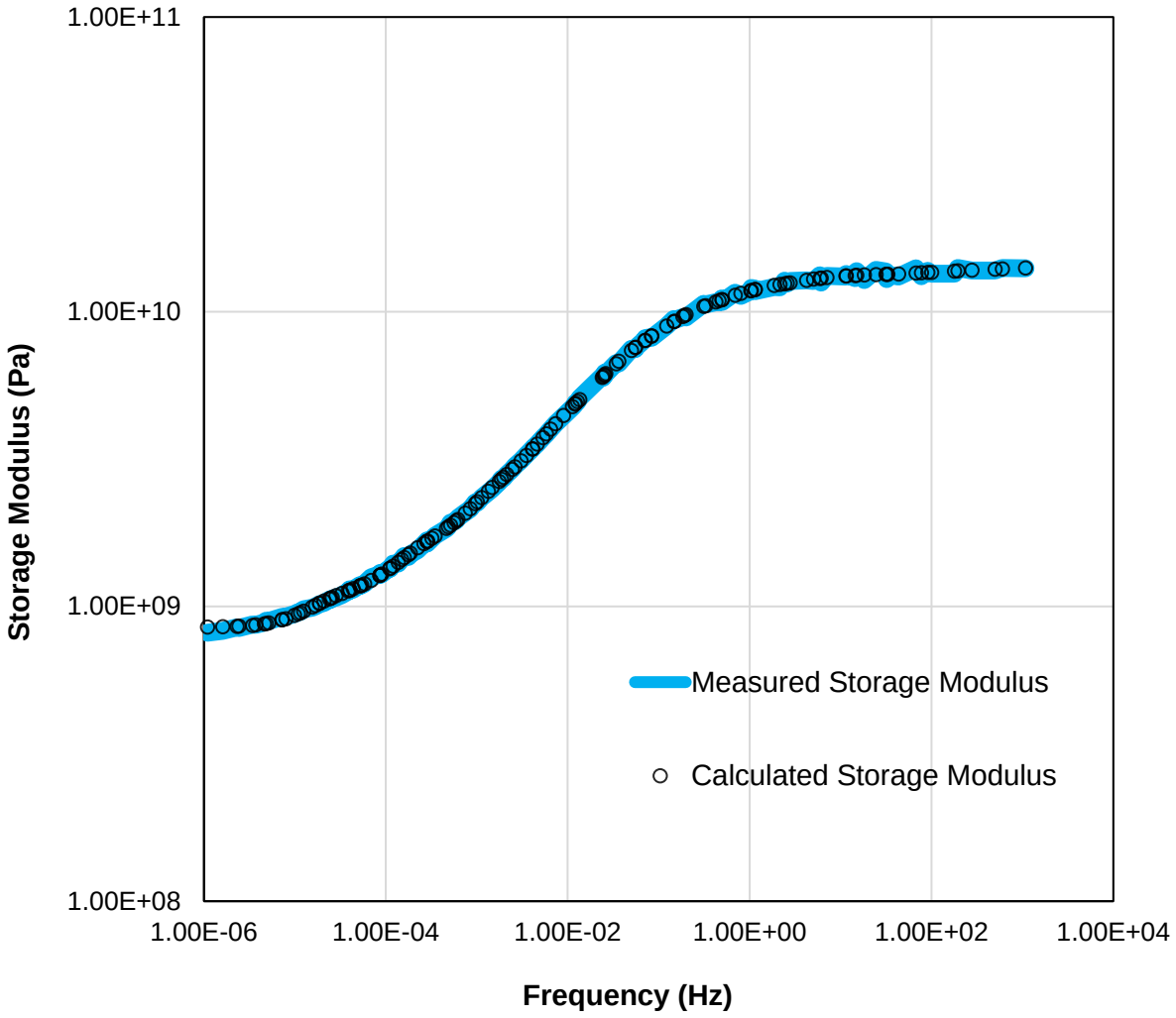

Figure 4.6: Measured and calculated storage modulus Vs Frequency at 170°C.

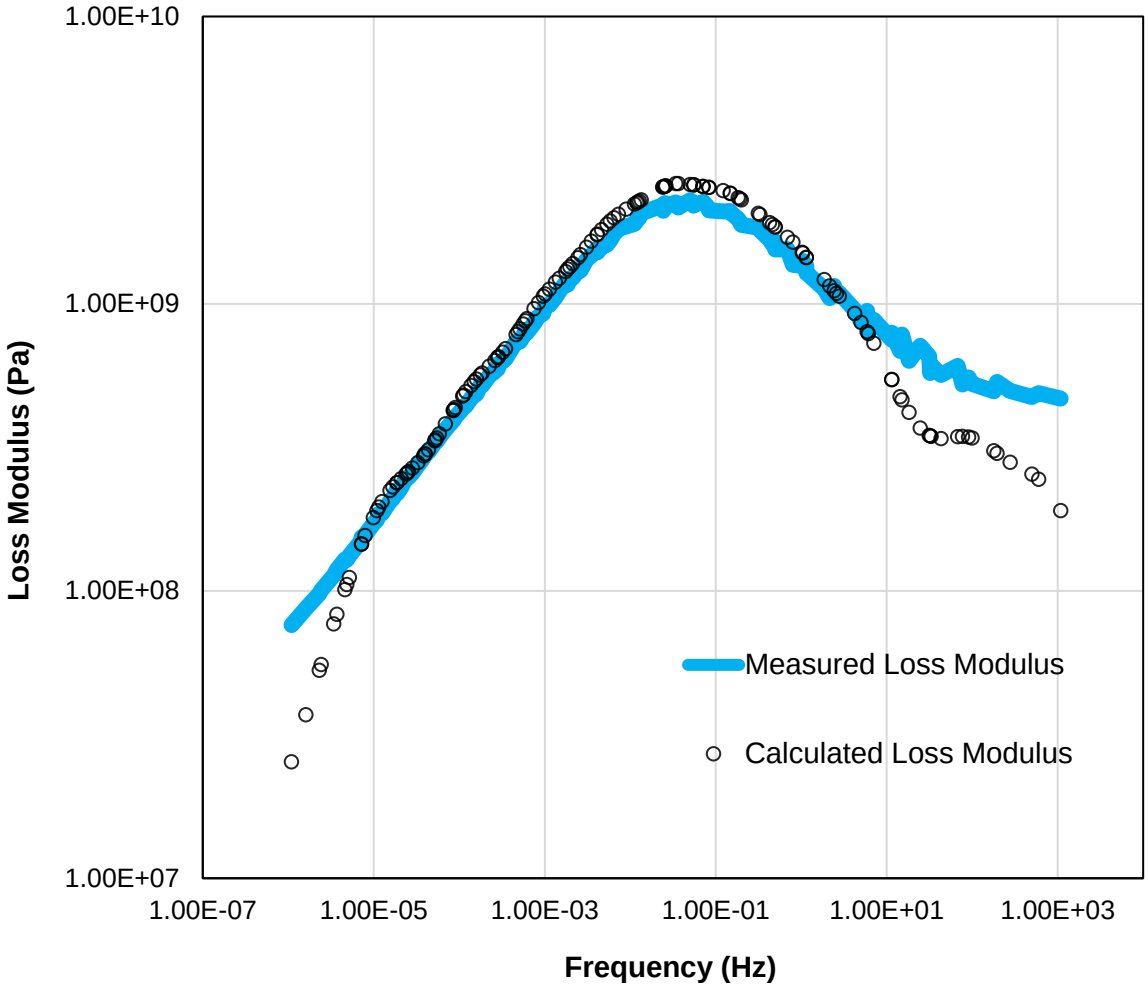

Figure 4.7: Measured and calculated loss modulus Vs Frequency at 170°C.

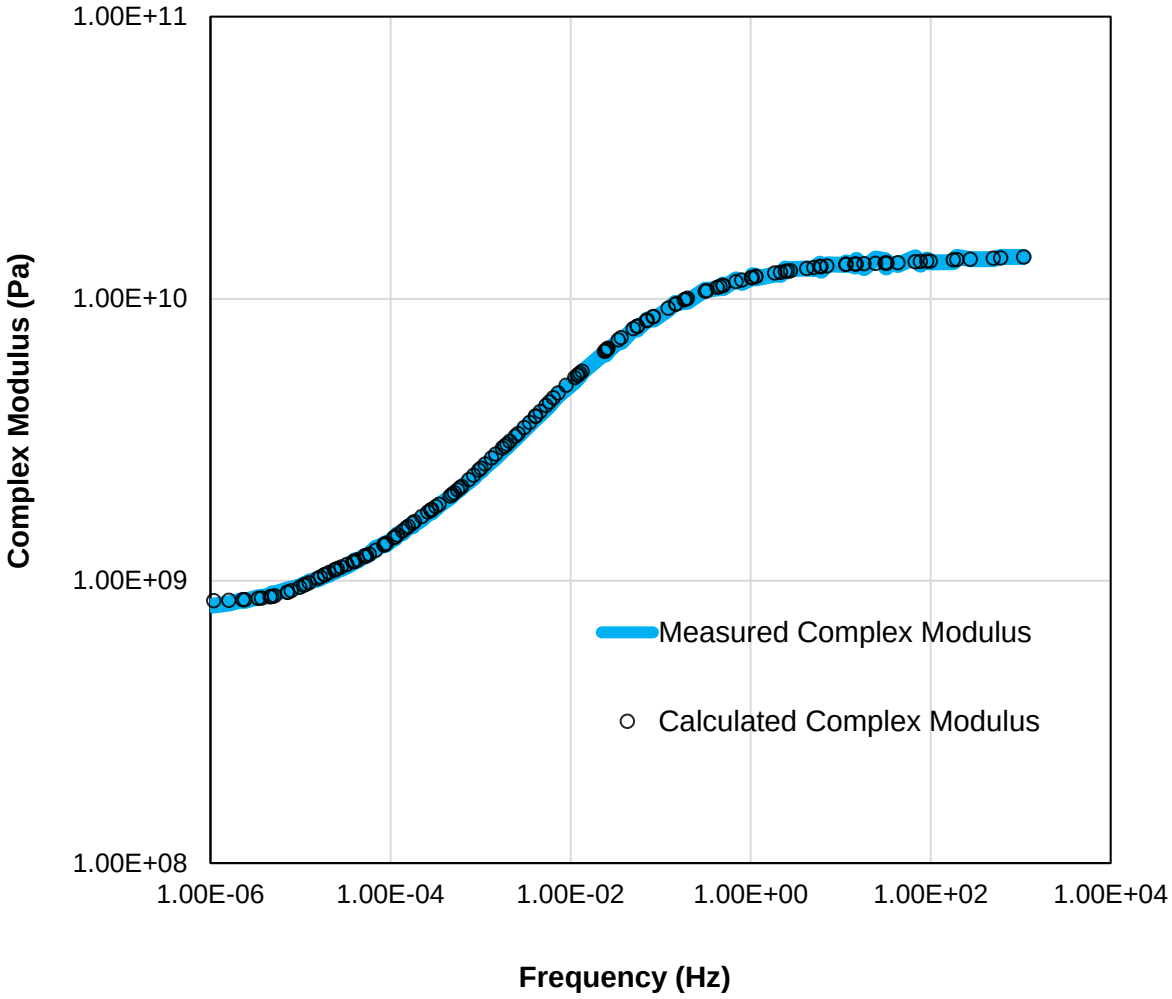

Figure 4.8: Measured and calculated complex modulus Vs Frequency at 170°C.

Chapter 5

FINITE ELEMENT ANALYSIS

5.1 Introduction to FEA

Finite Element Analysis is a logical and inexpensive computational approach used to solve engineering problems. Analysis in thermal, structural, fluid, hydraulics, electromagnetics, bio medical, nuclear engineering and so on can be done using FEA. It has numerous advantages like precise dimensions in the construction or geometry, allowance to have multiple options for material problems and it can be analyzed one at a time. It is inexpensive because the testing does not involve the actual product but only its material properties and geometry. Also, if the tests must be repeated with some modifications or with some experimentations, it can be done easily and simultaneously on FEA [2].

Finite Element Method works on a principle in which it divides the component into smaller elements with 3 to 4 nodes. Polynomial interpolation is used to find the displacement of these nodes. The load or force is replaced by the equivalent system of forces at each node. The governing equation is as follows.

$$[F] = [K] * \{u\}$$

Where, $[F]$ is the force vector, $[K]$ is global stiffness matrix, $\{u\}$ is the nodal displacement. The global stiffness matrix depends on the material properties and geometry of the object. The force vector depends on the boundary conditions and the loading conditions along with the direction of the load applied. The displacement of nodes is obtained by mathematically solving in the software.

Finite Element Method solves in parts for each node and element and combines the result to generate the result for the entire body. Usually a problem on FEA is solved in three steps, Preprocessing, solution, post-processing. In the preprocessing step, the geometry of the model is created with precise dimensions and material properties are assigned to all parts of the body. Further the body is divided into nodes and smaller elements by creating mesh. In solution step, boundary conditions and loading conditions are applied to the body. The output and load step control are selected, and solution is obtained. In the post processing step results are reviewed and analyzed [2].

Therefore, any computational analysis involves these important steps:

1) Modeling and geometry
2) Material properties
3) Meshing
4) Boundary conditions and Loading
5) Solution and Results

5.2 Modeling

Depending on the speed and accuracy needed in the computational analysis, PCB modeling is done in three different ways [36].

1) Lumped board properties approach:
    - Orthotropic for in-plane and normal directions are assigned
    - Commonly used for system-level analysis where board performance is not the primary concern

- Solve time is reduced due to significantly less mesh count

2) Explicit Geometry approach:

- Detailed modeling including geometry of traces and vias is done
- Long solution times due to very high mesh count
- More accurate results
- Usually used when board performance is the primary focus

3) ECAD approach:

- Importing an ECAD file is necessary which is not easily available
- Mapping of metal fraction in each layer is done using ECAD data
- High accurate results can be achieved with relatively faster solution time

There are some assumptions made in the modeling of WCSP package in this work. The PCB is generally assumed to be orthotropic and linearly elastic according to lumped board properties approach. However, the motivation of this work is to check if the viscoelastic properties of PCB have an impact on the dynamic characteristics. The Low loss PCB is modeled in two different ways for computational analysis. The best and accurate way of modeling Low loss PCB can be determined by comparing the results of computational analysis for these two cases. For the first case, the Megtron-6 PCB or Low loss PCB was modeled as orthotropic and linear elastic and for the second case the PCB was modeled to be orthotropic and linear viscoelastic [37].

5.3 Material Properties and Geometry

A full model of the board with dimensions 66 mm x 38.5 mm x 1 mm is cut into quarter to reduce the simulation time [38] [39]. A package with dimensions of 2.5 mm x 2.5 mm

was used. An array of 7 x 7 solder balls was modelled on each package. The solder balls were modeled according to the Anand's Viscoplastic model SAC-396 [40] [41]. The main objective of the work is to compare the results for elastic modeling of Low loss PCB and viscoelastic modeling of PCB, and not to obtain the component failure or failure location. Therefore, the solder balls were modeled as rectangular blocks with dimensions 0.14mm x 0.14mm and a thickness of 0.22 mm to reduce the complexity in modeling. Anand's viscoplastic constants given in Table 3 were used in the modeling of the solder balls. Other materials like die, mold compounds, solder mask, copper pads were assumed as elastic. The material properties were used for the above-mentioned materials are shown in Table 4 [42].

Table 3: Anand's viscoplastic constants for modeling SAC-396 solder balls [41].

Constant	Name	Value	Unit
s_0	Initial Deformation Resistance	3.3	MPa
Q/R	Activation energy/Universal gas constant	9883	1/K
A	Pre-exponential factor	1.57×10^7	1/sec
$\boldsymbol{\xi}$	Multiplier of stress	1.06	Dimensionless
m	Strain rate sensitivity	0.3686	Dimensionless
h_0	Hardening constant	1077	MPa
$\hat{s}$	Coefficient of Deformation Resistance Saturation	3.15	MPa

n	Strain rate sensitivity of the saturation value of the deformation resistance	0.0352	Dimensionless
a	Strain rate sensitivity of the hardening process	1.6832	Dimensionless

Table 4: Material properties of the other components in the package [42].

Material	E (GPa)	CTE (ppm/ °C)	v
Die	131	3	0.28
RDL	130	16.8	0.34
Polyamide	1.2	52	0.25
Mold	24	20	0.30
Cu Pads	110	17	0.34
Solder Mask	4	30	0.40

5.4 Meshing of the model

The board where package is present was finely meshed, and the rest of the board was coarsely meshed. Measures were taken to have at least two elements through thickness even in the thin components like solder mask. Mesh sensitivity was done and the optimized mesh with 621,651 nodes and 131,982 elements was selected. Figure 5.1 shows the meshed quarter symmetric model of WCSP package used in the analysis.

Figure 5.2 shows fine meshing of the board and the components where package is present.

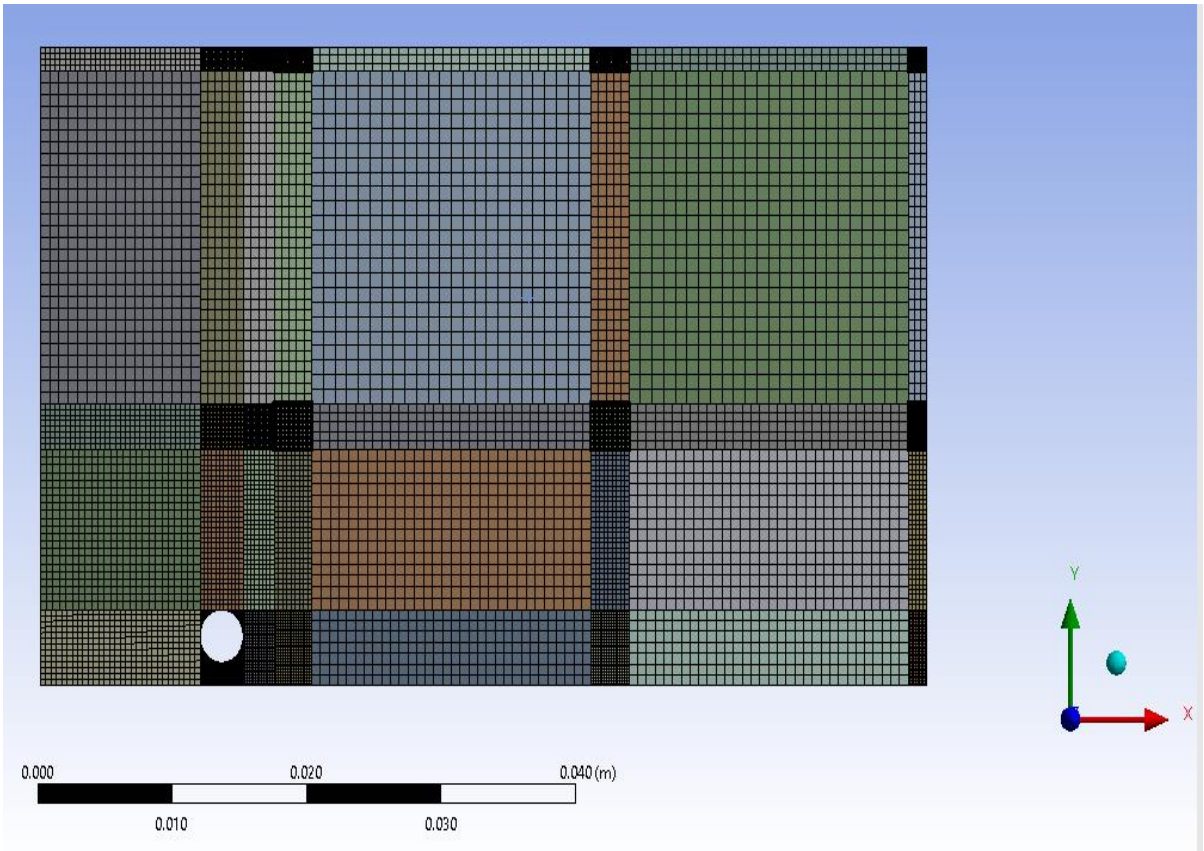

Figure 5.1: Meshed quarter symmetric model of WCSP package.

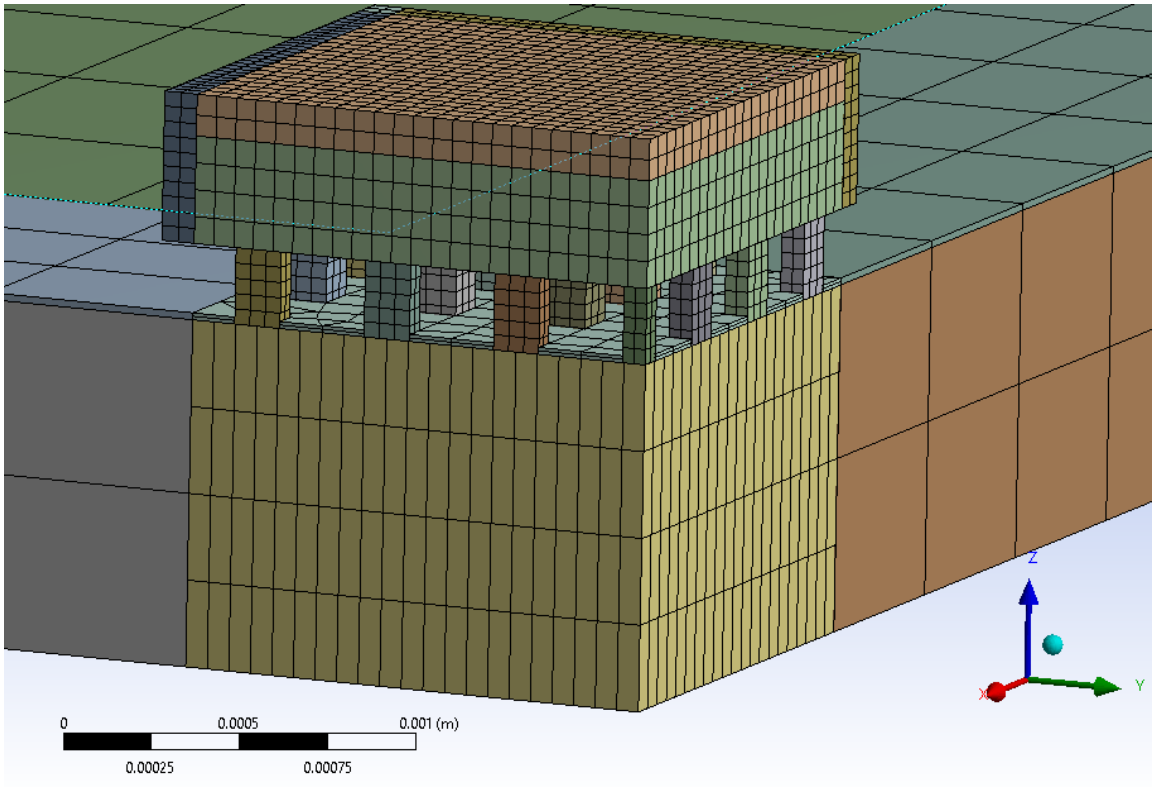

Figure 5.2: Fine meshing on the package.

5.5 Boundary Conditions

The boundary conditions applied for the model in the transient structural analysis were as follows:

(i) The corner node was fixed to avoid the rigid body movement during analysis

(ii) The symmetric faces were given frictionless boundary conditions

Figure 5.3 shows the boundary conditions applied to the respective node and the faces.

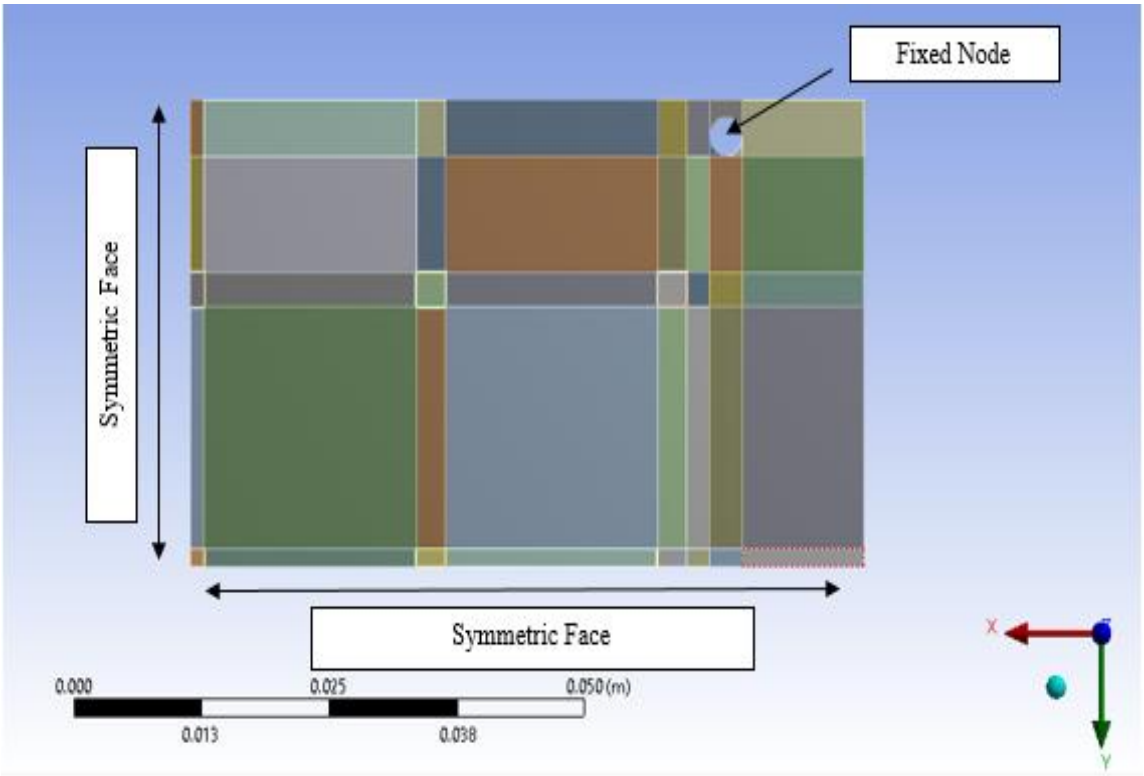

Figure 5.3: Boundary conditions applied in this analysis.

5.6 Loading

According to JEDEC standard JESD29-B111, the loading condition for a drop test has an input acceleration with a peak value of 1500G and the impulse duration is 0.5ms without rebound. The acceleration impulse measured by the accelerometer attached to the board is given by the equation,

$$a = \begin{cases} 1500g \ \sin\dfrac{\pi t}{t_w}, & t \le t_w,\ t_w = 0.5 \\ 0, & t > t_w \end{cases}$$

Where, a= acceleration (m/s^2); g= acceleration due to gravity (m/s^2); t= time (ms).

The Input G technique assumes that since the entire setup of the drop table and board act as a rigid body, it is realistic to apply the above acceleration impulse directly to the board.

5.6.1 Direct Acceleration Input (DAI)

The loading conditions can be simplified with a slight modification to the Input G method, where the acceleration input is directly applied to the board as body force. The following equation represents the acceleration impulse as a body force [13].

$$[M]\{\ddot{u}\} + [K]\{u\} + [C]\{\dot{u}\} = \begin{cases} 1500g \ \sin\dfrac{\pi t}{t_w}, & t \le t_w,\ t_w = 0.5 \\ 0, & t > t_w \end{cases}$$

$$\{u\}_{|t=0} = 0$$

$$\{u\}_{|t=at\ hole} = 0$$

These equations tantamount to the original problem definition except for the difference in rigid body movement. In this approach, the surfaces of the screws are fixed at all time [13]. The input acceleration at different time instances is given by the following table 5. Figure 5.4 shows the variation of acceleration loads with time during a drop test.

Table 5: Acceleration input at different time intervals according to JEDEC standard [43].

Time	Acceleration
0	0
0.00005	4.54E+09
0.0001	8.64E+09
0.00015	1.19E+10
0.0002	1.4E+10
0.00025	1.47E+10
0.0003	1.4E+10
0.00035	1.19E+10

0.0004	8.64E+09
0.00045	4.54E+09
0.0005	-4.7E-06

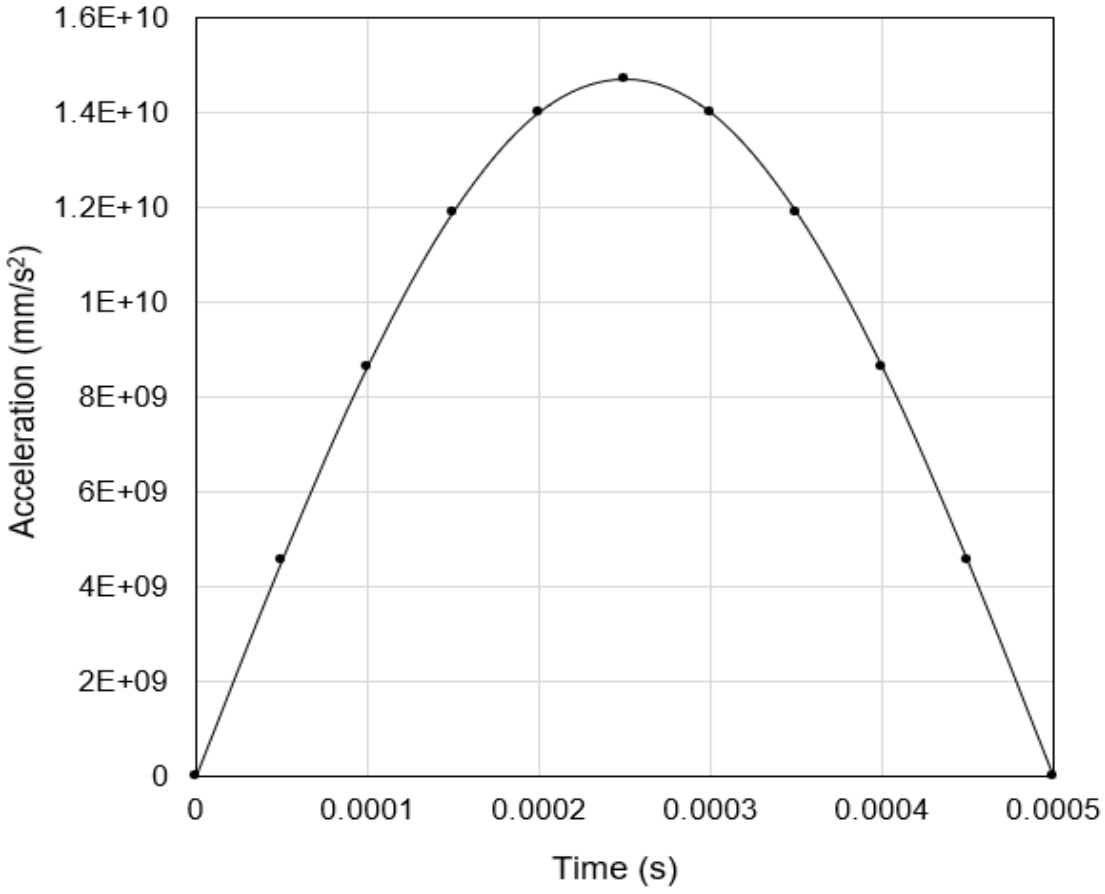

Figure 5.4: Drop test acceleration input Vs Time [43].

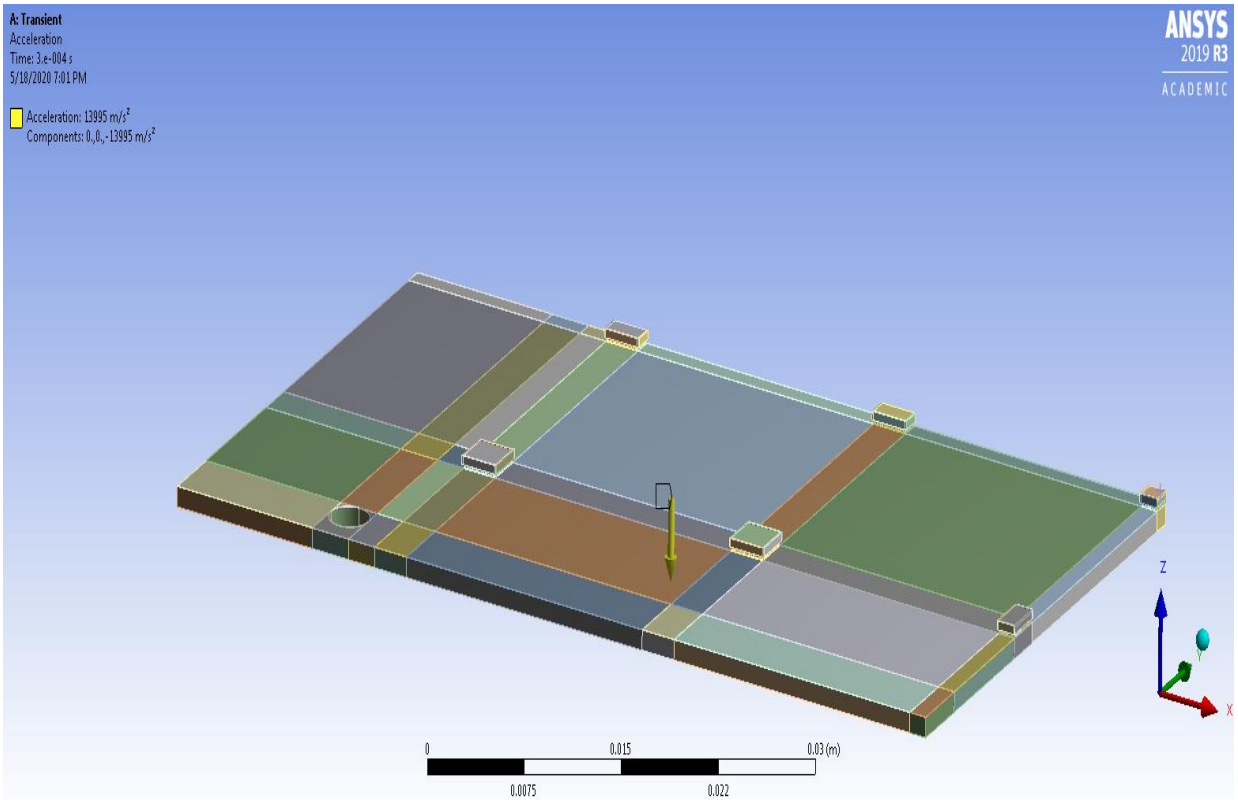

Figure 5.5: Drop test loading direction shown on the model.

The acceleration load for the drop test is applied on the package side of the board according to JEDEC condition JESD29-B111. The package side of the board is more vulnerable and susceptible to failure when dropped. Therefore, the acceleration load is applied in the direction as shown in the figure 5.5. The impact load is applied at a constant temperature throughout the model. In this study, the drop tests were done at temperatures 160°C, 180°C and 200°C.

Chapter 6

RESULTS AND SUMMARY

The computational analysis was done for temperatures 160°C, 180°C and 200°C for both the cases of low loss PCB modeling. Total deformation, total acceleration, equivalent strain results are analyzed and compared. The data was exported from ANSYS Workbench and OriginPro software was used for the plots.

6.1 Maximum Total Deformation

The total deformation of the board at different instances of time after drop test was observed and the maximum total deformation was plotted against time for the two cases of low loss PCB modeling at different temperatures. The red line in the plot represents viscoelastic maximum total deformation and the black dotted line represents the deformation of elastic case of PCB modeling. It was observed that at 160°C, which is below the Tg of low loss PCB used in this work, there is no difference between the elastic and viscoelastic cases as the deformation responses of the model are almost overlapping. However, at 180°C and 200°C the viscoelastic cases have a dampening effect in their maximum total deformation which is significantly different from elastic cases. Figure 6.1 shows the maximum total deformation of the model at different temperatures for the two kinds of low loss PCB modeled.

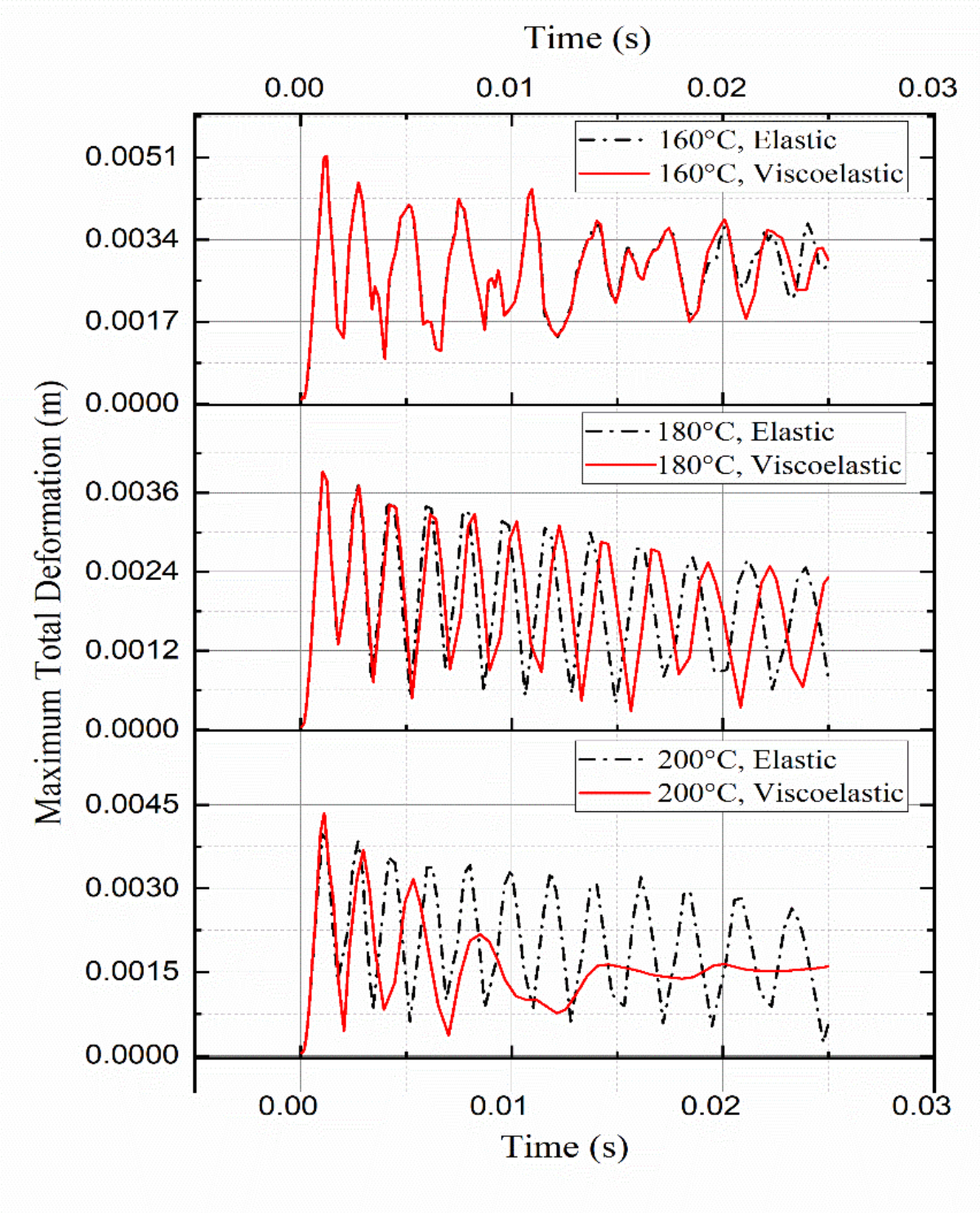

Figure 6.1: Maximum total deformation Vs Time at different temperatures.

6.2 Maximum Total Acceleration

The package experiences a varying acceleration for some amount of time due to the drop or impact loading. This acceleration value is not the same throughout the board at an instant of time. The maximum total acceleration of the package with time is plotted for 160°C, 180°C and 200°C for both the cases of low loss PCB modeling. The red line in the plot represents the maximum total acceleration for viscoelastic model and the black line represents the elastic model results For 160°C, there is negligible difference between the maximum total acceleration of elastic and viscoelastic cases, whereas, for temperatures 180°C and 200°C which is higher than the Tg of Megtron-6 board, the viscoelastic model captures a faster diminishing of total acceleration compared to the elastic model. Figure 6.2 shows the maximum total acceleration response of the package with time at different temperatures for elastic and viscoelastic modeling of the low loss PCB.

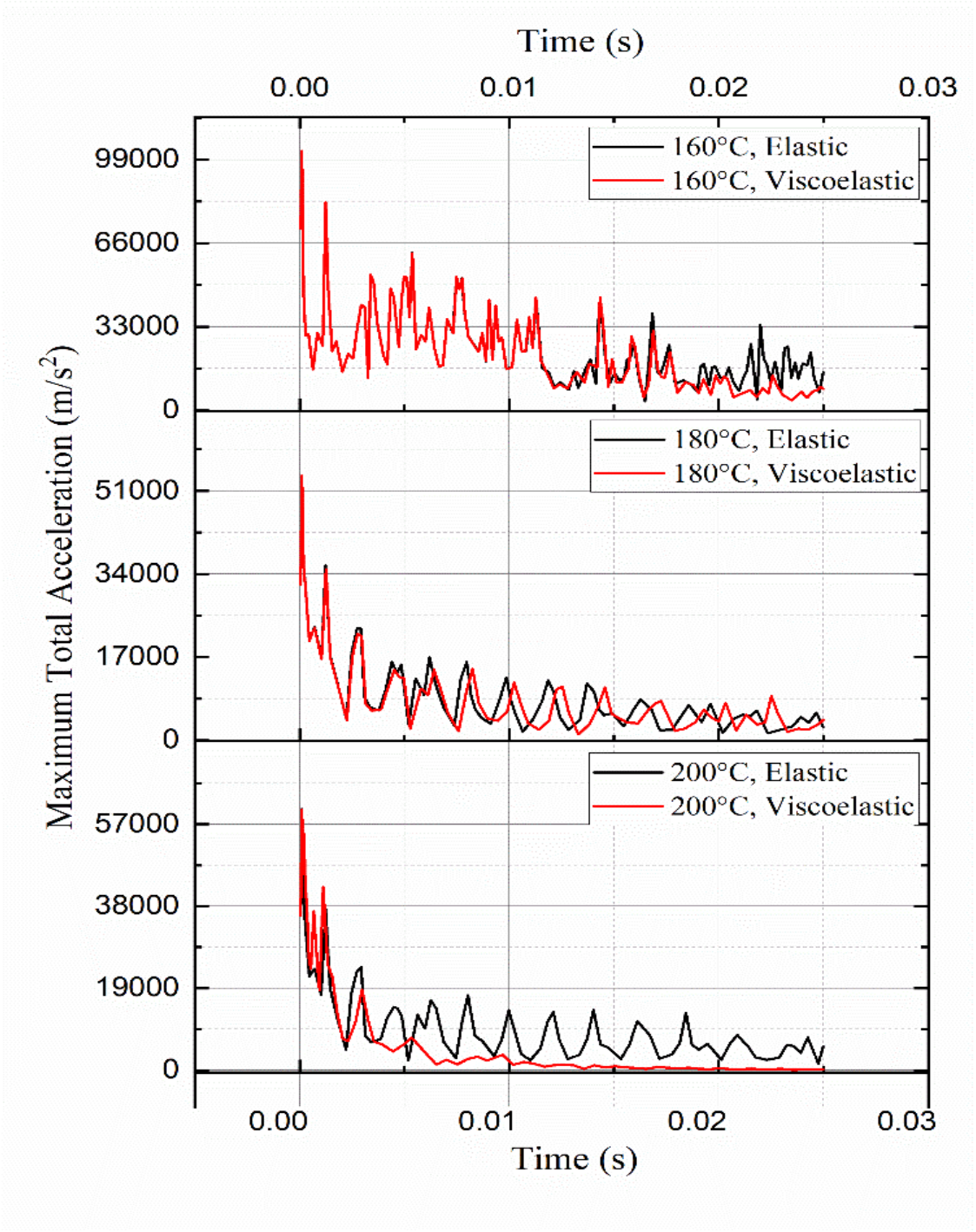

Figure 6.2: Maximum total acceleration Vs Time at different temperatures.

6.3 Equivalent Strain

The equivalent strain on the package was evaluated and the maximum equivalent strain values at different instances of time was observed. For temperature less than the glass transition temperature of the low loss PCB used in this work, it was seen that there is no difference in the maximum equivalent strain between the elastic and viscoelastic case. On the other hand, for temperatures, higher than Tg the equivalent strain is more for viscoelastic cases compared to elastic modeling of the low loss PCB. Figure 6.3 shows the maximum equivalent strain plotted for both the cases of PCB modeling at different temperatures.

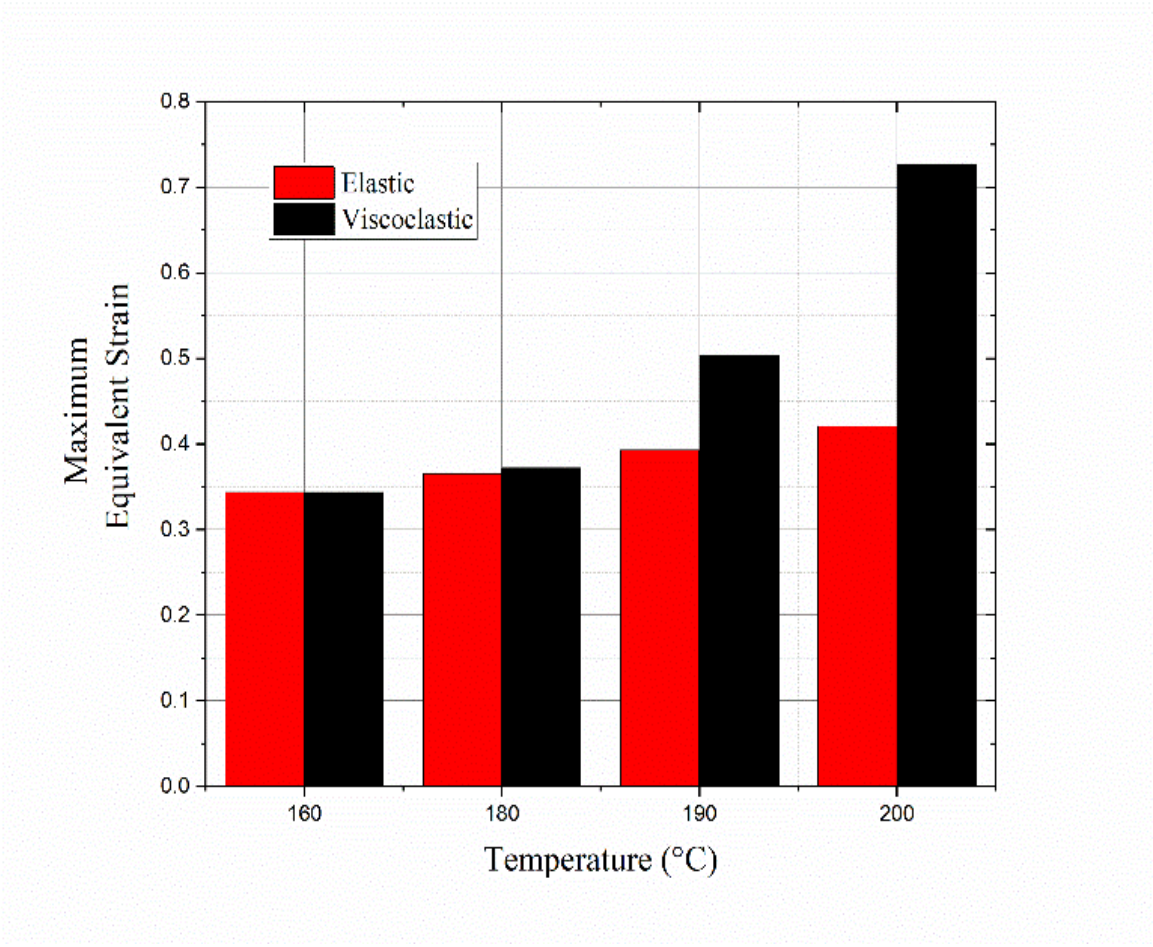

Figure 6.3: Maximum equivalent strain Vs Temperature.

Chapter 7

CONCLUSION AND FUTURE WORK

In this work, the impact of viscoelastic properties of low loss PCB on the reliability of the WCSP package under drop test was investigated. Owing to its superior electrical performance and other advantages over FR-4 laminates, low loss materials can be extensively used for high frequency applications. Therefore, it is necessary to ensure the reliability of these laminates to validate its use. The work from Liu et. al analytically proved that the viscoelastic properties of PCB had direct influence on its dynamic characteristics [18]. Also, as PCB mainly comprises of macromolecules which are typical viscoelastic materials, it is realistic to model the PCB as viscoelastic. Hence, the low loss PCB used in this work was modeled as orthotropic viscoelastic model and orthotropic elastic model for comparison. The Megtron-6 board was characterized on TMA and DMA to obtain their material properties. The DMA data was used to create master curve using WLF shift functions on TA7000 software. The master curve data was fitted on prony series using the Non-linear curve fitting tool on OriginPro software. The prony series constants obtained represent the viscoelastic properties of the Megtron-6 PCB and it is used in the computational analysis in ANSYS Workbench. The finite element analysis is done on a quarter symmetric WCSP package under drop testing conditions for both kinds of PCB modeling. The simulations were done for temperatures 160°C, 180°C, and 200°C. Total deformation, total acceleration and equivalent strain results were compared. A significant dampening effect was seen in the total deformation of the package of viscoelastic modeling at temperatures higher than the Tg of the low loss PCB. The acceleration response of the package was observed to be diminishing faster in the viscoelastic cases.

Also, greater equivalent strain was seen in the viscoelastic model for certain temperatures. However, there was no significant difference in the deformation, acceleration, and equivalent strain in the package between the two kinds of PCB modeling at temperature lower than the glass transition temperature of low loss PCB. The results were in accordance with the conclusions made from Liu's work [18].

This work concludes that the viscoelastic properties of the low loss PCB does have an impact on its dynamic characteristics for temperatures higher than its Tg. If the operating temperature of the package is greater than the glass transition temperature of the low loss PCB, it is necessary to include the viscoelastic properties in the PCB modeling to get accurate results in the computational analysis. If the use temperature of the package is lower than the Tg of the low loss PCB, it is sufficient to model the PCB as elastic for computational analysis to reduce simulation time and reduce the complexity in determining the viscoelastic properties. The future work can be determining the failure component and failure location in the package under drop testing using sub modeling technique.

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