STRUCTURAL OPTIMIZATION AND RELIABILITY ASSESSMENT OF HETEROGENEOUS 3D IC PACKAGES AND ANALYSIS OF RHEOLOGICAL PROPERTIES OF PARTICLE BASED THERMAL INTERFACE MATERIALS

by

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THESIS

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Dedication

I dedicate my work to my respected parents and to my loving husband for their enormous support and love which give me motivation to overcome the challenges and to pursue my goal. A special feeling of gratitude to my loving ones for believing in me and always being there with me both in my good time and hard time whenever I need them most. I will always appreciate all they have done and will always try my best to make them proud.

ABSTRACT

STRUCTURAL OPTIMIZATION AND RELIABILITY ASSESSMENT OF HETEROGENEOUS 3D IC PACKAGES AND ANALYSIS OF RHEOLOGICAL PROPERTIES OF PARTICLE BASED THERMAL INTERFACE MATERIALS

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The University of Texas at Arlington, 2021

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As computing and communication devices are converging with improved functionally, denser, and finer pitch which creates complexity of circuit interconnections for 2-D devices becomes a limitation for overall performance and drives up power dissipation [1]. Thus the ordinary 2-D structures of IC packages cannot address those demands where 3-D through-silicon via (TSV) is the key to 3-D IC integration and stacking of chips, is emerging now as a powerful tool to converge the needs of integrated circuit (IC) packages. In 3D TSV the chips are stacked on top of another so heat trapped in a small region which is difficult to dissipate that may cause failures in electronic devices [2]. Also, the high CTE mismatch between low k dielectric layer and the copper core is one of the critical challenges for 3-D IC packages. In this study, the effect of the optimization of the structure of a 2-die flip chip BGA package has been studied. Stress intensity factor, which indicates the state of stress near a crack tip and J-integral values are used to specify the crack driving force have been analyzed with the change of die thickness at different positions on TSV [3]. Varying the thickness of die the crack is modeled on TSV which is studied during the chip attachment process. Finite element analysis (FEA) is used to examine the thermo-mechanical stresses and fracture parameters of the 3D IC package. Under Reflow condition and Thermal

Cycling condition the optimization of the structure of the chips are taken place to analyze the reliability assessment of the package. The materials used for TSV and solder bumps are another important factor which impact package reliability. Comparisons of material properties of the copper core of TSV are studied to show how it can affect the package reliability.

The second half of the thesis contains the analysis of rheological properties of particle laden thermal interface materials. In today's digitalized industries one of the most critical challenge is thermal management of the electronic devices with improved functionality. As heat dissipation is very crucial thermal interface materials (TIMs) plays a vital role for dissipating heat of electronic devices. Particle based thermal interface materials are one of the most widely used TIMs in microprocessor cooling solutions. Thermal conductivity of such particle laden TIMs increases with the volume fraction of conductive particles added to the thermal interface materials. These volume fraction of conductive particles not only affects the thermal conductivity of thermal interface materials but also impacts the bond line thickness (BLT) and other rheological properties such as viscosity and shear modulus of TIMs after a certain limit [4]. The uniformity of particle laden TIMs to cover the interfaces of the components of electronic packages depend on the viscosity of such materials [5]. In this analysis two types of micro particle based TIMs, TIM A and TIM B are used to measure the change of viscosity at room temperature using Discovery Hybrid Rheometer (HR-2) at different gap between two parallel plates of the rheometer to see how the viscosity of these TIMs changed with confinement and reach to a constant value with the change of shear rate. It is crucial to measure the rheological properties of such particle laden thermal interface materials as it is related to the thermal conductivity of TIMs and can enhance thermal management or heat dissipation of electronic devices.

List of Illustrations

List of Tables

Table of Contents

Chapter 1: STRUCTURAL OPTIMIZATION AND RELIABILITY ASSESSMENT OF HETEROGENEOUS 3D IC PACKAGES

1.1 Introduction

Since 1996 the Electronics Industry has been the wide-ranging industry and one of the major inventions of the Electronics Industry is transistor which was invented by John Bardeen, Walter Brattain, and William Shockley in 1947 at Bell lab in New Jersey. Integrated circuit (IC) was invented by Jack Kilby in 1958 and Gordon E. Moore, founder of Intel wrote an article in Electronic Magazine in 1965 where he exhibited a graph that demonstrates number of components into an integrated circuit or the overall computing power for computers will double exponentially every 18 months will increase the functionality of a chip and reduce the cost per function. The scaling and integration in 2-D was weighted on a system-on-chip (SOC) configuration according to this law [6].

Over the past few decades integration of semiconductor technology has been largely extended in two-dimensional applications not only in the field of electronics but also in a variety of sectors such as optoelectronics, bioelectronics, medical systems, electronics analysis, computer systems, military systems, satellite systems, submarine systems, and so on. From our basic needs to ultra-high-end products and military usage, almost all industrial products incorporate semiconductor devices [7].

Generally, electronic packaging is a science and art which allows appropriate environment to the components of electronic devices to provide optimum performance reliably over a period. The word appropriate environment means thermal, electrical, and other issues related to electronic devices. Every technology associated with Integrated Circuit (IC) and the system needs this

appropriate environment of electronic packaging to achieve better performance and to gauge it properly after the product has been packaged. There are various levels of electronic packaging which are classified below:

0^{th} level packaging:

➢ Packaging different functions on a semiconductor

➢ Several transistors, circuits

➢ Gate to gate interconnection

➢ Multitudes of functions, processors, logic, memory

➢ Chip level interconnects etc.

1^{st} level packaging:

• Process of assembling a semiconductor chip or chips into an encloser/package as a-

➢ Single Chip Module (SCM) or

➢ Multi Chip Module (MCM)

To facilitate assembly on to a board.

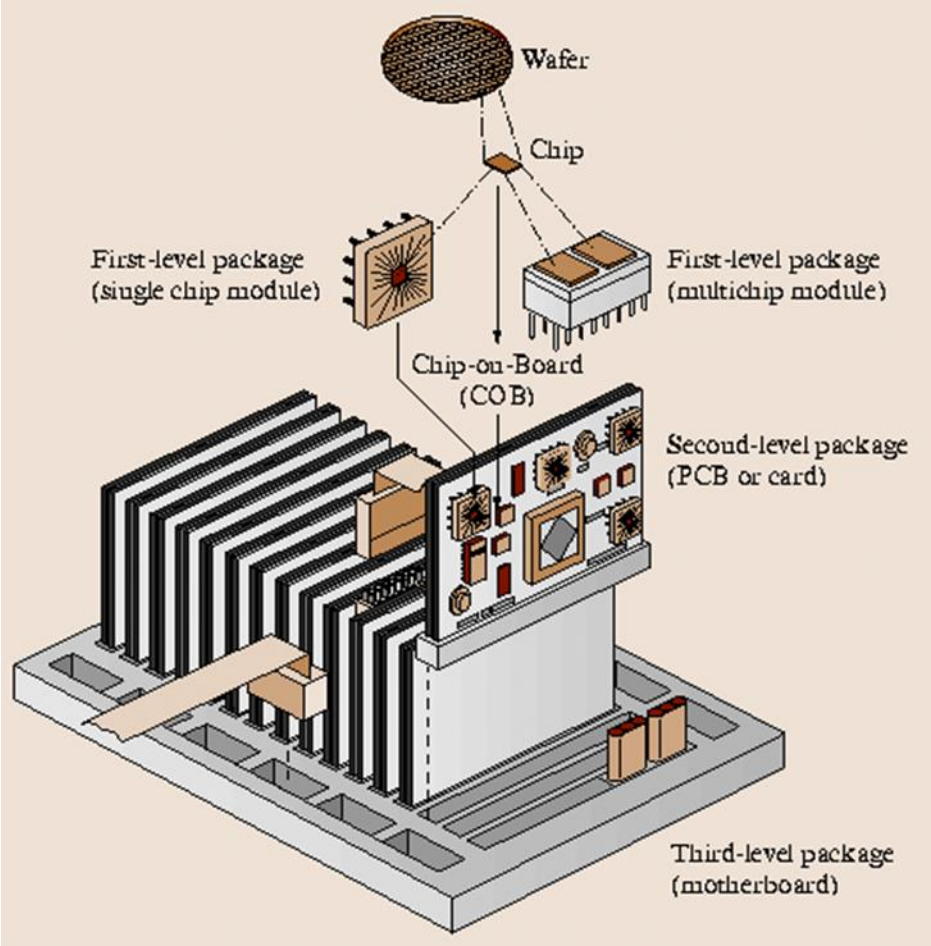

Fig. 1: Levels of electronic packaging [8].

2nd Level Packaging:

• Assemblies

➢ First level Packages on to a Printed Wiring Board

➢ Capacitors, Resistors, Inductances

➢ Switches Connectors

➢ Daughter Cards with devices already assemble

3rd Level Packaging:

➢ Assembling mother boards daughter cards, etc.

4th Level Packaging:

• Box Level Assembly with

➢ Storage devices

➢ Cables

➢ Rack and box assembly

5th Level Packaging:

• Host to terminals

• Printers, displays, keyboard, etc.

The roadmap of electronic packaging is moving in such a direction that chips with more input/output terminals, smaller footprint, less weight, faster signal processing time with lower power loss, better performance, possibly lower cost and state-of-the-art multifunctionality is going to take over. To fulfill such requirements in innovation, with respect to the design, material properties, manufacturing methods, and so on packaging technology exceeding the horizontal limit, engineers were consistently thinking out to find new scopes and one of the steps is 3D stacking in vertical dimension [3].

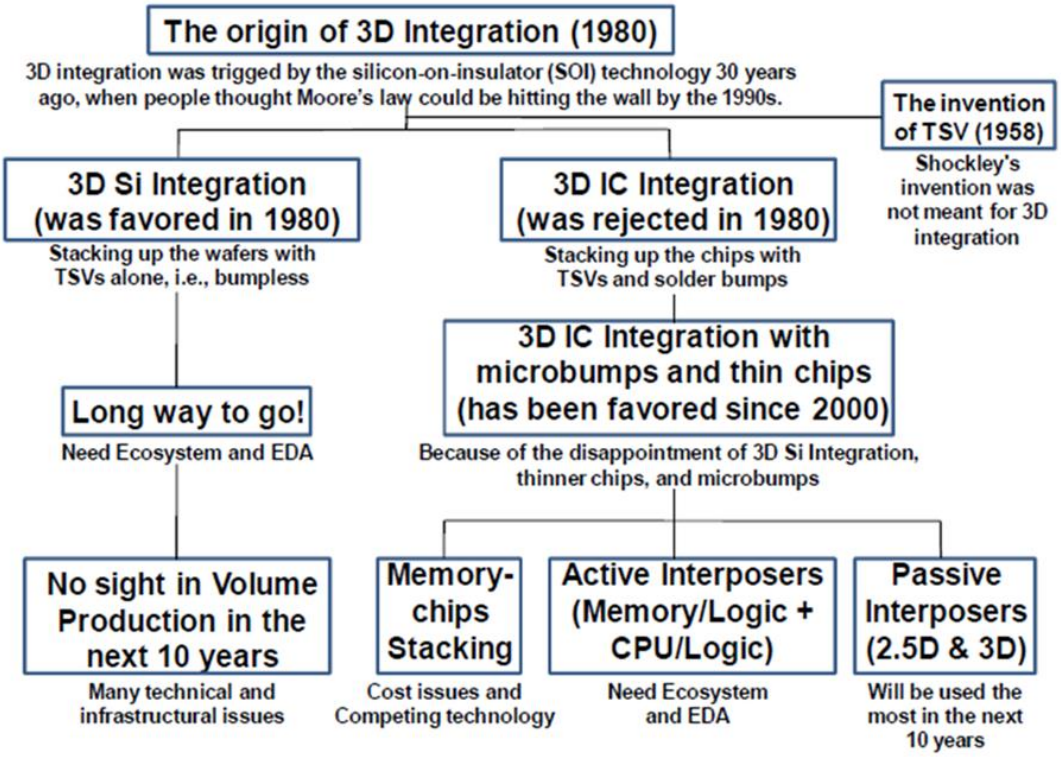

Fig. 2: Types of 3D integration [6].

1.1.1 Moore's Law vs More Than Moore

3D integration includes 3D IC packaging, 3D IC integration and 3D Si integration. Through Silicone Via (TSV) is the heart of 3D integration which separates 3D IC packaging from 3D IC integration and 3D Si integration. A thin silicon wafer with through holes is drilled in a typical 3D IC integration, and along the inside walls of the holes dielectric SiO2 is deposited, and then the hole is filled with Copper. In 3D IC integration chips are connected though silicon via (TSV) interconnects on top of another where in 3D IC packaging there is no interconnects to vertically connect the chips rather it uses ire bonding method or die attach to stack the dies vertically. Also, in 3D IC integration micro bumps exist under the chips to connect it to the

substrate where in 3D Si integration is bump less with tiny TSVs and thin wafers which includes chip to chip (C2C), chip to wafer (C2W) and wafer to wafer (W2W) bonding methods. The 3D IC integration and 3D Si integration are the results of the more-than-Moore's Law [6].

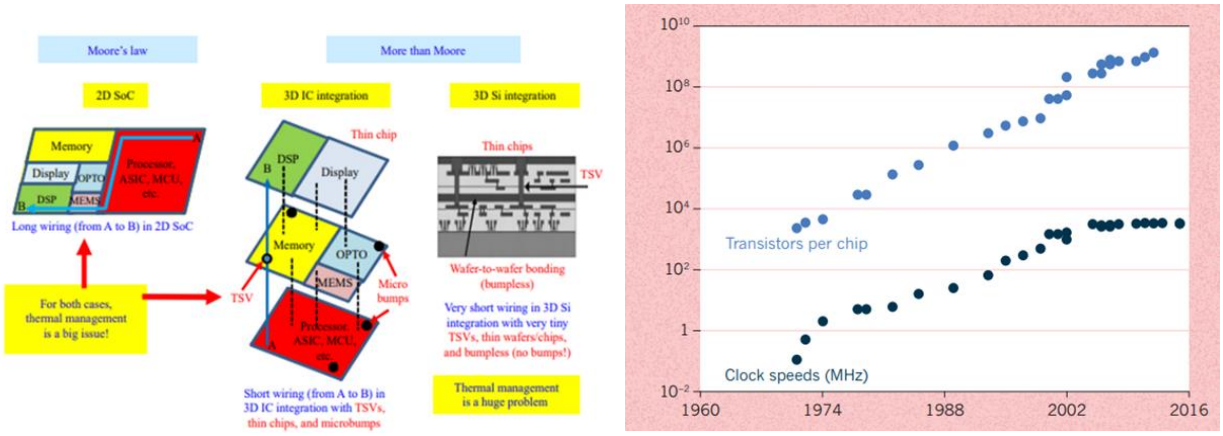

Fig. 3: Moore's law and more than Moore's law [6], [9].

From the above figure it can be observed that the number of transistors per chip is increasing at a higher rate at around 2004 but the clock speed during that period is not changing rather giving constant values with time. As the number of transistors per chip is increasing the size of the transistors is decreasing along with that and currently the microprocessors having circuit features at around 14 nanometers across. According to Dennard Scaling (1974) it is observed that the voltage and current is proportional to the linear dimensions of a transistor and as the size of the transistor shrank so did the necessary voltage and current; power is proportional to the area of the transistor. With the decreasing of the size and increasing the number of transistors per chip based on Moore's law is not giving promising results after a certain limit that is why the clock speed is getting constant though the transistors per chip is increasing at SOC configuration. Here comes the SiP configuration to utilize the chip real estate efficiently at 3D so that better performance and improved functionality can achieve without decreasing the size of the components and attaching

the dies on top of another vertically in an electronic package which is the results of more than Moore [9].

1.1.2 Classification of Package Interconnects

I. **Die-Die Interconnects:** In this case multiple dies are stack on top of another by vertical interconnectors in 3D.

a) Die-to-die attach process

b) Die-to-wafer attach process

c) Wafer-to-wafer attach process

II. **On-Package Die-to-Die Interconnects:** In this case die can be laterally connected to other dies on a package in 2D.

III. **Die-to-Package Interconnects:** In this case die is connected to the package which is known as first level interconnect (FLI).

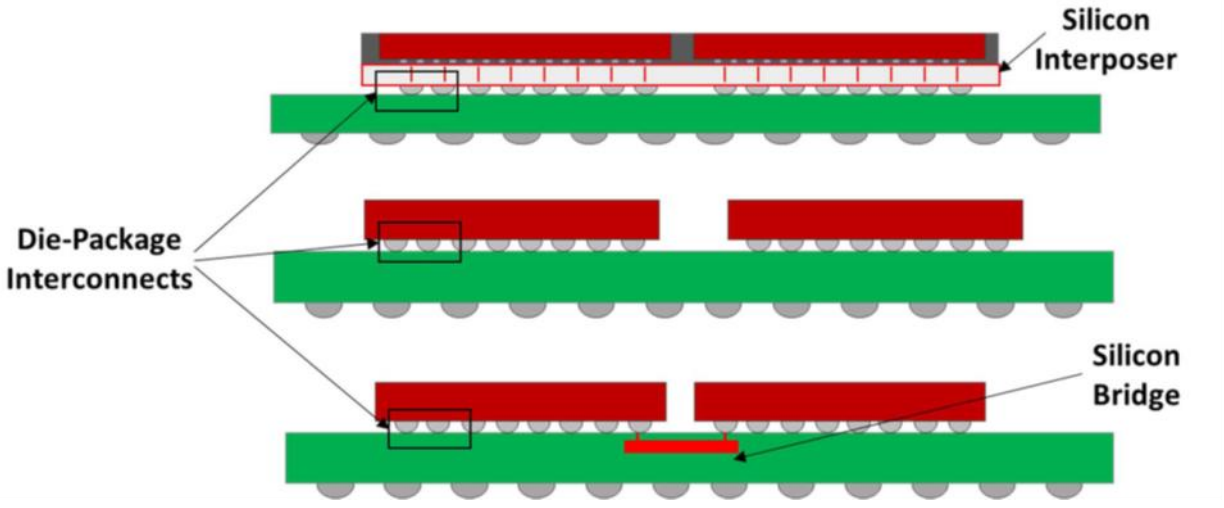

Fig. 4: Package-on-package (POP) architecture [10].

IV. **Within-Package Interconnects:** In this case two or more dies are laterally connected by interconnects within the package.

V. **Package-to-Board Interconnects:** In this case the package is interconnected to the motherboard which is next level packaging known as second level interconnect (SLI).

VI. **POP (Package-on-Package) Interconnects:** In this case one package is connected to other packages by peripheral package interconnects or Vertical Interconnects (VI). Generally used to stack memory packages on logic to create compact form factors shown in the figure below.

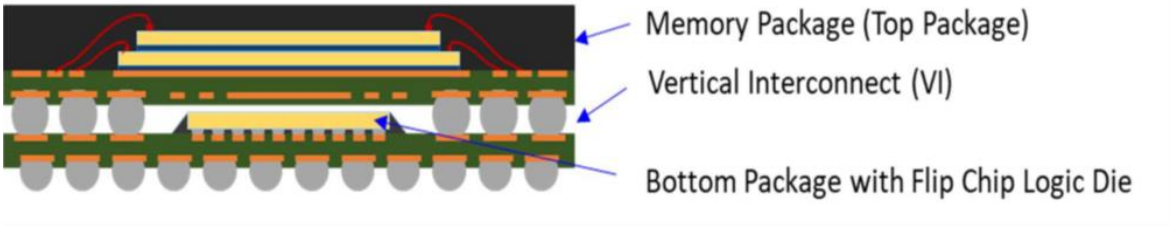

Fig. 5: Package-on-package (POP) architecture [10].

Silicon is one of the widely used materials in semiconductor industries because it is the second most abundant element in earth's crust after oxygen. Silicon crystal lattice has a diamond cubic crystal structure with a repeating pattern of eight atoms and each Silicon atom is attached with four neighboring atoms by four bonds. Because of it's stable structure, band gap, easy fabrication and one of the crucial properties is that it is a semiconductor which means it conducts electricity under some conditions and also behaves as an insulator under other conditions, it is the most common element used in semiconductor devices. Glass can also be used as an interposer, but one of the core ingredients of it is sand or silica which is made of the molecules of silicon dioxide [11].

1.1.3 Types of 3D Integration

In 3D integration two or more layers of active electronic components are attached vertically through TSVs, which are called the vertical interconnects. It was stimulated by silicon-on-insulator (SOI) technology where Gat and his colleagues first outlined it more than 30 years ago. 3D integration follows Moore's Law but it not only stacks chips in 2D but also it vertically stacks the chips in 3rd dimension with TSVs, thin chips and micro bumps to acquire better signal processing at a faster rate as the length of TSV is shorter with less loss of power and it is also cost effective [6].

There are two different groups of 3D integration:

I. Memory-chip stacking

II. Interposers (active and passive)

Memory-chip stacking:

TSVs interconnects are used to stack vertically memory chips, logics, and microprocessors with large input output interface in memory -chip stacking.

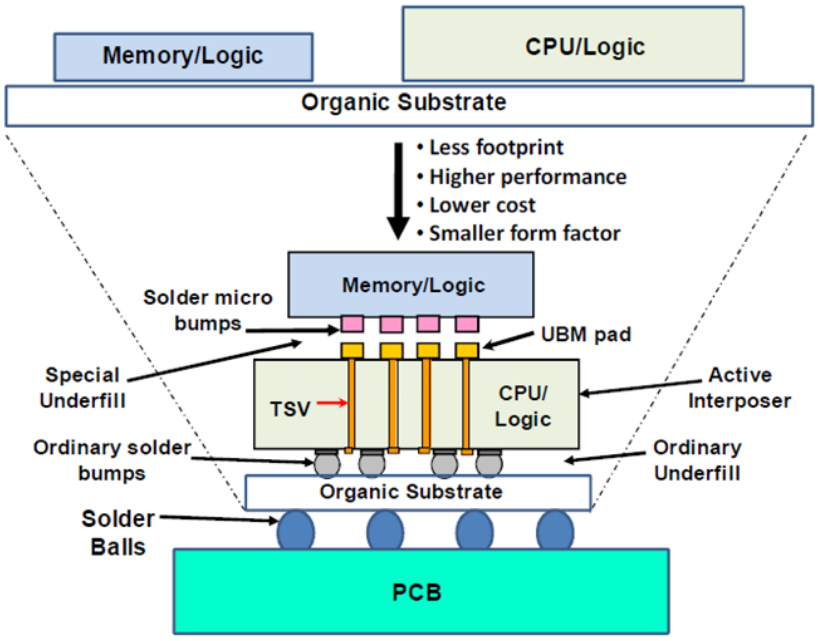

Fig. 6: Memory-chip stacking vertically [6].

Interposer (active or passive):

When the chip gets bigger with more input output terminals the distance between those decreases with denser pitch then the organic substrate cannot bear that chip which then required an intermediate substrate which is known as TSV interposer for that fine-pitch pads to redistribute the array to fewer and comparatively larger pitch pads as shown in figure 7 without adding any 3D layer to acquire a smaller footprint with better performance. Such type of packaging system is called 2.5D integration system-in-package (SiP) [6].

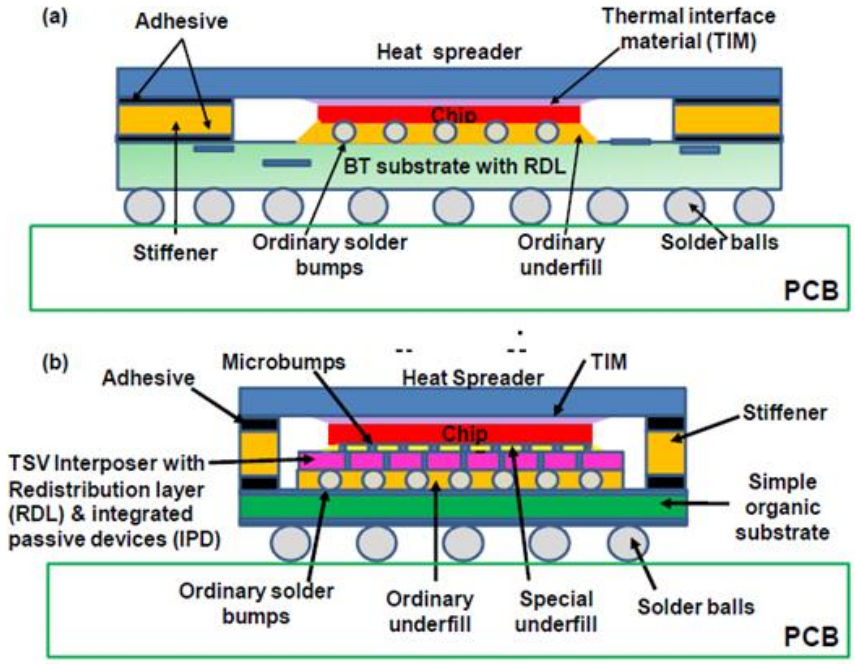

Fig. 7: IC integration with TSV interposer [6].

1.1.4 Heterogeneous 3D Integration

When separately manufactured components are combined to perform higher level assembly into a system-in-package (SiP) configuration to achieve improved functionality with enhanced operating characteristic is known as Heterogeneous Integration. The scope to tailor compound semiconductors and to integrate them onto foreign substrates which can provide to superior or novel functionalities with a potential impact on various areas in electronics, optoelectronics, spintronics, biosensing, and photovoltaics is referred as Heterogeneous Integration. Different components such as individual dies, MEMS device, passive components and assembled package or sub-system that are integrated into a single package provide broadest characteristics at system level performance in such type of integration [12]. Through the Heterogeneous Integration flexibility is acquired to select different components from various

manufacturer to get the highest efficient performance in a cost-effective way. Below the figure is shown for a Heterogeneous Integrated circuit diagram of a 3D integration [13].

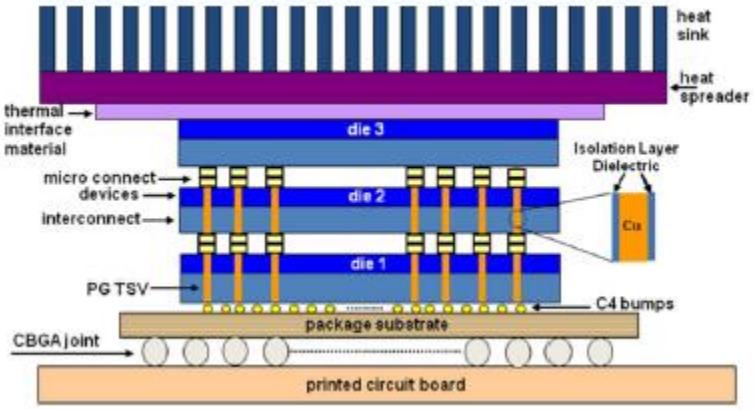

Fig. 8: Heterogeneous 3D integration [14].

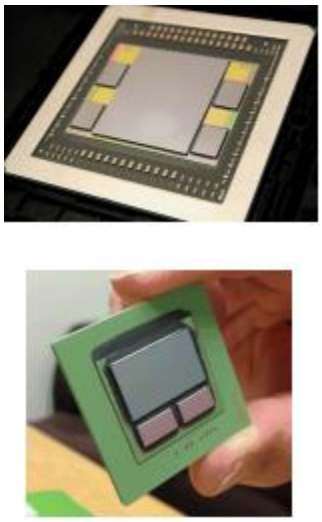

Fig. 9: Different heterogeneous 3D integration [15].

In a flip chip BGA 3D IC package, we can use both sides of the chip to make an optimum utilization of it with maximum inputs and outputs to design the PCB real estate efficiently. On the

other hand, previously in wire bonding package one side of the chip is used to attach with adhesive and heat spreader where proper utilization was not possible.

Though there are lots of advantages of heterogeneous 3D integration, but it requires successful communication be carried on between the IC's and the electronic systems without compromising with the cost and the increased complexity. Therefore, some issues need to be dealt effectively during electronic packaging of 3D integration such as signal processing time, heat dissipation, structural integrity, chip package interaction, TSV wafer warpage, Design software limitation and difficulties in handling and inspection of TSV etc. which need to explore more [1], [12]. In this paper, by optimizing the structure of the die of 3D integration the values of J- integral has been studied which specified as the crack driving force and the values of Stress Intensity Factor which indicates the state of stress near crack tip has been studied with respect to different positions of TSV by FEA to determine how the optimization of the structure impact the reliability of the heterogeneous 3D IC package [2].

1.1.5 Literature Review

John Lau in his paper gave a proper idea about the evolution of 3D integration and TSV and the outlook of 3D integration and it's advantages and disadvantages in microelectronic devices. He also proposed a low cost and thermally enhanced 3D IC integration system-in-package (SiP) is proposed for high performance applications [6].

Mohammed Shahid Ali in his thesis for different die and substrate thickness analyzed and predicted the prevalent modes of fractures in TSV and modify the structure accordingly to reduce failure probability [3].

Unique Rahangdale in his thesis varied die and substrate thickness and analyzed the fracture parameters how it changes with the structural change of the package at different positions of TSV and at BEOL [2], [16].

Pavan Rajmane in his thesis analyzed chip-package-interaction (CPI) and mechanical integrity of a 2die 3D TSV package during the attachment process to substrate [1], [16].

J. Van Olmen et al. in his work first time demonstrated die-to-die stacking using TSV for 3D integrated circuit and also explained chip integrity after the stacking process [17].

Xiaowu Zhang et al. in his paper described the fabrication process of a Si interposer with TSV which is a demanding alternative as the conventional organic substrate cannot bear bigger chips with denser pin out and finer pitch. He also conducted moisture sensitivity test and thermal cycling to provide reliability assessments of the package [18].

Makoto Motoyoshi in his study worked on 3D large-scale integration (3D LSI) using TSV and explained current and future 3D LSI technologies with TSV [7].

Flynn P. Carson et al. in his work indicated package-on-package (PoP) and package-in package (PiP) two different ways to stack packages in vertical integration and also described the development of such technologies [19].

Nauman H. Khan et al. in his analysis investigated various methods to improve 3D power delivery of vertical IC integration based on TSV [20].

Ralf Rieske et al. in his paper found laser drilling as an exciting way which can be applied to drill out the hole in the hetero system package in which 3D TSV is used as an interconnect [21].

Aditya P. Karmarkar et al. in his study proposed the stress distribution of silicon and interconnect are affected by the diameter and geometric layout of the interconnect. The stress induced on TSV can change the silicon mobility and hamper performance of the device which can lead to crack and impact reliability of the structure of the package. Material choice for interconnect which is reliable for this part of the package can have adverse effect on other regions which also studied in this paper [22].

Xuefeng Zhang et al. in his work analyzed different low-k dielectric materials and packaging materials by finite element analysis to see how the coefficient of thermal expansion (CTE) mismatch between these materials can affect package reliability during chip-package interaction (CPI) [23].

P. Ramm et al. in his paper addressed one of the most propitious technologies which uses TSV the vertical interconnects to connect devices on wafer level to provide better electrical performance with high density interconnects at smallest form factor 3D structure [1], [16], [24].

Cheryl S. Selvanayagam et al. in his study analyzed the nonlinear stresses in the micro-bumps between the silicon chip and TSV interposer at a wide range of via sizes and pitches, and at different temperatures to see if an underfill is necessary for reliability issues of the package and considering various underfill material to reduce the stresses and strains at the micropumps [25].

Moongon Jung et al. in his work proposed a proper thermomechanical stress and reliability tool and design optimization methodology to analyze detailed thermomechanical stresses at TSV for different structures and also validate the linear superposition principal of the analysis [26].

Xi Liu et al. in his performed thermomechanical analysis using Finite-Element (FE) models and X-ray diffraction (XRD) experiments at TSVs. A fracture mechanics analysis has also been

done in this study to show the interfacial cracks and its propagation on Cu/SiO_2 at the corner locations [27].

1.2 Fundamentals

1.2.1 Challenges of 3D Package

Efficient utilization of CRE (Chip real estate) is the most challenging part in 3D integration. Only the peripheral area of silicon is utilized by using wire bonding to stack chips. Wire bonds create power loss issues, RC delay and only utilizes peripheral inputs and outputs, with reduced multifunctionality. Improved functionality and more inputs and outputs with proper utilization of the chip real estate, less RC delay can be achieved by through-silicon via (TSV) which is a realistic solution of 3D integration. Design flexibility with the shorter die-to-die interconnects, high bandwidth, smaller footprint, efficient utilization of CRE, functional integration, and less parasitic resistance are the advantages offered by this technology. Utilization of the chip area efficiently, power loss and RC delay are the challenges faced by 3D wire bonding. TSV provides alternatives to such problems [1], [2], [3].

1.2.2 Limitations of TSV Technology

Enormous research effort has been done to the expansion and improvement of various TSV manufacturing process but relatively less work has been addressed to the TSV reliability issues. Limited studies have focused on the analysis of thermo-mechanical failure mechanism, and most of these studies have approached this problem empirically [27]. Though these vertical interconnects TSVs are prominent solution of 3D integration hence there are few limitations related to this technology which need to be effectively dealt with. Heat is the major problem in

electronic devices and in 3D integration, removing heat from the system is a big challenge [28]. Because of the unique features of TSV structure and the high mismatch of the coefficient of thermal expansion (CTE) between silicon substrate, dielectric layer material and copper core, immense thermal stress may develop, and these stresses may lead to structural integrity like cracking, warpage such various reliability issues [27], [29]. Since the TSV's go through dies, and dies have transistors and components which cannot be placed in a thermally stressed area, so, it is crucial to dissipate heat from the chips which are stacked. Various materials try to expand and compress according CTE values. As interface of silicon/SiO2 is brittle, hence crack can form at Si/SiO2 interface and also at the Cu core of TSV due to the high mismatch of CTE of such materials.

1.2.3 Reason Behind Using Fracture Mechanics

This study emphasizes on the analysis of structural integrity during chip attachment process of a 2-die 3D flip chip BGA package to measure the stress intensity factor (K) and J-integral as fracture parameters in TSV/Silicon interface thereby highlighting the prevailing modes of cracking on TSV at both low k dielectric layer and copper core. The value of stress intensity factor (K) and on J-integral is analyzed at different positions of TSVs for different die thickness and showed the reliability assessment of the vertical interconnect at different locations with respect to design changes.

The reason behind the application of fracture mechanics in my study is stress concentration equation cannot deal with any flaw which has sharp corners. When there are elliptical or square holes, stress concentration is present. It is being addressed by linear elastic theory. But at the crack tip where the radius is small, stress becomes infinity which cannot be handled by linear elastic

solution. As plasticity occurs, fracture mechanics needs to apply hence, stress intensity factor is coming into play [2].

In the TSV fabrication process sidewall insulation of SiO2 is one of the crucial and challenging steps. The quality of the sidewall isolation layer becomes a major concern. Failure of insulation layer may result in electrical leakage or other worse reliability problems, and directly affect the yield of devices or systems based on through-silicon vias. Also, Cu core is used for signal passing through TSV for the whole package so the quality of the Cu core is important to pass signal along TSV and any fracture in Cu core can create failure in the whole system [30].

1.2.4 Application of Fracture Mechanics to 3D Integration

- **Stress Intensity Factor**

From various analysis, engineers have identified that cracking is one of the basic reasons most of structures and components start to fail. The relation between fracture, stress, and toughness was first introduced by Griffin in 1920. The conception of strain energy release rate was proposed by Irwin in 1950s. When the strain energy release rate extends a critical value, crack propagates. That critical value is fixed for specific materials and named as fracture toughness (K_C). The stress intensity factor (K) also performs on a similar approach. It can anticipate the state of the stress (stress intensity) near the crack tip due to the developed stresses (Remote or residual). The result of fatigue crack propagation rate at different amplitude and crack lengths in single and polycrystalline materials can be normalized by stress intensity factor, which is a useful tool[31]. The location of the crack, size, sample geometry and other factors affect the magnitude of stress intensity factor, K [3].

$$\sigma_x = \frac{K}{\sqrt{2\pi r}} cos\frac{\theta}{2}\left[1 - sin\frac{\theta}{2} sin\frac{3\theta}{2}\right] + \cdots$$

$$\sigma_y = \frac{K}{\sqrt{2\pi r}} cos\frac{\theta}{2}\left[1 + sin\frac{\theta}{2} sin\frac{3\theta}{2}\right] + \cdots$$

$$\tau_{xy} = \frac{K}{\sqrt{2\pi r}} sin\frac{\theta}{2} cos\frac{\theta}{2} cos\frac{3\theta}{2} + \cdots$$

Where K, is the stress intensity factor (with unit of stress × $length^{1/2}$). From the above equation we can say if r goes to 0 then the stress will become infinity, where linear elastic solution will not be applicable, plasticity takes place as the value of stress is exceeding the material's yield strength. So, the application of fracture mechanics comes to play an important role here. However, if the crack tip zone is quite small as compared to the crack length still the asymptotic stress distribution near the tip is pertinent [32].

- **J-Integral**

With the base of the fundamentals of fracture mechanics being established in 1960s, Rice presented that the method of energy release rate can be expanded to nonlinear materials, with energy release rate being expressed as a path-independent line integral, called J integral. It is one of the techniques to compute the strain energy release rate (work energy per unit fracture surface area) in a material [3]. The equation of J-integral is given below:

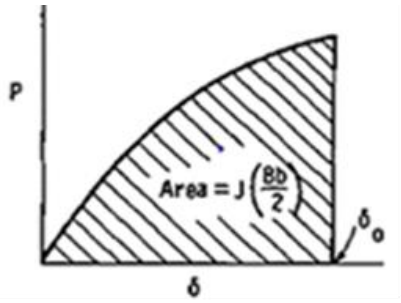

Fig. 10: Rice et al. approximation [2].

$$J = \int_{\tau} \left(W dy - T \frac{\partial u}{\partial x} ds\right)$$

$$W = W(x, y) = \int_0^z \sigma_{ij} d\varepsilon_{ij}$$

Where W is the strain energy density per unit volume, ds is an infinitesimal element of the contour, Γ denotes any contour path surrounding the crack tip, and T and u are traction and displacement vectors along Γ Curve.

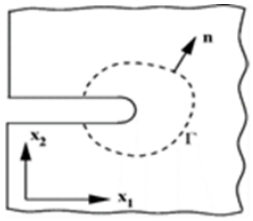

Fig. 11: Line integral around crack tip [2].

1.2.5 Modes of Cracking

Fracture mechanics mainly can interpret fracture using three linearly independent cracking modes. These load types are classified as Mode I, II, or III as shown in the figure-

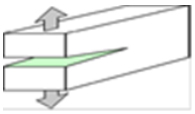

Fig. 12: Mode 1 cracking [3].

In the figure, Mode I crack is shown which is an opening (tensile) mode where the crack surfaces move directly apart due to tensile load.

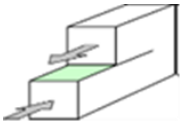

Fig. 13: Mode 2 cracking [3].

Mode II is a sliding mode cracking where the crack surfaces slide over one another in a direction perpendicular to the leading edge of the crack.

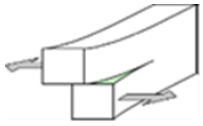

Fig. 14: Mode 3 cracking [3].

Mode III is a tearing mode cracking where the crack surfaces move relative to one another and parallel to the leading edge of the crack. One of the most common load types is Mode I in engineering design.

Studying the dynamics by which the crack grows inside the material, notable understanding can be acquired about the different modes of fracture. Analysis has shown that crack seems to slowly propagate with high plastic deformation rate in ductile materials. The crack can propagate and continue in the material as long as the stress is being applied. With decreasing temperature, the fatigue crack propagation in ductile materials decreases. In brittle materials crack undergo very rapid propagation with little to no plastic deformation, their magnitude growing and increasing after their initiation. Temperature change is a significant factor for any type of cracking in materials [3], [31].

1.2.6 Stress Intensity Factor and Fracture Toughness

The value of critical stress intensity factor is the threshold value for a material, when this value exceeds, fracture generates into the material. It is alike to analogy of yield strength. Fracture toughness, which is denoted by Kc, is the value of stress intensity factor after exceeding that suddenly the crack propagates in a rapid manner of a material. This can be explained by the mathematical expression given below:

If K=Kc,

then crack propagates.

Fracture toughness provides information about the stress intensity field at crack location. Fracture toughness depends upon temperature, rate of strain, and thickness of the material. The thickness of the material is an important factor to predict the way how a crack can propagate [3].

The classification of stress intensity factors is given by the subscripts explained below. For the crack opening mode, K_I is used to imply the stress intensity factor for mode I. For the shearing (crack sliding) mode, K_{II} is used to imply the stress intensity factor for mode II. For the tearing (out of plane) mode, K_{III} is used to imply the stress intensity factor for mode III. These 3 designations with their respective relations are given below:

$$K_I = \lim_{r \to 0} \sqrt{2\pi r}\,\sigma_{yy}(r, o)$$

$$K_{II} = \lim_{r \to 0} \sqrt{2\pi r}\,\sigma_{yx}(r, o)$$

$$K_{III} = \lim_{r \to 0} \sqrt{2\pi r}\,\sigma_{yz}(r, o) \quad [3].$$

1.3 Model Description and Analysis Technique

Design Modeler is used to build the full array model and the quarter symmetry of the array model, which is a compact model is used to analyze. ANSYS 2019 is being leveraged for modeling all types of fracture parameters. Quarter symmetry of 2 die 3D flip chip BGA package is used to simulate under reflow condition to analyze the various stresses developed within the TSV. Sub-modeling technique is used to analyze the fracture parameters of copper core and the dielectric layer of the TSV. The cracks are modeled at a different position on TSV. Varying the thickness of the top die, the behavior of stress intensity factor and J-integral is studied. Material properties of the components of the electronic devices such as solder joints, interconnects are one of the critical factors that can affect package reliability. Two types of properties such as copper linear and copper elastoplastic are used in this study for the vertical interconnects to analyze the stress intensity factors and J-integrals to investigate how it can influence package reliability. Nine cracks were modeled along the TSV at same direction. The temperature boundary condition applied to the package is 200°C to room temperature in 300s [33]. This independent loading condition is Reflow condition. Reflow soldering is the widely used method of attaching microelectronic components to the printed circuit board after that the whole assembly is subjected to controlled heat. Solder paste is used to attach the electronic components. Here, crack was modeled along the TSV and reflow thermal load is applied to the 3D package for assembly. In reflow condition, the thermal load is applied at 200℃ and in 300 seconds and brought to the room temperature i.e. 25℃ and remain in room temperature for 50 seconds more [2], [34], [35]. Thermal cycling is a method by which the electronic devices are gone through a specific thermal load for a particular amount of time to see the strength of the components of the electronic devices to perform reliably. It is conducted to determine the stability of the region which are more vulnerable to crack such as-

solder joint, BEOL and interconnects of electronic devices. The method is used here to analysis the equivalent stress of the whole global model of the 2-die flip chip BGA package is JEDEC standard JESD22-A104D. The temperature changed from -40℃ to 125℃ for 10800 seconds to see how it can impact the reliability of the interconnects of the package [34], [36], [37], [38].

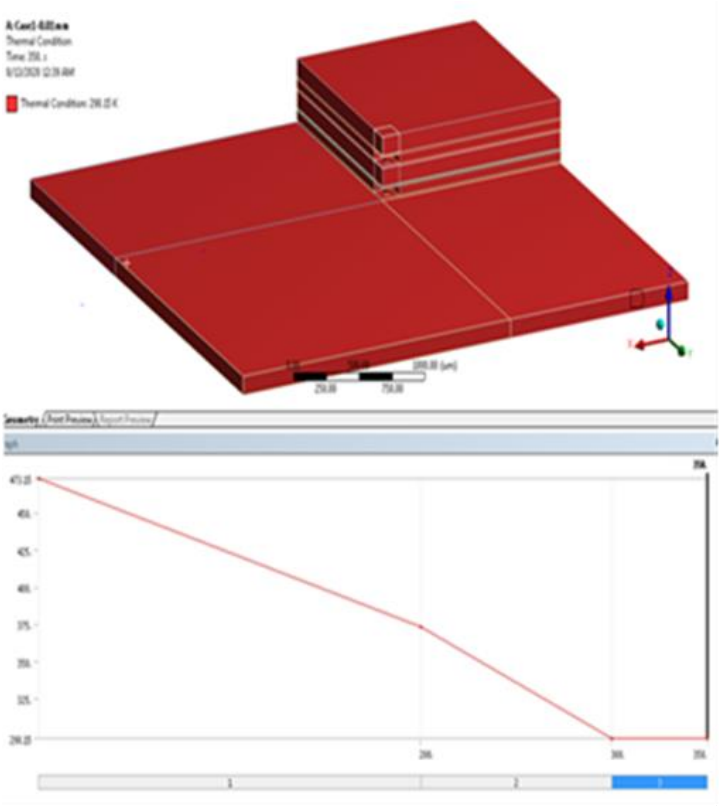

Fig. 15: Reflow condition thermal load profile.

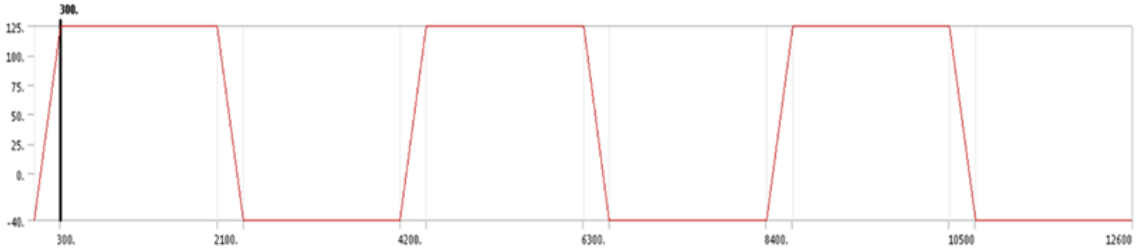

Fig. 16: Thermal cycling condition thermal load profile.

2 die 3-D flip chip package along with the TSV has been studied with respect to the crack propagation analysis. The dimension for the substrate is 7.5 mm on each side and the thickness is 0.1mm. The dimension for the bottom die is 3 mm on each side and 0.1mm thickness. The dimension for the top die is 3 mm on each side and the thickness varies from 0.1mm to 0.3mm. TSV has a diameter of 0.01mm including 0.5μm of the area covered by a dielectric and Cu core has a diameter 0.009 mm. Mirza et al. have put forward a novel perspective of using compact model to simulate the fracture, as the size of the full model is large with 484 TSVs and micro-bumps. Based on application the numbers of TSVs can be changed. In order to avoid ample amount of time to solve the computational analysis the compact model is used so that reasonable computational time can be maintained[39], [40]. There are 3 steps that play an essential role in simulation. At first, a quarter symmetry of the full array on the compact scale is formulated and solved. The results from these solutions are used to originate boundary conditions to the sub model 1 which is part of the vulnerable region having detailed features. On the sub model 2 these boundary conditions are applied which is part of the sub model 1and it is one of the vulnerable parts of the package. A center node at the bottom is fixed to prevent rigid body motions and frictionless support is provided with respect to the symmetric faces. Anand's visco-plastic material property considering plastic deformations has been modeled. To describe the inelastic behavior of lead-free solder, Anand's visco-plastic constitutive law is used. Anand's law has total nine material constants A, Q, ξ, m, n, h, a, s, ŝ are applied throughout the solder strain-rate and temperature sensitivity [1], [2], [41].

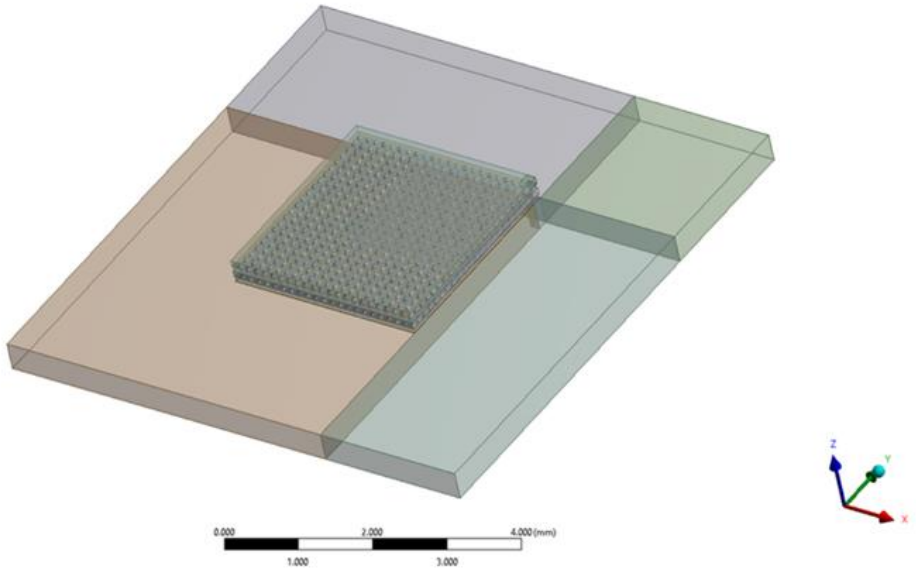

Fig. 17: Full array model.

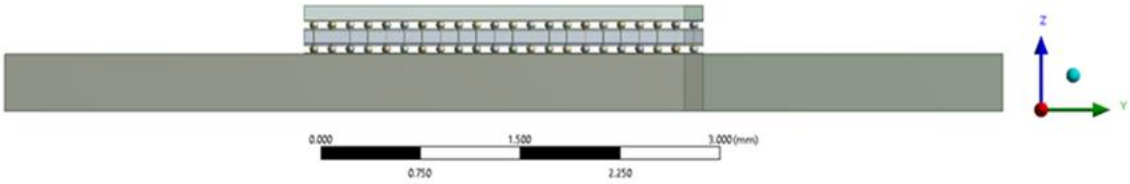

Fig. 18: TSVs of the array model.

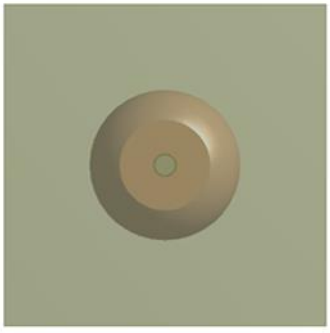

Fig. 19: Single TSV of the array model inside the solder ball.

Following is the quarter symmetry of the compact model:

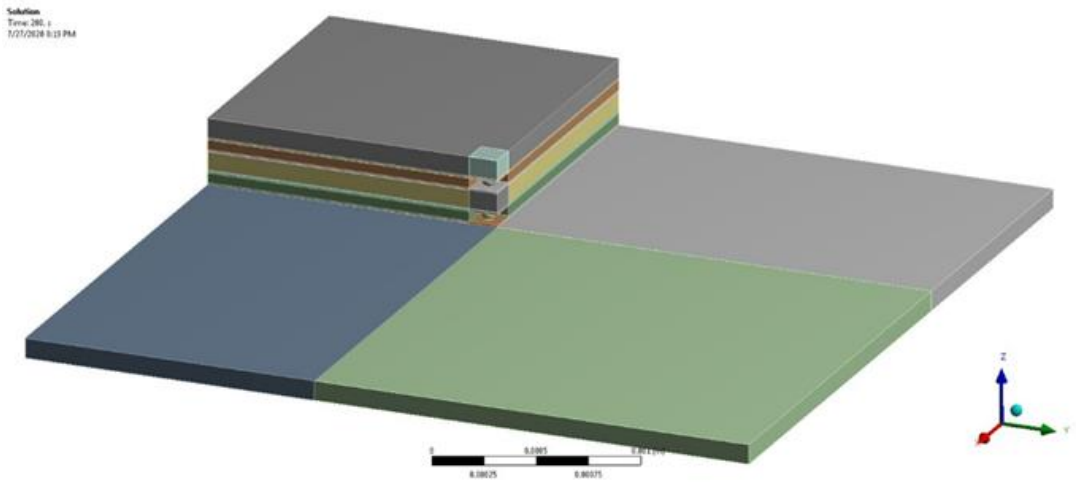

Fig. 20: Quarter Symmetry of the compact model.

Following is the unit cell of the compact model which is the vulnerable part of the model with detailed features:

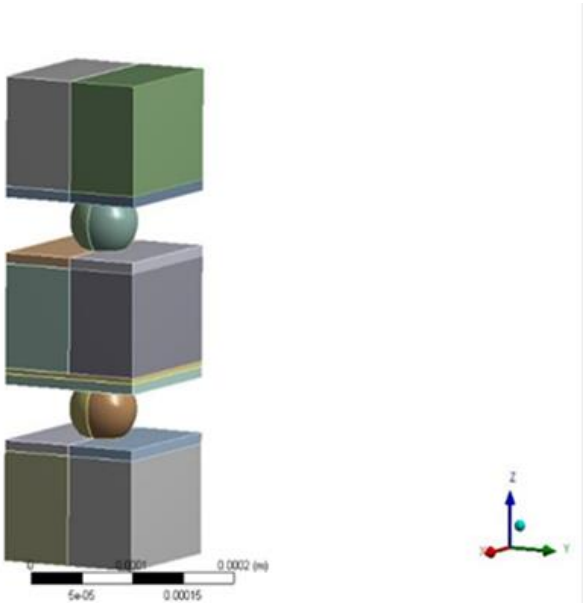

Fig. 21: Sub model 1(unit cell).

Applying sub modeling technique, the boundary conditions are applied from compact model to sub-model 1 and then sub-model 1 to sub-model 2.

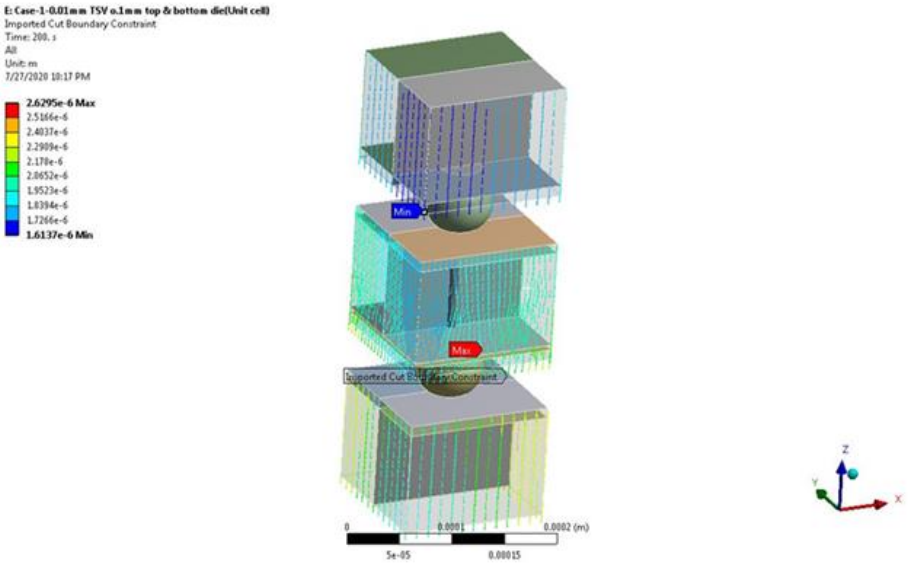

Fig. 22: Sub modeling techniques of Sub-model 1.

Following is the figure of sub-model 2 which the vertical interconnect of the package.

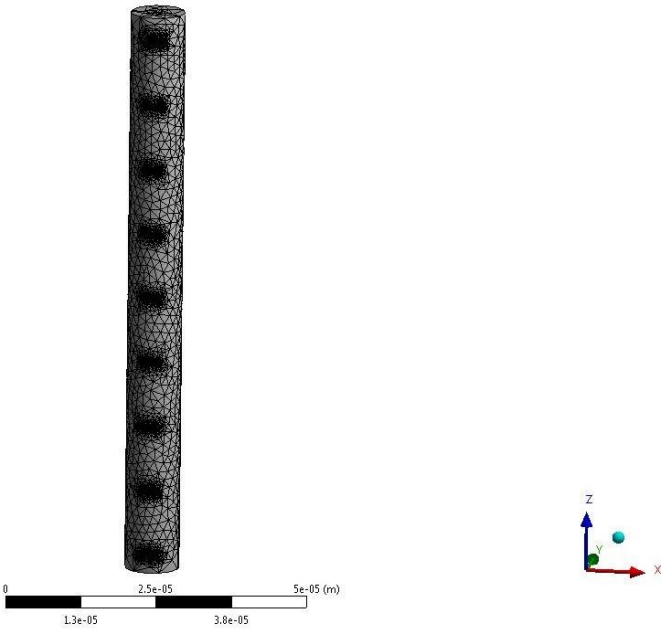

Fig. 23: Sub model 2.

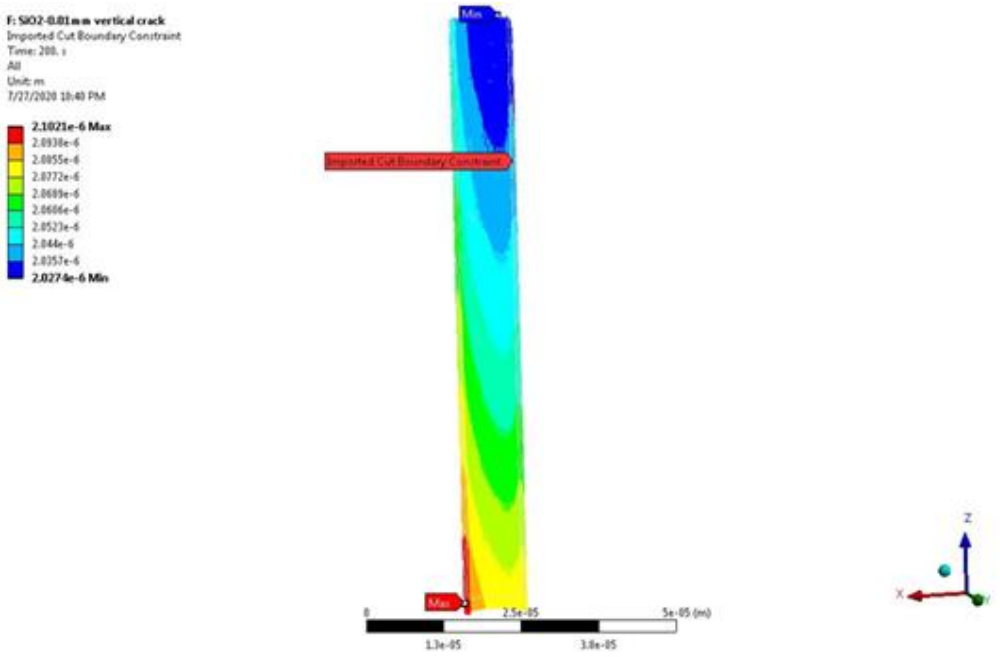

Fig. 24: Sub modeling techniques of Sub-model 2 on SiO2 layer.

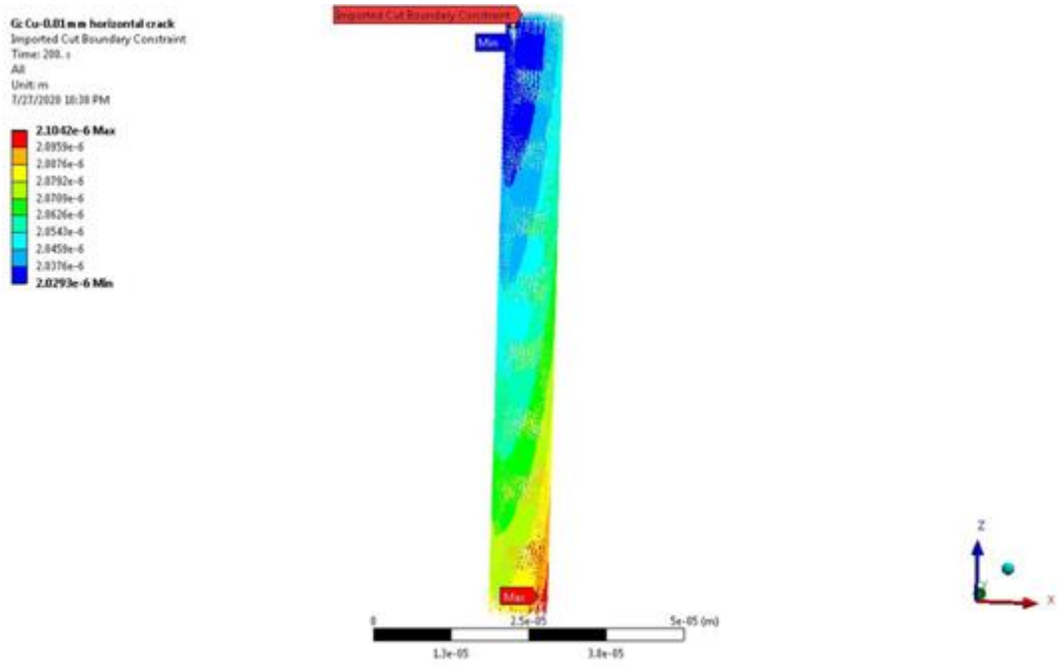

Fig. 25: Sub modeling techniques of Sub-model 2 on Cu core.

Boundary conditions of the package is given below:

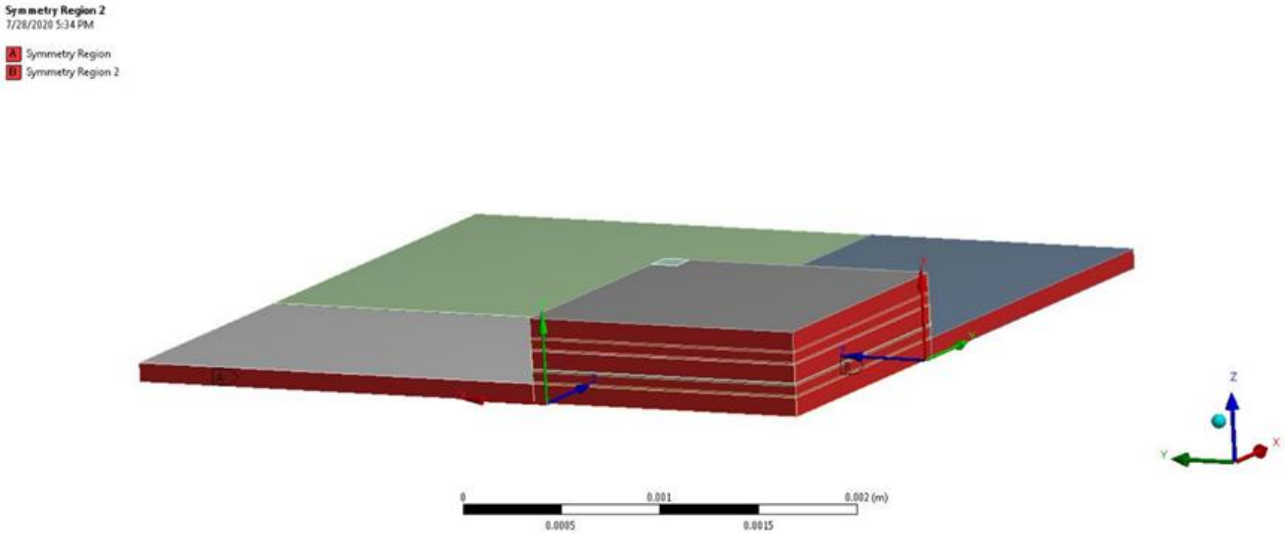

Fig. 26: Boundary Conditions of Symmetric regions.

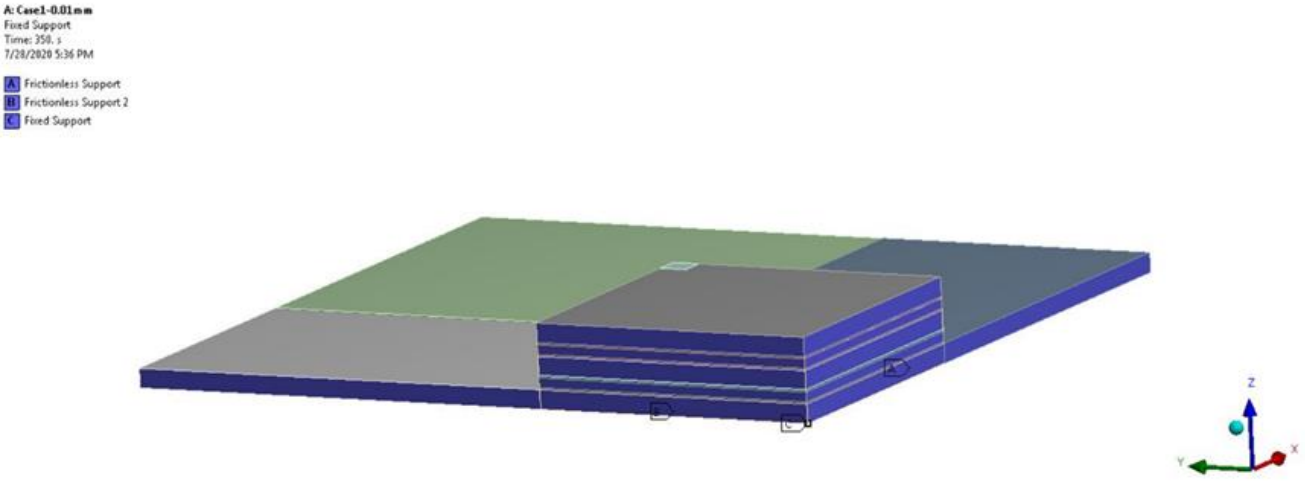

Fig. 27: Boundary Conditions Frictionless and Fixed Support.

The quarter symmetry of the compact model is given below:

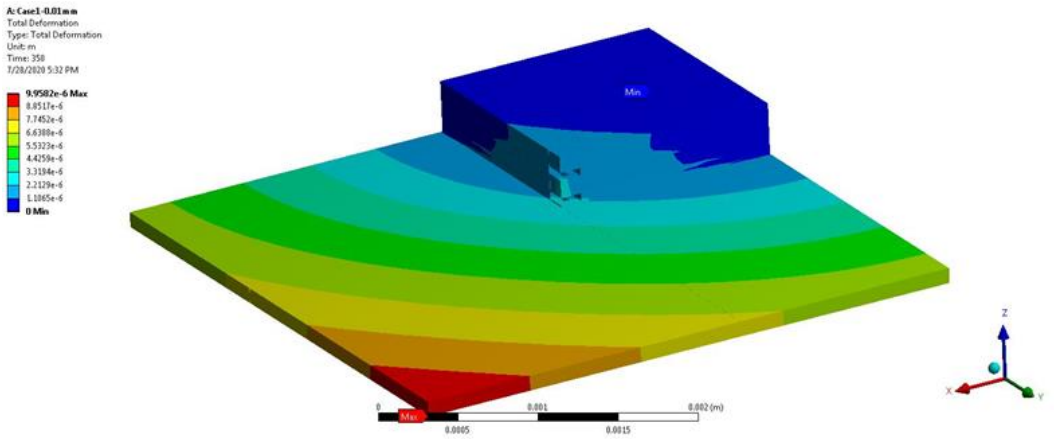

Fig. 28: Equivalent Stress of the Global Model.

In the following tables Anand's visco-plastic properties are given for SAC305 and Effective Block in the Compact Model:

Table 1. Anand's Constant for SAC305 [41]

S. No	Anand's Constant	Unit	Value
1	s_o	MPa	1.3
2	Q/R	1/K	9000
3	A	Sec^{-1}	500
4	ξ	Dimensionless	7.1
5	m	Dimensionless	0.3
6	h_0	MPa	5900
7	$\hat{S}$	MPa	39.5
8	n	Dimensionless	0.03
9	a	Dimensionless	1.5

Table 2. Anand's Constant for Effective Block in the Compact Model [41]

S. No	Anand's Constant	Units	Value
1	s_o	MPa	0.15
2	Q/R	1/K	9000
3	A	Sec^{-1}	500
4	ξ	Dimensionless	7.1
5	M	Dimensionless	0.3
6	h_0	MPa	5900
7	$\hat{S}$	MPa	3
8	N	Dimensionless	0.03
9	A	Dimensionless	1.5

1.3.1 Crack Modeling

Crack propagation is placed at different positions along the cylindrical dielectric layer and Cu core of TSV. This is the distinguished region where more chances to crack due to the developed thermal stress because of CTE mismatch between SiO2 and copper. All modeling and formulation of horizontal and vertical crack for the TSV package has been done by using ANSYS 2019 bundle specially ANSYS Mechanical is used to perform the analysis. The tetrahedron mesh profile is used for semi-elliptical cracks on the exterior surface of TSV using the software [42]. In the sub model 2, which is one of the symmetrical halves of sub model 1 the crack has been modeled. The sub model 2 was again subjected to the same reflow condition with importing cut boundary constraints from the sub model 1, which is the sub model of the quarter symmetry of the compact model with all detailed feature. Ten divisions with equal space have been taken for simulating the cracks along

the total length of TSV on sub model 2. When components are attached to the substrate under reflow condition thermal load is applied in 3D TSV package from 200℃ to room temperature in 300 s and keep it in room temperature for 50 s more. The plots with the relation between stress intensity factor (K) and crack locations have been shown in this study. Also, J-integral is shown in the following plots at different locations on TSV. The results show that the dielectric layer and copper core of TSV is much affected by these fracture parameters along with the change of top die thickness of the 3D package. To avoid propagation of crack, K should be less than Kc, i.e. K<Kc where Kc is fracture toughness of silicon [2], [3]. Also, by changing the material properties of the TSV the crack is modeled on both layers of these vertical interconnects to see the impact of it on package reliability.

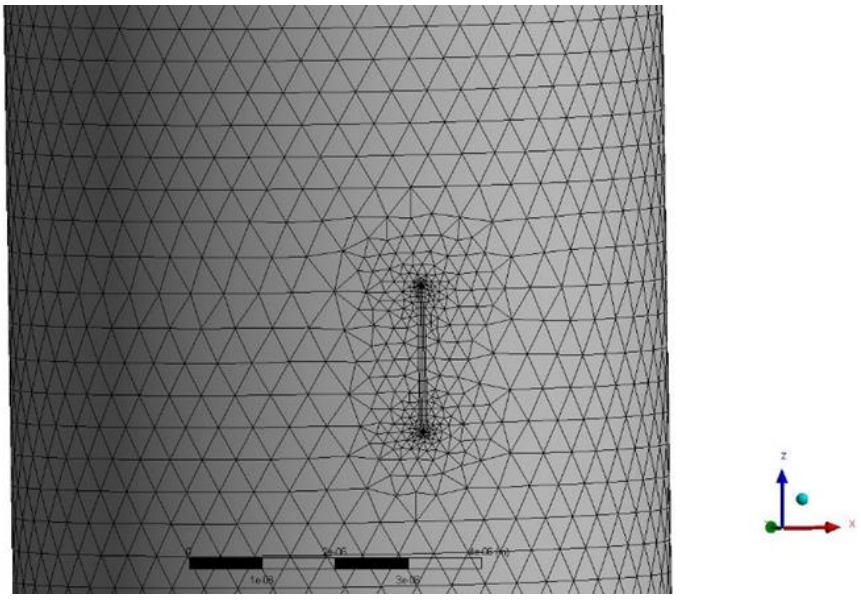

Fig. 29: Vertical crack induced on Cu core.

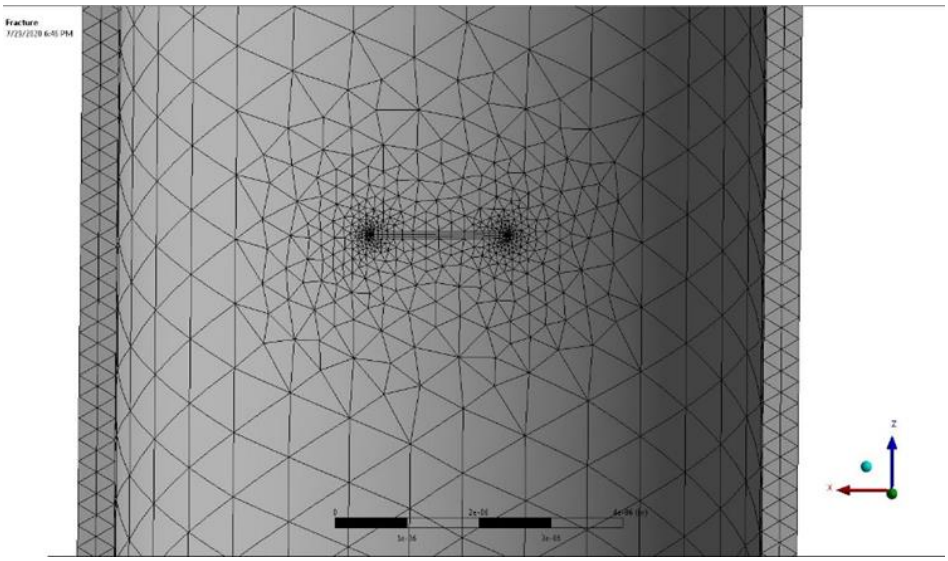

Fig. 30: Horizontal crack induced on SiO2 layer.

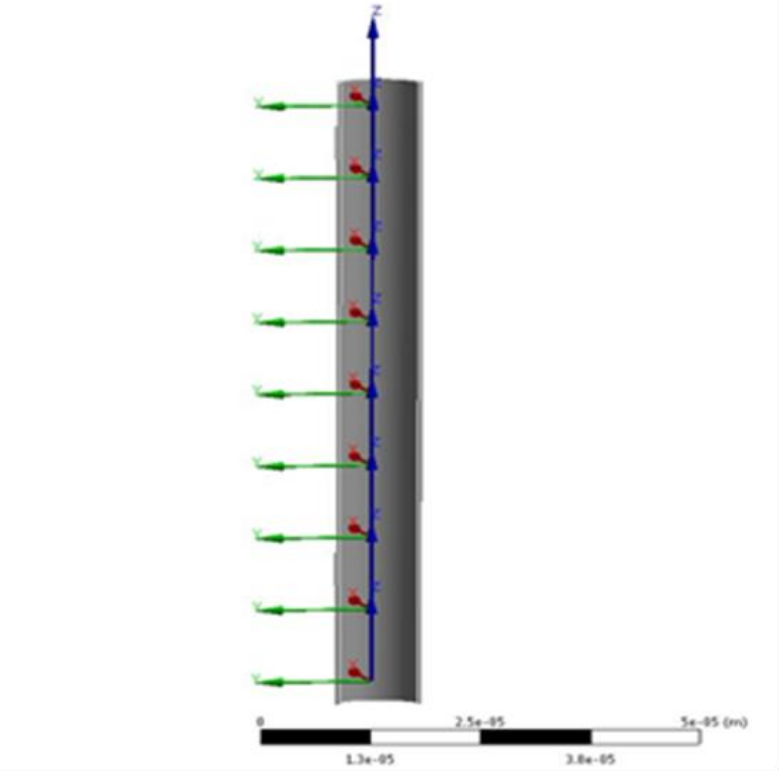

Fig. 31: Generation of crack coordinates on SiO2 layer.

1.4 Results and Discussions

The analysis of the results shows that the maximum equivalent stress of the global compact model with the changes of die thickness. The value of equivalent stress (Von-Mises) obtained after simulating under reflow condition for both Global Model and for unit cell. Figure 32 and 33 shows the change of the values of equivalent stress at Global Model and at unit cell respectively.

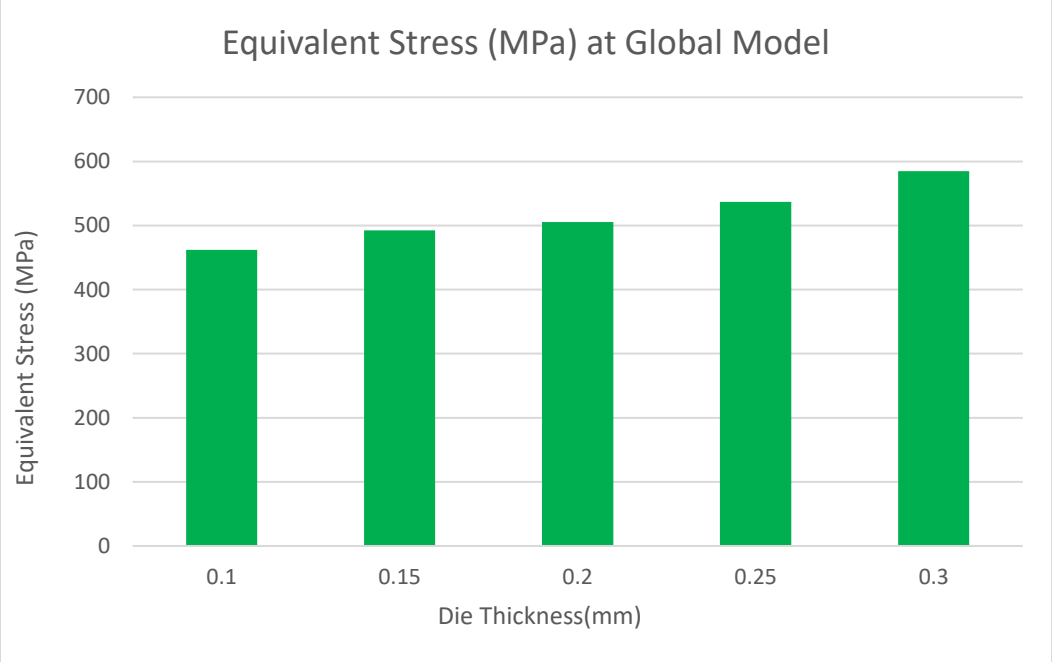

Fig. 32: Equivalent Stress on the Global Model.

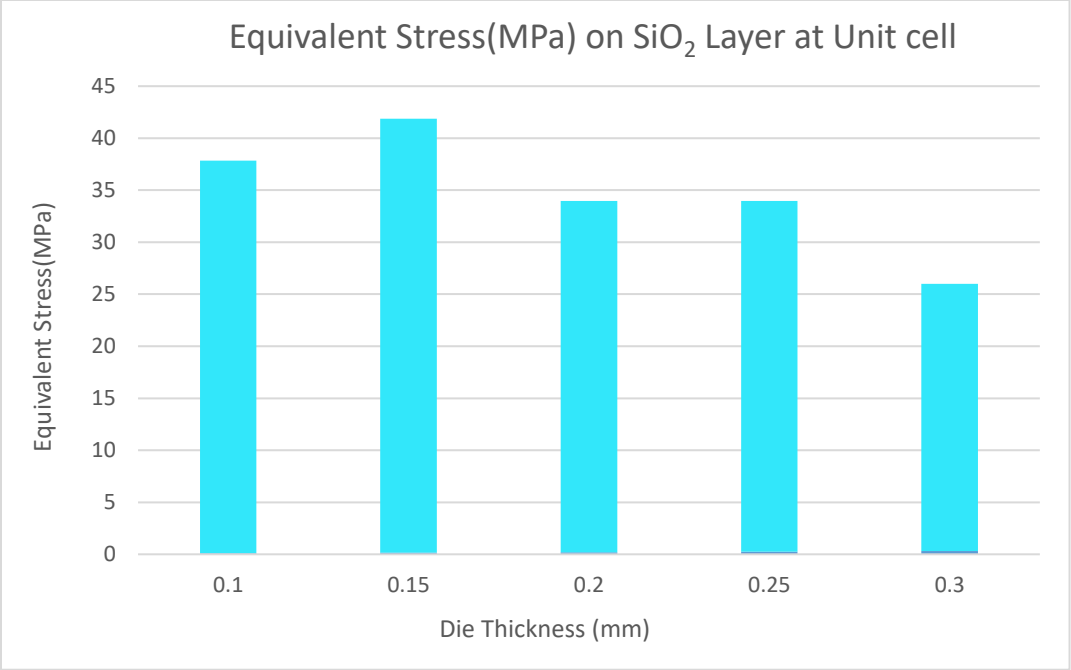

Fig. 33: Equivalent Stress on the Unit Cell.

From figure 32 and figure 33 it can be observed that among all the combinations of 2 die flip chip BGA package 0.1 mm die at a top and bottom is a good combination where the equivalent stress is low at the Global Model of the package. If the die thickness is increasing the stress goes up and if the thickness is decreasing more than that which also become another challenge to dissipate heat from very tiny region.

The crack behavior on TSV for both SiO_2 layer and Cu surface has been studied by the variation of die thickness to analyze if there is any notable change occurs in the value of J-integral and stress intensity factor which can impact the reliability issues of the package. Here the values of J-integral are shown in the following plots with respect to crack locations on TSV. The values are mostly changing in the top and bottom positions of the TSV on SiO_2 layer specially at 2nd and 8th locations. In all the observations the values of J-integral gradually changing in the 3, 4, 5 no

crack positions where at the top and at bottom the values changed drastically, which are more vulnerable parts of the TSVs.

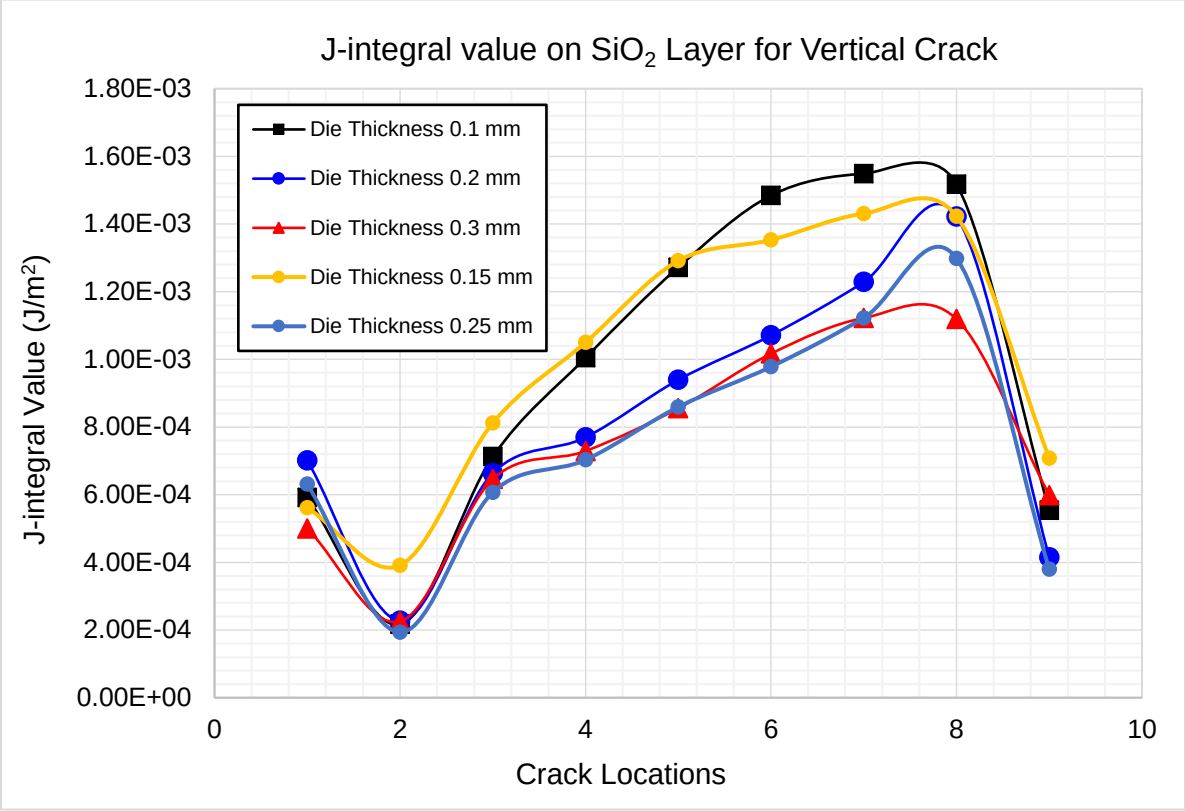

Fig. 34: J-Integral Value on SiO2 layers for Vertical Cracks.

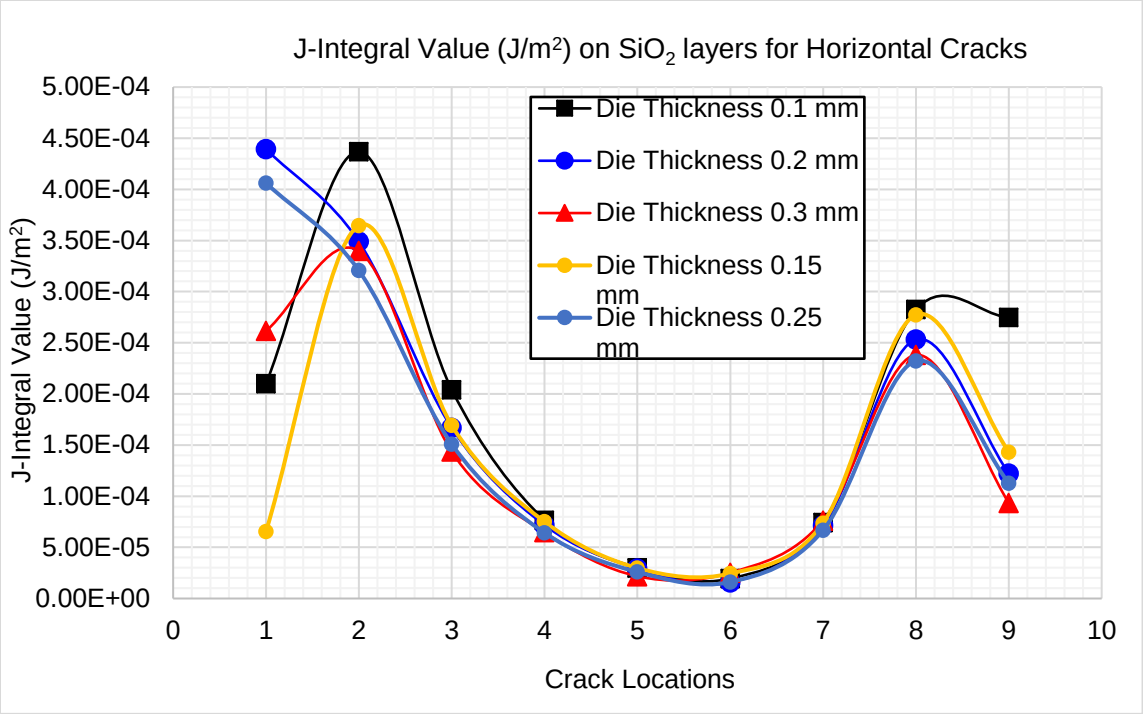

Fig. 35: J-Integral Value on SiO2 layers for Horizontal Cracks.

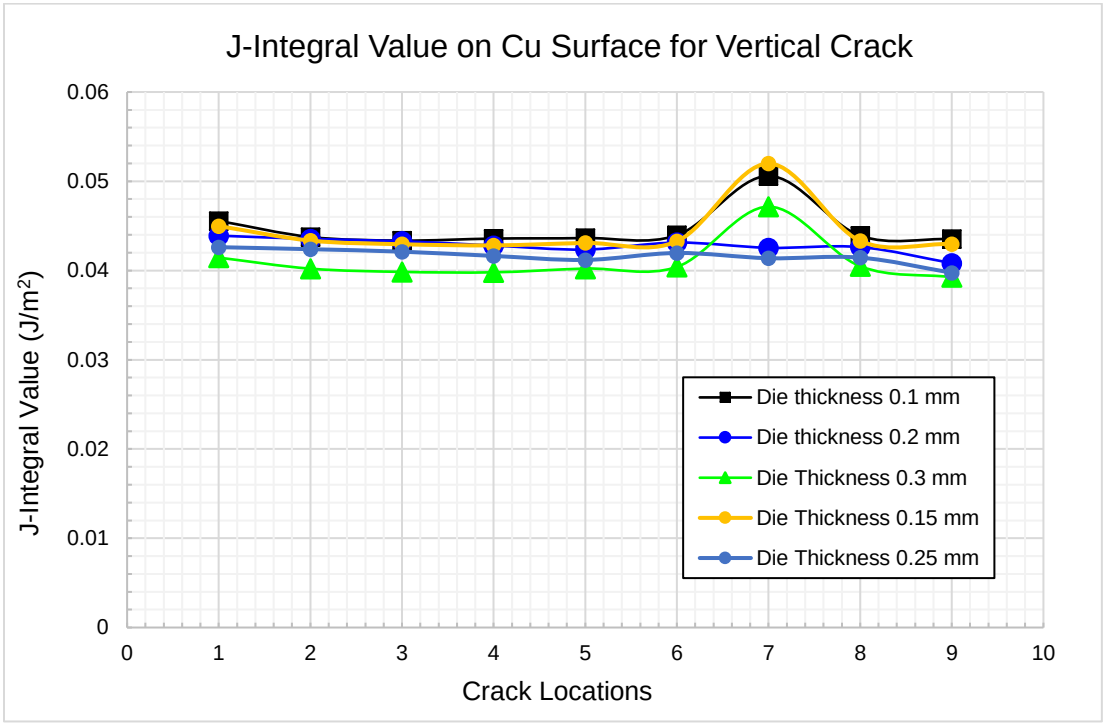

Fig. 36: J-Integral Value on Cu Surface for Vertical Cracks.

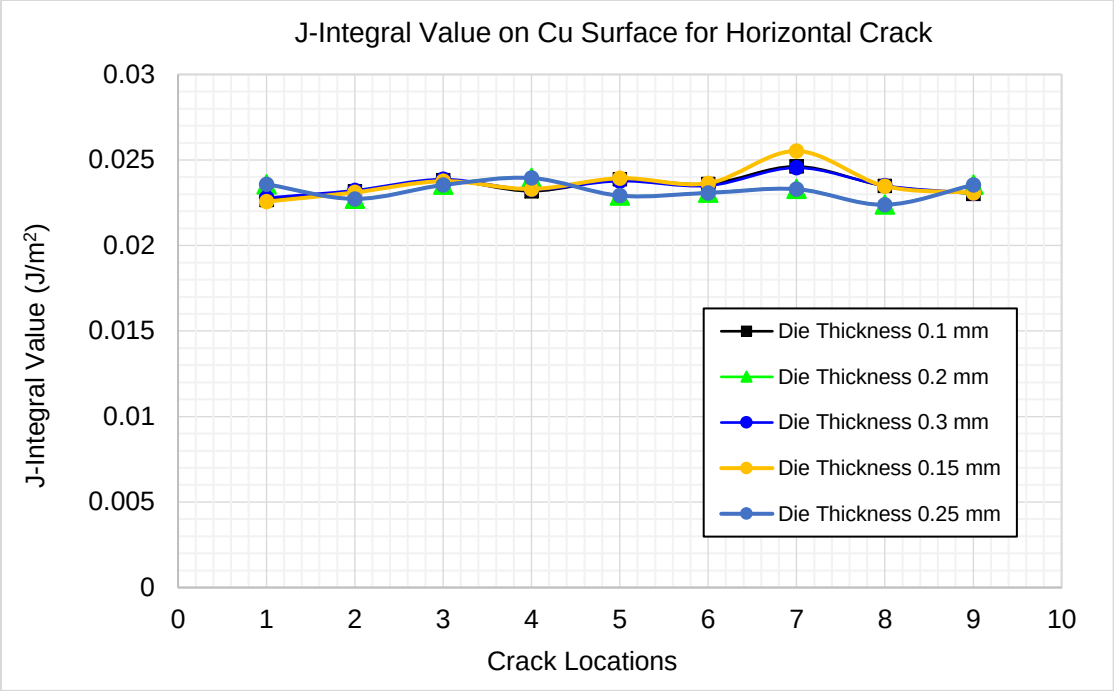

Fig. 37: J-Integral Value on Cu Surface for Horizontal Cracks.

Changing the top die thickness from 0.1 mm to 0.3mm the values of J-integral are analyzed from the above plots for different crack positions. From the observation of these plots above, the values of J-integral show consistent for all different variations except the top and bottom positions. When design such interconnects for vertical interconnections designer and engineering need to focus more on the top and bottom parts of the TSVs than the middle region to make the package more reliable.

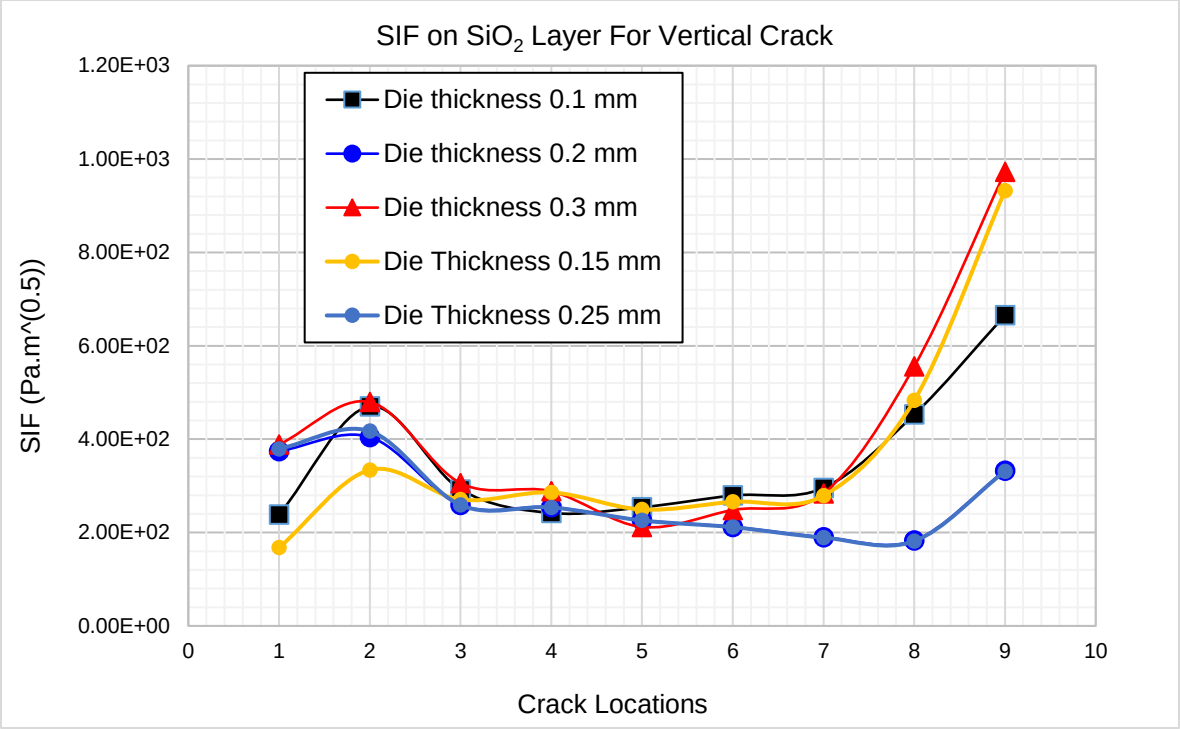

Fig. 38: SIF on SiO2 Layer for Vertical Crack.

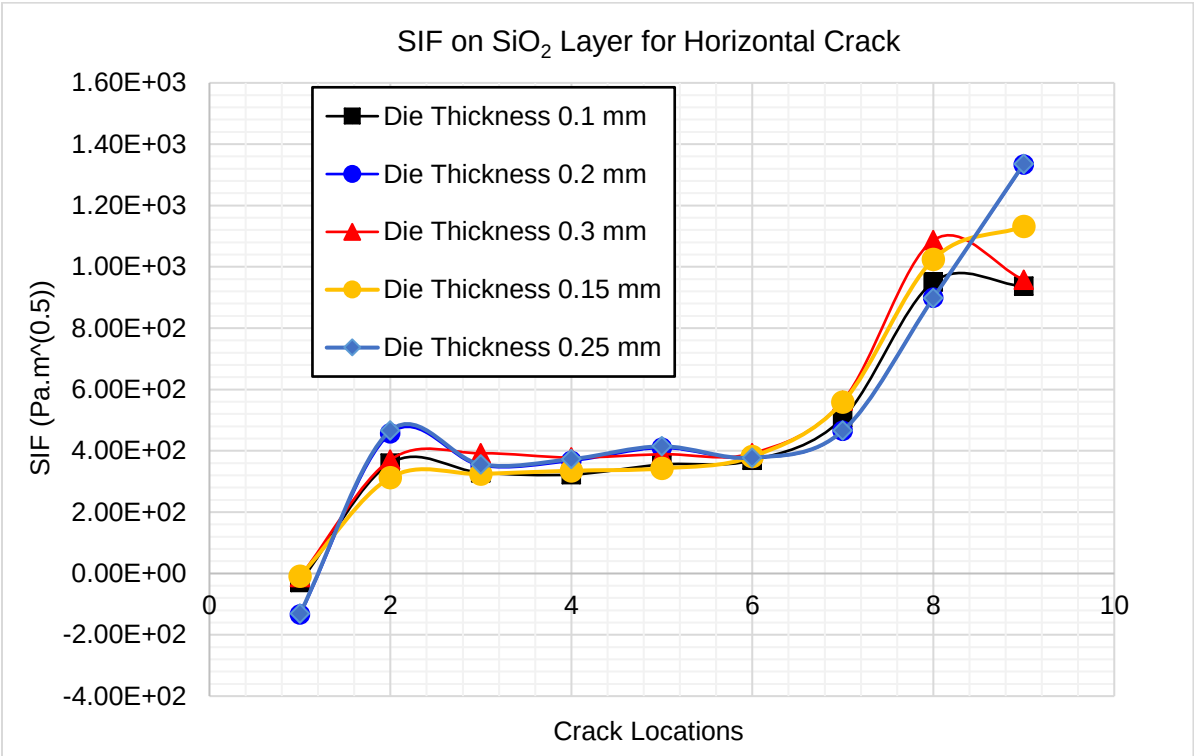

Fig. 39: SIF on SiO2 Layer for Horizontal Crack.

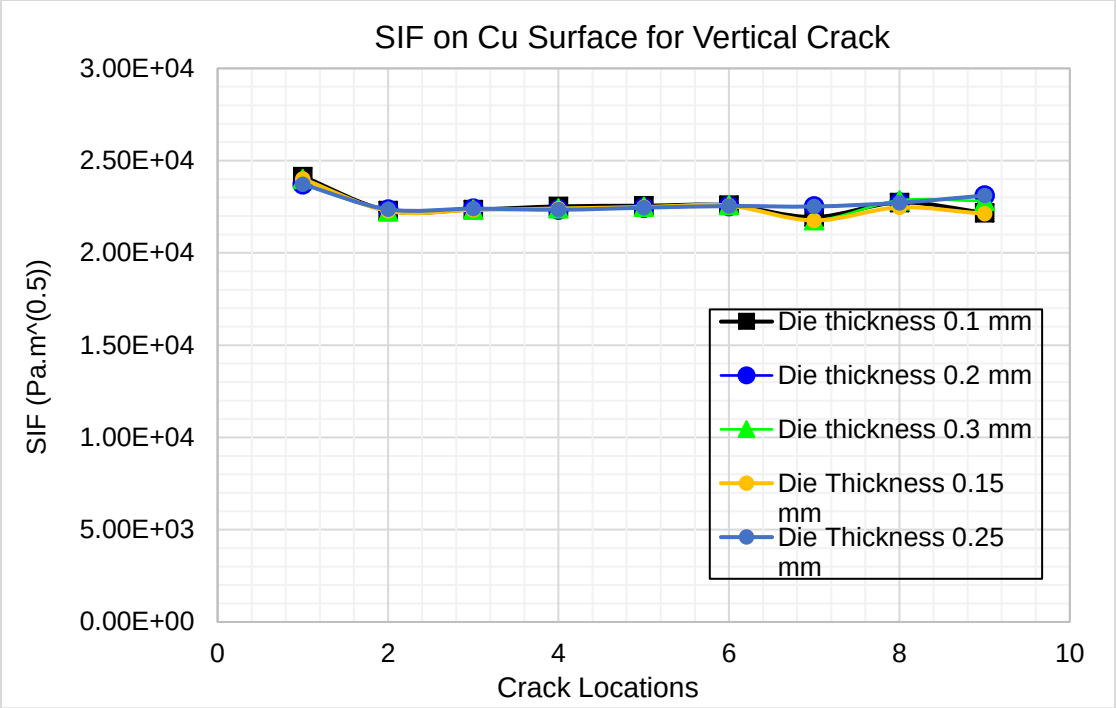

Fig. 40: SIF on Cu Surface for Vertical Crack.

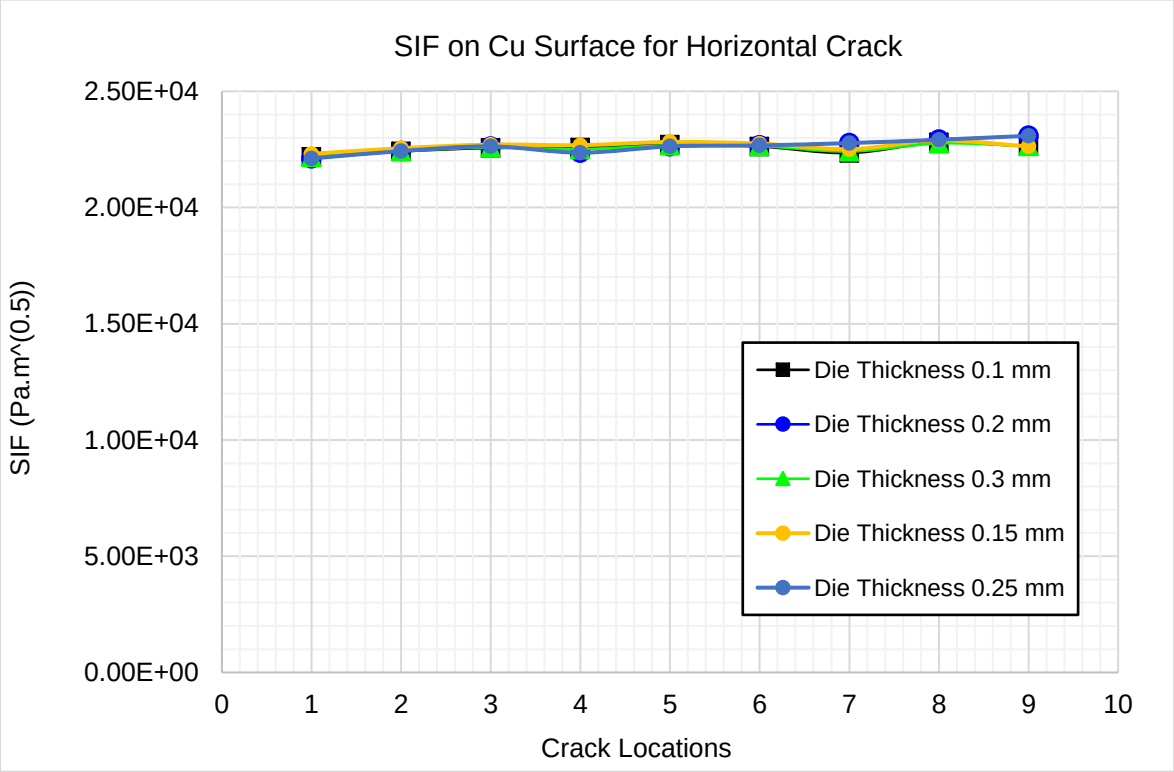

Fig. 41: SIF on Cu Surface for Horizontal Crack.

Conducting with thermo-mechanical reliability issues in TSV during the chip attachment process to the substrate under reflow conditions, thermal stress is developed due to CTE mismatch between Cu and SiO_2 layer of TSV. Fracture toughness of silicon crystal in nanometer-scale singular stress field varies with size such as length, width, and thickness of a specimen. It can be K_{IC} = 0.83 to 1.35 $MPam^{1/2}$ based on the size of the singular stress field [43]. Fracture toughness of thin-film SiO_2 deposited on silicon wafers via plasma enhanced chemical vapor deposition and measured by micromachined devices is 0.77± 0.15 $MPam^{1/2}$ [44]. From the above plots stress intensity factor (SIF) for various top die thickness is shown at different positions on TSV where the values of SIF are less than fracture toughness of SiO_2. From the analysis of stress intensity factor on SiO_2 layer it is observed that the value is low at initial positions where at the end the values are high enough [45]. But in the middle region it is almost giving uniform values. Here it can be highlighted again that the middle region of the vertical interconnects is more reliable than the top and bottom positions. As SiO_2 is a brittle material the change in the value of SIF is more prominent here than the change in Cu core as Cu is a ductile material [46]. Based on literature fracture toughness of copper films of different thickness varies from 800 nm to 100nm can be predicted from R-curve concept is K_{IC} = 7.81 ± 1.22 MPa$m^{1/2}$ to 2.34 ± 0.54 MPa$m^{1/2}$. In figure 40 and figure 41 the plots are showing the change in SIF with respect to different crack locations on Cu core of TSV where the results are steadier compared to SiO_2 layer on TSV. Observing all the results of SIF and J-integrals on TSV at both Cu core and SiO_2 layer it can be predicted that the middle of the TSV is susceptible to mode I cracking where the top and bottom region is more vulnerable to mode II and mode III cracking because of the fluctuation and the higher values of fracture parameters. From such observation structural integrity and signal integrity of these vertical interconnects can be analyzed.

1.4.1 Comparison of Material Properties of TSV

The comparison of material properties in this paper is done by two types of materials which are used for the Cu core of TSV. One is Cu elastoplastic and another one is Cu linear elastic.

- **Cu Elastoplastic**

Metals like copper shows elastic behavior for small loads. When the load is increased the material can undergo plastic deformation. Such materials are called elastoplastic [47]. To define an elastoplastic material, Isotropic as the symmetry type and Elastoplastic as the Stress-Strain Response on the Material Definition dialog box need to be selected. The change in stress with the change of plastic strain is shown in figure 42.

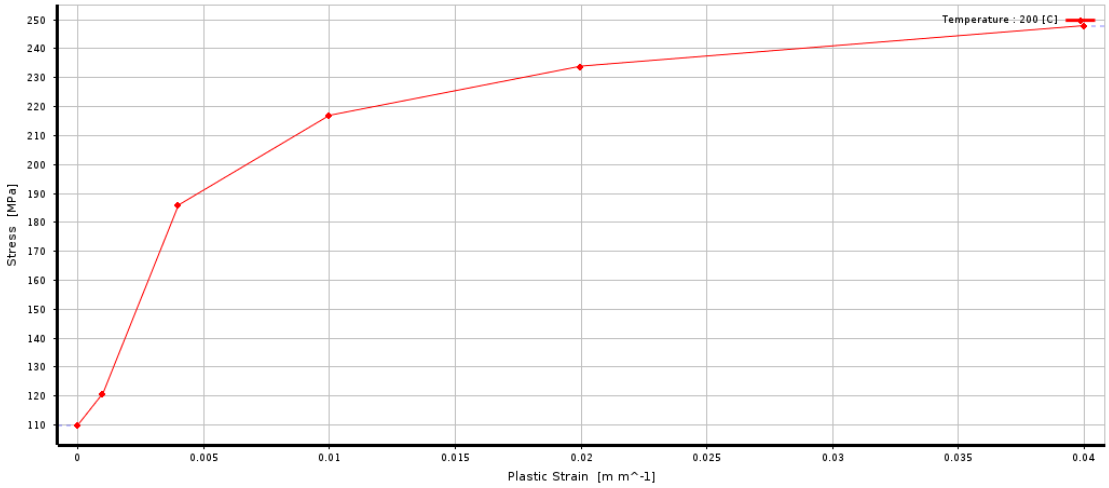

Fig. 42: Cu Elastoplastic.

- **Cu Linear Elastic**

In Cu linear elastic material, the relationship between stress and strain in the material is proportional. After removing the load linear elastic material will return to the unloaded state without any permanent deformation [48]. The change in Young's modulus with the change of temperature is shown in figure 43.

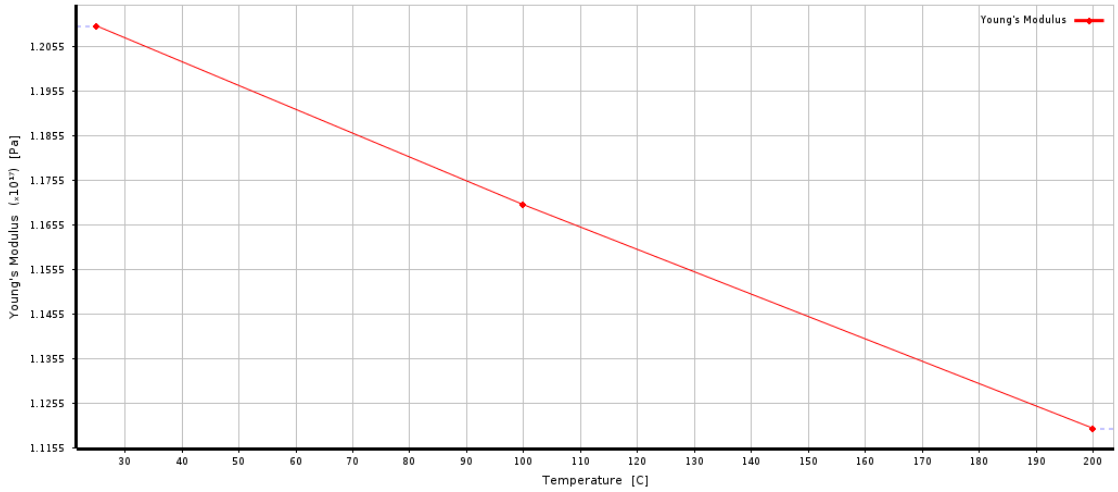

Fig. 43: Cu linear elastic.

By applying these two material properties for Cu core of TSV under reflow condition here the plots are shown the values of J-integral and stress intensity factor (SIF) with respect to crack positions by varying top die thickness from 0.1mm to 0.3mm. Material properties of a TSV, Back End of Line (BEOL) and solder bumps are important to escalate the reliability of the 3D package. Because of CTE mismatch and due to high thermal stress crack and warpage may develop in the region so the choice of material property is very influential here to maintain a good quality of signal passing between the interconnects without any leakage current for 3D integration.

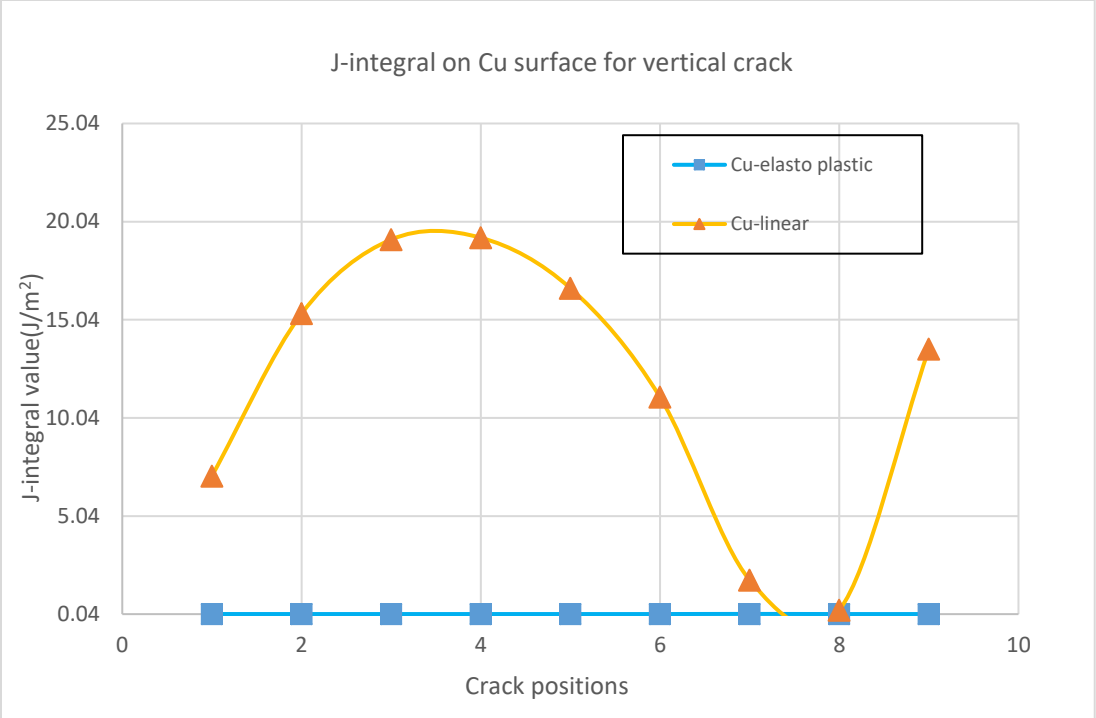

Fig. 44: J-Integral Value on Cu Surface for Vertical Cracks.

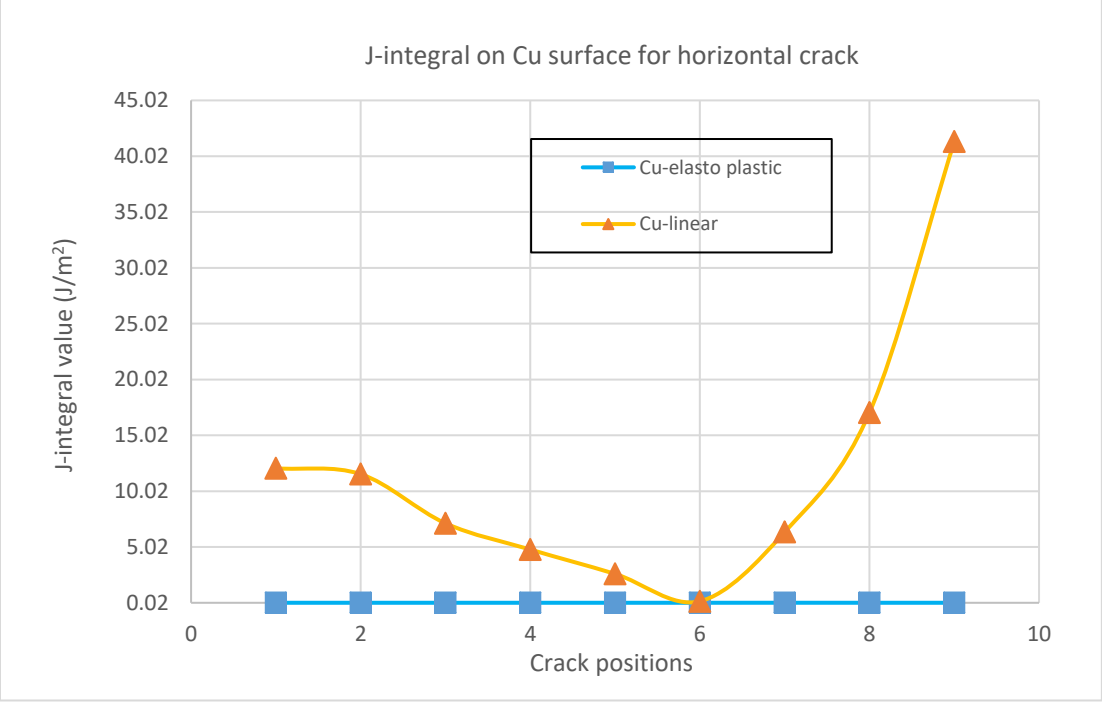

Fig. 45: J-Integral Value on Cu Surface for Horizontal Cracks.

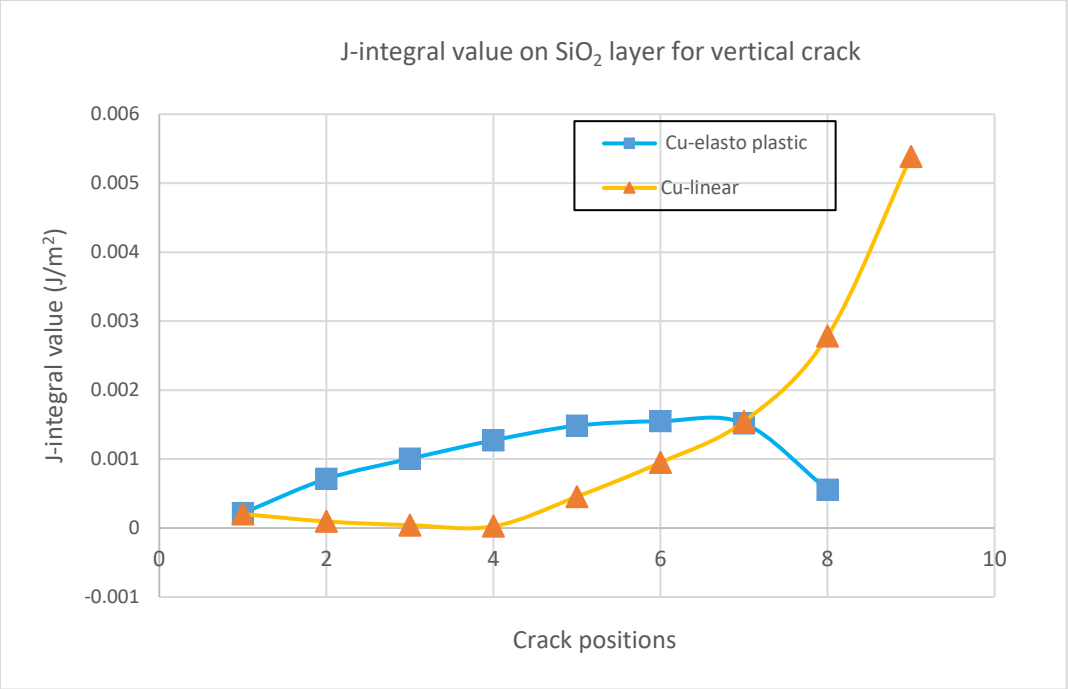

Fig. 46: J-Integral Value on SiO2 layers for Vertical Cracks.

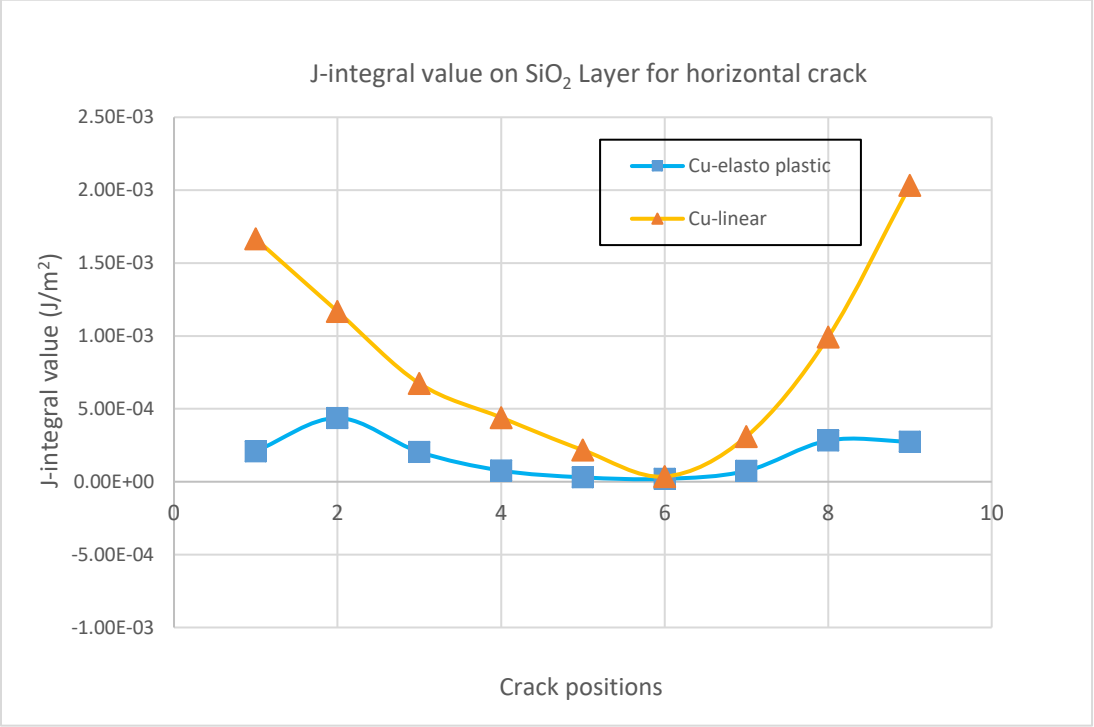

Fig. 47: J-Integral Value on SiO2 layers for Horizontal Cracks.

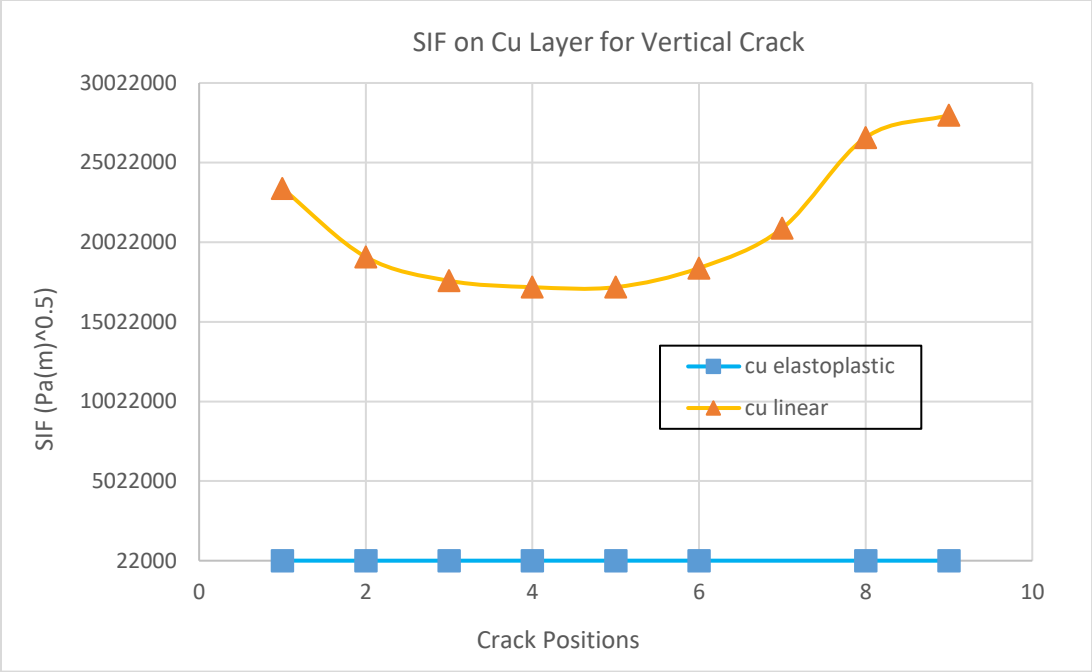

Fig. 48: SIF on Cu Surface for Vertical Crack.

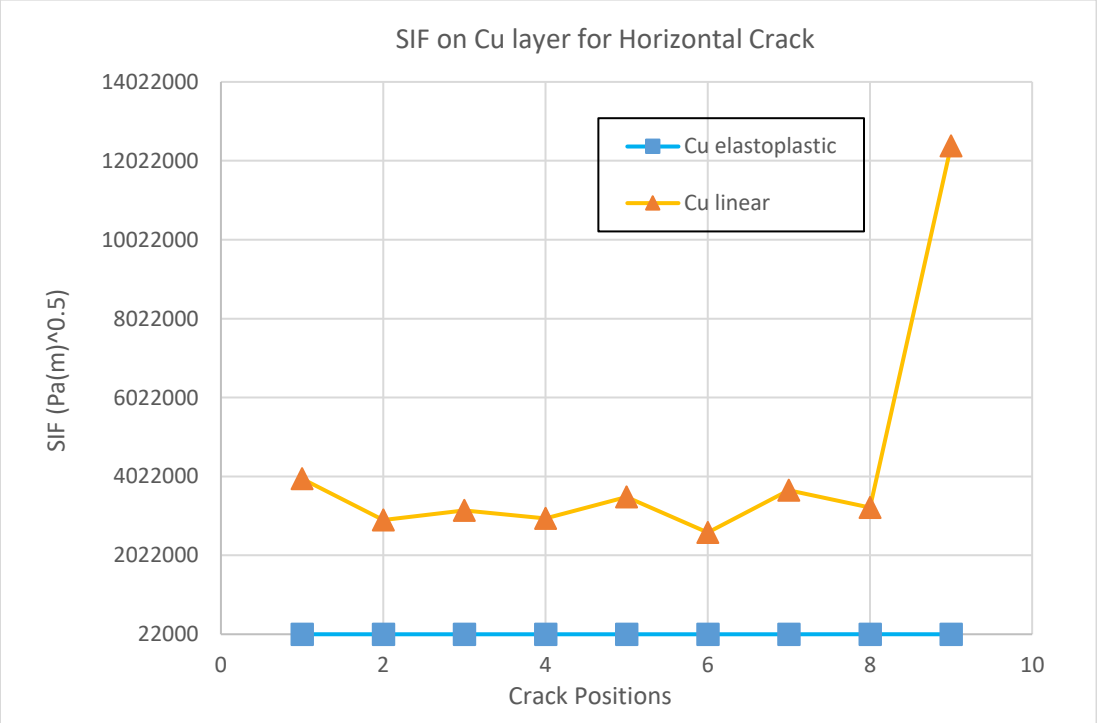

Fig. 49: SIF on Cu Surface for Horizontal Crack.

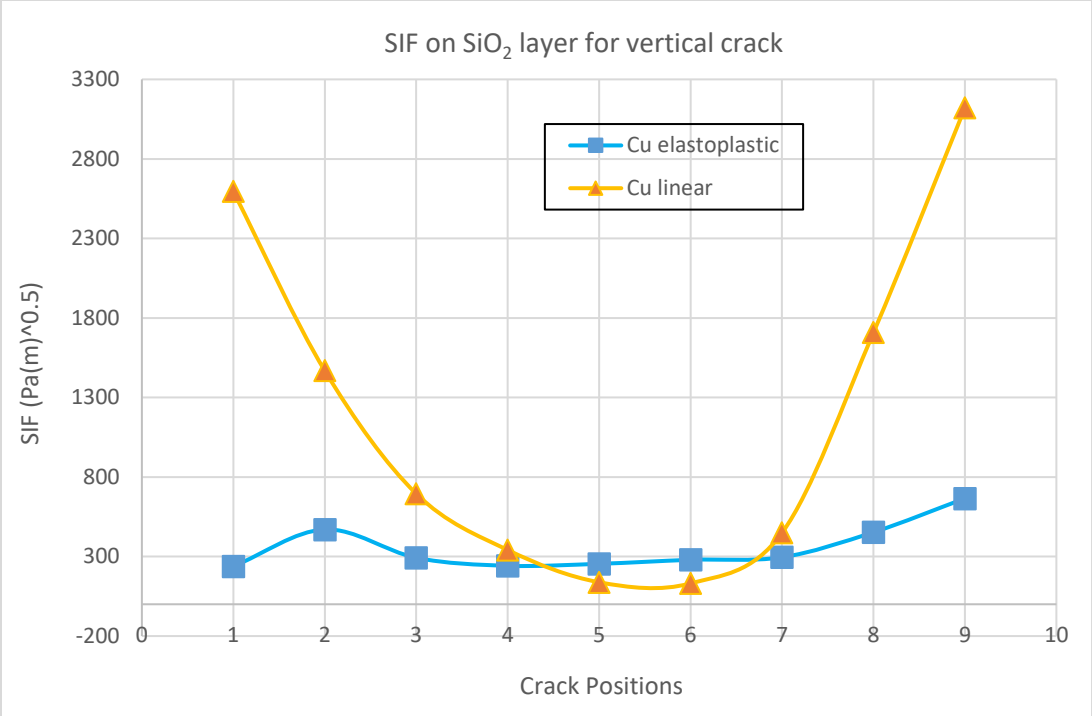

Fig. 50: SIF on SiO2 Layer for Vertical Crack.

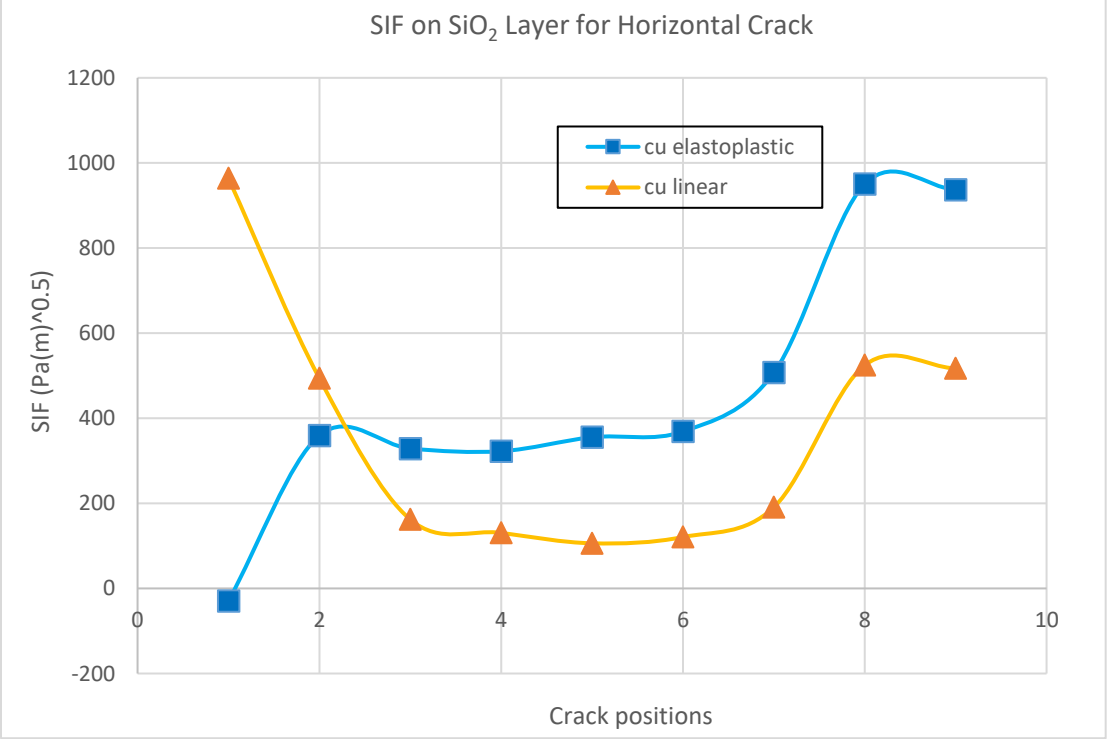

Fig. 51: SIF on SiO2 Layer for Horizontal Crack.

In all the cases, it is found that for Cu linear the values of J-integral and stress intensity factor (SIF) are high and changing more rapidly than the values of J-integral and SIF for Cu elastoplastic. When the values of J-integral and SIF are high it is more susceptible to the propagation of crack as the strain energy release rate per fracture will become high for that. Comparing these two material properties of Cu core of TSV it is predictable that Cu elastoplastic can be a suitable choice and more reliable for a 3D integration than Cu linear elastic material.

1.4.2 Thermal Cycling

Thermal cycling is a method which can determine the stability of the region that are more vulnerable to crack such as- solder joint, BEOL and interconnects of electronic devices under thermal load for a certain period of time. The standard that used here to analysis the equivalent stress of the whole global model of the 2-die flip chip BGA package is JEDEC standard JESD22-A104D. The temperature changed from -40℃ to 125℃ for 10800 seconds to see how it can impact the reliability of the vertical interconnects of the package through this cycling [2], [38].

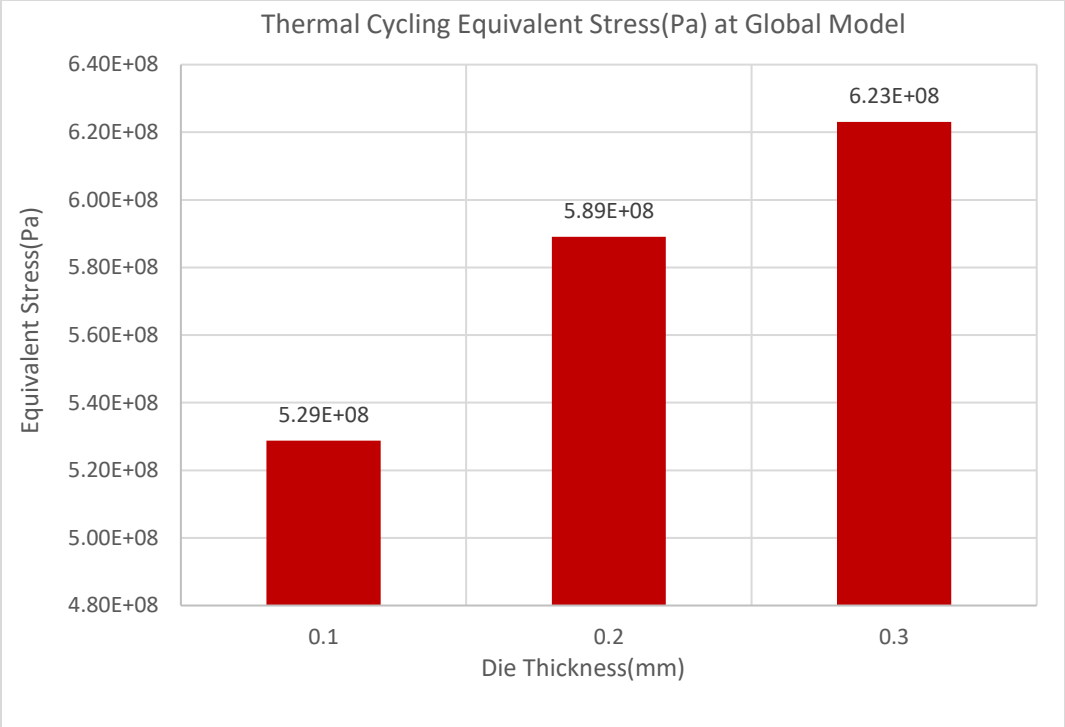

Fig. 52: Equivalent Stress on the Global Model.

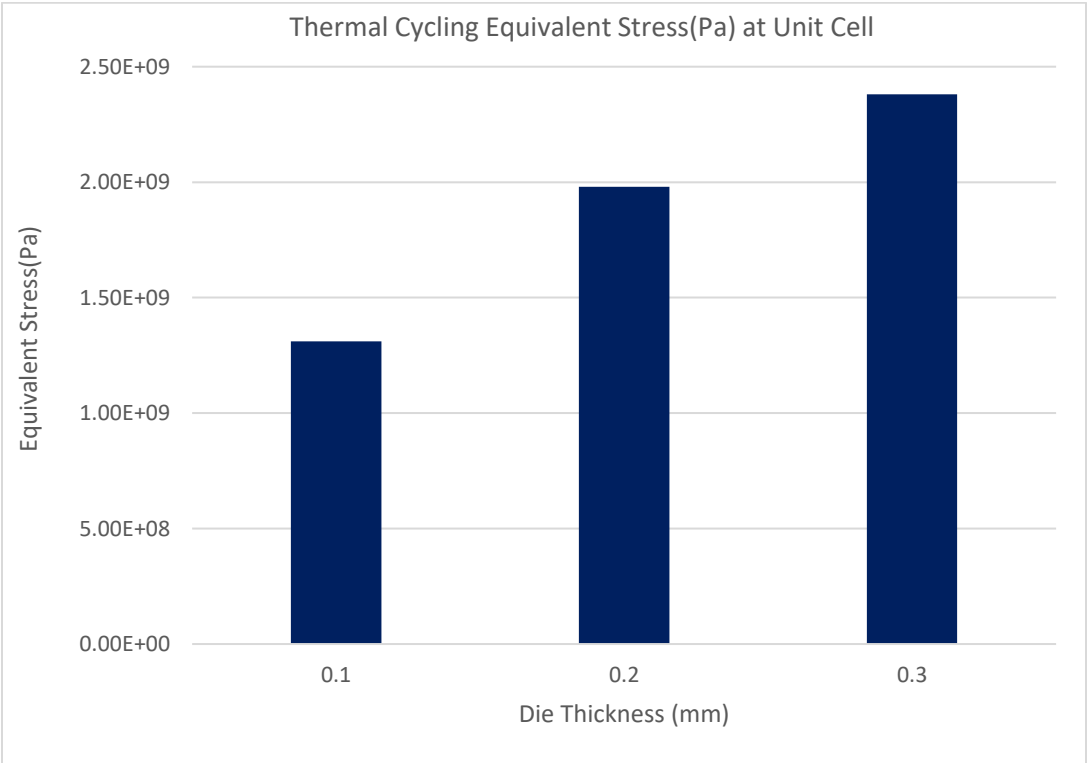

Fig. 53: Equivalent Stress on the Unit Cell.

After the analysis of Thermal Cycling plots for both Global Model and unit cell it can be observed that 0.1 mm thickness for both top and bottom die is the best combination for 2 die flip chip BGA package as the equivalent stress for this combination is less than the other two. Also, if the size of the die gets increased more it will increase the dimension of the whole package and if it got decreased it will become difficult to dissipate heat from that very little surface area. Considering all these and after studying the result it can be shown that 0.1 mm top and bottom die is a good combination and reliable design for 3D integration.

1.5 Conclusion

3D integration which includes 3D IC packaging, 3D IC integration and 3D Si integration is a vast field of science which can be explored in a variety of way to improve the multifunctionality of the electronic devices with reduced cost and better signal processing time. In this analysis structural optimization of the package has been done to perform the computational analysis of the fracture parameters of the vertical interconnects of the system to give a reliability assessment about 3D integration using through silicon vias (TSVs). Also, by comparing the material properties of the components of the 3D interconnects it is shown that the fracture parameters changed drastically with the change of the characteristics of the material properties of such components of electronic systems. It is very crucial to make a proper selection of materials for the vulnerable parts of 3D integration such as TSVs, micro bumps, solder balls and BEOL to improve package reliability. To conclude, along the length of TSV on both SiO2 layer and on Cu core crack propagation has been successfully studied. Generation of fracture has been propitiously modeled in sub model 2 which is part of sub model 1 and simulation has been done by importing cut boundary conditions from global model to sub model 1 to address the areas susceptible to

different modes of cracking on TSV. For various locations at the vertical interconnect the values of stress intensity factor (SIF) and J-integral are analyzed and identified which modes are widespread in the different regions of TSV along the length. The variation of die thickness has also been properly leveraged to explore its effect on equivalent stress of the whole global model to predict a good combination of 3D integration. Stress intensity factor and J-integral has been analyzed at different locations of TSVs to state the stress near the crack tip and how it can impact the reliability issues of a package. Also, changing the material properties of the vertical interconnect stress intensity factor and J-integral has been studied to identify which material properties are giving more reliable results for the 3D integration of the package [1]–[3].

1.6 Future Work

This study is important for optimizing the package geometry under reflow condition and thermal cycling condition and to understand the crack propagation depending on structural integrity and comparing the material properties of a 3D TSV package. Lots of new approaches related to TSV oriented research is possible and it seems to have a better extent for extensive study related to the optimization of design and reliability of heterogeneous 3D Integration. Not only the whole global model but different components of 3D IC integration or Si integration can be modified such as the design of the vertical interconnects, micro bumps, solder balls can be modified to optimize the structure for overall reliability enhancement of the electronic devices. For example, diameter of the vertical interconnects and height of the solder balls can be changed to see how it can affect the fracture parameters of 3D integration. Also, by comparing the material properties of different components of 3D integration the reliability issues of a 3D IC packages can be emphasized and necessary selections can be made to enhance the package reliability [2], [3]. Along with finite element analysis (FEA), computational fluid dynamics (CFD) analysis can be performed using ANSYS Icepak or fluent in order to find out the heat transfer coefficient of the components of 3D integration to determine the rate of heat dissipation which is a critical issue of electronic devices when applied stacking of dies on top of another. Lots of research have been done and several innovative ideas have been applied on the fabrication process of 3D integration, but more works need to be focused on the structural optimization, material selection and reliability enhancement of the components of electronic devices.

Chapter 2: ANALYSIS OF RHEOLOGICAL PROPERTIES OF PARTICLE BASED THERMAL INTERFACE MATERIALS

2.1 Introduction

As electronic devices are developing with multifunctionality and getting denser, lighter with reduced cost heat dissipation is becoming a critical issue to maintain package reliability. In electronic devices when two components are placed on top of another because of the surface roughness some void exists in between those mating parts which increase thermal resistivity and hamper heat dissipation of the system. Thermal interface materials (TIMs) enhance thermal coupling between two mating parts of electronic devices which increase thermal conductivity by minimizing the resistivity or void between two adjacent parts and improve thermal management of the package. Total thermal resistance of thermal interface materials depends on the bulk thermal resistance (R_{bulk}) of the thermal interface material and thermal interfacial resistances (R_c) of the interfaces between thermal interface materials and the chips and thermal interface materials and the heat spreader. In the heat transfer of electronic devices thermal contact resistance plays a significant role [5].

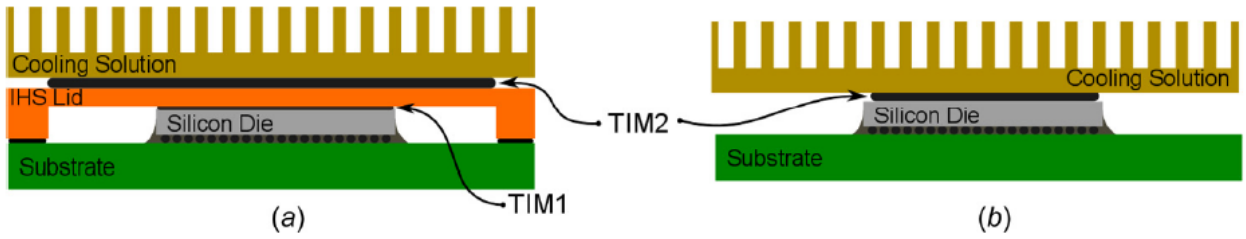

Fig. 54: Schematics of typical flip chip package cooling solution (a) TIM 1 between the silicon die and the lid (b) between the silicon die and the heat spreader [5].

When thermal interface materials are placed in between two components of electronic devices thermo-mechanical stresses can develop because of the mismatch of coefficient of thermal expansion (CTE) which can create delamination of TIMs. For a thermal interface material with known bond line thickness (BLT) and bulk thermal conductivity (K_{TIM}) which delaminates from the adjacent part can be externally pressurized to reduce thermal resistance.

$$R = \frac{BLT}{K_{TIM}} + R_{c1} + R_{c2}$$

When thermal interface materials are placed between two surfaces of surface roughness σ and the bulk thermal resistance R_{bulk} for thermal conductivity and the contact resistance of the mating parts are R_{c1} and R_{c2} then the total thermal resistance for such scenario is given below by figure 2.

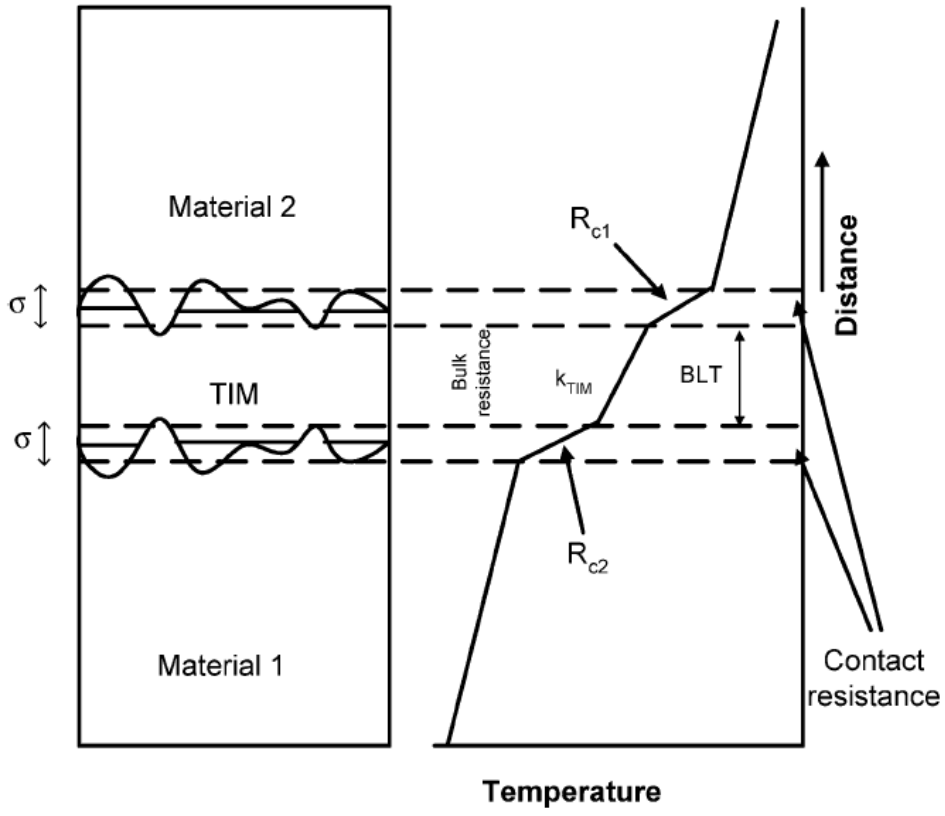

Fig. 55: The schematic of total thermal resistance of thermal interface materials between two adjacent parts [49].

2.1.1 Ideal Characteristics of TIMs

Ideal characteristic of thermal interface material:

➢ High thermal conductivity

➢ Low thickness

➢ Deformable

➢ Maintain performance indefinitely

➢ Manufacturable

➢ Stay in place

Fig. 56: Thermal Interface Materials [50].

2.1.2 Types of TIMs

There are several types of thermal interface materials exist commercially such as:

- Elastomeric pads
- Greases
- Thermal paste compound
- Thermal conductive gap fillers
- Phase change materials
- Solder

Fig. 57: Thermal Paste Compound.

Among all different types of TIMs particle laden thermal interface materials are one of the broadly used materials in microprocessor cooling solutions. Volume fractions of these conductive particles in TIMs increases the thermal conductivity of the materials [51], [52]. It also affects the bond line thickness (BLT) and other rheological properties such as viscosity of the thermal interface materials. Based on literature review it can be stated if the added volume fraction of such micro or nano particles exceed a certain limit it can increase the resistivity of the TIMs instead of increasing the conductivity of particle laden thermal interface materials (TIMs) and hence also affect BLT of thermal interface materials [53]. The BLT of these particle laden TIMs relies on rheological behavior such as viscosity, modulus, and yield stress of such materials. It is very important to measure the rheological properties of particle based thermal interface materials to understand about the performance of these TIMs as it has impact on the resistivity and can affect thermal conductivity of such materials [4]. In this study two types of commercially available micro particle based thermal interface materials is used to analyze the rheological properties of such materials. One type is TIM A, which is composed of carbon micro-particles and the other one is TIM B which is composed of silver, sub-micron zinc oxide, aluminum oxide and boron nitride particles [54], [55]. These thermal cooling compound pastes are used to cool down the temperature in Central Processing Unit (CPU) and Graphics Processing Unit by minimizing any void between the CPU and the heat sink or the GPU and the heat sink and hence reducing thermal resistivity and increasing the heat dissipation or thermal conductivity. These thermal cooling compounds do not contain any metallic particles so electrical conductivity would not be an issue. Using these two types of TIMs at room temperature the viscosity of these materials is measured with changing the shear rate by Discovery Hybrid Rheometer at different gap between the two parallel plates.

2.1.3 Viscosity of fluids

Density and specific weight are such properties of fluid which used to measure the heaviness of fluid, but these two properties are not sufficient to uniquely characterize the behavior of two different fluids. For example, with approximately close values of density the fluids can behave quite distinctively. In this situation some additional property such as viscosity plays an important role to determine the fluidity of the fluid. For common fluids for example water, oil, gasoline, and air the shearing stress is proportional to the rate of shearing strain and the relationship is given below:

$$\tau = \mu \frac{du}{dy}$$

Where the Greek symbol μ is known as absolute viscosity or simply the viscosity of fluid [56]. The values of viscosity vary for different fluids and for a certain fluid it highly depends on temperature. When the value of shearing stress is linearly related to the rate of shearing strain is known as Newtonian fluids according to Isaac Newton (1642-1727) and if such criteria is not maintained then those fluids are known as Non-Newtonian fluids. While no real fluids maintain perfectly the conditions for Newtonian fluids, but water and air are assumed as Newtonian fluids under certain conditions but non-Newtonian fluids are comparatively more common such as non-drip pain, molten polymers, many solid suspensions, blood and highly viscous fluids are example of non-Newtonians fluids. Generally, the viscosity of non-Newtonian fluids deepens on shear rate [56]. In order to characterize the non- Newtonian fluids measurement of rheological properties is one of the best ways to use to describe those fluids. In this analysis such measurement are taken place using discovery hybrid rheometer to characterize two different types of micro particle based

thermal cooling compound of electronic devices by studying the change of viscosity with respect to shear rate for different gap between the two parallel plates of the HR 2 rheometer.

Viscoelastic materials are generally show both elastic solid and viscous fluid behaviors. Elastic solids are such materials that follow Hooke's Law. That means for these materials stress is proportional to strain. On the other hand, the relationship between shear stress and the rate of strain of a viscous fluid is proportional with proportionality constant called viscosity. Viscoelastic materials show time and frequency dependent behavior and also need a function to express the behavior [57].

A temperature dependent viscoelastic material shows two regions to exhibit the behavior when it changes in a proper way and that two regions are glass transition temperature and liquid point. The temperature below glass transition will behave like solid or the temperature above liquid point will behave like viscous liquid [58]. And in between these two points means in between glass transition temperature and liquid point it behaves like viscoelastic materials [57].

Viscosity of such viscoelastic materials depend on some variables like temperature, frequency and strain amplitude so on. Along with the variables mentioned viscosity of viscoelastic materials also depends on the confinement between two plates where these materials are used [59]. One of the most familiar techniques to analyze the rheological properties of the viscoelastic materials is the rheometer, which is simple to use and largely used to investigate such properties. Based on literature it has been studied that the confinement between the two solid-liquid interfaces in the rheometer can show a transition from liquid-like behavior to solid-like behavior at a lower temperature and increasing the frequency or changing the composition which is known as *solidification through confinement* or *liquid to solid transition due to confinement* [57]. So, it is important to analyze the viscosity of viscoelastic materials with respect to shear rate at different

gap between two parallel plates of the rheometer to see how it can impact the rheological properties of such materials.

2.1.4 Storage Modulus and Loss Modulus

The ratio of shear stress to shear strain is known as shear modulus which also indicate the elastic shear stiffness of a material.

$$G = \frac{\tau_{xy}}{\gamma_{xy}}$$

Where G is the shear modulus, τ_{xy} is the shear stress and γ_{xy} is the shear strain [56].

Elastic behavior of a material can be measured by Storage modulus (E') and it estimates how much energy is stored in the materials. Viscous behavior of a material can be measured by Loss modulus (E") and it estimates how much energy is dissipating from the materials. In this study oscillatory sweep test is performed to get the idea of the microstructure of the viscoelastic materials. Microstructure shows there are forces between the molecules of the materials. To break the microstructure applied force needs to higher than the force holding it. If the applied force is lower than the inter molecular force, then E' is greater than E" that means energy stored in the material. And if the applied force is larger than the inter molecular force then E" is greater than E' where microstructure of the materials collapse, and it dissipates energy. In this analysis storage modulus and loss modulus of TIM A and TIM B with respect to angular frequency has been analyzed at room temperature and at different confinement between two parallel plates of HR-2 to see how the result varies with the change of angular frequency.

2.1.5 Literature Review

Ravi S. Prasher et al. in his paper used different types of greases and by adding volume fraction of conductive particle into it analyzed how it can affect the rheological properties of those thermal interface materials [4].

Patricia E. Rodrigues et al. in his paper studied the effect of confinement on viscoelastic materials by using rheometer and showed how the storage modulus of such materials changed with respect to gap thickness [57].

Ravi S. Prasher et al. in his paper analyzed contact resistance of curable polymer gel thermal interface materials in which the mechanical properties of such materials vary with rheological properties. He also proposed a novel method of determining the transition of grease type behavior to gel type behavior which is crucial for post reliability stress performance [49].

Vijay Subramanian et al. in his proposed mechanical characterization and it's challenges of thermal interface materials as it is very important for reliable performance of such materials in thermal management of electronic devices for extended period of time [60].

Le Hoang Sinh et al. in his paper invented a novel Aluminum Nitride/Liquid Crystalline Copoly (ester amide) Composite to use as Thermal Interface Materials and analyzed viscosities, thermal conductivities and dielectric properties of the TIM [5].

Wattana Sukhlaaied et al. in his paper investigated the variation of dynamic viscosity and shear stress-shear rate curves of poly (vinyl alcohol) (PVAM) and poly (vinyl alcohol)-graft-gelatin (PVAM-g-GT) solution using a rheometer and also studied the results that how the values of dynamic viscosities changing with the change of shear rate of the materials [61].

Abel Misrak et al. in his paper investigated the effect of thermal aging on the mechanical properties of thermally conductive gap filler materials. As degradation of mechanical properties due to thermal aging can affect the overall thermal performances of TIMs in electronic devices [62].

2.2 Materials and Experimental Technique

2.2.1 Materials

Two types of commercially available paste type thermal cooling compounds are used in this analysis TIM A and TIM B. TIM A is composed of carbon micro particle to increase the conductivity of the materials and TIM B is containing silver, sub-micron zinc oxide, aluminum oxide and boron nitride particles to enhance heat dissipation of the material. As these thermal cooling compounds contains polymerizable liquid matrix and huge volume fraction of electrically insulating but thermally conductive filler and also do not contain any metallic particles and it is applied as a paste form in between the CPU or GPU and cooling solution of electronic devices so electrical conductivity would not be an issue. Also, these TIMs consists of Al_2O_3 (Aluminum Oxide) is an electrical insulator with high thermal conductivity so, it dissipates heat and enhance thermal management of the system.

2.2.2 Experimental Technique

Discovery Hybrid Rheometer (HR-2) is a technique used to measure the rheological properties of materials at a largest range of measurement conditions. Modifications in core measurement technology allow more precise measurements with superior precision. HR-2 can be

applied to measure lower viscosities and storage modulus and loss modulus of weaker liquid, paste and soft-solid structures at a wide range with accuracy.

Fig. 58: Discovery Hybrid Rheometer.

Fig. 59: Discovery Hybrid Rheometer.

Discovery Hybrid rheometer (HR-2) provides low torque sensitivity which enables to measure lower viscosities and weaker intermolecular structures. In HR-2 it has feature such as Magnetic Thrust Bearing which lower the friction of the basic system by 70% and by minimizing high-pressure turbulent air flow from the measurement system, lower torques can be measured reliably and accurately [63].

Fig. 60: Magnetic Thrust Bearing of (HR-2) [63].

In HR-2 along with the Magnetic Thrust Bearing an Advanced Drag Cup Motor is integrated which improved torque precision and enhances the accuracy of all the measurement especially at low torques [63].

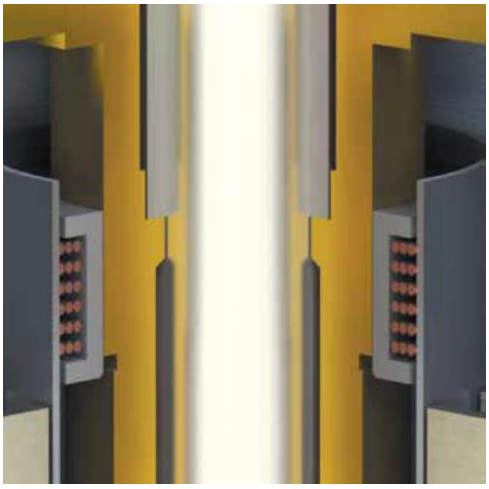

Fig. 61: Advanced Drag Cup Motor of (HR-2) [63].

In this study using HR-2 viscosity, storage modulus and loss modulus of TIM A and TIM B is measured with respect to the change of shear rate and angular frequencies respectively at 25°C

for various gap thickness between two parallel plates of the discovery hybrid rheometer. 40 mm diameter two parallel plates are used to perform the tests where sample are placed in between the two plates.

Fig. 62: Sample placed between two parallel plates of Discovery Hybrid Rheometer (HR-2).

The gap between two plates varies from 50 μm,70μm ,90 μm to 110 μm to perform the analysis of rheological properties of particle based thermal cooling compounds. The Soak time is 180 s and at 1% strain, the angular frequency varies from 100.0 rad⁄s to 0.1 rad⁄s. Superior dynamic performance provides better accuracy in characterizing the rheological properties of TIM A and TIM B.

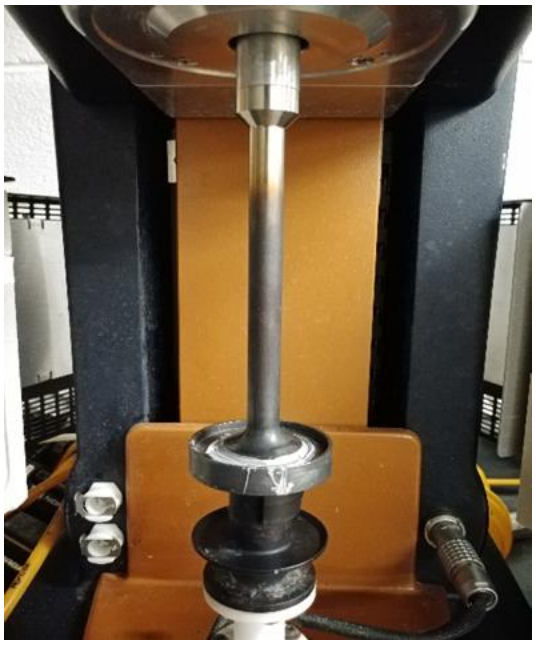

Fig. 63: Sample loading on Discovery Hybrid Rheometer (HR-2).

2.3 Results and Discussions

2.3.1 Viscosity vs Shear Rate of TIM A

TIM A is composed of carbon micro particles. Following the plots of viscosity with respect to shear rate at room temperature for different confinement between two parallel plates of HR-2 rheometer is given below. From the pattern of all the plots below it is shown that viscosity of TIM A is decreasing and showing almost constant values with the increasing shear rate for all different gap thickness. Based on literature it can be stated that this is happening due to the broken H-bonding as the energy of the H-bonding interaction is less than the energy of carbon-carbon covalent bonding.

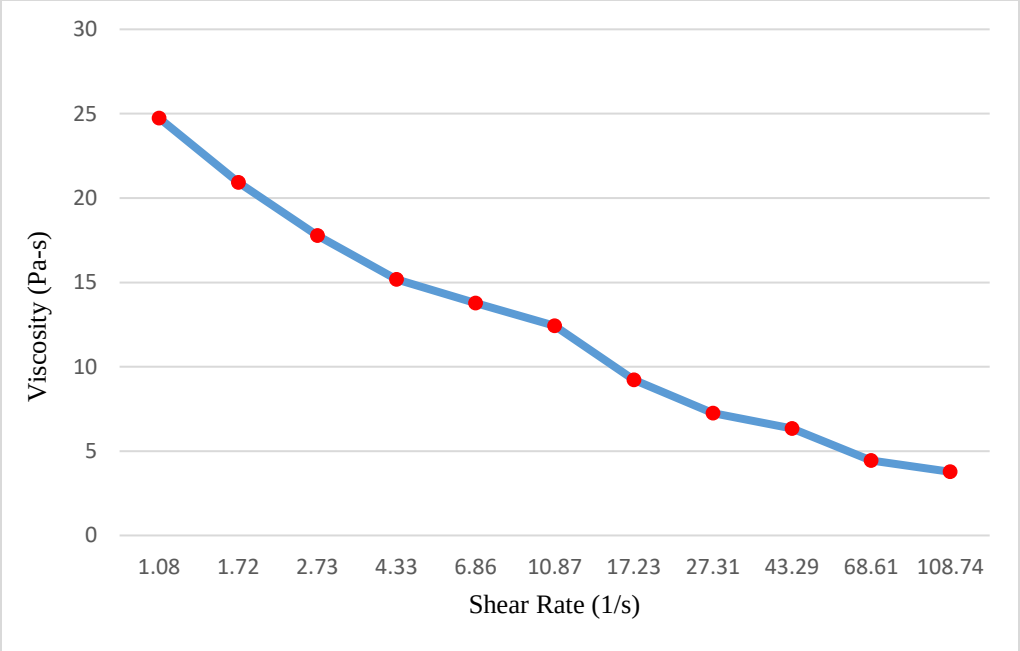

Fig. 64: Change of viscosity with respect to shear rate at 110 µm.

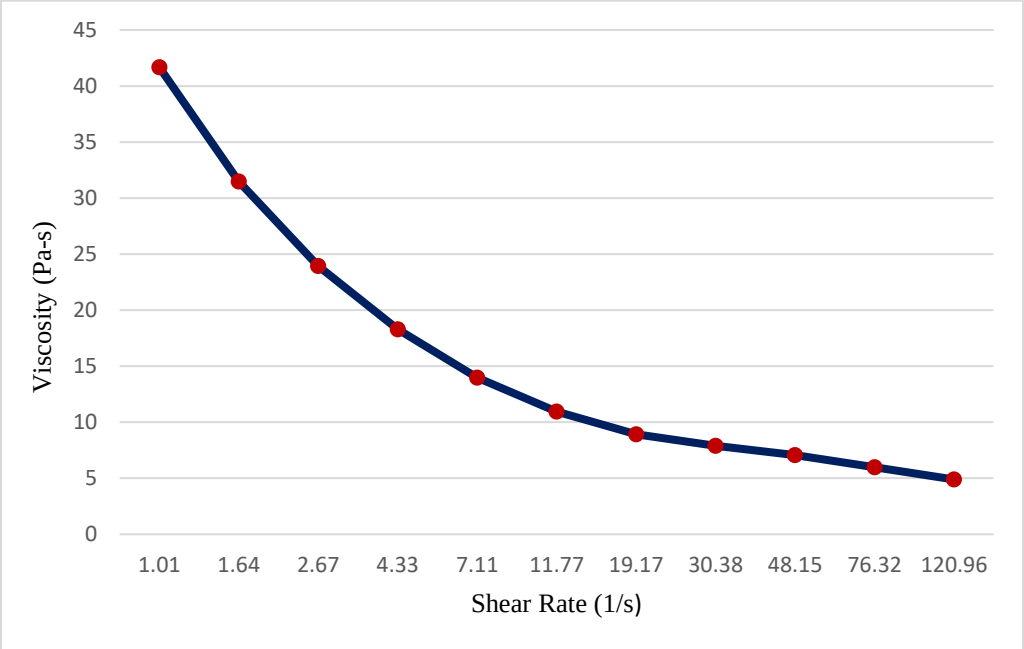

Fig. 65: Change of viscosity with respect to shear rate 90 µm.

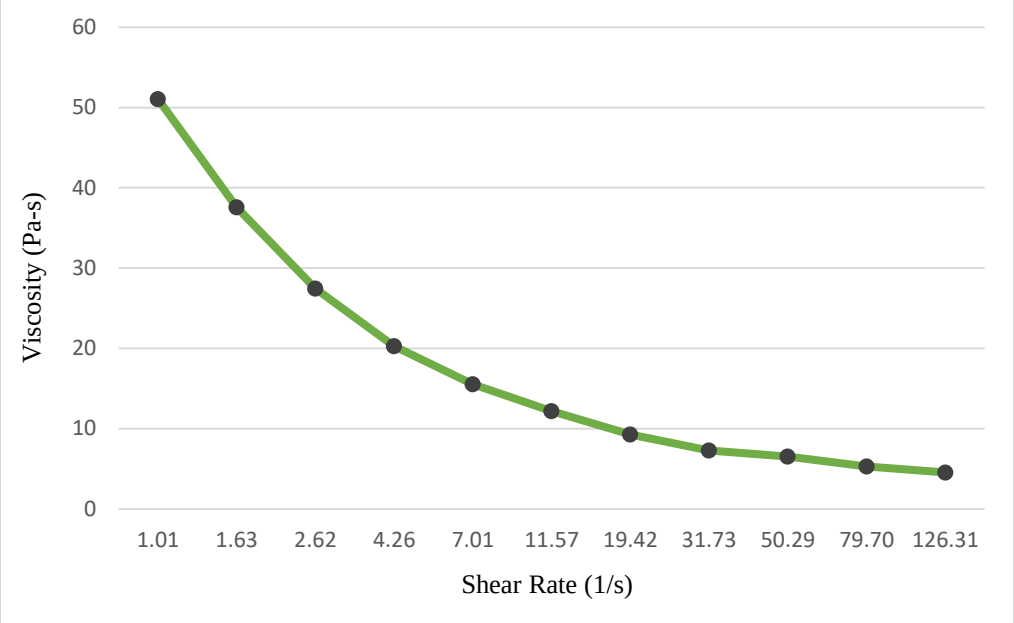

Fig. 66: Change of viscosity with respect to shear rate 70 µm.

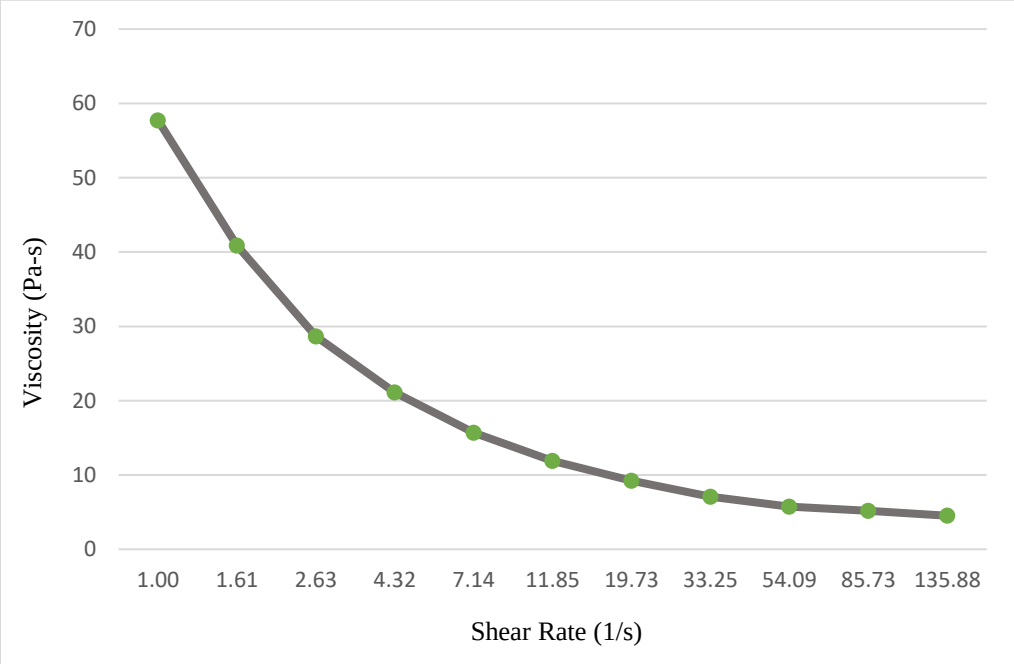

Fig. 67Change of viscosity with respect to shear rate 50 µm.

Analyzing the plots above it is shown that the viscosity of TIM A is increasing with the decreasing gap thickness between two parallel plates of HR-2. At reduced temperature and with increasing shear rate liquid through solid transition due to confinement could happen which can increase the viscosity of the thermal cooling compound at a higher rate and can create some issues at conformity of the TIMs when applied between two surfaces of electronic devices. When applying these thermal cooling compound in electronic devices this issue needs to be considered. Also, too low viscosity at a higher gap thickness can make pump out issue of these cooling compound. When powering up and powering down is happening because of the relative motion or in-plane and out-of-plane motion between the chip and heat spreader this cooling compound can squeeze out and can hinder the performance of it in an electronic device. These issues need to be examined before applying these cooling compound in any electronic system.

2.3.2 Modulus vs Angular Frequency of TIM A

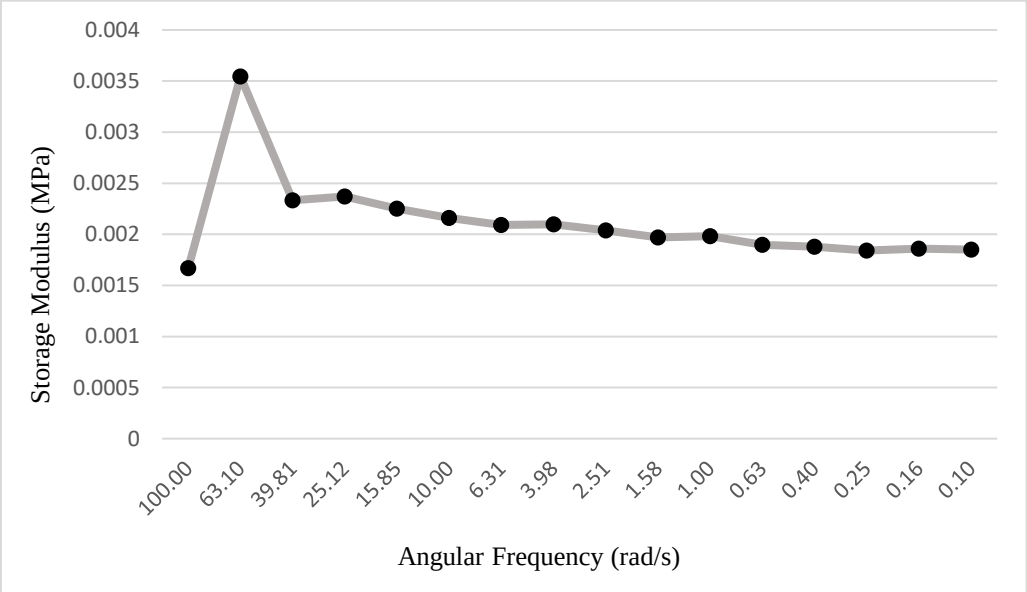

Fig. 68: Change of storage modulus with respect to angular frequency 110 μm.

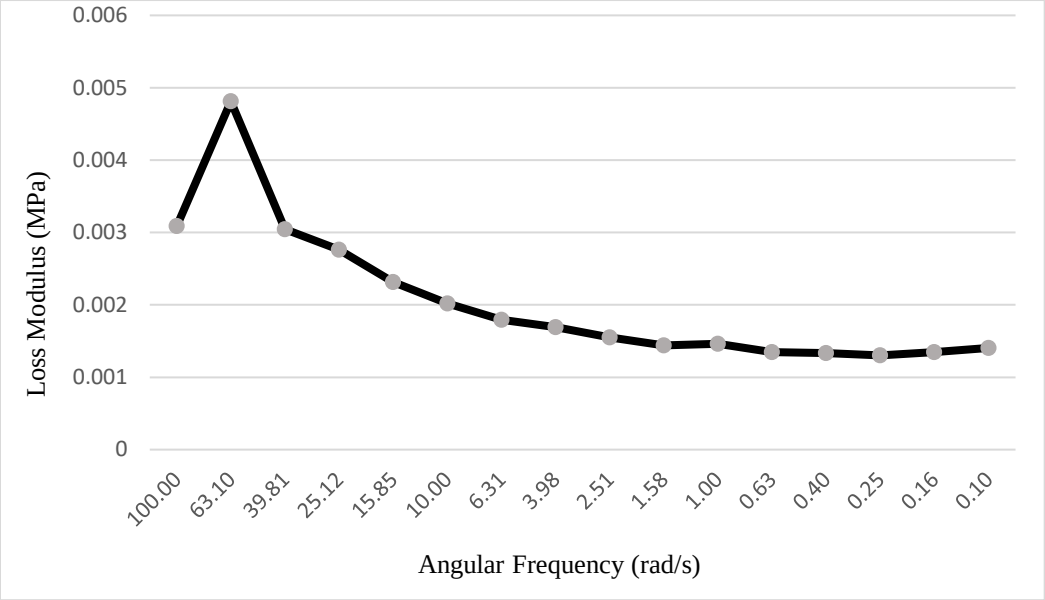

Fig. 69: Change of loss modulus with respect to angular frequency 110 µm.

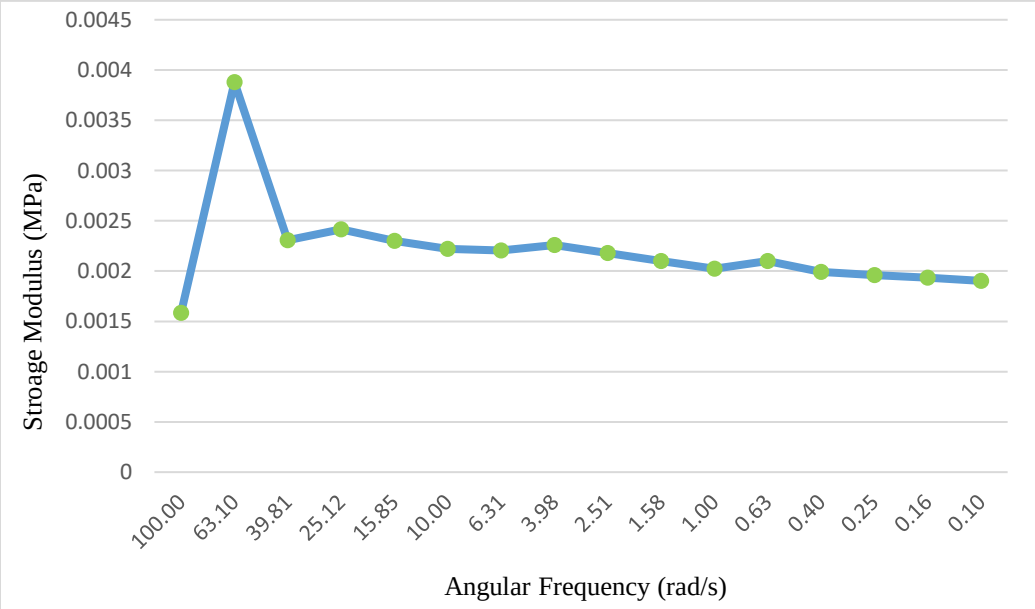

Fig. 70: Change of storage modulus with respect to angular frequency 90 µm.

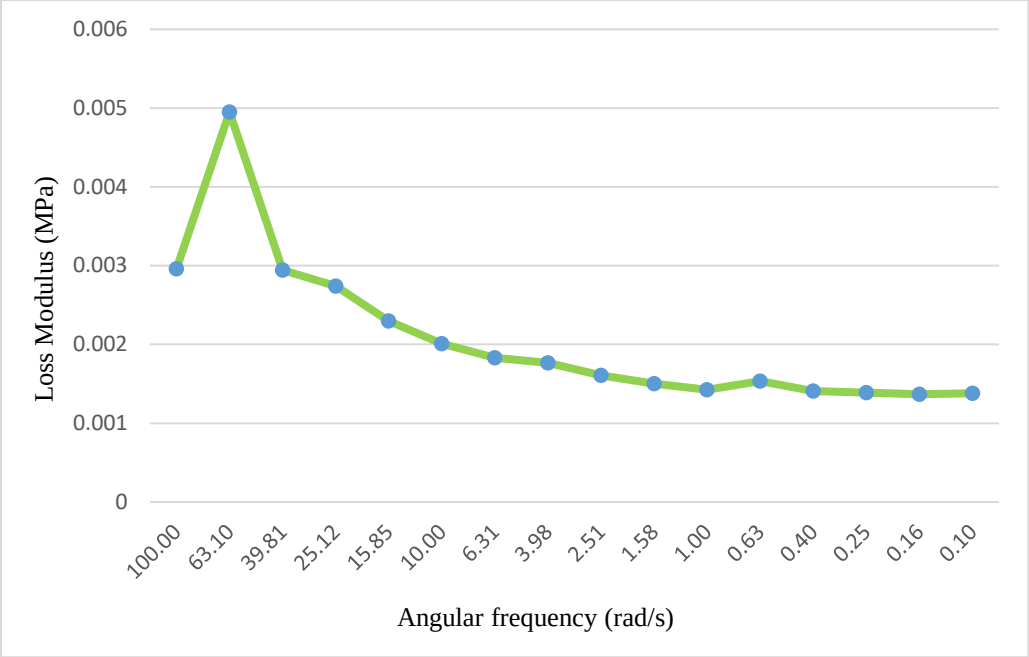

Fig. 71: Change of loss modulus with respect to angular frequency 90 µm.

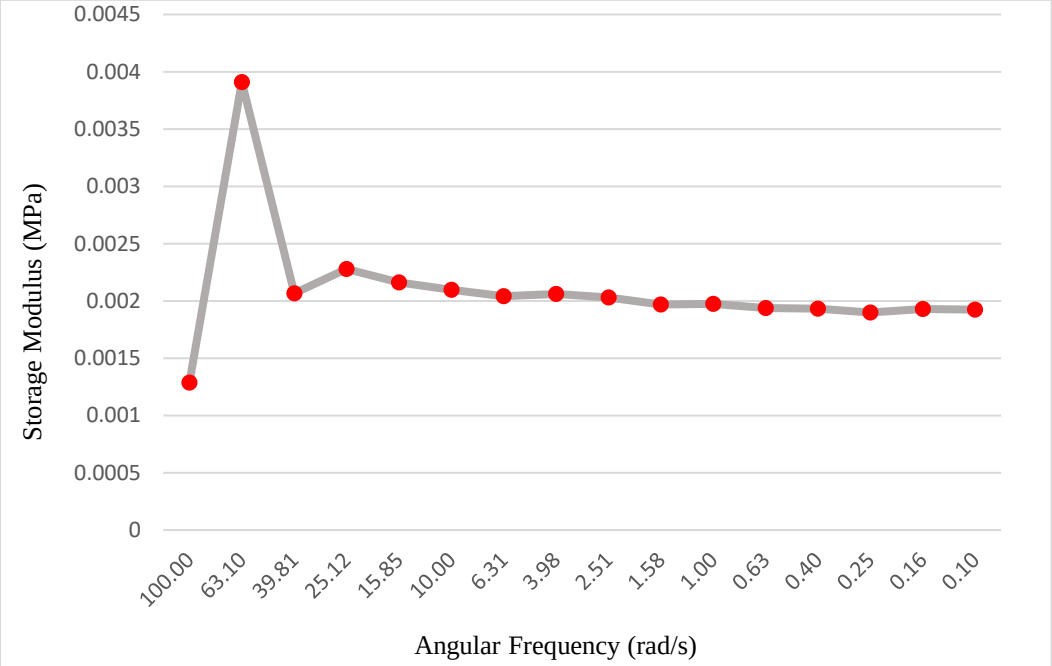

Fig. 72: Change of storage modulus with respect to angular frequency 70 µm.

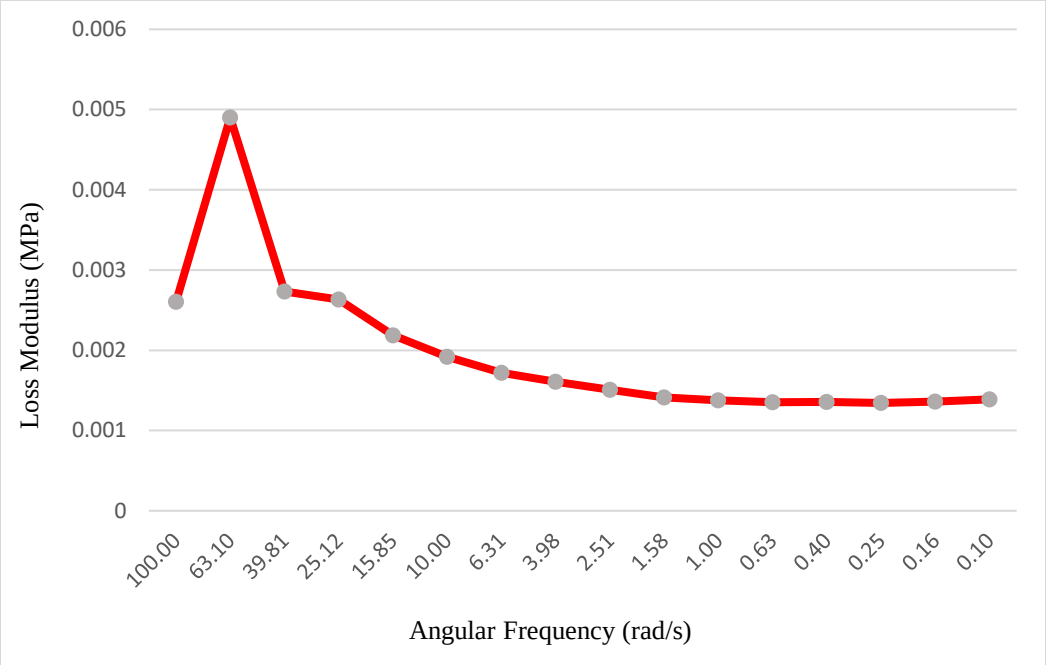

Fig. 73: Change of loss modulus with respect to angular frequency 70 µm.

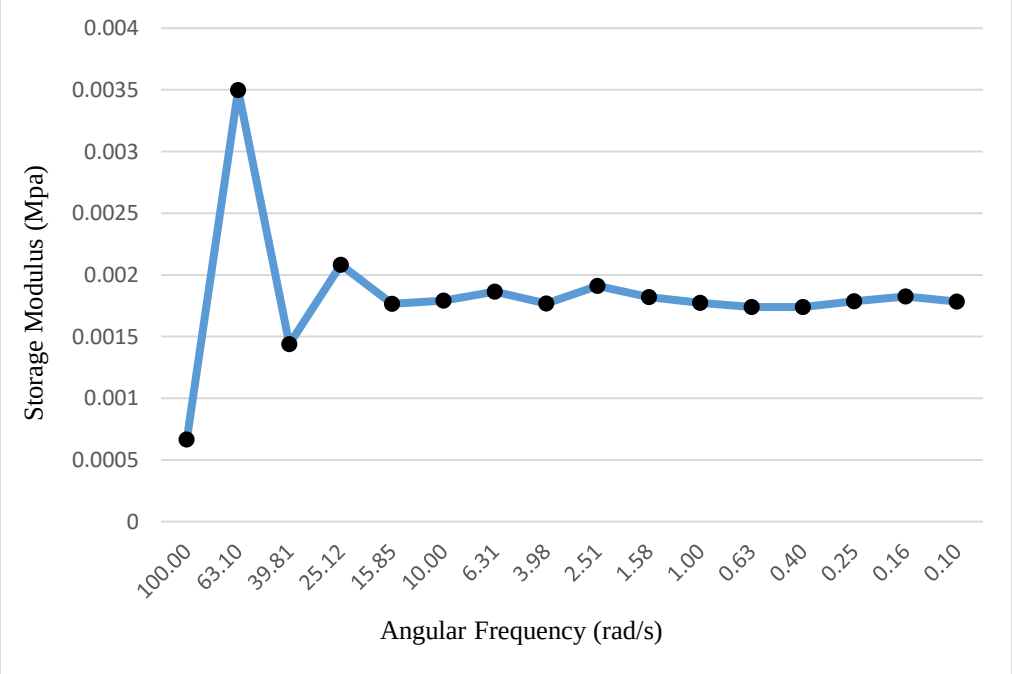

Fig. 74: Change of storage modulus with respect to angular frequency 50 µm.

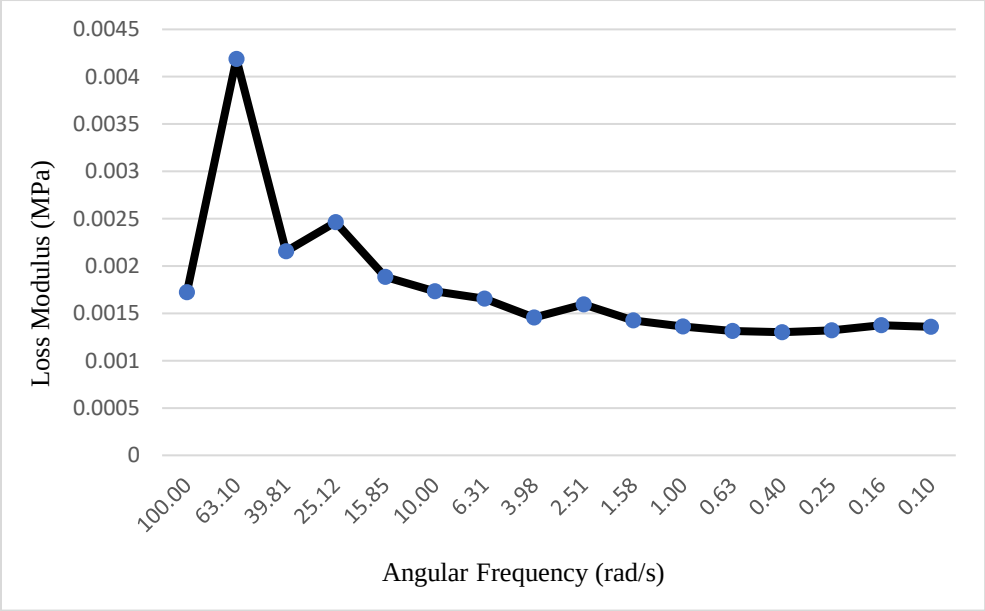

Fig. 75: Change of loss modulus with respect to angular frequency 50 μm.

The figures above show the change of storage modulus and loss modulus with respect to angular frequency at room temperature for different gap thickness between the parallel plates of HR-2. For all different gap thickness it is shown that storage and loss modulus increase with increasing frequencies and decrease with decreasing frequencies which support the material to flow for a longer time.

2.3.3 Viscosity vs Shear Rate of TIM B

The plots for TIM B, which is composed of silver, sub-micron zinc oxide, aluminum oxide and boron nitride microparticles is given below. The plots show the change of viscosity with respect to shear rate at room temperature for different gap thickness between the parallel plates of HR-2.

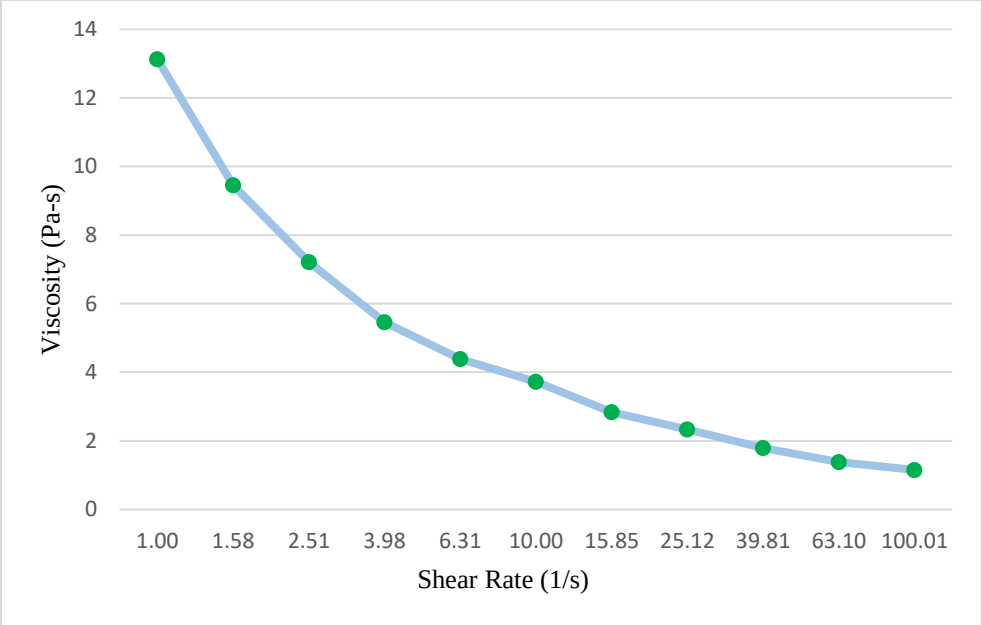

Fig. 76: Change of viscosity with respect to shear rate 110 µm.

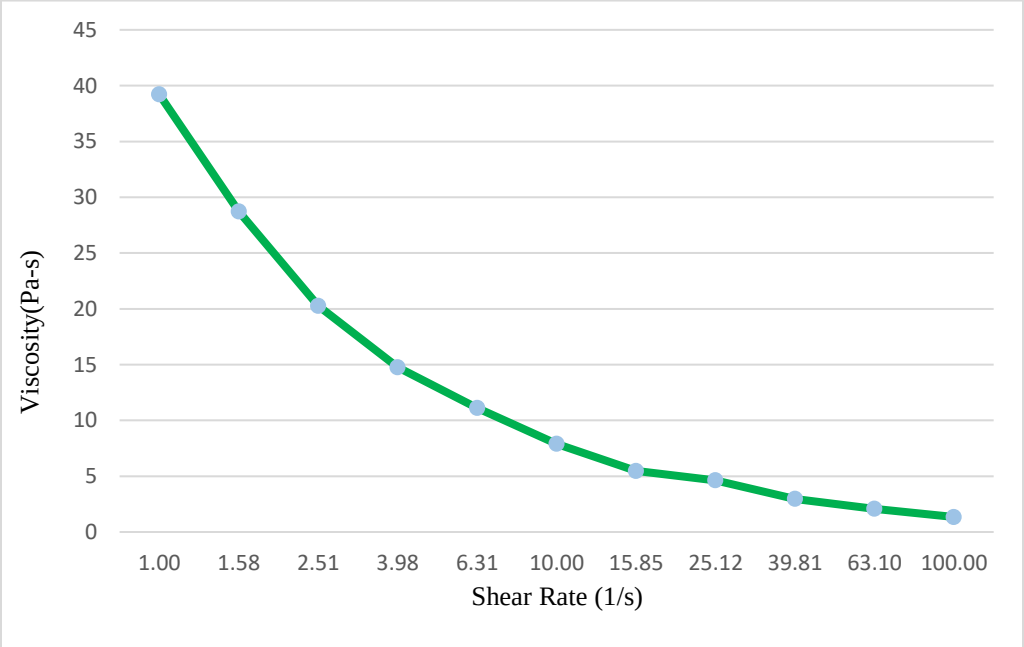

Fig. 77: Change of viscosity with respect to shear rate 90 µm.

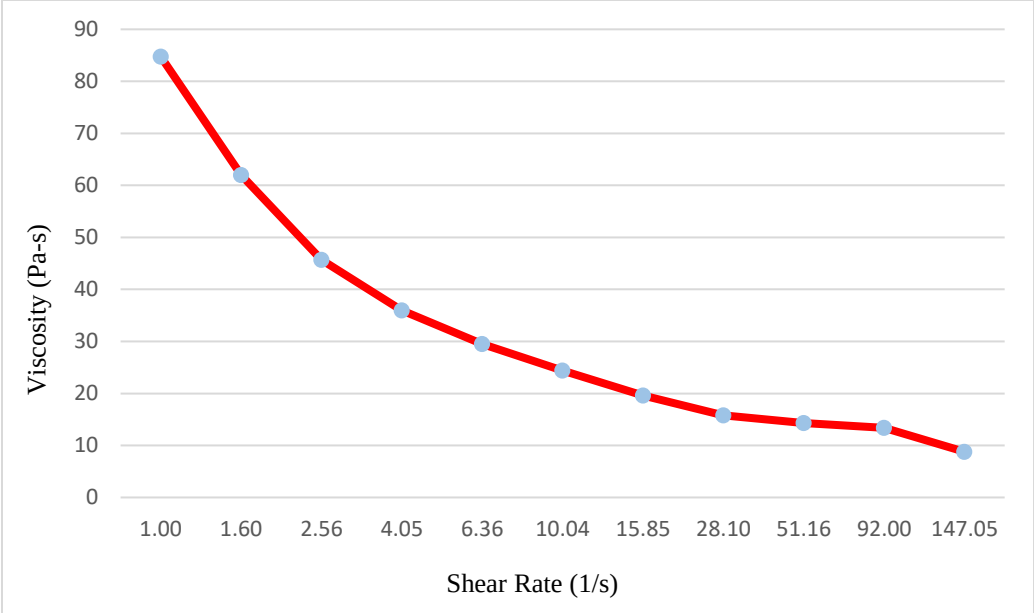

Fig. 78: Change of viscosity with respect to shear rate 70 µm.

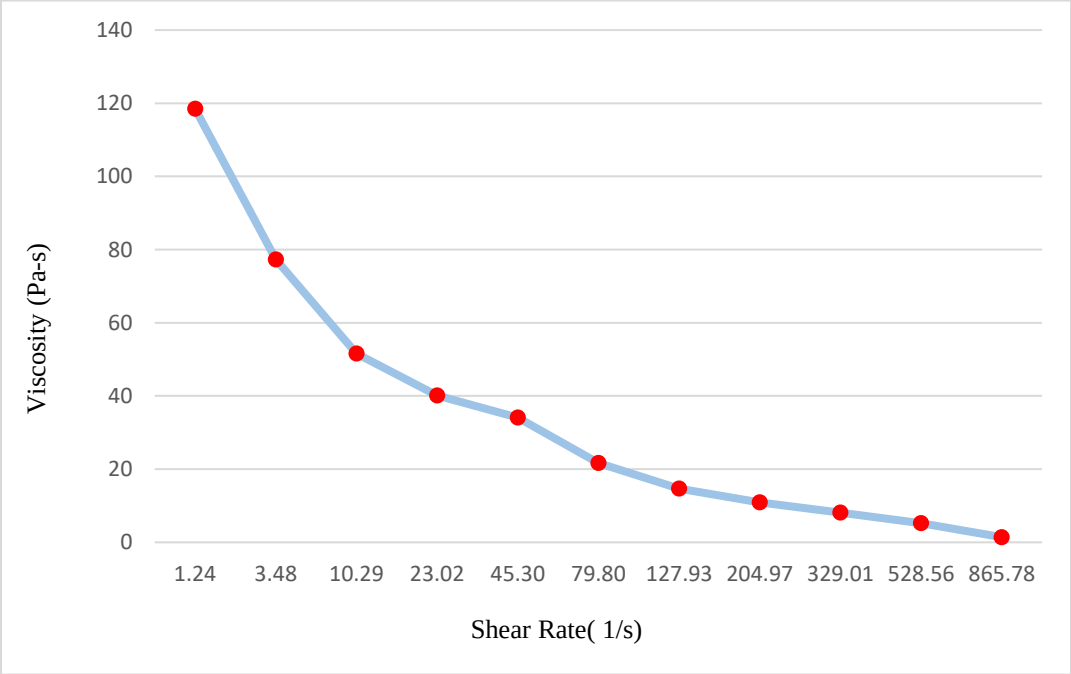

Fig. 79: Change of viscosity with respect to shear rate 50 µm.

At a lower gap thickness such as 50 μm the value of viscosity is too high almost 120 Pa-s but at higher gap thickness such as 110 μm the value of viscosity is low enough approximately 13 Pa-s. But in between at 90 μm gap thickness the value of viscosity is approximately 39 Pa-s. Which need to be carefully investigated when applying these cooling compound at electronic devices or any other applications.

2.3.4 Modulus vs Angular Frequency of TIM B

Following plots are showing the change of storage modulus and loss modulus with respect to with respect to angular frequency at room temperature for different gap thickness between the parallel plates of HR-2.

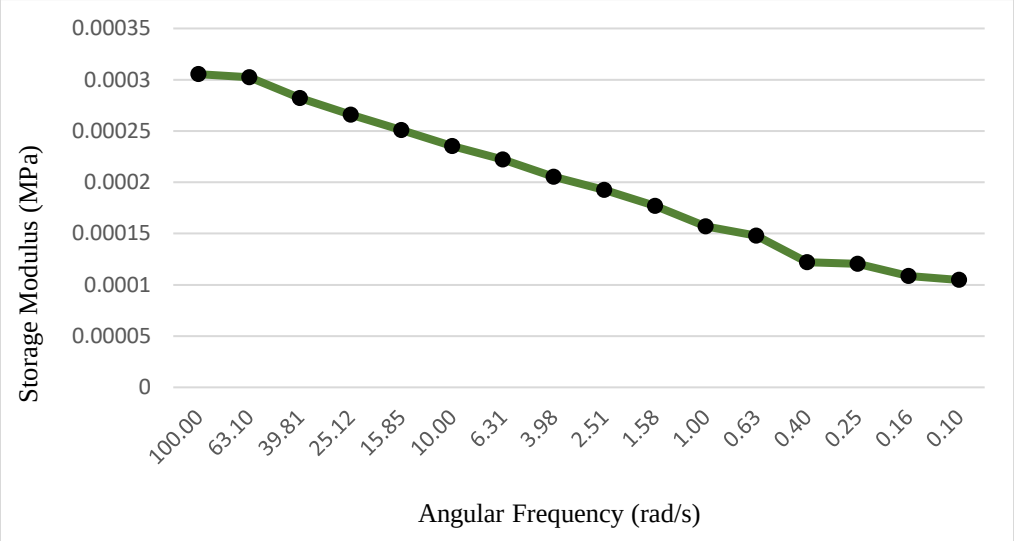

Fig. 80: Change of storage modulus with respect to angular frequency 110 μm.

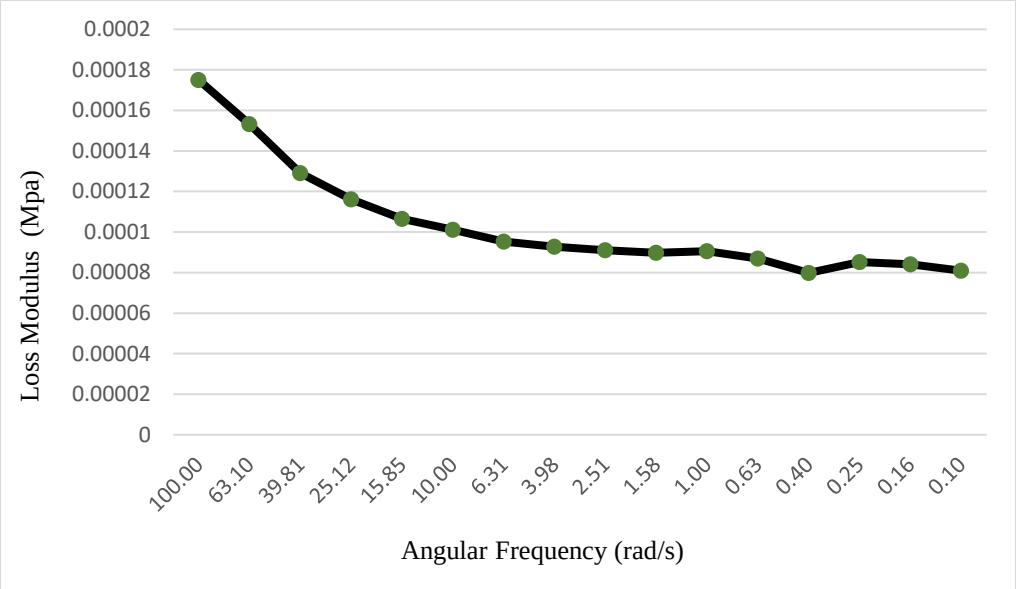

Fig. 81: Change of loss modulus with respect to angular frequency 110 µm.

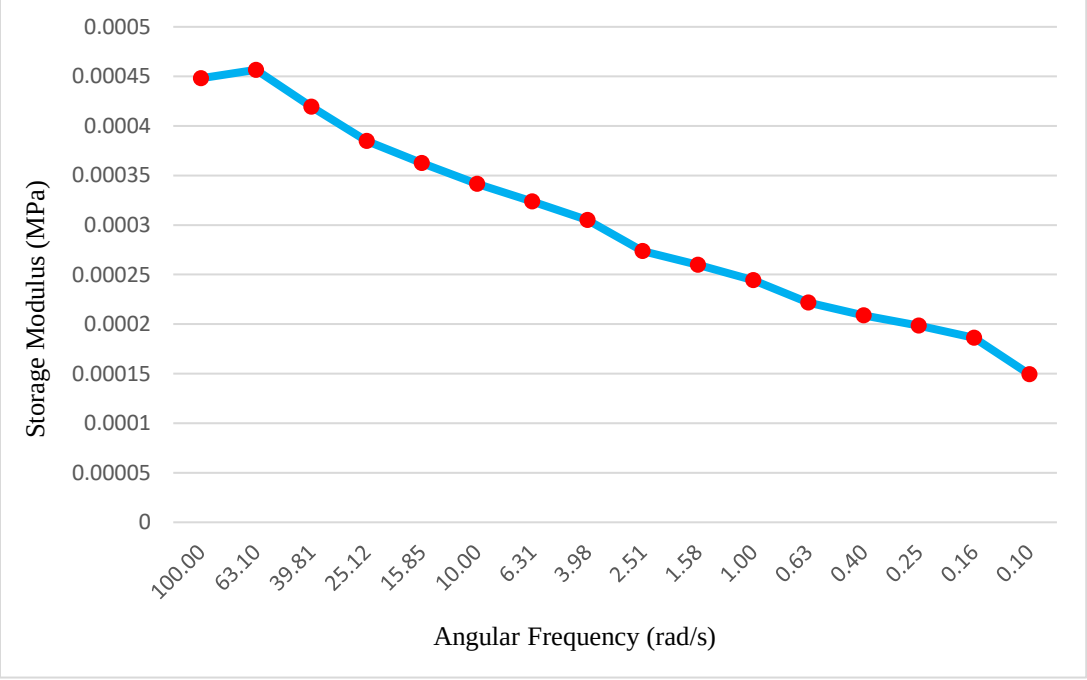

Fig. 82: Change of storage modulus with respect to angular frequency 90 µm.

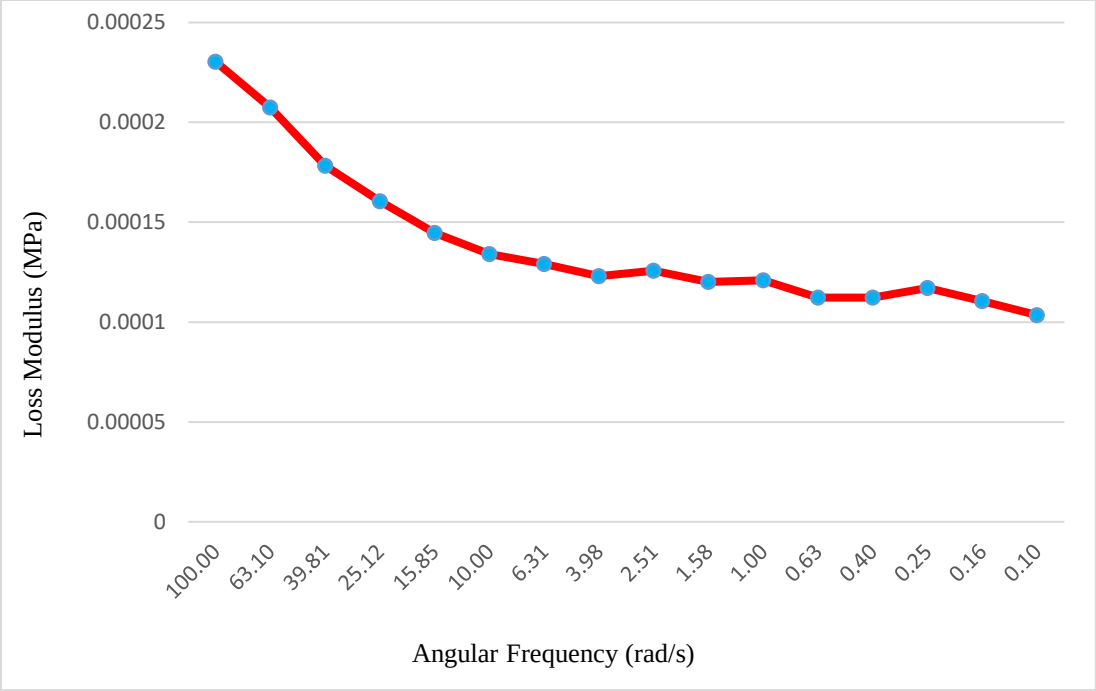

Fig. 83: Change of loss modulus with respect to angular frequency 90 µm.

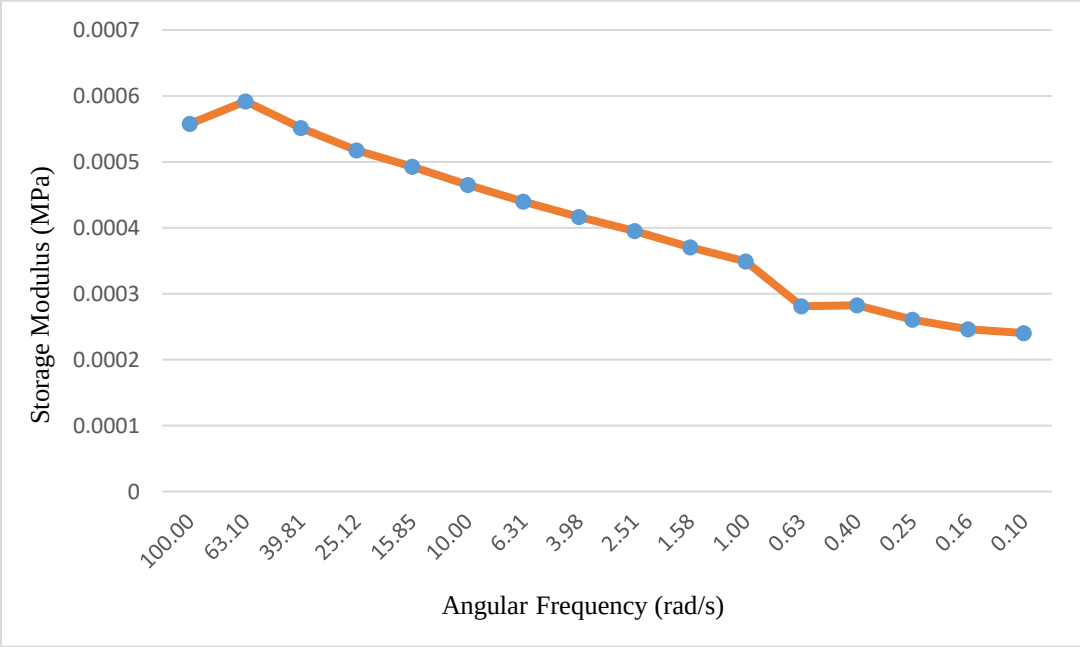

Fig. 84: Change of storage modulus with respect to angular frequency 70 µm.

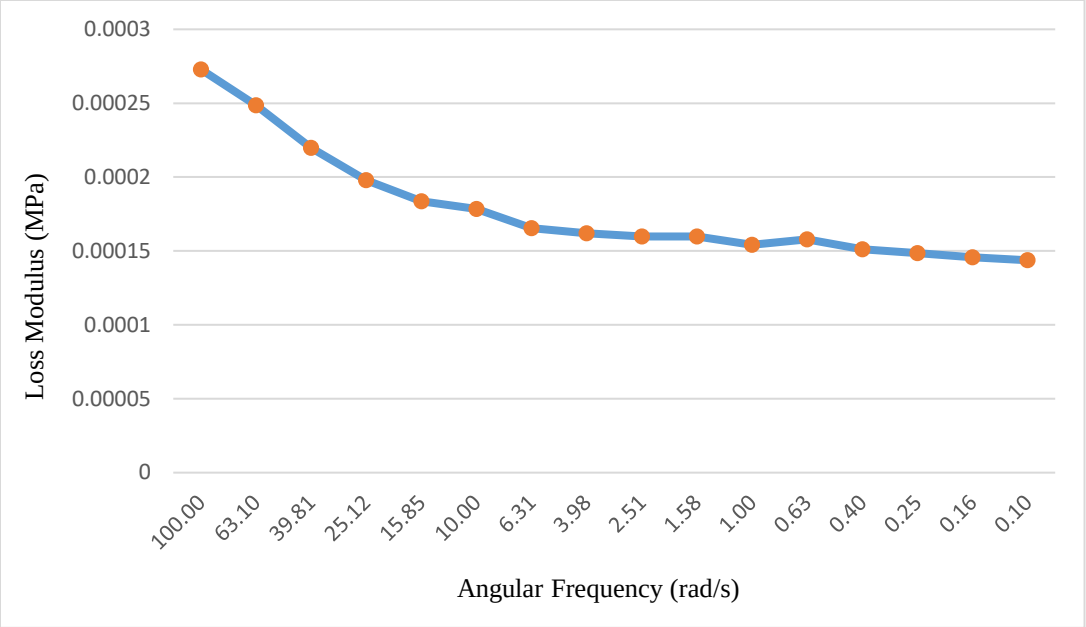

Fig. 85: Change of loss modulus with respect to angular frequency 70 µm.

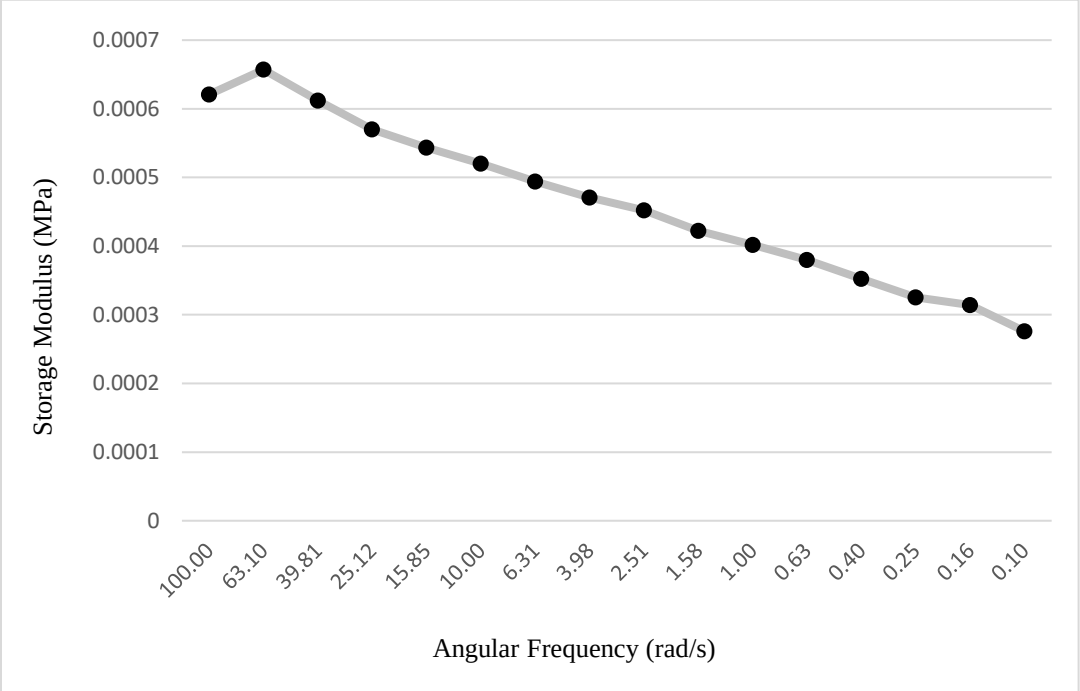

Fig. 86: Change of storage modulus with respect to angular frequency 50 µm.

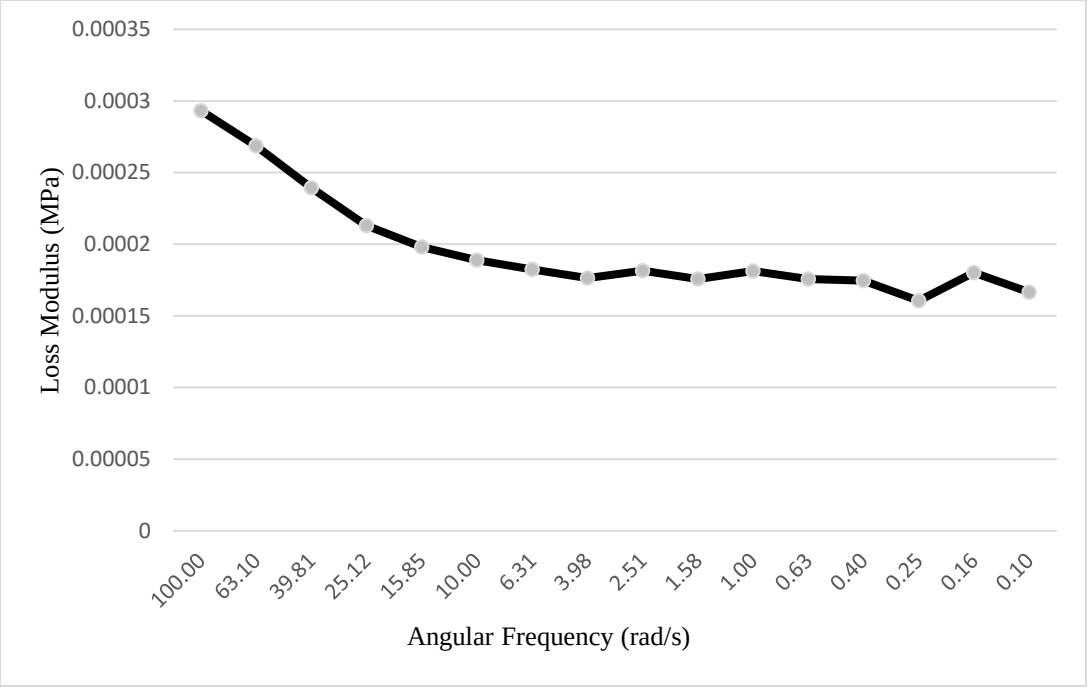

Fig. 87: Change of loss modulus with respect to angular frequency 50 μm.

From the above figures storage modulus and loss modulus of TIM A and TIM B is studied which give information about the microstructure of these cooling compounds. At a low frequency the value of loss modulus is almost constant and storage modulus is increasing gradually. With increasing frequency stimulation will increase the tension developed. When the frequency is high a larger force is applied to the intermolecular bonding of those materials which increase the value of stored energy and hence the value of storage modulus is high at higher frequencies. After a limit when the value of applied force become so high with increasing frequencies it collapse the intermolecular bonding of the material and it starts dissipating energy instead of storing at a higher rate so the value of loss modulus is also larger at a high value of frequencies. So, these thermal cooling compounds are good to apply in such applications where the values of frequencies are low to get better performances of these TIMs. For TIM A the values of storage modulus and loss modulus do not change much with different confinement between two parallel plates of the

rheometer but for TIM B the values of storage modulus and loss modulus increases with decreasing the gap thickness between two parallel plates of the rheometer.

2.4 Conclusion

In this analysis the change of rheological properties of two types of thermal interface materials TIM A and TIM B has been studied by Discovery Hybrid Rheometer (HR-2). For TIM A and TIM B change of viscosity with respect to shear rate and change of storage and loss modulus with respect to angular frequency has been analyzed for different confinement of the two parallel plates of HR-2. It is observed that the values of viscosities increased with increasing shear rate and decreasing the gap thickness between two parallel plates of the rheometer. It has been examined that the values of storage modulus and loss modulus increases with increasing angular frequencies and decreases by giving approximately constant values with decreasing angular frequencies. When the gap thickness between two parallel plates of HR-2 changes and decreases from 110 μm to 50 μm for TIM A the values of storage and loss modulus do not vary much but for TIM B the values of storage and loss modulus with respect to angular frequencies vary from a lower values to higher values with decreasing the gap thickness between the interfaces. Finally, it is observed that the rheological properties of these thermal cooling compounds depend shear rate, angular frequency, and confinement of the parallel plates of the rheometer and hence it can affect the BLT of the materials. As thermal resistance of these particle based polymeric thermal interface materials relies on BLT so changes in rheological properties has impact on the overall performance of these cooling compounds in any electrical devices. So, it is crucial to do the proper analysis of the rheological properties of TIMs to get optimum performances.

2.5 Future Work

Particle based thermal interface materials are one of the extensively used TIMs in semiconductor industries for microprocessors cooling solutions. As different types of volume fraction of micro or nano particles increase the thermal conductivity of such materials so it can be applied to different types of greases to see how it can impact the conductivity of the TIMs. Also, BLT thickness is another important factor need to consider when adding volume fraction of micro-nano particles to the thermal cooling compound to increase conductivity. So, using different TIM tester BLT of these thermal interface materials need to measure to make sure that it is not exceeding the limit and increasing resistivity rather than increasing conductivity of the TIMs. Rheological properties need to measure at a variety of conditions such as changing the temperature, frequency and strain amplitude at a higher and lower rate to see how it can impact the performance of these particle based thermal interface materials and hence enhance the thermal management of semiconductor devices.

References

[1] P. RAJMANE, “Chip Package Interaction Study To Analyze the Mechanical,” 2015.

[2] U. RAHANGDALE, “STRUCTURAL OPTIMIZATION & RELIABILITY OF 3D PACKAGE BY STUDYING CRACK BEHAVIOR ON TSV & BEOL & IMPACT OF POWER CYCLING ON RELIABILITY FLIP CHIP PACKAGEtle,” University of Texas at Arlington, 2017.

[3] M. S. ALI, “ESTIMATION OF FRACTURE MECHANICS PARAMETERS IN 3D TSV PACKAGE DURING CHIP ATTACHMENT PROCESStle,” University of Texas at Arlington.

[4] R. S. Prasher, J. Shipley, S. Prstic, P. Koning, and J. L. Wang, “Rheological study of micro particle laden polymeric thermal interface materials: Modeling (Part 2),” *ASME Int. Mech. Eng. Congr. Expo. Proc.*, vol. 7, pp. 53–59, 2002.

[5] J.-Y. B. Le Hoang Sinh, Jeong-Mi Hong, Bui Thanh Son, Nguyen Ngoc Trung, “Thermal, Dielectric, and Rheological Properties of Aluminum Nitride/Liquid Crystalline Copoly(ester amide) Composite for the Application of Thermal Interface Materials,” *Polym. Polym. Compos.*, pp. 2140–2146, 2012, doi: 10.1002/pc.

[6] J. H. Lau, “Evolution and outlook of TSV and 3D IC/Si integration,” *2010 12th Electron. Packag. Technol. Conf. EPTC 2010*, pp. 560–570, 2010, doi: 10.1109/EPTC.2010.5702702.

[7] M. Motoyoshi, “Through-Silicon Via (TSV),” vol. 97, no. 1, pp. 43–48, 2009.

[8] R. R. Tummala, “Introduction to Microsystems Packaging,” p. 923, 2001.

[9] M. M. Waldrop, “More than Moore,” *Nature*, vol. 530, p. 144+, Apr. 2016, [Online]. Available: https://link.gale.com/apps/doc/A443132364/HRCA?u=acd_galeaccess&sid=HRCA&xid=fbfe6543.

[10] Heterogeneous Integration Roadmap, “2019 HIR Chapter 22: Interconnects for 2D and 3D Architectures,” *Heterog. Integr. Roadmap*, 2019, [Online]. Available: http://eps.ieee.org/hir.

[11] H. H.-T. GLOBAL, “The semiconductor material silicon.” https://www.hitachi-hightech.com/global/products/device/semiconductor/silicon.html (accessed Jul. 03, 2021).

[12] A. Misrak *et al.*, “Impact of Die Attach Sample Preparation on Its Measured Mechanical Properties for MEMS Sensor Applications,” *J. Microelectron. Electron. Packag.*, vol. 18, no. 1, pp. 21–28, Apr. 2021, doi: 10.4071/imaps.1234982.

[13] SEMI, “HETEROGENEOUS INTEGRATION ROADMAP.” https://www.semi.org/en/communities/hir#:~:text=Heterogeneous Integration refers to the,functionality and improved operating characteristics. (accessed Oct. 03, 2021).

[14] SIEMENS, “TECH DESIGN FORUM.” https://www.techdesignforums.com/practice/technique/eight-requirements-3d-ic-design/ (accessed Oct. 02, 2020).

[15] S. S. Iyer, “Heterogeneous Integration for Performance and Scaling,” *IEEE Trans. Components, Packag. Manuf. Technol.*, vol. 6, no. 7, pp. 973–982, 2016, doi: 10.1109/TCPMT.2015.2511626.

[16] U. Rahangdale, P. Rajmane, A. Doiphode, A. Misrak, and D. Agonafer, “Structural Integrity Optimization of 3D TSV Package by Analyzing Crack Behavior at TSV and BEOL,” pp. 201–208, 2017.

[17] J. Van Olmen *et al.*, “3D stacked IC demonstration using a through silicon via first approach,” *IMAPS Int. Conf. Exhib. Device Packag. DPC 2012 - Conjunction with Glob. Bus. Counc. GBC 2012 Spring Conf.*, pp. 76–79, 2012.

[18] X. Zhang *et al.*, “Development of through silicon via (TSV) interposer technology for large die (21x21mm) fine-pitch Cu/low-k FCBGA package,” *Proc. - Electron. Components Technol. Conf.*, no. 25x25 mm, pp. 305–312, 2009, doi: 10.1109/ECTC.2009.5074032.

[19] F. P. Carson, Y. C. Kim, and I. S. Yoon, “3-D stacked package technology and trends,” *Proc. IEEE*, vol. 97, no. 1, pp. 31–42, 2009, doi: 10.1109/JPROC.2008.2007460.

[20] N. H. Khan, S. M. Alam, and S. Hassoun, “Power delivery design for 3-D ICs using different through-silicon via (TSV) technologies,” *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 19, no. 4, pp. 647–658, 2011, doi: 10.1109/TVLSI.2009.2038165.

[21] R. Rieske, R. Landgraf, and K. J. Wolter, “Novel method for crystal defect analysis of laser drilled TSVs,” *Proc. - Electron. Components Technol. Conf.*, pp. 1139–1146, 2009, doi: 10.1109/ECTC.2009.5074155.

[22] A. P. Karmarkar, X. Xu, and V. Moroz, “Performanace and reliability analysis of 3D-integration structures employing through silicon via (TSV),” *IEEE Int. Reliab. Phys. Symp. Proc.*, pp. 682–687, 2009, doi: 10.1109/IRPS.2009.5173329.

[23] X. Zhang, Y. Wang, J. H. Im, and P. S. Ho, “Chip-package interaction and reliability improvement by structure optimization for ultralow-κ interconnects in flip-chip packages,” *IEEE Trans. Device Mater. Reliab.*, vol. 12, no. 2, pp. 462–469, 2012, doi: 10.1109/TDMR.2012.2192122.

[24] P. Ramm *et al.*, “Through silicon via technology -processes and reliability for wafer-level 3D system integration,” *Proc. - Electron. Components Technol. Conf.*, pp. 841–846, 2008, doi: 10.1109/ECTC.2008.4550074.

[25] C. S. Selvanayagam, J. H. Lau, X. Zhang, S. K. W. Seah, K. Vaidyanathan, and T. C. Chai, “Nonlinear thermal stress/strain analyses of copper filled TSV (Through Silicon Via) and their flip-chip microbumps,” *IEEE Trans. Adv. Packag.*, vol. 32, no. 4, pp. 720–728, 2009, doi: 10.1109/TADVP.2009.2021661.

[26] M. Jung, J. Mitra, D. Z. Pan, and S. K. Lim, “TSV stress-aware full-chip mechanical reliability analysis and optimization for 3D IC,” *Commun. ACM*, vol. 57, no. 1, pp. 107–

115, 2014, doi: 10.1145/2494536.

[27] X. Liu, Q. Chen, P. Dixit, R. Chatterjee, R. R. Tummala, and S. K. Sitaraman, “Failure mechanisms and optimum design for electroplated copper through-silicon vias (TSV),” *Proc. - Electron. Components Technol. Conf.*, pp. 624–629, 2009, doi: 10.1109/ECTC.2009.5074078.

[28] F. Ahsan and L. Ladani, “Temperature Profile, Bead Geometry, and Elemental Evaporation in Laser Powder Bed Fusion Additive Manufacturing Process,” *Jom*, vol. 72, no. 1, pp. 429–439, 2020, doi: 10.1007/s11837-019-03872-3.

[29] S. Ramdas, P. Rajmane, T. Chauhan, A. Misrak, and D. Agonafer, “Impact of Immersion Cooling on Thermo-Mechanical Properties of PCB’s and Reliability of Electronic Packages.” Oct. 07, 2019, doi: 10.1115/IPACK2019-6568.

[30] X. Sun *et al.*, “Electrical characterization of sidewall insulation layer of TSV,” *Proc. - 2010 11th Int. Conf. Electron. Packag. Technol. High Density Packag. ICEPT-HDP 2010*, pp. 77–80, 2010, doi: 10.1109/ICEPT.2010.5582360.

[31] H. Ishii and J. Weertman, “Fatigue crack propagation in copper and Cu-Al single crystals,” *Metall. Mater. Trans. B*, vol. 2, no. 12, pp. 3441–3452, 1971, doi: 10.1007/BF02811626.

[32] M. Liu, Y. Gan, D. A. H. Hanaor, B. Liu, and C. Chen, “An improved semi-analytical solution for stress at round-tip notches,” *Eng. Fract. Mech.*, vol. 149, pp. 134–143, 2015, doi: 10.1016/j.engfracmech.2015.10.004.

[33] D. Ri *et al.*, “Damage Progression Study of 3D TSV Package during Reflow, Thermal Shocks and Thermal Cycling,” pp. 2–8.

[34] M. Chaudhari, A. S. M. R. R. Chowdhury, U. Rahangdale, A. Misrak, P. Rajmane, and U. States, “RELIABILITY ASSESSMENT OF BGA SOLDER JOINTS - MEGTRON 6 VS FR4 PRINTED CIRCUIT BOARDS,” in *SMTA International*, 2019, pp. 136–141.

[35] M. Kabir, A. S. M. R. Chowdhury, K. Shivaraju, and S. Dhandharphale, “ENHANCING THE RELIABILITY OF 3D PACKAGE BY ANALYZING CRACK BEHAVIOR ON TSV THROUGH STRUCTURAL OPTIMIZATION AND COMPARING MATERIAL PROPERTIES OF THE PACKAGE The University of Texas at Arlington,” 2020.

[36] T. Chauhan, A. Misrak, R. Bhandari, P. Rajmane, and R. Chowdhury, “IMPACT OF THERMAL AGING AND CYCLING ON RELIABILITY OF THERMAL INTERFACE MATERIALS The University of Texas at Arlington,” in *SMTA International*, 2019, pp. 118–123.

[37] U. Rahangdale *et al.*, “Effect of PCB thickness on solder joint reliability of Quad Flat no-lead assembly under Power Cycling and Thermal Cycling,” *Annu. IEEE Semicond. Therm. Meas. Manag. Symp.*, pp. 70–76, 2017, doi: 10.1109/SEMI-THERM.2017.7896911.

[38] Rahangdale, Unique *et al.*, “Solder Ball Reliability of WLCSP- Power Cycling Versus Thermal Cycling,” vol. 0.

[39] S. Dhandarphale, T. Chauhan, A. S. M. R. Chowdhury, D. Ph, D. Agonafer, and D. Ph, "IMPACT OF SINGLE-PHASE IMMERSION COOLING ON COEFFICIENT OF THERMAL EXPANSION OF PCBS AND IMPACT OF CHANGE IN THEMO-MECHANICAL PROPERTIES ON RELIABILITY OF SECOND LEVEL SOLDER JOINT OF BGA PACKAGE University of Texas at Arlington," in *SMTA International*, 2020, pp. 408–412.

[40] S. Ramdas, A. S. M. R. R. Chowdhury, A. Lakshminarayana, R. Bhandari, A. Misrak, and D. Agonafer, "Impact of Thermal Aging on Thermomechanical Properties of Oil-Immersed Printed Circuit Boards," *SMTA Int.*, pp. 772–778, 2019.

[41] F. MIRZA, "COMPACT MODELING METHODOLOGY DEVELOPMENT FOR THERMOMECHANICAL ASSESSMENT IN HIGH-END MOBILE APPLICATIONS – PLANAR AND 3D TSV PACKAGES," THE UNIVERSITY OF TEXAS AT ARLINGTON, 2014.

[42] A. S. M. R. R. Chowdhury, M. R. H. Sarker, N. Love, and A. Choudhuri, "Testing of a new drag relationship for non-spherical particle geometries using the two fluid model," *52nd Aerosp. Sci. Meet.*, no. January, pp. 1–10, 2014, doi: 10.2514/6.2014-1535.

[43] T. Sumigawa, S. Ashida, S. Tanaka, K. Sanada, and T. Kitamura, "Fracture toughness of silicon in nanometer-scale singular stress field," *Eng. Fract. Mech.*, vol. 150, pp. 161–167, 2015, doi: 10.1016/j.engfracmech.2015.05.054.

[44] V. Hatty, H. Kahn, and A. H. Heuer, "Fracture toughness, fracture strength, and stress corrosion cracking of silicon dioxide thin films," *J. Microelectromechanical Syst.*, vol. 17, no. 4, pp. 943–947, 2008, doi: 10.1109/JMEMS.2008.927069.

[45] M. J. Mian, J. Razmi, and L. Ladani, "Defect analysis and fatigue strength prediction of as-built Ti6Al4V parts, produced using electron beam melting (EBM) AM technology," *Materialia*, vol. 16, p. 101041, 2021, doi: https://doi.org/10.1016/j.mtla.2021.101041.

[46] H. Hirakata, O. Nishijima, N. Fukuhara, T. Kondo, A. Yonezu, and K. Minoshima, "Size effect on fracture toughness of freestanding copper nano-films," *Mater. Sci. Eng. A*, vol. 528, no. 28, pp. 8120–8127, 2011, doi: 10.1016/j.msea.2011.07.071.

[47] "Is copper wire elastic, plastic or brittle?," *Quora*. https://www.quora.com/Is-copper-wire-elastic-plastic-or-brittle (accessed Oct. 06, 2020).

[48] "Difference between linear and nonlinear elastic material," *Enterfea*. https://enterfea.com/difference-between-linear-and-nonlinear-elastic-material/#:~:text=Linear%2520elastic%2520%25E2%2580%2593%2520the%2520%25E2%2580%259Cnormal%25E2%2580%259D%2520way!&text=This%2520is%2520a%2520property%2520that.

[49] R. S. Prasher, S. Member, and J. C. C. Matayabas, "Polymeric Thermal Interface Material," *IEEE Trans. Components Packag. Technol.*, vol. 27, no. 4, pp. 702–709, 2004.

[50] Momentive, "Thermal Management." https://www.momentive.com/en-us/industries/electronics/thermal.

[51] F. Ahsan, J. Razmi, and L. Ladani, "Experimental measurement of thermal diffusivity,

conductivity and specific heat capacity of metallic powders at room and high temperatures," *Powder Technol.*, vol. 374, pp. 648–657, 2020, doi: 10.1016/j.powtec.2020.07.043.

[52] M. P. Hossain and K. Paul, "Thermal conductivity analysis of single-walled carbon nanotube using finite element modeling," *AIP Conf. Proc.*, vol. 1980, no. 1, p. 60007, Jul. 2018, doi: 10.1063/1.5044375.

[53] P. Shahi, S. Agarwal, S. Saini, A. Niazmand, P. Bansode, and D. Agonafer, "CFD Analysis on Liquid Cooled Cold Plate Using Copper Nanoparticles." Oct. 27, 2020, doi: 10.1115/IPACK2020-2592.

[54] M. R. H. Sarker, A. S. M. R. Chowdhury, and N. Love, "Prediction of gas-solid bed hydrodynamics using an improved drag correlation for nonspherical particles," *Proc. Inst. Mech. Eng. Part C J. Mech. Eng. Sci.*, vol. 231, no. 10, pp. 1826–1838, 2017, doi: 10.1177/0954406215622652.

[55] A. Niazmand, P. Murthy, S. Saini, P. Shahi, P. Bansode, and D. Agonafer, "Numerical Analysis of Oil Immersion Cooling of a Server Using Mineral Oil and Al2O3 Nanofluid." Oct. 27, 2020, doi: 10.1115/IPACK2020-2662.

[56] B. Munson, *Philip M. Gerhart Andrew L. Gerhart John I. Hochstein*. 2016.

[57] P. E. Rodrigues, "Shear modulus of heavy oils: Confinement effects in rheometer measurements," *Fuel*, vol. 153, pp. 520–525, 2015, doi: 10.1016/j.fuel.2015.03.031.

[58] M. R. H. Sarker, A. S. M. R. R. Chowdhury, N. Love, and A. Choudhuri, "Flow field visualization and drag analysis of particles in a gas-solid fluidized bed," *51st AIAA Aerosp. Sci. Meet. Incl. New Horizons Forum Aerosp. Expo. 2013*, no. January, pp. 1–11, 2013, doi: 10.2514/6.2013-597.

[59] A. Lakshminarayana, A. Misrak, R. Bhandari, T. Chauhan, A. S. M. Raufur Chowdhury, and D. Agonafer, "Impact of Viscoelastic Properties of Low Loss Printed Circuit Boards (PCBs) on Reliability of WCSP Packages under Drop Test," *Proc. - Electron. Components Technol. Conf.*, vol. 2020-June, pp. 2266–2271, 2020, doi: 10.1109/ECTC32862.2020.00353.

[60] V. Subramanian *et al.*, "Mechanical Characterization of Thermal Interface Materials and Its Challenges," *J. Electron. Packag. Trans. ASME*, vol. 141, no. 1, 2019, doi: 10.1115/1.4042805.

[61] W. Sukhlaaied, S. A. Riyajan, and G. R. Palmese, "Dynamic viscosity of maleate poly(vinyl alcohol) and its copolymer measured by rheometer," *Polym. Test.*, vol. 56, pp. 387–393, 2016, doi: 10.1016/j.polymertesting.2016.10.008.

[62] A. Misrak, T. Chauhan, P. Rajmane, R. Bhandari, and D. Agonafer, "Impact of Aging on Mechanical Properties of Thermally Conductive Gap Fillers," *J. Electron. Packag.*, vol. 142, no. 1, pp. 1–9, 2020, doi: 10.1115/1.4045157.

[63] TA Instrument, "Discovery Hybrid Rheometer."

Biography

Mehzabeen Binte Kabir received her Bachelor of Science degree in Physics from University of Dhaka, Bangladesh, in the year 2016. She pursued her Master of Science degree in Mechanical Engineering from University of Texas at Arlington in Fall 2019. During her graduate program at UT Arlington she worked as a graduate teaching assistant in Mechanical Engineering department and conducted her research in Electronics, MEMS & Nanoelectronics Systems Packaging Center (EMNSPC) with Prof. Dereje Agonafer. She is a motivated, dynamic engineer who is fascinated by the extensive research area of next generation packaging and fabrication technology of electronic devices. Her expertise relies on structural optimization and reliability assessment of electronic devices and characterization of different packaging materials which impact the overall performance of various electronic system. She was an integral part of the project where characterization of different packaging materials was performed in collaboration with a company named TDK Invensense. She worked as an executive officer at Surface Mount Technology Association (SMTA) UTA chapter and as a treasurer at International Microelectronics Assembly and Packaging Society (iMAPS) UTA chapter. Mehzabeen is author and co-author of several notable conference and journal papers. After graduation, Mehzabeen plans to pursue her career in the semiconductor industries to apply her knowledge for the development of advanced and reliable electronic devices with honesty and hard work.