Study of Effect of Energy Filtering on Subthreshold Slope of Transistors

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ABSTRACT

STUDY OF EFFECT OF ENERGY FILTERING ON SUBTHRESHOLD SLOPE OF TRANSISTORS

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The inability to scale down the supply voltage of transistors has been a limiting factor that leads to excessive power consumption. The supply voltage is forced to remain at a high value (>0.5 V) due to the subthreshold slope limit of 60 mV/decade at room temperature for MOSFET devices. This high subthreshold slope value is caused by the thermal excitation of electrons following the Fermi-Dirac distribution and is a limiting factor in the functionality of various modern electronic devices. This study investigated a new type of transistor in which the thermally excited electrons are filtered out by a quantum well state, suppressing the thermal excitation of electrons and thereby increasing the steepness of the subthreshold slope. Silicon-based transistors capable of filtering out thermally excited electrons have been fabricated. A 2 nm QW layer of Cr_2O_3 and 1-2 nm SiO2 tunnelling barrier were inserted between the source electrode and the Si channel, where thermally excited electrons in the source are filtered out by a discrete state of the Cr_2O_3 QW and tunnel to the Si channel. The I-V's and subthreshold slopes of fabricated devices with and without the energy filter were compared. A steeper subthreshold slope was observed for the transistor with the energy filter. A steeper subthreshold slope was also observed for devices with decreasing gate length.

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Chapter 1 – Introduction

One of the most important components present in modern electronic systems is the transistor. As such, there is an increasing demand for improving the performance of the transistors. In the last few decades, there has been exponential improvement in the efficiency of transistors while reducing their sizes[1]. At this stage, however, we have reached a bottleneck and further improvement in the power consumption efficiency and reduction of size for the transistors has hit a limit. This is due to the inability to further reduce the supply voltage with the scaling of the transistor devices[2, 3]. This limitation is because of the thermal excitation of electrons at room temperature following Fermi-Dirac distribution[4, 5] leading to a gradual subthreshold slope which forces the supply voltage to a high value (> 0.5V).

At room temperature, the electrons in solids can be thermally excited to high energy states following Fermi-Dirac electron distribution. This phenomenon supresses various technologically significant phenomenon such as coulomb blockade[6-13], etc. This thermal excitation of electrons is also responsible for the excessive power dissipation in transistors. A transistor is basically an on-off switch. It has three core components – a source electrode, a drain electrode, and a gate electrode. Electron transfer occurs between the source and drain electrodes. This electron transfer is controlled by the gate electrode. The conduction band of the silicon channel connecting the source and drain acts as an energy barrier between the two electrodes. Now, when there is no bias applied to the gate and there is a potential difference between the source and drain electrodes, the energy barrier should be sufficient to prevent the flow of electrons from the source to the drain electrode. However, at room temperature, due to the thermal excitation of electrons from the source electrode, some of these electrons have sufficient energy to jump over the silicon conduction band energy barrier and reach the drain

electrode which gives us a source-drain current. This source-drain current in the transistor off-state (zero gate bias) is undesirable and causes an unwanted off-state power dissipation.

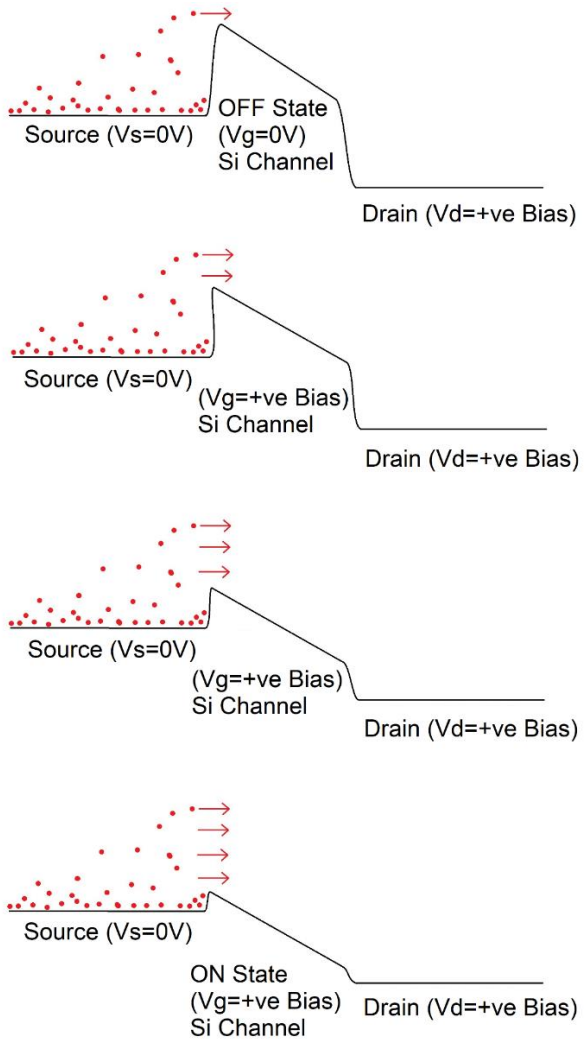

Figure 1: *Energy diagram of a simple MOSFET device*

When a positive gate bias is applied to the gate electrode, the conduction band of the silicon channel is reduced to a lower energy level. This lowers the energy barrier between the source and drain electrode fermi levels. As this energy barrier is lowered, the thermally excited electrons from the source electrodes are still able to jump over the lowered energy barrier and generate a source-drain current. This results in a gradual increase in the source drain current

when a positive bias is applied to the gate electrode. This gradual increase in the source-drain current leads to a gradual subthreshold slope. At room temperature, the subthreshold slope limit for a MOSFET is 60 mV/dec at 300 K (Figure 2 (Left)) and is considered as a fundamental limit[14-17]. A high supply voltage during on-state of transistor leads to a high on-state power consumption. Lowering the supply voltage will cause a shift in the IV curve towards the left (Figure 2 (Right)) as the subthreshold slope is limited to 60 mV/dec and the ON-state current is fixed resulting in an increase in the off-state current and thereby the OFF-state power consumption. Therefore, the gradual subthreshold slope pushes the supply voltage, V_{dd} to a higher value which results in a high ON-state power consumption. Thus, we need to find a way to lower the supply voltage without increasing the OFF-state current. The fundamental limit for the subthreshold swing can be reduced to go lower than 60 mV/dec if we are able to suppress the thermal excitation of electrons. That is, if the subthreshold slope becomes steeper, we can have a ON-state current at a lower V_{dd} without increasing the OFF-state current. This will reduce the power consumption of the transistor device several fold. Lowering the subthreshold slope has been the focus of many recent research efforts to reduce the power consumption of transistor devices[17-31]. Multiple approaches such as the use of nano or micro-electromechanical forces[32-39] have been suggested to achieve low power consumption devices. These devices utilize mechanically controlled components which limits their utilization in high speed functionalities. Other approaches to reduce the subthreshold swing include impact-ionization transistor[40-43], high-k gate dielectrics[44, 45], ferroelectric high-k gate dielectric[46-51] MOSFET device and band to band tunnelling in Tunnel Field effect transistors[29, 32, 52-59]. Various device architecture and different material systems using graphene based vertical architecture transistors in combination with MoS_2, hBN, WSe_2 heterostructures[60-64], etc. and low power vertical TFETs[52], heterojunction tunnelling transistors[65], vertical InAs-GaSb nanowire TFETs[66, 67] and other III-V nanowire/Si

heterojunction TFETs[68-72] for steep subthreshold slope operation, etc. have also been investigated. Combinations of above approaches with organic transistors[73-75] have also been studied.

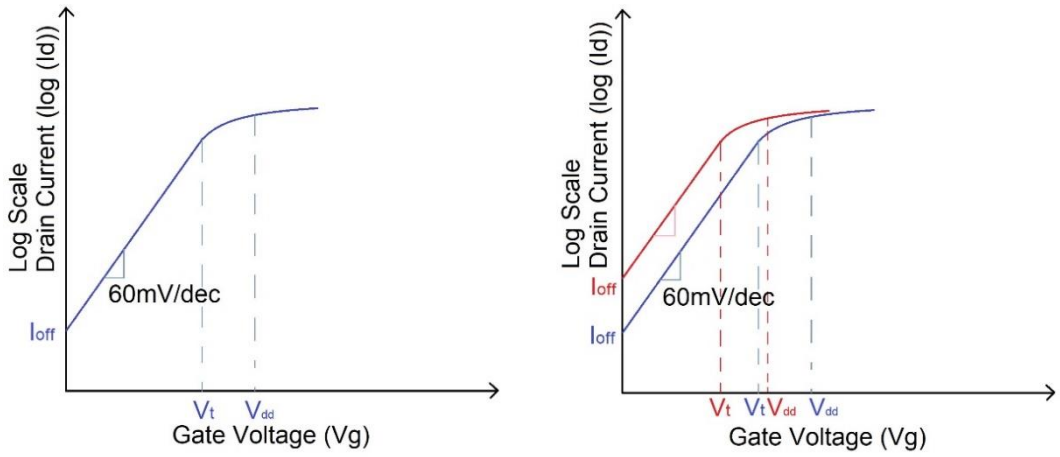

Figure 2: Subthreshold swing showing (Blue) fundamental limit at 300 K. The red IV shows the effect of reducing the Vdd causes the IV to shift to the left which increases the unwanted Off state current

Earlier efforts to suppress thermally excited electrons were successful but required the entire system to be cooled to cryogenic temperatures[76-79]. Schottky transistors have been extensively utilized to aid in the scaling of transistor devices. Schottky barrier transistors have been researched extensively[80-86] to obtain low power consumption in transistor devices. In other research, a weaker than regular dependence of subthreshold slope on temperature has been demonstrated using a dual-independent gate silicon FinFET[87].

The focus of this research is to reduce transistor power consumption by increasing the steepness of the subthreshold slope. In order to achieve that, it is important to understand the factors influencing the subthreshold slope. Subthreshold slope value depends on the temperature[30, 88] at which the transistor is operating and the gate capacitance which can be controlled by the device architecture. Higher temperature will lead to a larger number of electrons tunnelling through the silicon conduction band which will in turn lead to a gradual increase in the source-

drain current resulting in a gradual subthreshold slope. Tunnelling of electrons from source through the Si channel to the drain electrode although enhances the source drain current, it causes a degradation in the subthreshold slope[89, 90].

Chapter 2 – Energy Filtering for Electron Thermal Suppression

Previously our group demonstrated successful suppression of electron thermal excitation at room temperature without external cooling[91, 92]. Electron temperature was lowered by utilizing discrete quantum state as energy filter[93-95] for electrons tunnelling from the source electrode. They fabricated a double barrier tunnelling junction device in order to achieve this effect. The device architecture consists of source and drain electrode connected using a quantum dot placed accurately between the two conductors and separated from each electrode using thin 2 nm tunnelling barriers and 2 nm Cr_2O_3 films. The 2 nm Cr_2O_3 film forms a quantum well and serves as an energy filter.

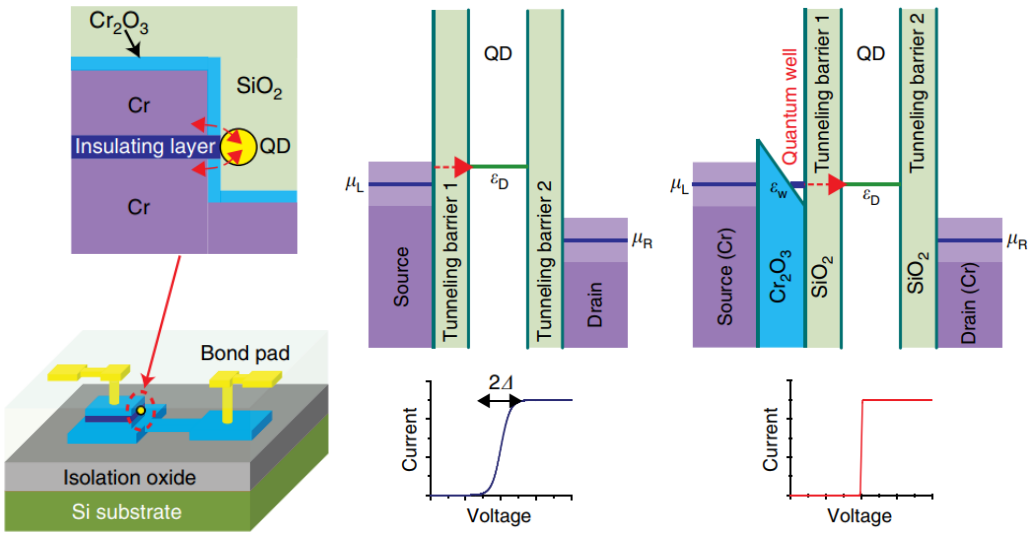

Figure 3: DBTJ device structure and energy band structure[91]

The principle at work here is as follows. For a conventional MOSFET device, at room temperature, the electrons in the source electrode get excited to above the fermi level. These high energy electrons are then able to tunnel through the tunnelling barrier and jump onto the quantised energy level of the quantum dot and are transported to the drain electrode. But, when we insert a quantum well layer between the quantum dot and the source electrode, quantum well structure is tuned such that the discrete energy levels of the quantum well are separated

by a large energy gap. In this case, there is only one energy level close to the fermi level of the source electrode. When the thermally excited electrons jump over the energy barrier and enter the quantum well structure, the electrons are forced to occupy the closest discrete energy level. As there is no excitation path available for the electrons in the quantum well, these confined electrons should be effectively cooled to 0K.

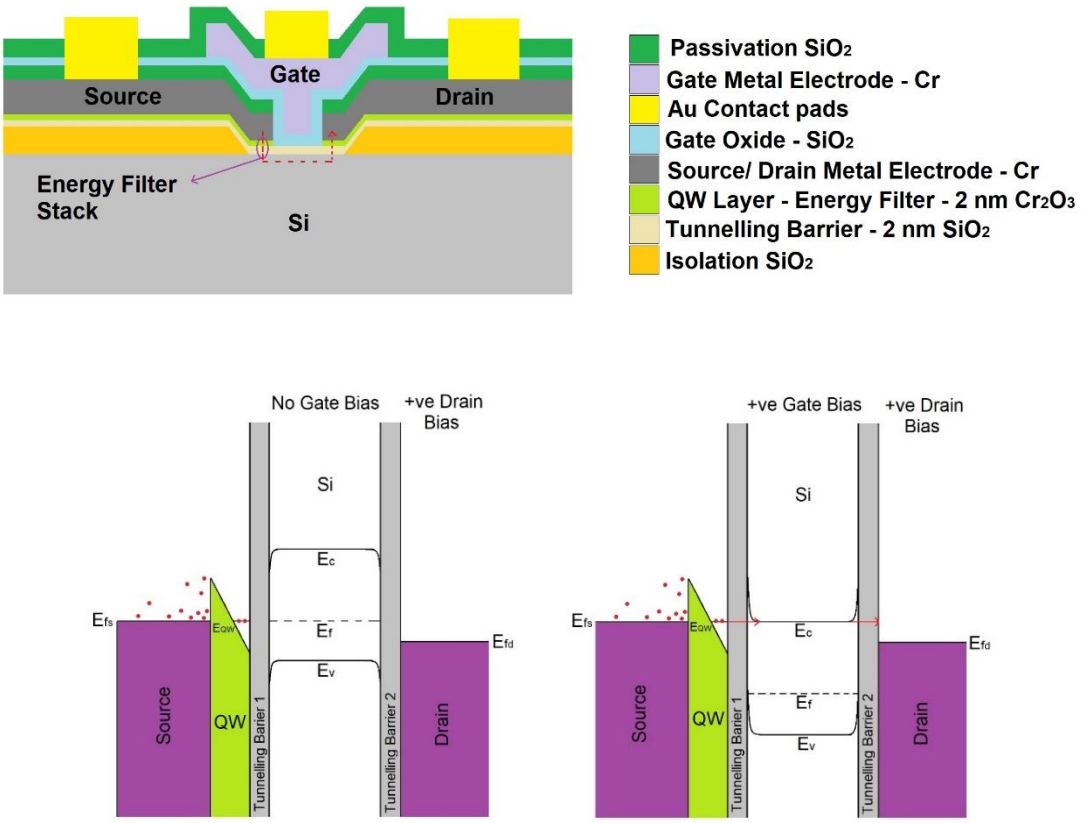

Figure 4: CET device schematic (top). Energy band diagram showing the principle of CET

This research establishes and optimizes a fabrication procedure for cold-electron transistors – transistors with energy filter architecture. It also studies the effect of energy filtering on subthreshold swing.

Chapter 3 – Fabrication of Cold electron Transistors

3.1 Introduction

This chapter provides the fabrication procedure for the Cold electron Transistors using fabrication techniques suitable for large scale fabrication. This chapter also discusses in detail the problems occurred during the fabrication process and the steps taken to resolve the said problems relating to the gate oxide and passivation films, wet etching processes and reactive ion etching processes. Our devices were fabricated on a 4-inch p-type silicon wafer. The wafer is subject to several processes like Doping, Thermal Oxidation, E-beam Evaporation, Plasma-Enhanced Chemical Vapor Deposition, Photolithography, Reactive Ion Etching and Wet Etching and so on before the devices are completed and were ready for IV Characterization. The entire process was carried out in a class-100 cleanroom facility in the Nanofab Research Facility at the University of Texas at Arlington.

The entire process is detailed in this chapter.

3.2 Photomask for Cold Electron Transistor device

For the fabrication of Cold electron transistor devices standard photolithography technique is used. We used a photolithography mask designed by Professor Seong Jin Koh. The photomask consists of four separate layers for each feature in the device like the Si-electrode contact island, Source and Drain electrodes, Gate electrode and Bond Pads. Our initial mask design contained all four mask layers on a single mask. The first mask layer is the island for contact between the Si and the Source and Drain electrodes. It is used to separate the Source and Drain electrodes and to create a contact region between the source and drain electrodes and the Si beneath the Silicon Dioxide film. The island width is also used to set the gate length. The second mask is the Source and Drain Electrode pads connected by a thin strip. We align the Second mask such that the thin strip connecting the Source and Drain pads crosses the island thus separating the

two pads. The third mask is the Gate electrode which is used to deposit the Gate isolation oxide followed by the gate electrode. The fourth mask is for the contact bond pads on the Gate, Source and Drain electrodes to measure the IV characteristics. The entire process initially took one month to fabricate.

Our new mask design, on the other hand helped us to reduce the fabrication time to one week. For the new design, the first mask island is used to create contact between the Si Substrate and the Source and Drain electrodes. The second mask consists of the Source and Drain electrode pads. The narrow strip extending from the pads towards each other is not connected. The gap between them determines the gate length. The third mask is the Gate electrode and the fourth mask is for the contact bond pads on all three electrodes.

3.3 Initial Fabrication Process

In this section, we shall detail the initial fabrication procedure we used for fabricating the Cold Electron Transistors. Test grade p-type silicon (100) wafers are used as substrate for Cold Electron Transistors Device fabrication. Before proceeding with the processing, the wafers are cleaned using Piranha solution. The wafers are immersed in a 3:1 Piranha solution of H_2SO_4:H_2O_2 for 30 minutes to remove any organic impurities accumulated on the wafers. The wafers are taken out of the piranha solution and immersed in DI water container for 5 minutes, rinsed under running DI water and then immersed in a fresh DI water container for another 5 minutes. This thorough DI water rinsing process is needed to completely remove any remaining Piranha solution on the wafer surface. When silicon wafers are stored in contact with air containing oxygen, it develops a thin layer of silicon dioxide on the top surface.

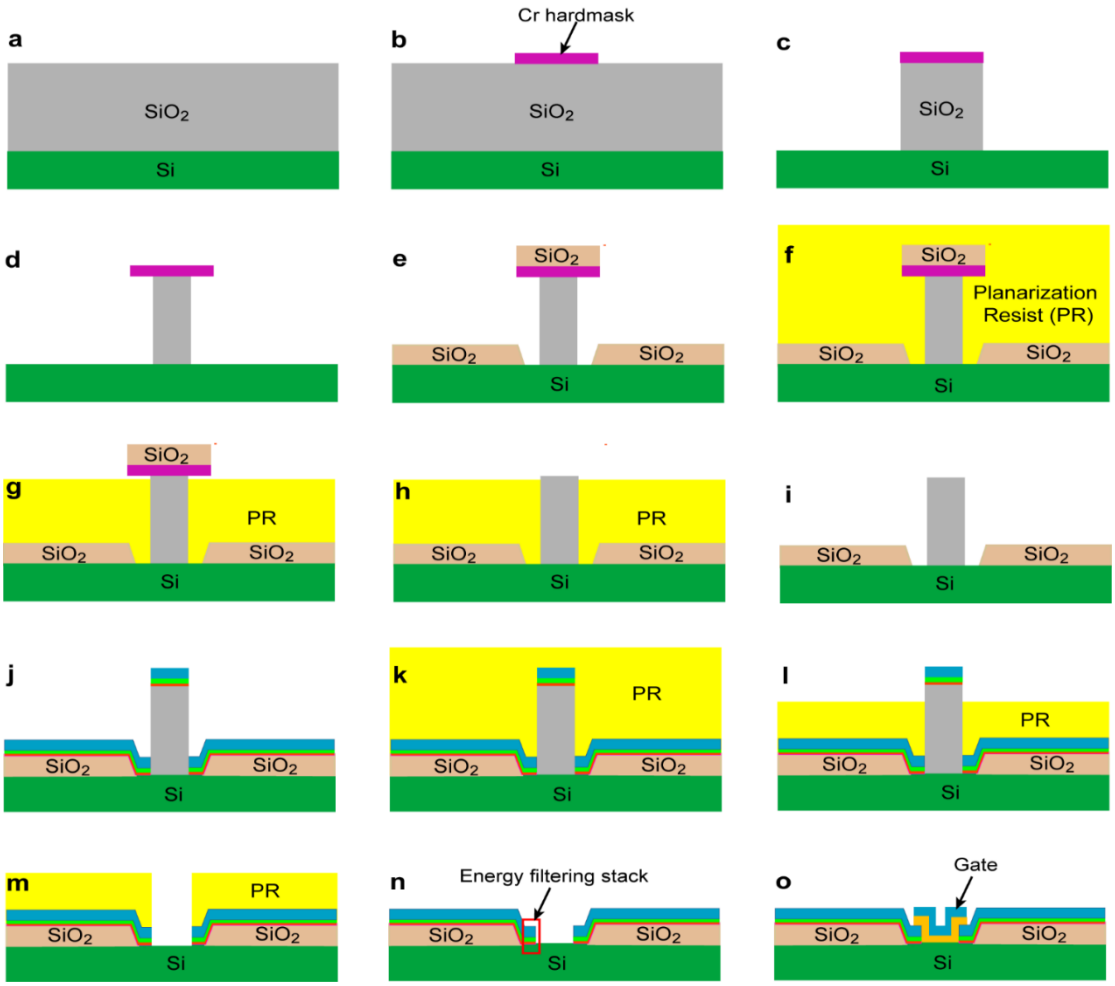

Figure 5: Process flow for large scale fabrication of CET devices (Initial method)

This oxide is called a native oxide. The thickness of the native oxide when allowed to grow naturally for 2 days is usually a few nanometres. In order to further process our wafers, we need to get rid of this native oxide formation. Thus, the next step of cleaning our wafers after subjecting them to Piranha cleaning is an HF (10:1) etching process. The wafers are then immersed into a 10:1 Hydrofluoric acid in a plastic container for 5 minutes to etch any native silicon dioxide grown on the wafers. The etch rate calculated for thermal oxide is 0.32 nm/s. The above mentioned 5 minutes of HF (10:1) etching should be able to etch away 96 nm of silicon dioxide. The wafer is then taken out and a DI water rinsing process is carried out, i.e. Wafer is immersed in DI water container for 5 minutes, followed by rinsing under running DI

Water and immersing in a fresh DI water container for 5 more minutes. Once the cleaning process is done, we can move on to start with the first step in the fabrication process.

3.3.1 Silicon Dioxide Deposition for First Mask island formation

A thick Silicon dioxide film is needed in order to form a pillar structure required in the subsequent steps. For this purpose, we deposit a silicon dioxide thickness of 450 nm. The quality of the silicon dioxide deposited determines the etch rate we get during the HF (10:1) etch back step. As this initial thick silicon dioxide is used as a sacrificial oxide film which we will be etching away using HF (10:1) after first mask alignment step, we can use e-beam evaporation to deposit the silicon dioxide which gives us a slightly lower quality oxide than thermal oxidation process. The deposition is done using CHA E-beam Evaporator. The chamber conditions are as follows:

Chamber Pressure: 4×10^{-7} Torr

Deposition Current: 4.7 mA

Deposition Temperature: Room Temperature

Deposition Rate: 1.5 A/s

Thickness Monitor Reading: 4500 A

The wafer is fixed on a sample holder using clamps on the edges. The CHA e-beam evaporator sample holder can hold 1 wafer at a time to ensure uniform deposition. The sample holder is inserted into sample holder slot in the CHA e-beam evaporator main chamber. We need to insert a graphite crucible filled up to two-thirds of the crucible with silicon dioxide pellets into the target slot in the CHA e-beam evaporator. Once the target and the sample holder are inserted inside the main deposition chamber, the chamber hood is lowered. The chamber is then pumped to a pressure of 100 mTorr with a rough pump followed by a turbo pump to achieve a high

vacuum of 5 x 10^{-6} mTorr. The deposition parameters need to be programmed into the thickness monitor. The thickness monitor shows the current deposition rate of the material and the actual thickness deposited in real time by measuring the deposited film on the thickness monitor crystal. The readings will be accurate as long as the crystal life is above 75 percent. The parameters programmed into the thickness monitor include the film number, the deposition rate, density, and the acoustic impedance of the film to be deposited. These parameters are needed to determine the deposited thickness in real time on the crystal. The film number determines which target slot will be targeted with the electron beam for evaporation. Once the chamber pressure reaches the required value, the source shutter is opened, and we start to increase the e-beam current very gradually while regularly monitoring the target through a window in the main chamber wall. When we are able to see a faint illumination incident on the silicon dioxide pellets in the crucible, we can adjust the location and frequency of the e-beam incident on the target using the control knobs situated on the e-beam control panel. Once we centre the e-beam on the target and make sure that the e-beam does not hit any adjacent crucible walls, we can then begin to increase the e-beam current gradually till we obtain a deposition rate of 1.5 A/s. At this stage the silicon dioxide pellets glow a brilliant white color. We then wait for a few seconds for the deposition rate to stabilize. Once the e-beam is stabilized, we can then open the substrate shutter. This starts the deposition process. The thickness monitor needs to be set to zero the moment the substrate shutter is opened. We need to keep monitoring the deposition rate and adjust the e-beam current if we see any fluctuations in the deposition rate. Once the thickness monitor reading shows a thickness of 4500 A, we close the source and substrate shutter immediately. We then gradually ramp down the e-beam current back to zero. The target crucible is allowed to cool down to room temperature. The main deposition chamber is then purged with nitrogen until the chamber pressure reaches atmosphere pressure. The chamber hood is lifted, and the sample holder and the target crucible are taken out after

allowing it to cool down to room temperature. The thickness deposited on the wafer is measured using Ellipsometer and Reflectometer (Ocean Optics). If the deposited thickness is close to the thickness monitor reading, we can then proceed to the next step in the fabrication process.

3.3.2 First Mask Lithography to Pattern Silicon Island Region

After sacrificial silicon dioxide layer is deposited, the next step is to pattern the samples with the First Mask pattern in order to create an island structure on the sample. This island structure is needed to form a contact region between the source and drain metal electrodes and the silicon semiconductor channel. It also helps in the formation of a gap region between source and drain electrodes, which determines the gate length for each device.

The first mask pattern for each sample is divided into four identical regions which we will name Regions A through D. Each region is an array of 5 rows and 7 columns. Each of the 5 rows are also identical. The columns are arranged in an order of increasing island width from a to d, and e to g.

Before proceeding with the first mask alignment we need to cut the wafer into 3 samples with dimensions of roughly 1 inch by 1 inch. The wafer is cut using a diamond cutter to mark the boundary and snapping either sides of the scratch mark using Teflon tweezers. This will ensure that all four regions of the first mask pattern along with the alignment marks are printed well inside the margins of the sample dimensions. These samples will be named henceforth as Sample A, Sample B and Sample C.

Each of these samples is first spin coated with a negative tone resist – NR9-1000PY. The spin coating parameters are as follows:

Step 1: 500 rpm; 100 rpm/s; 5 seconds

Step 2: 3000 rpm; 1000 rpm/s; 60 seconds

Step 3: 0 rpm; 1000 rpm/s; 0.1 seconds

After spin coating is done, the samples are pre heated at 150°C for 1 minute on a hot plate. The samples are loaded one by one on to a OAI aligner for first mask alignment and exposure. The exposure parameters are as follows:

Mask mode: Vacuum Contact Mode

Pressure setting current: 14 mA

Measured Beam Intensity: 17.7 mW/cm^2

Exposure Time: 6.8 seconds

Dose: 120 mJ/cm^2

After exposure the samples are post baked on a hot plate at 100°C for 1 minute. The samples are allowed to cool down and the developed in a negative resist developer – RD6 for 10 seconds, followed immediately by rinsing in a DI water container for 5 minutes with regular stirring, transferred to a second DI water container for 5 minutes with regular stirring. The samples are taken out and slowly blow dried with nitrogen.

All three samples are then observed under optical microscope to confirm that all alignment marks are printed perfectly and that the island patterns are present as well. The island with the smallest width is not clearly printed due to the dimensions of the pattern on the chromium mask and the limitations of the photolithography tool and human error. Thus, the islands printed are from columns b, c, d, e, f and g for all 5 rows and all 4 regions.

3.3.2 Hard Mask Deposition for protection against etching

After confirmation, we move on to hard mask deposition to protect against Reactive Ion Etching and wet etching using HF (10:1). Initially, we deposited a 100nm layer of Chromium as a hard mask. This mask protected the silicon dioxide beneath it from RIE process, but the

wet etch step using HF (10:1) created pitting holes in the chromium layer and penetrated through it to damage the silicon dioxide beneath it.

To remedy this, we changed the structure of the hard mask into a 5-layer structure of Cr/Au/Cr/Au/Cr with thickness of 5nm/ 20nm/ 50nm/ 20nm/ 50nm. The bottom 5 nm chromium layer is used as an adhesive layer between the 20nm gold film and the silicon dioxide layer beneath. The double gold layer sandwiched between the Cr films will help stop the HF (10:1) from penetrating through the hard mask.

The deposition is done using CHA e-beam evaporator solution tool. The main deposition chamber is vented to atmosphere upon which we can open the chamber door and load the samples inside. The samples are fixed on to a sample holder using clamps. The sample holder is then loaded into the main deposition chamber. The target source materials – chromium pellets and gold target are filled up to two-thirds inside a graphite crucible and loaded into their respective specific target notches. The main chamber door is then closed. The rest of the deposition is fully automated. But he deposition principle is the same as the e-beam evaporation deposition. The process parameters are programmed into the process editor. The film number and film thickness requirements are programmed into five steps, with each step for specific film deposition in the process editor. The density and z-factor for each film to be deposited is checked. The deposition rate for both the chromium and gold films is set to 0.5 A/s to get a uniform and good quality deposition. Once all the parameters are set, the autorun process is started. The rest of the process is automated. The chamber is first evacuated to a pressure setpoint of 3×10^{-6} mTorr, the e-beam current is automatically ramped up gradually till a stable deposition rate of 0.5 A/s is obtained, the shutters are opened and the deposition starts. After all films are deposited and deposition is completed the system asks whether we want to vent the chamber. We wait for 2 minutes for the target material to cool down to room temperature

before venting the main deposition chamber. Once the vent is complete, the target crucibles and the samples are taken out and the chamber door is closed.

3.3.3 Lift-Off

Our initial lift-off process was immersing the samples in acetone and sonicating for 15 minutes. However, we found that this leaves behind a lot of residue particles scattered on the samples as observed under an optical microscope. We then added a 15-minute sonication in iso-propyl alcohol step after the acetone sonication step. We also added a couple more steps detailed below in order to be completely sure to remove any residue from the samples after sonication step.

Our modified lift-off process is as follows. We hold the sample upside down with a Teflon tweezer in an acetone filled beaker for 1 minute without any shaking. Then we move it to a second acetone beaker and vigorously shake the sample held upside down. The metal layers above the photoresist will start flaking in the first step and will fall down into the acetone beaker in the second upside down shaking step. We then hold the sample with a Teflon tweezer and rinse it with an acetone squeeze bottle to remove any remaining visible resist from the sample. The samples are then transferred to a third acetone beaker and sonicated for 15 minutes. The samples are then taken out and rinsed under IPA using a squeeze bottle and transferred to an IPA filled beaker and sonicated for 15 minutes. After the sonication, the samples are taken out and gently blow dried with nitrogen. They are observed under an optical microscope to see if the samples are devoid of any debris from sonication and to check if the patterns are well defined.

3.3.4 Reactive Ion Etching – Dry etching

Now that we have the island regions covered with the hard mask structure, we can proceed to etch away all the surrounding Silicon dioxide sacrificial layer. To this end we first etch back using reactive ion etching which gives us a unidirectional etching profile. The 5-layer hard

mask protects the silicon dioxide beneath it, thereby forming a pillar structure with the hard mask on top.

We leave behind a margin of nominal 70 nm of silicon dioxide and etch back the rest of the silicon dioxide using RIE. The margin is left behind so that the silicon surface is not exposed to the etching gases as this might damage the contact area for the source and drain electrodes. The process parameters for the RIE are as follows:

Step 1:

Power: 600 W

Pressure: 160 mTorr

CF_4: 30 sccm

O_2: 3.6 sccm,

Time: 229 seconds

Step 2:

Power: 350 W

Pressure: 200 mTorr

O_2: 11 sccm

Time: 286 seconds (1.25 times the SiO_2 etch time)

The remaining silicon dioxide thickness is measured using Ellipsometer and Reflectometer (Ocean Optics) using a measured refractive index of 1.4668 for CHA e-beam evaporator silicon dioxide.

3.3.5 HF Lateral etching

After the reactive ion etching, the remaining feature will look like a silicon dioxide pillar with a hard mask made of 5 layers on top. The width of the hard mask and the top of the pillar has the same width. We now need to etch the remaining silicon dioxide present on the rest of the sample. In addition, we also need to laterally etch the silicon dioxide pillar. This will create a T shaped feature in the island region and expose the silicon surface beneath the T feature. We can then use this region to establish a contact area between the source and drain metal electrodes and the silicon channel. We need to laterally etch a nominal thickness 400 nm to 800 nm on both sides of the silicon dioxide pillar. The island widths that are printed vary from 1.6 um ~ 1.8 um to 5.4 um. After lateral etching, this will leave behind a very thin island for the smallest width island. This lateral etching process needs to be well controlled. For this purpose, we ran multiple etch rate tests on dummy samples to determine the etch rates for various silicon dioxide films. For CHA e-beam evaporation deposited silicon dioxide, the etch rate using HF (250:1) was calculated to be 0.57 nm/s. This gave us enough control to not over etch the side walls of the silicon dioxide pillars. For a nominal etch width of 800 nm, the nominal etch time for CHA e-beam evaporator silicon dioxide using HF (250:1) is 23 minutes and 23 seconds. The samples are immersed in a beaker containing HF (250:1) for 23 minutes and 23 seconds. After the etching is completed, the samples are transferred to a fresh DI water container and stirred regularly for 5 minutes, rinsed under running DI water and then immersed into another DI water beaker with regular stirring for 5 minutes. The samples are then very gently blow dried with nitrogen. The blow drying needs to be very gentle as after the HF etch, the remaining island pillars are very thin and could be destroyed by high pressure nitrogen blow drying.

3.3.6 Passivation Layer – Silicon Dioxide deposition

After the HF lateral etch process is complete, the rest of the sample substrate needs to be protected using a passivation layer. However, we also need to leave the exposed silicon region around the silicon dioxide pillar intact to create contact region with the source and drain electrodes. We need to deposit 30nm silicon dioxide using a deposition method which is not conformal deposition. E-beam evaporation is not a conformal deposition method, thus the overhang of the hard mask above the silicon dioxide pillar will create a small region around the pillar which will not be deposited with any material.

For this passivation layer, we deposit 30 nm of silicon dioxide using CHA e-beam evaporator. The deposition process for CHA e-beam evaporator is the same as explained in section 3.3.1. The samples are fixed on a sample holder using clamps and loaded into the main deposition chamber along with the crucible containing the source target material, i.e. silicon dioxide pellets filled to two-thirds of its capacity. The hood is closed, main chamber is pumped down to a pressure of 5×10^{-6} mTorr and the deposition is started after checking the film parameters in the thickness monitor. After deposition, the samples are taken out and we can proceed to the next step in the fabrication process.

3.3.7 Planarization Coating and RIE Etch Back

In order to proceed with the fabrication process, we need to get rid of the 5-layer hard mask deposited on top of the silicon dioxide pillar. We need to do this without attacking the rest of the sample surface. To this end, we spin coat the samples with a planarization resist and then etch back until only the top of the hard mask is exposed. We use a planarization resist because this will help create a nearly flat surface after spin coating and not form a bump on top of the hard mask on top of the island region. That would defeat the purpose of the resist coating and etch back.

The planarization resist we use is PC3-700. The spin coating parameters are as follows:

Step 1: 800 rpm; 100 rpm/s; 80 seconds

Step 2: 0 rpm; 1000 rpm/s; 0.1 seconds

The sample is then preheated on a hot plate at 200°C for 2 minutes. The refractive index for the planarization resist was measured using Metricon equipment. The thickness of the planarization resist on the samples is measured using Ellipsometer using the measured refractive index of 1.6189. The average thickness was measured to be 1061.52 nm. The island structure consists of 450nm of silicon dioxide pillar and 145 nm of hard mask layers and 30nm of passivation silicon dioxide film on top. The etch back process needs to etch just enough to expose the flat top surface of the passivation oxide layer on top of the hard mask without exposing the silicon dioxide pillar underneath. Thus, we have a margin of 175 nm after the top flat surface is exposed. This makes the total height of the pillars to be 625 nm. The pillar structure is the same as that of the alignment marks. Using reactive ion etching we etch back slightly more than 436.52 nm. The RIE process parameters are as follows:

Power: 350 W

Pressure: 200 mTorr

O_2: 11 sccm

Nominal Time: 800s + additional etch time if flat surface is not exposed.

After the initial 800 seconds etching, the samples surface profile is measured using a profilometer. We use KLA Tencor – P6 profilometer to measure the surface profile around the alignment marks on the samples. If the profile shows a flat surface, we move on to the wet etching step. If the profile is not a flat surface, we need to etch additional 50 seconds using the above recipe. We check for the flat surface using profilometer and if there is no flat surface

visible, we repeat the process until we observe a flat surface using the profilometer. Once all samples have a visible flat surface in the profilometer profile and the height of the flat surface from the surrounding planarization resist surface is less than 175 nm, this means that the silicon dioxide pillar is not exposed and we can proceed to the next step.

3.3.8 Wet etching for Hard Mask

As the flat top surface of the alignment marks is exposed, this indicates that the flat surface of the islands is also exposed. We can then systematically etch each layer present on top of the silicon dioxide pillar. The top surface is 30nm silicon dioxide followed by 50 nm of chromium, 20 nm of gold, 50 nm of chromium, 20 nm of gold and 5 nm of chromium. Thus, we use the following chemicals and wet etch steps to remove these layers:

HF (50:1): 30 seconds – to remove 30 nm of CHA e-beam silicon dioxide

HCl: 10 seconds – to remove any Cr_2O_3 formed on top of Cr layer

Cr Etchant: 1 minute – to remove 50 nm Cr layer

Au Etchant: 30 seconds – to remove 20 nm Au layer

HCl: 10 seconds – to remove any Cr_2O_3 formed on top of Cr layer

Cr Etchant: 1 minute – to remove 50 nm Cr layer

Au Etchant: 30 seconds – to remove 20 nm Au layer

HCl: 10 seconds - to remove any Cr_2O_3 formed on top of Cr layer

Cr Etchant: 10 seconds – to remove 5 nm Cr layer

The samples are rinsed in a DI water beaker after all the wet etch steps are completed.

3.3.9 PR removal and Sample Cleaning

After the wet etch is completed, we need to remove the planarization resist from the samples so that we can process the rest of the sample area. The Planarization resist is removed by immersing the samples in an acetone filled beaker and sonicating them for 15 minutes followed by immersing them in an isopropanol filled beaker and sonicating for 15 minutes. The samples are rinsed in isopropanol from an isopropanol squeeze bottle prior to immersing them in the isopropanol filled beaker. This is followed by a UV ozone cleaning process. The samples are placed under a UV lamp and ozone is pumped into the chamber. The UV ozone cleaning process is done for a duration of 15 minutes.

3.3.10 Degassing

Due to the low quality of the CHA e-beam evaporator silicon dioxide, after the acetone sonication process, acetone can seep into the pores in the silicon dioxide used for the passivation oxide layer. We need to get rid of this acetone diffused inside the silicon dioxide layer. To this end, we introduced the degassing step to our fabrication process. In this step, we need to heat the samples to 200°C in an evacuated environment to facilitate easy evaporation and evacuation of acetone from our samples. We use the AJA sputter tool to degas the samples at 200°C. The samples are fixed on to a sample holder using clamps. The sample holder is then loaded into a load lock chamber. The load lock chamber is pumped down to a pressure of 5 x 10^{-5} mTorr. The sample holder is then inserted into the main deposition chamber which is maintained at a pressure lower than 3 x 10^{-7} mTorr. Once the samples are inside the main chamber, the substrate rotation is turned on. The temperature of the heater inside the chamber is slowly ramped up to 200°C over a period of 30 minutes to avoid thermal shock to the samples. The temperature is maintained at 200°C for 2 hours after which the heating is turned off. The chamber temperature takes 1 hour and 30 minutes to return to room temperature. The samples are unloaded and stored for further processing.

3.3.11 Second Mask Lithography for Source and Drain Electrode Patterning

The next stage in the fabrication process is the second mask lithography for patterning the source and drain electrode pads. The Lithography Mask pattern consists of the source and drain electrode pads connected by a thin strip. This pattern needs to be perfectly aligned on top of the silicon dioxide island in the middle which will separate the source and drain electrodes. The samples are spin coated with a negative tone resist – NR9-1000PY. The parameters for spin coating are as follows:

Step 1: 500rpm, 100rpm/s, 5s

Step 2: 3000rpm, 1000rpm/s, 60s

Step 3: 0rpm, 1000rpm/s, 0.1s

The samples are pre-baked after spin coating at 150°C for 1 minute. The Lithography is done using OAI Aligner tool in the Bay 1 area of the Nanofab cleanroom facility. The photomask and substrate carrier are loaded into the OAI aligner. The sample is placed on the substrate carrier and is fixed in place using scotch tape. The alignment marks on the sample from the first mask patterning and the alignment marks of the second mask pattern need to be perfectly aligned using the X-axis and Y-axis movement and rotation movement of the substrate. After the alignment is perfect the substrate is pushed upwards to make contact with the photomask. The motion of the substrate needs to be slow so that the alignment is not disturbed. Once the contact is made and the alignment is still perfect, the contact vacuum function is enabled to hold the substrate to the mask firmly in place. The samples coated with the negative photoresist are then exposed to UV light to print the pattern onto the resist. The exposure parameters are as follows:

Mask mode: Vacuum Contact Mode

Pressure setting current: 14 mA

Measured Beam Intensity: 17.4 mW/cm^2

Exposure Time: 6.9 seconds

Dose: 120 mJ/cm^2

After exposure, the samples are then post baked at a temperature of 100°C for 1 minute on a hot plate. After allowing the samples to cool down to room temperature, the resist is developed in a Negative Resist developer – RD6. The samples are immersed in the RD6 developer with constant stirring for 10 seconds and immediately transferred to a DI water container under regular stirring for 10 minutes. The DI water container is changed after 5 minutes with fresh DI water in a second container.

The samples are blow dried gently with nitrogen and observed under an optical microscope to confirm whether the patterns are printed perfectly on top of the islands. Now, the immediate region beside the silicon dioxide pillar is bare silicon area and has been exposed after the second mask lithography. We then move on the next step. The subsequent deposition steps will deposit the layers in the bare silicon region exposed by the second mask lithography step and on top of the passivation silicon dioxide layer, also exposed after the second mask lithography step and on the rest of the sample covered by the negative photoresist.

3.3.12 Tunnelling Barrier Deposition

At this stage, we separate the samples into three different structures for the interface region between the silicon channel and the source and drain electrodes. For Sample A, the source and drain metal electrodes, namely, chromium needs to be in direct contact with the silicon channel. For Sample B, we want to separate the metal electrode from the silicon channel by using a tunnelling barrier – a 2 nm silicon dioxide layer to separate the source and drain electrodes

from the silicon channel. For sample C, in addition to the tunnelling barrier, we introduce another layer which acts as an energy filter that should help in suppressing the thermally excited electrons and preventing them from passing through the silicon channel without applied gate bias. Thus, our sample A will act like a normal MOSFET transistor, Sample B will behave like a MOSFET transistor with a slightly controlled current flow between source and drain. Sample C will behave as a Cold Electron Transistor.

Thus, after the second mask lithography is completed, samples B and C need to be deposited with 2 nm film of silicon dioxide. This deposition is done using AJA Sputter tool. The deposition rate of silicon dioxide using AJA Sputter is 0.00528 nm/s. This slow rate of deposition gives us a very good control over the thickness of the silicon dioxide tunnelling barrier deposition. Thus, in order to deposit a thin film of 2 nm of silicon dioxide, AJA sputter deposition was a suitable deposition method. Samples B and C were fixed on to the sample holder using clamps and loaded into the main deposition chamber using a load lock mechanism. The substrate rotation is turned on and the deposition process is started. The deposition process is divided into two steps. The first step is called the spark step followed by the actual deposition step. The spark step helps to ignite the plasma. The deposition parameters are as follows:

Step 1: SiO_2 Spark

Ignition Pressure: 35 mTorr

Power: 64 W

Ar: 30 sccm; O_2: 6 sccm

Temperature: Room Temperature

Coat Time: 3 seconds (Plasma ignition)

Step 2: 2 nm SiO_2 Deposition

Power: 148 W

Deposition Pressure: 5 mTorr

Ar: 30 sccm; O_2: 6 sccm

Temperature: Room Temperature

Pre-sputter Time: 120 seconds (required for target cleaning) (Sample shutter is closed.)

Deposition Time: 313.3 seconds

During the beginning of deposition process the load and tune parameters need to be manually adjusted so that the reflected power remains at a minimum of 0 W to 1 W. Once it stabilizes at a value of 1 W or 0 W, the rest of the deposition process is automated. Once the deposition process is done the samples are unloaded through the load lock mechanism.

3.3.13 Energy Filter Deposition – 2 nm Chromium Oxide deposition

After deposition of 2 nm silicon dioxide tunnelling barrier, the sample holder is unloaded, and sample B is taken out to be stored. The sample holder with the sample C is inserted back into the AJA sputter load lock and transferred to the main deposition chamber. The loading procedure is the same as in section 3.3.14. We now need to deposit the energy filter layer of 2 nm of Cr_2O_3 which is an essential component to distinguish the devices on sample C into Cold Electron Transistor devices. As before, the deposition process is made up of two steps. The process parameters are as follows:

Step 1: Cr_2O_3 Spark

Ignition Pressure: 35 mTorr

Power: 64 W

Ar: 30 sccm; O_2: 6 sccm

Temperature: Room Temperature

Coat Time: 3 seconds (Plasma ignition)

Step 2: 2 nm Cr_2O_3 Deposition

Power: 148 W

Deposition Pressure: 5 mTorr

Ar: 30 sccm; O_2: 6 sccm

Temperature: Room Temperature

Pre-sputter Time: 120 seconds (required for target cleaning) (Sample shutter is closed.)

Deposition Time: 200 seconds

At the start of the deposition process the load and tune parameters need to be manually adjusted in order to keep the reflected power to a minimum of 0W to 1 W. After the reflected power stabilizes, the rest of the deposition process is automated.

Once the deposition is completed, the sample holder is taken out through the load lock chamber. The sample C is then taken out and stored.

3.3.13 Metal Electrode Deposition

At this stage, we now have the three samples A, B and C. Each sample has a different channel junction structure. Sample A has bare silicon in the immediate surrounding region of the silicon dioxide pillar. Sample B has 2 nm of silicon dioxide deposited on top of the bare silicon region surrounding the silicon dioxide pillar and the metal electrode pad area above the passivation silicon dioxide and over the negative photoresist covering the rest of the sample. Sample C has 2 nm of silicon dioxide and 2 nm of Cr_2O_3 deposited on top of the bare silicon region

surrounding the silicon dioxide pillar and the metal electrode pad area above the passivation silicon dioxide and over the negative photoresist covering the rest of the sample. We can now proceed with deposition of the metal electrode on all three samples. The metal electrode we are depositing here will be Chromium due to this providing a band bending behaviour when in contact with the 2 nm chromium oxide which acts as an energy filter and enabling the suppression of thermally excited electrons.

The deposition is done using CHA e-beam evaporator solution tool. The samples are fixed on a sample holder with clamps and loaded into the main deposition chamber of CHA E-beam Evaporator Solution after venting the chamber. The source target of chromium pellets is filled up to two thirds of a graphite crucible and loaded into the target slot inside the main deposition chamber. The chamber door is closed shut, and the automated deposition process is started after programming the deposition parameters into the process editor. The process parameters are as follows:

Chamber Pressure: 3×10^{-6} mTorr

Deposition Rate: 1.0 A/s

Deposition thickness: 1000 A = 100 nm

Deposition temperature: Room Temperature

Once the deposition is done the samples are taken out and we proceed to the next step.

3.3.14 Lift-off / Sample Cleaning and Degassing

It is imperative that the Lift-off process be carried out on the same day as the spin coating process for the second mask lithography as a delay in the photoresist removal will result in an increase in the difficulty to remove the resist coating.

The samples A, B and C are held upside down for 1 minute under immersion in acetone. They are then shaken upside down in a second beaker filled with acetone for 1 minute and then rinsed under acetone from a squeeze bottle and transferred to a third beaker filled with acetone and sonicated for 15 minutes. The samples are taken out and rinsed with isopropanol from a squeeze bottle without allowing the acetone on the samples to dry. If the acetone is allowed to dry on the samples, it leaves behind white marks on the samples which are difficult to remove. After rinsing with isopropanol, the samples are transferred to a beaker filled with isopropanol and sonicated for 15 minutes. The samples are taken out and gently blow dried with nitrogen. The samples are then cleaned using UV/ Ozone cleaning step. The samples are placed under a UV lamp while ozone gas is being pumped into the chamber. This process is done for 15 minutes. As the samples have been sonicated in acetone, we need to get rid of the acetone that has seeped inside the pores of the passivation silicon dioxide layer. As stated in section 3.3.10 the degassing procedure is the same as before. The samples are loaded into AJA sputter tool and evacuated to 3 x 10^{-7} mTorr. The temperature is ramped up gradually to 200°C in 30 minutes. The samples are maintained at 200°C for 2 hours and the heating is turned off. The chamber takes 1 hour and 30 minutes to return to room temperature.

3.3.15 Passivation Oxide Deposition

We now, need to deposit passivation layer of silicon dioxide over the entire sample. The deposition is done using AJA Sputter. As the samples are already inside the AJA sputter during the degassing step, we can start the deposition process once the chamber temperature reaches room temperature. As before the deposition is done in 2 steps. The deposition parameters are as follows:

Step 1: SiO_2 Spark

Power: 64 W

Pressure: 35 mTorr

Ar: 30 sccm; O_2: 6 sccm

Temperature: Room temperature

Coat Time: 3 seconds (Plasma ignition)

Step 2: 50 nm SiO_2 Deposition

Power: 148 W

Deposition Pressure: 5 mTorr

Ar: 30 sccm; O_2: 6 sccm

Temperature: Room Temperature

Pre-sputter Time: 120 seconds (required for target cleaning) (Sample shutter is closed.)

Deposition Time: 7837 seconds

The deposition rate for the 50 nm Silicon dioxide was calculated to be 0.00638 nm/s. After deposition the sample holder is taken out and samples are unloaded for the next process.

3.3.16 Planarization Coating and RIE etch back

Now that the source and drain electrode pads have been deposited, and the silicon dioxide island pillar has helped to create contact with silicon channel and to separate source and drain electrodes, we no longer need the silicon dioxide pillar. In fact, we need to remove this pillar structure in order to deposit the gate oxide and gate electrodes. For this purpose, we need to etch away the silicon dioxide pillar without affecting the surrounding silicon dioxide and metal layers.

The first step to do this is to coat the entire sample with planarization resist and then etch back till the pillar is exposed. The spin coating parameters for the planarization resist is as follows:

Step 1: 800 rpm; 100 rpm/s; 80 seconds

After spin coating the samples are heated to 200°C for 2 minutes on a hot plate.

The next step is to etch back the planarization resist to expose the top flat surface of the pillar. As before we start by etching for 800 seconds using reactive ion etching and measuring the surface profile using KLA Tencor P6 – Profilometer. If the flat surface is not exposed, then we repeat the etch step for 50 seconds and measure again. Once the flat surface is visible in the profilometer surface profile of the alignment mark area, this means that the flat surface area for the pillar region is also exposed and we can move on to the wet etch step for the pillar removal.

3.3.17 Chromium and Silicon Dioxide Pillar removal

Now, with the top surface of the pillar exposed and the rest of the sample protected by the planarization resist, we can begin to systematically etch away the layers and get rid of the pillar. The top surface is a 50 nm layer of silicon dioxide followed by 100 nm of Chromium, 2 nm of chromium oxide, 2 nm of silicon dioxide and 450 nm of silicon dioxide pillar. The wet etch steps and etchants used for the wet etch step are as follows:

HF (50:1): 40 seconds – to remove 50 nm of AJA Sputter silicon dioxide – Etch Rate = 3.2 nm/s

HCl: 10 seconds – to remove any Cr_2O_3 formed on top of Cr layer

Cr Etchant: 35 seconds – to remove 100 nm Cr layer – Etch Rate = 4 nm/s

HF (50:1): 350 sconds~480 seconds – to remove 450 nm of CHA e-beam evaporated silicon dioxide pillar.

Samples are rinsed in DI water containers and blow dried with nitrogen after the wet etch steps are completed.

The etch rate for the pillar is much slower than expected due to the multiple degassing steps which heated and evacuated the oxide layer during fabrication process and improved the quality of the silicon dioxide used for the pillar formation. The final HF (50:1) step is repeated until there is no more silicon dioxide remaining in the island region. This can be roughly determined by observing under an optical microscope. The silicon island coloration needs to be uniform in order to have etch away all the silicon dioxide in the region to be etched away.

3.3.18 Planarization Resist Removal / Sample Cleaning and Degassing

Once we established that there is no more silicon dioxide present in the island region, we can then proceed to remove the planarization resist from the samples. The Planarization resist removal and sample cleaning procedure is the same as in section 3.3.9 and for degassing in section 3.3.10. The PR removal step consists of 15 minutes of sonication in acetone followed by 15 minutes of sonication in isopropanol and 15 minutes of UV/ Ozone cleaning. The degassing is done in AJA Sputter tool at 200°C for 2 hours. After the chamber temperature returns to room temperature after 1 hour and 30 minutes, the samples are taken out and are ready for the next stage in the Cold Electron Transistor fabrication procedure.

3.3.19 Gate Oxide Deposition

We now have source and drain electrodes for our devices and an energy filter mechanism at the silicon channel junction. We have etched away the silicon dioxide pillar between the source and drain electrodes and exposed the silicon channel. The next stage required to complete the transistor device is to pattern and deposit a gate oxide and gate electrode in the channel region.

For, the gate oxide dielectric choice we started with silicon dioxide. Initially we used AJA sputter to deposit 10 nm gate oxide. But after device completion, we found that there was a lot

of gate leakage. So, our next goal was to reduce the gate leakage in the transistor device. We increased the gate oxide thickness to 20 nm of Sputtered oxide, but the gate leakage was still present. We then assumed that the problem was with the quality of the silicon dioxide used as a gate oxide. Thus, we switched to plasma enhanced chemical vapor deposition to deposit 10 nm silicon dioxide as a gate oxide. The PECVD deposition process was done in multiple steps. The PECVD equipment is a fully automated deposition tool. The first step we run before beginning our process is the PECVD clean recipe programmed into the computer. Then we run a conditioning recipe to deposit 50 nm thickness of silicon dioxide using our recipe. If the deposition rate is close to the established value, we can then proceed with silicon dioxide deposition for the main samples. The process parameters we use for this deposition process are as follows:

Step 1:

RF Power: 0 W

ICP Power: 0 W

Temperature: 380°C

Time: 1200 seconds

Step 2:

RF Power: 10 W

ICP Power: 500 W

Temperature: 380°C

Time: 35 seconds.

After the deposition for the actual samples is done, we can then proceed to the next step in the fabrication process. With this silicon dioxide as gate oxide, we found a reduction in the gate leakage for our devices, but the leakage was still present. We needed to find a better method to prevent the gate leakage current. We have established a method in section 3.4.11 with the newer fabrication process and found there was negligible leakage to the gate electrode with higher gate bias.

3.3.20 Third Mask Lithography for Gate Metal Electrode Patterning

Now that the gate oxide dielectric layer has been deposited, we can now move on to pattern the samples to create gate electrode. Again, we use the negative tone resist – NR9-1000PY for this purpose. The negative photoresist is spin coated on all three samples. The spin coating parameters are as follows:

Step 1: 500 rpm; 100 rpm/s; 5 seconds

Step 2: 3000 rpm; 1000 rpm/s; 60 seconds

Step 3: 0 rpm; 1000 rpm/s; 0.1 seconds

After spin coating is done the samples are pre-baked on a hot plate at 150°C for 1 minute before proceeding to photolithography. The patterning is done using OAI aligner. The mask is loaded into the aligner with the third mask pattern. The samples are loaded into the aligner substrate wafer. The alignment is done with the help of the alignment mark patterned on the samples in the second mask lithography step and the alignment marks for the third mask pattern present on the chromium mask. Once the alignment is complete, the samples are exposed under UV light. The exposure parameters are as follows:

Mask mode: Vacuum Contact Mode

Pressure setting current: 14 mA

Measured Beam Intensity: 17.7 mW/cm^2

Exposure Time: 6.8 seconds

Dose: 120 mJ/cm^2

After exposure, the samples are post-baked on a hot plate at 100°C for 1 minute. After the samples are allowed to cool down to room temperature, they are immersed in a developer solution – RD6 which helps to dissolve the unexposed negative photoresist. The samples are immersed into the RD6 solution for 10 seconds with regular stirring. The samples are taken out and immersed into two DI water containers with regular stirring – with 5 minutes in each container. The samples are taken out and blow dried with nitrogen. This prints the gate electrode pattern on the photoresist.

3.3.21 Metal Electrode Deposition for Gate Electrode Pattern

Next, we need to deposit the gate electrode in the region exposed by the negative photoresist pattern area. We use Chromium metal as the gate electrode, same as the source and drain electrodes. 100 nm chromium is deposited using e-beam evaporation over the entire sample. The deposition is done using CHA e-beam evaporation solution equipment. The samples are fixed on to a sample holder using clamps. The main deposition chamber is purged with nitrogen and the samples are loaded into the chamber. Chromium pellets are filled into a graphite crucible up to the two-thirds level and the crucible is loaded into the target slot of the main deposition chamber in CHA e-beam evaporator solution. The process parameters are programmed into the process editor and the deposition process is started. The process parameters are as follows:

Chamber Pressure: 3×10^{-6} mTorr

Deposition Rate: 1.0 A/s

Deposition thickness: 1000 A = 100 nm

Deposition temperature: Room Temperature

Once the deposition is done, we need to wait for a few minutes for the chromium pellets to cool down to room temperature, before venting the chamber. The samples are taken out.

3.3.22 Lift-off, Sample Cleaning and Degassing

We need to cover the entire sample with a passivation oxide layer to protect the sample. In order to do this, we need to remove the photoresist from the sample. The samples are immersed into acetone beaker and held stationary upside down for 1 minute. The samples are moved to a second acetone beaker and shaken vigorously, also upside down. The samples are then transferred to a third acetone beaker, right side up and sonicated for 15 minutes in acetone. After acetone sonication is complete, the samples are taken out and rinsed under isopropanol using an IPA squeeze bottle. The samples are then immersed into an isopropanol filled beaker and sonicated for 15 minutes. After sonication, the samples are taken out and blow dried with nitrogen.

The next step in the cleaning process is UV/Ozone cleaning. The samples are placed on a sample stage in the UV / Ozone tool. The samples are placed under a UV lamp. When the lamp turns on the samples are exposed to UV light for 15 minutes. The UV also generates ozone gas inside the exposure chamber. The chamber is pumped out at a steady rate. After 15 minutes is complete the lamp is turned off. We need to wait for a few minutes for the Ozone gas generated inside the chamber to be completely pumped out. The samples are then taken out and we proceed to the next step. As before, as we processed the samples using acetone sonication, the acetone might have seeped into the pores of the silicon dioxide layers deposited prior to the sonication process. Thus, we get rid of this acetone inside the silicon dioxide pores using a degassing step. The samples are heated at 200°C in an evacuated environment. This is carried

out using the AJA sputter deposition tool. The samples are loaded into the load lock chamber after fixing them on a sample holder using clamps. The load lock chamber is evacuated to a pressure of 2 x 10^{-5} mTorr. The sample holder is inserted inside the main deposition chamber using a transfer rod mechanism. The sample height is adjusted, and the sample holder rotation is turned on to 50 rpm. The Temperature of the heater is gradually raised to 200°C over a period of 30 minutes. The samples are heated at this temperature for 2 hours and then the heating is turned off. The deposition chamber takes 1 hour and 30 minutes to cool down to room temperature.

3.3.23 Passivation Oxide Deposition

The passivation oxide layer we have used here is silicon dioxide. We deposit this using AJA Sputter tool. The samples are already loaded into the AJA Sputter tool during the degassing process. The sample holder height and rotation are also already turned on. The deposition parameters are programmed into the deposition software. The deposition parameters are as follows:

Step 1: SiO_2 Spark

Power: 64 W

Pressure: 35 mTorr

Ar: 30 sccm; O_2: 6 sccm

Temperature: Room temperature

Coat Time: 3 seconds (Plasma ignition)

Step 2: 50 nm SiO_2 Deposition

Power: 148 W

Deposition Pressure: 5 mTorr

Ar: 30 sccm; O_2: 6 sccm

Temperature: Room Temperature

Pre-sputter Time: 120 seconds (required for target cleaning) (Sample shutter is closed.)

Deposition Time: 7837 seconds

After the deposition is done, the samples are taken out and stored for the next stage of the fabrication process.

3.3.24 Fourth Mask Alignment for Source, Drain and Gate Metal Electrode Contact Bond Pads

The fabrication of our devices is almost complete. We have fabricated the source, drain and gate electrode structures on the samples. But there is passivation oxide present on all three electrodes. In order to make connections to external circuits, the electrodes need to be exposed. We need to etch the oxide layer from the top of the electrodes. Before we do this, we need to protect the surrounding region from the etch process. Our fourth Mask lithography step comes into play here. The fourth mask pattern consists of three circular shaped patterns above the source, drain and gate electrode. We use a negative photoresist – NR9-1000PY for this process. The resist is spin coated on to the samples using the following parameters:

Step 1: 500 rpm; 100 rpm/s; 5 seconds

Step 2: 3000 rpm; 1000 rpm/s; 60 seconds

Step 3: 0 rpm; 1000 rpm/s; 0.1 seconds

The samples are pre-heated at 150°C for 1 minute. The lithography is done using OAI Aligner. The chromium mask with the fourth mask pattern is loaded into the OAI Aligner. The samples

are loaded onto a carrier wafer and loaded into the OAI Aligner. The alignment is done using the alignment marks printed onto the sample during third mask lithography and the alignment marks present on the fourth mask. Once the alignment is good, the samples are exposed to the UV light. The exposure parameters are as follows:

Mask mode: Vacuum Contact Mode

Pressure setting current: 14 mA

Measured Beam Intensity: 17.4 mW/cm^2

Exposure Time: 6.9 seconds

Dose: 120 mJ/cm^2

After exposure, the samples are post-baked at 100°C for 1 minute. The samples are allowed to cool down and are then immersed in a developing solution – RD6 while stirring regularly for 10 seconds. The samples are then transferred to a DI water container for 5 minutes and stirred regularly. After 5 minutes the samples are transferred to a second DI water container with regular stirring for 5 more minutes. The samples are taken out and blow dried with nitrogen.

3.3.25 Passivation Oxide Etching for Metal Electrode Exposure

The next step is to etch away the silicon dioxide present on top of the three electrodes. The source and drain electrodes have 50 nm of silicon dioxide as a passivation oxide layer deposited after the second mask lithography, 10 nm of PECVD deposited silicon dioxide deposited during gate oxide deposition and another 50 nm of global silicon dioxide as a passivation oxide layer deposited after the third mask lithography step. This brings the total thickness of silicon dioxide on top of source and drain chromium electrodes to 110 nm.

The gate chromium electrode on the other hand has 50 nm of global silicon dioxide on top of it which was deposited after the third mask lithography step.

We use reactive ion etching to etch away the silicon dioxide from the circular shaped holes in the photoresist created using the fourth mask lithography. We need to adjust the reactive ion etching time to etch the 110 nm of silicon dioxide present on top of the source and drain chromium electrodes. We also need to have a margin of at least 20% to ensure that all the silicon dioxide is etched from the circular region. As we are aiming to etch the 110 nm of silicon dioxide from the source and drain circular region, this will also etch the 50 nm of silicon dioxide present on top of the gate chromium electrode. The etch rate for silicon dioxide was calculated to be 0.7 nm/s when photoresist is present on the sample. The etch parameters used for this process are as follows:

Step 1:

Power: 600 W

Pressure: 160 mTorr

CF_4: 30 sccm

O_2: 3.6 sccm,

Time: * seconds

Step 2:

Power: 350 W

Pressure: 200 mTorr

O_2: 11 sccm

Time: 120 seconds

After the etching is done, the samples are taken out and the contact current is measured for random devices in each region of the sample. For this purpose, two probe tips are connected to

the same electrode circular pad and IV is measured after applying a potential of 0 V to 0.01 V. For good contact, the IV needs to be linear and the current value should be in the 10^{-4} A range. This will confirm that the chromium metal electrode beneath the silicon dioxide is exposed. If the IV is not linear or if the current is very low, this would indicate that there is still some silicon dioxide present on top of the chromium. We then need to etch for more time and repeat the IV measurements for confirmation.

Once we obtain a good contact IV measurements, we can move on to the next step.

3.3.26 Contact Bond Pads Metal Deposition

The chromium metal of the electrodes is now exposed. If we leave it alone, exposed to the air, the chromium surface will get oxidised and a thin layer of a few nm of chromium oxide will form on the chromium metal electrode. This will insulate the metal electrode from the IV probe station probe tip connections.

In order to prevent oxidation, we need to coat the chromium electrode with a thin layer of gold. As gold will not get oxidised when left in the air, and it is also a good conductor, it is an ideal material to coat the chromium metal electrodes. We need to deposit 5 nm of chromium and 20 nm of gold on top of the samples. The deposition is done using CHA e-beam evaporator Solution tool. The samples are fixed on to a sample holder using clamps and are loaded into the main deposition chamber of the CHA e-beam evaporator solution. Two crucibles filled up to two-thirds with chromium and gold are loaded into the respective target slots. The chamber door is closed, the deposition parameters are programmed into the software and the process is started. The deposition parameters are as follows:

Chamber Pressure: 3×10^{-6} mTorr

Deposition Rate: 0.5 A/s

Deposition thickness:

Film 1: Cr :: 50 A = 5 nm

Film 2: Au :: 200 A = 20 nm

Deposition temperature: Room Temperature

The samples are taken out after the deposition is done.

3.3.27 Lift-Off and Sample Cleaning

The next step is to remove the photoresist beneath the chromium and gold layers. The lift-off process is the same as before. The steps are given below:

Step 1: 1-minute stationary upside down in acetone: Beaker 1

Step 2: 1-minute vigorous shaking upside down in acetone: Beaker 2

Step 3: 15-minute sonication in acetone: Beaker 3

Step 4: Rinsing sample in isopropanol using IPA squeeze bottle

Step 5: 15-minute sonication in isopropanol: Beaker 4

After the above steps are completed, the samples are blow dried with nitrogen. We then place the samples under a UV lamp in a isolated chamber for 15-minutes. The UV light exposure also generates ozone gas which is continuously pumped out. After the process is complete, the samples are taken out.

The fabrication procedure for the samples is now complete and the devices can now be measured for IV data using the IV Probe Station.

3.4 New Fabrication Process

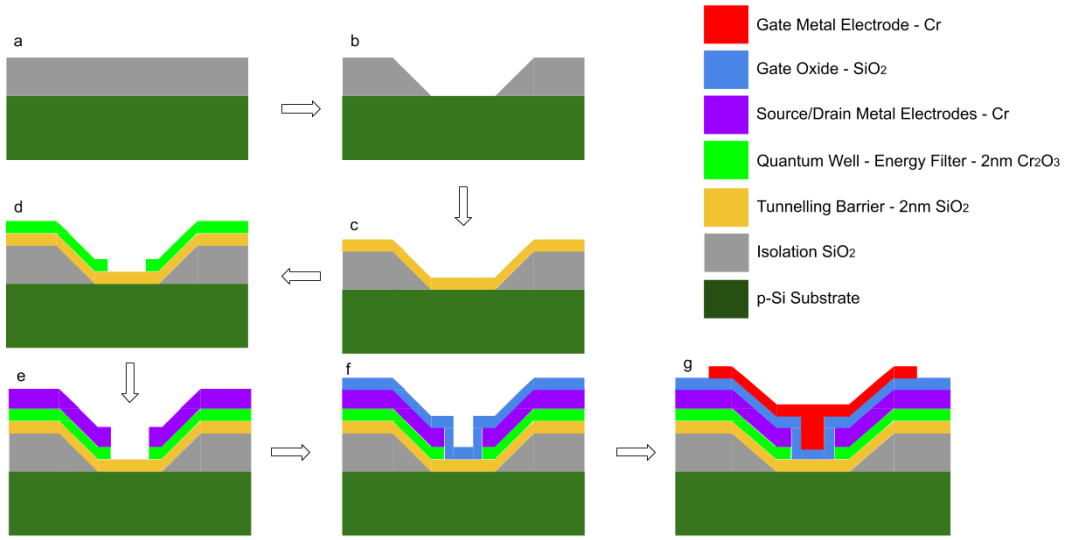

Figure 6: Process flow for large scale fabrication of CET using new mask design

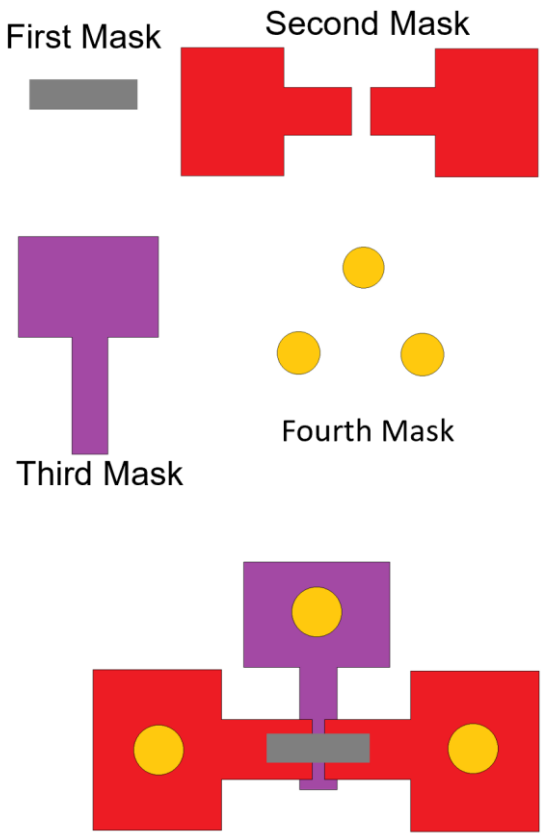

Figure 7: New Mask Design for faster fabrication procedure

3.4.1 Phosphorous Doping (n-type) for p-type Si wafer

Test grade p-type Silicon (100) wafers are used as substrate for Cold Electron Transistor Devices and are heated at 200° C for 20 minutes on a hot plate. They are then immersed in a 3:1 Piranha solution of H_2SO_4:H_2O_2 for 30 minutes to get rid of any organic impurities on the wafer. The wafers were then rinsed with DI Water by immersing it in a DI water container for 5 minutes followed by Rinsing the wafer under running DI water and immersing in fresh DI water container again for 5 minutes which is hereafter referred to as the DI water rinsing process. After getting rid of any organic impurities, the wafers are then immersed in 10:1 Hydrofluoric acid for 5 minutes to remove the native oxide from the wafers, followed by the Di water rinsing process.

The cleaned wafers are then spin coated with Phosphorus dopant. The spin-coating was done in a 2-step process. Step 1 rotates the sample at 500rpm for 30 seconds which spreads the dopant evenly all over the Si Wafer. Step 2 rotates the sample at 4000 rpm for 60 seconds. The wafer is then loaded into Lindberg furnace. The furnace then runs a Semi-automatic process which is programmed into it before loading the wafers. This is the Pre-Dep step. Here the dopant ions are diffused into the wafer surface. Multiple temperature setpoints and the time to reach each setpoint are specified and the process is then started. Setpoint 1 - 25° C to Setpoint 2 - 900° C is set to reach in 25 minutes. The temperature is held constant at 900 ° C for 10 minutes and then the heating is turned off. When the temperature cools down to room temperature, the wafers are taken out and striped with HF (10:1) etching for 5 minutes to remove any dopant liquid remaining on the wafer surface. The next step is the Drive-in where the ions diffused into the wafer surface are driven deeper inside the wafer. The drive-in process setpoint is at a higher temperature of 1100° C. It is programmed to take 30 minutes to reach this temperature where the furnace remains for 2 hours. Then the furnace heating is turned off. Upon cooldown the wafer is taken out and another HF (10:1) strip is done by immersion for 5

minutes to clean the surface of any remaining diffused impurities. The wafer is now ready for isolation oxide coating.

3.4.2 Isolation Oxide Deposition / Growth

The cleaned wafers are then loaded into the Tystar thermal oxidation in order to grow the desired thermal oxide thickness which acts as the isolation oxide for our device. The wafers were inserted into the quartz tube held at 450° C at a rate of 1 inch/minute to reduce any chance of thermal shock. As the wafer is being inserted into the tube, the chamber is continually being purged with nitrogen gas at 5000 sccm. The loading process takes 15 minutes. The wafers will be situated roughly in the mid zone of the quartz tube. The temperature of the furnace is then slowly ramped up to 700°C in 30 min and is held at that temperature for 15 minutes to stabilize the chamber condition. The temperature is then ramped up to 800°C over another 15 minutes. Upon reaching 800°C, the nitrogen gas is turned off and the chamber is purged with oxygen gas at 3000 sccm and is held for 3 hours 27 minutes. Once the duration is over the temperature is set to cool down to 700°C in 2 hours where it is held till unloading. The samples are then taken out of the furnace and allowed to cool down before transferring it to a sample box. The thickness of the SiO_2 film grown is measured using Ocean Optics NC-UV-Vis Reflectometer and Gaertner Ellipsometer. The thickness was found to be ~62nm to 69nm. The isolation oxide thickness was adjusted to 100nm for the subsequent batches following the etch rate fluctuation to leave a sufficient margin of thickness for SiO_2. The oxidation temperature was adjusted to 1100°C and the growth time was adjusted to 35 minutes. The thickness was measured to be 100 nm to 110nm.

3.4.3 Photolithography – First Mask for Island Pattern

Once the isolation oxide is grown, the next step in the fabrication process is to pattern the island region between Source and Drain electrodes in order to make contact between the source-drain electrodes and Si substrate which acts as the channel for current flow between source and drain.

The wafer is cut into four quadrants. One quadrant is used for each batch of Samples and can be further divided into three samples – A, B and C. The quadrant is heated at 200°C for 20 minutes on a hot plate. After cooldown, the quadrant is then spin coated with negative tone resist – NR9-1000PY at 3000 rpm for 60s. The quadrant is then baked at 150°C for 1 minute. The quadrant is patterned using OAI Aligner. It is exposed under the first mask pattern. The exposure is done at a dose of 120mJ/cm^2. The OAI aligner beam intensity is 19.7 mJ/cm^2, thus an exposure time of 6.1 seconds gives us a dose of 120 mJ/cm^2. After exposure, the quadrant is post baked at 100°C for 1 minute and allowed to cool down. It is then developed in a developer – RD6 for 10s and transferred to DI water container for 5 minutes under regular stirring and then transferred again to another DI water container for 5 more minutes under regular stirring. The alignment marks patterned by the first mask are observed under microscope to see if the pattern is printed well.

3.4.4 Reactive Ion Etching for SiO_2 Etch back and PR Removal

Now with the island pattern printed in the photoresist, the next step is to etch away all the SiO_2 in the island region and leave behind only Si. In order to achieve this, we use a two-step process. The first step is to etch back using RIE, leaving behind a small amount of SiO_2 so that RIE does not damage the Si surface. This is followed by a wet etching process using HF (10:1) to etch the remaining SiO_2.

Leaving behind a margin of a few nanometres, we need to etch the rest of the silicon dioxide using a CF_4 etch recipe. Initially I left behind a margin of 10nm for the 70nm isolation oxide.

The nominal time for the 60nm CF4 etch is determined using a dummy sample etch test run. The etch rate of thermal SiO_2 is determined to be 0.6 nm/s to 0.8nm/s when the photoresist is coated on the quadrant for different dummy samples. We use the average SiO_2 etch rate of 0.7nm/s to etch 60nm. The nominal etch time is 85s. Due to the fluctuation of the etch rate due to different chamber conditions and different sample sizes, some samples were over etched, while some samples had too thick SiO_2 remaining. We decided to increase the isolation oxide thickness from 60nm to 100nm. The margin of SiO_2 thickness to be left behind was adjusted to 20nm. The nominal etch time for 80nm SiO_2 was calculated to be 114s using etch rate of 0.7nm/s.

After the CF4 etch, the photoresist needs to be removed. The quadrant was rinsed with acetone for 1 minute, then sonicated in acetone for 15 minutes. This was followed by sonication in Isopropanol for 10 minutes.

After removing the PR, the etched profile is measured using KLA Tencor - P6 profilometer. If the profile was around 80nm, then we proceeded to the next step of wet etching using HF.

3.4.4 Wet Etching – HF Etch

The next step is to etch away the remaining SiO_2 in the island region to expose the Silicon surface using wet etching with the help of HF (10:1). The Etch rate was calculated using dummy samples by making a etch time vs thickness etched plot. It was determined to be 0.32nm/s for thermal oxide. The Wet etch was done in two steps of etching for half the time in each step to account for the fluctuation in the actual etch rate. HF (10:1) etching will laterally etch SiO_2 in all directions. The Silicon dioxide island length is in the order of micrometres and hence the short duration of HF (10:1) etch will only etch a few nanometres. Now since the SiO_2 remaining in the island region is around ~20nm, and we need to etch a minimum of 20nm. The minimum SiO_2 thickness of the region surrounding the first mask islands that is needed to

clearly see the alignment marks for the second mask alignment is 40nm. Thus, the maximum SiO_2 we can etch is 60nm. In this step, we etch 50 nm SiO_2 (margin of ~10nm) in two steps of 25nm each, that is a nominal etch time of 78s for each step. The thickness of the SiO_2 remaining after the first HF(10:1) etch is measured using Reflectometer and Ellipsometer. The second HF(10:1) etch time is adjusted according to the remaining SiO_2. Once both the wet etch steps are completed, the SiO_2 thickness profile is measured using KLA Tencor – P6 profilometer. The SiO2 alignment mark profile now shows reduced height of around 40nm from the initial 80nm. This reduction in the profile height confirms that the silicon surface has been exposed.

3.4.5 Tunnelling Barrier – 2nm Thermal Oxide Growth

Now, we separate the three samples A, B and C by cutting the quadrant into three parts. For Sample A, the source and drain metals will be in direct contact with the silicon surface which acts as a channel between source and drain. Sample B will have a tunnelling barrier between the source-drain metal and the silicon channel. The Sample C will have a tunnelling barrier and energy filter to separate the source-drain metals from the silicon channel. Initially, sample B and sample C were coated with 2nm of thermally grown oxide using Tystar Oxidation furnace. The loading and oxidation procedure is the same as the isolation oxide growth in the earlier stage. In order to grow 2nm thermal oxide on the silicon surface in the island region, the oxidation is carried out at 800C for 1 hour and 21 minutes. But thermal oxidation growth rate was hard to control to deposit 2nm oxide. The silicon dioxide thickness was measured before and after thermal oxidation. The measured thickness difference was around 6nm to 10nm. We adjusted the growth time to 40 minutes, but the measured thickness still fluctuated between 4nm to 10nm.

Thus, we needed to switch to a more controlled process for SiO2 deposition. For this, we used AJA Sputter to deposit 2nm of sputtered silicon dioxide on Sample B and Sample C. This was followed by the second mask alignment and development for all three samples in turn followed

by 100nm Cr deposition. IV measurement was done by measuring the current (Source-Drain IV) between source and drain for samples A, B and C to check the contact between the source and drain metal and the silicon channel. The IV showed that the current for sample B and C was very low of the order of ~ 10^-13 A indicating that the channel between source and drain was disconnected. This could have been due to one of two reasons: either the contact between the probe tips and the source-drain metal was not good or the sputtered oxide used as a tunnelling barrier was too thick. We confirmed that the probe tip contacts had no problem by testing IV measurement on Cr and Au coated samples. Thus, the problem lay with the tunnelling oxide thickness. We then adjusted the tunnelling oxide thickness to 1nm of sputtered silicon dioxide for subsequent samples.

3.4.6 Photolithography – Second Mask Alignment for Source and Drain Electrode

After sample B and C were sputtered with 1 nm of silicon dioxide, the next step in the fabrication process is to pattern the source and drain electrode pads for all three samples A, B and C. The samples are heated at 200°C for 20 minutes on a hot plate. After the samples are cooled down, they are spin coated with negative photoresist NR9-1000PY at 3000rpm for 60s. After spin coating, the sample is pre-baked at 150°C for 1 minute. The samples are patterned using OAI Aligner. The second mask pattern is used for exposure. Varying dosages were used for multiple dummy samples to optimize the correct dose for the required gap length between source and drain electrodes. The optimum dose was determined to be 200mJ. The OAI aligner beam intensity is 19.7 mJ/cm^2, thus an exposure time of 10.1 seconds gives us a dose of 200 mJ. The alignment is done using alignment marks on the sample patterned using the first mask and the alignment marks on the second mask. The samples are post baked after exposure at 100°C for 1 minute and allowed to cool down to room temperature. Development time is the same as the first mask development in RD6 developer for 10s and is then transferred to a DI

water container for 5 minutes under regular stirring and then transferred again to another DI water container for 5 more minutes under regular stirring. The samples were then blow dried with nitrogen. The samples are observed under optical microscope to see if the alignment is perfect. As we are dealing with precise placement of source-drain gap on the silicon island from the first mask (of the order of 0.1 micrometres), even a slight misalignment will get compounded and ruin the final device. If the alignment is not perfect, we rinse the samples using acetone and strip the photoresist by sonicating with acetone and isopropyl alcohol for 10 minutes each. This is followed by heating the sample again at 200°C for 20 minutes and repeating the second mask alignment procedure. If the alignment is good, we deposit 2nm Cr_2O_3 on sample C which acts as the energy filter for thermally excited electrons. We adjusted the energy filter thickness to 1nm due to the 2nm thickness causing the contact between the source-drain electrodes and the silicon surface in the island region to be poor.

3.4.7 Energy Filter: Chromium Oxide Deposition

After the second mask alignment, we need to deposit the energy filter layer for sample C. This means that Sample C has 1nm of silicon dioxide as a tunnelling barrier and a 1nm film of Cr_2O_3 as the energy filter between the source-drain electrodes and the silicon surface, which acts as the channel, in the island region. The 1 nm of Cr_2O_3 is sputtered on the Sample C using AJA sputter equipment. The sputter deposition is a two-step process. The first step is the spark step to heat up the target. The RF power is set to 64W with the pressure is set to 35mTorr. The next step is the sputter deposition. The RF power for sputtering is maintained at 148W and pressure is maintained at 5 mTorr. The sputter is carried out at room temperature. We get a thickness of 1 nm of Cr_2O_3 for a deposition time of 125s. This was calculated by depositing 10nm of Cr_2O_3 using the deposition rate of 0.01nm/s and measuring the deposited thickness using the pre-programmed refractive index in the Ocean Optics Reflectometer. Using the measured Cr_2O_3

thickness, the deposition rate for chromium oxide was recalculated to be 0.008nm/s which we used for deposition of the energy filter layer of Cr_2O_3 on subsequent samples.

3.4.8 Metal Electrode deposition for Source and Drain – Chromium Deposition

We then proceed with Chromium deposition for samples A, B and C. The deposition is done using AJA e-beam evaporator. The samples are fixed onto a sample holder using clamps. The sample holder is loaded upside down into the load lock chamber which is pumped down to a pressure of 2 x E^{-5} mTorr before the sample holder is inserted into the main chamber. The chamber pressure is maintained at 3 x E^{-7} mTorr. The sample holder is rotated at 50 rpm. The source shutter is opened along with the thickness monitor shutter. The e-beam current is slowly ramped up. The evaporation starts when the e-beam current reaches 2.5 mA. When the current reaches 2.7mA the deposition rate is stable at 1.0 Å/s. The substrate shutter is then opened, and the deposition starts. The substrate shutter and the source shutter are closed when the thickness monitor shows 1 kÅ and the current is slowly turned back down to 0 mA. The rotation is then turned off and the sample holder is unloaded into the load lock chamber. After purging the load lock chamber, the sample holder is taken out and the samples are unloaded. Before proceeding to the next step, the source and drain electrode pads need to be checked to confirm that the contact surface is conducting. Contact IV is measured for source and drain pads for all three samples A, B and C. The measured contact IV for Cr surface should be of the order of 10 μA to 0.1 mA to ensure a good conductivity.

3.4.9 Passivation Oxide Deposition – AJA Sputter

After establishing that the electrode surface is conducting the next step is to cover the metal surface with a passivation oxide layer. This is to prevent the formation of chromium oxide on the metal surface. The passivation oxide we used was silicon dioxide. It is deposited using AJA sputter equipment. The sample loading procedure is similar to AJA e-beam evaporation. Again,

the sputter deposition is a two-step process. The first step is the spark step. This is to heat up the substrate and enable easier generation of the plasma for the deposition step. For this purpose, the power is ramped up to 64W and the pressure is set to 35 mTorr. Argon flow rate is set to 30 sccm and Oxygen flow rate is 6 sccm. This step is carried out at room temperature. The next step is for deposition. Now, the power is set to 142W and the pressure is maintained at 5 mTorr. The argon and oxygen flow rates are kept the same as in the earlier step – Ar: 30 sccm, O_2: 6sccm. The sputter deposition is carried out at room temperature. Pre-sputter time is set to 120s to allow the deposition rate to stabilize. The reflected power is adjusted to as low as possible during this time ~0W to ~2W. The required thickness for the passivation oxide is 50 nm of SiO_2. The deposition rate for sputtered oxide is 0.00574 nm/s. The deposition time is calculated to be 8707 seconds. After deposition, we move on to the next step, which is lift-off.

3.4.10 Lift-off and Degassing

The lift-off process removes the photoresist from the sample surface. The photoresist while being removed takes along all the layers deposited on top of it, thereby, leaving behind the deposited layers in the source and drain electrode region as defined by second mask photolithography.

The lift-off process involves immersing the samples in acetone and sonicating them. However, it was observed under an optical microscope that this leaves behind debris on the sample. In order to avoid debris on the sample surface, the samples were held stationary upside down with a tweezer for 1 minute in acetone. We can observe the flakes falling. This is followed by vigorously shaking the sample upside down for 1 minute in a second acetone beaker. This should remove the photoresist and the layers above the photoresist without depositing them on the substrate. The samples are then rinsed using acetone squeeze bottle to remove any remaining debris. The samples are then transferred to a third acetone beaker for sonication. The samples are kept immersed in acetone and sonicated for 15 minutes. The samples are taken out

of acetone and rinsed with Isopropanol squeeze bottle before transferring them to another beaker and immersing them in Isopropanol. The samples are sonicated for another 15 minutes in isopropanol. Isopropanol is denser than acetone. It is observed that this step removes any remaining debris from the sample surface. The top surface of the electrodes is covered with sputtered silicon dioxide which is a poor-quality oxide and is porus. The sonication process might have introduced acetone inside the pores of this silicon dioxide. In order to get rid of the acetone from the pores, we need to heat the samples to 200°C, which is well above acetone boiling point. Since we are subjecting the sample to this high temperature, we need to carry out this process in an evacuated chamber. For this purpose, we used the AJA sputter equipment which had the option to heat the substrate in the evacuated environment. This process is called degassing. Any acetone present in the pores will get vaporized and pushed out of the sample surface and then evacuated using the chamber turbo pump. The samples are heated for 2 hours at 200°C in AJA sputter chamber. After the 2 hours is over, the heater is turned off. The chamber takes 1 hour and 30 minutes to cool down to room temperature. The samples are then taken out and stored for the next stage in the fabrication process.

3.4.11 PECVD Side wall and Gate Oxide deposition

The samples A, B and C now have different configuration for contact with the channel between source and drain. For Sample A, the source and drain electrodes are in direct contact with the silicon channel. For Sample B, the semiconductor channel between source and drain is separated from the source and drain electrodes with the help of 1-2 nm sputtered silicon dioxide which acts as a tunnelling barrier. For Sample C, the source and drain electrodes are separated from the silicon channel by a 1-2 nm silicon dioxide tunnelling barrier and 1 nm of chromium oxide (Cr_2O_3) which acts as the energy filter. The source and drain electrodes of the devices on the samples are separated by varying lengths of gaps in the second photomask pattern. After lift-off process, this gap which is the silicon surface of the source-drain channel is now exposed

to air. This gap acts as the gate length. We need to deposit an isolation gate oxide in this gap. We use silicon dioxide as the dielectric to separate the gate electrode from the silicon channel. In order to reduce gate leakage as much as possible the quality of the gate oxide plays an important role. For this purpose, we deposit silicon dioxide using plasma enhanced chemical vapor deposition. The thickness of the PECVD SiO_2 deposited is varied from 5 nm to 20 nm for different batches to study the effect of the varying gate oxide thickness on the gate modulation of the cold electron transistor devices.

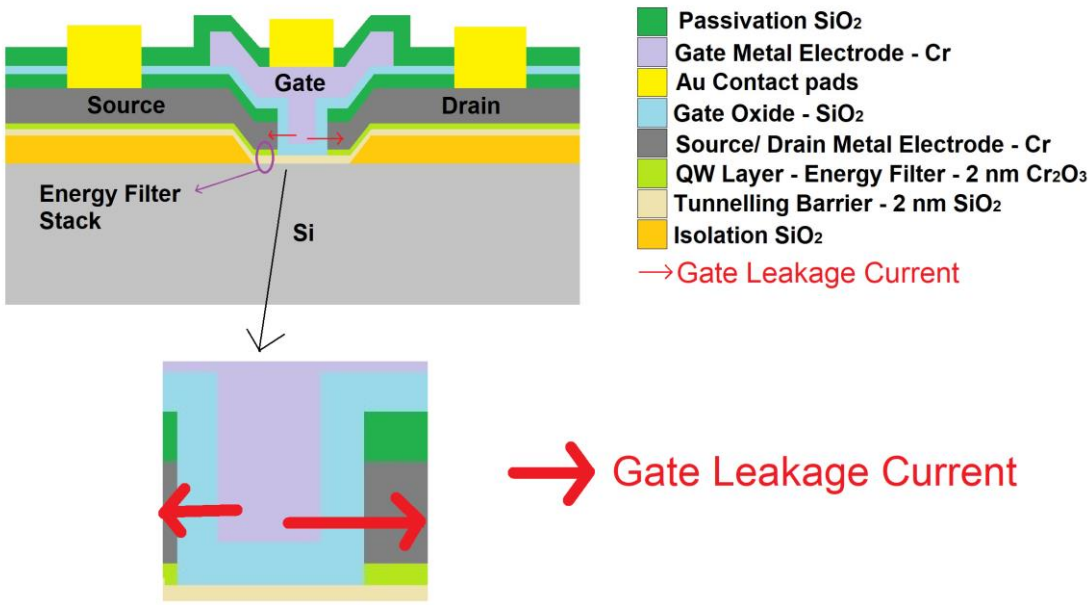

Figure 8: Schematic showing gate leakage taking place through gate dielectric between gate and source/drain electrodes

Before depositing the gate oxide, we introduced an additional step to reduce gate leakage further. This step is the PECVD SiO_2 sidewall deposition[96-99]. In this step we coat the side walls of the metal electrodes of source and drain with PECVD SiO_2. In order to achieve this, it requires a multi-step process. The sidewall thickness was required to be 50 nm SiO_2.

Before we start the process, we need to run a standard clean recipe for PECVD. The duration for the clean recipe is 3 minutes.

Next, we run a PECVD conditioning which is a nominal 50 nm SiO_2 deposition recipe on a dummy sample. The deposition is done using a three-step process. The PECVD chamber is maintained at 380°C. The samples are placed on a four-inch carrier wafer in a load lock chamber. The rest of the process is automated. The wafer is slowly inserted into the deposition chamber. Step 1 is stabilization step. The chamber pressure is maintained at 100 mTorr and is held for 1200 seconds at 380°C. Step 2 is the deposition step. Pressure is set to 1000 mTorr, Temperature is 380C and ICP power of 500W. The nominal deposition rate is 0.1618 nm/s. The deposition time is calculated using this rate for 50 nm SiO_2 which comes out to be 309 seconds. After deposition, the third step, the chamber is kept at 250 mTorr and 360C for 180 seconds before the wafer is moved into the load lock chamber. The thickness of the SiO_2 deposited is measured using Ocean Optics Reflectometer and Ellipsometer and the deposition rate is recalculated according to the deposited SiO2 thickness. If the deposition rate is close to the nominal deposition rate, the quality of the oxide deposited should be of good. We then proceed with the 50 nm SiO2 deposition for the actual samples. For this purpose, we used the recalculated deposition rate for PECVD silicon dioxide. The thickness of the oxide is measured before and after the deposition. At this point the PECVD oxide deposited is around 50 nm to 55 nm. The sidewall of the metal electrodes is inclined at an angle. Thus the vertical thickness on the sidewalls has a higher thickness than on the flat areas as PECVD deposition is conformal and is grown perpendicular to the surface of the sample features. As the inclined thickness at the sidewalls is 50 nm, the vertical thickness is much higher than 50 nm. The next step is to etch back 45 nm of silicon dioxide using Technics Reactive Ion Etching, leaving behind 5 nm of the oxide to prevent damaging the silicon surface due to RIE. The RIE etch back is done in two stages, each of which will etch nominally half the required etch thickness. Each etch stage has 2 RIE steps, the first step is carried out at 600W power and 160 mTorr chamber pressure. The gasses used for etching SiO_2 are CF_4 with a flow rate of 30 sccm and Oxygen with a flow

rate of 3.6 sccm. The etch rate was determined by running the etch recipe on multiple dummy samples with same initial silicon dioxide thickness. Different etch times were used on the different samples and the final thicknesses were measured. The data was compiled to obtain the etch rate for PECVD silicon dioxide. The recipe etches the PECVD silicon dioxide at a rate of 1.4 nm/s. The next step is an oxygen clean recipe, which is needed to remove any organic impurities redeposited on the sample after the first step. This step is carried out at 350W power and 200 mTorr. The oxygen flow rate is maintained at 11 sccm. The total etch time for 45 nm of PECVD silicon dioxide is calculated using the previously optimized etch rate. The etch time is divided into two. The first etch stage is used to etch 22.5 nm. The oxygen clean recipe time is set to 120 seconds. The thickness of the remaining silicon dioxide is measured using both reflectometer and ellipsometer. And the etch rate for the second stage is adjusted according to the etch rate obtained from the first stage. The etch time for the second stage is determined by subtracting the etched thickness from the required etch thickness and dividing it by the newly obtained etch rate. For the second stage of RIE etching, after the silicon dioxide etch recipe, the oxygen clean recipe is run for a total of 600 seconds. The slight variation in the Technics reactive ion etching etch rate from the optimized etch rate is due to the difference in chamber conditions, difference in sample size which leads to different amount of the etching gas being consumed. The variation is close to the 1.4 nm/s etch rate, thereby reducing the risk of over etching as the halved etch time helps keep the etched thickness within the 45 nm of required etch thickness.

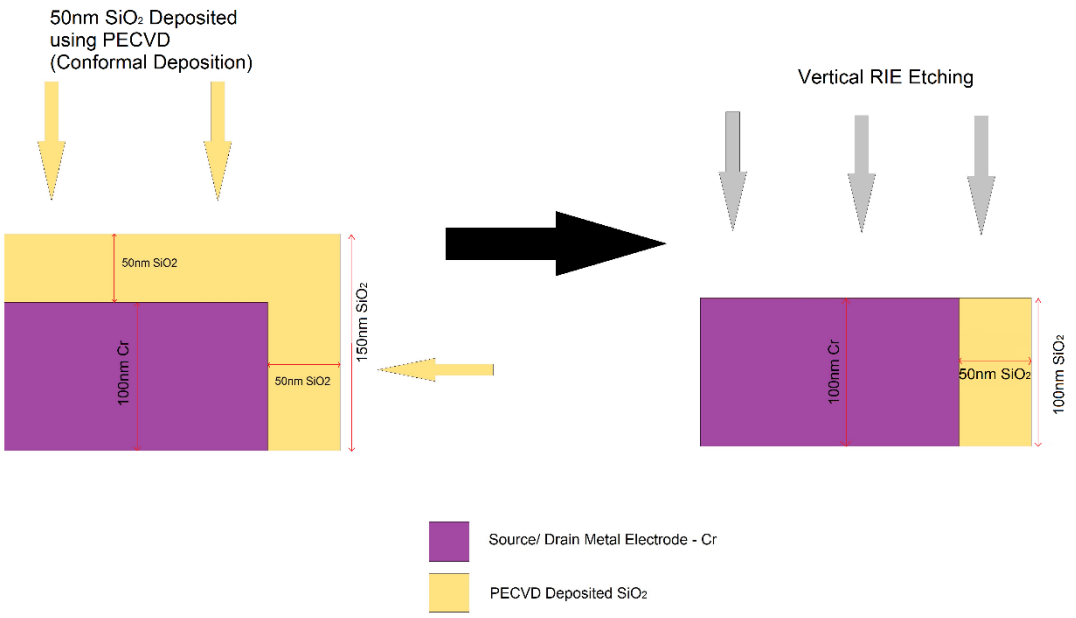

Figure 9: Schematic showing PECVD side wall deposition principle

After the two stages of reactive ion etching is completed, the thickness of the silicon dioxide remaining is measured again using reflectometer and ellipsometer. Due to the two-stage process of etching, we accurately obtain 5 nm remaining oxide in the island region. The next step is to deposit more PECVD silicon dioxide according to the requirement of the gate oxide thickness. For our purposes, we deposit from 5 nm SiO2 to 15 nm SiO2 using PECVD resulting in a gate oxide thickness of 10 nm to 20 nm. The final thickness is confirmed using reflectometer and ellipsometer measurements. The reflectometer and ellipsometer measurements are done in the centre of the samples which is clear of any devices. Once the gate oxide deposition is over and we have obtained the required gate oxide thickness, we proceed to the next stage of the fabrication process.

3.4.12 Third Mask Photolithography for Gate Electrode

The next stage of the fabrication process is the third mask photolithography in order to pattern the gate electrode on the devices. The samples are spin coated with negative tone resist – NR9-1000PY at 3000 rpm for 60 seconds. The spin coater is ramped up to 500 rpm at a rate of 100

rpm/s where it stays for 5 seconds before it is ramped up to 3000 rpm at a rate of 1000 rpm/s where it stays for 60s. This ensures an even spread of the negative resist on the entire sample. After spin coating, the samples are pre-baked at 150C for 1 minute. Now, the samples are loaded onto the OAI Aligner for photolithography. The chromium mask is oriented in such a way that the third mask pattern is approximately on top of the sample. The alignment is done using the alignment marks of the second mask pattern imprinted on the sample and the alignment marks of the third mask. The alignment needs to be accurate as the width of the gate strip needs to lie exactly above the island gap between source and drain. We have a margin of 1 μm. If the alignment is within this error margin, most of the samples will have the gate strip region above the island gap region. After alignment, the mask is pressed onto the sample using contact vacuum feature of the OAI aligner. The samples are then exposed to the UV light. The exposure intensity was optimized at 120mJ/cm^2 using dummy samples. The UV light in the aligner has an intensity of 19.7 mW/cm^2. The exposure time is set to 6.1 seconds. After exposure, the samples are post baked on a hot plate at 100C for 1 minute. After the samples are allowed to cool down, the samples are developed in RD6 developer for 10 seconds while shaking vigorously. The samples are then transferred to a DI water container, shaken vigorously, then transferred to another DI water container for 5 minutes while stirring regularly. After 5 minutes, the samples are transferred to another DI water container for 5 more minutes while stirring continuously. The samples are then blow-dried using nitrogen and observed under microscope to check whether the alignment was accurate.

3.4.13 Gate Electrode Deposition

The next step is to deposit the gate electrode metal. We use chromium as the metal electrode. 100 nm of Cr is deposited using AJA e-beam evaporator on the samples. The samples are loaded into the AJA e-beam evaporator using a load lock mechanism. The samples are fixed onto a sample holder using clamps which is inserted into the load lock chamber upside down.

The chamber is pumped down using a turbo pump to a pressure of 2 x E^{-5} mTorr before being transferred into the main deposition chamber which is maintained at a pressure of 3 x E^{-7} mTorr. The sample holder is rotated at 50 rpm. The deposition is done at room temperature at a deposition rate of 1.0 Å/s which is obtained at a e-beam current of 2.7 mA. The e-beam current is ramped up very slowly in order to avoid damaging the electronics. After deposition the samples are unloaded from the AJA e-beam evaporator.

3.4.14 Lift-off and Degassing

The lift-off process is the same as the lift-off after the second mask alignment and metal electrode deposition. The samples are held stationary upside down in acetone for 1 minute and then shaken vigorously upside down in a second beaker, after which they are transferred to a third acetone beaker. The samples are sonicated for 15 minutes in acetone. They are then taken out and rinsed with isopropanol using IPA squeeze bottle. The samples are transferred to a beaker with isopropanol and sonicated for another 15 minutes. The samples are then blow-dried with nitrogen and observed under microscope.

The samples are then loaded into AJA sputter equipment. The samples are fixed on a sample holder using clamps and loaded upside down into the load lock chamber. The load lock chamber is pumped down to a pressure of 2 x E^{-5} mTorr before being transferred to the main deposition chamber. The deposition chamber is maintained at a pressure of 3 x E^{-7} mTorr. The sample holder rotation is turned on at 50 rpm. And the substrates are gradually heated to a temperature of 200°C. The temperature is maintained at this temperature for 2 hours after which the heating is turned off. It takes 1 hour and 30 minutes for the chamber and substrate to cool down to room temperature. The samples are left inside the AJA sputter deposition chamber in order to continue with the next step.

3.4.15 AJA Sputter Oxide for Passivation Oxide deposition

Now, the next step is to deposit a passivation oxide on top of the gate metal electrode in order to prevent oxidation of the metal surface. Here we deposit 50 nm of sputtered silicon dioxide over the entire substrate to passivate the entire surface of the samples. The samples are already loaded into the AJA sputter equipment for the previous degassing step. After the deposition chamber is cooled down to room temperature, the 50 nm SiO2 deposition recipe is run. The rest of the deposition process is automated. The first step of the deposition process is the spark step. In this step, the RF power is ramped up to 64W and the pressure is maintained at 35 mTorr. Argon gas and oxygen is pumped into the chamber to generate a plasma. The flow rate of Argon is 30 sccm and for oxygen it is 6 sccm. This step is allowed to run for 60 seconds. The next step is the deposition step. The power is ramped up to 142W and the pressure is maintained at 5 mTorr. The pre-sputter time is set to 120 seconds to allow for the deposition rate of silicon dioxide to stabilize. The deposition starts after the pre-sputter time is finished. The SiO_2 deposition rate for AJA sputter is 0.00574 nm/s. The deposition time for the 50 nm silicon dioxide is 8707 seconds. After the deposition is done the samples are taken out through the load lock.

3.4.16 Fourth Mask Alignment for Gate, Source and Drain Electrode Contact Bond Pads

The next stage in the fabrication process is to create bond pads on the source, drain and gate electrodes. In order to achieve this, we need to pattern the samples with the fourth mask pattern. We use negative tone resist – NR9-1000PY and spin coat it on the samples. The samples are coated with the NR9-1000PY resist using a dropper and then spin coated in two steps at 500 rpm ramped up at 100 rpm/s for 5 seconds and at 3000 rpm which is ramped up at 1000 rpm/s. The samples are then pre-baked at 150°C for 1 minute. After cooldown, the samples are then

loaded onto the OAI aligner carrier wafer and placed in the aligner. The fourth mask is fixed onto the OAI aligner such that the fourth mask pattern is approximately situated above the sample. The alignment is done using the alignment marks of the third mask pattern on the samples and the alignment marks of the fourth mask. This alignment has a large margin of error. As long as the alignment marks are roughly aligned, the circular bond pads will lie within the source, drain and gate electrode pads. The fourth mask is then pressed onto the sample using contact vacuum and exposed to UV light. The exposure dose used was 120 mJ/cm^2. The measured intensity of the UV lamp was 19.7 mW/cm^2. The exposure time was calculated to be 6.1 seconds. After exposure, the sample is unloaded from the OAI aligner and is post baked at 100°C for 1 minute on a hot plate. The samples are allowed to cool down and are developed in a RD6 developer for 10 seconds while stirring vigorously and then transferred to a DI water container shaken vigorously, before transferring it to another DI water container and stirring regularly for 5 minutes. After 5 minutes, the samples are then transferred to another DI water container for 5 minutes while stirring regularly. The samples are taken out and blow-dried with nitrogen and observed under optical microscope.

3.4.17 Silicon Oxide Etching using Reactive Ion Etching to Expose Metal Electrode

The metal electrodes of the source, drain and gate need to be exposed in order to perform IV measurements on the cold electron transistor devices. At this stage, the source and drain metal electrodes have 50 nm silicon dioxide deposited using AJA sputter after second mask alignment, 20 nm of silicon dioxide deposited using PECVD for gate oxide deposition and 50 nm silicon dioxide deposited using AJA sputter after third mask alignment. That is, the source and drain metal electrodes have a total of 120 nm of silicon dioxide on top of it. Whereas the gate metal electrode has 20 nm silicon dioxide deposited using PECVD and 50 nm silicon dioxide deposited using AJA sputter equipment. The gate electrode has a total of 70 nm of

silicon dioxide on top of it. Thus, in order to expose the metal electrodes from the source, drain and gate electrodes, we need to etch the silicon dioxide from the electrode contact pads which were exposed after the fourth mask alignment and development.

The etching is done using Technics Reactive Ion Etching. The etch recipe consists of two steps. The first step is the SiO_2 etch using CF_4 gas with a flow rate of 30 sccm and oxygen gas with a flow rate of 3.6 sccm. The Power is fixed at 600W with a pressure of 160 mTorr. The etch rate for the thermal and PECVD grown silicon dioxide is 0.6 nm/s when photoresist is present on the sample. This is because, some of the gas present in the chamber is consumed by the photoresist thus reducing the amount of etching gas plasma available to etch the SiO_2 surface. This reduces the etch rate of PECVD SiO_2 from 1.4 nm/s to 0.6 nm/s. We need to etch a nominal thickness of 120 nm of silicon dioxide in order to expose the metal electrode under the source and drain contact pads. This will also etch the 70 nm silicon dioxide present in the gate electrode pad. The nominal etch time according to this etch rate is 200 nm/s. For the actual etch step, the CF_4 etch process is done for a total of 320 seconds to make sure that all the silicon dioxide is etched out. The next step in the etch process is the oxygen clean recipe. The power is set to 350W, with a pressure of 200 mTorr. The oxygen clean recipe is run for a total of 140 seconds. This step is necessary in order to remove the build up of organic impurities on the metal electrode surface from the photoresist being etched. Once the Reactive ion etching process is completed, the contact IV for the source, drain and gate electrodes is measured to check if the surface is conducting. If the current measured is not linear or if the current measured is too low for Chromium metal surface, then the reactive ion etching for silicon dioxide step is repeated. The IV is measured again. By this step, the contact surface of the metal electrodes should be exposed, and we should be able to see a linear current in the order of 0.1 mA.

3.4.18 Chromium and Gold Deposition for Contact Bond Pads

Now, if left exposed to air, the chromium metal electrodes will get oxidised and a layer of chromium oxide will be formed on the surface. Therefore, we need to deposit a thin layer of gold on top to prevent oxidation and keep the surface of the three electrodes conducting. For this purpose, we deposit 5 nm chromium layer followed by 10 nm layer of Au. The 5 nm chromium layer is deposited to help improve the adhesion of Au to the Cr electrodes. The deposition is done using AJA e-beam evaporator. The samples are fixed onto a sample holder using clamps and loaded upside down into the load lock chamber. The load lock chamber is pumped down to 2 x E^{-5} mTorr pressure and then the sample holder is transferred to the main deposition chamber. The Cr is deposited on the sample at a deposition rate of 0.5 Å/s when the e-beam current is 2.6 mA. After depositing 5 nm Cr, the shutter is closed and the current is ramped down to zero, the target is rotated till the Au target is in position and the current is ramped up to 2.3 mA. This achieves a deposition rate of 0.5 Å/s for Au. The shutter is opened, and deposition starts. Once the deposition is completed the shutter is closed and the current is ramped down to zero. The samples are taken out through the load lock.

3.4.19 Lift-off and Degassing

The samples are held upside down in acetone stationary for 1 minute. They are then shaken vigorously for 1 minute in a second beaker with acetone, still held upside down and are then transferred to a third beaker and immersed in acetone. The samples are sonicated for 15 minutes in acetone. After the sonication, the samples are taken out and rinsed in isopropanol with a squeeze bottle and transferred to another beaker with isopropanol. They are then sonicated in isopropanol for 10 minutes before taking them out and blow-drying them with nitrogen.

The samples are then fixed onto a sample holder using clamps and are loaded into the load lock chamber of AJA sputter equipment. The load lock chamber is pumped down to 2 x E^{-5} mTorr

and then we transfer the sample holder into the main chamber which is maintained at a pressure of 3 x E^{-7} mTorr. The sample holder rotation is turned on at 50 rpm. The heating is turned on and set to 200°C. The temperature takes 20 minutes to ramp up where it is held for 2 hours. After two hours the heating is turned off and the temperature takes 1 hour and 30 minutes to cool down to room temperature. Once the chamber temperature reaches room temperature, the sample holder is taken out through the load lock and the samples are unloaded.

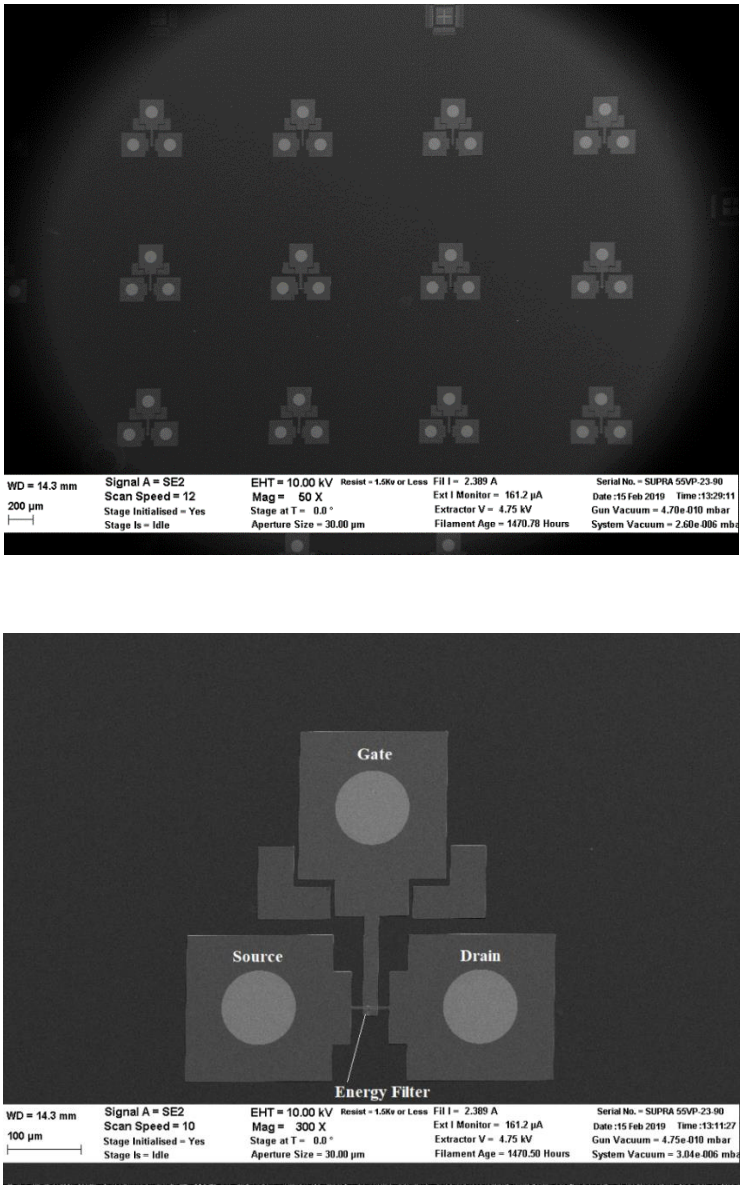

Figure 10: SEM images showing (top) CET devices array and (bottom) top view of a single device fabricated using the new mask design fabrication procedure

The cold electron transistor device fabrication is now completed, and the devices are ready for IV measurements.

Chapter 4 – Results and Discussion

4.1 Introduction

In the previous chapter we explained the fabrication procedure for the cold electron transistor devices. In this chapter we discuss the various problems that arose during fabrication procedure and how each of these issues were resolved. In addition, we also present the electrical characterization of the fabricated Cold-electron transistor devices.

4.2 Etch Rate Determination

For the 1st Mask section of the fabrication procedure, the determination of the etch rates for the thermally grown silicon dioxide plays a very important role. We need to determine the etch rates for silicon dioxide using reactive ion etching and HF etching.

Initially, the thermal oxide thickness grown was 70nm. After the first mask alignment, we needed to etch 50nm of SiO2 present in the island region. This region is exposed after the first mask alignment and development and can thus be etched using reactive ion etching. The rest of the substrate is protected from the reactive ion etching by the photoresist used during the first mask alignment. However, if we etch all the silicon dioxide in the island region the etching gasses in RIE will reach the silicon channel surface. These gasses may react with the silicon surface and damage it. Therefore, we leave a margin of 10 nm and etch the remaining SiO2 using reactive ion etching.

For this purpose, we needed to determine the etch rate for thermally grown silicon dioxide. We used three dummy samples, which have been etched using HF (10:1) for 5 minutes to remove any native oxide present on the samples. 60nm of thermal oxide was grown on these samples. These samples were then etched for different times using reactive ion etching. Dummy sample 1 was etched for 30 seconds, dummy sample 2 was etched for 60 seconds and dummy sample 3 was etched for 90 seconds. The Reactive ion etching parameters used for etching SiO2 are:

Step 1:

Power: 600 W

Pressure: 160 mTorr

CF4 gas flow: 30 sccm

O2 gas flow: 3.6 sccm

Step 2:

Power: 350 W

Pressure: 200 mTorr

O2 gas flow: 11 sccm

Etch time: 120 seconds

The remaining silicon dioxide thickness on each sample was measured using Ocean Optics Reflectometer and Ellipsometer. These thicknesses were plotted against the total etch time and the RIE etch rate for thermally grown silicon dioxide was determined to be 1.4 nm/s.

4.3 PECVD Deposition rate and Reactive Ion Etching etch rate

Another process step that requires careful attention and control is the silicon dioxide side wall formation and gate oxide deposition using plasma enhanced chemical vapor deposition. As the required gate oxide layer is very thin ~10nm, the deposition rate of the silicon dioxide using PECVD is very critical. For this purpose, we established the deposition rate using dummy samples and depositing different thicknesses using plasma enhanced chemical vapor deposition. The PECVD clean recipe was used to clean the PECVD chamber of any previously used gases. This was followed by a conditioning recipe which uses the actual deposition parameters on a dummy sample to adjust the PECVD chamber condition to optimal for the

actual deposition process. Multiple dummy samples were prepared by etching them with HF (10:1) for 5 minutes to completely etch any silicon dioxide present on the samples. The dummy samples are now bare silicon samples and can be used for the deposition rate determination. All dummy samples were approximately the same size. Each sample was deposited with silicon dioxide using PECVD with varying deposition times for each sample. The deposition parameters were as follows:

Step 1:

Temperature: 380°C

Time: 1200 seconds

N_2O: 170 sccm

Step 2:

Temperature: 380°C

Time: * seconds

N_2O: 170 sccm

Step 3:

Temperature: 360°C

Time: 180 seconds

N_2O: 170 sccm

After deposition, the samples were taken out and the deposited thicknesses were measured using ellipsometer and reflectometer. The refractive index we used is the same as the refractive index for thermally grown oxide. Both the thermally grown oxide and PECVD silicon dioxide are similar in quality and have close values of refractive index. The refractive index we use for

ellipsometer and reflectometer is 1.4571. This data was compiled in an excel sheet and the deposition rate was calculated. Below is the deposition thickness data measured using ellipsometer, arranged in a table:

Ellipsometer PECVD Growth Rate										
Time (in seconds)	0	200	227	264	285	400	530	530	530	600
Thickness	0	25.992	42.3	47.6	63.832	64.975	90.826	88.558	91.612	113.291

Table: Deposition times and corresponding deposited SiO_2 thickness measured using Ellipsometer

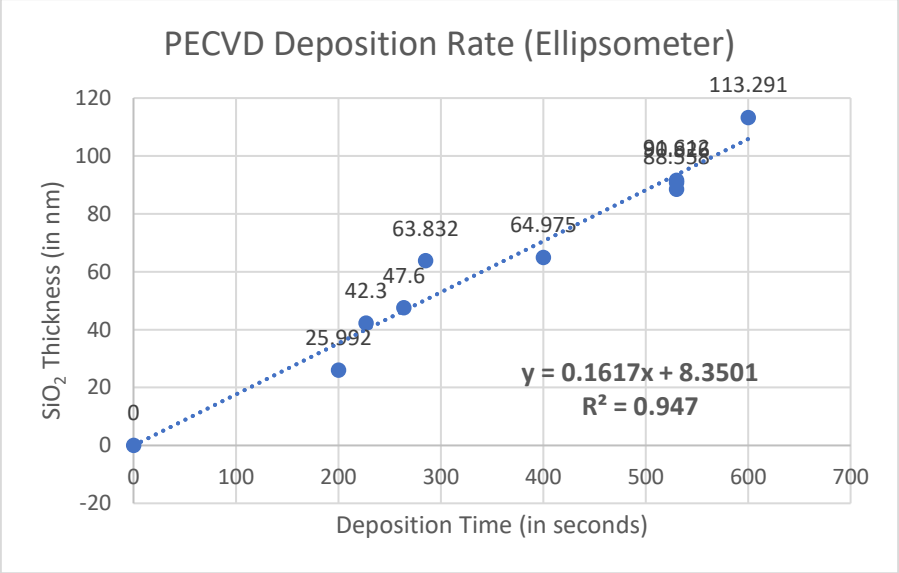

Figure 11: SiO2 Thickness deposited vs Deposition time (in seconds) measured using Ellipsometer showing deposition rate of 0.1617 nm/s

The deposition thickness data measured using reflectometer is given below:

	Reflectometer PECVD Growth Rate									
Time (in seconds)	0	200	227	264	285	400	530	530	530	600
Thickness	0	30.1	44.9	50.2	63.3	71.2	90.9	88.6	94.1	115

Table: Deposition times and corresponding deposited SiO_2 thickness measured using Reflectometer

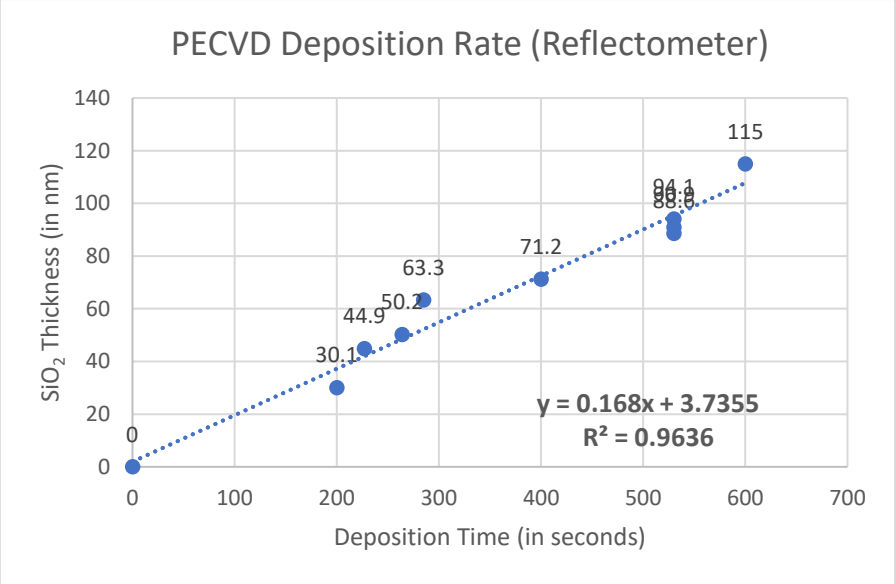

Figure 12: SiO2 Thickness deposited (in nm) vs Deposition time (in seconds) measured using Reflectometer showing deposition rate of 0.168 nm/s

Both the Ellipsometer and reflectometer data show that the measured deposition rate for the plasma enhanced chemical vapor deposition is at a stable value of 0.16 nm/s. We utilize this deposition rate for our actual samples.

Every time we use the PECVD tool, we need to run a PECVD clean recipe followed by a conditioning recipe which is the actual deposition recipe for a dummy sample. We compare the deposition rate obtained for this dummy sample with the deposition rate we have calculated. If the deposition rate is close to the calculated value, we can go ahead and use the calculated deposition rate for our actual samples.

The next step in this process is to determine the etch rate of the plasma enhanced chemical vapor deposition. The etch rate is important for the silicon dioxide side wall formation. If we over etch the silicon dioxide, this will etch away the excess silicon dioxide present on the side walls of the device structure. This will defeat the purpose of the entire side wall deposition process we have utilized here. The etch rate determination is done using the dummy samples previously deposited with the silicon dioxide using PECVD. Here, we use multiple dummy

samples deposited with the same silicon dioxide thickness using plasma enhanced chemical vapor deposition. Each dummy sample is etched using reactive ion etching with different etch times. The remaining thickness is measured using ellipsometer and reflectometer and is compiled in an excel sheet to obtain the etch rate data for plasma enhanced chemical vapor deposition. The etch rate determination data and plot for measurement using ellipsometer is shown below:

Ellipsometer				
Etch Time	20	30	40	50
Etched thickness	27.63	47.594	59.068	67.89

Table: Etch times and corresponding etched SiO_2 thickness measured using Ellipsometer

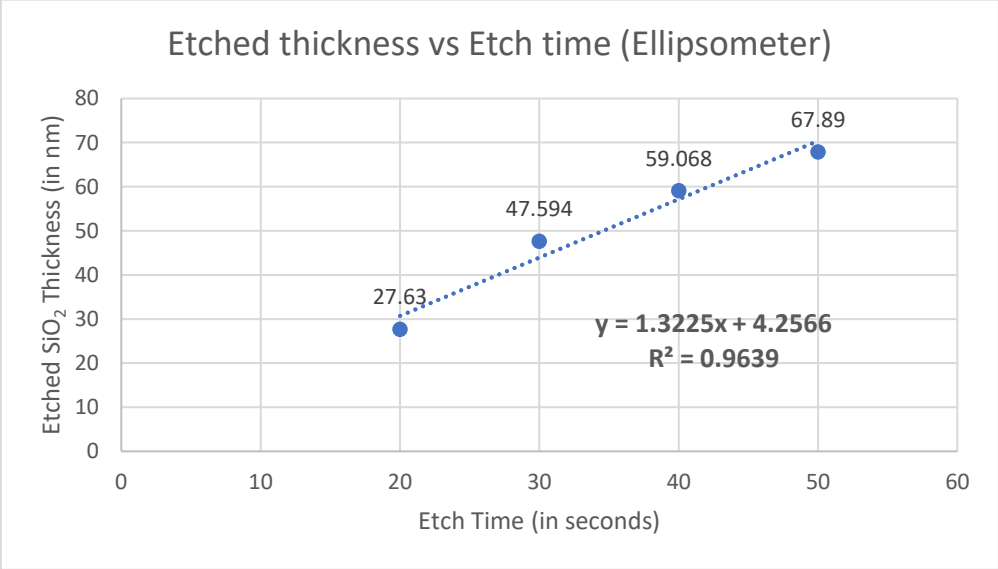

Figure 13: Etched SiO_2 thickness (in nm) vs Etch time (in seconds) measured using Ellipsometer

The etch rate determination data and plot measured using reflectometer is shown below:

Reflectometer				
Etch Time	20	30	40	50
Etched thickness	19.3	36.7	44.4	54.7

Table: Etch times and corresponding etched SiO_2 thickness measured using Reflectometer

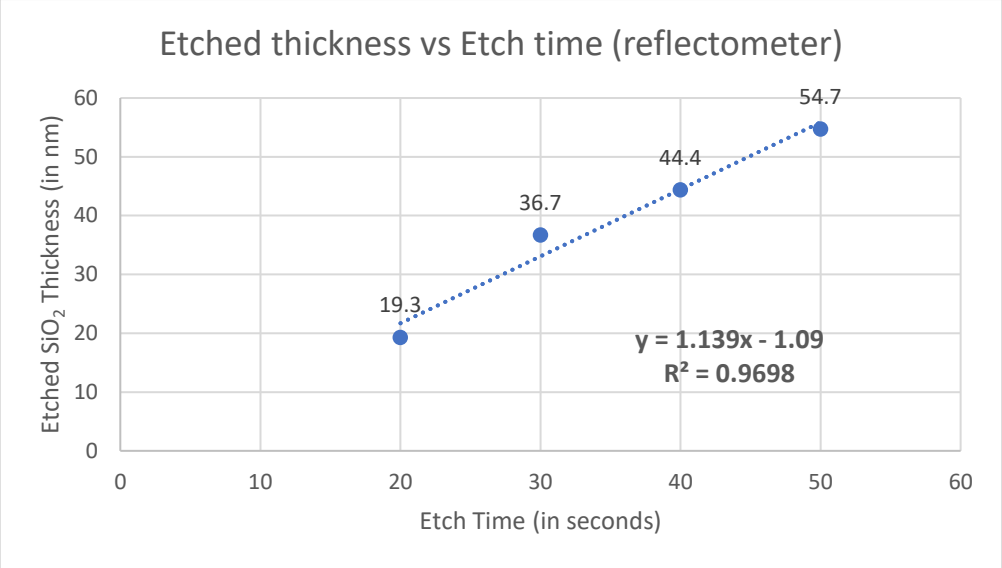

Figure 14: Etched SiO_2 thickness (in nm) vs Etch time (in seconds) measured using Reflectometer

As seen from the data above, the etched thickness measured for ellipsometer and reflectometer vary from each other slightly. The etch rate for silicon dioxide deposited using plasma enhanced chemical vapor deposition determined from ellipsometer measurements is 1.32 nm/s and that determined from reflectometer is 1.14 nm/s. This variation could be due to a variety of factors: the reflectometer incident light has a larger spot size than ellipsometer, the point of measurement might vary resulting in slight variations in thickness, the ellipsometer measurements couple to the nearest minima or maxima and if there are multiple such regions near the accurate thickness value, it might jump to a different minima or maxima and give us a slightly deviated measurement. Thus, we assume that the etch rate for the PECVD deposited silicon dioxide lies between 1.14 nm/s and 1.32 nm/s. We can then use the higher etch rate and etch half of the required etch thickness for the main samples. Using this etched thickness, we calculate the new etch rate for that sample and adjust the second etch time for the remaining amount of the required etch thickness. This helps us to reduce any error with over etching. We noticed that the sample size plays an important role in determining the etch rate for the samples. Smaller size samples show higher etch rate and larger size samples show lower etch rate. This makes the two-step etch process crucial for our purposes.

4.4 Electrical Characterization

After the device fabrication is complete, we now need to measure the IV characteristic behaviour of the devices. The electrical characterization is done using Agilent 4155C parameter analyser. The probe station setup uses 3 probes. The probes are connected to the parameter analyser using connector hub. The probes are connected to individual SMU units which are in turn connected to the parameter analyser. The IV measurements for each device are done in three steps – i. Contact IV measurements for source, drain and gate contact bond pads. ii. Source-Drain IV measurement without gate connected. iii. Gate Modulation IV measurement after connecting the gate probe to the gate contact bond pad.

Our initial measurements gave us poor contact IV, indicating that there was poor contact between the probe tips and the contact bond pads. We tried cleaning the probe tips with methanol, scratching the contact surface with the probe tips, and replacing the probe tips with new ones. The new tips worked well and gave us good contact IV for chromium metal bond pads. However, we needed to clean the probe tips after every few measurements using methanol to get good contact IV measurements. We suspected this was due to the formation of a thin chromium oxide layer ~1nm~2nm on top of chromium metal after it was left exposed to air over a period. When the probe tips came in contact with the chromium oxide layer, the tips broke through the thin layer due to the applied pressure. But, when the probes were lifted, they carried with them a coating of the chromium oxide layer. After a few repetitions of this, the tips are thoroughly coated with the chromium oxide film, thereby reducing the contact IV current readings. The Probe tips were cleaned using Methanol squeeze bottle rinsing and scrubbing the tips with a lint-free cleanroom paper. We resolved the issue of the chromium oxide layer formation by depositing chromium metal and gold layer deposition on top of the metal electrodes after the fourth mask lithography. The 5 nm chromium layer is used to improve adhesion for the 20 nm gold layer deposited on top. The gold layer helps to protect the

chromium layer beneath from oxidising. We observed that the probe tips remained clean after multiple measurements after replacing the top electrode surface with gold and the contact IV current gave a high current value in the range of 10^{-4} A.

The next electrical measurement we did for our devices was the source-drain IV. Here we touch the SMU probe tips to the source and drain contact bond pads. The source pad is maintained at a fixed potential of 0V and the drain pad is applied with a sweep pattern from 0V to 2.5V. The measurement is done using a long integration time. For Sample A measurement, the Source-Drain current behaviour should follow the characteristic behaviour of a transistor IV characteristic at 0V Gate Bias. Sample B on the other hand has tunnelling barrier present on both ends of the silicon channel. This reduces the overall current flow from source and drain. The tunnelling barrier will allow only electrons having a certain energy to tunnel through the barrier and transmit to the other terminal. Now Sample C, in addition to the tunnelling barrier has an energy filter which should lower the energy of the thermally excited electrons. Thus, we should see a much lower current flow between source and drain without applying gate bias.

The third electrical measurement for the device was to observe the gate modulation behaviour with applied increasing gate bias. The third probe tip is connected to the gate contact bond pad. The gate applied bias is increased in steps, while the source to drain sweep is carried out for each applied gate bias step. We start with varying the gate bias from 0V to 2V. If there is no leakage to gate electrode, we can slowly increase the gate bias to study the effect of increased bias on the source-drain current.

Using the initial fabrication procedure, we were able to fabricate a working transistor device for Sample B and Sample C. We observed gate modulation for the devices.

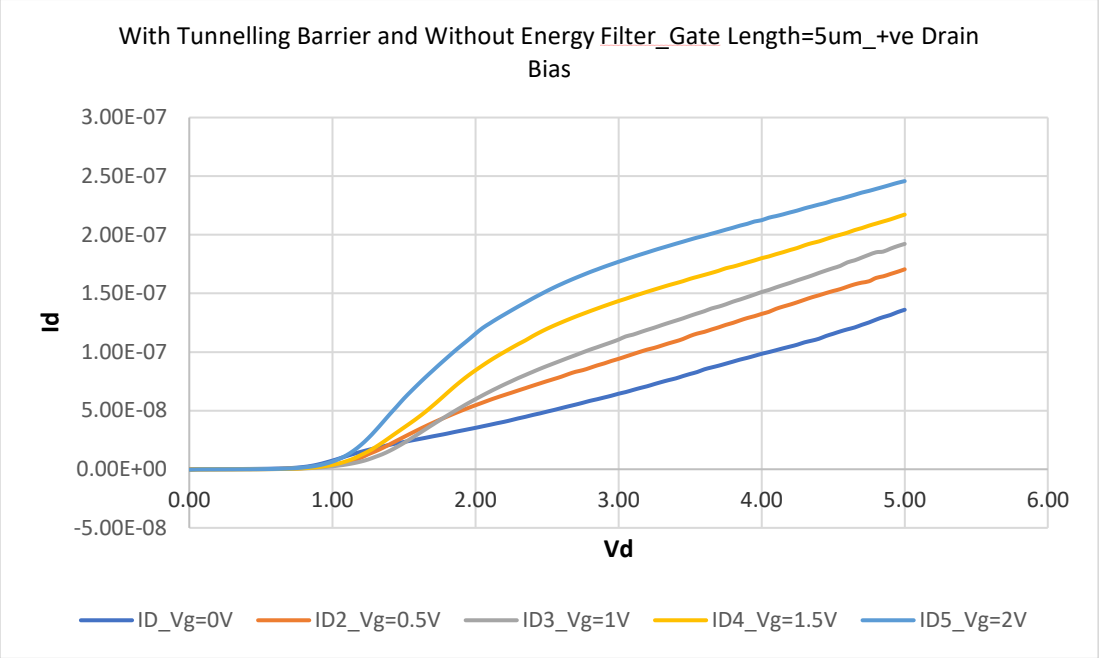

Figure 15: Demonstration of transistor behaviour - Id vs Vd for increasing applied gate bias for Device with tunnelling barrier and without energy filter

Figure 15 shows gate modulation for transistor device fabricated on sample B – with tunnelling barrier and without energy barrier. Here, the applied gate bias was varied from Vg=0V to Vg= 2V in steps of 0.5V. The IV characteristics observed in Figure 14 can be explained using the Energy band diagram in Figure 15. When we apply a positive drain bias, the fermi level of the drain electrode is lowered. Now, when there is no gate bias applied, the conduction band of the silicon channel is at a higher energy level than the source fermi level[100-102]. However, due to the thermal excitation of electrons in the source electrode, some of these thermally excited electrons have enough energy to jump over the energy barrier and tunnel through the silicon conduction band and reach the drain electrode.

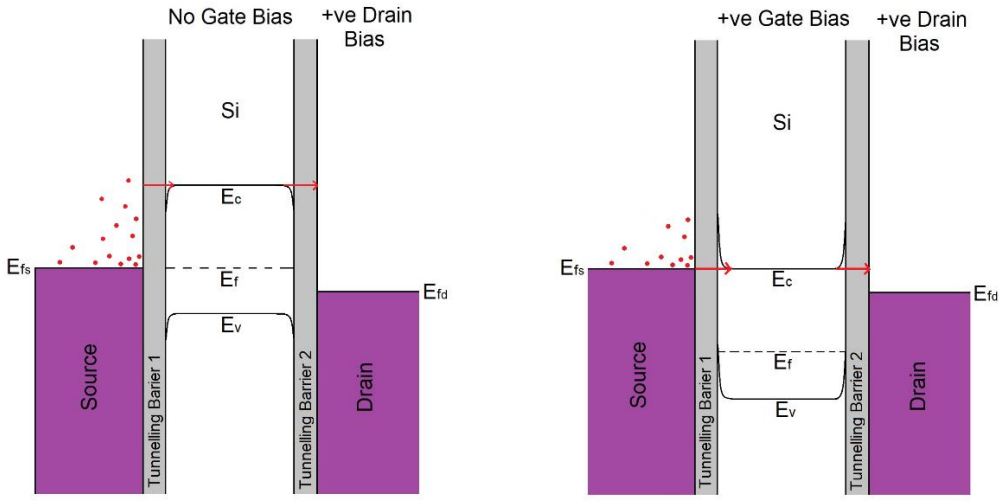

Figure 16: Energy band diagram showing mechanism of electron transfer for positive gate modulation of transistor device with positive drain bias

In addition, when a positive bias is applied to the drain, this lowers the drain electrode fermi level, which in turn pulls down the silicon channel conduction band along with it and lowering the energy barrier further. This allows the electrons from the source fermi level to tunnel into the silicon conduction band and reach the drain electrode. Thus, in the OFF state, i.e. when no gate bias is applied and a positive drain bias is applied, these two factors contribute to the source-drain current.

Now, when we apply a positive gate bias, the conduction band of the silicon is lowered. This results in the thinning of the energy barrier between the source electrode and the silicon semiconductor conduction band. The electrons from the source electrode are able to tunnel through this thinner energy barrier into the silicon conduction band and reach the drain electrode. Here, the major contribution of current is from the electrons in the source fermi level. The thermally excited electrons are also able to tunnel through the energy barrier into the silicon conduction band to the drain electrode when the conduction band is being lowered due to the applied gate bias. This leads to a gradual increase in the source-drain current resulting in a gradual subthreshold slope.

We carried out a second IV measurement for the device, but this time we applied a negative drain bias.

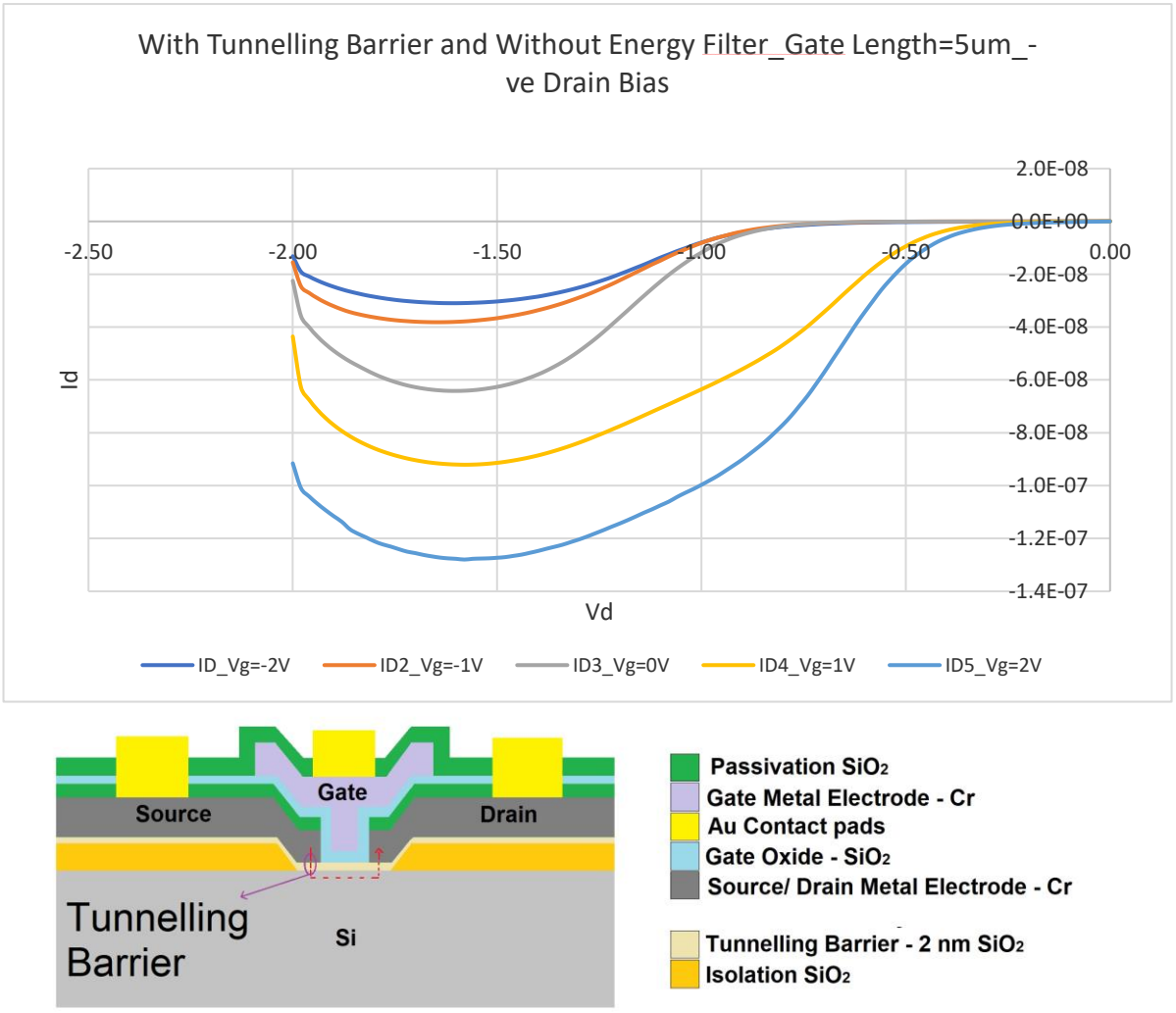

Figure 17: (top) Id vs Vd for increasing +ve applied gate bias for transistor device with tunnelling barrier and without energy filter (bottom) Device Architecture for Sample B

When a negative drain bias is applied to the drain electrode, it raises the fermi level of the drain electrode to a higher energy level. Let us consider the case when the applied drain bias is -0.5V. When there is no gate bias applied, the conduction band of the silicon channel is at a higher energy level than the fermi level of the drain electrode. However, at room temperature, due to thermal excitation of the electrons in the drain electrode, some of the electrons have

sufficient energy to jump over this energy barrier and tunnel through the silicon conduction band and reach the source electrode resulting in an OFF-state current.

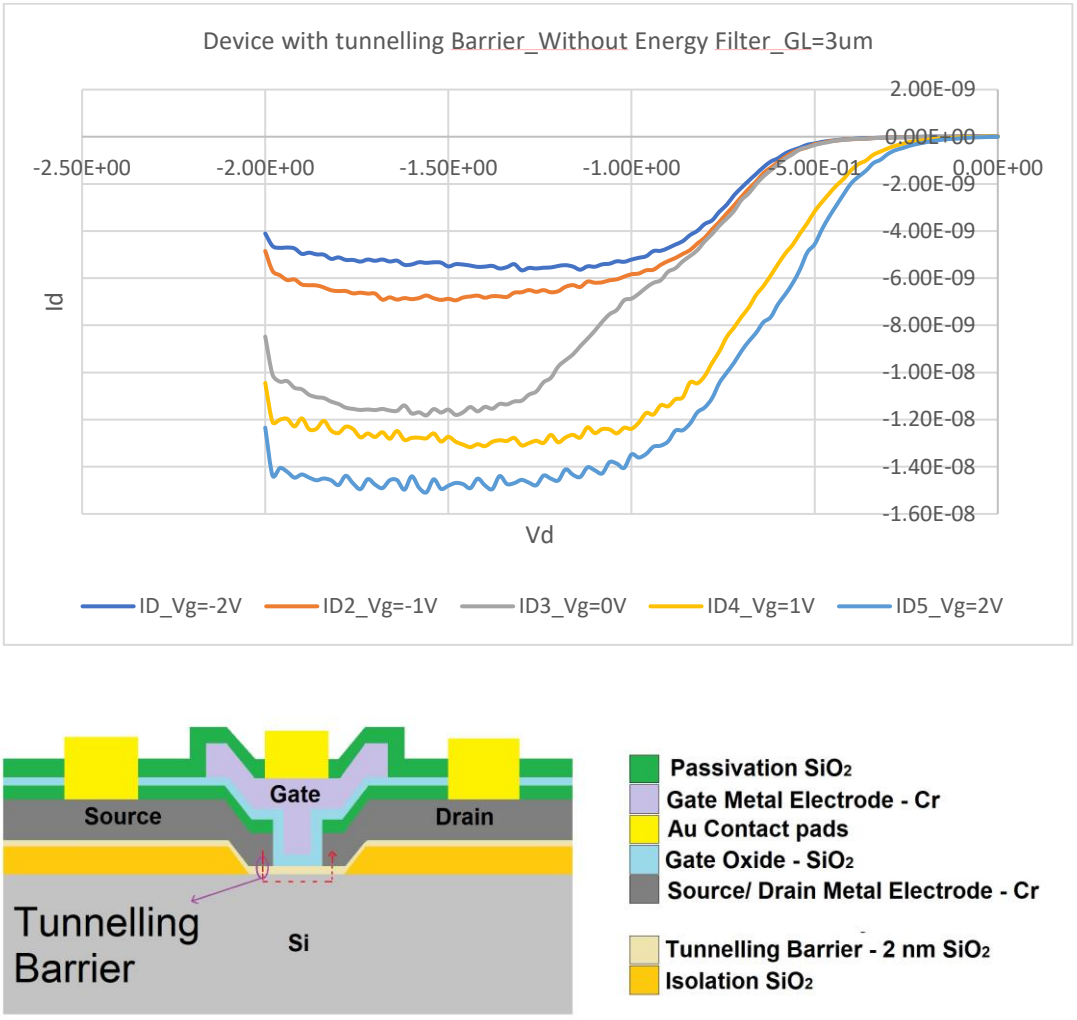

Figure 18: (top)Id vs Vd for increasing +ve applied gate bias for transistor device with tunnelling barrier and without energy filter (Bottom) Device architecture for Sample B

When a negative bias is applied to the gate electrode, this raises the conduction band of the silicon to a higher energy level. This increases the energy barrier between the Silicon conduction band and the drain electrode. In this case, some of the thermally excited electrons from the drain electrode are still able to jump over this increased energy barrier and tunnel through the silicon conduction band (Figure 18) and there is a small source-drain current.

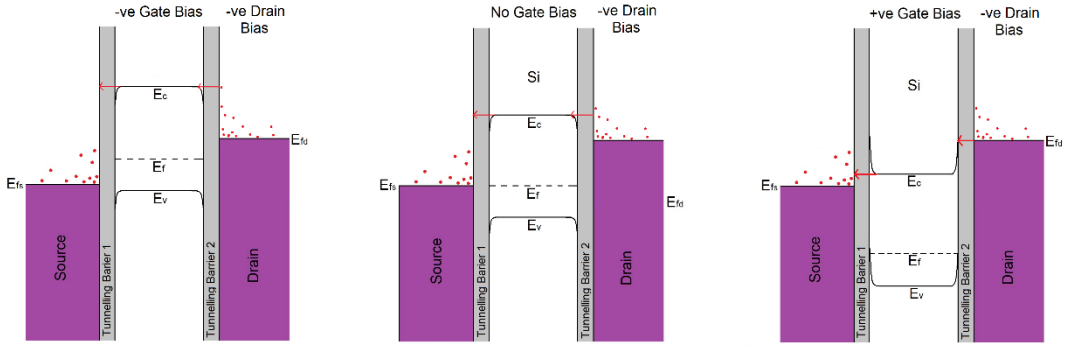

Figure 19: Energy band diagram showing mechanism of electron transfer for positive and negative gate modulation of transistor device with negative drain bias

Now, when a positive bias is applied to the gate, the silicon conduction band is lowered to a lower energy level than the drain electrode fermi level. This causes the energy barrier between the silicon conduction band and the drain electrode to become thinner. Thus, the electrons from the drain electrode fermi level are able to tunnel through this thinner energy barrier into the silicon conduction band and reach the source electrode. As the silicon conduction band is being lowered due to applied positive bias, when the energy barrier between the two is sufficiently low, the thermally excited electrons in the drain electrode now have enough energy to tunnel through to the silicon channel and reach the source electrode. These two contributing factors result in the ON-state source-drain current when a positive gate bias is applied to the gate.

We repeated the measurement a few times and the IV characteristics were consistent. The device was stable and showed gate modulation.

We observed gate modulation for the Sample C device (with tunnelling barrier and with energy filter layers) with a gate length of 3 μm as shown in figure 20. The mechanism taking place for this device is shown in figure 21.

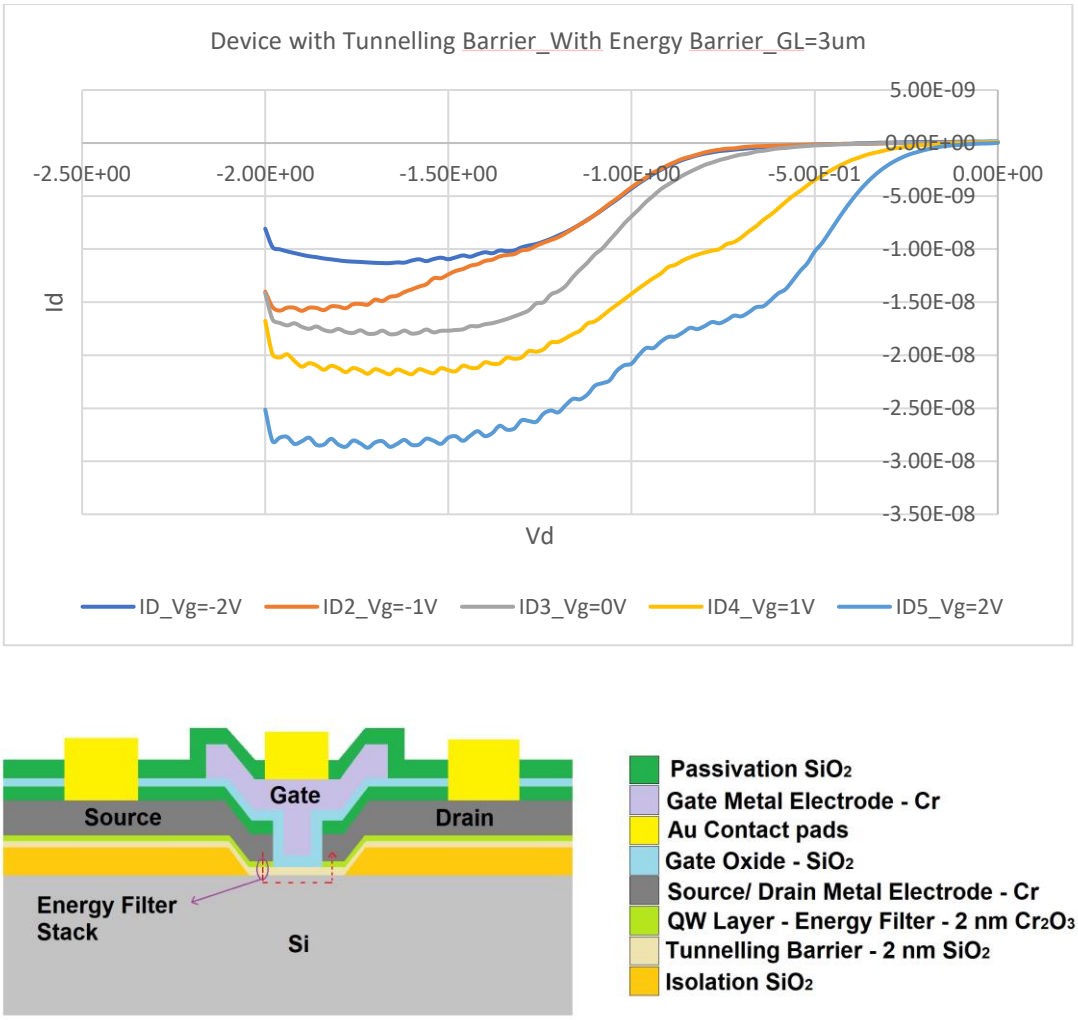

Figure 20: (top) Id vs Vd for increasing +ve applied gate bias for transistor device with tunnelling barrier and with energy filter (bottom) Device architecture for Sample C

A negative bias is applied to the drain. This raises the fermi level of the drain electrode to a higher energy level. The drain electrode and the conduction band of the silicon channel is separated by a 2 nm layer of Cr_2O_3 which acts as the energy filter and a 2 nm layer of silicon dioxide which is the tunnelling barrier. When there is no Bias applied to the gate and a negative bias of -0.5V is applied to the drain electrode, the electrons from the fermi level of the drain electrode and the thermally excited electrons in the drain electrode upon entering the quantum well layer of the energy filter (2 nm Cr_2O_3) occupy the closest discrete energy level of the quantum well.

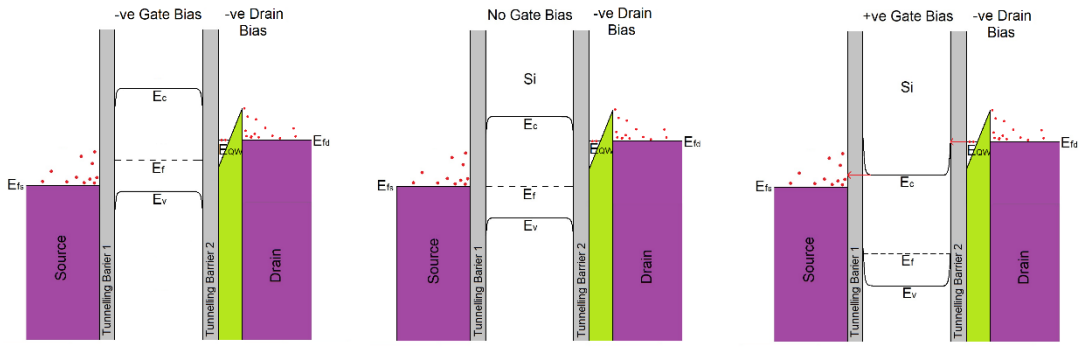

Figure 21: Energy band diagram showing mechanism of electron transfer for positive and negative gate modulation of transistor device for negative drain bias with tunnelling barrier and energy filter

Now, inside the quantum well discrete energy level the electrons no longer have a path to jump to a higher energy level. The room temperature thermal energy is not enough for the electrons to jump to an adjacent discrete energy level due to the significantly larger energy gap between these discrete energy levels. Thus, when there is no gate bias applied, the conduction band is at a higher energy level than the quantum well discrete energy state. As there is no path available for the thermal excitation of the electrons, there will be no electron transfer from the quantum well discrete energy level to the conduction band of silicon channel and there will be no current flow.

When we apply a negative bias to the gate electrode, the conduction band of the silicon is raised to a higher energy level. As the energy level of the conduction band is at a higher energy than the discrete energy level of the quantum well, the electrons in the discrete energy level cannot tunnel through the conduction band of the silicon channel leading to no source-drain current for negative gate bias at -0.5V bias for drain electrode. Now, when a positive bias is applied to the gate electrode, the conduction band of the silicon channel will be lowered. As long as the conduction band energy level is still above the discrete energy level of the quantum well, there will be no electron transfer. However, when the positive bias applied to the gate is sufficient to lower the conduction band of the silicon channel to the same energy level or to a lower energy

level than that of the discrete energy state of the quantum well, the electrons from the discrete energy level of the quantum well can now tunnel through the silicon conduction band and reach the source electrode. Thus, we have a source-drain current for the ON state. As there are no thermally excited electrons tunnelling through when the conduction band is being lowered, the subthreshold slope will not be gradual. Instead, due to the sudden flow of current when the silicon conduction band and the discrete energy level are aligned, the subthreshold slope will be steeper than when there is no discrete energy level present, i.e. when there is no quantum well layer present in the device architecture.

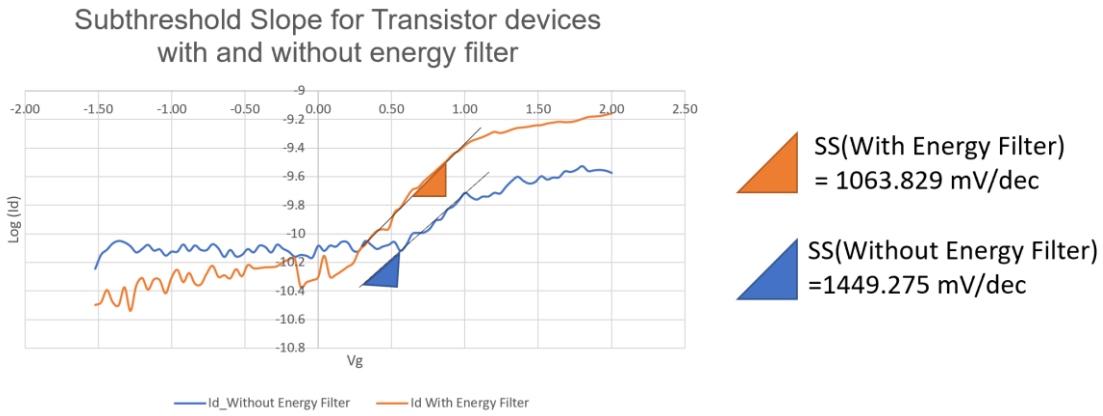

Figure 22: Subthreshold slope variation for transistor devices with tunnelling barriers and with and without energy filter architecture

The subthreshold slopes of the devices in sample B (with tunnelling barrier and without the quantum well energy filter) and sample C (with tunnelling barrier and with the quantum well energy filter) were measured and plotted as shown in Figure 22. An increase in the steepness of the subthreshold slope was observed for the device with energy filter architecture. The subthreshold slope measured for the device without energy filter was measured to be 1449.275 mV/dec and the subthreshold slope for the device with energy filter was measured to be 1063.829 mV/dec.

SS (Without Energy Filter)	*SS (With Energy Filter)*
1449.275	*1063.829*

Table: Shows subthreshold slope for transistor devices with and without energy filter

At this stage, we only have this single set of data to corroborate the increase in the steepness of the subthreshold slope. A large percentage of the devices fabricated on the samples did not survive the fabrication procedure due to large gate leakage between the gate electrode and the source/drain electrodes (Figure 23).

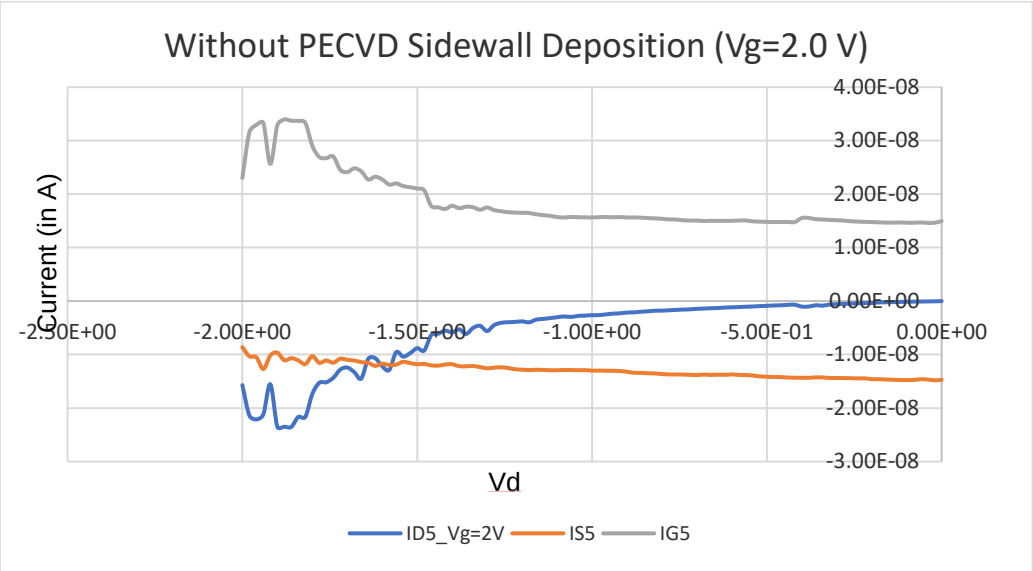

Figure 23: Source, Drain and Gate current comparison vs drain voltage for an applied Gate Bias, Vg= 2V

The gate leakage current measured for this device was of the order of 10^{-8} A. After we resolved the gate leakage issue, the devices were fabricated again using the new fabrication process and the PECVD sidewall deposition for thicker isolation between the gate and source/drain electrodes. This significantly reduced the gate leakage problem with the devices. The source drain and gate current for the fabricated device was measured (Figure 24).

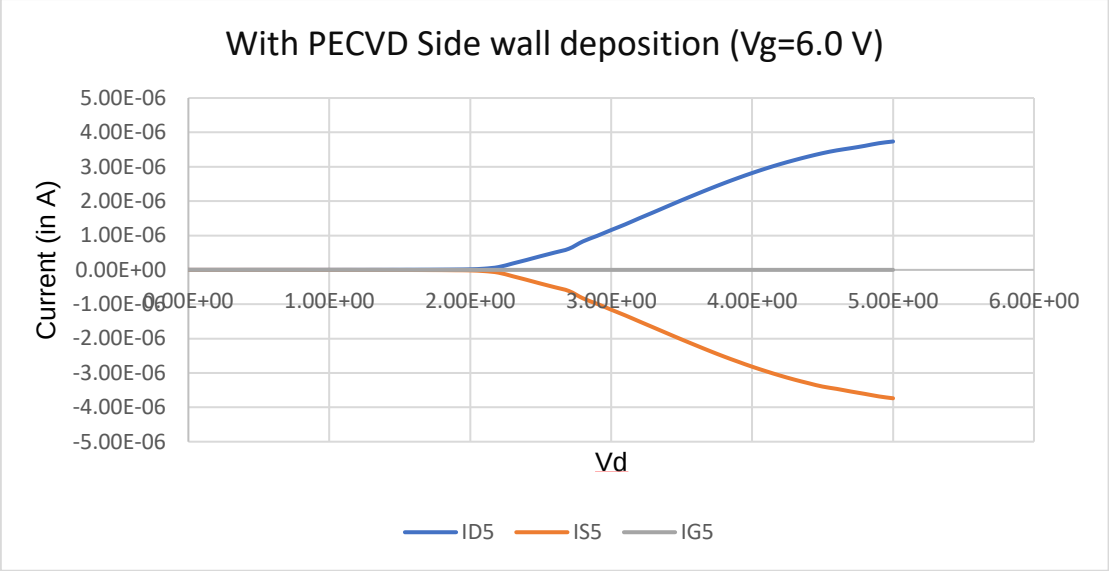

Figure 24: Source, Drain and Gate Current comparison vs drain voltage for an applied Gate Bias, Vg= 6V

The device showed very low gate leakage of the order of 10^{-11} A to 10^{-13} A even with a gate bias of 6V. The comparison of source, drain and gate currents was done for samples with tunnelling barrier and without energy filter architecture.

We observed transistor behaviour for device fabricated using the new design fabrication procedure. Figure 25 shows positive and negative gate modulation for a device fabricated on sample B (With tunnelling Barrier and without energy filter architecture). This device was fabricated on p-type silicon wafer lightly doped with n-type phosphorous dopant. The n-type doping raises the fermi level of the silicon close to the conduction band. The energy band diagram shows the mechanism for electron transfer taking place for this device.

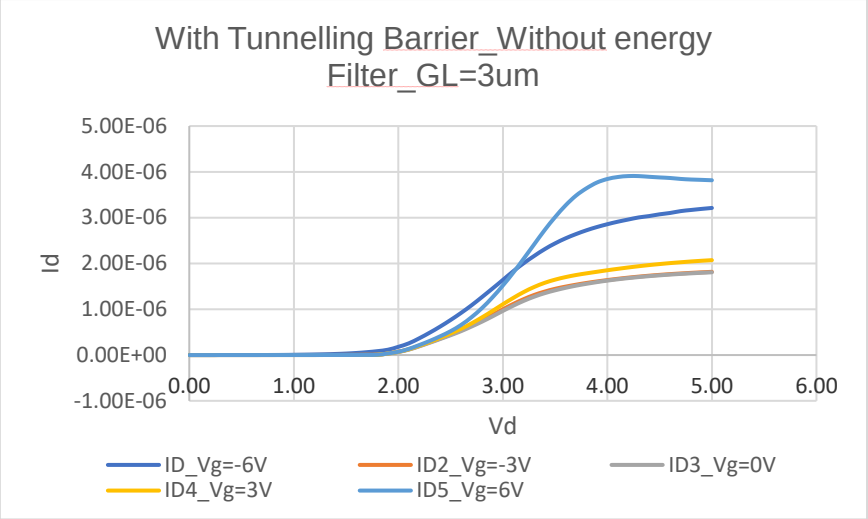

Figure 25: Demonstration of transistor behaviour - Id vs Vg plot for transistor device fabricated using new mask design fabrication process. Device architecture consists of tunnelling barrier without energy filter. Device is lightly doped with N-type dopant

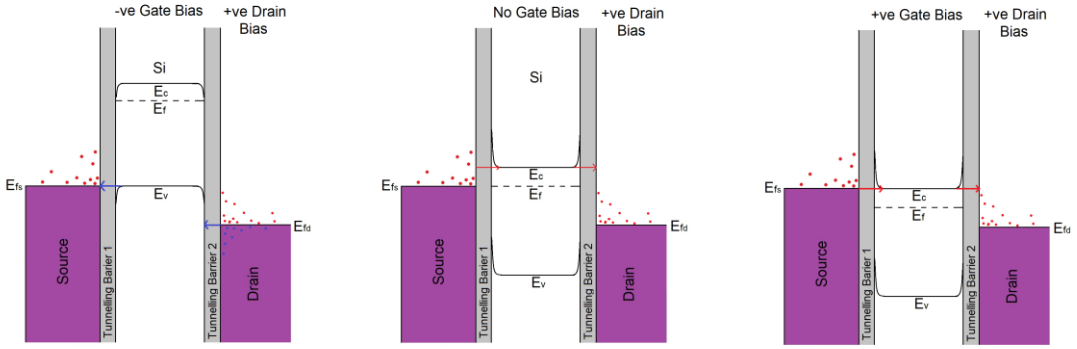

Figure 26: Energy band diagram showing mechanism for electron transfer for positive and negative gate modulation of transistor device for positive drain bias with tunnelling barrier and without energy filter

When no gate bias is applied, the fermi level of the silicon is aligned with the source electrode fermi level. A positive bias is applied to the drain electrode which lowers the drain fermi level to a lower energy than the source electrode fermi level. When the drain fermi level is lowered, it pulls the silicon energy bands along with it. Due to the n-type doping, the fermi level of silicon is close to the conduction band.

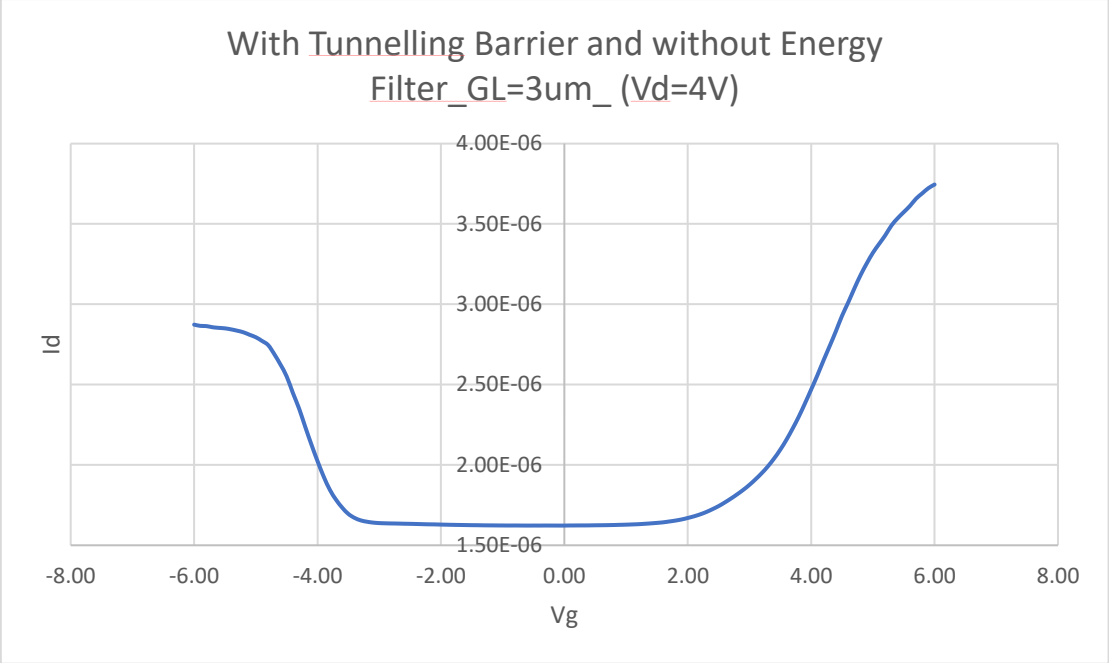

Figure 27: Drain current as a function of the Gate Voltage bias for Sample B device with tunnelling barrier and without energy filter and gate length of 3 μm

When no bias is applied to the gate, the conduction band of silicon is close to the source electrode fermi level, i.e. the energy barrier between the source electrode fermi level and the silicon conduction band is lowered. This means that the thermally excited electrons from the source electrode have sufficient energy to jump over this energy barrier and tunnel through the silicon conduction band to reach the drain electrode and we can observe a source-drain current.

When a positive bias is applied to the gate electrode, this further lowers the conduction band energy level causing the energy barrier between the source and silicon conduction band even thinner. Electrons from the source fermi level and the thermally excited electrons from the source electrode are able to tunnel through this thinned energy barrier into the silicon conduction band and reach the drain electrode. Both these factors contribute to the ON-state current.

When a negative bias is applied to the gate, this raises the conduction band of the silicon channel to above the source fermi level. When sufficient negative bias is applied, this energy

barrier between the source fermi level and the conduction band is large enough that thermally excited electrons from source are unable to overcome this energy barrier. However, when the conduction band of the silicon is raised to a higher energy level due to the negative gate bias, it also raises the valence band of the silicon channel. When this valence band is raised to an energy above the energy level of the drain fermi level, the holes from the drain electrode close to the drain fermi level are able to tunnel through the energy barrier between the valence band of silicon and the drain fermi level. These holes from the drain electrode tunnel through the silicon valence band and reach the source electrode and we have a source-drain current.

We varied the contact area between the source/drain electrodes and the silicon channel for our subsequent measurements. Contact area is the section of the source/drain electrode that is responsible for electron transfer between the source/drain electrode and the silicon channel. These measurements were done for sample B devices (with tunnelling barrier and without energy filter).

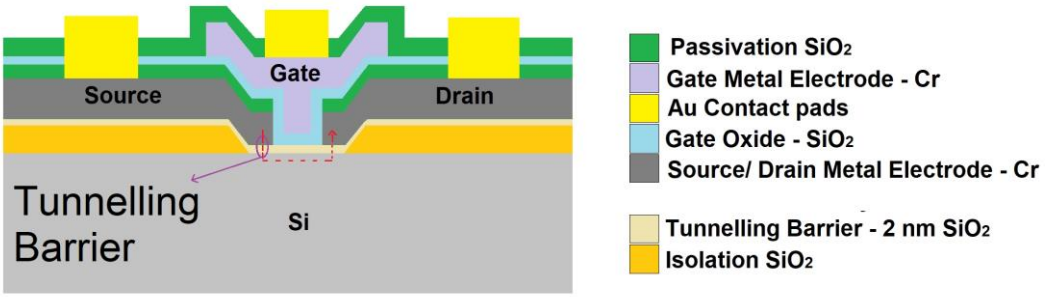

Figure 28: Device architecture for Sample B with tunnelling barrier and without energy filter layer

The measurement showed an increase in the source-drain current for an increase in the contact area for these devices as shown in Figure 29-30. We measured two sets of data in different regions on the same sample and both sets of devices showed a consistent increase in the source-drain current with increasing contact area.

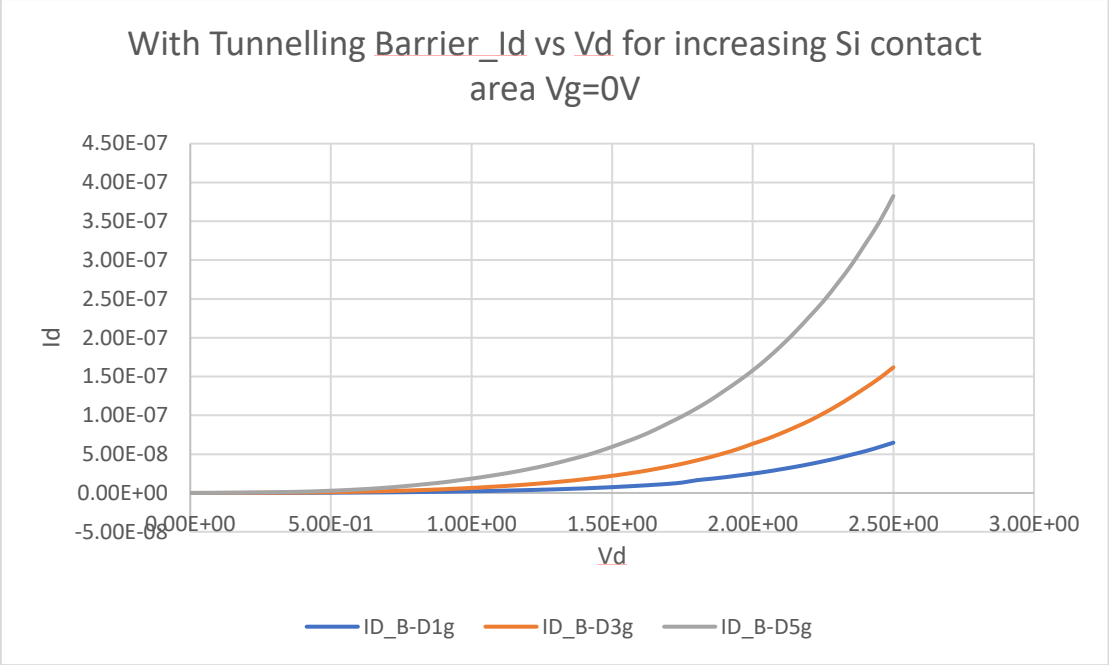

Figure 29: Increasing contact area source-drain IV measurements for transistor devices with tunnelling Barrier in region D of Sample B. Region D of the sample has a high width gate electrode covering

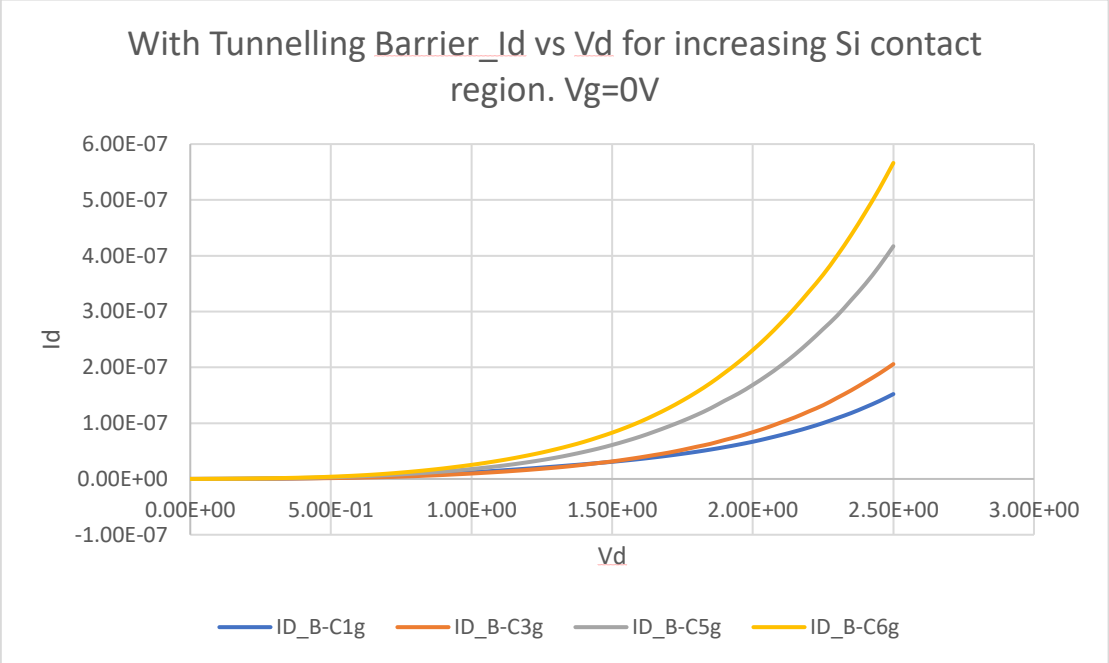

Figure 30: Increasing contact area source-drain IV measurements for transistor devices with tunnelling Barrier in region C of Sample B. Region C of the sample has lower width of gate electrode covering

Another experiment we performed was to study the effect of gate length on the subthreshold slope for these transistor devices. IV measurements (Figure 29) were done for devices with decreasing gate length of 5 μm, 3 μm and 2 μm. The subthreshold slopes for these devices were plotted and compared. The measurements showed that there was an increase in the subthreshold slope value with increasing gate length, i.e. with decreasing gate length there was an increase in the steepness of the subthteshold slope for these devices. The subthreshold slope depends on the temperature and the gate capacitance. We suspect that the decreasing gate length may be resulting in a more effective gate coupling, which in turn leads to an increase in the steepness of the subthreshold slope for these devices.

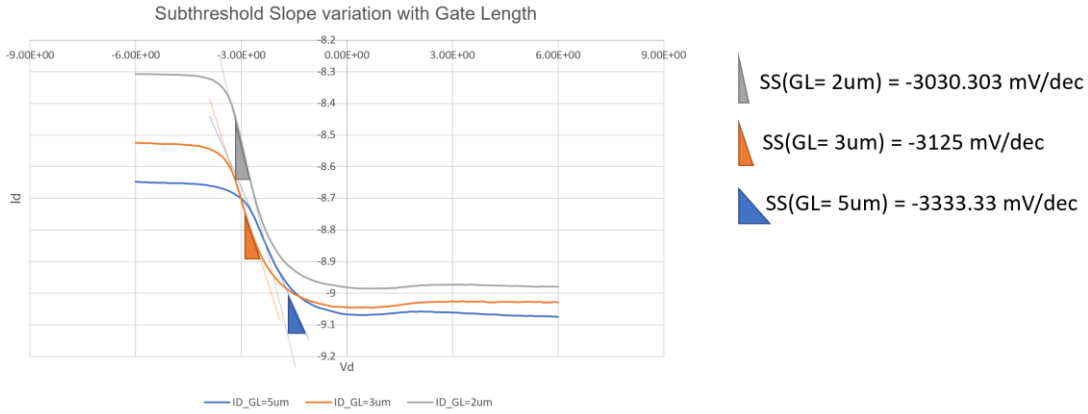

Figure 31: Subthreshold slope variation for devices with tunnelling barrier and without energy filter architecture for decreasing gate length

SS_GL=5um	*SS_GL=3um*	*SS_GL=2um*
-3333.333333	*-3125*	*-3030.30303*

Table: Subthreshold slope variation with decreasing Gate Length

At this stage, we have only one set of data to corroborate this gate length dependence of the subthreshold slope. Further IV measurements for additional fabricated devices will be needed to verify this result.

Chapter 5 – Conclusion

In this work, the method and materials for the fabrication of transistors with an energy filter layer stack for suppressing thermal excitation of electrons have been established. The fabrication procedure was optimized, transistors were successfully fabricated, and their gate modulations were observed. An increase in the subthreshold slope steepness was observed for a device with energy filter architecture when compared with device without the energy filter. The measured subthreshold slopes were 1449.275 mV/decade and 1063.829 mV/decade for transistors without and with the energy filter, respectively. The increase of subthreshold slope steepness indicates that the energy filtering structure plays a role, although it needs further verifications. A faster fabrication procedure was developed, reducing the fabrication time from one month to one week. The source-drain current for devices with increasing contact area between source-drain electrodes and the silicon channel was compared. There was an increase in the source-drain current with an increase in source/drain and silicon channel contact area. Also, the subthreshold slope variation was measured for devices with decreasing gate length. The subthreshold slopes were measured to be -3333.33 mV/dec, -3125 mV/dec and -3030.3 mV/dec for gate length of 5 μm, 3 μm and 2 μm, respectively. The reason for the increase in subthreshold slope steepness with the decrease in gate length could be the improved gate coupling, thereby resulting in an increase in the steepness of the subthreshold slope. Due to not-yet optimized gate coupling, the absolute values of the subthreshold slope for these devices were significantly higher than those of the current advanced MOSFETs. Further research will be focused on enhancing the gate coupling and enhancing the energy suppression in the devices, thereby obtaining a steeper subthreshold slope.

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