RELIABILITY OF A 2.5D TSV PACKAGE

by

NEHA VINAYAK GAIKWAD

Presented to the Faculty of the Graduate School of

The University of Texas at Arlington in Partial Fulfillment

of the Requirements

for the Degree of

MASTER OF SCIENCE IN MECHANICAL ENGINEERING

THE UNIVERSITY OF TEXAS AT ARLINGTON

May 2018

Copyright © by Neha Vinayak Gaikwad 2018

All Rights Reserved

Acknowledgements

I would like to thank the Almighty and my parents whose immense love and encouragement keeps me to perform better in life always. I would like to thank Dr. Agonafer to give me the opportunity to research in his EMNSPC team. His guidance and support motivated me throughout my research.

I thank Mr. Pavan Rajmane for guiding me to perform this research. I also thank Dr. Abdolhossein Haji-Sheikh and Dr. Fahad Mirza.

Last but not the least, I also thank Dr. Ratan Kumar, Wendy Ryan and my friends for their support throughout my graduate program at the university.

May 3, 2018

Abstract

RELIABILITY OF A 2.5D TSV PACKAGE

Neha Vinayak Gaikwad, MS

The University of Texas at Arlington, 2018

Supervising Professor: Dereje Agonafer

In the recent years, the Through Silicon Vias (TSVs) are helping a huge variety of the 3D IC and the 2.5D IC packaging applications to try to fulfill their requirements of functionality and higher connectivity at the expense of lower power consumption and minimum heat dissipation. The TSVs offer great interconnect density, high device density, short connection paths, great space efficiency and high interconnect bandwidth. The basic difference between a 3D TSV package and a 2.5D TSV package is that the 2.5D one interconnects the dies side by side on a silicon interposer, over its entire length. The interposer, placed between the package substrate and the dies consists of the TSVs that are the interconnections between the top and bottom layers, whereas the 3D one interconnects the dies one above the other, i.e. on the top of each other. In this, the TSVs are present in the die at the bottom, which is just above the package substrate. Apart from the various advantages of the TSVs, the challenges associated with them are higher utilization of the manufacturing area and thus they ultimately result in the position barriers by securing an entire layer. Also the metal degradation impact on them, their failure due to the environmental stresses induced in them and the overall impact of these on the entire package are also some of the challenges in TSVs, which question the reliability of the packages. In this research, a 2.5D TSV package was subjected to a thermal cycling test to investigate its reliability. For that, at first a detailed model of a 2.5D IC package is

created and analyzed in ANSYS 18.0. But considering its huge number of elements and higher computational time, the compact modeling technique is implemented on it. The compact model is then subjected to thermal cycling and the output parameter thus obtained for it is compared and validated to that obtained for the detailed model.

Table of Contents

Acknowledgements ... iii

Abstract ... iv

List of Illustrations ... vii

List of Tables ... viii

Chapter 1 Introduction ... 1

1.1. Essentials of the Electronic Packaging ... 1

1.2. 3D and 2.5D packages ... 2

1.3. Through Silicon Vias in 3D/2.5D packages ... 4

Chapter 2 Recent Trends in 2.5D packaging ... 6

2.1. 2.5D Packaging in the IC Industry ... 6

2.2. The 2.5D Packaging Solutions ... 8

Chapter 3 Model Description ... 10

Chapter 4 Compact Modeling Technique ... 15

Chapter 5 Results and Discussion ... 17

Chapter 6 Conclusion ... 21

6.1. Concluding Remarks ... 21

6.2. Future Work ... 21

References ... 22

Biographical Information ... 24

List of Illustrations

Figure 1-1 Levels of Electronic Packaging.......... 2

Figure 1-2 A 2.5D and a 3D package 3

Figure 1-3 TSVs in an FPGA package.......... 4

Figure 1-4 TSVs in a DRAM device 5

Figure 2-1 The 2.5D Packaging and HBM 6

Figure 2-2 A 2.5D packaging solution 8

Figure 2-3 Fan-out wafer-level-packaging 9

Figure 3-1 Cross section of the detailed model of the 2.5D TSV package 11

Figure 3-2 Octal model.......... 12

Figure 3-3 Meshing done on the octal model 12

Figure 4-1 Cross section of the compact model 16

Figure 4-2 Meshing done on the compact model 16

Figure 5-1 Thermal cycling analysis on the detailed model 17

Figure 5-2 The total deformation on the detailed model 17

Figure 5-3 Thermal cycling analysis on the compact model 18

Figure 5-4 The total deformation on the compact model 19

List of Tables

Table 3-1 Anand's Constants for the solder SAC 305 13

Table 3-2 Anand's Constants for the Effective Block in the Compact Model 14

Table 5-1 The total deformation values at different time intervals 18

Table 5-2 : Comparison and validation of the total deformation for both the models……19

Chapter 1

Introduction

1.1. Essentials of the Electronic Packaging

Electronic Packaging is one of the crucial pursuits to manufacture the microsystems like the MEMS, RF switches, sensors, actuators, accelerometers, optoisolators, biomedical instruments, microscanners etc. Basically, electronic packaging serves the purpose of interconnecting the various chips, integrated circuits and other constituents to form an electronic system [11]. The essence of electronic packaging is that it is multidisciplinary. It is surrounded by various fields like physics, chemistry, electrical engineering, electronics, mechanical engineering etc. A fabricated die or an entire electronic system works well if it is produced by an appropriate packaging methodology. There are three levels in packaging viz., chip level, board level and system level [12].

Chip Level Packaging: This is the lowest packaging level amongst all three. It consists of stages and operations to hold the bare die properly so as to package it on the boards, etc. This is done as it is not possible to directly use the bare dies in practice. However, now we can use the bare dies directly in a particular electronic system.

Board Level Packaging: In this level, to perform the system level operations, the bare dies held and packaged in the chip level packaging are installed and assembled together on the system level boards.

System Level Packaging: It is the level of packaging in which the other two levels are incorporated together to initiate an electronic system to carry out a particular task according to the demand of the user.

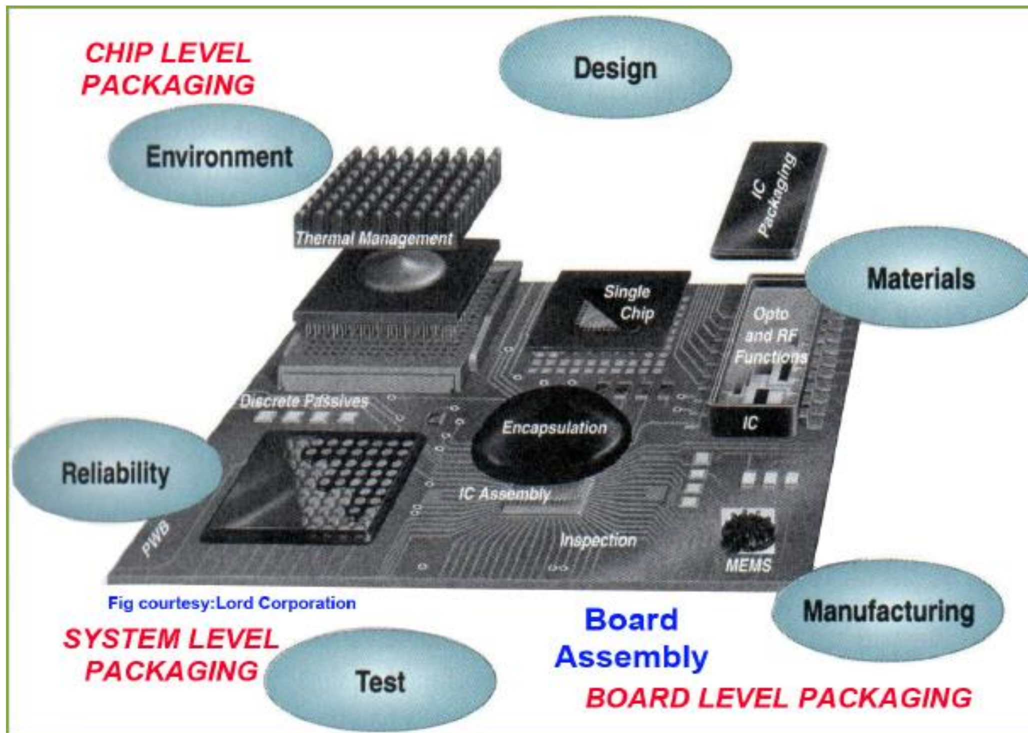

Figure 1-1: Levels of Electronic Packaging [13]

As the customers demand for a high performance, low cost and a portable electronic device, it has always been a serious concern to retain the stability of these three factors while doing the electronic packaging. Thus, it is necessary to have a systematic compromise between these factors to produce an ideal product. Along with the miniaturization, the evaluation and the reliability of the product is also crucial so that the product performs well at all the time under different sets of conditions throughout its life span.

1.2. 3D and 2.5D packages

3D packaging is being implemented in the electronics industry since many years. The Package-on-Package and Package-in-Package are two of the many types of 3D packages which do not completely satisfy the product requirements of performance, power and form factor of true 3D ICs. One of the additions of the 3D package notion into

integrated circuits is to add a silicon interposer (which includes TSVs that connect the upper metal layers to the lower ones) in between the package substrate and the dies to give finer interconnections which ultimately raises the performance and reduces the power consumption. This approach is termed as 2.5D packaging. The figure 1-2 illustrates the concept of a 2.5D and a 3D package in ICs.

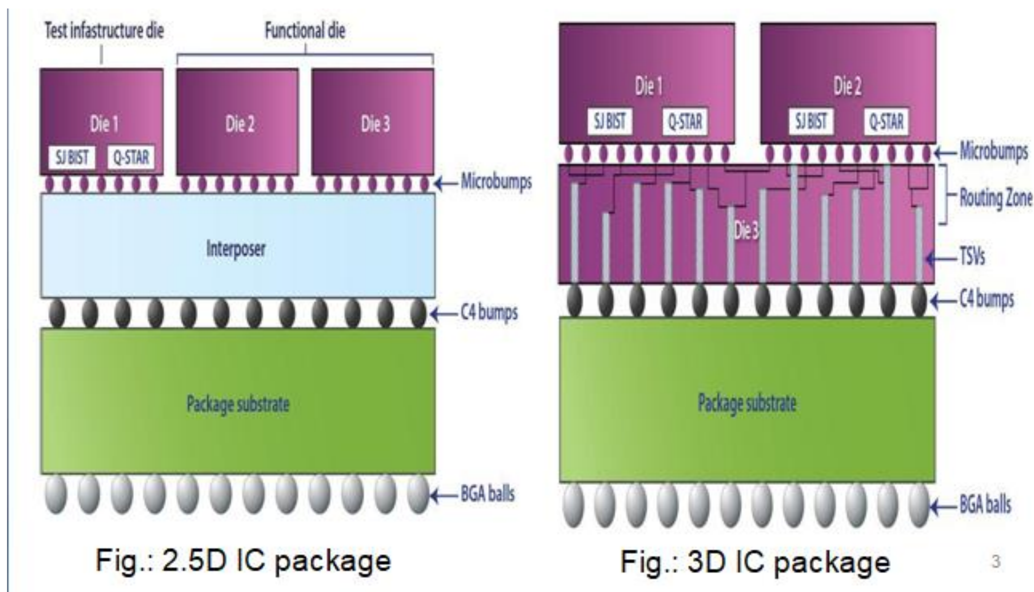

Figure 1-2: A 2.5D and a 3D package

The 2.5D packages have got a huge capacity and high performance. They also offer yield advantages as it's easier to make high quantity small dies than to make a single large die. However it is not so significant to do all this, hence this is the main limitation of the 2.5D packages. The 3D packages have the same and more advantages than the 2.5D ones. The limitations in 3D ones include cost, device impact, design flow and reliability.

1.3 Through Silicon Vias in 3D/2.5D packages

The through-silicon-vias (TSVs) are the vertical electrical interconnects etched in a silicon die. The reduced connection length, with short vertical connections through the silicon die is the basic advantage of the incorporation of TSVs in a package. The TSVs provide decreased latency, high bandwidth and allow high speed communications and low power level communication links between circuits [14]. Also they are known for the high performance in packages and high interconnection density.

In a 2.5D package, a silicon interposer with fine TSV pitch is needed. The silicon interposer gives high connectivity between the die. This interposer has some issues like warpage after die attach, workability etc. Hence, this interposer is not used in high volume production. Figure 1-3 shows a field programmable gate array (FPGA) device which were the first device to make use of silicon interposers.

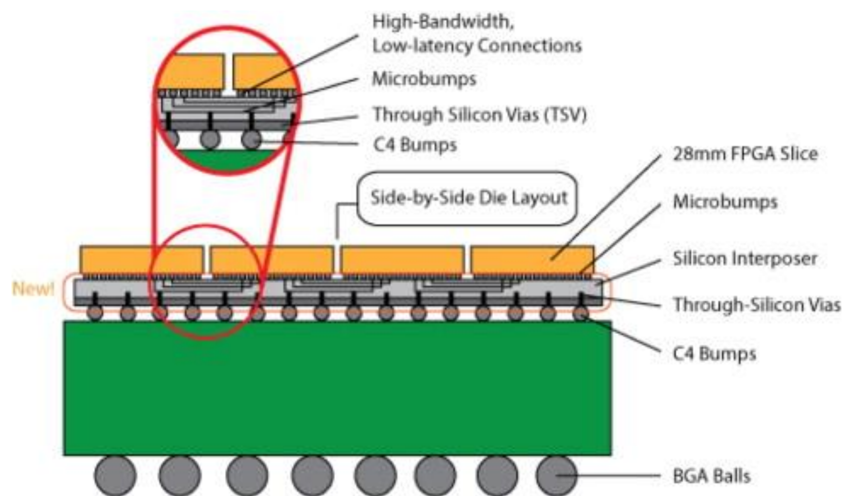

Figure 1-3 TSVs in an FPGA package

A 3D stacked die with TSVs needs a TSV pitch similar to that of the 2.5D interposer. The challenges associated in this case are of testing, assembly and the heat removal from the stack. The wide I/O DRAM devices (which use the stacked die with TSVs) are shown in

figure 1-4. The bandwidth association between the memory and the microprocessor in the DRAM device is high as shown in figure 1-4 [14].

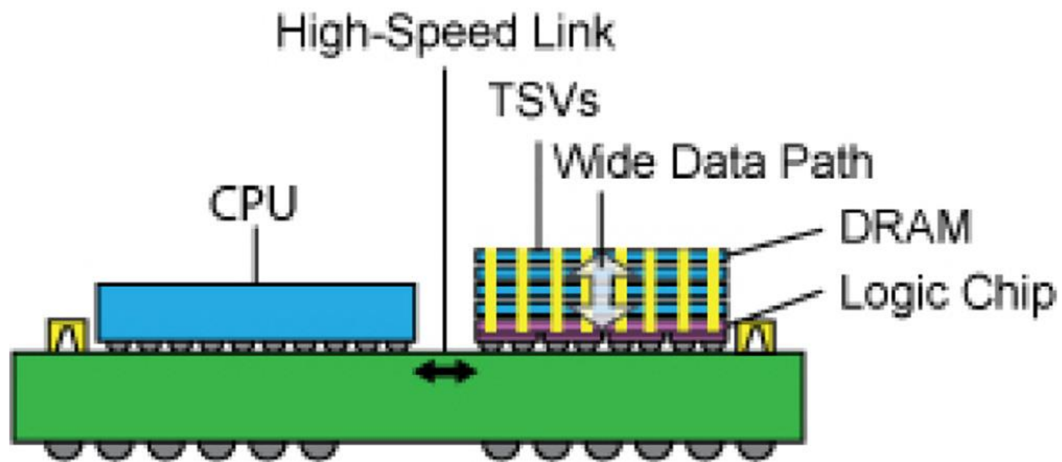

Figure 1-4 TSVs in a DRAM device [14]

Chapter 2

Recent Trends in 2.5D packaging

The 2.5D packaging is an addition to the 3D packaging technology using a silicon interposer with TSVs as explained earlier. The TSVs play a crucial role in 2.5D packaging. In the 2.5D packaging, the technologies like TSVs and the other interconnections within themselves like between chip to chip or chip to wafer etc. are used. In the recent years, there has been advancement in the 2.5D packaging technology, one of which is the copper pillar bump technology. This technology is quite important and prominent in providing a low pitch and high interconnection density. In this technology, a solder cap is used in the copper pillar which is responsible for a lot of benefits like low solder spread out, high ball standoff etc. This technology's limitations are studied by considering the solder cap material's impact on the package. An alternate approach to avoid this limitation is to connect two copper pillars without the aid of any material for the solder caps. Also the important factor in 2.5D packaging is the use of various flip chip packaging technologies [15].

2.1 2.5D Packaging in the IC Industry

Figure 2-1 The 2.5D packaging and HBM [16]

The 2.5D provides the heterogeneous integration of the integrated circuit products on the one and only silicon interposer and packaged as a system in package. This package can integrate the logic die, radio-frequency devices etc. in various technologies and can be improved 100 times in the bandwidth and about 50% energy savings. In this way, the packaging of a 2.5D device has a low cost of the entire package. There is a better output in a die with smaller size as compared to the larger one and hence, there is lower die cost reduction. The cost of the silicon interposer is an additional cost in the 2.5D packaging. There is a reduction of cost in the NPUs with the 2.5D memory packaging.

The silicon interposer is very important as far as the 2.5D packaging is considered. Hence the accessibility of the different interposer technologies is the crucial factor in this packaging of electronic devices like the High Bandwidth Memory (HBM). The figure 2-1 depicts the HBM in which four dies are mounted on the top of a base die. In each of the four layers, the top metal line is connected to the microbump of the DRAM layer. The bottom one is connected to the Through-Silicon-Vias, except for the uppermost die. The size of the interposer should be large so that the integration of more number of components can be done on the interposer and hence this results in higher performance of the 2.5D device than before.

Nowadays instead of the silicon interposer, an organic interposer is used for the 2.5D packaging. The technologies associated with the organic interposers can eliminate the limitations of the size and the warpage issue of the silicon interposer and can result in half of the cost reduction as compared to silicon. The warpage issue in Si interposer is due to the CTE mismatch between the interposer and an organic substrate. Due to symmetry in the structure, the organic interposers experience less warpage. [16]

2.2 The 2.5D Packaging Solutions

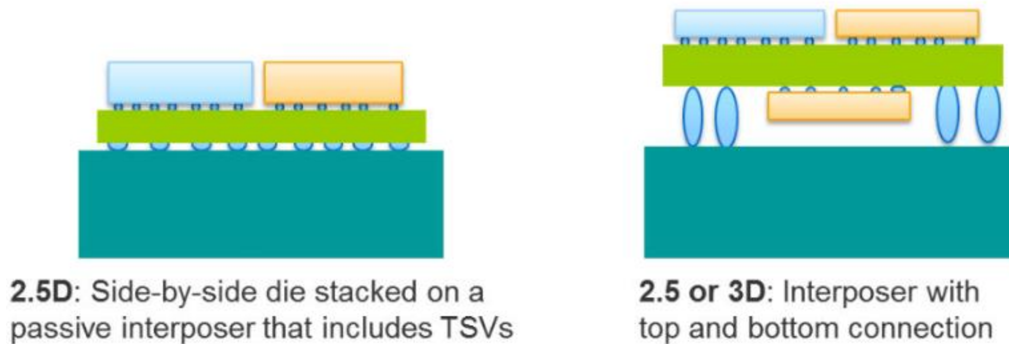

Figure 2-2: A 2.5D Packaging Solution [17]

A new series of solutions is introduced in the integrated circuits industry now by implementing the heterogeneous integration of these ICs and the wafer level packages. This series is called as advanced packaging, which offers high interconnection density and low power consumption as compared to that of the solutions of the conventional packaging.

The figure 2-2 shows a conventional 2.5D package with a silicon interposer on the left hand side and the silion interposer with top and bottom connection. This is one of the packaging solutions with the HBM, high speed interconnects, space efficiency and low power consumption. The silicon or organic interposers are used to stack the dies to get a better interconnection between the wafer and the die. The issues like heat dissipation, high cost of TSVs production and warpage occur due to the dies' vicinity in the 2.5D packaging.

The figure 2-3 shows the fan-out wafer-level-packaging (FOWLP) technology which is used as a substitute for the 2.5D packaging. The fan-in wafer-level chip-scale-packaging (WLCSP) technology runs a single die whereas the FOWLP runs numerous dies. The thickness and the form factor of the packages made using FOWLP technology is quite

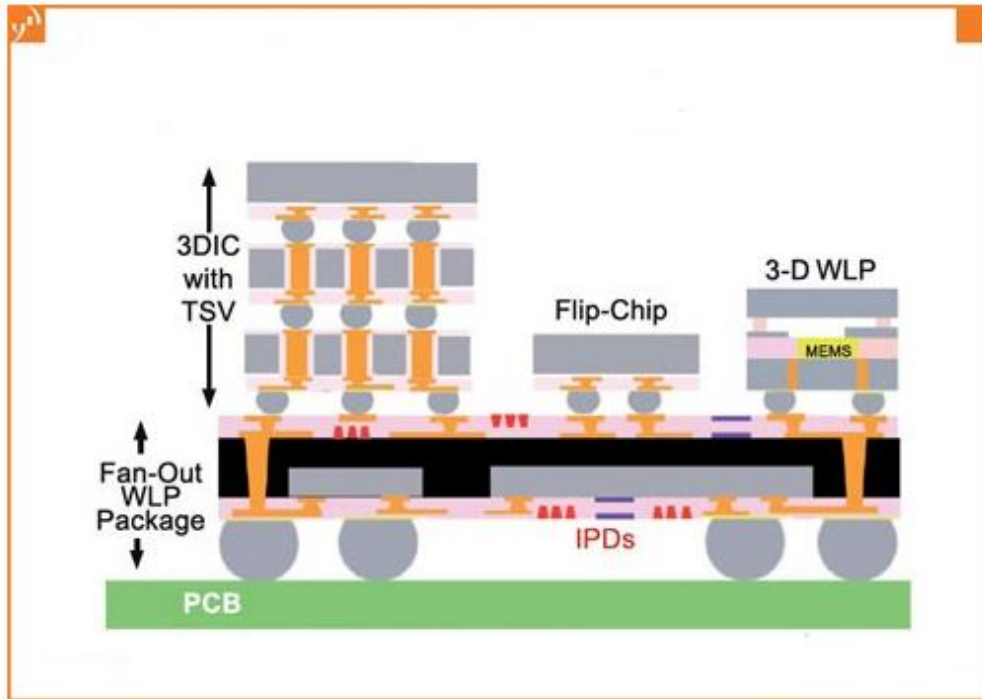

Figure 2-3 Fan-out wafer-level-packaging [17]

small whereas the density of its input output terminals is large. Also this FOWLP technology can reduce the cost and can overcome the associated challenges. Hence it is used as a substitute for the 2.5D packaging considering its heterogeneous integration. There are few other 2.5D packaging solutions like implementation of the TSV technology in it, the enhancement of the redistribution layers etc. [17].

Chapter 3

Model Description

ANSYS 18.0 has been used to model the 2.5D TSV package that consists of huge number of solder balls, TSVs and microbumps. This created model is called as the detailed model and an octal model is made out of it using the octal symmetry concept. This octal model is then subjected to a thermal cycling test. After analyzing this octal model, the compact modeling technique is applied on it by replacing the solder balls and the microbumps with the corresponding effective blocks. Then this compact model is subjected to a thermal cycling test and the output parameter for this model is compared and validated to that for the octal model.

The reliability of a 2.5D TSV package is studied by subjecting the package model, taken from [3], to a thermal cycling test. It consists of TSVs with the diameter 30 μm, depth 150 μm and pitch 300 μm. However, the two underfills in the model of [3] are not used in this detailed model to minimize the complexity of its geometry while solving it. A new compact modeling method shown by Rajmane et al. [2], has been implemented in the detailed model to reduce its total number of elements and also to reduce the solve time to a considerable extent. The analysis is carried out as given here: Firstly, a detailed model is created and the octal symmetry conditions are applied on it. Then this obtained octal model is solved by subjecting it to a thermal cycling test, to get the output parameter as the total deformation; but still the number of elements in it are not reduced to a greater extent and hence the computational time while solving it is still high. Hence the compact modeling method is applied on this model. In the compact model, the solder balls below the silicon interposer are replaced with an effective block. An another effective block similar to this one is created to replace the microbumps above the silicon interposer. This compact model is then solved by subjecting it to another thermal cycling test and the

output parameter that is the total deformation obtained is then compared and validated to that of the detailed model. The materials for the different elements are modeled using the linear elastic properties except the TSVs (Cu metal) and solder balls (SAC 305). The solder balls are modeled as a rate-dependent viscoplastic material using the Anand's viscoplasticity properties. Anand's Viscoplasticity has the nine material constants of the Anand's viscoplastic constitutive law, viz., ŝ, A, ξ, m, h_0, a, n, s_0, Q and thus the material properties for the solder balls are defined using these constants. These constants are also used to describe the material properties for the effective blocks in the compact model. The fixed support boundary condition is applied on the vertex of one of the bottom edges and the frictionless support boundary condition is applied on the two adjacent symmetric faces of the models. Figure 3-1 depicts the detailed model of the 2.5D package in ANSYS whereas figure 3-2 depicts its octal model.

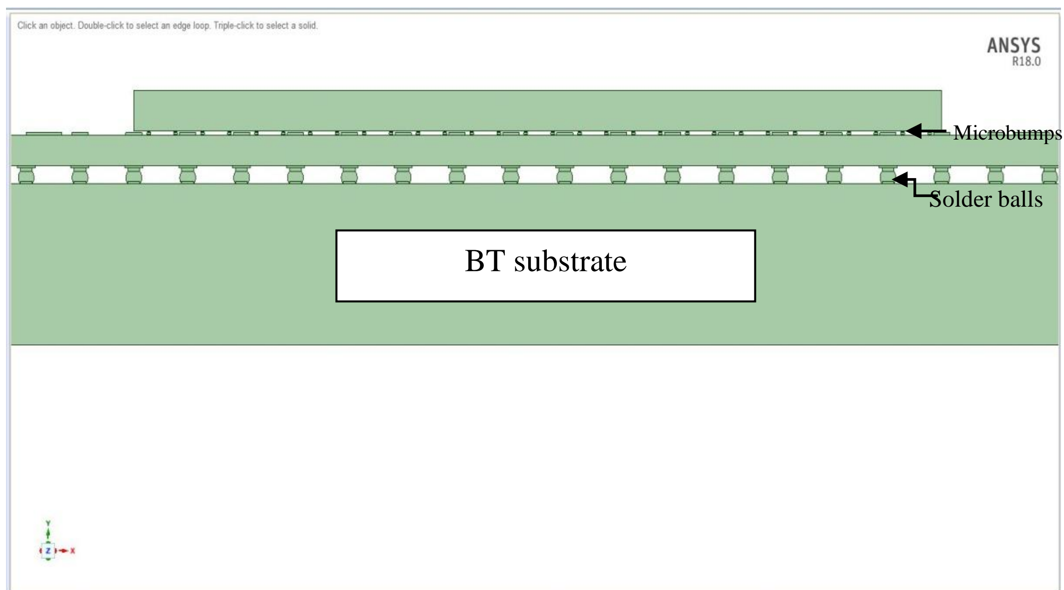

Fig 3-1: Cross section of the detailed model of the 2.5D TSV package

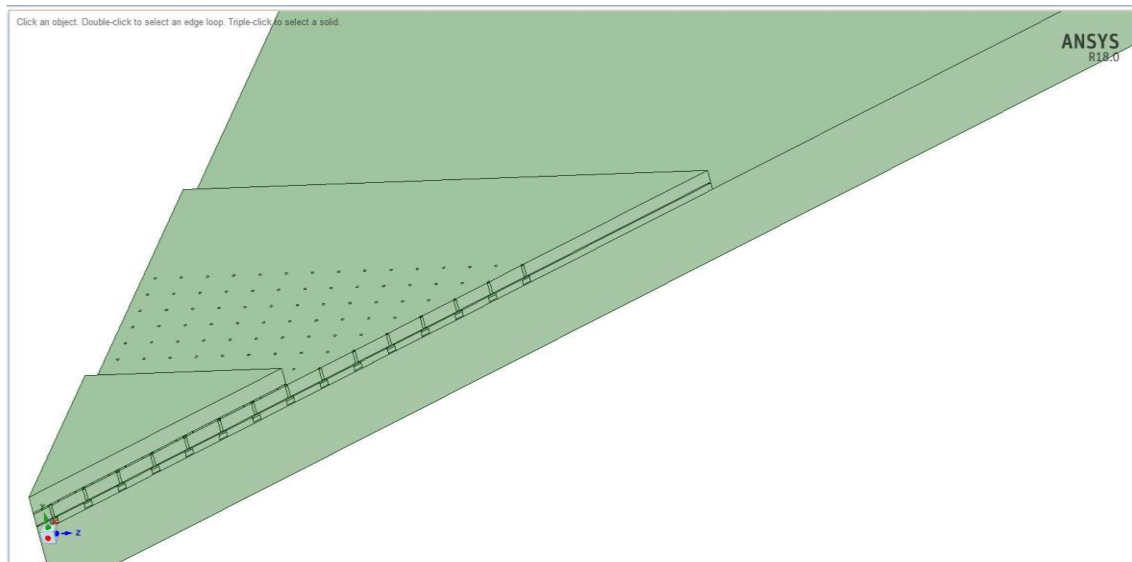

Fig 3-2: Octal model

Figure 3-3 depicts the mesh generated on the octal model.

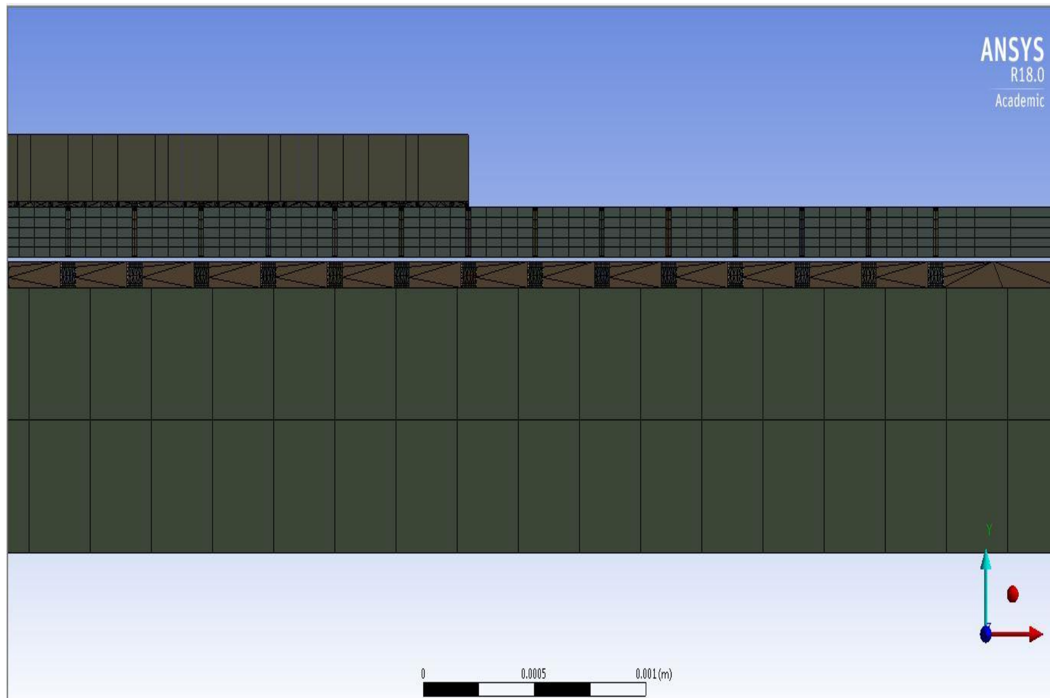

Figure 3-3: Meshing done on the octal model

Table 3-1 Anand's Constants for SAC305 [2]

S. No.	Anand's Constant	Units	Value
1	s_0	Mpa	1.3
2	Q/R	1/K	9000
3	A	sec^{-1}	500
4	ξ	Dimensionless	7.1
5	m	Dimensionless	0.3
6	h_0	Mpa	5900
7	$\hat{s}$	Mpa	39.5
8	n	Dimensionless	0.03
9	a	Dimensionless	1.5

As shown in the figure 3-3, the meshing is done on the octal model with an intention to have an optimum value for the body sizing of each element in the model so as to have a minimum number of nodes and the mesh elements in it. Thus the Hex Dominant Method is applied on this model to generate the mesh.

Table 3-2 Anand's Constant for Effective Block in the Compact Model [2]

S. No.	Anand's Constant	Units	Value
1	s_0	Mpa	0.15
2	Q/R	1/K	9000
3	A	sec^{-1}	500
4	ξ	Dimensionless	7.1
5	M	Dimensionless	0.3
6	h_0	Mpa	5900
7	Ŝ	Mpa	3
8	N	Dimensionless	0.03
9	A	Dimensionless	1.5

CHAPTER 4

Compact Modeling Technique

In this paper, the 2.5D IC package consists of 1600 solder balls and 400 microbumps and their diameter and pitch being in micrometers. Considering the quantity of both, their interconnectivity to the adjacent edges and the overall space consumed by them in the package, the entire structure thus becomes huge and its geometry is quite complex. Due to this, it becomes difficult to solve this 2.5D package model (the detailed model) while performing the thermal cycling analysis on it, and even if it is solved, it consumes a lot of time in it.

In an attempt to get rid of these issues, a compact modeling technique is implemented on this package as shown by Rajmane et al. [2] and an effective block, with the lumped material properties, replaces the solder balls and the microbumps. When the mesh is generated in the compact model, it is seen that the size of the mesh is such that the total number of elements decreased from 301725 to 11739 and the total number of nodes decreased from 610824 to 23849, which ultimately simplified the geometry of the package model and reduced the solve time as well.

The cross section of the compact model is shown in figure 4-1. The solder balls above the BT substrate is replaced by the effective block, whereas the microbumps above the silicon interposer is replaced by an another effective block. Figure 4-2 shows the mesh generated on the compact model.

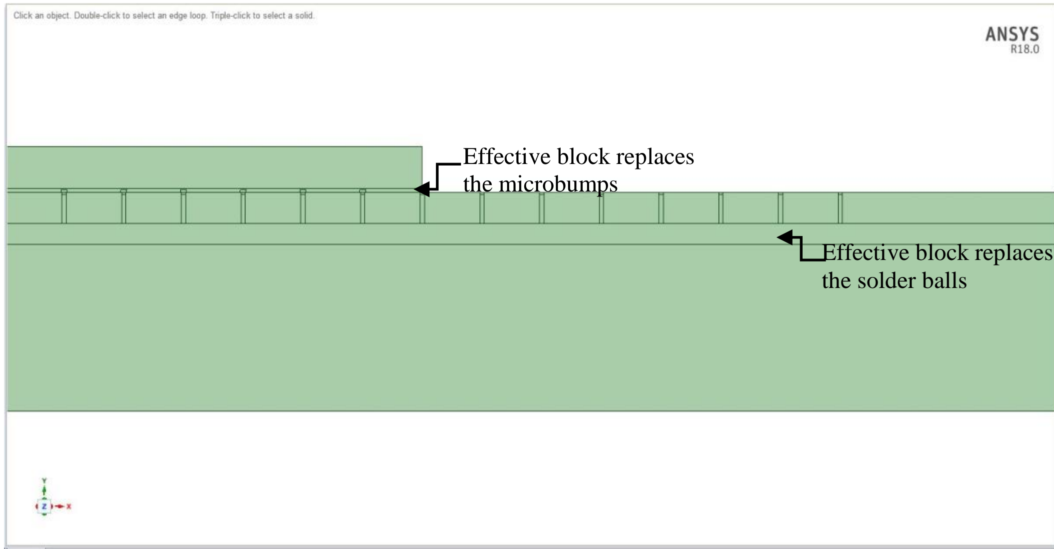

Figure 4-1 Cross section of the compact model

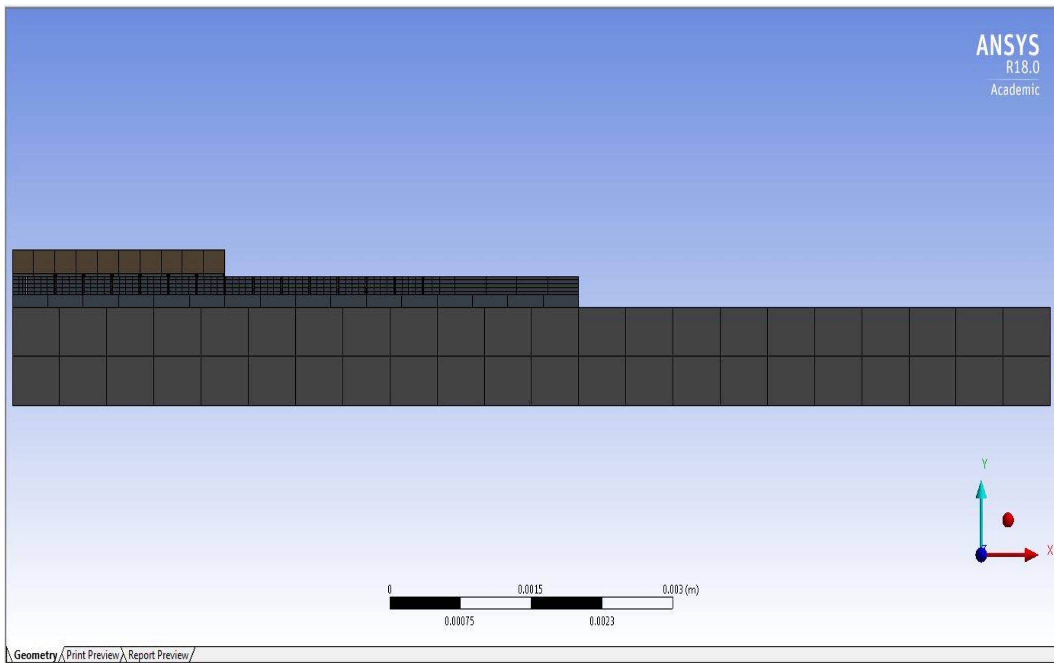

Figure 4-2 : Meshing done on the compact model

Chapter 5

Results and Discussion

Simulation and Validation :

As discussed in the previous sections, at first, thermal cycling is performed on the detailed model, with the temperature range from -40 degree Celsius to 125 degree Celsius (as per the JEDEC standard original loading conditions for thermal cycling). Three cycles of 60 minutes each with the 15 minutes ramp and 15 minutes dwell were applied [1]. The graph for the thermal cycling is as shown in Figure 5-1 below.

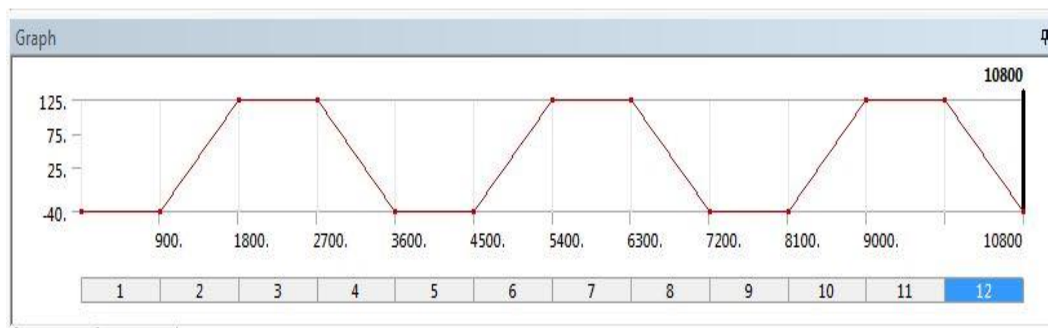

Figure 5-1 Thermal cycling analysis on the detailed model

The output parameter for this thermal cycling analysis is the total deformation which is shown in the Figure 5-2. The total deformation values for this model is as shown in Table 5-1.

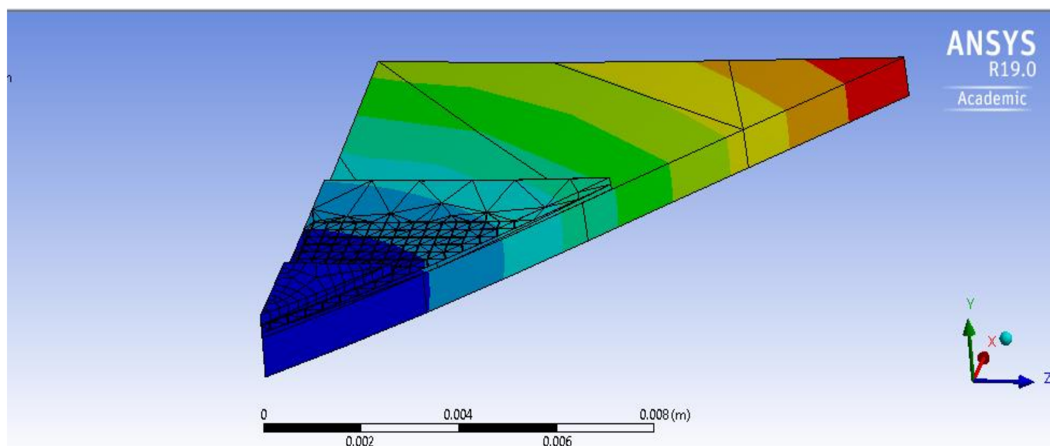

Figure 5-2 The total deformation on the detailed model

Table 5-1 : The total deformation values at different time intervals

Time (s)	Total deformation (mm)
900	0.95108
3600	0.95029
4500	0.95029
7200	0.95108
8100	0.95108
10800	0.95029

Considering the total number of elements in the detailed model and its overall computational time, the compact modeling technique is implemented on it as an attempt to resolve these issues. The compact model is then subjected to another thermal cycling test with the same range of temperature and the same number of cycles with the same time intervals. The graph for this is as shown below in Figure 5-3.

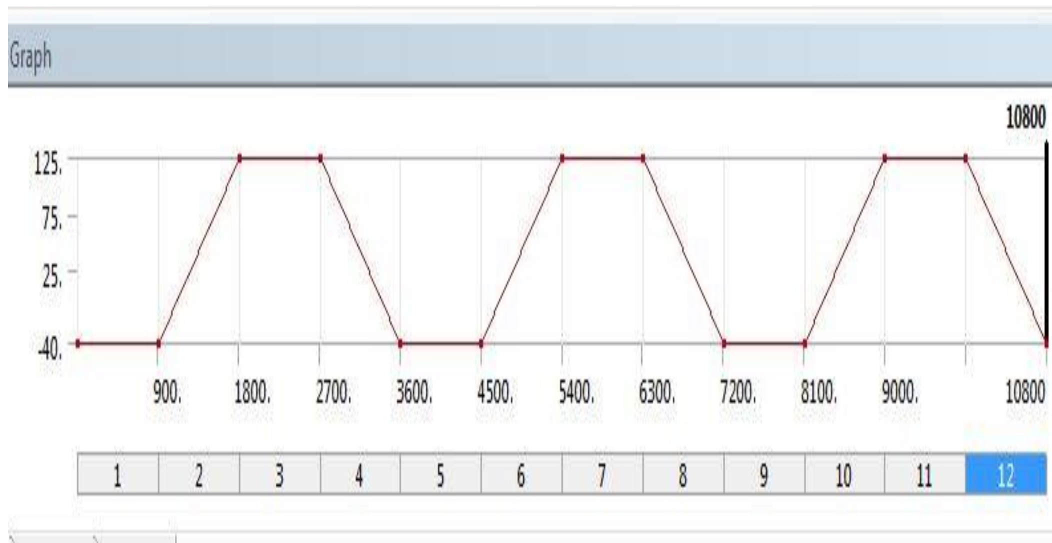

Figure 5-3 Thermal cycling analysis on the compact model

Again, the total deformation for this analysis is as shown below in the Figure 5-4.

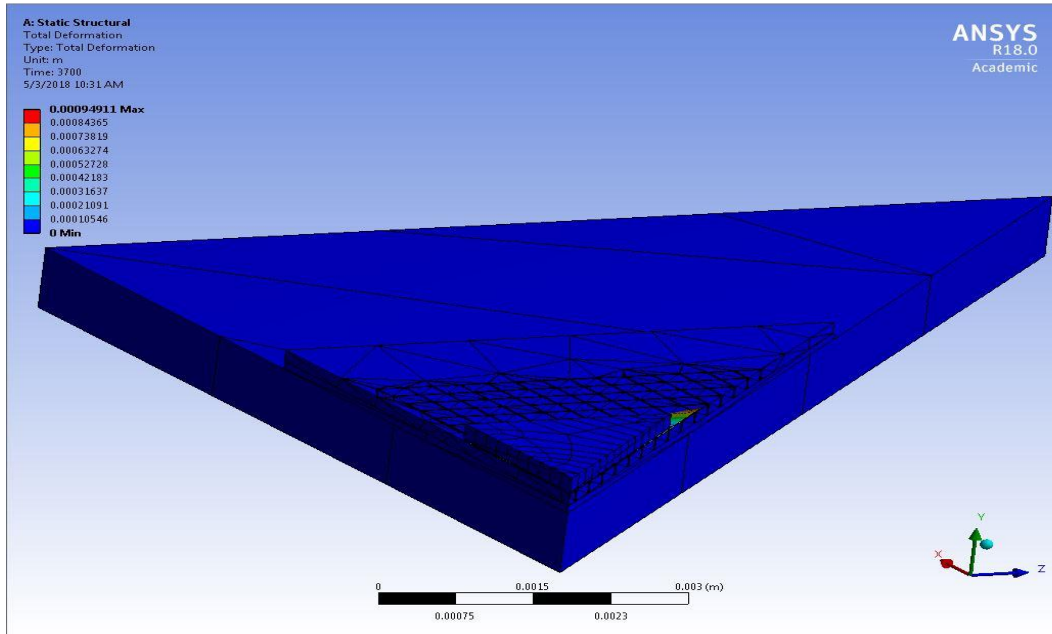

Figure 5-4 : The total deformation on the compact model

The total deformation for these thermal cycling analyses for each of the two models is compared and validated as shown in the Table 5-2 below.

Table 5-2 : Comparison and validation of the total deformation for both the models

Time (s)	Detailed model	Compact model	Percentage diff. %
900	0.95108 mm	0.94911 mm	0.21
3600	0.95029 mm	0.94898 mm	0.14
4500	0.95029 mm	0.94898 mm	0.14
7200	0.95108 mm	0.94911 mm	0.21
8100	0.95108 mm	0.94911 mm	0.21
10800	0.95029 mm	0.94898 mm	0.14

It can be seen from Figure 5-3, Figure 5-4, Table 5-1 and Table 5-2 that the compact modeling technique is effectively implemented on the 2.5D package model and the results obtained in the compact model analysis are in good sync with that obtained in the detailed model analysis. The obtained results for both the models vary gradually over the time as we can see from Table 5-2. Also the maximum percentage difference in their total deformation is 0.21% and the minimum is 0.14% which is quite good in terms of validation results.

Chapter 6

Conclusion

6.1 Concluding Remarks

To investigate the reliability of the 2.5D TSV package, the compact modeling technique is implemented on it. The output parameter i.e. the total deformation for the compact model is compared and validated with that of the detailed model and thus this validation shows how practical this compact modeling technique is. The values have been compared with the fracture toughness of silicon. The total deformation for the compact model is in good compatibility with that of the detailed model. The maximum percentage difference for the total deformation is 0.21%. The simplified geometry and a significant reduction in the solve time is fulfilled by the application of the compact modeling technique with the results for both the models being similar.

6.2 Future Work

The compact model is validated with the detailed model and thus the future work can be carried out on it in different ways. The compact model can be subjected to power cycling to induce the thermal stresses in it to check for its reliability. These stresses may result in the formation and propagation of the crack at the interface of the silicon interposer and the TSVs. Then the different output parameters like stress, strain energy etc. could be used to investigate the reliability of the model. Also the drop impact test can be carried out on this model to check for its reliability.

References

[1] Pavan Rajmane et al., “ Failure mechanisms of boards in a thin wafer level chip scale package,” 2017, 16th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm), Orlando, FL, 2017, pp. 1099-1105.

[2] Pavan Rajmane, Hassaan Ahmad Khan, Fahad Mirza, Dereje Agonafer, “Chip Package Interaction Study to Analyze the Mechanical Integrity of a 3D TSV Package”, ASME International Electronic Packaging Technical Conference and Exhibition, Interpack 2015.

[3] He Ma, Daquan Yu, Jun Wang, “The development of effective model for thermal conduction analysis for 2.5D packaging using TSV interposer”, Microelectronics Reliability, 54, 2014, 425-434.

[4] 3DIC & 2.5D TSV Interconnect for Advanced for Advanced Packaging 2014 Business Update report, Yole Development, July 2014.

[5] Fahad Mirza, Gaurang Naware, Ankur Jain, Dereje Agonafer, “Effect of Through-Silicon-Via Joule Heating on Device Performance for Low-Powered Mobile Applications”, Journal of Electronic Packaging, 136, 2014.

[6] F. Mirza, “Compact Modeling Methodology Development for Thermo-Mechanical Assessment in High-End Mobile Applications” - Planar 3D TSV Packages, Arlington, TX, 2014.

[7] C. Shah, F. Mirza and C. S. Premachandran, "Chip Package Interaction(CPI) Risk Assessment On 28nm Back End Of Line(BEOL) Stack Of A Large I/O Chip Using Compact 3D FEA Modeling," in EPTC, Singapore, 2013.

[8] Yuan Lu1,2, Wen Yin1,2, Bo Zhang1,2, Daquan Yu1,2, Lixi Wan2, Dongkai Shangguan, “A New 2.5D TSV Package Assembly Approach,” IEEE, 2013.

[9] Dhafer Abdulameer Shnawah, Mohd Faizul Mohd Sabri, Irfan Anjum Badruddin, “A review on thermal cycling and drop impact reliability of SAC solder joint in portable electronics products,” Microelectronics Reliability 52 (2012) 90–99.

[10] Meng-Jen Wang, Chang-Ying Hung, Chin-Li Kao, Pao-Nan Lee, Chi-Han Chen, Chih-Pin Hung and Ho-Ming Tong, “TSV Technology for 2.5D IC Solution,” IEEE, 2012.

[11] http://electronicpackaging.org/electronicpackaginginfo

[12] http://nptel.ac.in/courses/108108031/module1/Lecture01.pdf

[13] http://nptel.ac.in/courses/108108031/module1/Lecture02.pdf

[14] Jeffrey P. Gambino et al., “An overview of through-silicon-via technology and manufacturing challenges,” Microelectronic Engineering 135 (2015) 73–106

[15] Dapeng Liu, Seungbae Park, “Three-Dimensional and 2.5 Dimensional Interconnection Technology: State of the Art,” Journal of Electronic Packaging, March 2014.

[16] K. Tran, "Scaling the Next-Generation Architecture: The Integration of 2.5D and 3D Integrated Circuits," in *IEEE Solid-State Circuits Magazine*, vol. 8, no. 2, pp. 3

[17] https://www.electronicproducts.com

Biographical Information

Neha Vinayak Gaikwad has done the Bachelors in Mechanical Engineering major in May 2016 from Shivaji University, Kolhapur, India. She started the Masters program in Mechanical Engineering at The University of Texas at Arlington in August 2016. She joined the EMNSPC Lab (Electronics MEMS & Nanoelectronics Systems Packaging Center) under Dr. Dereje Agonafer and worked on the reliability of the electronic packages.