# SOLDER JOINT DESIGN OPTIMIZATION OF QUAD-FLAT PACKAGE WITH GULLWING LEADS UNDER ACCELERATED THERMAL CYCLING AND POWER CYCLING

**BY**

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May 20, 2018

# Abstract

SOLDER JOINT DESIGN OPTIMIZATION OF QUAD-FLAT PACKAGE WITH GULLWING LEADS UNDER ACCELERATED THERMAL CYCLING AND POWER CYCLING.

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Ever growing complexity in designing of Integrated Circuits and accommodating high number of Interconnections in the device is the main source of motivation in today's world of IC devices. Quad Flat Package (QFP) with Gullwing leads is spearhead technology which enables high connectivity levels required to be customized in most convenient and advantageous form. Gullwing leads have the advantage of having a large area in contact with solder and also work as mechanical springs. They also make it easier to inspect and rework. Lot of work has been carried out on inspecting the reliability of solder joints in QFP packages under Accelerated Thermal Cycling (ATC) as the only load.

Devices go under a loading condition when you switch it on and off numerous times. This type of load is known as Power Cycling. Past studies have shown that some of the organic packages fail early in power cycling but perform better in ATC [1]. In predicting life of the package, we usually consider Accelerated Thermal Cycle (ATC) in which we believe temperature is uniform through-out. But by taking Power Cycling into account we have non-uniform temperature in the assembly where die is the only source of heat generation. In this paper, Solder joint reliability of QFP with Gullwing leads is evaluated by using Finite Element Analysis (FEA) under two Loading conditions and the combination of two. For design optimization, our main focus is on the shape of solder.

From past studies its concluded that amount of solder affects the reliability of solder joints. Geometry of QFP package with different solder shapes, angles and Gullwing leads were modeled using Ansys Design modeler tool. These models were then subjected to ATC and Power Cycling to assess the stress distribution and the plastic work in the solder joints. We leveraged this comparative study to predict best solder profile design by analyzing results obtained from simulations to lessen the solder wreck and increase life of the package.

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Chapter 1

# INTRODUCTION

## 1.1 3-D PACKAGES

**Electronic packaging** is ever growing domain in the field of providing secured environment for proper functioning of electronic circuits. By secured it means including protective features for dissipation of heat, damages from both electro-magnetic and mechanical, better signal distribution and economical power distribution.

### 1.1.1 Hierarchy of Packaging levels

All the electronic components most importantly require high reliability and performance keeping in check the cost, weight and size. Inherent development in designing of Integrated Circuits and accommodating high number of Interconnections has been foothold to come up with various packaging technologies. All of these factors depend on the capabilities related to making more integrated components, which in turn depend on advanced assembly equipment that can put a large number of small components into smaller and smaller areas. It is a technology which is classified into Chip level, Board level, System level.

1 CHIP LEVEL PACKAGING

2 BOARD LEVEL PACKAGING

3 SYSTEM LEVEL PACKAGING

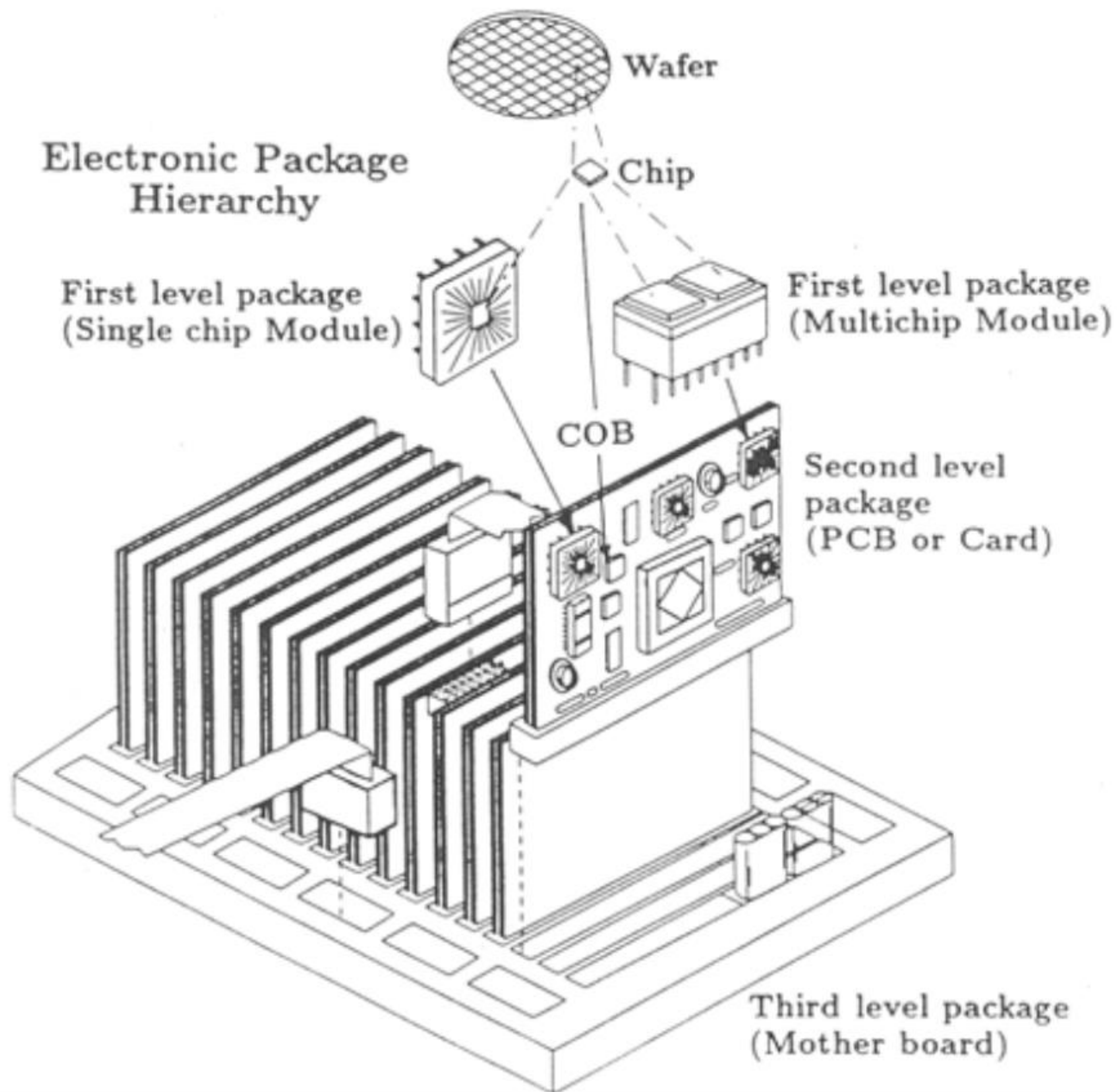


*Figure 1 Hierarchy of Packaging Levels*

**Level – 0:**

This level includes various components like transistors, resistors, capacitors with no packaging. A bare die or chip is designed and manufactured for IC circuits.

**Level - 1:**

When this die is encapsulated in the mold we get an integrated circuit as per many interconnection methods.

**Level - 2:**

In this level the bare Chips or bare dies are solder to the PCB.

**Level - 3:**

In this level PCBs are stacked on to the motherboards or the systems.

**Level - 4:**

These racks are then installed in the final system.

EX: ETHERNET LAN

### 1.1.2 Breakthroughs in Chip packaging

It includes technologies that have been emerged right from Through hole mounting and then developing to Surface mount and later to chip scale packages.

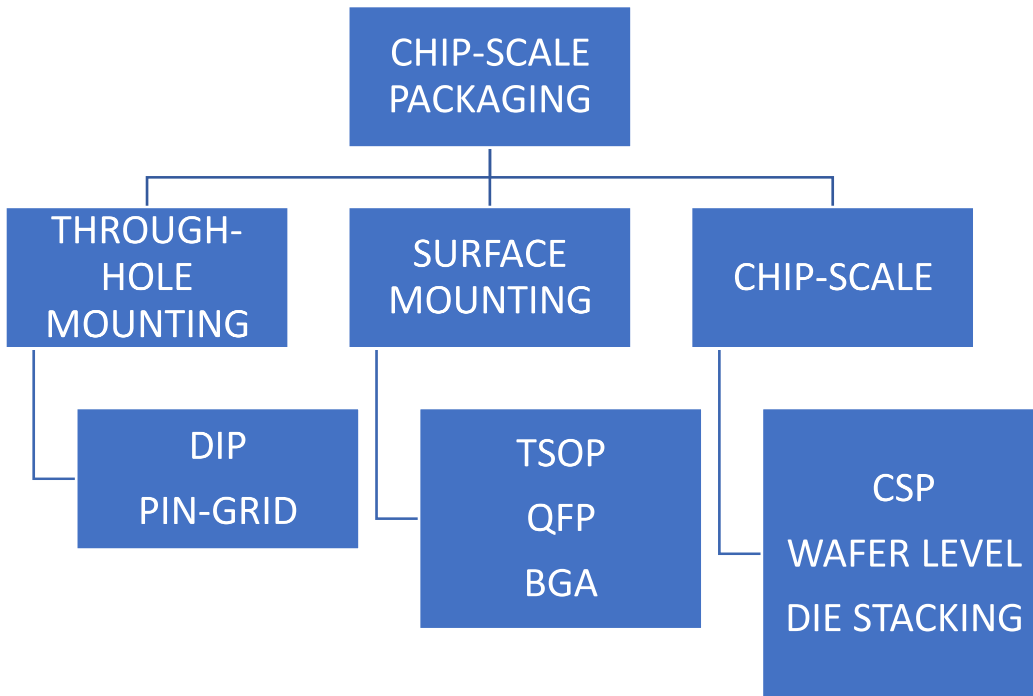


*Figure 2 Development in Chip-scale packaging*

## 1.2 QUAD-FLAT PACKAGE (QFP)

Quad Flat Package is an integrated circuit package splaying IC leads on all four sides of the package. These leads are of gullwing shape allowing solid foothold on the PCB. Where the manufactures over the globe are aiming to tackle various

complexities in the packages and come up with thinner, compact and thermally improved QFP package with multi connections. Very high number of interconnections in QFP make it very important for the manufacturers to take great deal of care in developing and designing Printed circuit boards.

With all the advantages, QFP has become an asset for electronic companies but there are various factors to be considered to make the package reliable. Solder Joint Failure is the most severe of the problems. Most commonly, ATC is used to evaluate and determine the Solder Joint failure in which temperature distribution is uniform throughout the system. But as the matter of fact die is the one which is the main source of heat and shouldn't be neglected.

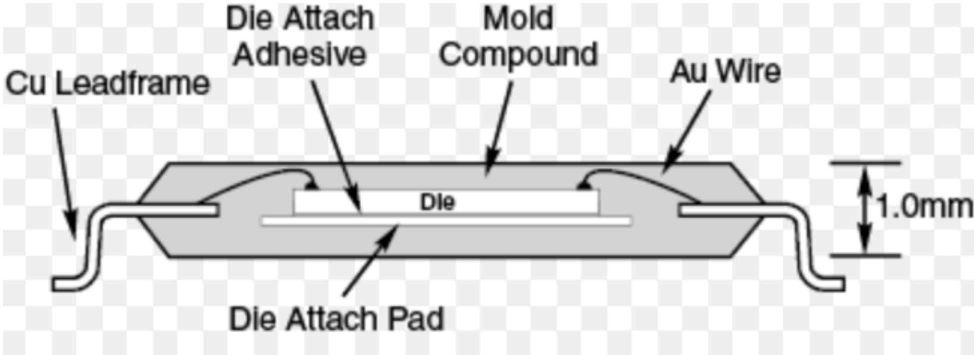


*Figure 3 Quad-Flat Package with Gull wing leads*

### 1.2.1 Basic components of Quad Flat Packages

- Substrate
- Die
- Die attach
- Cu leadframe
- Bond wire

- Substrate

Substrate can be defined as the base formed by semiconductor material such as silicon. It is also widely called as wafer and it's the first level of electronic packaging. It acts as an understructure on to which integrated circuits, resistors, diodes etc are mounted.

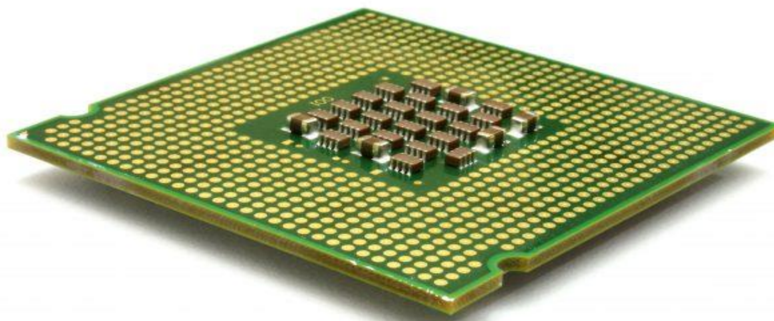

*Figure 4 Substrate*

- Die

Die acts as a functional device in electronic packages and its made up of semiconductor material as well. Many different functional circuits are incorporated in the Die.

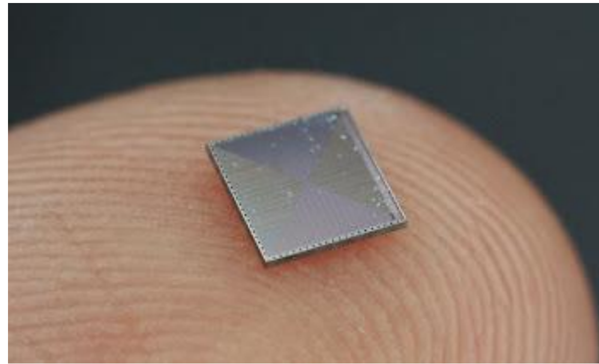

*Figure 5 Die*

- Die attach

Die attachment compound is used to adhere the die. It also is responsible to provide electrical grounding and thermal dissipation in most effective way.

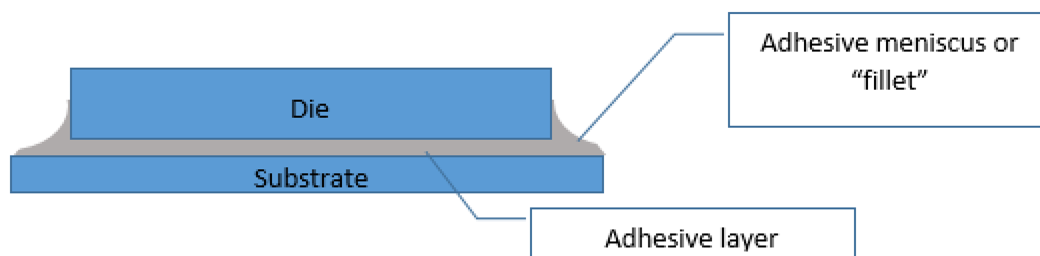


*Figure 6 Die attach*

- Cu Lead frame

Cu lead frame is a structure used to connect Integral circuit to the PCB. It transfers the signal from internal circuit to the external circuit via bond wires to leads and then to the PCB.

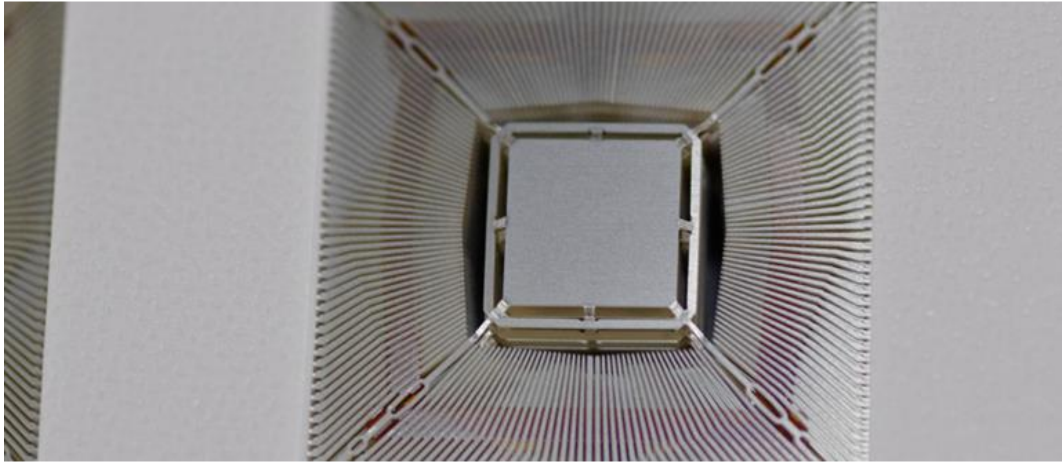

*Figure 7 Cu Lead-frame*

- Bond wire

Wire bonds are used for interconnection between integrated circuit and to other external circuits or to the PCB. It is used to transfer the signal from Integrated circuit and usually made up of gold and aluminum.

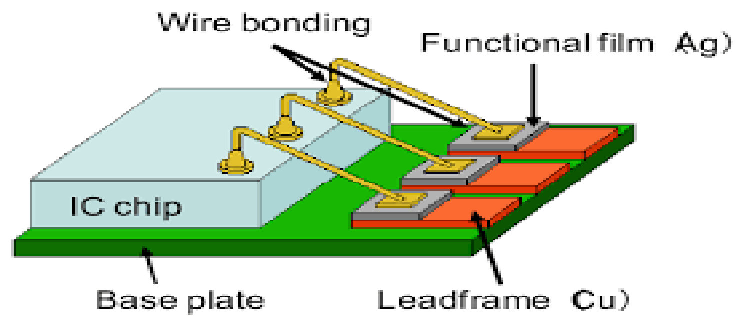


*Figure 8 Bonding wire*

# Chapter 2

# LITERATURE REVIEW

## 2.1 Reliability

Reliability Engineers all over the world come up with new technologies every day, what is new today is going to be out dated tomorrow. So, in today's world of electronics with new complex designs and the structures of the packages make it is very important to make them reliable to various problems. Some of them are, solder fatigue failure due to power transient and environmental changes is a primary interest for assemblies. Factors like thermal expansion mismatch which arise due to presence of so many elements configured on printed circuit boards. Also, package-specifics like mountings, construction, electronic housing and configuration of printed circuit boards play major role in reliability of the electronic package.

Why carrying out reliability test on electronic packages is required? Its required for the sake of providing most robust products in the market. When these products are put under actual working conditions we mostly see that failure occurs at system level. But what we fail to understand that failure actually starts at component level. We see time and temperature dependent creep develop from resulting thermal expansion mismatch between the various package materials. When the packages are put under repeated loading and unloading of thermal cycles and power cycles we find accumulation of plastic strain which eventually leads to solder joint failure and breaking of integrated circuit.

In this paper, Solder joint reliability of QFP with Gullwing leads is evaluated by using Finite Element Analysis (FEA) under two Loading conditions and the combination of two. For design optimization, our main focus is on the shape of solder. From past studies its concluded that amount of solder affects the reliability of solder joints. Geometry of QFP package with different solder shapes, angles and Gullwing leads were modeled using Ansys Design modeler tool. These models were then subjected to ATC and Power Cycling

to assess the stress distribution and the plastic work in the solder joints [5]. We leveraged this comparative study to predict best solder profile design by analyzing results obtained from simulations to lessen the solder wreck and increase life of the package.

## 2.2 Finite element modeling

Finite element analysis is most widely used analysis tool which uses finite element method to analyze and do simulations on various engineering systems and components. It is a design utility package which comes with tons of advantages like optimization of designs, reducing development time by reducing testing time. It allows carrying out analysis in number of analysis areas of which we are going to use static structural and transient thermal analysis for our study.

Complex parts are modeled and subdivided into finite number of elements or discretization by FEA and obtaining a simpler analysis. Following are the steps followed in solving and finite element problem.

- Create geometry
- Defining material properties
- Meshing
- Define load and applying boundary conditions
- Solution

## 2.3 Constitutive Equations

The cause of the failure can be mechanical, thermal, electrical or combination of them. Lot of variation is seen in the mechanical properties and performance of materials by little change in temperature. Some of them are directly proportion

while others are inversely related. It is very necessary to know the material properties of various components. Temperature dependent properties such as Coefficient of thermal expansion, Young's modulus and Poisson's ratio are critical in Finite Element analysis.

Where temperature rises materials become more ductile and at the same time it's elastic modulus and strength have inverse effects i.e they decrease. So, it is very important to understand and predict plastic strain as the function of stress, temperature and time. Taking all these factors into consideration along with the fact that the solders are modeled visco-plastic, therefore equation for inelastic strains incorporates both rate-independent plasticity and rate-dependent deformation.

## 2.4 Creep Curve

Creep can be defined as slow but permanent deformation over the period of time under load and mechanical stresses. Creep can also be called as Time-dependent plasticity. It is generally seen at high temperatures and in the materials whose absolute temperature is greater than half of absolute melting temperature [9].

Creep is a slow process and takes place in three stages primary, secondary and tertiary as shown in the fig.

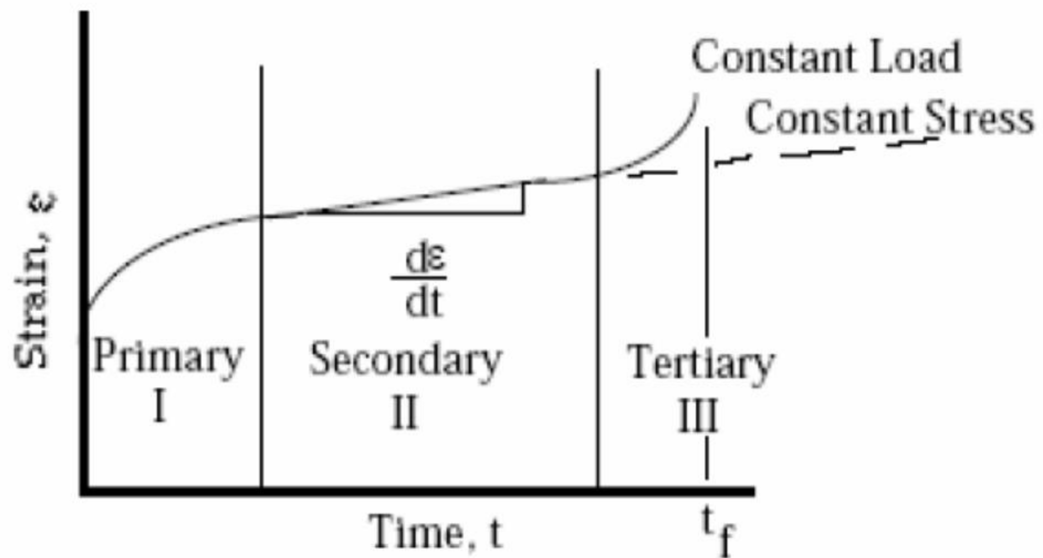


*Figure 9 Creep curve*

Primary Creep - Its instantaneous and then slows down.

Secondary Creep - Its very slow and increases over large period of time. This stage is of our interest.

Tertiary Creep - Creep rate increases quickly and leads to failure.

## 2.5 Anand's Visco-plastic Model

Visco-plasticity is defined as unifying equations for temperature dependency and stress and strain dependency. Anand's model is widely used by incorporating it into Ansys. Arrhenious rate model for steady state creep strain is given by where

$$\dot{\varepsilon}_c = A\sigma^n e^{-(Q/R_g T)}$$

ε is the steady state creep strain rate, σ is the current stress, *A* and *n* are experimentally determined material constants, *Q* is the activation energy for creep, *Rg* is the universal gas constant, and *T* is the temperature in Kelvin.

Stress and strain rate dependency of Garafalo equation is given by,

$$\dot{\gamma}_s = C_1 \frac{G}{T}\left[\sinh\left(\alpha \frac{\tau}{G}\right)\right]^n \bullet \exp\left(\frac{-Q}{kT}\right)$$

where $\gamma_s$ is the steady state shear strain rate, $C1$, $n$, and α are experimentally determined material dependent constants, $Q$ is the material activation energy for creep, τ is the shear stress, $G$ is the shear modulus, $T$ is the absolute temperature, and $k$ is the Boltzmann's constant.

Anand's model incorporates an Arrhenius term for the temperature dependent strains and the stress and strain rate of the Garafalo equation.

Therefore, combining two equations we get Anand's unified equation as,

$$\dot{\varepsilon}_p = Ae^{(-Q/RT)}\left[\sinh\left(\xi \frac{\sigma}{s}\right)\right]^{1/m}$$

This model consists of single scalar internal state variable 's', called the deformation resistance.

$$s^* = \hat{s}\left[\frac{\dot{\varepsilon}_p}{A} e^{(Q/RT)}\right]^n$$

Anand's law consists of nine material constants A, Q, ξ, m, n, hu, a, $s_u$, ŝ.

## 2.6 Fatigue life prediction model

A signal is transferred from integrated circuit via lead-frame to any external circuit. That makes Fatigue life modeling of solder joints of sheer importance for the overall reliability of electronic package. Here we are going to list all the available fatigue life prediction models and discuss which we are going to use in our studies. These models basically tell us the overall life or number of cycles component will work fine in the working environment.

Following are some of the life prediction models,

- Coffin mason
- Stress based
- Strain energy density based-Darveaux Methodology
- Creep strain based
- Damage mechanics based

### 2.6.1 Darveaux methodology

As explained above there are numerous methods available of which Darveaux methodology or Energy based fatigue model Is widely used and we will also incorporate it in our study. Darveaux [1] experimentally found out 4 growth rate constants and equations to find out number of cycles and the crack propagation rate.

Firstly, plastic work of the most critical solder joint is calculated and the used to find weighted average plastic work,

$$\Delta W_{ave} = \frac{\sum_{i=1}^{Element} \Delta W_i \times V_i}{\sum_{i=1}^{Elements} V_i}$$

Where *Wi* is plastic work density in ith element and *Vi* is volume of that element.

A thermal cycle to crack initiation,

$$N_o = K_1 \Delta W_{ave}^{K_2}$$

Crack propagation rate per thermal cycle

$$\frac{da}{dN} = K_3 \Delta W_{ave}^{K_4}$$

*Table 1 Darveaux Coefficient*

| | |
|---|---|
| K1 | 56300 CYCLES/PSI |
| K2 | 1.62 |
| K3 | 3.34E-07 |
| K4 | 1.04 |

## 2.7 Loads & Boundary conditions

- Quarter symmetry geometries were created to minimize the computation time and memory.
- We have fixed on bottom end of the PCB i.e. corner after symmetry so as to have restricted motion in z-direction.
- Temperature was set so that overall temperature was controlled and not to go above 125 degrees.

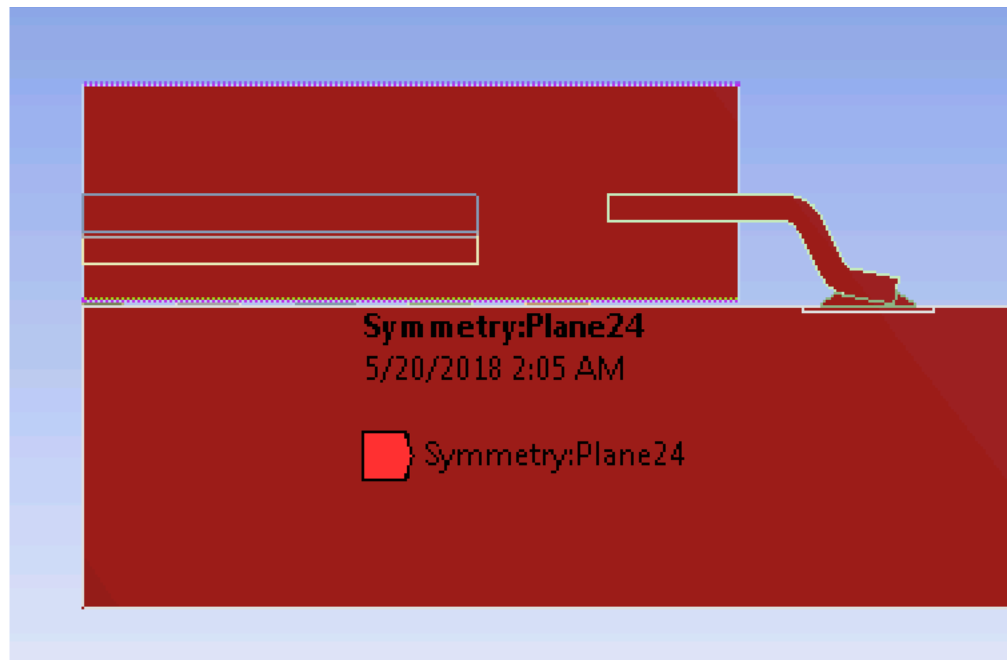


*Figure 10 Symmetric Boundary Condition*

### 2.7.1 Assumptions

- All materials considered linear elastic except solder.
- Solders are considered viso-plastic also,
- PCB is considered linear orthotropic elastic.

### 2.7.2 Accelerated thermal cycle

Accelerated thermal cycle is an accelerated life testing method to know how reliable the product is and it will sustain in the real life under working conditions. The bathtub curve [10] easily tells us how important reliability is, as defective parts and products with below acceptance level are already rejected and only fine and robust parts are moved forward in the production line and later in the market. The failure chance of these products is minimal and it's over the period of time and not abrupt.

The method of thermal cycling was referred from JEDEC standard JESD22-A104D. It is the method to examine the accelerated life of the product by applying Thermal cycling load of -40 to 125. Its applied for 15 min ramp/dwell on all the models. Repeated temperature changes can result in thermal fatigue which can be seen after three cycles. The initial stress-free temperature was set to be maximum temperature in the thermal cycle.

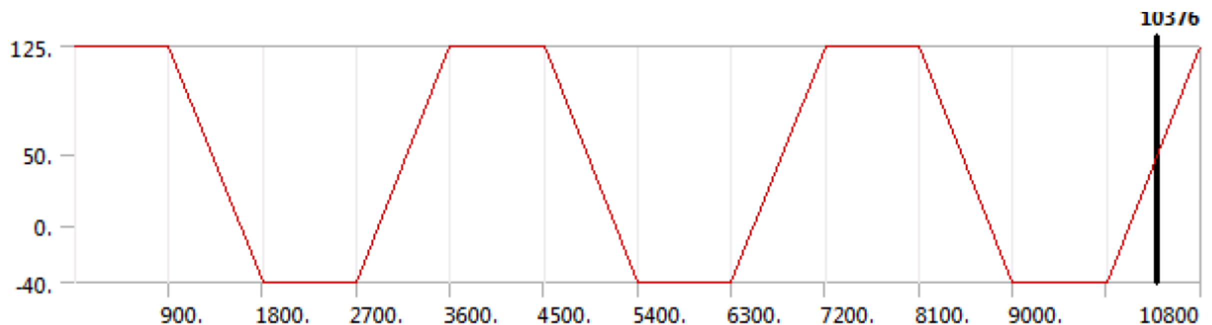


*Figure 11Accelerated Thermal Cycling Graph*

Time of one thermal cycle is 3600 seconds and is applied for 10800 seconds. The power cycling profile is shown in through the plot. This modeling methodology would provide damage predictions caused due to global and local CTE mismatch between the different package components[12].

| | Steps | End Time [s] |
|---|---|---|
| 1 | 1 | 900. |
| 2 | 2 | 1800. |
| 3 | 3 | 2700. |
| 4 | 4 | 3600. |
| 5 | 5 | 4500. |
| 6 | 6 | 5400. |
| 7 | 7 | 6300. |
| 8 | 8 | 7200. |
| 9 | 9 | 8100. |
| 10 | 10 | 9000. |
| 11 | 11 | 9900. |
| 12 | 12 | 10800 |
| * | | |

*Figure 12 Time steps for ATC*

We divided time cycle into 12 steps each step for 900 secs. Package was simulated for 15 mins ramp and 15 mins dwell.

### 2.7.3 Power Cycle

The on and off power cycles of functional devices for example die in the package will produce non-uniform temperature distributions within package components and between the package and interconnected hardware as well. In Power Cycling die is the main source of heat as it is turned on and off several times. The stresses which are resulted from such temperature variations are not similar to what are found in accelerated thermal cycling which has isothermal thermal distribution.

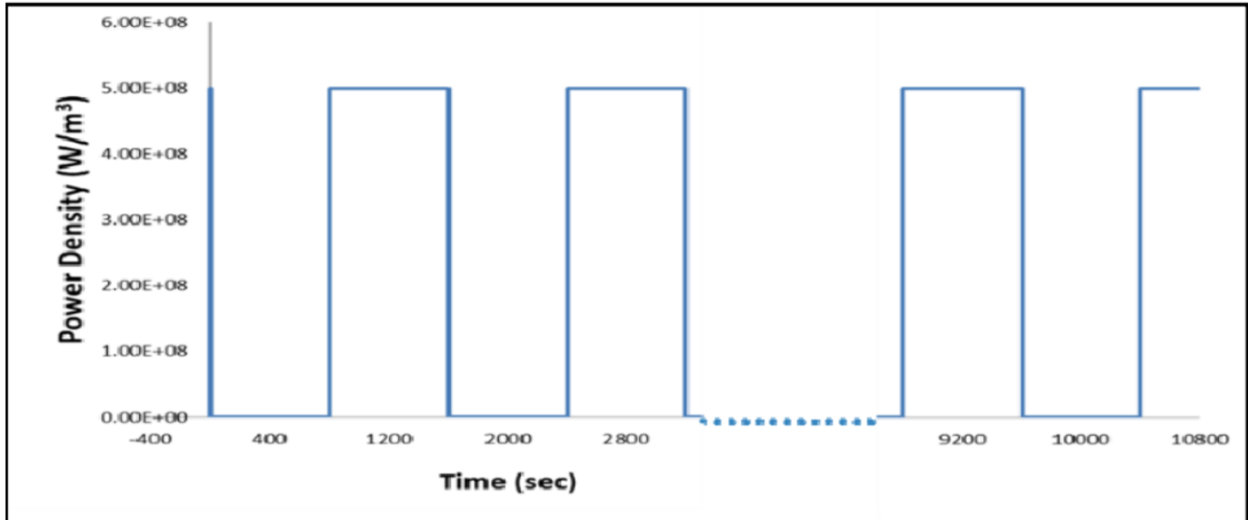


*Figure 13 Power Cycle Graph*

An assembly is also subjected to Power Cycling i.e. non-uniform temperature with the chip as the only source of heat generation [6]. In power cycling we get more reliable and realistic results in order to come up with most robust designs. As die is main source of heat it is obvious that much more thermal load will be acting on die and area around it. So, we are going to put 0.5 W/mm$^3$ power density on die and see its effects, we also apply convective heat transfer coefficient of 23 W/m$^2$.°C on all the faces.

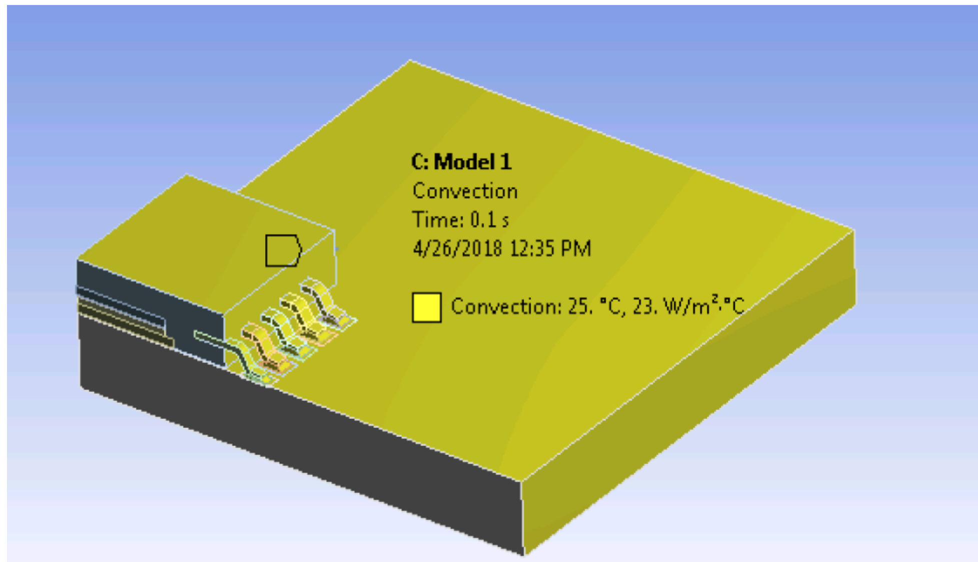


*Figure 14 Convective heat transfer*

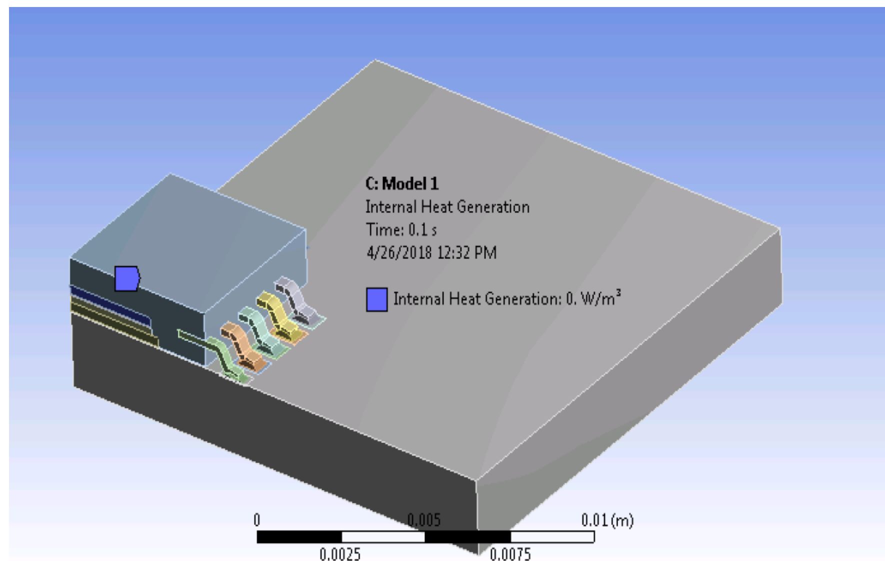


*Figure 15 Internal heat generation*

|  | Steps | Time [s] | ☑ Internal Heat Generation [W/m³] |
|---|---|---|---|
| 1 | 1 | 0. | 5.e+008 |
| 2 | 1 | 0.1 | 0. |
| 3 | 2 | 720. | 0. |
| 4 | 3 | 720.1 | 5.e+008 |
| 5 | 4 | 1440. | 5.e+008 |
| 6 | 5 | 1440.1 | 0. |
| 7 | 6 | 2160. | 0. |
| 8 | 7 | 2160.1 | 5.e+008 |
| 9 | 8 | 2880. | 5.e+008 |
| 10 | 9 | 2880.1 | 0. |
| 11 | 10 | 3600. | 0. |
| 12 | 11 | 3600.1 | 5.e+008 |
| 13 | 12 | 4320. | 5.e+008 |
| 14 | 13 | 4320.1 | 0. |
| 15 | 14 | 5040. | 0. |
| 16 | 15 | 5040.1 | 5.e+008 |
| 17 | 16 | 5760. | 5.e+008 |
| 18 | 17 | 5760.1 | 0. |
| * |  |  |  |

*Figure 16 Internal heat generation*

So, every time any functional device is turned off and turned on it heats up. Following time sequencing was used in our study [5]. This gives us non-uniform temperature distribution which helps us in getting more realistic results and give us clear idea about optimization of solder profile. JEDEC standard power cycle is used. Both the cycles are so set to get atleast three cycles so as get plastic work in critical solders.

## 2.8 Summary

Ten QFP models were created by changing various factors. Geometry of QFP package with different solder shapes, angles and Gullwing leads were modeled using Ansys Design modeler tool 18.0 Design modeler with given package dimensions. Thermomechanical Analyzer (TMA) was used to get the values of CTE's and glass transition temperatures. Dynamic Mechanical Analyzer (DMA) was used to calculate Young's Modulus and Poisson's Ratio. Power Cycling and convection is tested in Transient thermal analysis to get the thermal load acting on the package. This thermal load further was used in Static structural analysis along with Accelerated thermal cycling.

# Chapter 3

# OBJECTIVES AND APPROACH

## 3.1 Previous work

M Niessner *et al* [3] studied QFP by changing various factors in geometry and varying sizes of die and exposed pad. But this study was done considering Accelerated thermal cycling as the only load. Further, Unique's [5] work on QFN by taking power cycle into consideration and getting more realistic results has lead the foundation to this study. Lot of work has been done by various authors on reliability of solders in QFN and BGA packages considering various factors [7-9]. We are going to study QFP package with gullwing leads under combined loading condition Accelerated thermal cycling plus power cycling by changing various factors like solder volume, solder design, number of leads and size of the die.

## 3.2 Objectives

Lot of work has been carried out on inspecting the reliability of solder joints in QFP packages under Accelerated Thermal Cycling (ATC) as the only load. Drop impact is not only loading that can affect reliability, but the simultaneous thermal load, moisture, convection is also acting[11].

Past studies have shown that some of the organic packages fail early in power cycling but perform better in ATC [5-6]. In predicting life of the package, we usually consider Accelerated Thermal Cycle (ATC) in which we believe temperature is uniform through-out. But by taking Power Cycling into account we have non-uniform temperature in the assembly where die is the only source of heat generation.

We are going to study QFP package with gullwing leads under combined loading condition Accelerated thermal cycling plus power cycling by changing various factors like solder volume, solder design, number of leads and size of the die.

## 3.3 Approach

Quad flat package model was created in Ansys 18.0 Design modeler with given package dimensions. Thermomechanical Analyzer (TMA) was used to get the values of CTE's and glass transition temperatures. Dynamic Mechanical Analyzer (DMA) was used to calculate Young's Modulus and Poisson's Ratio. Power Cycling and convection is tested in Transient thermal analysis to get the thermal load acting on the package. This thermal load further was used in Static structural analysis along with Accelerated thermal cycling.

## 3.4 Package description

Ansys Designer modeler was used to create the geometry of Quad flat package (QFP) with gull wing type leads as finite element model under consideration. Some of the dimensions were taken from [8] as shown in the fig.

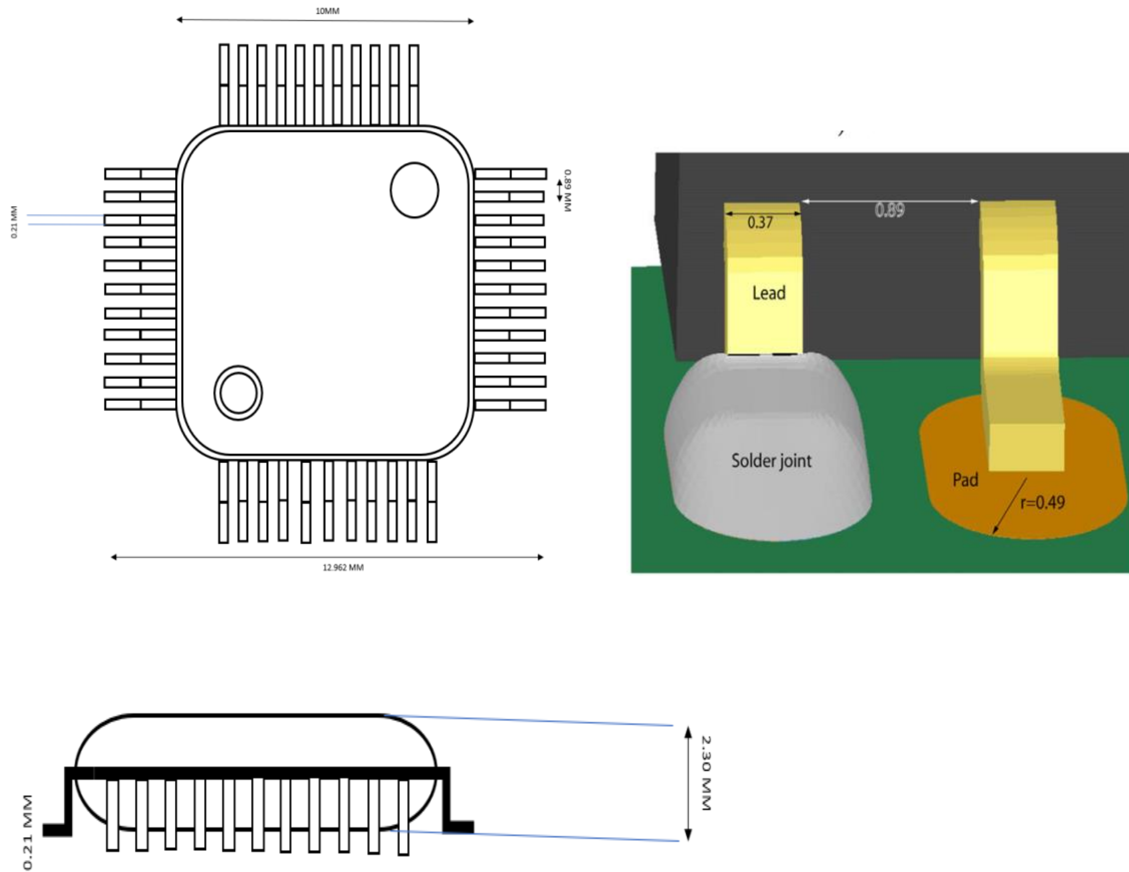


*Figure 17 Package description*

Ten QFP models were created by changing various factors. Geometry of QFP package with different solder shapes, angles and Gullwing leads were modeled using Ansys Design modeler tool.

## 3.5 Material characterization

Material characterization is the most important and the first step in Finite Element Analysis. It is very necessary to know the material properties of various components. Temperature dependent properties such as CTE, Young's modulus and Poisson's ratio are critical in Finite Element analysis. The material properties from experimental data was used in this study [7].

Thermomechanical Analyzer (TMA) was used to get the values of CTE's and glass transition temperatures. Dynamic Mechanical Analyzer (DMA) was used to calculate Young's Modulus and Poisson's Ratio.

### 3.5.1 Thermomechanical Analyzer (TMA)

TMA is a device which measure displacement as a function of temperature, time and force which is applied in a thermal chamber having good temperature range. TMA is widely used to measure in- plane and out-plane CTE of the different boards. To get these properties we cut a sample of 8*8 mm and place it in thermal chamber. The quartz probe in the TMA provide CTE plot.

*Figure 18 Thermomechanical Analyzer*

### 3.5.2 Dynamic analyzer

Dynamic mechanical analyzer is a device used to measure Young's modulus and Poisson's ratio as a function of temperature, time and frequency. In DMA we apply sinusoidal deformation to a sample to get the desired properties. Coefficient of Thermal expansion CTE of the die, die attach, lead frame, were obtained from literature provided by Texas Instruments. for the provided boards.

*Figure 19 Dynamic Analyzer*

Following values for Coefficient of Thermal expansion of the various components were taken from Texas Instruments literature. [10]

*Table 2 Values of CTE*

| **Material** | **CTE (ppm/°C)** | **E (GPa)** |
| --- | --- | --- |
| Die | 2.61 | 131 |
| Die Attach | 64 | 11.8 |
| Lead Frame | 17 | 129 |
| Epoxy Mold | 10.3 | 3 |
| Epoxy die pad | 17 | 129 |
| PCB (62 mil) | α(x,y)=15.5<br>α(z)=39.4 | 15.37 |

Chapter 4

# PARAMETRIC ANALYSIS

## 4.1 Models and Simulation

Finite element analysis was done in two parts. Firstly, models were created in Ansys 18.0 design modeler. Meshing and analysis settings were kept constant for all the models. We wanted to know how much impact is seen on the model by the introduction of power cycle. So, models were put under Accelerated thermal cycle and results were recorded. Later, in the Transient thermal analysis Convective heat transfer coefficient of 23 $W/m^2$. °C was applied to the outer surface of the package. Environment temperature was set such that package temperature does not exceed 125°C.

### 4.1.1 Study 1: Amount of Solder

Firstly, we changed the amount of solder is to be used because it can certainly affect the reliability of electronic package. Lead height is taken to be 0.21mm. So, we came up with three basic designs to understand effect of amount of solder we put on the reliability of solders as well as whole package. In the standard design we kept solder till the mid-section of the lead i.e. at 0.105mm. Subsequently, in the next two models we kept solder till 0.07875mm and 0.1575mm. These models were simulated in Static Structural Analysis under Accelerated thermal cycle for 10800 secs. Environment around the package was set so that it does not exceed 125°C.

1. Plastic Work

Plastic work can be defined as hardening of metal by plastic deformation. It is calculated in Ansys APDL by using following code,

```
/post1 allsel,all
!CALC AVG PLASTIC WORK FOR CYCLE1
set,4,last,1
cmsel,s,botsolder,elem                                ! Not to use space in the name
etable,vo1table,volu
pretab,vo1table
etable,vse1table,nl,plwk
pretab,vse1table
smult,pw1table,vo1table,vse1table
ssum
*get,splwk,ssum,,item,pw1table
*get,svolu,ssum,,item,vo1table
pw1=splwk/svolu              ! Average plastic work

!CALC AVG PLASTIC WORK FOR CYCLE2
set,8,last,1
cmsel,s,botsolder,elem                                ! Not to use space in the name

etable,vo2table,volu
pretab,vo2table
etable,vse2table,nl,plwk
pretab,vse2table

smult,pw2table,vo2table,vse2table

ssum
*get,splwk,ssum,,item,pw2table
*get,svolu,ssum,,item,vo2table
pw2=splwk/svolu              ! Average plastic work

!CALC DELTA AVG PLASTIC WORK
pwa=pw2-pw1

!CALC AVG PLASTIC WORK FOR CYCLE3
set,12,last,1
cmsel,s,botsolder,elem                                ! Not to use space in the name
etable,vo3table,volu
pretab,vo3table
etable,vse3table,nl,plwk
pretab,vse3table
smult,pw3table,vo3table,vse3table
ssum
*get,splwk,ssum,,item,pw3table
*get,svolu,ssum,,item,vo3table
pw3=splwk/svolu              ! Average plastic work

!CALC DELTA AVG PLASTIC WORK
pwb=pw3-pw2
my_dpw=pwb
```

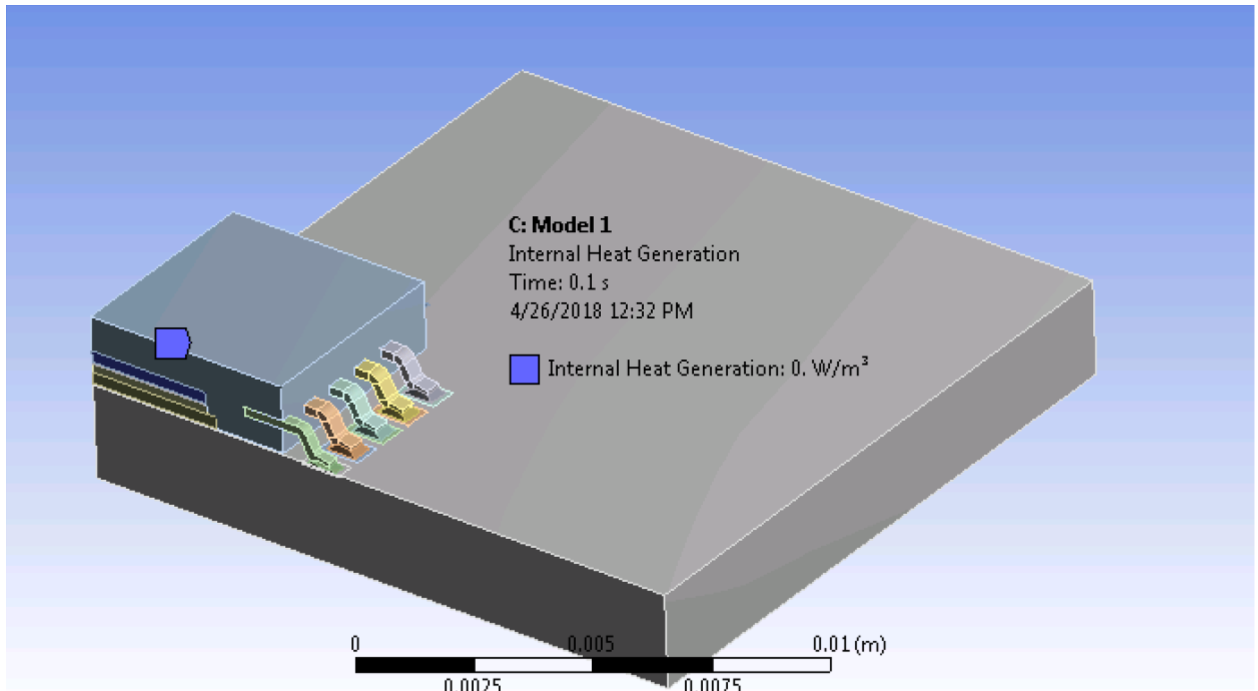


*Figure 20 QFP under consideration.*

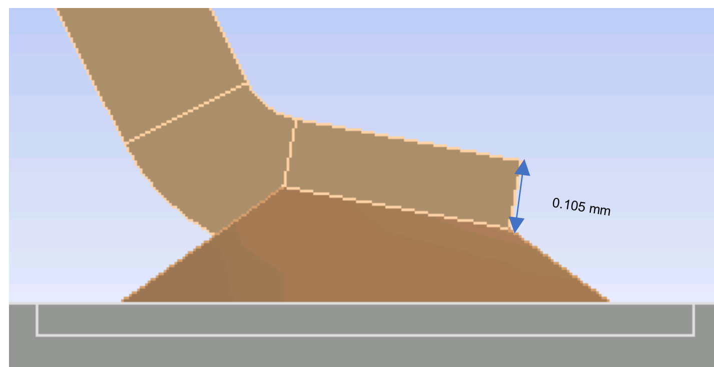


*Figure 21 Model 1*

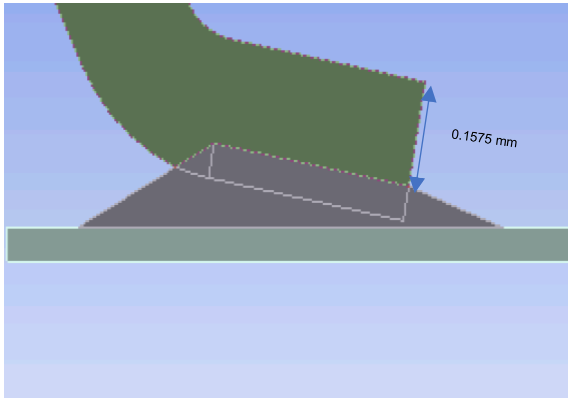


*Figure 22 Model 2*

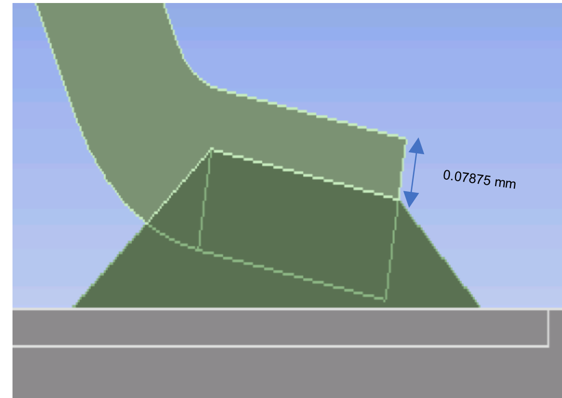


*Figure 23 Model 3*

*Table 3 Solder Volume Analysis*

| Models | Model1 | Model2 | Model3 |
|---|---|---|---|
| Solution | | | |
| Max Stress (Pa) | 2.60E+08 | 2.29E+07 | 3.35E+07 |
| Max Stress Solders (Pa) | 2.15E+07 | 2.17E+07 | 2.21E+07 |
| Max Strain (m/m) | 0.0022196 | 0.0002975 | 0.00021615 |
| max Strain Solders (m/m) | 0.00031561 | 0.00029 | 0.00031452 |
| Strain Energy (J) | 8.80E-07 | 2.41E-08 | 1.97E-08 |
| Total Deformation (m) | 3.93E-05 | 4.36E-08 | 1.07E-07 |

*Table 4 Plastic work comparison*

| Plastic work | 11682 | 10000 | 6933.7 |
|---|---|---|---|

After analyzing results for above three models it is evident that as solder goes on increasing amount of plastic strain accumulated in solders decreases.

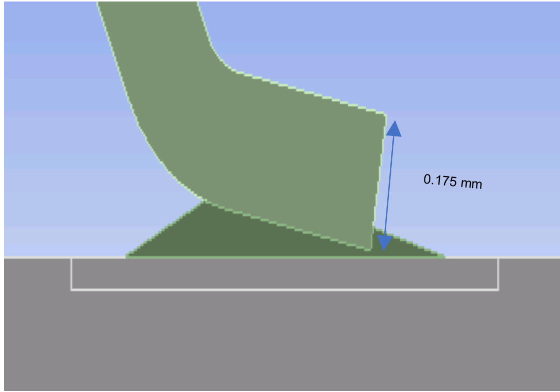


*Figure 24 Model4*

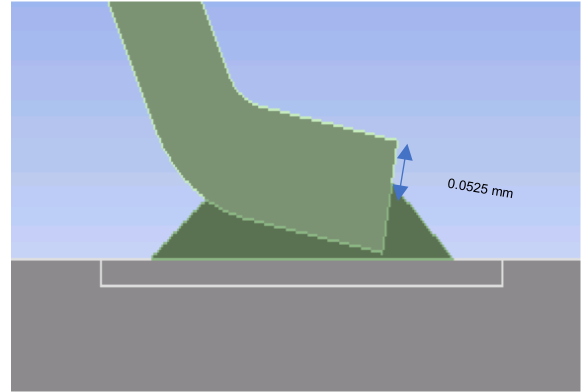


*Figure 25 Model 5*

To clarify these results, we came up with two more models in which we decreased and increased amount of solder as shown in fig…… And they were put under similar loads and boundary condition.

### 4.1.2 Solder volume analysis

Analysis results were retrieved, and we found out that as we decreased the solder plastic work in critical solder went on increasing. Whereas, as solder amount was increased plastic work went down. But other way around as for stress analysis as the solder volume decreased overall maximum stress on the solders as well as on the package.

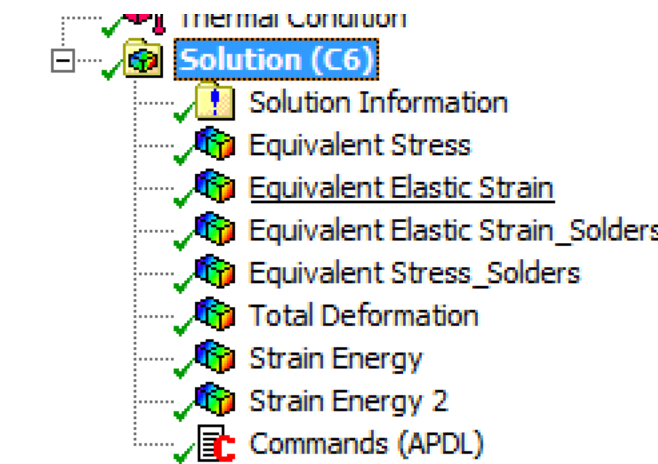


*Figure 26 Ansys solution window*

*Table 5 Solder Volume Analysis 2*

| Models | Model1 | Model2 | Model3 | Model4 | Model5 |
|---|---|---|---|---|---|
| Solution | | | | | |
| Max Stress (Pa) | 4.95E+07 | 2.94E+07 | 2.96E+07 | 5.89E+07 | 5.78E+07 |
| Max Stress Solders (Pa) | 2.03E+07 | 2.13E+07 | 2.04E+07 | 2.20E+07 | 2.06E+07 |
| Max Strain (m/m) | 0.0030674 | 0.00029 | 0.000251 | 0.004978 | 0.0049 |
| max Strain Solders (m/m) | 0.00028 | 0.00029 | 0.000279 | 0.0003044 | 0.000295 |
| Strain Energy (J) | 5.69E-08 | 7.48E-08 | 4.13E-08 | 6.15E-08 | 6.28E-08 |
| Total Deformation (m) | 2.32E-07 | 1.25E-07 | 1.04E-07 | 1.06E-05 | 5.23E-04 |

*Table 6 Plastic Work Comparison*

| MODEL | PLASTIC WORK |
|---|---|
| MODEL 1 | 11682 |
| MODEL 2 | 10000 |
| MODEL 3 | 6933.7 |
| MODEL 4 | 10106 |
| MODEL 5 | 7839.9 |
| | |
| | |

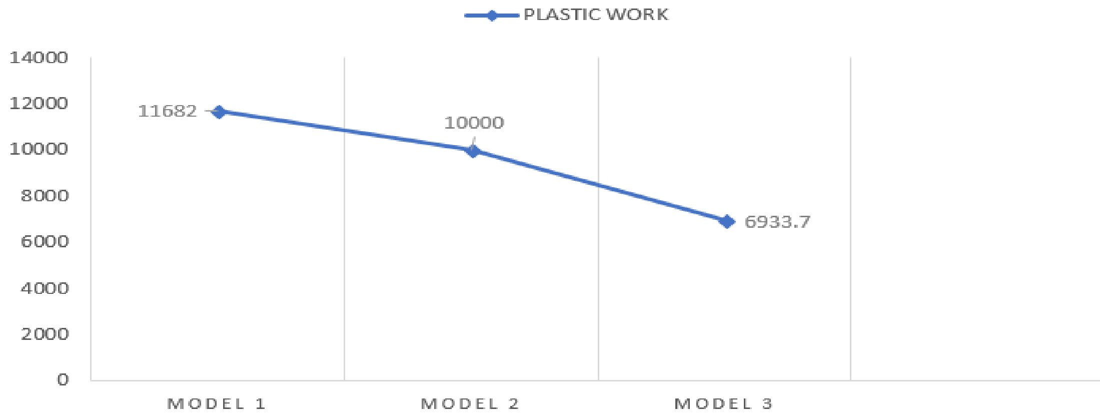


*Figure 27 Plastic work comparison*

As we are using Darveaux methodology we are going to compare the plastic work accumulated in the critical solder. On that basis when solder was kept till 0.07875mm of the height of lead we got minimum plastic work compared to other design. We also increased it above 0.07875mm and found that plastic work increased. Solder volume does have critical effect on the reliability of solders.

### 4.1.3 Study 2: Changing pitch and number of solders

Following the development in knowing the effects of amount of solder we came up with few more models in which number of leads were increased so was pitch decreased. It was done to understand as more and more interconnections to be made possible in an electronic package. These models were simulated under similar conditions.

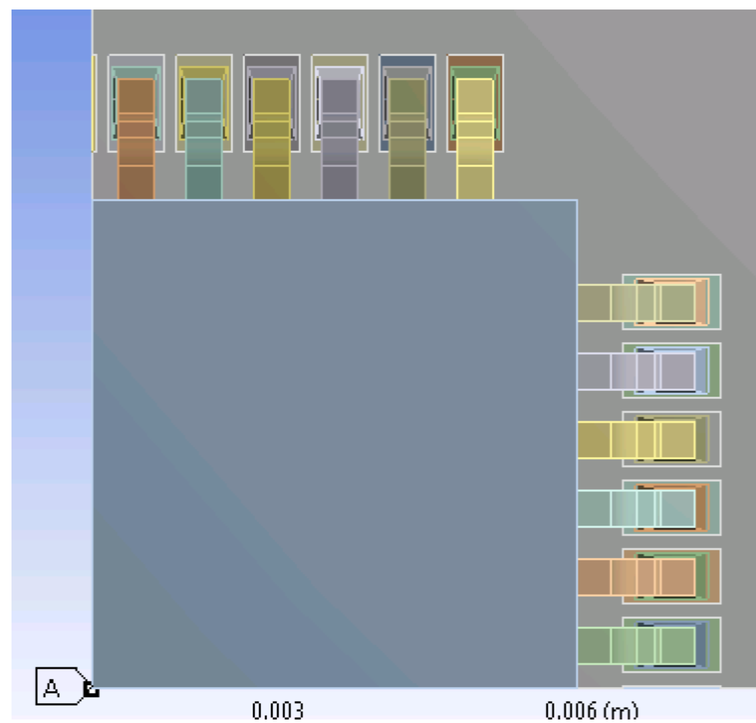


*Figure 28 Increasing number of leads*

### 4.1.4 Analysis results

As number of leads increased plastic work in critical solder from 36 to 44. From which we can conclude that number of leads and pitch are critical while design electronic package. On the other hand minimum changes were seen in the maximum equivalent stress and strain on the package and on the solders.

*Table 7 Analysis results*

| Models | Model1 | Model3 | Model7 |
|---|---|---|---|
| Solution | | | |
| Max Stress (Pa) | 2.60E+08 | 3.35E+07 | 8.35E+07 |
| Max Stress Solders (Pa) | 2.15E+07 | 2.21E+07 | 2.76E+07 |
| Max Strain (m/m) | 0.0022196 | 0.00021615 | 0.0071 |
| max Strain Solders (m/m) | 0.00031561 | 0.00031452 | 0.000362 |
| Strain Energy (J) | 8.80E-07 | 1.97E-08 | 7.40E-08 |
| Total Deformation (m) | 3.93E-05 | 1.07E-07 | 3.55E-04 |
| Plastic work | 11682 | 6933.7 | 10897 |

### 4.1.5 Changing Die Size

Die size was considered on the factors that would have considerable effect on solder and overall package reliability. So, we came up with two more models by increasing and decreasing die size.

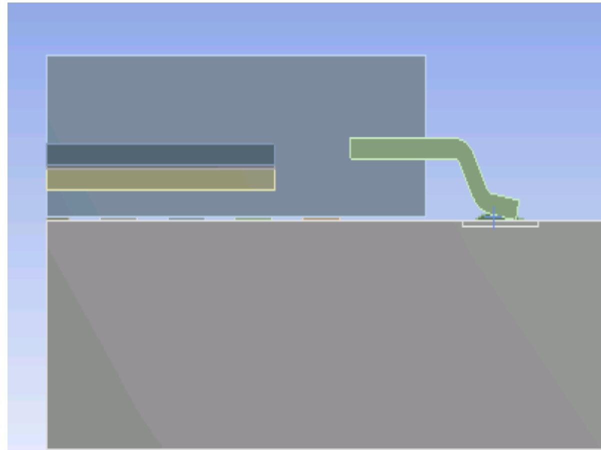

*Figure 29 Decreasing die size*

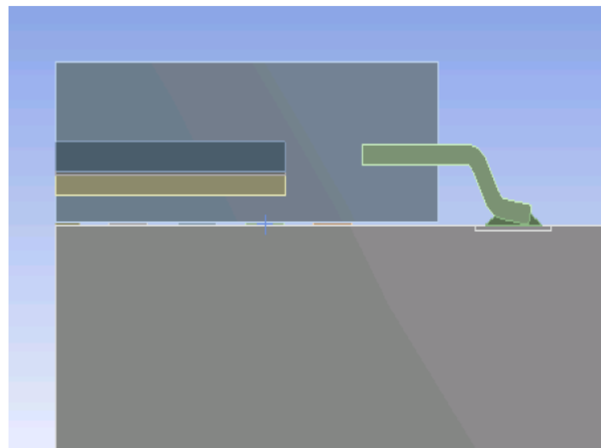

*Figure 30 Increasing Die Size*

*Table 8 Comparison of Model 7 & 8*

| Models | Model8 | | Model9 | |
|---|---|---|---|---|
| Solution | | | | |
| Max Stress (Pa) | 2.21E+08 | | 2.24E+08 | |
| Max Stress Solders (Pa) | 2.10E+07 | | 1.93E+07 | |
| Max Strain (m/m) | 0.0188 | | 0.01923 | |
| max Strain Solders (m/m) | 0.000277 | | 0.0002563 | |
| Strain Energy (J) | 2.54E-05 | | 2.56E-05 | |
| Total Deformation (m) | 0.0001784 | | 3.83E-05 | |
| Plastic work | 17171 | | 11290 | |

Though we can conclude that changing die size has minimum effect on stress and stress values of the package. But as we can see there is rise in the plastic work.

### 4.1.6 Study 3: Introducing power cycle

Lot of research has been carried out till this point where accelerated thermal cycle was used as only load. But as explained above little study has been done considering power cycle. In this section we will first carry out simulation in the transient thermal analysis. Surrounding temperature was to be maintained 125°C so Convective heat transfer coefficient was applied to all the faces of quarter geometry model. Further die is the functional device which when turned on and turned off heats up. Therefore, for internal heat generation Power density of 0.5 W/mm$^3$ was applied on the die.

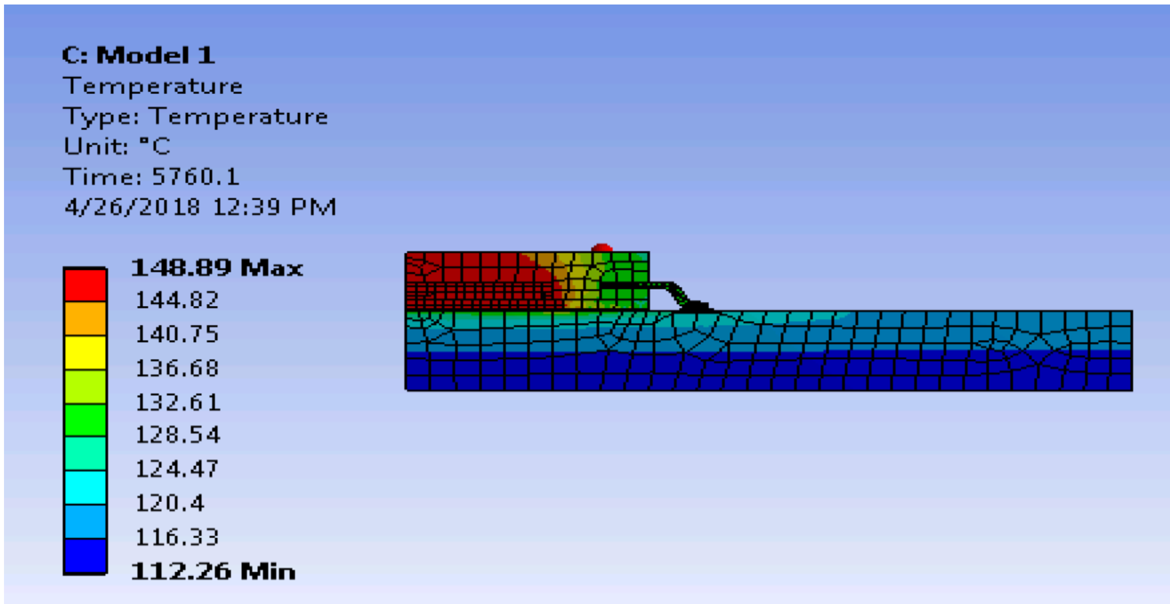


*Figure 31Die heating due to internal heat generation*

The stresses which are resulted from such temperature variations are not similar to what are found in accelerated thermal cycling which has isothermal thermal distribution. But during power cycling as die is the only source of heat so the temperature distribution is not uniform and area around the die

heats up more as shown in fig. Time of one power cycle is 1600 seconds and is applied for 10800 seconds. The power cycling profile is shown in through the plot.

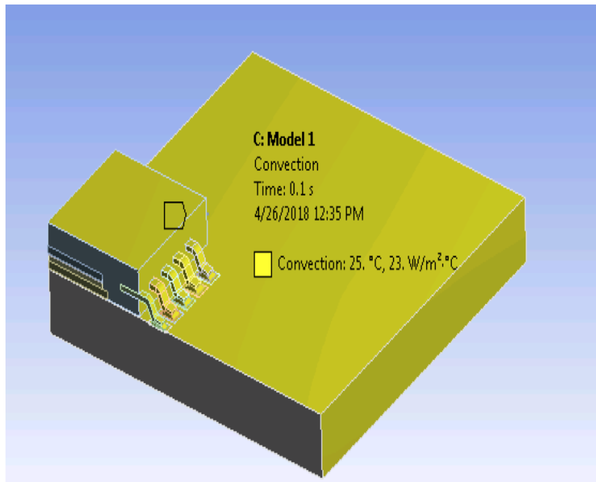


*Figure 32 Convection on the package*

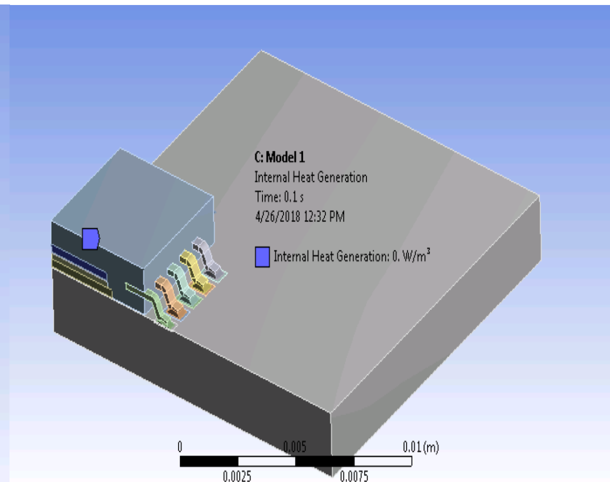


*Figure 33 Internal heat generation*

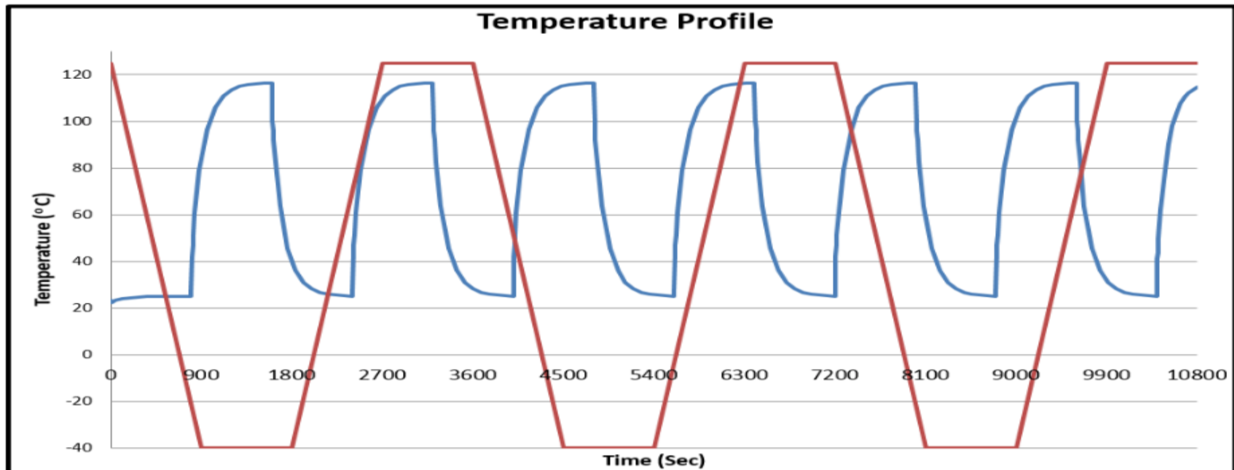


*Figure 34 Combined Load*

The temperature load gathered from the transient thermal analysis is used in static structural analysis. Thermal load obtained from Transient thermal analysis is combined along with Accelerated Thermal Cycle. This load acts as combined load on the package.

### 4.1.7 Combined load analysis

*Table 9 Combined load analysis*

| Models | Model1 | Model2 | Model3 |
|---|---|---|---|
| Solution | | | |
| Max Stress (Pa) | 7.54E+07 | 8.04E+08 | 2.51E+08 |
| Max Stress Solders (Pa) | 5.52E+06 | 6.80E+06 | 8.50E+06 |
| Max Strain (m/m) | 0.00477 | 0.00287 | 0.01896 |
| max Strain Solders (m/m) | 9.75E-05 | 0.0001006 | 0.00012 |
| Strain Energy (J) | 2.75E-07 | 2.44E-07 | 9.66E-06 |
| Total Deformation (m) | 2.24E-05 | 2.30E-05 | 2.87E-05 |
| | | | |

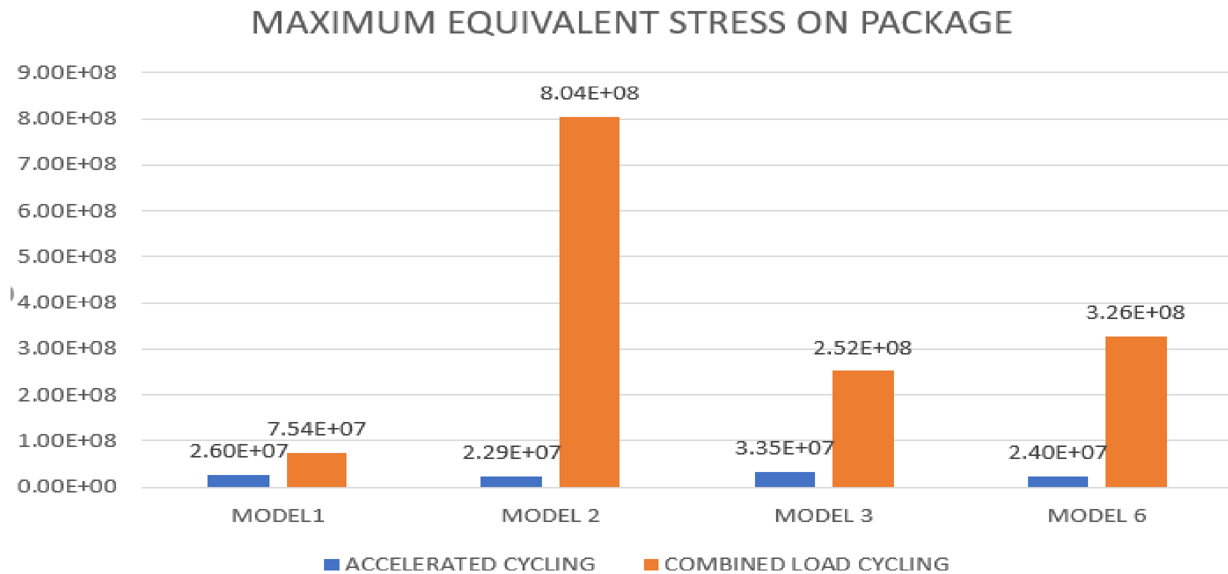


*Figure 35 Maximum Equivalent Stress on the Package*

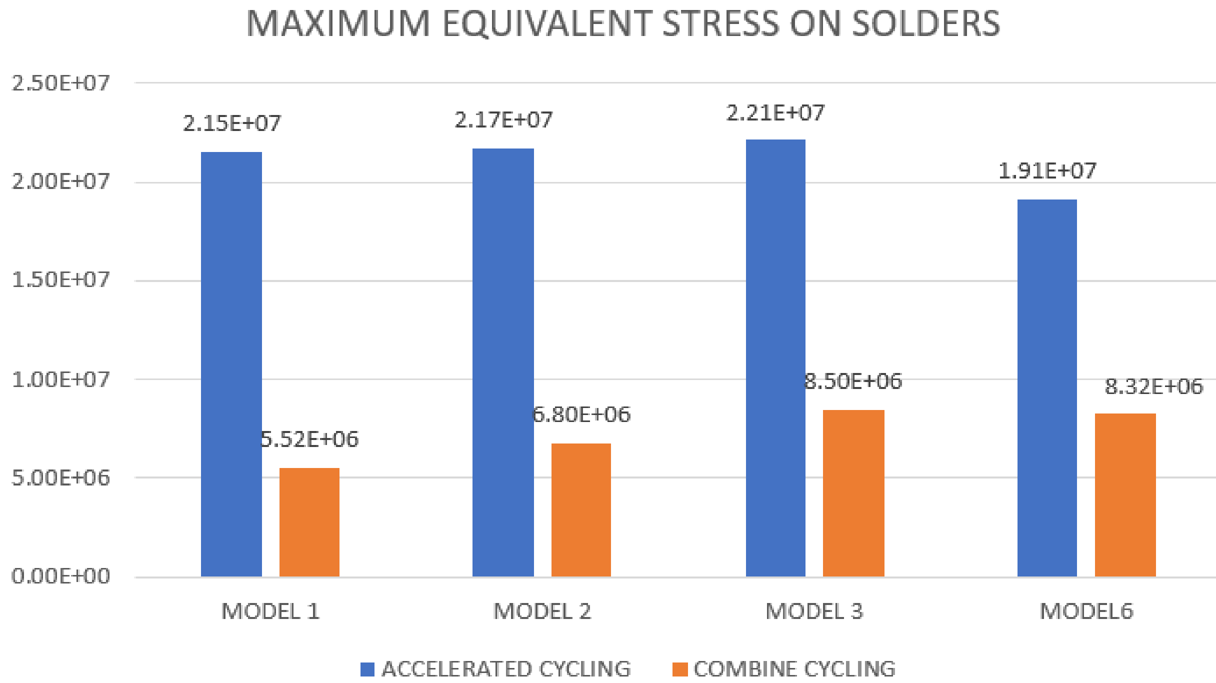


*Figure 36 Maximum equivalent stress on solders*

Results clearly show that overall stress in the package has increased considerably. Also, we can see that Accumulated stress and creep strains in the solder have decreased. This is due to the fact that of the non-uniform temperature distribution from the heating of the die. Plastic work in the solders had minimum change in the package.

Chapter 5

Results and Conclusions

## 5.1 Results

Results that we got made number of good revelations as how to optimize the solder design to get better reliability of overall package. We started off by carrying out analysis in static structural to get the simulation results on the package under accelerated thermal cycling as only load.

Due to coefficient of thermal expansion we see stresses induced in the corner solder joint and we then went on to optimizing the design to understand the effects of various factors and improve the reliability of the package.

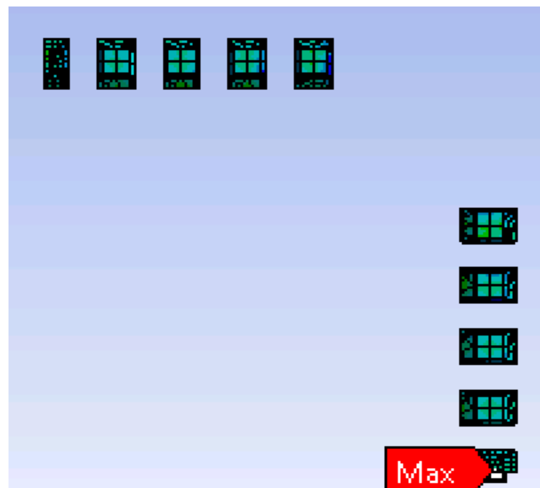


*Figure 37 Stress on solders*

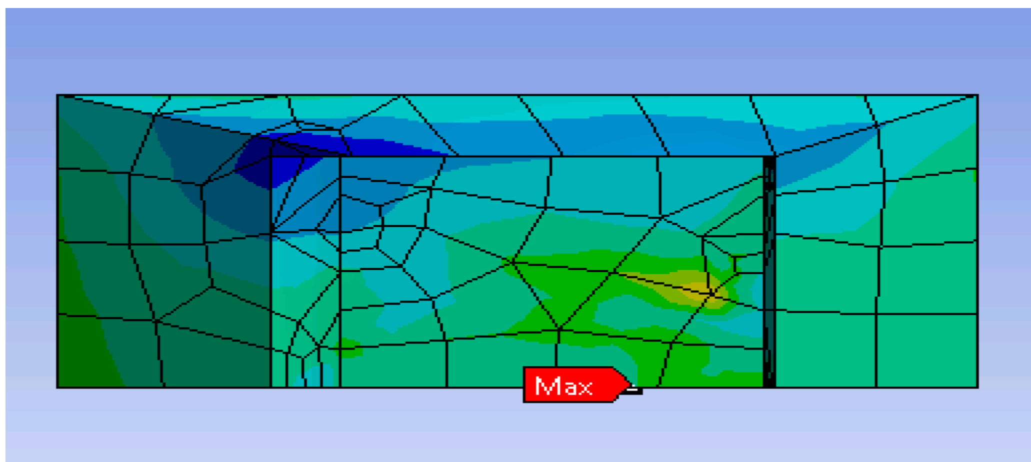


*Figure 38 Corner solder joint*

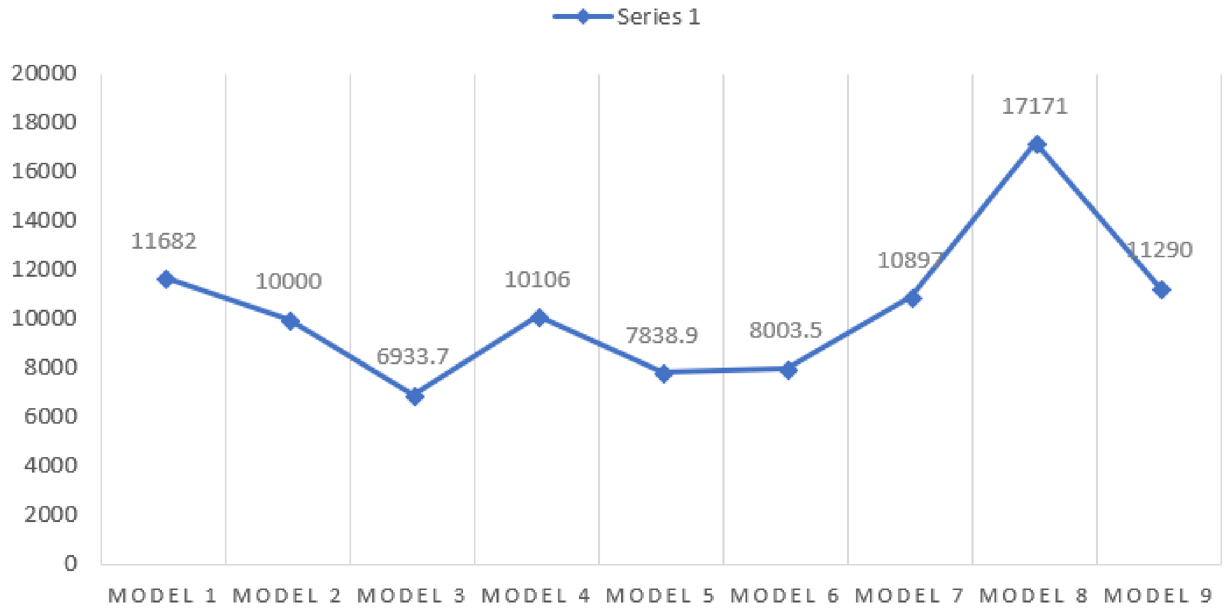


*Figure 39 Comparison of Plastic work*

Carrying out stress and strain analysis we can conclude that under only accelerated thermal cycle (ATC) due to CTE mismatch we get deformation in different rates that causes stress. But when we incorporated power cycle and carried out simulation under combined load, the maximum stress on the package increased considerably. But maximum stress on solders decreased and that is why power cycling load cannot be neglected. Also, we can see that total deformation under combined load is much higher than only under ATC.

## 5.2 Conclusion

Finite element analysis was carried on ten different geometry models to understand the reliability of quad flat package with gullwing leads. Successful parametric analysis was done initially considering only Accelerated thermal cycle as loading condition in Ansys 18.0 incorporating darveaux model by calculating plastic work in all the critical solder joints. To understand visco-plastic behavior of solders we used Anand's model in the Ansys. Major change in the results was seen when we introduced power cycle in the analysis of all the models.

Also, further study was done by changing number of leads, increasing and decreasing die sizes and changing pitch of the leads. We can conclude that when combined load acts the stresses acting on the package are much higher otherwise. But it also reveals that the maximum stress on the solders decrease and more study has to be done on understanding why. We tried increasing corner thickness of the solders and providing fillets to get more reliable designs. Amount of volume of solder is important factor while making design considerations. When solder is kept till lead height of 0.07875mm we get least amount of plastic work accumulated. As volume of solder went down or up from this point so did plastic work.

This study comes up with design optimization of solder joints of quad flat package under different loading conditions and effects of change in various factors leading to package reliability. In future, electronic packages are going to become smaller and compact and so will solders and their properties are going to be more intricate and complex. So, correct finite element modeling and analysis is must for robust results and effective reliability.

## 5.3 Summary

Material characterization of different components was successfully done using TMA and DMA to find Young's Modulus, Coefficient of Thermal Expansion and Poisson's Ratio which are later used in FEA analysis. Parametric analysis was performed to determine design parameters critically affecting QFP reliability on this board. Power cycle does have considerable effect in fatigue modelling and shouldn't be neglected. Study of maintaining correct solder volume and increasing edge thickness makes QFP model more reliable.

## 5.4 Future work

- More work has to be carried on understanding behavior of solders under combined load as to why stresses induced in them drop when power cycle is introduced.
- These are only analysis results and need to be validated by experimental data.
- SAC305 was used as solder material, other new materials should be used and see the difference in analysis.
- Lead was considered to be of copper where new development suggests plating them with Au, Ni and Sn gives better results.
- Study the effect of humidity on reliability of Quad flat package as more modeling consideration.

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# Biographical Statement

Pranav Nikam received his bachelor's degree in Mechanical Engineering from University of Mumbai, India. He pursued his Master's in Mechanical Engineering at University of Texas at Arlington from Fall 2016. He joined the Electronics MEMS & Nanoelectronics Systems Packaging Center (EMNSPC) under Dr. Dereje Agonafer in 2017, this soon generated interest in the field of reliability of electronic packages for him. He has actively submitted two papers on reliability of QFP and QFN packages at IMECE2018. He graduated from The University of Texas at Arlington with master's Degree in mechanical engineering in May 2018.