

STRUCTURAL AND ELECTRICAL CHARACTERIZATION OF SINGLE  
CRYSTALLINE  $\text{SrZr}_x\text{Ti}_{1-x}\text{O}_3$  THIN FILMS ON GERMANIUM

by

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Presented to the Faculty of the Graduate School of Electrical Engineering

The University of Texas at Arlington in Partial Fulfillment

for the Degree of

DOCTOR OF PHILOSOPHY

THE UNIVERSITY OF TEXAS AT ARLINGTON

May 2017

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## Acknowledgements

I am sincerely thankful to my advisors, Professor Kambiz Alavi and Dr. Joesph H Ngai, for their continued support and contribution in the development of my research. Their clear vision and expert guidance has helped me stay on track and made successful completion of my work possible. I would also like to express my gratitude to my thesis committee members Dr. Alex Weiss, Dr. Robert Magnusson, and Dr. Kamisetty R. Rao. I would like to thank my parents Homa and Alireza, my brother Milad and my sister Mahkam for their constant encouragement and support without which this work would have not been possible. I would like to thank all my UT Arlington and Texas friends specially, Pedram, Kourtlyn, Valeriia and their families for friendship and emotional support.

Finally, but really foremost, I thank the Lord, for the strength, intelligence, perseverance and wisdom he has given me to realize my dreams and perform this work.

April 18, 2017

## Abstract

# STRUCTURAL AND ELECTRICAL CHARACTERIZATION OF SINGLE CRYSTALLINE $\text{SrZr}_x\text{Ti}_{1-x}\text{O}_3$ THIN FILMS ON GERMANIUM

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The University of Texas at Arlington, 2017

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The epitaxial growth of crystalline oxides on semiconductors provides a pathway to introduce new functionalities to semiconductor devices. Key to coupling crystalline oxides to semiconductors electrically, to realize functional behavior, is controlling the manner in which their bands align at the interfaces. This document reports on the three research projects on Crystalline Oxide/Semiconductor heterostructures. In the first project we applied principles of band-gap engineering traditionally used at heterojunctions between conventional semiconductors to control the band offset between a single crystalline oxide and a semiconductor. Reactive molecular beam epitaxy is used to realize atomically abrupt and structurally coherent interfaces between  $\text{SrZr}_x\text{Ti}_{1-x}\text{O}_3$  and Ge, in which the band-gap of the former is increased with increasing Zr content  $x$ . Structural and electrical characterization of  $\text{SrZr}_x\text{Ti}_{1-x}\text{O}_3$ -Ge heterojunctions for

$x = 0.2$  to  $0.75$  is performed and reported. The results demonstrate that by increasing the Zr content the band offset between the oxide and semiconductor can transition from type-II to type-I. In the second project ferroelectric materials integrated on semiconductors were particularly studied, which could lead to low-power field-effect devices that can be used for logic and memory. Essential to realizing such field-effect devices is the development of ferroelectric metal-oxide-semiconductor (MOS) capacitors, in which the polarization of a ferroelectric gate is coupled to the surface potential of a semiconducting channel. Here we demonstrate that ferroelectric MOS capacitors can be realized using single crystalline  $\text{SrZr}_x\text{Ti}_{1-x}\text{O}_3$  ( $x = 0.7$ ) that has been epitaxially grown on Ge. We find that the ferroelectric properties of  $\text{SrZr}_x\text{Ti}_{1-x}\text{O}_3$  are exceptionally robust, as gate layers as thin as 5 nm corresponding to an equivalent-oxide-thickness of just 1.0 nm exhibit a  $\sim 2$  V hysteretic window in the capacitance-voltage characteristics. The development of ferroelectric MOS capacitors with ultrathin nanoscale gate thicknesses opens new perspectives for electronic devices. Finally, in the third project the interface trap density of the thin film  $\text{SrZr}_x\text{Ti}_{1-x}\text{O}_3$  on Ge was studied and it was shown that the interface trap density of such structures can be dependent to the history of the junction and polarization state.

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## List of Tables

Table 1-1 List of performed characterization by collaborators. **Error! Bookmark not defined.**

## List of abbreviations

AFM	Atomic force microscopy
CB	Conduction band
C-V	Capacitance-Voltage
DFT	Density functional theory
HAADF	High-angle annular dark-field imaging
PFM	Piezo response force microscopy
PNR	Polar Nano region
PUND	Pulse Up and Down method
STEM	Scanning transmission electron microscopy
VB	Valance band
XRD	X-ray diffraction

## Chapter 1

### Introduction

#### 1-1 Perovskite structure and property

Perovskite structured oxides in a form of  $(ABO_3)$  show many intriguing properties. In particular, the epitaxial growth of multifunctional oxides on semiconductors has opened a pathway to introduce new functionalities for semiconductor device technologies. Specifically, ferroelectric materials integrated on semiconductors could lead to low power field effect devices that can be used for logic or memory.

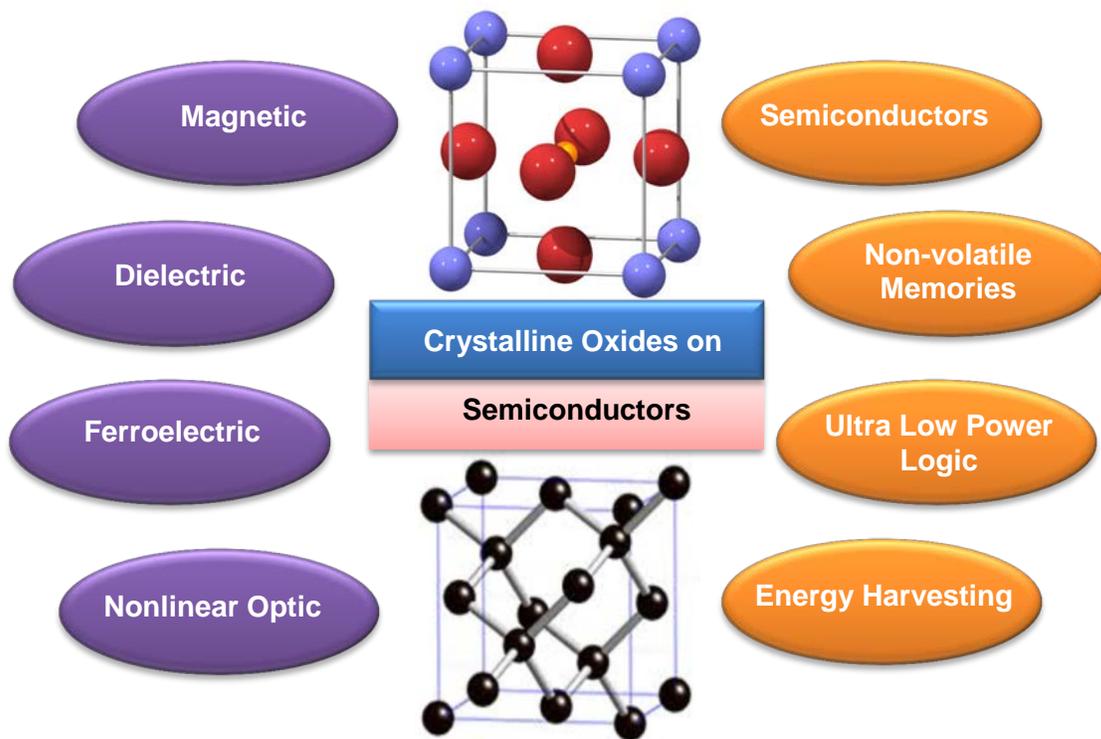


Figure 2-1 Perovskite  $ABO_3$  on semiconductor. Left: fascinating properties of oxides. Right: possible applications.

### *1-2 Critical problems for implementation of oxides on semiconductor*

Essential to realizing such field-effect devices is the development of ferroelectric metal-oxide-semiconductor (MOS) capacitors. A challenge for achieving such devices includes:

- a) Continuity in electric displacement (smaller interface traps and wider hysteresis width).
- b) Requirement of type-I band offset for MOS capacitor.
- c) Difficulty in scaling ferroelectric layer (ferroelectricity is weakened by thickness reduction).

In this research, we were successful to overcome these challenges. First, we studied the properties of the single crystalline  $\text{SrZr}_x\text{Ti}_{1-x}\text{O}_3$  that has been epitaxially grown on Ge. This study showed that the band-gap of the former is enhanced with variation of the Zr content  $x$ .

Electrical characterization of  $\text{SrZr}_x\text{Ti}_{1-x}\text{O}_3$ -Ge heterojunctions for  $x = 0.2$  to  $0.75$  were studied through Capacitance-Voltage (CV) and Current-Voltage (IV) measurements. Structural and surface characterizations were performed by utilizing X-ray diffraction (XRD), STEM and AFM techniques. Band gap alignments were determined by core-level and valence band X-ray photoemission spectroscopy. It was found that the band offset can be tuned from type-II to type-I. This was a significant discovery since the type-I band offset provides a platform to integrate the dielectric, ferroelectric, and ferromagnetic functionalities of oxides on semiconductors for device applications. These results demonstrated that band-gap engineering can be used to realize functional semiconductor–crystalline oxide heterojunctions.

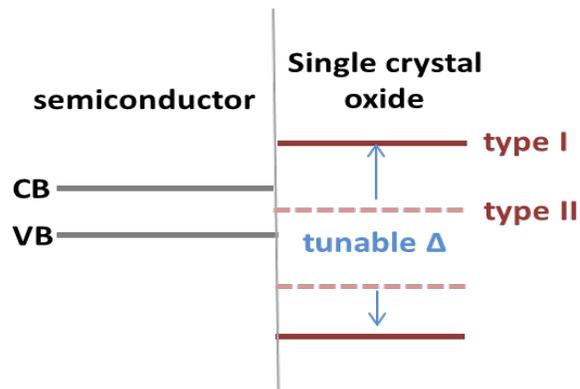


Figure 1-3 Illustration of the bandgap transition.

In a later study we demonstrated that ferroelectric MOS capacitors can be realized using single crystalline  $\text{SrZr}_x\text{Ti}_{1-x}\text{O}_3$  ( $x = 0.7$ ) that has been epitaxially grown on Ge. CV and Pulse Up and Down (PUND) measurements performed to study the hysteresis behavior of the capacitance and showed the difference of polarization in up and down ferroelectric states. Piezo Force Microscopy (PFM) also confirms butterfly-like hysteresis and  $180^\circ$  phase shift in the amplitude and phase response.

STEM imaging reveals evidence of non-uniform atom column displacements in the films, which are consistent with Polar-Nano Regions (PNRs). CV measurements at higher temperatures also confirm ferroelectric relaxor behavior to be the origin of ferroelectricity in SZTO. DFT modeling showed that existence of non-centrosymmetric displacements of B-site cations relative to the A-site sub-lattice is the origin for formation of PNRs. STEM imaging showed the magnitude and direction of Zr/Ti column displacement.

Ferroelectric characterization of thin film  $\text{SrZr}_x\text{Ti}_{1-x}\text{O}_3$  on Germanium showed that the gate layers as thin as 5 nm (corresponding to an equivalent-oxide-thickness of 1.0 nm) with  $\sim 2$  V hysteretic window can be achieved. The development of

ferroelectric MOS capacitors with nanoscale gate thicknesses opens new pathways for Nano-electronic devices. Finally, we investigated the interface trap density on ferroelectric oxide-semiconductor interface. This study is showed that the interface trap density is as low as  $10^{13} \text{ eV}^{-1}\text{cm}^{-2}$  and it is also different in up and down state. As far as we know this is the first study that shows the dependence of interface trap density to the history of junction.

### *1-3 Statement of originality and structure of the dissertation*

The work contained in this thesis has not been previously submitted for a degree or diploma at any other higher education institution. Much of the writing appearing in Chapters 2 and 3 are derived from manuscripts written and edited predominantly by my thesis advisor, Dr. Joseph Ngai.

This dissertation is arranged in three next chapters: First, the research on bandgap engineering is shown in chapter two. Growing single crystalline films were mostly performed by Kamyar Ahmadi-Majlan, and I was mostly involved in XRD, CV and IV measurements and characterization.

Second, investigation on ferroelectricity is shown in chapter three. The idea of this project formed when I found the ferroelectric CV hysteresis, while performing the measurements for the project one. STEM imaging performed by Everett D. Grimley and James M. Lebeau, PFM characterization performed by Zhiyong Xiao and Xia Hong, DFT simulation where performed by Peter V. Sushko and Phuong-Vu Ong and guidance and support from Scott A. Chambers. More detailed list of collaborators participation is shown in table 1-1.

Third, deeper investigation on interface trap densities and the effect of polarization and history of junction on determination of the interface trap density, which is importance for possible device application, is shown in chapter four.

Table 2-1 List of performed characterization by collaborators.

Measurement	Fact studied	Collaboration
RHEED	In-situ growth control	UTA
CV and IV	Electrical properties	UTA
PUND	Ferroelectric polarization	UTA
AFM	Surface roughness	UTA
PFM	Ferroelectric properties, polarization stability	University of Nebraska
XRD	Structural properties	UTA
STEM	PNR, Structural properties	North Carolina State University
XPS, XRD, EELS	Bandgap, Structural properties	Pacific Northwest National Laboratory
DFT	Understanding of the origin ferroelectricity	Pacific Northwest National Laboratory

## Chapter 2

### Bandgap engineering at crystalline oxide interface

#### 2-1 Introduction

The integration of multifunctional oxides on conventional semiconductors enables new functionalities to be introduced to semiconductor devices.[1-2] Perovskite structured oxides ( $ABO_3$ ) are of particular interest since a broad range of material behaviors can be realized by simply tuning the stoichiometry of the A- and B-site ions. The ability to realize a broad range of material behaviors within a single structure is advantageous for epitaxial integration. In this regard, McKee *et al.* pioneered the growth of single crystalline  $SrTiO_3$  on Si(100) with atomically abrupt and structurally coherent interfaces.[3] Since then,  $SrTiO_3$  on Si(100) has been utilized as an epitaxial platform to monolithically integrate multifunctional crystalline oxides on semiconductors.[4–13]

Despite the ability to monolithically integrate crystalline oxides on semiconductors, electrically coupling the properties of the former with the latter to realize functional behavior has proven challenging. One of the principal reasons is that  $SrTiO_3$  is limited in its ability to act as an electrical platform for coupling oxides to semiconductors, despite being an excellent epitaxial platform. The band alignment between  $SrTiO_3$  and Si, Ge, and GaAs is type-II, namely, the conduction (valence) band of the  $SrTiO_3$  is below the conduction (valence) band of the semiconductor.[14–16] To couple dielectric, ferroelectric and ferromagnetic properties of oxides with semiconductors, a platform with a type-I band offset in which the conduction (valence) band of the oxide is above (below) the conduction (valence) band of the semiconductor is needed. For example, crystalline  $SrTiO_3$  was extensively explored as a gate

dielectric on Si due to the low interface trap densities and high dielectric constant that could be achieved through epitaxial growth.[17,18] However, the type-II band alignment gave rise to excessive leakage currents that limited the effectiveness of crystalline SrTiO<sub>3</sub> as a gate dielectric.[17,19] Consequently, the introduction of an intermediary layer of rocksalt structured AeO (Ae = Sr, Ba) between the Si and SrTiO<sub>3</sub> was necessary to reduce charge leakage.[9,11] Similarly, ferroelectric BaTiO<sub>3</sub> has been epitaxially grown on Si and Ge to explore the development of a non-volatile, ferroelectric field-effect transistor.[4,6,8,10-12] However, the near alignment of the conduction bands between BaTiO<sub>3</sub> and Si or Ge gives rise to leakage currents that prevent the polarization of the former to maintain accumulation or depletion in the latter. [12] Thus, controlling band alignments between crystalline oxides and semiconductors is critical to coupling their properties at interfaces. For compound III-V semiconductors, the control of band alignments and band gaps, i.e. band-gap engineering, has led to the development of a range of device technologies.[20] Here we apply principles of band-gap engineering, namely, band-gap enhancement through control of stoichiometry, to manipulate the band alignment between a semiconductor and a crystalline perovskite oxide. Reactive oxide molecular beam epitaxy (MBE) is utilized to create heterojunctions between single crystalline SrZr<sub>x</sub>Ti<sub>1-x</sub>O<sub>3</sub> (SZTO) and Ge, in which the band-gap of the former is enhanced through Zr content x.[21] We show that atomically abrupt and structurally coherent interfaces between SZTO and Ge can be achieved through careful control of kinetic and thermodynamic conditions during deposition. A type-I band offset is manifested through current-voltage (I-V) and capacitance-voltage measurements (C-V), in which the former shows significantly reduced gate leakage with Zr content, and the latter indicates that inversion on p-type

Ge can be achieved. High-resolution core-level and valence band x-ray photoemission spectroscopy measurements verify and quantify the type-I offset that is achieved for high Zr content  $x$ . These results demonstrate that band-gap engineering can be exploited to realize functional semiconductor crystalline oxide heterojunctions. SZTO provides a high- $k$  perovskite structured electrical platform for the integration of dielectric, ferroelectric and ferromagnetic functionalities of oxides onto semiconductors.

### 2-2 Growth and Physical Structure

Crystalline SZTO films were grown on p-type Ge (100) wafers ( $\rho \approx 0.02 \Omega\cdot\text{cm}$ ) in a custom MBE chamber. Figure 2-1 shows reflection high energy electron diffraction (RHEED) images obtained at various stages of growth.

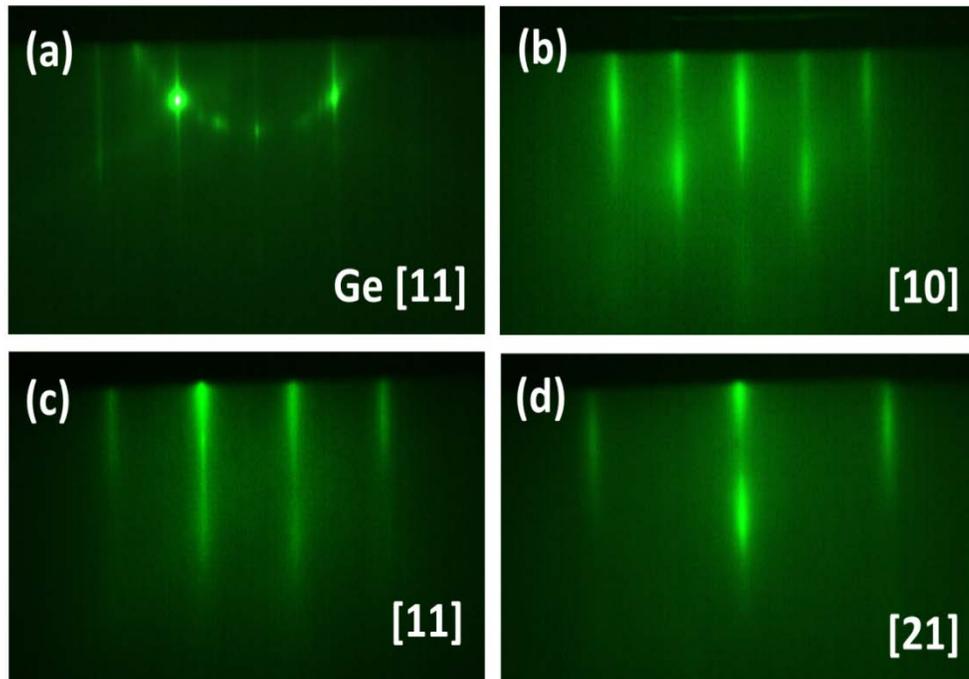


Figure 2-1 RHEED of SZTO ( $x = 0.7$ ) on Ge. (a) After 0.5 monolayers of Sr, showing an unusual reconstruction. (b) 38 unit-cell thick SZTO on Ge taken along [10] and (c) [11] and (d) [21] directions.

A half monolayer (ML) of Sr metal was deposited on a clean Ge (100) surface, resulting in the disappearance of the  $2 \times$  structure associated with the dimerized Ge surface and the emergence of a more complicated reconstruction shown in Figure 2-1(a). The reconstruction we observe at 0.5 ML Sr coverage is consistent with the  $9 \times$  structure observed in previous studies.[22] An initial, 2.5 unit-cell (u.c) thick layer of amorphous SZTO was deposited at room temperature and subsequently crystallized at high temperature. The perovskite unit-cell of SZTO is rotated  $45^\circ$  with respect to the diamond-cubic lattice of Ge, i.e. the registry is  $(001)[100]\text{SZTO} // (001)[110]\text{Ge}$ . Additional layers of crystalline SZTO were deposited until 38 u.c (~15 nm) thick films were obtained. Figure 2-1 (b), (c) and (d) shows RHEED images of a typical SZTO film along the of the [10], [11] and [21] directions, respectively. A series of films with nominal Zr content ranging from  $x = 0.2$  to 0.75 were grown.

X-ray diffraction (XRD) measurements confirm single crystalline growth of SZTO on Ge. Figure 2-3(a) shows survey scans of SZTO films of various Zr content. The unit-cell expands along the c-axis with increasing Zr, as indicated by a shift in the (002) peak that is shown and summarized in Figure 2-3(b) and Figure 2-3(c), respectively. The surfaces of films of higher Zr content, which are better lattice matched to Ge, are typically smoother than films with less Zr, as evidenced by enhanced finite thickness fringes in the case of the former. Imaging of the films of higher  $x$  using atomic force microscopy quantifies the surface roughness  $< 1$  nm, as shown in Figure 2-2. Similarly, the full-width-at-half-max (FWHM) of rocking curves taken on our films are generally narrower for higher  $x$ , ranging from  $\Delta\omega \approx 0.390$  to  $\Delta\omega$

$\approx 0.650$ . The films remain largely strained to the Ge substrate as shown in the direct space map of Figure 2(d) of a  $x = 0.65$  film. Since the perovskite unit-cell of SZTO is rotated  $45^\circ$  with respect to the diamond-cubic unit-cell of Ge, the lattice parameters of the former have been multiplied by  $\sqrt{2}$  to enable comparison on the same plot.

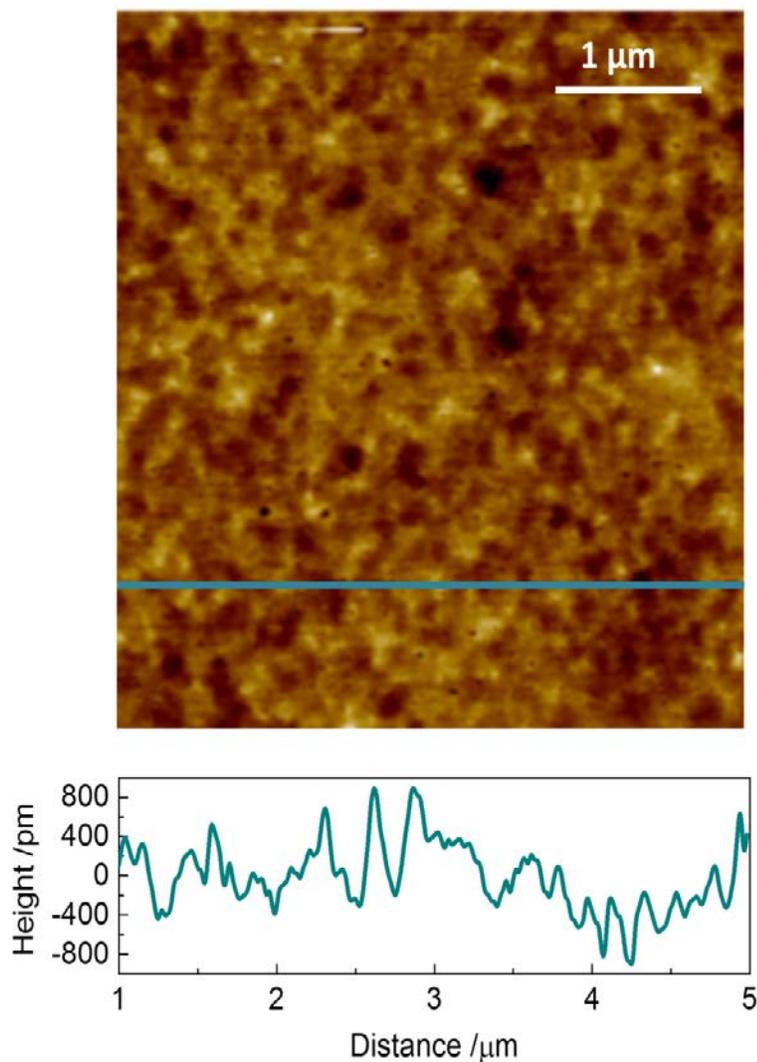


Figure 2-2 Atomic force microscopy image of a typical SZTO-Ge sample ( $x = 0.70$ ) showing surface roughness that is less than 1 nm.

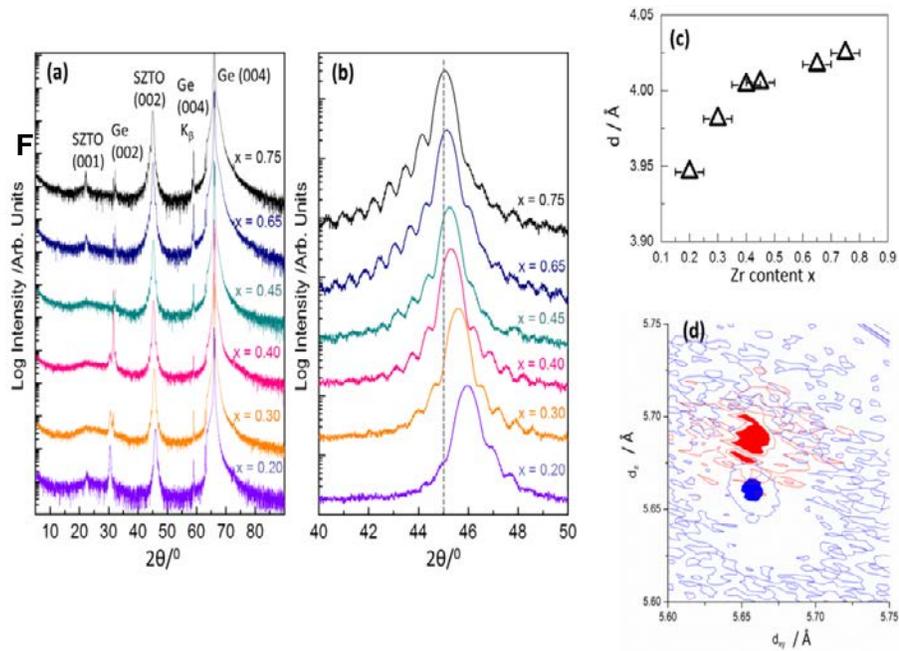


Figure 2-3 X-ray analysis of the film (a) Survey scan of SZTO-Ge heterojunctions for various  $x$ . (b) A shift in the (002) peak is observed with increasing Zr content indicating enhancement of the out-of-plane lattice constant as summarized in (c). (d) Direct-space map of a  $x = 0.65$  SZTO-Ge heterojunction.

Scanning transmission electron microscopy (STEM) measurements provide atomic scale images of the film and interfacial structure between SZTO and Ge. Figure 2-4(a) is a high-angle annular dark field (HAADF) image of a  $x = 0.70$ , showing epitaxial registry of the SZTO with the underlying Ge substrate. Particularly noteworthy is the abruptness of the heterojunction, with no extended interfacial layers comprised of amorphous GeO<sub>2</sub>.

The alternating A and B site planes that comprise the perovskite structure is particularly clear due to the closely matched atomic masses of Sr and Zr. Electron energy loss spectroscopy line scans (STEM-EELS) along the [001] direction across the

interface corroborate the abruptness of the junction shown in the HAADF image. The distribution of Ti, O and Ge, which are retrieved by integrating the intensity of each EELS spectrum, indicates the thickness of the transition layer is less than 1 nm, as shown in Figure 2-4(b).

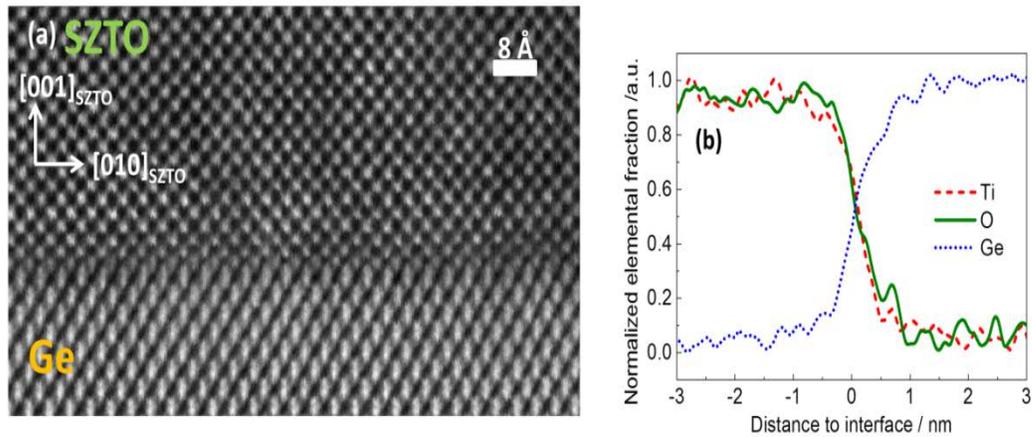


Figure 2-4 STEM and EELS analysis (a) STEM characterization of the interface between crystalline SZTO  $x = 0.70$  and Ge (100). The interface between SZTO and Ge is atomically abrupt and structurally coherent. (b) EELS line scan across interface along  $[001]$  direction, showing elemental fraction of Ti, O and Ge.

### 2-3 Electrical Characterization

The effect of Zr substitution in SZTO on the band alignment at the interface can be seen in measurements of charge leakage through the heterojunctions. Figure 2-5 shows current-voltage I-V measurements through the SZTO-Ge heterojunctions, where the bias

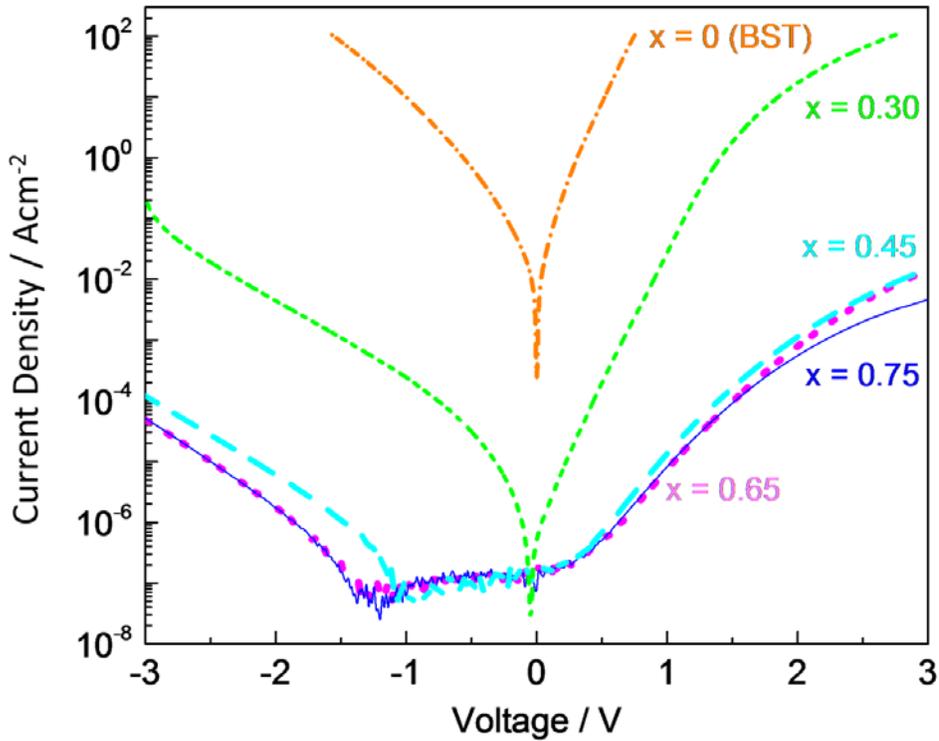


Figure 2-5 I-V characteristics of SZTO-Ge and BST-Ge heterojunctions. SZTO-Ge heterojunctions exhibit significantly less leakage than BST-Ge heterojunctions, consistent with the presence of a conduction band offset.

is applied to a Ni electrode deposited on top of the SZTO. To demonstrate the effect of Zr substitution in creating a band offset, I-V measurements of a 15 nm thick  $\text{Ba}_{0.4}\text{Sr}_{0.6}\text{TiO}_3$  (BST) film is also shown. The substitution of Ba for Sr reduces lattice mismatch with Ge but has little effect on the band-gap or offset. The SZTO-Ge heterojunctions exhibit leakage current that is orders of magnitude less than the BST-Ge heterojunction, consistent with the presence of a type-I band offset.

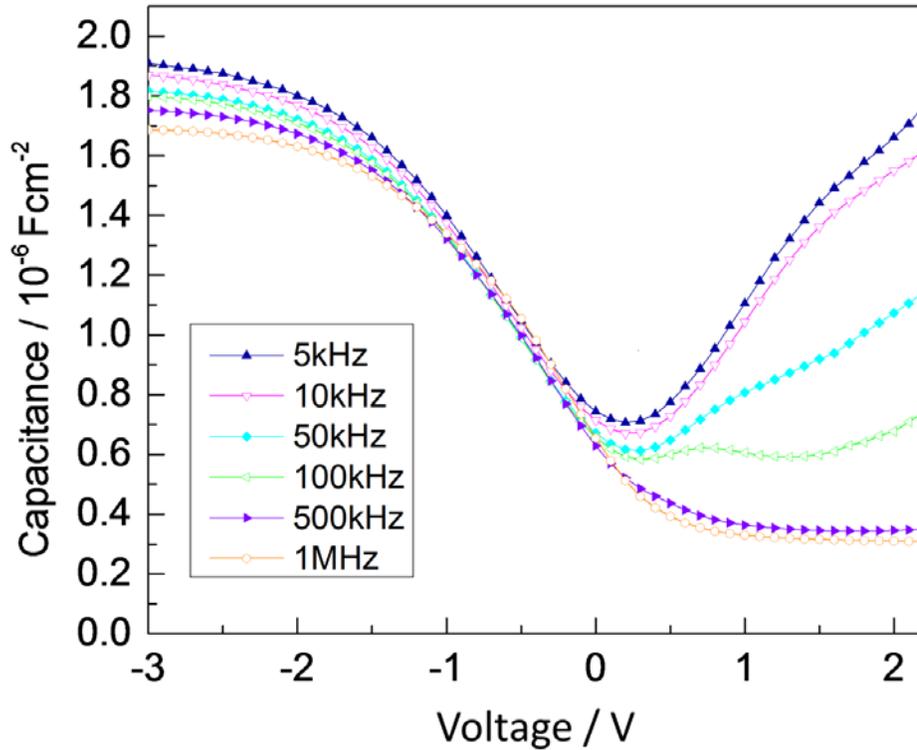


Figure 2-6 C-V characteristics of SZTO-Ge heterojunctions (x = 0.70)

The asymmetric behavior of the measured I-V curve as shown in Figure 2-5 is due to the difference in barrier height from top Ni electrode to oxide in comparison to the lower barrier height from Ge to oxide in reverse and forward bias respectively.[17] The current was measured by sweeping the voltage from 0V to +3V and again from 0V to -3 volt and averaged over 10 different junctions to reduce noise and remove the ferroelectric memory effect as much as possible. Conduction mechanism is investigated by finding a piecewise fit to the I-V curve above the detection noise level for positive and negative bias by using equation 2-1.

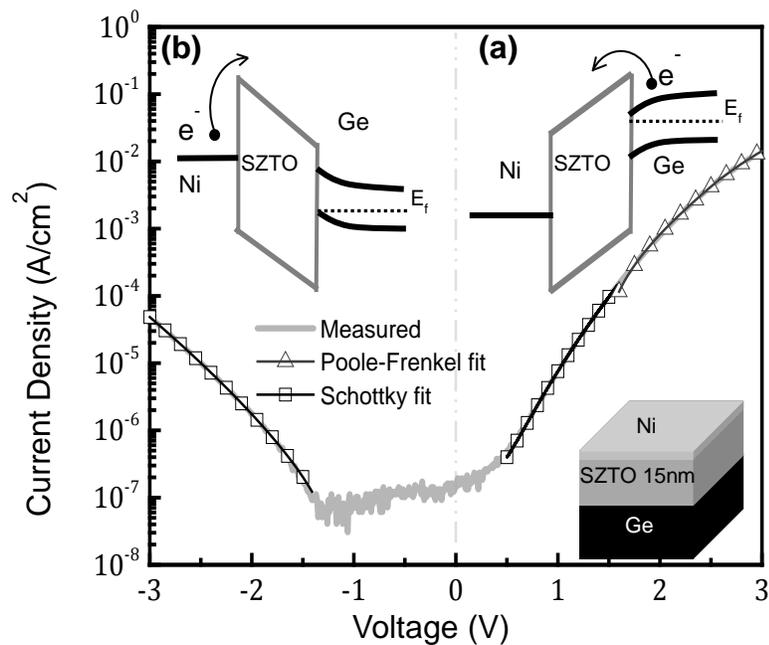


Figure 2-7 Current-Voltage characterization of Ni/SZTO/P-Ge on Ge. (a) MOS Type-I junction in forward and (b) in reverse bias.

$$J = J_0 \exp\left(\frac{\beta E^{0.5}}{k_B T}\right) \quad (2-1)$$

Where  $\beta$  is a constant,  $E$  is the electric field,  $k_B$  is Boltzmann's constant, and  $T$  is temperature.

For the positive bias in Figure 2-7 two different mechanisms can be observed. First, for bias less than 1.5 V the calculated  $\beta \sim 0.09 \times 10^{-21}$  is consistent with electrode-limited (Schottky) conduction while for the bias larger than 1.5 V, calculated  $\beta \sim 0.6 \times 10^{-21}$  is more relevant to the bulk-limited (Pool-Frenkel) conduction mechanism [42]. However, in negative bias a single curve fitting with  $\beta \sim 0.09 \times 10^{-21}$  is more relevant to the Schottky conduction mechanism. The type-I band offset is also manifested in capacitance-voltage measurements of our SZTO-Ge heterojunctions. C-V measurements of a  $x = 0.70$  SZTO-Ge heterojunction are shown in Figure 2-6 as a function of frequency. The capacitance at 1 MHz for  $V > 1$  V matches the expected minimum capacitance for our heavily doped p-type Ge substrates, and C-V measured in 5 kHz indicates that inversion has been achieved. In the absence of a type-I band offset between the oxide and semiconductor, leakage currents would prevent inversion from occurring on p-type substrates.

A shift in the flat-band voltage is observed, which we attribute to positive charges in the SZTO that are likely associated with oxygen vacancies, as has been found in related studies [26]. The flatband voltage should be around 0.38 V in the absence of trapped oxide charges. [26] We estimate the dielectric constant of the SZTO to be  $\kappa_{\text{SZTO}} = 29$ , based on the capacitance in accumulation at 1 MHz (i.e.,  $1.7 \times 10^{-6} \text{ F cm}^{-2}$ ). The value of  $\kappa_{\text{SZTO}} = 29$ , which is near the dielectric constant of bulk

$\text{SrZrO}_3$  ( $\sim 30$ ) is comparable to some of the highest dielectric constants amongst gate materials that have been reported for Ge.[27-30] In this regard, crystalline SZTO on Ge can potentially be utilized as a gate dielectric for the next-generation field-effect devices. The performance of complementary-metal-oxide-semiconductor (CMOS) devices has reached a plateau due in part to the fundamental materials limitations of Si. Key to extending CMOS technology is to replace the Si channel with a high mobility material such as Ge.[31] A more thorough evaluation of crystalline SZTO on Ge as a gate dielectric, including thickness dependence of dielectric properties and analysis of interface state densities, will be presented in the next chapter.

To quantify the valence band offsets of SZTO on Ge, we have performed high-resolution core-level (CL) and valence band (VB) x-ray photoemission spectroscopy measurements on a  $x = 0.65$  film. We used a combination of CL and VB spectra for thin and thick film samples to determine the valence band offset (VBO) similar to what was done for  $\text{SrTiO}_3/\text{Si}(001)$ . [14, 33-35] The Sr 3d and Ge 3d peaks were used because they are intense, and do not overlap with XPS and Auger peaks from other elements, with the exception of the Ge 3d and Zr 4p. However, for the 6 u.c. film specimen, the Zr 4p is sufficiently weak that it doesn't affect the more intense Ge 3d line shape or binding energy in any measurable way.

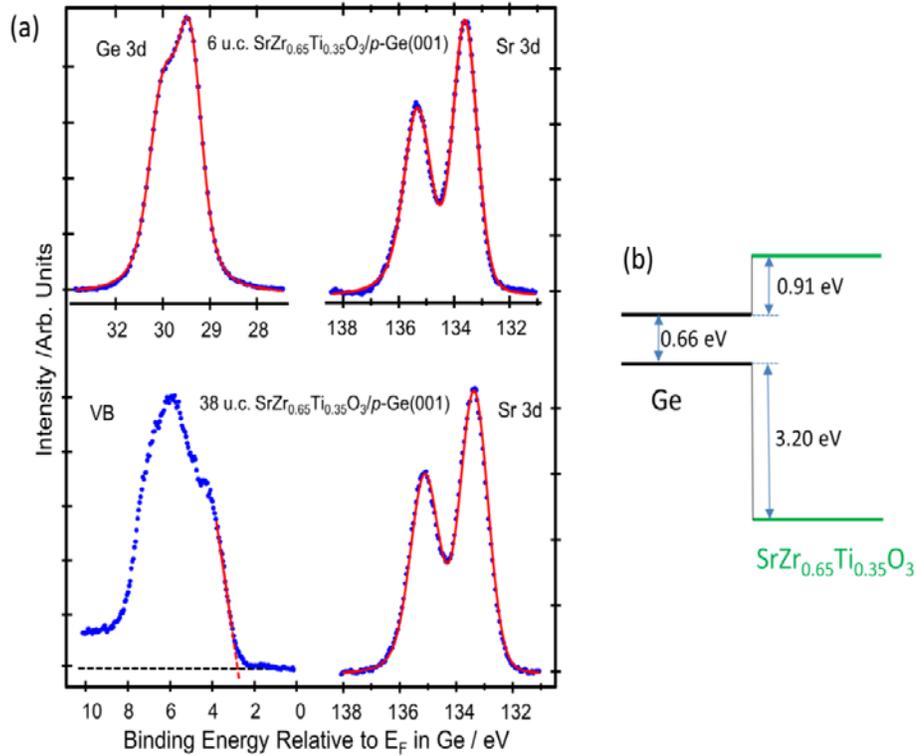


Figure 2-8 XPS analysis of the bandgap (a) Core-level and valence band x-ray photoemission spectra taken on a 6 u.c. thick (top) and 38 u.c. thick (bottom)  $x = 0.65$  SZTO-Ge heterojunctions. Solid lines are fits to the data. (b) Band diagram showing conduction and valence band offsets for a  $x = 0.65$  SZTO-Ge heterojunction.

The results are shown in Figure 2-8. The energy from the top of the VB to the Sr  $3d_{5/2}$  core peak,  $(ESr3d_{5/2} - EV)SZTO$ , was measured to be 30.59(6) eV for the 38 u.c. film. This quantity was combined with an analogous energy difference for clean Ge(110),  $(EGe3d_{5/2} - EV)Ge = 29.52(4)$  eV, and the 1 core-level binding energy difference for the 6 u.c. heterojunction,  $(ESr3d_{5/2} - EGe3d_{5/2})HJ = 104.27(2)$  eV, to yield a VBO given by  $\Delta EV = (ESr3d_{5/2} - EGe3d_{5/2})HJ + (EGe3d_{5/2} - EV)Ge - (ESr3d_{5/2} - EV)SZTO = 3.20(8)$  eV.[36]

On the premise the band-gap of SZTO follows Vegard's law, the conduction band offset for  $x = 0.65$  is estimated to be 0.91 eV.[21]

Aside from serving as a candidate gate dielectric for field-effect devices, SZTO can serve as both an electrical and epitaxial platform for integrating multifunctional crystalline oxides on semiconductors. For ferroelectrics, SZTO could serve as an intermediate layer to inhibit charge transfer from a ferroelectric to a semiconductor, thus enabling a capacitor to form in which the polarization of the former maintains accumulation or inversion in the latter.[12] As an intermediate buffer, the relatively high-K would reduce effects of depolarization fields in the ferroelectric. For spintronic applications, SZTO could serve as a tunnel barrier through which spin-polarized carriers from a crystalline half-metallic oxide can be injected into a semiconductor. As a candidate tunnel barrier, SZTO is single crystalline, which could potentially enhance injection efficiency.[37] Furthermore, the barrier height is adjustable through control of Zr content.

Previously, rocksalt structured AeO (Ae = Sr, Ba, Ca) were explored as intermediary buffer layers between Si or Ge and AeTiO<sub>3</sub> to mitigate the absence of a type-I band offset. [19] However, AeO can react with AeTiO<sub>3</sub> leading to instability of the rocksalt/perovskite stack. [38] Epitaxially integrating additional layers of multifunctional oxides on AeO is thus challenging. Furthermore, AeO exhibit relatively low dielectric constants, limiting their effectiveness as gate dielectrics. Also, AeO are hygroscopic and are thus unstable in ambient conditions. Finally, the band offset between AeO and semiconductors cannot be continuously tuned from type-II to type-I. Thus, our approach to directly engineer the band-gap of a perovskite oxide on a

semiconductor circumvents the challenges of combining rocksalt and perovskite oxides in heterostructures, and enables additional tunability of the band offset

Lastly, we make a few remarks on the flexibility of the perovskite structure in enabling band offsets to be engineered at semiconductor - crystalline oxide interfaces. The enhancement of the band-gap and band offset with Zr substitution is accompanied by a concomitant increase in the lattice constant of SZTO, thereby improving the lattice match with Ge, as shown in Figure 2-3(c). Generally, it would be more ideal to be able to tune the offset and lattice constant independently. In this regard, the perovskite structure allows for substitution of both A- and B-site cations. Whereas B-site substitution of Zr for Ti affects both the band-gap and lattice constant of SZTO, A-site substitution predominantly affects the lattice constant only. The substitution of Ba (Ca) for Sr could be utilized to increase (decrease) the lattice constant, independent of the Ti to Zr ratio within some regime. Thus, high quality epitaxial films that match well with the semiconducting substrate can, in principle, be achieved for a desired band offset. Future work will focus on exploring this possibility.

#### *2-4 Experimental Section*

Crystalline SZTO films were grown on p-type Ge (100) wafers (AXT Inc.,  $\rho \approx 0.02 \text{ } \Omega \cdot \text{cm}$ ) using reactive MBE in a custom-built chamber operating at a base pressure of  $< 2 \times 10^{-10}$  Torr. The Ge wafers were introduced into the growth chamber after an etch and oxidation process that involved repeated dips in diluted HCl and H<sub>2</sub>O<sub>2</sub>. [25]

A clean dimerized Ge surface was obtained by thermally desorbing the resulting GeO<sub>2</sub> from the surface in ultra-high vacuum at  $\sim 600 \text{ } ^\circ\text{C}$ . The Ge was then

cooled to  $\sim 400$  °C at which a half monolayer of Sr metal was deposited to passivate the clean Ge surface. Thermal effusion cells (Veeco and SVT Associates) were used to evaporate all source materials for growth, and fluxes were calibrated using a quartz crystal monitor (Inficon). The Ge was then cooled to room temperature at which 1.5 monolayers of SrO was co-deposited with 2 monolayers of  $Zr_xTi_{1-x}O_2$  in an oxygen background pressure of  $3 \times 10^{-7}$  Torr. The Ge was then heated to  $\sim 550$  °C to crystallize the 2.5 u.c of SZTO. Subsequent SZTO layers were deposited 3 u.c at a time at a substrate temperature of  $\sim 250$  °C, and background oxygen pressure of  $3 \times 10^{-7}$  Torr. The substrate temperature was increased to  $\sim 580$  °C in ultra-high-vacuum after each 3 unit-cell deposition of SZTO to improve crystallinity.

The cross-sectional STEM specimens along [110] direction of Ge were prepared by a focused ion beam (FIB) lift-out technique using a FEI-Helios FIB system. A Ga-ion beam (5 kV) was used for final thinning to remove the damaged surface layer. Imaging of the SZTO/Ge heterojunction was performed in an aberration-corrected Hitachi HD2700C dedicated STEM equipped with a high-resolution parallel EELS detector (Gatan Enfina-ER). During the measurement, we used a 1.3 Å probe with a beam current of 12 pA. The energy resolution of EELS spectrum was about 0.35 eV.

XRD measurements were performed in a Bruker D8 thin-film diffractometer using Cu  $K_\alpha$  radiation. The direct-space map was measured on a Panalytical Materials Research Diffractometer. The Ge (224) and perovskite (103) peaks were mapped separately because they are widely separated in diffraction space. These peaks were chosen because they can both be measured at the same angle (rotation about the sample surface normal) and therefore errors arising from a difference between the

[001] and  $\phi$  - axis are avoided. The scattering vector in real space was resolved into in-plane and out-of-plane components and multiplied by  $\sqrt{(h^2 + k^2)}$  and  $l$  respectively to give dimensions matching the lattice parameters. The coordinates of the perovskite SZTO map

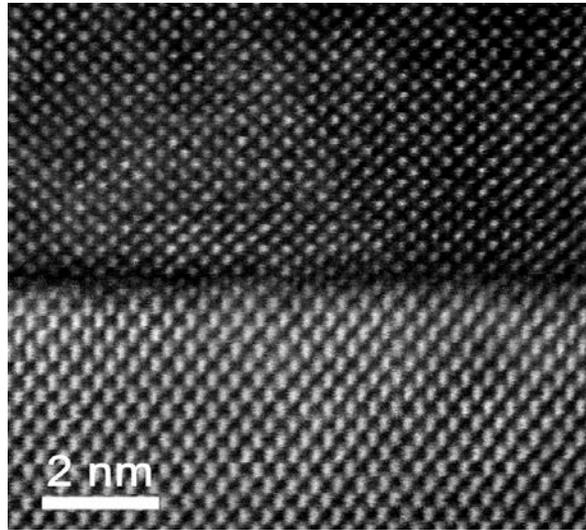


Figure 2-9 Annealing effect on the interface. Cross-section high-resolution transmission electron microscopy image of a SZTO  $x = 0.70$  sample after annealing at  $350^{\circ}\text{C}$  in flowing wet oxygen for 20 minutes showing an atomically abrupt and structurally coherent interface.

comparison on the same plot. High-resolution core-level (CL) and valence band (VB) x-ray photoelectron spectra were measured for as-received  $\text{SrZr}_x\text{Ti}_{1-x}\text{O}_3$  ( $x = 0.65$ ) films of thickness equal to 6 u.c and 38 u.c. using monochromatic  $\text{Al K}\alpha$  x-rays ( $h\nu = 1486.6$  eV) and a VG/Scienta SES 3000 electron energy analyzer. All spectra were measured in the normal-emission geometry and with a total energy resolution of (0.5 eV).

Prior to C-V and I-V characterization, both SZTO-Ge and BST-Ge heterojunctions were annealed for (20 to 30 minutes) at (350 °C) in flowing wet oxygen.[40] Wet oxygen is ultra-high purity oxygen that has been bubbled through de-ionized water prior to flowing through a tube furnace. As was found in previous studies, low temperature annealing in wet oxygen reduces residual oxygen vacancies.[41] However, this low temperature anneal does not affect the structurally coherent atomic registry at the SZTO and Ge interface (i.e. no GeO<sub>2</sub> formed), as revealed in high resolution transmission electron microscopy images of post-annealed samples Figure 2-9.[23] 30 nm thick Ni electrodes ranging in diameter from (20 μm) to (270 μm) were deposited through a shadow mask using electron beam evaporation. The backsides of the Ge wafers were mechanically scratched and InGa eutectic was applied to form a counter electrode. The I-V and C-V characterizations were performed on a Micromanipulator 8060 probe station using flexible, 10 micron radii, Tungsten probe whiskers. An Agilent 4155C and an Agilent 4284A LCR meter were used for the I-V and C-V measurements, respectively. I-V measurements were performed by ramping the voltage applied to the Ni electrode from (0 V to +3 V). To avoid effects due to charge trapping or junction degradation, a different junction was used to measure leakage current in the range of (0 V to -3 V). The I-V characteristics summarized in Figure 2-5 were averaged over 10 junctions for each film.

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## Chapter 3

### Ferroelectric thin film oxide on semiconductor

#### 3-1 Introduction

Ferroelectrics integrated on semiconductors have long been proposed to serve as a materials platform for a variety of electronic device technologies.[1-2] These proposed technologies envision utilizing the ferroelectric as a field-effect gate material in which its re-orientable polarization is coupled to itinerant carriers in a semiconducting channel. For applications in sensing, ferroelectric gate materials could lead to smart transistors that are sensitive to temperature and pressure.[3] In regards to computing, stabilization of the negative capacitance of ferroelectric gate materials could lead to field-effect transistors that require very little power to operate.[4] Ferroelectric gate materials could also lead to field-effect devices for non-volatile logic and memory due to the hysteretic remnant polarization that persists after power is removed.[5] Such hysteretic devices could also be exploited in computing based on emerging neuromorphic architectures.[6] In short, a materials platform that combines ferroelectrics and semiconductors could lead to field-effect devices that far surpass the performance and functionality of present devices.

In this regard, advancements in thin film growth have enabled single crystalline ferroelectrics to be epitaxially integrated on semiconductors,[7] such as  $\text{Pb}(\text{Zr}_{0.2}\text{Ti}_{0.8})\text{O}_3$  on Si,[8]  $\text{BaTiO}_3/\text{Ba}_x\text{Sr}_{1-x}\text{TiO}_3$  on Si,[9-10]  $\text{SrTiO}_3$  on Si,[11]  $\text{BaTiO}_3$  on GaAs[12] and  $\text{BaTiO}_3$  on Ge.[13-14] The growth of crystalline ferroelectrics on semiconductors offers a pathway to achieve material properties that are ideal for device applications, such as mono-domain states, and improved interfacial structure with the semiconductor. In

addition, the properties of crystalline oxide thin films can be controlled and enhanced through the effects of epitaxial strain.[15]

### *3-2 Ferroelectric thin film on semiconductors*

Despite such progress, the development of scalable, metal-oxide-semiconductor (MOS) capacitors using single crystalline ferroelectric gate materials remains elusive. MOS capacitors enable the surface potential of a semiconductor to be modulated through an applied bias, and thus underpin the functionality of field-effect devices. Modulation of the surface potential gives rise to a change in the capacitance of the semiconducting electrode, which is manifested as dispersion in the capacitance-voltage (C-V) characteristics of a MOS capacitor. When the re-orientable polarization of a ferroelectric gate material is coupled to the surface potential, hysteresis in the C-V characteristics typically emerges.[16] Realizing ferroelectric MOS capacitors is challenging for several reasons. First, coupling of the polarization of a ferroelectric to the surface potential of a semiconductor requires continuity in the electric displacement between materials that differ in elemental composition and bonding. Dangling bonds at interfaces between a ferroelectric and a semiconductor can trap charges that electrically screen the polarization. Second, a type-I arrangement in which the conduction (valence) band of the ferroelectric is above (below) the conduction (valence) band of the semiconductor is needed to enable ferroelectric MOS structures to function as capacitors.[17] Unfortunately, ferroelectrics such as BaTiO<sub>3</sub> exhibit a type-II band alignment with respect to Si, Ge and GaAs, in which the conduction band of the oxide is below that of the semiconductor.[18-19] Third, for applications in computing, the continued lateral scaling of field-effect transistors places constraints on

the thickness of gate materials that can be used in practical devices.[20-21] For example, present state-of-the-art transistors utilize gate oxides that are only a few nanometers thick.[22] However, ferroelectricity is generally weakened at such thicknesses because of depolarization fields, which are particularly strong for ferroelectrics grown on semiconductors due to longer screening lengths in the latter.[23] Due to the above challenges, prior reports of single crystalline ferroelectric MOS capacitors have typically utilized thick ( $\geq 90$  nm) ferroelectric layers.[24-25]

### *3-3 Specifications of this work*

Here we present ferroelectric MOS capacitors comprised of single crystalline  $\text{SrZr}_x\text{Ti}_{1-x}\text{O}_3$  ( $x = 0.7$ ) (SZTO) that has been grown on Ge, a semiconductor that is of interest for next-generation field-effect transistors due to its high carrier mobility. The ferroelectric properties of SZTO have been characterized using piezo-response force microscopy (PFM), polarization-voltage PUND, and C-V measurements. Analysis of high angle annular dark-field (HAADF) images obtained through scanning transmission electron microscopy (STEM) reveals evidence for relaxor behavior, namely, regions that exhibit non-centrosymmetric displacements of Ti/Zr cations, consistent with the presence of polar nano-regions (PNRs).[26-27] Ab initio density functional theory (DFT) calculations suggest that non-centrosymmetric displacements of Ti cations substituted in a sublattice dominated by larger Zr cations play a key role in the

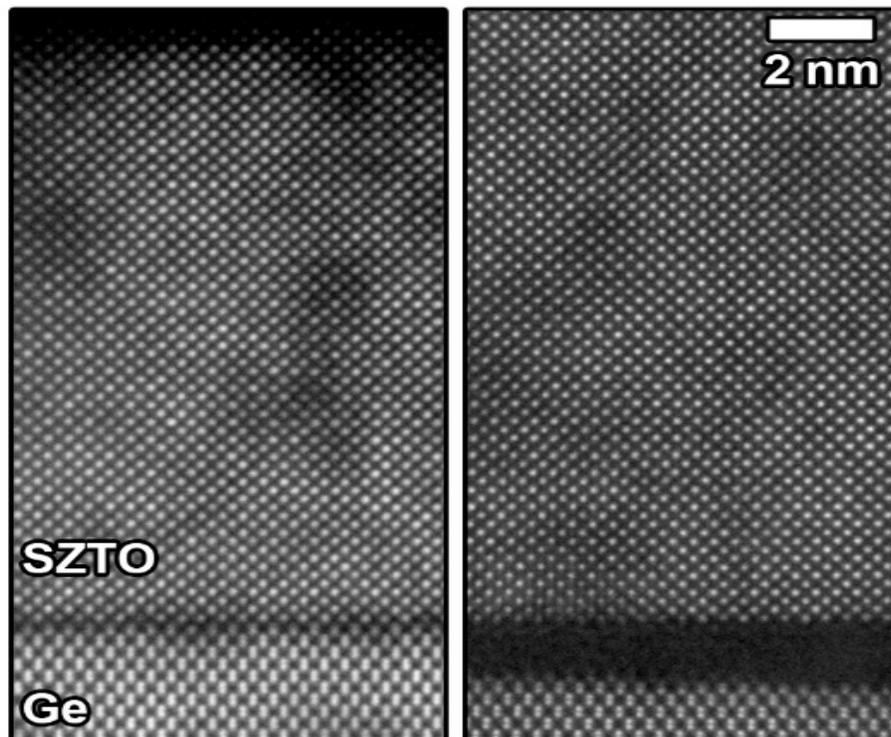


Figure 3-1 Annular dark field - RevSTEM images of 15 nm thick SZTO in unannealed (left) and annealed (right) conditions, showing formation of a 1-2 nm thick  $\text{GeO}_x$  layer at the interface due to the particular annealing conditions. The surface of the unannealed (left) and annealed (right).

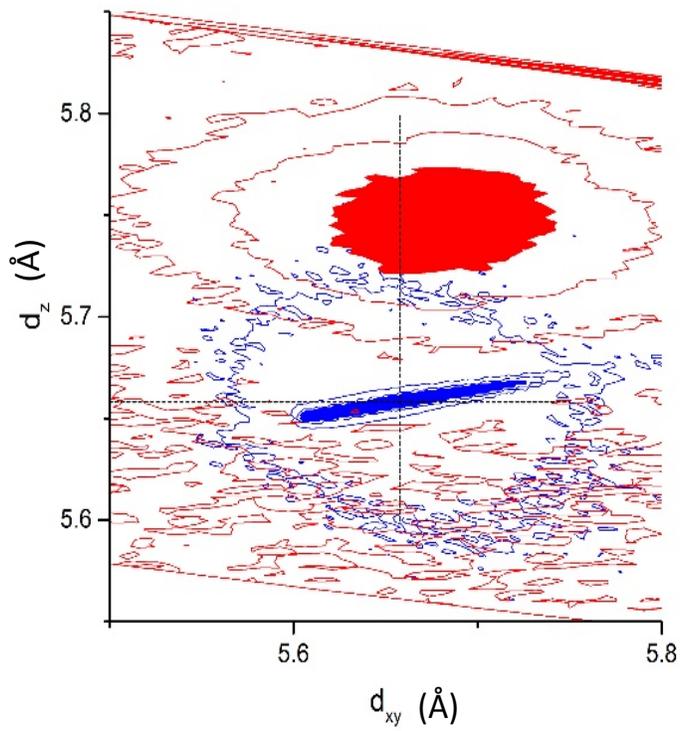


Figure 3-2 Direct space map of annealed 15 nm thick SZTO film on Ge. The formation of an interfacial layer of  $\text{GeO}_x$  causes the SZTO to relax slightly from the Ge substrate.

formation of PNRs. We find that the ferroelectricity in SZTO is exceptionally robust, as 5 nm thick films corresponding to an equivalent-oxide-thickness (EOT) of 1.0 nm exhibit a  $\sim 2$  V wide hysteretic window in the C-V characteristics, opening a pathway to realize highly scalable ferroelectric field-effect devices.

Epitaxial SZTO films are grown on p-type Ge using oxide molecular beam epitaxy (MBE). As grown films are electrically leaky, which is attributed to residual oxygen vacancies formed in the relatively low oxygen background pressure of the ultra-high vacuum MBE chamber.

To minimize the presence of residual vacancies, the SZTO films are annealed ex situ in oxygen after growth, which reduces the leakage currents over several orders of magnitude. We present electrical characterization of annealed, 15 and 5 nm thick SZTO films on Ge below.

Aside from minimizing residual vacancies, annealing can create a thin layer of  $\text{GeO}_x$  at the interface as shown in Figure 3-1 and Figure 3-10 for the 15 and 5 nm thick films, respectively. The annealed films are compressively strained ( $a = 4.03$  Å and  $c = 4.07$  Å) relative to bulk SZTO of the same  $x = 0.7$  Zr content ( $a = 4.048$  Å and  $c = 4.052$  Å), [28] as shown in Figure 3-2.

We find that annealing is essential to observe effects of ferroelectricity in our films, as further discussed in the next section.

High-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) using the RevSTEM technique reveals that the 5 nm and 15 nm SZTO films grown on Ge are of good crystalline quality, though both exhibit some mosaicity that likely arises out of misfit-induced defects or steps/flaws on the Ge surface. The

images indicate orientation alignment of the [100] type SZTO zone axis to the <110> type Ge zone axis.

For the 5 nm sample, the in- and out-of-plane lattice parameters with standard error of the mean measured from multiple STEM images are  $a = 402.7 \pm 0.2$  pm and  $c = 407.0 \pm 0.2$  pm, yielding a  $c/a$  ratio of approximately 1.01. From these same images, the lattice parameters and standard error of the mean of Ge are measured to be  $a/\sqrt{2} = 400.6 \pm 0.1$  pm (which scales to  $a = 566.5 \pm 0.2$  pm) and  $c = 566.3 \pm 0.2$  pm.

Measurement of the in-plane  $a$  parameter reveals an SZTO/Ge interfacial misfit of approximately 2 pm. Similar to the 5 nm thick SZTO, we find that the formation of  $\text{GeO}_x$  for the 15 nm thick annealed SZTO films causes the film to relax slightly, as shown in the direct space map of Supplementary Figure S2. Lattice constants for the 15 nm thick film from x-ray diffraction are found to be  $a = 4.03$  Å and  $c = 4.07$  Å.

Stable ferroelectric domains can be written on SZTO using PFM. Figure 3-3(a) and 3-3(b) show spatial mappings of phase and amplitude response for a domain structure written on a 15 nm thick film. Here, a conductive atomic-force-microscope (AFM) tip held at a bias of -10 V is used to write a rectangle, followed by an adjacent rectangle written at a tip bias of +10 V.

The topography, shown in the inset of Figure 3-4(a), indicates that no irreversible electrochemical reactions occur on the surface due to poling. Figure

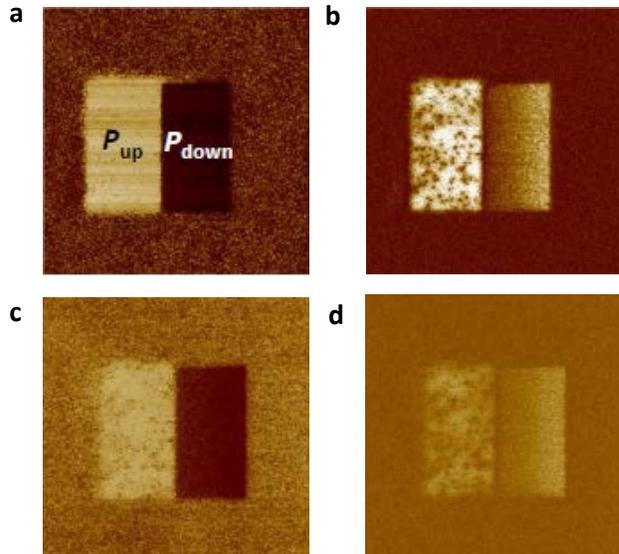


Figure 3-3 Piezo-response force microscopy of 15 nm thick SZTO film on Ge. (a) Phase and (b) amplitude response of domain structures 2.5 hours after writing. (c) Phase and (d), amplitude response of the same domain structures 48 hours after writing.

3-3(c) and 3-3(d) show the phase and amplitude responses, respectively, of the same region 48 hours after poling.

The PFM amplitude response exhibits a fast relaxation right after the domain writing, and then stabilizes for the duration of the measurements as shown in Figure 3-4(a). The time scale of the initial relaxation ( $\sim 10$  hours) is consistent with that observed for complete screening of the high bound charge density on a freshly switched ferroelectric domain,[29]and significantly longer than that required to screen the static surface charge induced by the tip bias during domain writing.[30] The persistence of spatially poled regions for extended periods of time in the absence of electrochemical changes on the surface is consistent with the creation of ferroelectric domains.

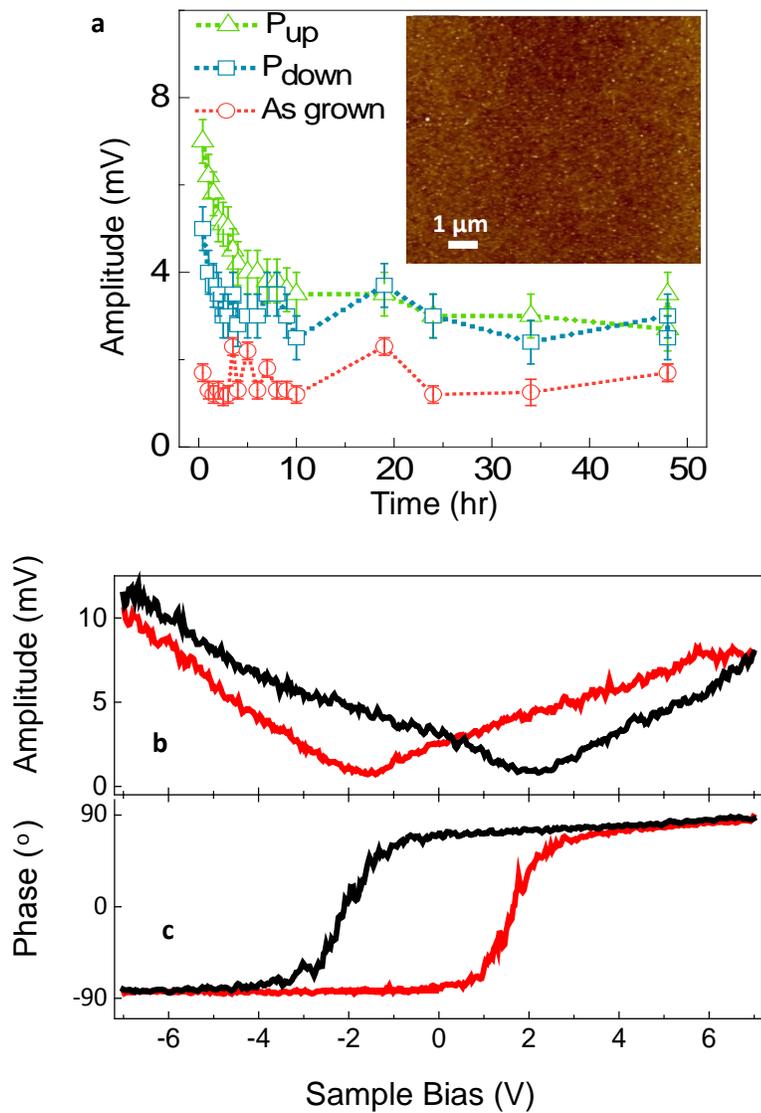


Figure 3-4 Amplitude response as a function of time for  $P_{UP}$  and  $P_{DOWN}$  domain structures, and as-annealed parts of film surface. (a) Inset shows the topography of the film after domain writing, indicating no tip induced electrochemical changes on the surface. (b) Amplitude and (c), phase piezo-response taken in spectroscopy mode, showing butterfly-like hysteresis and 180 $^{\circ}$  phase change, respectively.

Ferroelectric switching is also manifested in piezo-response spectroscopy measurements, in which the tip is held in one location and the phase and amplitude response are measured as a function of applied bias. Figure 3-4(b) and Figure 3-4(c) show the amplitude and phase responses of the tip, revealing ferroelectric butterfly-like hysteresis, and  $180^\circ$  phase shift, respectively. The PFM measurements also reveal that as-annealed films are preferentially poled in the downwards direction, i.e. with a polarization oriented towards the Ge electrode. The downwards polarization is so strong in some nanoscale regions that a -10 V tip bias is insufficient to switch the polarization upwards. Regions that exhibit asymmetric coercive voltages that favor a downwards polarization are also observed in piezo-response spectroscopy measurements (not shown).

To corroborate the evidence for ferroelectric behavior found in the PFM measurements,[31] we also perform C-V and polarization-voltage PUND measurements. In contrast to BaTiO<sub>3</sub> on Si [9] [10], SrTiO<sub>3</sub> on Si [11], BaTiO<sub>3</sub> on GaAs [12], and BaTiO<sub>3</sub> on Ge [14] which exhibit type-II band offsets, SZTO on Ge exhibits a type-I band offset, thus C-V and polarization-voltage measurements are possible. [32-33] Capacitance-voltage measurements demonstrate that the ferroelectric polarization of SZTO is coupled to the surface potential of Ge, which is essential for device applications. Figure 3-5(a) shows C-V characteristics of 15 nm thick SZTO taken between  $\pm 3$  V,  $\pm 4$  V and  $\pm 5$  V. Hysteresis is observed, with an orientation with respect to the direction of the sweeping voltage that is consistent with

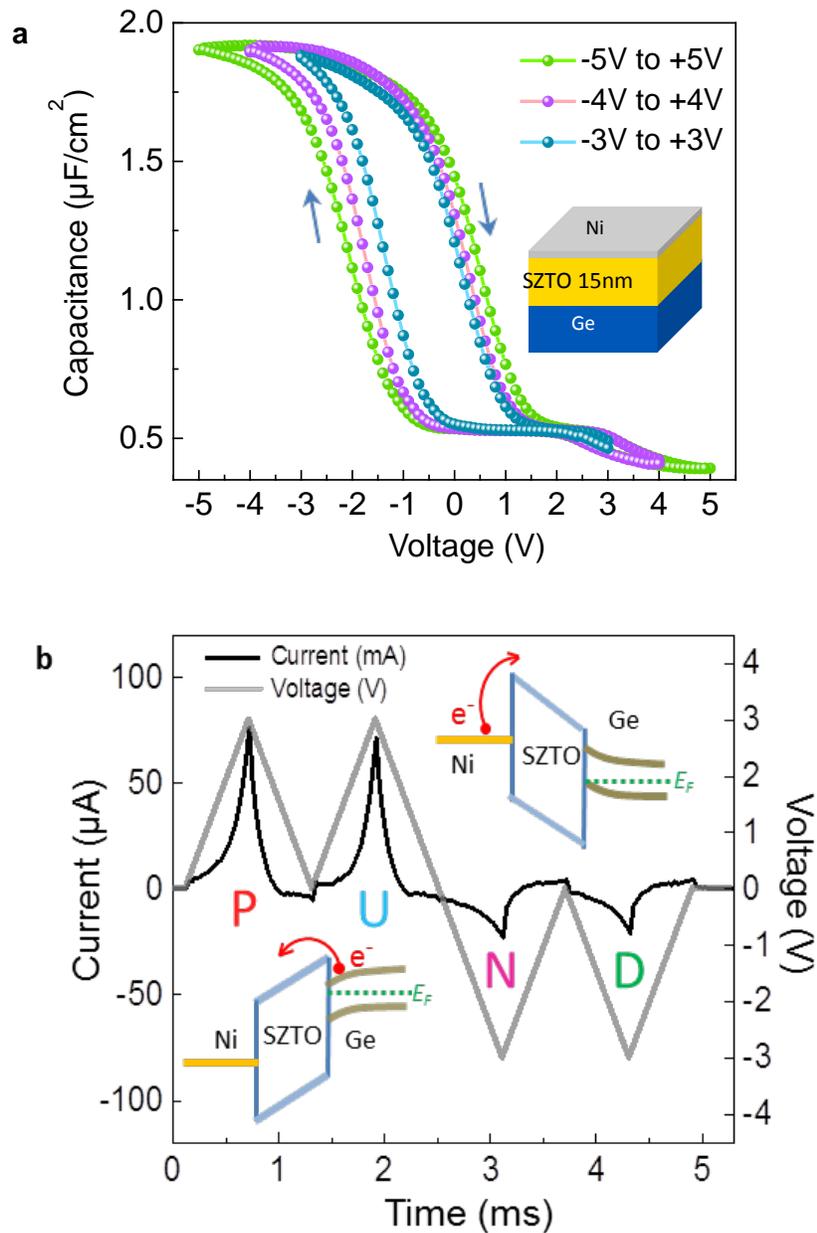


Figure 3-5 C-V and P-V characterization for 15 nm thick SZTO film on Ge. (a) C-V measurements showing hysteresis obtained for  $\pm 3$  V,  $\pm 4$  V and  $\pm 5$  V sweeps. (b) Current (black) measured through the Ni-SZTO-Ge stack in response to the PUND waveform (grey) applied to the Ni electrode. Bottom left (top right) inset illustrates the band diagram of the Ni-SZTO-Ge stack under positive (negative) bias.

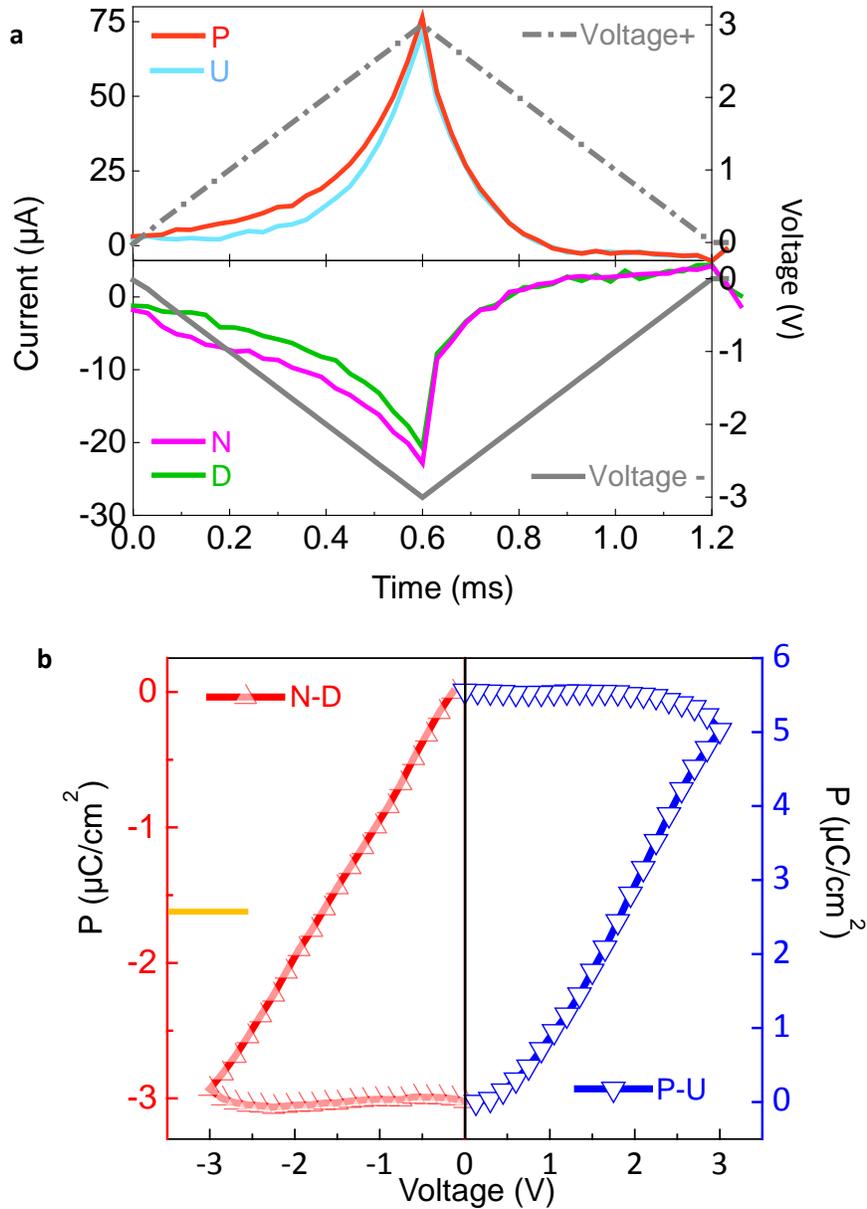


Figure 3-6 PUND current pulse and polarization (a) Current measured from each voltage ramp of the PUND waveform plotted independently on the same time scale to enable comparison. Switching of the hysteretic component of ferroelectric polarization is observed as excess current is measured on the rising (falling) side of the P (N) voltage ramp relative to the rising (falling) side of the U (D) ramp, as shown in the upper (lower) panel. (b) P-V half-loops obtained by integrating switching currents from the PUND measurements taken using  $\pm 3$  V voltage ramps.

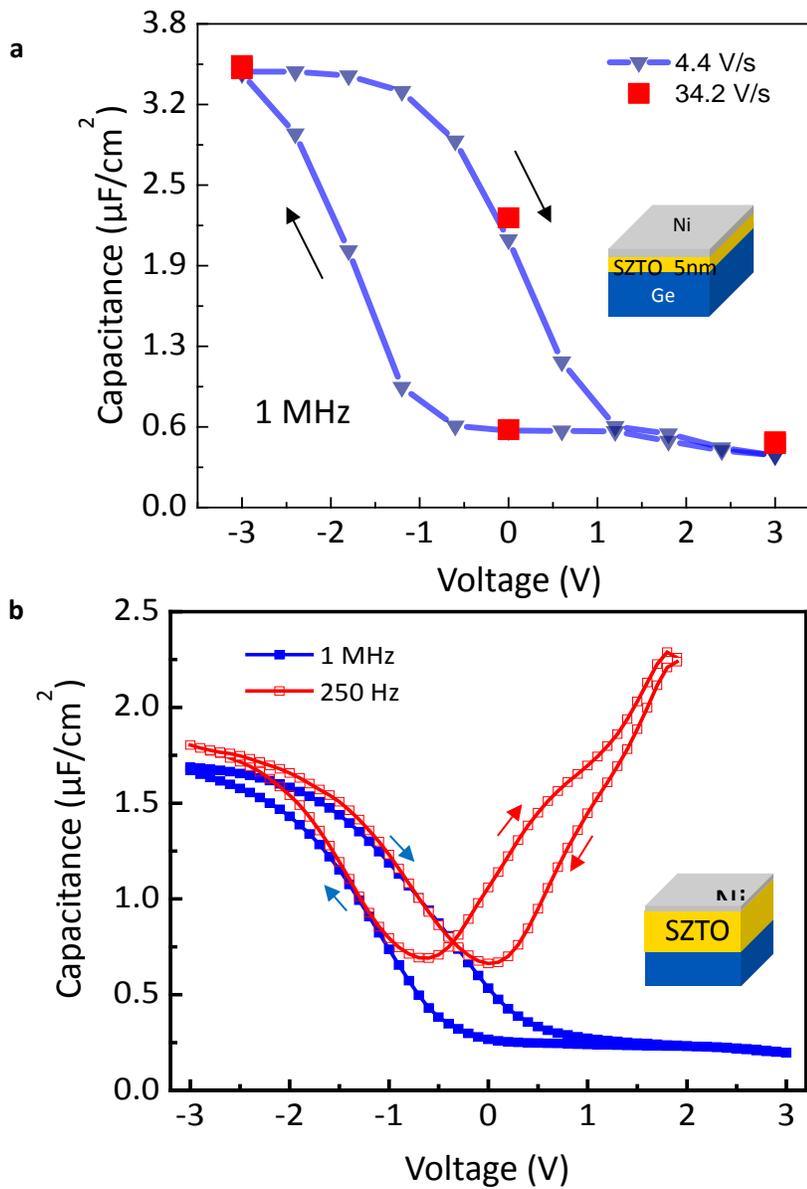


Figure 3-7 CV measurements on 5nm thick SZTO (a) C-V measurements taken function of rate at which the applied voltage is swept. The data presented in Figure 3-5(a) was taken at a slow sweep rate of 0.1 V/s. Here we show measurements taken at higher sweep rates. (b) C-V measurements taken on a 15 nm thick SZTO film at 1 MHz (blue) and 250 Hz (red). The upturn in capacitance observed for 250 Hz is evidence that inversion can be achieved in our SZTO MOS capacitors. Charge leakage likely causes the upturn not to saturate at the oxide capacitance.

switching of ferroelectric dipoles, as opposed to hysteresis induced by interfacial trap states. Mobile ions also cannot account for the hysteresis observed in our capacitors,

since a positive flat-band voltage is achieved, and the hysteresis does not diminish by increasing the rate at which the voltage is swept between positive and negative values, as shown in Figure 3-5.[5] Inversion can be achieved in our ferroelectric junctions, as shown in Figure 3-7(b). In general, we note that the hysteretic window in C-V tends to be centered towards negative bias, indicating the presence of fixed oxide charge, possibly due to residual oxygen vacancies. However, the shift due to fixed oxide charges can be compensated by applying a large negative bias, as was done for the C-V data shown in Figure 3-5(a). The enhancement in hysteresis with magnitude of applied voltage, and ability to shift the centering of the hysteresis can be attributed to non-saturated behavior in the polarization.

The type-I band offset *also* enables the hysteretic, or remnant component of polarization to be estimated. Measurements are performed using the PUND technique [33-35] to isolate the hysteretic component of current due to ferroelectric switching from leakage currents, the latter of which are sizeable due to the thinness of the SZTO films. Figure 3-5(b) shows the current (black) measured in response to the PUND waveform (grey), consisting of switching P, N and non-switching U, D voltage ramps applied for positive and negative polarities to a Ni electrode. The magnitude of leakage current is larger for positive P, U voltage ramps in comparison to negative N, D voltage ramps, due to a difference in barrier height for charge injection, as illustrated by the band diagrams shown as insets in Figure 3-5(b). Ferroelectric switching is clearly resolved, as excess current on the rising (falling) side of the P (N) voltage ramp is measured relative to the rising (falling) side of the U (D) ramp as shown in Figure 3-6(a). The excess switching current is distributed over a broad voltage range in Figure 3-6(a), indicating the absence of a well-defined coercive voltage, which is likely due to some

nanoscale variation in electronic properties. Integration of the excess currents in P and N voltage ramps results in the two-respective polarization half-loops shown in Figure 3-6(b). Note the different scales used for each polarization half-loop, as the amount of charge switched for positive polarity P ramp ( $5.5 \pm 0.8 \mu\text{C}/\text{cm}^2$ ) is larger than the charge for negative polarity N ramp ( $3.0 \pm 0.4 \mu\text{C}/\text{cm}^2$ ). The difference in switching charge between P and N polarities could be due to several factors. The leakage currents are very large in comparison to the switching currents, rendering precise measurement of the latter difficult. Leakage currents that are a function of the polarization could also give rise to the observed difference.[13] From the charges that are switched, we estimate a remnant polarization of  $2.1 \pm 0.2 \mu\text{C}/\text{cm}^2$ . We find that the amount of charged switched can be enhanced by increasing the magnitude of the voltage ramps, as shown in Figure 3-8 for PUND measurements taken between  $\pm 4$  V. The enhancement of charged that is switched with increasing magnitude of applied voltage, i.e. electric field, indicates that the polarization of SZTO has not reached saturation, which behavior appears to be typical of ferroelectrics integrated on semiconductors. In terms of magnitude, the remnant

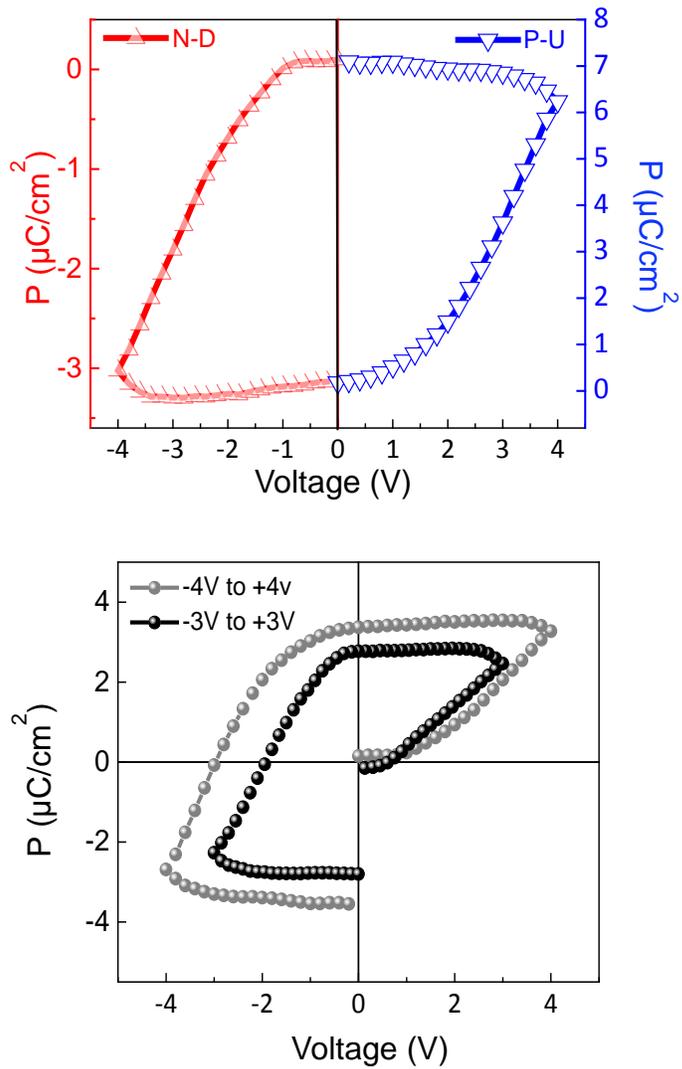


Figure 3-8 Polarization half-loops obtained through PUND measurements on a 15 nm thick SZTO film on Ge using voltage ramps of  $\pm 4$  V. The switching charge between positive (negative) polarity P, U (N, D) voltage ramps is  $\sim 6.9 \pm 0.8 \mu\text{C}/\text{cm}^2$  ( $\sim 3.3 \pm 0.4 \mu\text{C}/\text{cm}^2$ ).

polarization we measure is comparable to or larger than the those of other ferroelectric films integrated on semiconductors.[5,24]

Yet more remarkable, we find that the ferroelectricity in SZTO grown on Ge is robust for films as thin as 5 nm. Figure 3-9(a) shows the C-V characteristics of 5 nm thick film taken between  $\pm 3$  V, which results in a 2 V wide hysteretic window. Ferroelectric domains can be written on the 5 nm thick SZTO films using PFM, as shown in the inset of Figure 3-9(a), and piezo-response spectroscopy also confirms butterfly-like hysteresis and  $180^\circ$  phase-shift in the amplitude and phase response, shown in Figure 3-9(b) and 3-9(c), respectively. Compressive strain imparted from the Ge substrate likely contributes to the stability of ferroelectricity in our 5 nm thick SZTO films.[11] The relaxor nature of SZTO also likely contributes to the stability of ferroelectricity, as supported by a recent study in a related relaxor system, SrTiO<sub>3</sub>. [27] The annealed 5 nm thick SZTO films also exhibit relatively abrupt interfaces with Ge, as shown in the HAADF STEM images in Figure 3-10. An average  $\sim 0.6$  nm thick layer of interfacial GeO<sub>x</sub> is achieved with regions that even exhibit no discernible GeO<sub>x</sub> (top panel) using our basic annealing set-up. In principle, more advanced techniques such as rapid thermal annealing should enable better control of the oxidation process to further minimize GeO<sub>x</sub>. The 5 nm SZTO yields an EOT of 1.0 nm, which is approaching the EOT of gate oxides used in present conventional MOS transistors. The large hysteretic window in C-V achieved with an EOT of 1.0 nm opens a pathway to realize highly scalable ferroelectric field-effect devices.

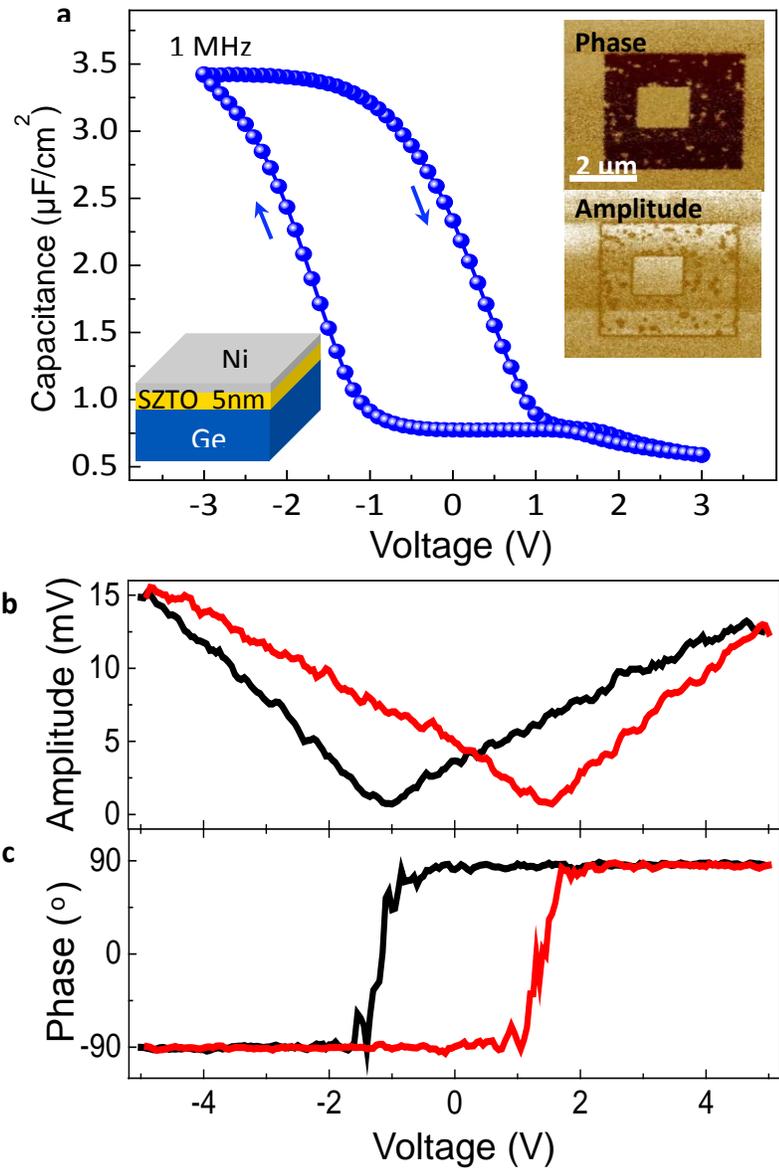


Figure 3-9 Electrical and structural characterization of 5 nm SZTO film on Ge. (a) C-V measurement of 5 nm thick SZTO film on Ge. Inset shows phase and amplitude contrast of domain structures written using PFM. (b) Amplitude and (c) phase piezo-response spectroscopy measurements of 5 nm thick SZTO on Ge.

STEM imaging reveals evidence of non-uniform atom column displacements in the films which are consistent with PNRs associated with relaxor materials. Spatial regions that exhibit non-centrosymmetric displacements of B-site cations relative to the A-site sub-lattice are a signature of PNRs in ABO<sub>3</sub> structured perovskites. To look for such displacements, mappings of the deviations of the Zr/Ti B-site atom columns from the ideal center of the perovskite cells bounded by their four neighboring A-site Sr atom columns are performed on HAADF images of a 5 nm thick film, as shown in Figure 3-11. The directions and lengths of the arrows superimposed on the HAADF image represent the directions and magnitudes, respectively, of the non-centrosymmetric Zr/Ti displacements. Consistent with the presence of PNRs, spatial correlation between the magnitudes and directions of the non-centrosymmetric displacements is observed, as regions that contain larger-than-average displacements are aligned in similar directions. In contrast, the magnitudes and the directions of displacements are typically random in non-polar structures.[36] Mapping the deviation of a dumbbell from the center of its four neighboring dumbbells in the Ge substrate reveals typically smaller displacements that are not aligned, as shown in Figure 3-12(a). In general, we find that regions exhibiting non-centrosymmetric Zr/Ti displacements vary in size, shape, and direction of displacement. For 5 nm thick films, the regions containing ordered displacements are found to align with preference towards the +c and -c directions of the film. It should be noted that no electric field was applied to the films prior to preparation for STEM imaging, thus the absence of a net alignment amongst the PNRs is expected.[26] While we have not measured the oxygen sub-lattice, and thus cannot comment on the polarization of PNRs, the displacements we measure are comparable to or larger than those of archetype BaTiO<sub>3</sub>. It is interesting to note a recent study by

Lee *et al.*, which found PNRs in SrTiO<sub>3</sub> thin films that exhibited local polarizations of  $\sim 24 \mu\text{C}/\text{cm}^2$  that gave rise to a macroscopic remnant polarization that is  $< 1 \mu\text{C}/\text{cm}^2$ . [27] In this regard, our displacement maps also suggest that the local polarization of PNRs can be much larger than the macroscopically measured polarization. In standard ABO<sub>3</sub> perovskite structured relaxors, the origin of PNRs is linked to disorder in the composition of the B-site cation. In this regard, SZTO is similar to BaZr<sub>x</sub>Ti<sub>1-x</sub>O<sub>3</sub>, which is a relaxor that has been extensively characterized. [37] Unlike BaZr<sub>x</sub>Ti<sub>1-x</sub>O<sub>3</sub>, however, relaxor behavior has yet to be reported in bulk SZTO. [38]

To gain insight on how PNRs form in strained SZTO thin films, we performed *ab initio* DFT modeling of this system. We first seek to understand the behavior of Ti cations substituted into a B-site sublattice dominated by Zr, as shown in Figure 3-12(a). In pure SrZrO<sub>3</sub> (SZO) that is compressively strained to the lattice constant of Ge, all in-plane and out-of-plane Zr–O distances are 2.05 and 2.12 Å (see Figure 3-12(b)), respectively, indicating that bulk SZO does not exhibit lattice polarization even under compressive strain. In contrast, upon substituting a Ti atom into a Zr site, the out-of-plane TiZr–O bond lengths split into short (1.92 Å) and long (2.16 Å) ones, as shown in Figure 3-13(a) (hollow squares). This effect is attributed to the smaller ionic radius of Ti<sup>4+</sup> (74.5 pm) in comparison to Zr<sup>4+</sup> (86 pm), which leads to a double-well potential energy surface for Ti<sup>4+</sup> ions and, in turn, results in effectively 5-fold coordination of the TiZr site.

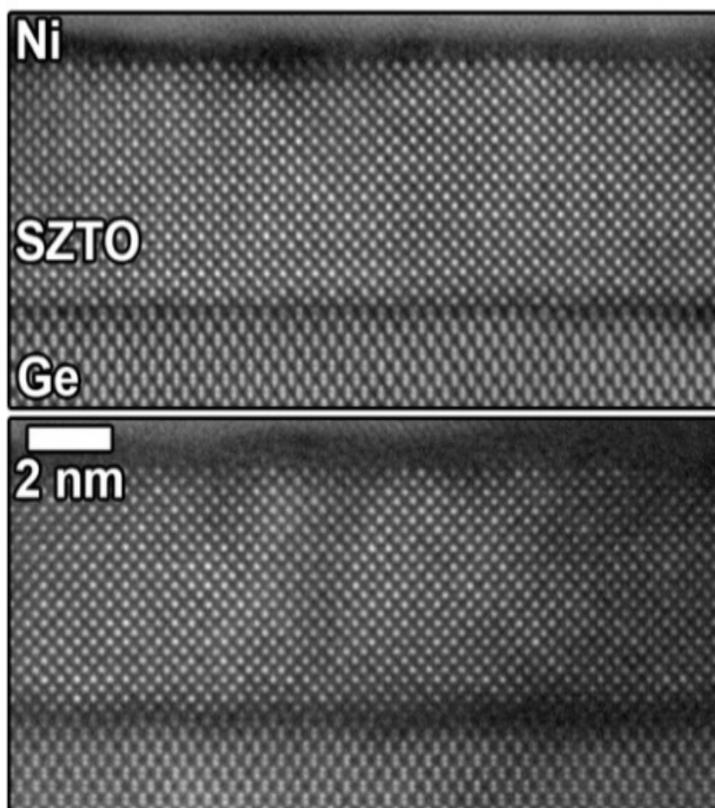


Figure 3-10 HAADF STEM images taken on annealed 5 nm thick SZTO on Ge, showing relatively abrupt interfaces. Both images are from the same lamella, and show the variation of GeO<sub>x</sub> formation at the interface, from little-to-no GeO<sub>x</sub> in the top panel to containing regions around 0.5 nm thick as in portions of the bottom panel. On average, there is ~ 0.6 nm thick interfacial GeO<sub>x</sub> between the 5 nm thick SZTO film and Ge.

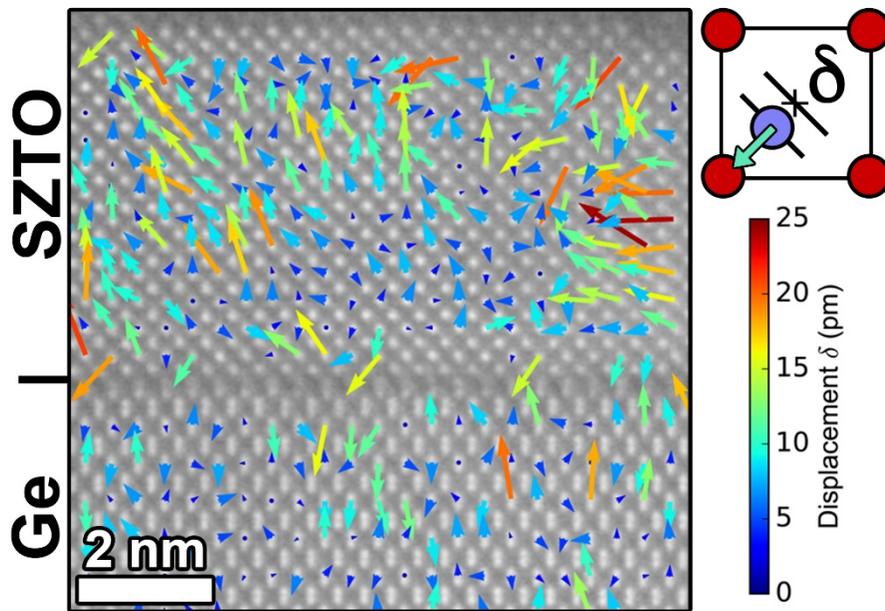


Figure 3-11 Magnitude and direction of non-centrosymmetric Zr/Ti column displacements  $\delta$  superimposed on HAADF image of annealed 5 nm thick SZTO film on Ge. Top right schematic shows how  $\delta$  is measured with respect to *A*-site and *B*-site cations. The color scale also indicates the magnitude of displacement, which was limited to 20 pm to emphasize the spread in color over the relevant distances.

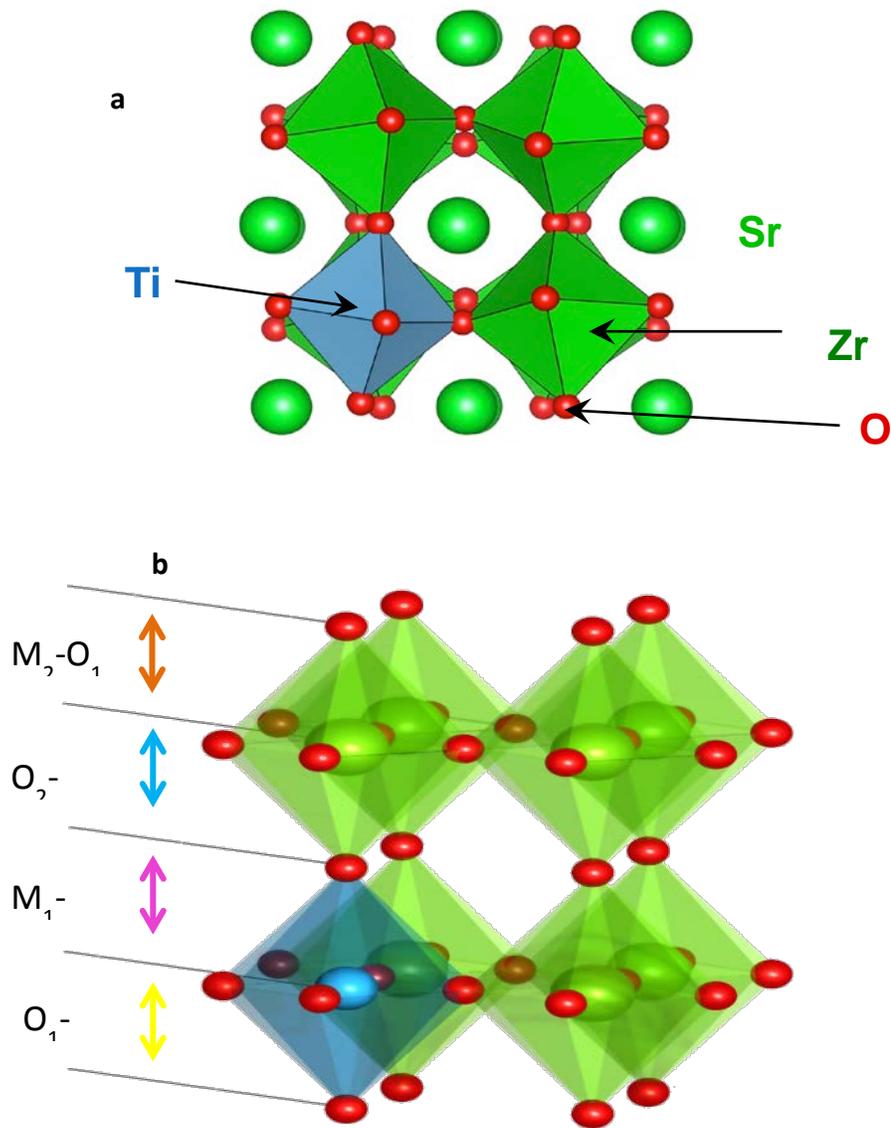


Figure 3-12 Structure of the bulk SZTO with Ti concentration of 12.5% as obtained using the 2x2x2 supercell subjected to compressive strain. (b) Metal-oxygen distances in O-(Zr,Ti)-O chains along the c-axis Ti-centered octahedra.

Importantly, the distortion of the Ti local environment induces disproportionation of Zr–O bond lengths into short (2.06 Å) and long (2.25 Å) ones at the neighboring Zr sites along the c-axis, (hollow squares in Figure 3-13(a), which indicates that not only are polarized themselves, but they also polarize neighboring Zr-centered octahedra.

To understand the cumulative effect of such displacements in a film which has random placement of Ti amongst a Zr sublattice, we consider 4 types of configurations of Ti cations, namely, column, screw, pairs and plane with an overall Ti concentration of 25%, as shown in Figure 3-13(b). The plane configuration was found to be energetically more favorable than the column (+0.1 eV) and the screw (+0.35 eV) configurations. However, given the small Ti to Zr ratio and the substrate temperatures used during film growth, the predominance of planar structures is unlikely. The remaining configurations are within 0.25 eV (0.05 eV per Ti) from each other, and we propose that all of them are equally likely to be realized. A periodic, 2×2 lateral supercell slab is used to model the SZTO film on a SrTiO<sub>3</sub> substrate, in which the in-plane lattice parameters are fixed to the experimental value of  $a = b = 4.03 \text{ \AA}$ , and the out-of-plane parameter is  $c = 50.0 \text{ \AA}$ . We choose SrTiO<sub>3</sub> (STO) as a substrate to bypass the complexities associated with modelling a SZTO/Ge interface with a partially oxidized GeO<sub>x</sub> layer.

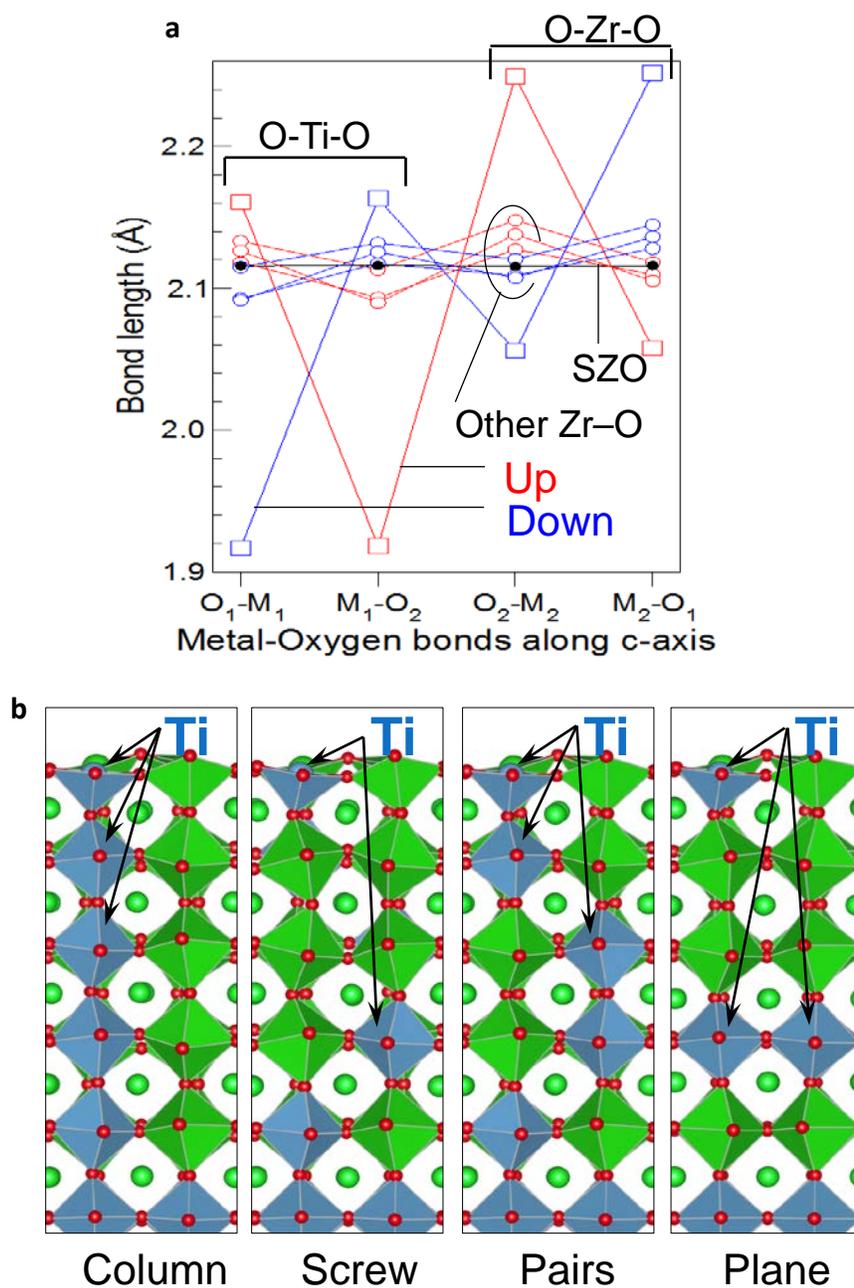


Figure 3-13 (a) Metal-oxygen distances in O-(Zr,Ti)-O chains along the *c*-axis show that polarization of Ti-centered octahedra induces similar along the *c*-axis between B-site (Ti,Zr) cations and oxygen anions located in adjacent planes. Each plane within the periodic slab is numbered as shown in polarization of Zr-centered octahedra. (b) DFT modelling of SZTO film with various configurations of Ti distributions, namely, column, screw, pairs and plane.

If all Ti cations are situated in a single column along the c-axis, we find that a continuous sequence of short-long-short-long-etc., Ti–O bonds forms. If Ti cations are in different columns in a screw or pairs configuration, short-long Ti/Zr–O bond length sequences also form, though the difference in length between short and long bonds is smaller. Finally, for the plane configuration, long-long-short-short-long-long bond sequences appear that are locally symmetric with respect to the Ti plane.

The sequences of Ti/Zr–O bond lengths give rise to a dipole moment within each  $\text{BO}_2$  plane. We note that in-plane components of polarization are also produced (not shown). The column configuration gives rise to a net polarization that is long-range, i.e. extends throughout the thickness of the film, while screw, pairs and plane configurations lead to polarizations that are shorter in range and smaller in magnitude. These results also yield insight as to the predominance of a downward oriented polarization. The existence of the surface/vacuum interface gives rise to an asymmetry in the structure of the film and, accordingly, lattice polarization. Since Ti–O bonds are shorter than Zr–O bonds, Ti atoms in the top plane displace down with respect to the average Zr position in the same plane, and thus favors the short-long-short-... Ti/Zr–O bond pattern that corresponds to a downward polarization. Aside from the dominant downward polarization at the surface, we find that the bulk corresponds to virtually zero net polarization because the statistical probability of distorted Ti/Zr-centered octahedra to contribute to upwards and downwards polarizations are the same everywhere except at the surface and the interface with the substrate. We note that our calculations do not consider defects, vacancies and variations in strain, all of which can affect the nucleation of PNRs.

### 3-4 Relaxor ferroelectric behavior with temperature variation

Dielectric permittivity of relaxor ferroelectrics reaches a maximum at the temperature  $T_{\max}$  for a particular frequency. As the frequency increases,  $T_{\max}$  increases to higher temperature. We have observed such behavior in temperatures around 300°C as shown in Figure 3-14.

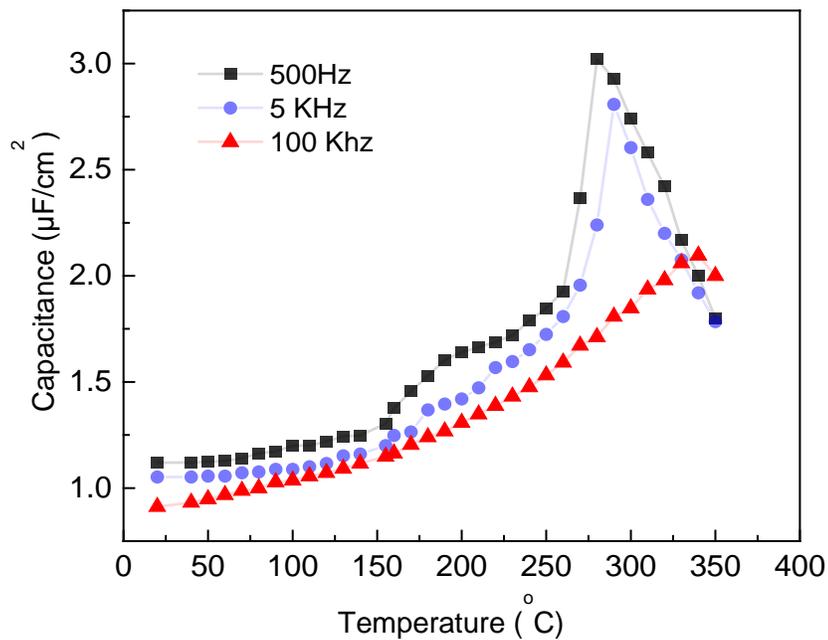


Figure 3-14 Temperature dependence of permittivity and  $T_{\max}$  shift toward higher temperatures as frequency increases observed at 15nm thick SZTO sample.

### 3-5 Experimental Section

Film growth - Crystalline SZTO films were grown on p-type Ge (100) wafers (AXT Inc.,  $\rho \approx 0.02 \Omega\text{cm}$ ) using reactive MBE in a custom-built chamber operating at a base pressure of  $< 2 \times 10^{-10}$  Torr. The Ge wafers were introduced into the growth

chamber after an etch and oxidation process that involved repeated dips in diluted HCl and H<sub>2</sub>O<sub>2</sub>. A clean dimerized Ge surface was obtained by thermally desorbing the resulting GeO<sub>2</sub> from the surface in ultra-high vacuum at ~ 600 °C. The Ge wafer was then cooled to ~ 400 °C at which a half monolayer (ML) of Sr metal was deposited to passivate the clean Ge surface. Thermal effusion cells (Veeco and SVT Associates) were used to evaporate all source metals for growth, and fluxes were calibrated using a quartz crystal monitor (Inficon). The Ge wafer was then cooled to room temperature at which an additional 1 ML of SrO was deposited, followed by co-deposition of 1.5 ML of SrO and 2 monolayers of Zr<sub>x</sub>Ti<sub>1-x</sub>O<sub>2</sub> in an oxygen background pressure of 3 × 10<sup>-7</sup> Torr. The temperature of each effusion cell was adjusted to control the relative flux rates of the metal sources to achieve the desired Sr, Ti and Zr ratios and enable co-deposition. The Ge was then heated to ~ 550 °C to crystallize the 2.5 unit-cells of SZTO. Subsequent SZTO layers were grown 3 unit-cells at a time through co-deposition of Sr, Ti and Zr fluxes at a substrate temperature of ~ 250 °C, and background oxygen pressure of 3 × 10<sup>-7</sup> Torr. The substrate temperature was increased to ~ 580 °C in ultra-high-vacuum after each 3 unit-cells deposition of SZTO to improve crystallinity.

Post-growth annealing - Both 15 nm and 5 nm thick SZTO films were annealed in a tube furnace (MTI corp.) at ambient pressures in flowing ultrapure oxygen that had been bubbled through high purity deionized water. Films were inserted into the tube furnace that was preset to a temperature of 400 °C, as measured by the thermocouple in the furnace. The data presented in this paper was for 20 minutes of annealing for the 15 nm thick SZTO and 5 minutes for the 5 nm thick SZTO.

Piezo-response force Microscopy - The polarization writing, switching hysteresis loop and time-dependence piezo-response amplitude study of SZTO films on Ge were studied at room temperature with a Bruker multimode 8 AFM working in the contact mode, with a small AC voltage applied to a conductive tip and the substrate grounded, or vice versa (SCM-PIT). Measurements were performed at frequencies close to the cantilever resonance (~300 kHz) with a bias voltage of 200-500 mV, to eliminate any spurious artifacts due to ion migration. [39] To measure the PFM switching hysteresis, we first applied a DC voltage pulse  $V_{\text{bias}}$  with a typical time period of  $t_{\text{pulse}} = 100$  ms, and then measure the PFM response after the removal of the DC bias for a wait time of  $t_{\text{wait}} = 100$  ms. The bias-off technique allows us to eliminate the electrostatic artifact associated with the DC tip bias.[40]

Capacitance-Voltage and Polarization-Voltage measurements - 30 nm thick Ni electrodes ranging in diameter from 20  $\mu\text{m}$  to 270  $\mu\text{m}$  were deposited through a shadow mask using electron beam evaporation. The backsides of the Ge wafers were mechanically scratched and InGa eutectic was applied to form a counter electrode. The C-V and P-V characterizations were performed on a probe station using flexible, 10 micron radii, tungsten probe whiskers. An Agilent 4284A LCR meter was used for the C-V measurements. A Radiant II ferroelectric tester was used for the PUND measurements. For the PUND measurement, each junction was measured 30 times and the data was averaged to improve signal to noise. For the PUND data shown in Figure 2 of the main text, the data was taken on a 270  $\mu\text{m}$  diameter electrode.

Scanning Transmission Electron Microscopy - STEM lamella were prepared using conventional wedge polishing with an Allied Multiprep followed by Ar + ion milling using a Fischione Model 1050, where final milling voltages were 500 V or less,

and where in some cases liquid nitrogen was used to cool the sample stage during milling. Samples were capped with Ni to protect the films during preparation. HAADF-STEM was conducted on a probe-corrected FEI Titan G2 60 – 300 kV operated at 200 kV with a detector inner semi-angle of approximately 77 mrad, and probe semi-convergence angles of either 13.5 or 19.6 mrad. Due to relative beam sensitivity of SZTO, beam currents of 60 pA or lower were used. STEM images were acquired utilizing the RevSTEM acquisition method to remove thermal drift related image distortion.[41] Acquisition parameters included using 20 to 40 1024 pix x 1024 pix image frames recorded with 2  $\mu$ s/pix dwell time and a 90° rotation of the scan coordinates between each successive image. In the case of the 5 nm thick SZTO film samples used for lattice parameter measurements, global residual distortion was removed using images of an Si substrate acquired during the same microscope session.[42] In these images, atom column locations were isolated and indexed.[43] A Gaussian template was used to fit the atom columns in the 5 nm thick films of SZTO, whereas either a Gaussian template or a  $\langle 110 \rangle$  dumbbell template was used to fit the locations of the Ge dumbbells. SZTO and Ge lattice parameters were taken from the same images, and are presented (see Supplementary Information) as the mean and standard error of measurements of four different images acquired from different sample regions and thicknesses, and even from different lamella. The Ge unit cells closest to the interface with SZTO were excluded from the Ge lattice parameter measurement. The deviations of an atom column were determined by taking the difference between the ideal position (the mean position of its four nearest neighbors, which is the cell center) and the measured position. GeO<sub>x</sub> layer thicknesses were measured as the distances between corresponding inflection points in the second derivative of

integrated line profiles taken from non-RevSTEM images. SZTO film thicknesses were measured using the same method and images for comparison (see Supplementary Information). These measurements were averaged over images acquired from different lamella regions and thicknesses.

Density Functional Theory Calculations were performed using the Vienna Ab Initio Simulation Package (VASP).[43-45] The projected augmented wave method was used to approximate the electron-ion potential.[46] Exchange-correlation effects were treated within the Perdew-Burke-Ernzerhof functional form of the generalized gradient approximation, modified for solids (PBEsol).[47] A plane-wave basis with a 500 eV cutoff and a  $2 \times 2 \times 1$  and  $2 \times 2 \times 2$  Monkhorst-Pack k-point meshes were used for the SZTO/STO slab and SZTO bulk, respectively. The charge and spin density distributions were analyzed using the Bader method [48]. The energies of self-consistent calculations were converged to  $10^{-5}$  eV/cell. For the bulk calculation, we consider a SZO  $2 \times 2 \times 2$  supercell and optimized the c-axis lattice parameter with the in-plane lattice parameters fixed at the experimental value of the annealed SZTO films. With the lattice parameters fixed, we then optimize the internal coordinates for a Ti concentration of 12.5%, as shown in Figure 3-12(a). For the SZTO/STO slab, the STO and SZTO parts of the system are three- and five-unit-cell thick, respectively, and a  $2 \times 2$  lateral supercell is used with the in-plane lattice parameters fixed at the experimental value corresponding to the annealed SZTO films.

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## Chapter 4

### Interface trap density

#### 4-1 Conductance method for determination of the interface trap density

In the conductance method, interface trap levels are detected through the loss derived from changes in their occupancy. Majority carriers are captured or emitted by applying a small ac signal that modulated the conduction band level from the semiconductor Fermi level. At the specific frequency traps can immediately respond and therefore the energy loss has minima in frequency. In addition to energy loss, interface traps can also hold an electron for specific time after capture. This emerges a capacitance called  $C_{it}$  proportional to the interface trap density. The equivalent circuit can be extracted from these assumption and their values can be determined by the measured impedance as shown in Figure 4-1. [1]

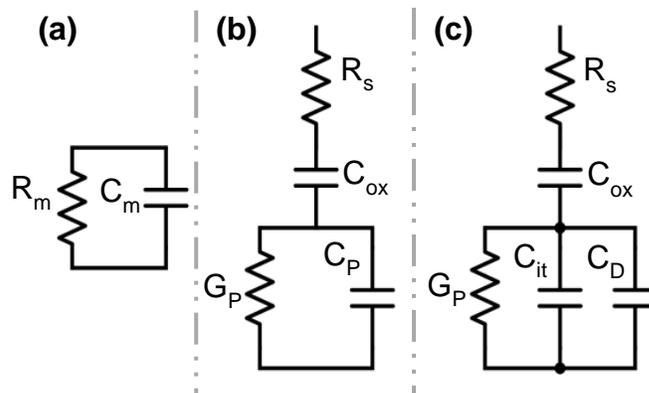


Figure 4-1 Equivalent circuit in conductance method. (a) Measured values by impedance analyzer. (b) Extracted components by applying conductance methods. (c) Complete circuit in depletion.

In this method it is required to calculate the corrected capacitance ( $C_c$ ) and equivalent parallel conductance ( $G_c$ ) from the measured capacitance ( $C_m$ ) and conductance ( $G_m$ ). First the, series resistance  $R_s$  and  $C_{ox}$  can be calculated by :

$$R_s = \frac{G_m}{G_m^2 + \omega^2 C_m^2} \quad 4-1$$

$$C_{ox} = C_m \left(1 + \frac{G_m}{(G_m + \omega C_m)^2}\right) \quad 4-2$$

Then MATLAB code can be used to extract the corrected conductance values  $G_c$  and  $C_c$  in Equation 4-3 and Equation 4-4.

$$C_c = \frac{(G_m^2 + \omega^2 C_m^2) C_m}{[G_m - (G_m^2 + \omega^2 C_m^2) R_s]^2 + \omega^2 C_m^2} \quad 4-3$$

$$G_c = \frac{(G_m^2 + \omega^2 C_m^2) [G_m - (G_m^2 + \omega^2 C_m^2) R_s]}{[G_m - (G_m^2 + \omega^2 C_m^2) R_s]^2 + \omega^2 C_m^2} \quad 4-4$$

For each frequency sweep conductance calculated by

$$\frac{G_P}{\omega} = \frac{\omega C_{ox}^2 G_c}{G_c^2 + \omega^2 (C_{ox} - C_c)^2} \quad 4-5$$

As it is explained by E. H. Nicollian and J. R. Brews this conductance is also theoretically related to surface potential fluctuation ( $\sigma_s$ ) and band bending as it shown in Equation 4-6.

$$\frac{G_p}{\omega} = \frac{q}{2} \int_{-\infty}^{+\infty} \frac{D_{it}}{\omega\tau} \ln(1 + \omega^2\tau^2) P(\sigma_s, E) dE \quad 4-6$$

Where P is a Gaussian distribution with variance  $\sigma_s^2$  and time constant  $\tau_p$  is the hole interface-trap time constants. At the  $(G_p/\omega)_{\max}$  the integral in Equation 4-6 that can be simplified by considering its maximum value of 0.4 (associated with  $\sigma_s=0$ ) which appears as a constant of 2.5 in Equation 4-7 by considering its minimum possible value.

$$D_{it} = \frac{2.5}{Aq} (G_p/\omega)_{\max} \quad 4-7$$

#### *4-2 interface trap density in UP and DOWN polarization*

The conductance method is a very well established and accurate method for determination of the interface trap density. For small bandgap materials such as Ge it is sometimes recommended to apply these measurements in lower temperature. Here we applied the measurement in room temperature for the ferroelectric on semiconductor MOS capacitor. The focus of this study is on comparing the UP and DOWN polarization state interface trap densities. Here we applied a voltage jump to +3V or -3V to pol the ferroelectric in pre-determined state and then applied a small bias near depletion based on the hysteresis C-V characterization. The typical C-V measurement discussed in previous chapters is measured and shown in Figure 4-2 for the small pad size with the surface area less than  $1000 \mu\text{m}^2$  to avoid large series resistance.

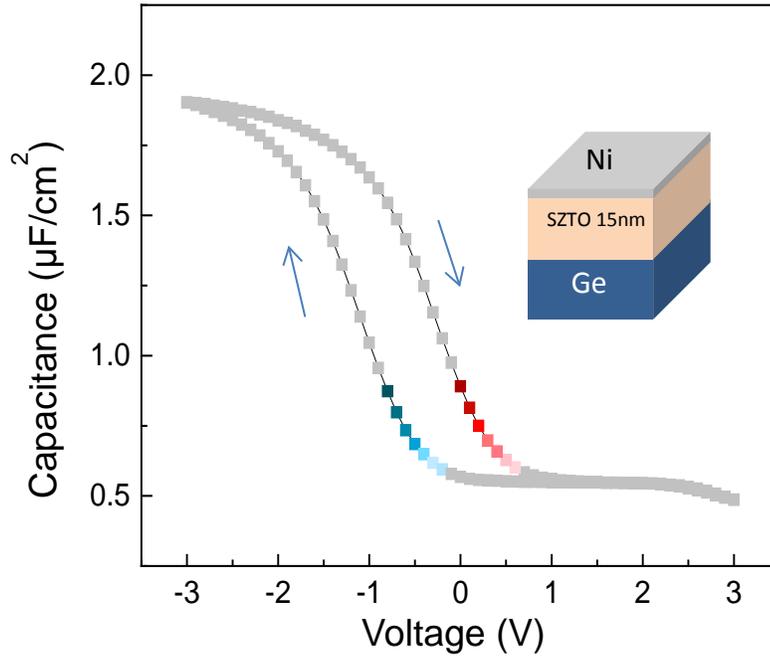


Figure 4-2 C-V characteristic of the 15nm SZTO on p-Ge. The red and blue points are selected on UP and DOWN polarization states respectively to calculate the interface trap density.

The polarization was switched to UP or DOWN states prior to conductance measurement near the depletion mode.[3] the color coding of red and blue in Figure 4-2 is associated with UP and DOWN polarization respectively and  $G_p/\omega$  information extracted by sweeping a frequency on logarithmic scale to obtain the maximum value. The result of this study is shown in Figure 4-3(a) for UP and Figure 4-3(b) for DOWN polarization respectively. By using Equation 4-7 the maximum numerical value for the interface trap density for UP polarization ( $D_{it \text{ max UP}}$ )  $1.2 \times 10^{13} \text{ eV}^{-1} \text{ cm}^{-2}$  and for the DOWN polarization  $D_{it \text{ max DOWN}}$  is  $6.4 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$ . Beside the amplitude change in different polarization, from the Figure 4-3 it can be seen that the frequency of the maximum has also shifted.

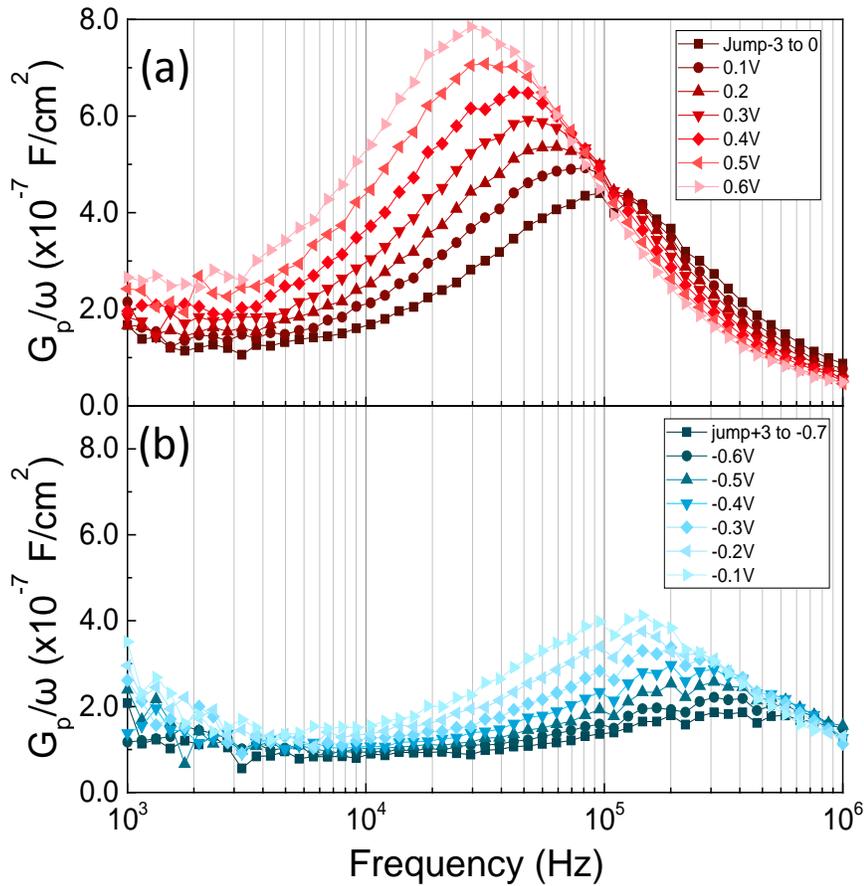


Figure 4-3 Conductance  $G_p/\omega$  vs. frequency for several bias points near depletion region. (a) UP polarization, the  $D_{it \text{ max}}$  for this state is  $1.2 \times 10^{13} \text{ eV}^{-1} \text{ cm}^{-2}$ . (b) For the DOWN polarization  $D_{it \text{ max}}$  is  $6.4 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$ .

One possible explanation for this change can be the variation of the capture cross section by the proximity of the polarization charges to the interface. In Equation 4-6 the log function has much slower variation than the  $1/x$  function. It means that by reduction of the  $\tau_p$ , the  $(G_p/\omega)_{\text{max}}$  will increase. It also important to note that the trap capture rate (holes in the case of p-doped Germanium) is given by Equation 4-8:

$$\tau_p = \frac{1}{c_p N_A} \quad 4-8$$

Where  $c_p$  is a capture cross section and  $N_A$  is the acceptor density. From Figure 4-4 it can be seen that in UP polarization (red) the negative charges due to polarization are closer to the interface, creating a deeper potential well and therefore capturing more residual charges at interface trap. For the opposite DOWN polarization (blue) the positive charges create a shallower well and therefore decrease the capture rate.

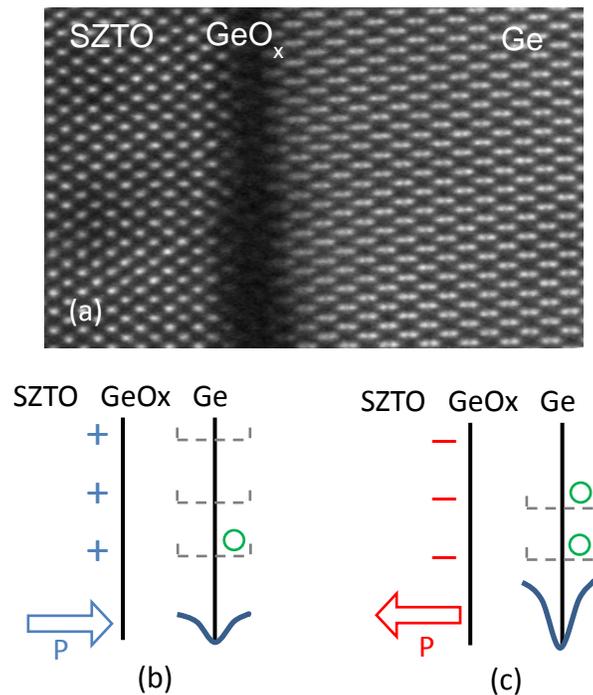


Figure 4-4 STEM image of the SZTO-Ge interface and illustration of polarization effect on capture rate. (a) SZTO-Ge interface. (b) DOWN polarization where lower potential well attracts less hole minority carriers. (c) UP polarization when negative bound charges near interface generate deeper potential well and attract more holes in comparison to DOWN polarization resulting different interface trap density between these two states.

As a result , by looking at Figure 4-2 and selecting points parallel to x-axis (with the same capacitance) it is possible to find a ratio of the capture rate in Equation 4-9:

$$\frac{\tau_p UP}{\tau_p DOWN} = \frac{f_{max} DOWN}{f_{max} UP} = 0.53 \quad 4-9$$

This shows that the change in the interface trap capture rate can be varied around 50% depending on the polarization and history of the junction. This study and possible reasoning is presented for the first time here.

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## Chapter 5

### Summary

We have applied principles of band-gap engineering to manipulate the band alignment between single crystalline SZTO and Ge, in which the band-gap of the former is enhanced through Zr content. Atomically abrupt and structurally coherent interfaces between SZTO and Ge can be achieved through careful control of kinetic and thermodynamic conditions during deposition. Current-voltage measurements show a significant decrease in gate leakage with Zr content, and capacitance-voltage measurements indicate that inversion can be achieved. These results demonstrate that band-gap engineering can be exploited to realize functional semiconductor crystalline oxide heterojunctions. SZTO can serve as a high-, perovskite structured electrical platform for integrating dielectric, ferroelectric and ferromagnetic functionalities of oxides onto semiconductors. The ability to electrically couple multifunctional oxides with semiconductors would enable a range of device technologies to be realized, advancing the oxide - semiconductor interface well beyond the paradigm of the metal-oxide-semiconductor capacitor.

we have realized ferroelectric MOS capacitors exhibiting ~ 2 V wide hysteretic C-V characteristics with a corresponding EOT of 1.0 nm using 5 nm thick, single crystalline SZTO. Through the epitaxial growth of SZTO on Ge, we have achieved continuity in the electric displacement, a type-I band offset, and robust ferroelectricity at nanoscale film thicknesses. The emergence of ferroelectricity in thin films of SZTO on Ge demonstrates how reduced dimensionality, strain and applied electric fields can be exploited to realize technologically important material behavior in multifunctional

oxides. The realization of a materials platform that combines nanoscale ferroelectrics with semiconductors opens new vistas for Nano-electronic devices.

Finally, we have applied the well-known conductance method for determination of interface trap density to our MOS/MFS capacitors. We have shown that presence of the polarization charge near the interface can affect the capture and release time and change the interface trap density in UP and DOWN polarization.

From my experience by looking into this universe, I realized that my knowledge is very limited. When we look into the unknown matters and try to explore them, we generate more unknowns. This can be confusing and stressful from time to time, but I am sure the architect of such a wonderful system that finessed all these details, had enjoyed doing it, therefore we should enjoy looking into it.

## Biographical Information

Reza M. Moghadam was born in Tehran, Iran, on May 1977. After graduation from Isfahan University of Technology in 2001 he entered the Electrical and Computer Engineering Research Center (ECERC) in 2002 and was a cofounder of Plasmatavan Company at Isfahan Science and Technology Town (ISCT) in 2007. He entered the Master of Science degree at University of Arlington in Texas in 2009 and PhD in 2012. He was a graduate student coordinator and camp director for the NSF REU site on sensors and application from 2012-6 recruiting and hosting more than 35 undergraduate students for the summer program. He started to work at the Physics department in an Oxide MBE field. He has several publications, including one provisional patent and many conference presentations in the field of oxide materials on semiconductors. His cover page design was also selected for the Advanced Materials Interfaces journal in 2016. Reza is a student member of IEEE, HKN honor society of electrical engineers, APS, AAAS, MRS, order of engineers and student physics society of UTA.