THERMO-MECHANICAL FEASIBILITY STUDY OF COPPER AND GOLD WIREBONDS IN 3D ELECTRONIC PACKAGE

by

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Abstract

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3 Dimensional (3D) Electronics Packaging has emerged as a revolutionary trend in the micro-electronics industry. It has made possible cost-effective system integration and size scaling while reducing the interconnect delay. The ever increasing demand for better mechanical, thermal, electrical performance, improved reliability and cost effective semiconductor manufacturing technology has encouraged the engineers to replace Gold (Au) by Copper (Cu). In a survey conducted by Semiconductor Equipment and Materials International, to study the industry mood related to wirebond technology, it was observed that 72% of the leading semiconductor companies are considering switching to Cu [1]. The only major concern regarding the use of Cu as an interconnect material is the in-service product reliability and unproven historical record. To facilitate a smooth transition from Au to Cu there is a need to carryout in depth research and analysis since material changes require requalification. Since there is a dearth of study on the reliability of Cu wirebond packages there is an urgent call for research to address the needs of ever growing semiconductor industry.

Thermo-Mechanical stresses are introduced in a package during fabrication processes or field use due to constant rise and fall in temperature. The mismatch in the Coefficient of Thermal Expansion (CTE) between various components results in significant mechanical stresses in the package. The overmold and wirebond have a considerable difference in there CTE's. Finite Element model was developed to simulate reliability tests for 3D wirebond package. Reliability test, Accelerated Thermal Cycling (ATC) or Thermal

shock test was simulated on a 3D wire bonded package. The thermo-mechanical response of package during Accelerated Thermal Cycling test was studied. Comparative analysis of thermo-mechanical response of the packages was carried out for different overmold compounds. Creep behavior of materials is used to capture their response during various temperatures and with time. Bilinear hardening curve is used to capture plastic deformation. Further the mechanical response of gold wirebond package is compared with that of copper wirebond package. The results were further utilized to carry out a parametric analysis to study the effect of wirebond diameter and number of wirebond on mechanical behavior the package.

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Chapter 1

Introduction

1.1 Introduction To Electronic Packaging And Wirebond Packages

1.1.1 What Is Electronic Packaging?

Electronics Packaging is the method of enclosing electronic components, assemblies of electronic components or finished electronic devices. Packaging of electronic components facilitates their protection from physical damage and moisture, helps in thermal management by controlled heat dissipation, circuit support and protection, signal distribution, power distribution etc. Low cost, small size and multi-functional electronic products are important drivers for the electronic packaging industry. Hence the industry is changing at a fast pace to keep up. In response to these requirements, packaging related areas such as design, packaging architectures, materials, processes and manufacturing equipment are all changing at a fast pace. Electronic Packaging is a multi-disciplinary field and requires the contribution of mechanical, thermal, structural, manufacturing, electrical, computer engineering, material science, physicists etc.

1.1.2 Hierarchy In Electronics Packaging

There are different levels in electronic packaging depending upon the location of the interconnect technology. The figure below shows some of the levels in packaging.

Level 0 -Gate to gate interconnections in silicon die

Level 1 -Chip to package interconnect

Level 2 -Component and PCB connection

Level 3 -Connection between PCB and motherboard

Level 4 -Connection between various assemblies

Level 5 -Connection between physically separate systems, LAN Ethernet etc.

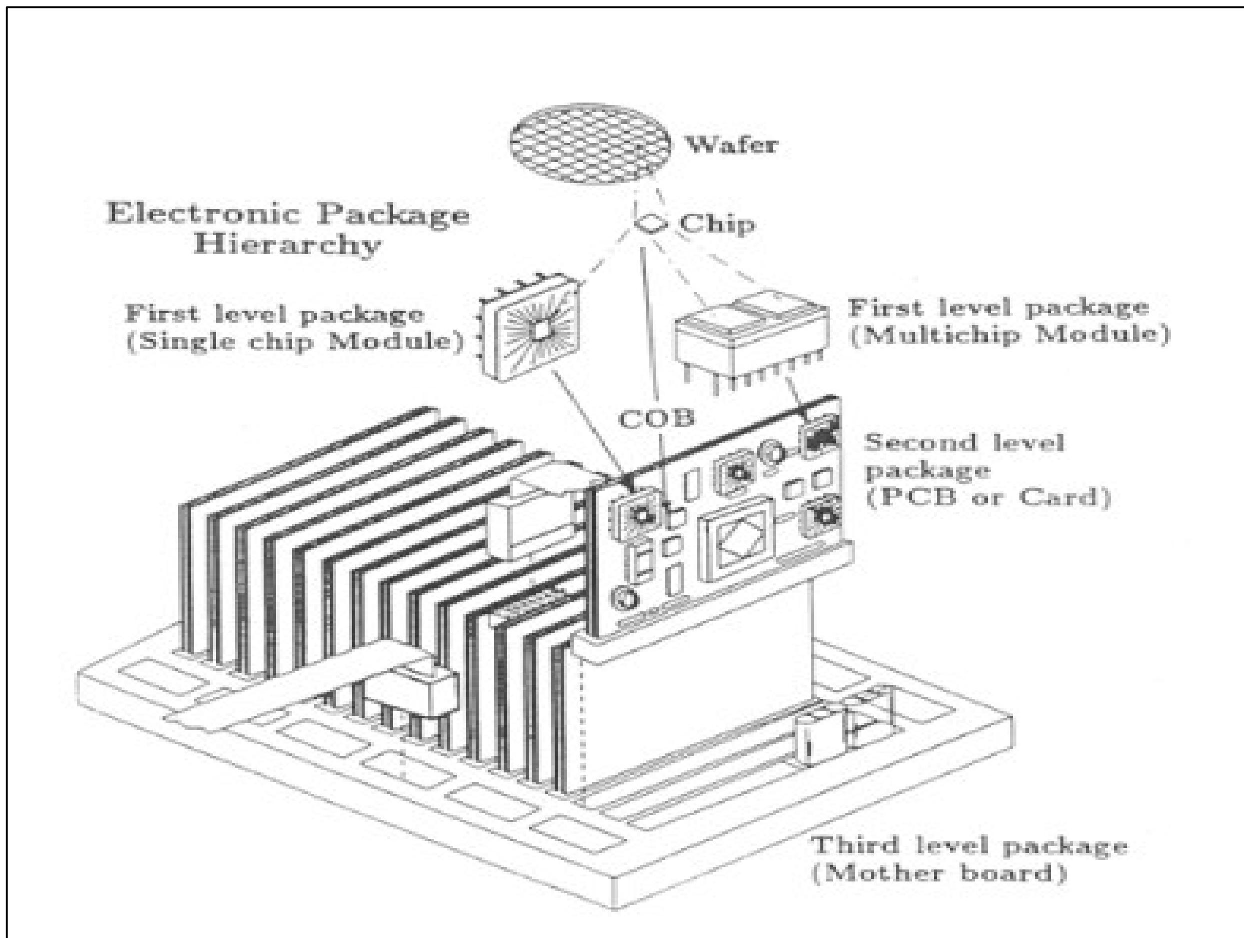


Figure1.1 Hierarchy of Interconnection levels [2]

Silicon Chip is obtained by extracting it from the silicon wafer. It is then placed on the carrier to protect and house it. This is known as the first level package. The first level package is then placed onto a Printed Circuit Board. The board not only carries these components on top and below but also interconnects every component with conductor wiring to form an interconnected system. This is known as the second level package. The third level package is then the assembly of second level package, connectors, cables etc. For the optimal and reliable working of the electronic products different thermo-mechanical techniques could be implemented based on the level of the package [2]. Figure 1.1 shows the packaging hierarchy with the different levels.

1.2 Thermal Management

In recent years, heat-sensitive electronics systems have been miniaturized far more than their heat-producing power supplies leading to major design and reliability challenges and making thermal management a critical design factor. There are three basic issues at the core of effective thermal management - how and where the heat is generated; how the temperature at a given point in the circuit is determined; and how the heat is removed [7]. Thermal management may employ different modes of heat transfer at different levels.

1.2.1 First / Device Level Cooling

The first / device level that forms the bottom of the packaging hierarchy comprises of the chip package that houses and protects the chip. Conduction of heat from the chip to the package surface and then into the printed wiring board is the primary concern for the thermal management at this level. In order to lower the chip temperature, reduction of thermal resistance between the die and the package surface would be the most effective way. This reduction in temperature can be brought about by using die attach adhesives with high conductivity, thermal greases. The cooling can be brought about by active cooling techniques such as by using heat sinks, jet impingement and dielectric liquids etc. [1].

1.2.2 Second / Package Level Cooling

The second / package level comprises of the printed circuit board where the heat removal occurs by conduction in the printed circuit board and by convection to the ambient air. Printed circuit boards with high thermal conductivity with heat sinks or heat pipes attached to the back side are some of the ways to take away the heat from the printed circuit board. Some of the other ways by which heat can be removed from the printed circuit board would be by fans or blowers that create internal air flow loops [1].

1.2.3 Third / System Level Cooling

The third / system level comprises of the motherboard which interconnects the printed wiring. Active thermal control measures such as air handling systems, heat pumps,

refrigeration systems are some of the thermal management criteria's at this level. The cooling of the rack or module can be done by the natural circulation of air depending on the application [1]. So the thermal aspects of third / system level cooling are the thermodynamic considerations, overall system balance and the application [8].

1.3 Mechanical Reliability

In the context of this overview reliability is defined as the ability of a device to conform to its electrical/visual or mechanical specifications over a specified period of time under specified conditions at a specific confidence level. In an electronic package the reliability of solder joints are of utmost concern as they are one of the most fragile elements of a package (mainly due to the fact that they are small in size and used at high temperatures relative to the melting points). For the improvement of solder joint reliability of any electronic package there has to be a good understanding of solder joint failures [9].

Temperature fluctuations caused due to power transients or environmental changes along with the resulting thermal expansion mismatch between the various package materials results in time and temperature dependent creep deformation of solder. With repeated cycling the deformation accumulates thereby causing solder joint cracking and interconnect failure.

1.4 Trends In Electronics Packaging

In 1965, Gordon E. Moore published a paper "Cramming more components onto integrated circuits". He observed that over the history of computing, the number of transistors doubles approximately every two years, figure 1.2. The semi-conductor industry has used this law for long term planning. The trend has continued for more than half a century and is expected to continue for at least another decade or so. Also the chip power has increased and will keep on increasing in the coming years.

Recently, the global semiconductor industry is seeing a new trend called "More-than-Moore" (MtM), where added values to devices are provided by incorporating functionalities that do not necessarily scale according to Moore's Law. [2] Due to the

physical properties of the chip, Moore's Law will one day face its ultimate limitation. While packing more transistors on a chip to add power and performance is still a key focus, developing novel MtM technologies on top of the Moore's Law technologies to provide further values to semiconductor chips has also become important.

That's what gave rise to MtM, which is symbiotic with Moore's Law and allows non-digital functionalities to migrate from the system board-level into the package (SiP) or onto the chip (SoC). More-than-Moore technologies cover a wide range of fields. For example, MEMS applications include sensors, actuators and ink jet printers. RF CMOS applications include Bluetooth, GPS and Wi-Fi. CMOS image sensors are found in most digital cameras. High voltage drivers are used to power LED lights. These applications add value to computing and memory devices that are made from the traditional Moore's Law technology.

The combined need for digital and non-digital functionalities in an integrated system is translated as a dual trend in the International Technology Roadmap for Semiconductors: miniaturization of the digital functions (“More Moore”) and functional diversification (“More-than-Moore”).

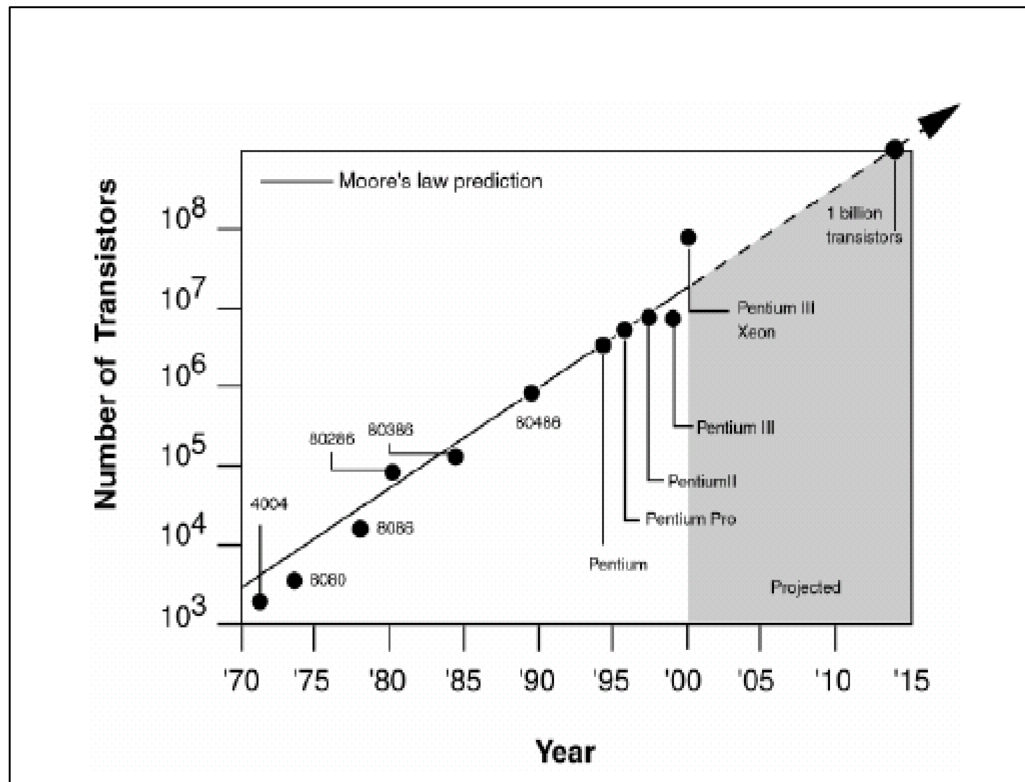


Figure 1.2 Moore's Law [1]

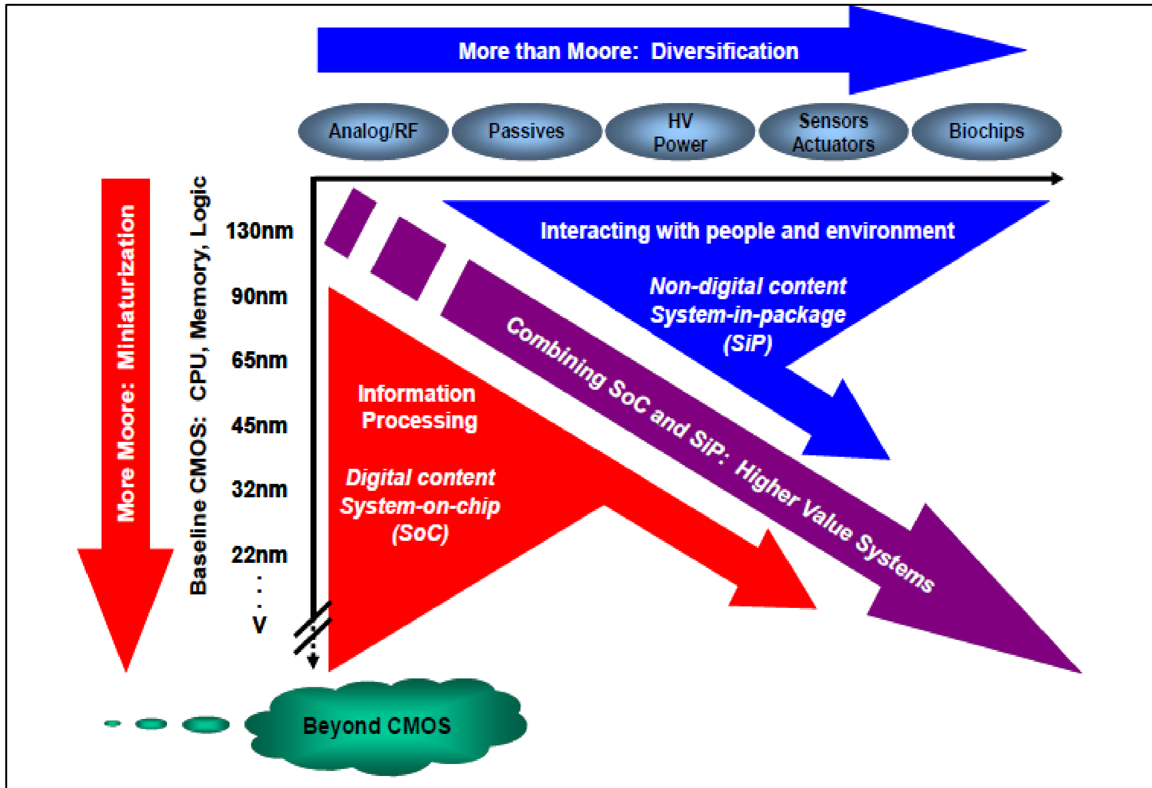


Figure 1.3 More than Moore [2]

1.5 3D Packaging Technology

Packaging has been the "silent partner" in electronics and information advances in the last three decades. Yet the desire for increased speed, density and affordability has increased the importance of this silent partner so that in some applications the packaging of the IC is the critical enabler in meeting customer requirements [10].

An IC is complete only when it has a suitable package. A package has to provide power to the chip as well as heat dissipation path for it in addition to protecting the IC from mechanical damage from outside elements. There are different types of chip packaging technologies available of which 3-dimensional (3D) packaging is considered to be one of the most efficient.

1.5.1 3D Packaging Technology

Continuous demand for miniaturization, increased functionality, better performance and lower cost has forced the electronics industry to shift from traditional packaging techniques to advanced packaging technologies such as stacked packaging, Package on Package (PoP) etc. This has resulted in increased packaging density thereby satisfying the current requirements [11]. Vertical integration of chips in a single package multiplies the amount of silicon that can be squeezed in a given package footprint and more data functions per cubic centimeter (cc) of application space, conserving less board real estate. In stacked packages, two or more silicon dice are stacked within a single package. Different die arrangements such as rotated, staggered, pyramid etc. are commonly adopted [12, 13]. The increasing trend of die stacking is shown in figure 1.4.

3D packaging technologies exploit the third or Z height dimension to provide a volumetric packaging solution for higher integration and performance. As a result 3D packaging has become critical in integrating the multi-media features and consumers demand in smaller and lighter products. This increasing functionality requires higher memory capacity in more complex and efficient memory architectures. 3D packaging as a result is experiencing high growth and new applications by delivering the highest level of silicon integration and area efficiency at the lowest cost [16].

A microelectronic device might consist of a number of packages that are mounted near each other on a single PCB thereby consuming a lot of real estate. As a result the size of the device increases and this type of configuration is referred to as 2D packaging. Hence some of the drivers of 3D integration are a) Interconnection in the third dimension which results in reduced chip area producing better yields and shorter global interconnection which gives better performance. (b) Logic plus memory: 2D interconnect results in long interchip connections between logic and memory, SOC solutions results in

large die and intrachip connections whereas 3D with through silicon vias provides the shortest interconnect between logic and memory functions [17].

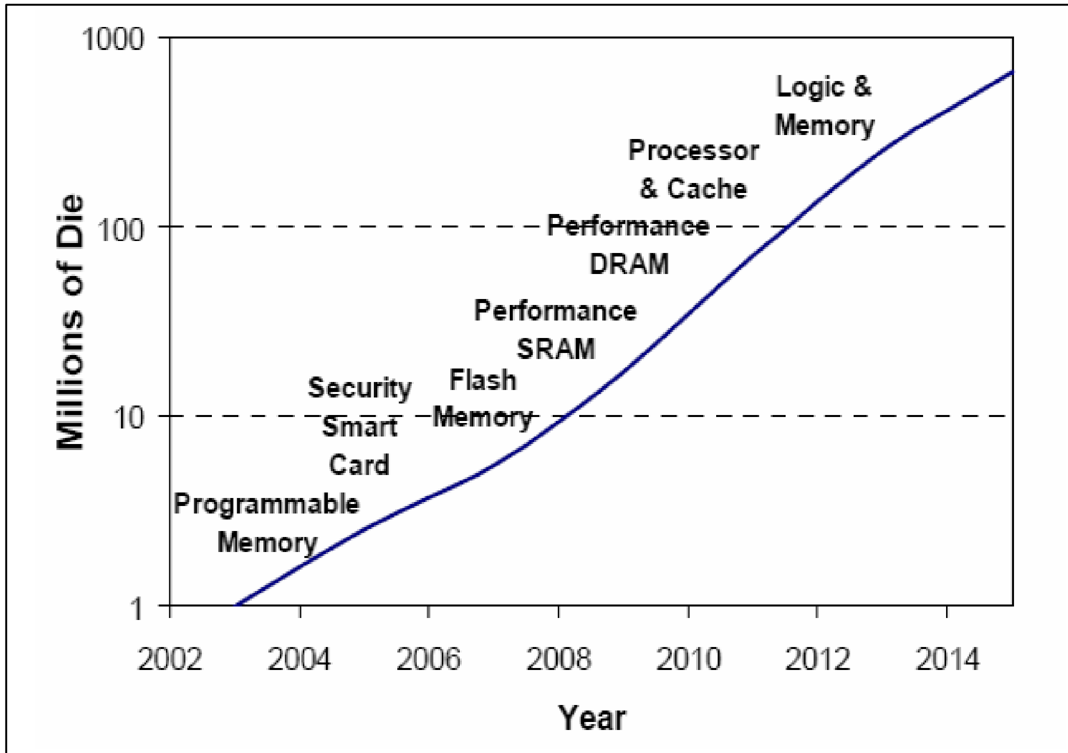


Figure 1.4 Die Stacking trend [13]

Based on the interconnects, the packages can be classified as wire bond package, flip chip (FC) package, ball grid array package (BGA) and chip scale package (CSP). These packages have their applications depending on the requirement. In wire bond packages, the wire bonds are the primary method of making interconnections between an IC and a PCB during semiconductor device fabrication. Although less common, wire bonding can be used to connect an IC to other electronics or to connect from one PCB to another. It is generally considered the most cost-effective and flexible interconnect technology and is used to assemble the vast majority of semiconductor packages. Bond wires are usually of one of the following materials: aluminum, copper or gold. The wire diameters start at 15 µm and can be up to several hundred micrometers for high-powered applications [5].

In flip chip packages, the interconnection between the die and the carrier is made through a conductive "bump" that is placed directly on the die surface. The bumped die is then "flipped over" and placed face down with the bumps connecting to the carrier directly. Once the die is soldered, underfill is added between the die and the substrate. Underfill is a specially engineered epoxy that fills the area between the die and the carrier, surrounding the solder bumps that are designed to control the stress in the solder joints caused by the difference in thermal expansion between the silicon die and the carrier [16].

Ball Grid Array or BGA is a surface-mount package that utilizes an array of metal spheres or balls as the means of providing external electrical interconnection. The balls are composed of solder and are attached to a laminated substrate at the bottom side of the package. The die of the BGA is connected to the substrate either by wire bonding or flip-chip connection. The substrate of a BGA has internal conductive traces that route and connect the die-to-substrate bonds to the substrate-to-ball array bonds. The main advantage of BGA as a packaging solution for integrated circuits is its high interconnection density, i.e., the number of pins (or balls, rather) that it offers per given package volume is high. A related advantage arising from this high I/O density is its small board space occupation [9].

A chip scale package or CSP is a type of integrated circuit chip carrier where the package area is no greater than 1.2 times of the die and it must be a single die. To qualify a package as a CSP its ball pitch should me no more than 1 mm [5].

1.5.2 Benefits of 3D Packaging Technology

In the webcast, “Ultra-Thin Wafer Processing Solutions” [21] and one of the white papers by Waytronx, Inc. [22], Steven Koester from CMOS technology at IBM, East Fishkill, N.Y. noted that “3D Integration will establish a new scaling path that will extend Moore’s Law beyond its expected limits”. Based on this, 3D packaging has the following benefits.

1. Shorter Interconnects:

The wiring does not scale down the way transistors do as the width of the wires is

reducing but not its length. Hence stacking of dice is a feasible solution that can allow interconnects to go between the dice thereby reducing their lengths upto 1000 times.

2. Increased System Performance:

In order to keep the system performance close to on-chip performance, high speed interconnections are necessary. 3D packaging can shorten communication paths, increase bus speeds and open up performance through economic parallel, fabric communications.

3. Reduction of Size and Weight:

3D packaging allows 40-50% reduction in weight and size and 5-6 times reduction in volume compared to conventional packaging [23].

4. Reduction of Signal Time Delay:

Shorter interconnection length and closer proximity of electronic components helps to reduce the signal time delay [24].

5. Reduce Power Consumption:

Boosting signals and combating low signal to noise in high speed chip interconnections takes away a significant percentage of system power.

6. Faster Time to Market:

By stacking the chips together, known good functions from the previous generation IP can be quickly integrated to achieve faster time to market, thereby reducing the development and engineering costs. Also the system functionality can be proven prior to production.

7. Speed:

Power saving achieved using 3D technology allows the 3D device to run at a faster rate of transitions per second with no increase in power consumption [25].

1.5.3 Limitations of 3D Packaging Technology

In any technology there are some tradeoffs that need to be performed for efficient operations. Some of those in 3D packaging are as follows

1. Design Complexity:

Although Moore's law when applied to IC design lasts for approximately 18 months, the size of wafers have been increasing at a faster rate than the present 3D technology allows for.

2. Thermal Management:

Thermal management is a very important factor in designing of 3D packages because of high power density.

3. Design Software:

This is one of the problem areas for 3D packaging as most of the design tool kits used are limited to manufacturers rather than having universal access. There is a need for the manufacturers to put their design rules in a format that is available in the popular design tools which would make it easily accessible to the designers [26].

4. Micro warming:

Micro warming starts at the transistor level and protracts to the integrated environment within and surrounding advanced devices. It is pervasive in every level of digital integration [22].

1.6 Different Types Of 3D Packaging Technologies

Increased functionality in a smaller area, high performance computing are some of the reasons for the development of 3D packages. They can be classified as stacked packages, Package on Package (PoP), Package in Package (PiP), Through Silicon Vias (TSVs).

Stacked die packaging is a packaging technology where two or more dice are stacked in a single package or multiple packages. Some of the benefits observed as a result are as follows:

- Smaller, thinner and lighter packages
- Reduced packaging costs and components
- Reduced system level cost for system in package (SiP) vs. System on Chip (SoC)

- Reduced system level size due to smaller footprints and decreased component count [27]

Stacked package have four different type of architectures and they are divided as pyramid, rotated, spacer and staggered.

Package on Package (PoP) has emerged as the vertical stacking solution to stack logic processor with memory due to its testability, business flow and configuration flexibility issues. The PoP solution typically consists of the logic processor in the bottom package and the memory device in the top package. PoP stacks discrete packages thus enabling greater flexibility of signal routing and resolve known good die (KGD) issue.

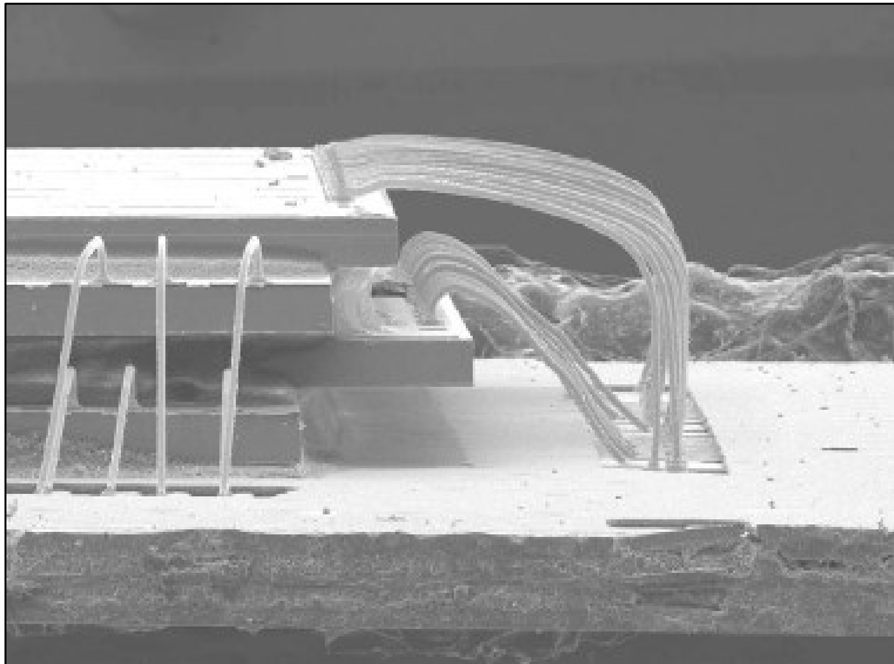


Figure 1.5 Stacked Package [3]

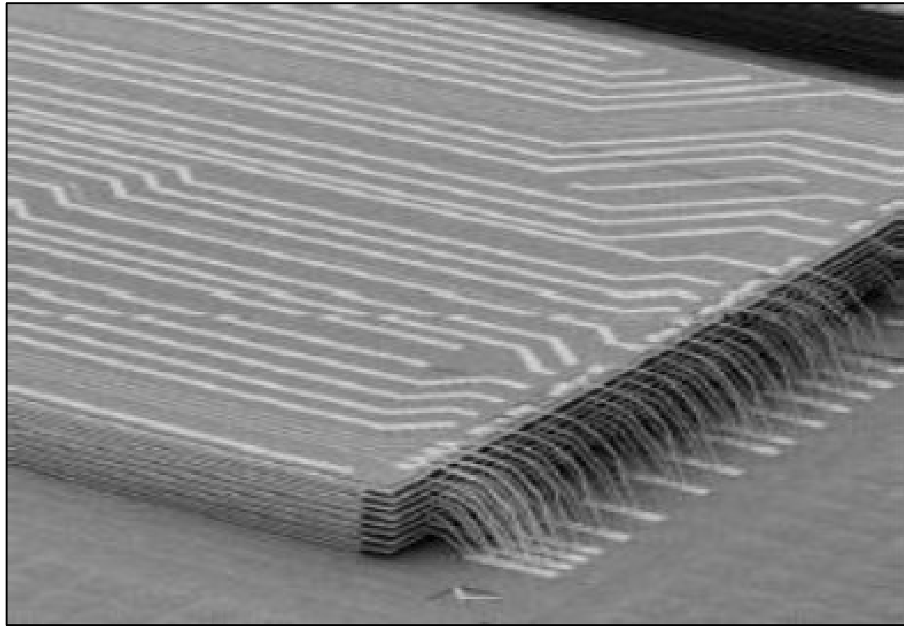


Figure 1.6 Multi Die Stacked package [3]

Chapter 2

Wirebond Electronic Package

2.1 Wirebond Electronic Package

Wirebonds are the most commonly used technique for first level interconnect. The technique for gold wirebonding in PEMs uses a combination of heat, pressure and/or ultrasonic energy to produce the bond. In the wirebonding process, a high bonding force can lead to material deformation, breaking up of any contamination layer and smoothing out surface asperity, but may also damage the silicon. This process can be enhanced at lower bonding energy by the application of ultrasonic energy. Heat can also improve the bonding by accelerating inter-atomic diffusion and thus, bond formation. The two major wirebonding techniques are ball bonding and wedge bonding.

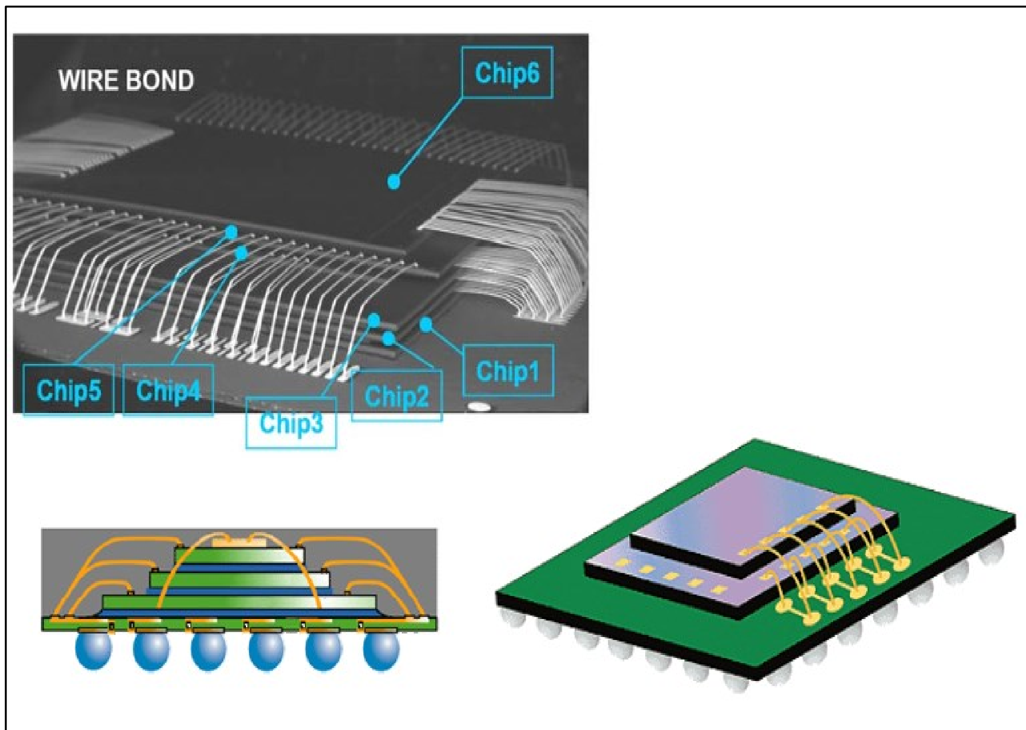


Figure 2.1 Wirebond Package [37]

2.1.1 Ball Bonding

In this technique, wire is forced out of a nozzle with hollow capillary. An EFO system (Electronic Flame off) is used to melt the wire at predetermined location. The ball bond is placed over the aluminum pad. The capillary-nozzle system exerts enough pressure on the aluminum pad to ensure there is intermetallic diffusion and hence a contact bond is formed as the material solidifies. The capillary is then raised and it moves to a substrate to place a wedge or stitch bond.

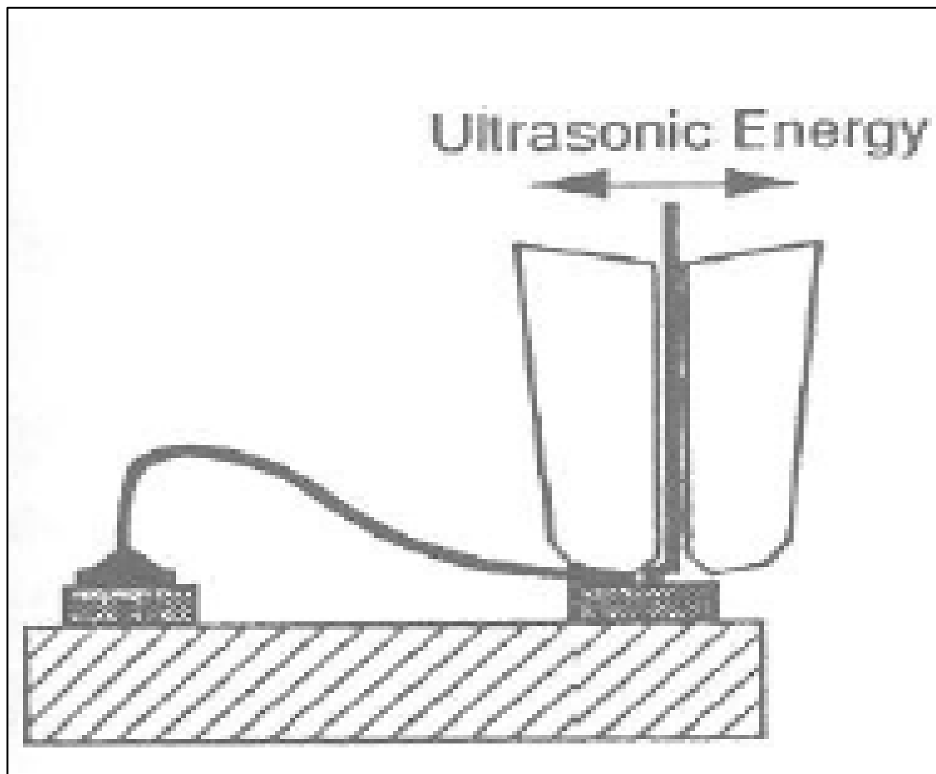


Figure 2.2 Capillary is used to place the ball bond [12]

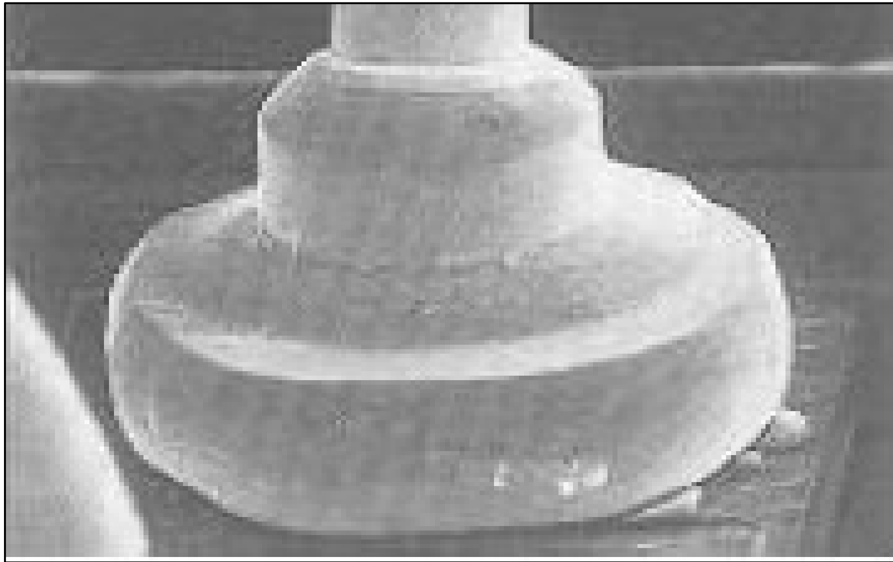


Figure 2.3 Ball Bond [12]

2.1.2 Wedge Bonding

In wedge bonding a wedge bond is placed at both the chip side and substrate side. The wedge bonding derives its name from the tool used for creating the bond. The wedge bond or sometimes called as stitch bond is of the shape of a fish tail. As can be seen from the figure below the wire is fed in a certain angle. The angle ranges from 30 to 60 degrees. This is done to ensure there is no edge shorts.

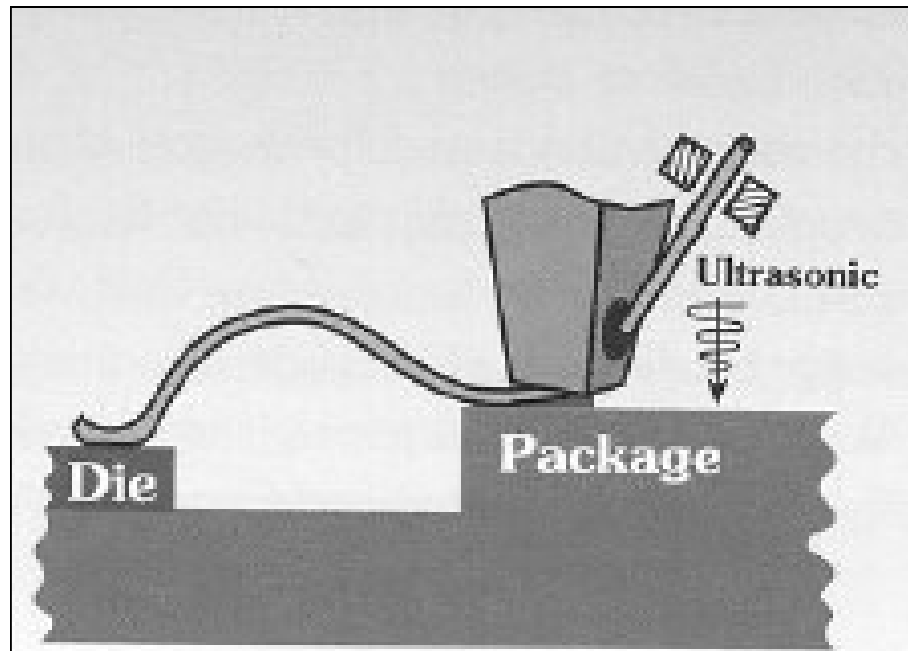


Figure 2.4 Wedge tool is used to place a wedge bond [12]

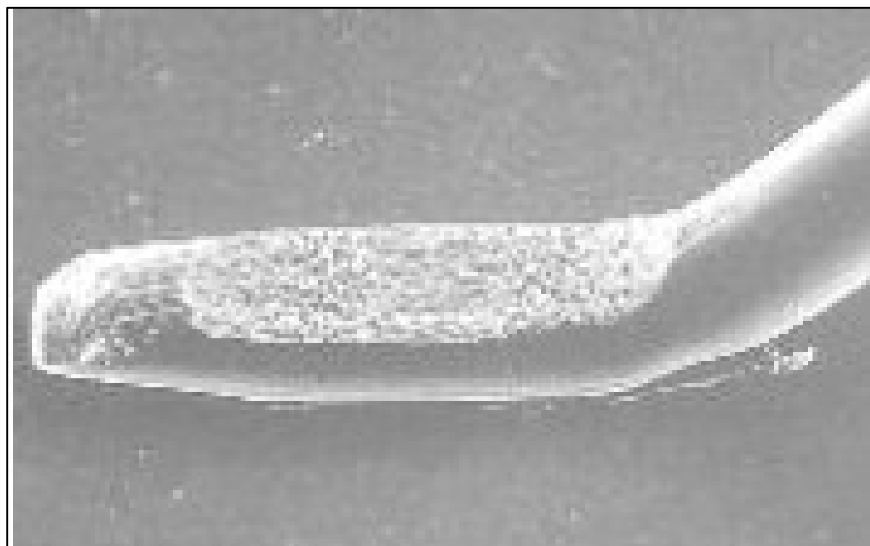


Figure 2.5 Wedge Bond [12]

2.2 Gold Wirebonding

Au wire bonds are being used since a long time, over 50 years. However due to the ever speculative escalating prices of Au the semi-conductor industry is trying to replace Au with Cu due to the superior properties of Cu. Engineers today have a task to replace the material with an economical material without any impact on the reliability. Also with the introduction of new materials there reliability and performance needs to be tested. The question ponders if the existing reliability tests are valid and whether there are any new undiscovered failure modes with the new materials [2]. The table below shows the comparison of material properties between Au and Cu properties.

2.3 Copper Wirebonding

After years in which the semiconductor industry postponed the introduction of copper wire bonding between silicon die pads and package leads, copper wire bonding technology has finally gained traction as a mainstream IC assembly solution. In the past, chip manufacturers relied on gold wiring because it is easy to work with, but gold has performance limitations that make it less than ideal in some applications. In addition, manufacturers needed to find an alternative solution against the rising cost of gold to ensure a steady, more stable supply to high-volume customers. Table 1 shows the comparison between the properties of gold and copper

Table 2.1 Comparison of properties of Gold and Copper

Property	Gold Wire	Copper Wire
Young's Modulus	79000 MPa	123000 MPa
CTE	14.2 ppm/°C	16.5 ppm/°C
Yield stress	200 MPa	160 MPa
Electrical Resistivity	2.2 10-8 ohm.m	1.7 10-8 ohm.m

2.3.1 Challenges In Copper Wirebonding

While copper might seem to be a natural fit for chip-to-package wiring because of its favorable cost, high electrical conductivity and other characteristics, in fact it presents a number of manufacturing challenges which hindered adoption. One of the major challenges in using copper is higher brittleness and hardness than gold. It has been observed that this damages the aluminum pad surface and the circuits beneath it. Also there are series of fabrication challenges in copper wirebonding. Copper oxidizes faster than gold. Gold is virtually inert material. But over the past decade, many semiconductor companies have dedicated development efforts and considerable quality and reliability testing in order to overcome these challenges. Figure below shows the new manufacturing technology developed to overcome these challenges.

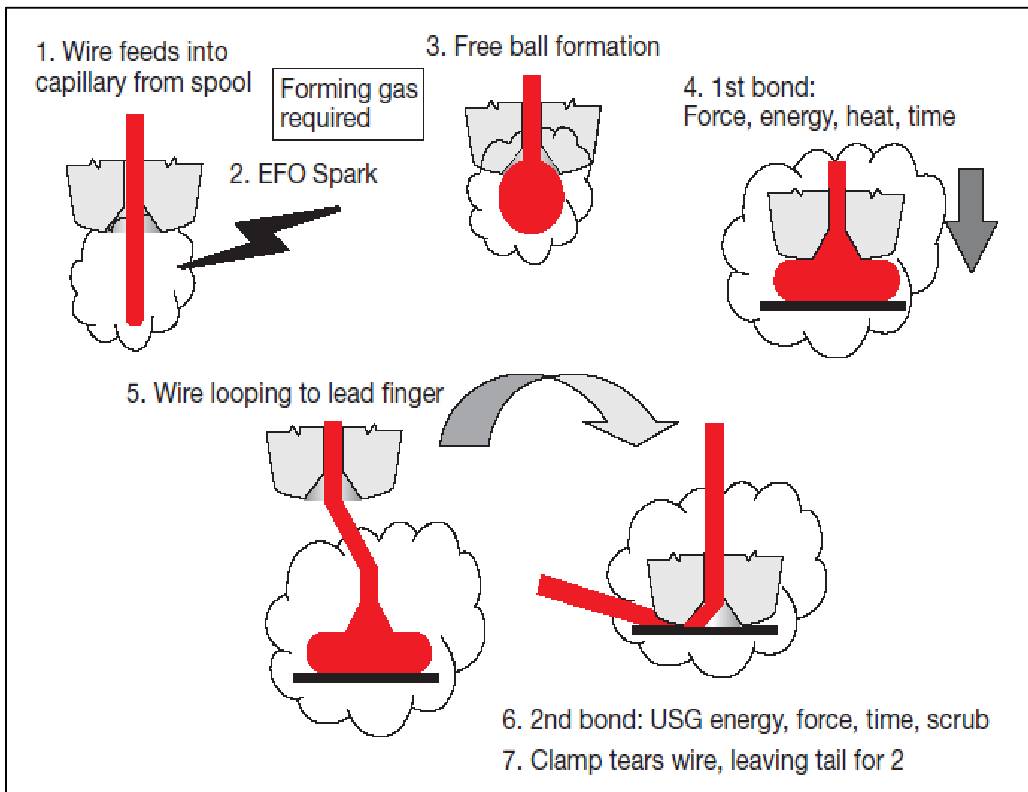


Figure 2.6 Forming gas used to prevent copper oxidization [11]

2.4 Objective And Motivation Of This Work

3 Dimensional (3D) Electronics Packaging has emerged as a revolutionary trend in the micro-electronics industry. It has made possible cost-effective system integration and size scaling while reducing the interconnect delay. The ever increasing demand for better mechanical, thermal, electrical performance, improved reliability and cost effective semiconductor manufacturing technology has encouraged the engineers to replace Gold (Au) by Copper (Cu). In a survey conducted by Semiconductor Equipment and Materials International, to study the industry mood related to wirebond technology, it was observed that 72% of the leading semiconductor companies are considering switching to Cu [1]. The only major concern regarding the use of Cu as an interconnect material is the in-service product reliability and unproven historical record. To facilitate a smooth transition from Au to Cu there is a need to carryout in depth research and analysis since material changes require requalification. Since there is a dearth of study on the reliability of Cu wirebond packages there is an urgent call for research to address the needs of ever growing semiconductor industry.

Thermo-Mechanical stresses are introduced in a package during fabrication processes or field use due to constant rise and fall in temperature. The mismatch in the Coefficient of Thermal Expansion (CTE) between various components results in significant mechanical stresses in the package. The overmold and wirebond have a considerable difference in there CTE's. Finite Element model was developed to simulate reliability tests for 3D wirebond package. Reliability test, Accelerated Thermal Cycling (ATC) and Thermal ageing tests were simulated on a 3D wire bonded package to capture the Mechanical response of the package. The thermo-mechanical response of package during Accelerated Thermal Cycling test and Thermal ageing test was compared. Comparative analysis of thermo-mechanical response of the packages was carried out for different overmold compounds. Creep behavior of materials is used to capture their response during various temperatures and with time. Further the mechanical response of gold wirebond package is

compared with that of copper wirebond package. The results were further utilized to carry out a parametric analysis to study the effect of wirebond diameter and number of wirebond on mechanical behavior the package. The simulation results show that Cu wirebond package has superior thermo-mechanical response compared to Au wirebond package.

CHAPTER 3

Finite Element Analysis

3.1 Introduction To Finite Element Analysis

Finite Element Analysis is an approach based on numerical methods for solving multi-physics problems. The major areas of interest include structural analysis, fluid flow, heat and mass transport, electromagnetic Interference etc. This technique is being used in various fields of engineering discipline ranging from defense and aerospace applications, manufacturing and fabrication, automotive, microfluidics, Nano electronics to medical applications, earthquake impact prediction, and nuclear breakdown impact prediction etc. Other than this it is considered as the most sophisticated tool for solving engineering problems.

In this method the geometry under analysis is divided into finite number of elements. The elements are divided into number of nodes. The unknown are the displacements of these nodes. To describe the unknown displacements at each point a polynomial interpolation function is used. The entire force applied to the structure is replaced by an equivalent system of forces applied to the nodes. The result of the entire displacement of the structure is obtained by assembling the governing equation. These complex equations are solved to find the approximate solution. Usually due to the complexity of the equations, the solutions are not easily obtainable and hence advanced numerical methods are applied to find acceptable solutions.

Depending upon the type of problem, the solution would be determining the nodal displacement, temperature at nodes or fluid pressure etc. These problems can be very complicated and it can take years or decades, even centuries to solve them using the paper pencil method of solving mathematical equation. Hence the computational power of a computer is used to solve these complex problems.

The equation below is used to find the Nodal Load vector,

{F} = [K] {u} ,where

{F} = Nodal Load Vector

[K] = Global Stiffness Matrix

{u} = Nodal Displacements

3.2 History Of Finite Element Methods

The modern development of finite element methods began in 1940. It was first used by Hrennnikoff in the field of structural engineering. Courant in his paper in 1943 proposed a method to solve the structural problems. Argyris and Kelsey developed the method of structural analysis using matrices and energy principles. The name Finite Element Methods was coined by Clough in 1960. FEA was applied in various fields of engineering using computational power and mainframe computing since the advancements in computers. In 1971, ANSYS a code written for FEA, was first introduced. These days it is very commonly used in various fields of engineering discipline.

3.3 General Procedure and Process Flow for FEA

Preprocessing:

- Model the geometry of the problem
- Define contacts between various parts of model
- Define the type of elements used for analysis
- Assign the material properties for the elements
- Mesh the model with desired element size
- Define the type of analysis viz. structural, thermal, electromagnetics etc.
- Define boundary conditions i.e. loads, supports, thermal conditions etc.

Solution:

- The computer solves the equations that define the loads, boundary conditions and stiffness
- The unknown variables are calculated
- The computed values are then used by reverse substitution to calculate change of values, nodal displacement, heat flow etc.

Post processing:

- The postprocessor is used to plot the results
- The graphical user interface is very useful in advanced post processing

3.4 Stiffness Matrix

In finite element method the stiffness matrix represents the system of linear equations that are solved to obtain the solution of partial differential equations. In case of a structural finite element, the stiffness matrix contains the geometric and material behavior data. This data gives us the information of the how the element resists the deformation when subjected to loading. The deformation can be of different forms like torsional, shear, bending axial. In case of heat and mass or fluid flow transfer, the matrix represents the resistance to temperature change and fluid pressure respectively.

3.5 Thermal Analysis

Thermal analysis is used to calculate the heat transfer, thermal gradient, thermal flux and thermal profiling. The thermal analysis finds its application in various fields.

- Heat flow in pipes
- Heat generation in IC's
- Manufacturing processes
- Heat generation in engines
- Turbo machinery
- Under the hood applications

The three modes of heat transfer, conduction convection and radiation, are analyzed using finite element analysis. Thermal analysis is performed as static or transient analysis. In static analysis the thermal loading is static i.e. it does not change with time. While in transient analysis the thermal load changes with respect to time.

3.6 Structural Analysis

Structural analysis is used in calculating the elastic/plastic deformation, maximum principal stress, maximum principal strain etc. This helps in quick and efficient design of mechanical components, machines, electronic components etc. The modern software technology enables calculating effect on the structure due to complex loading situations. The following are the areas in which structural analysis play a major role,

- Static Analysis – Under static loading conditions, determining the displacements and stresses.
- Modal Analysis – For determining the mode shapes and natural frequencies of a structure.
- Harmonic Analysis – Under time varying loads, determining the harmonic response of the structure
- Transient Dynamic Analysis – Under random time varying loads, determining the response of the structure
- Spectrum Analysis – Due to a response spectrum or a random vibration input, calculating the stresses and strain of the structure
- Buckling Analysis – For calculating the buckling loads and determining the buckling load shape.
- Advance Structural Analysis – This examines the dynamic response, stability and nonlinear behavior of the structure.

Linear Static Analysis

In most of the analysis when assumptions like small deformation, perfectly elastic material and loads are assumed to be static, the analysis can be treated as a specific linear problem

CHAPTER 4

Finite Element Modelling And Analysis

4.1 Modeling Of 3D Wirebond Package

In any electronic package, the different electronic components are made of different materials and hence have different material properties. These components during manufacturing or during field use are subjected to temperature loads ranging from higher temperatures like 150˚C. Due to the difference between coefficients of thermal expansion of each component, thermal stresses are induced in the components. These thermal stresses can be so huge that they can lead to plastic deformation of the electronic components. Crack is initiated in some case while in others there is warping and curling of components. This leads to failure of electronic devices. Such a damage of electronic components can result in loss of human life. For example there have been many instances of life loss due to failure of electronic components of control systems of an airplane. To avoid such situations, the electronic packages are tried and tested. Various reliability tests are performed on the electronic package to test it under extreme conditions.

In this study the reliability test, Accelerated thermal cycling is simulated. Finite element method is used to study the effect of CTE mismatch on the thermo mechanical behavior of the 3D wirebond electronic package when subjected to thermal cyclic loading. The FEA analysis is carried out in commercially available FEA code ANSYS Mechanical 14.5. The 3D wirebond package is shown in figure below. The package consists of various layers. The substrate, die attach, bottom chip, Cu-Sn pillars, top chip, overmold, wirebonds. The 3D wirebond package with mm x mm size substrate, mm x mm die attach size, mm x mm bottom chip size, mm diameter size of Cu-Sn pillar, mm x mm size top chip, mm x mm overmold size, and diameter of wirebond mm is subjected to thermal cyclic loading or thermal shock to determine the thermo mechanical behavior.

Assumptions:

- The material properties of all materials were considered independent of temperature except for wirebond and overmold material
- The Anand's viscoplastic constitutive relation was used for solder pillars
- The material for wirebond were considered 100% pure for simplification purposes

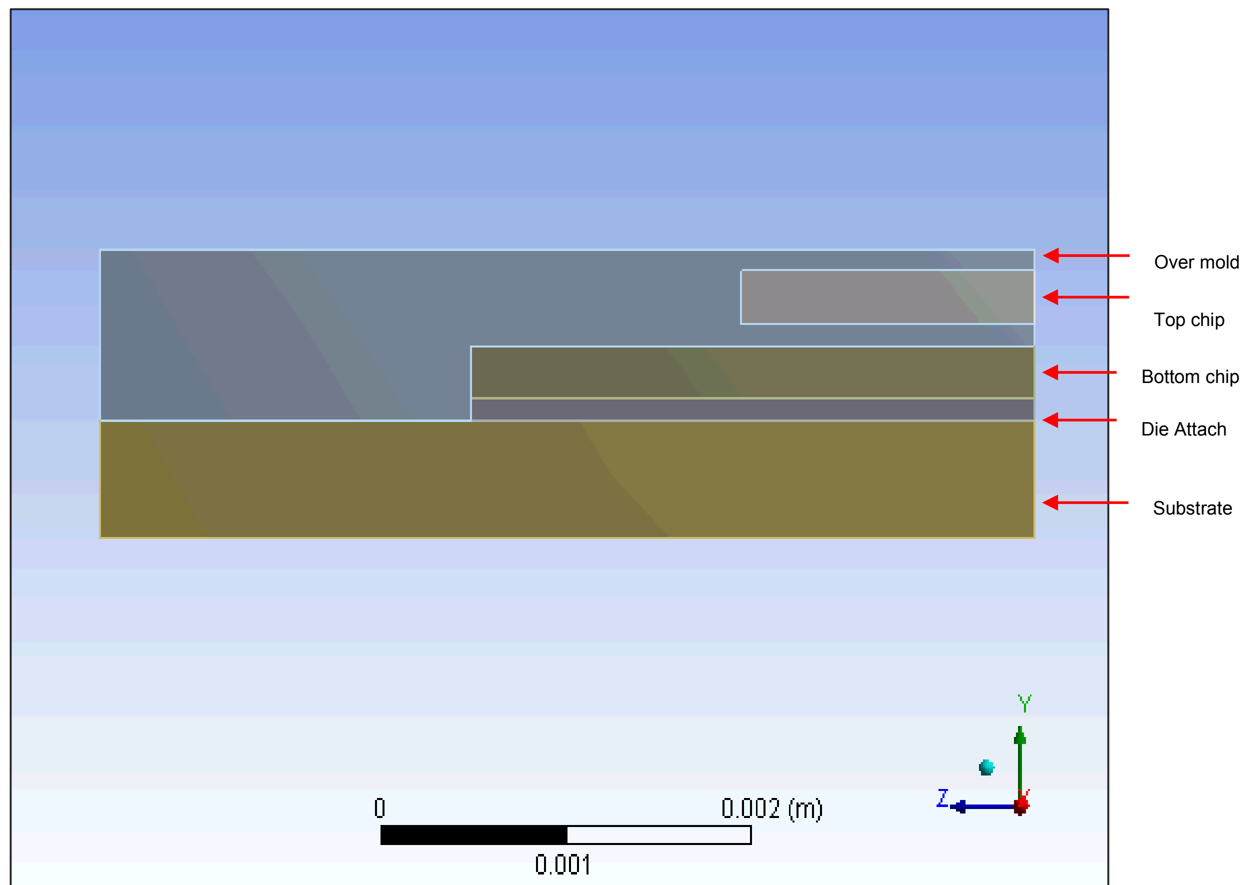


Figure 4.1 Electronic Package components

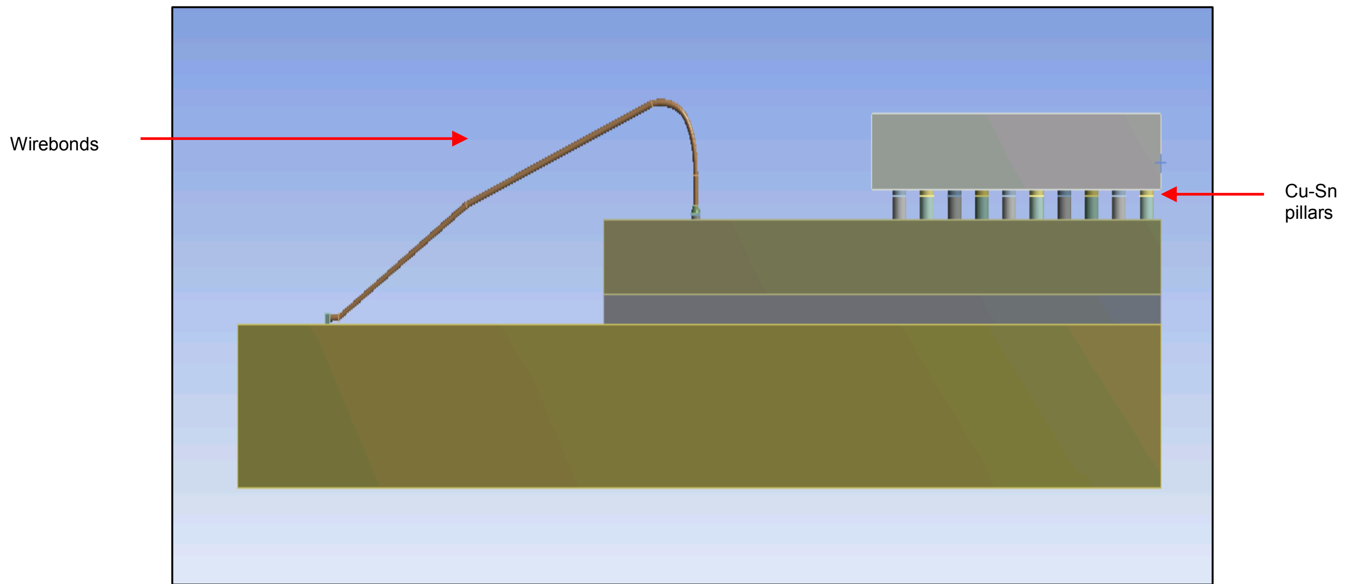


Figure 4.2 3D wirebond package without overmold

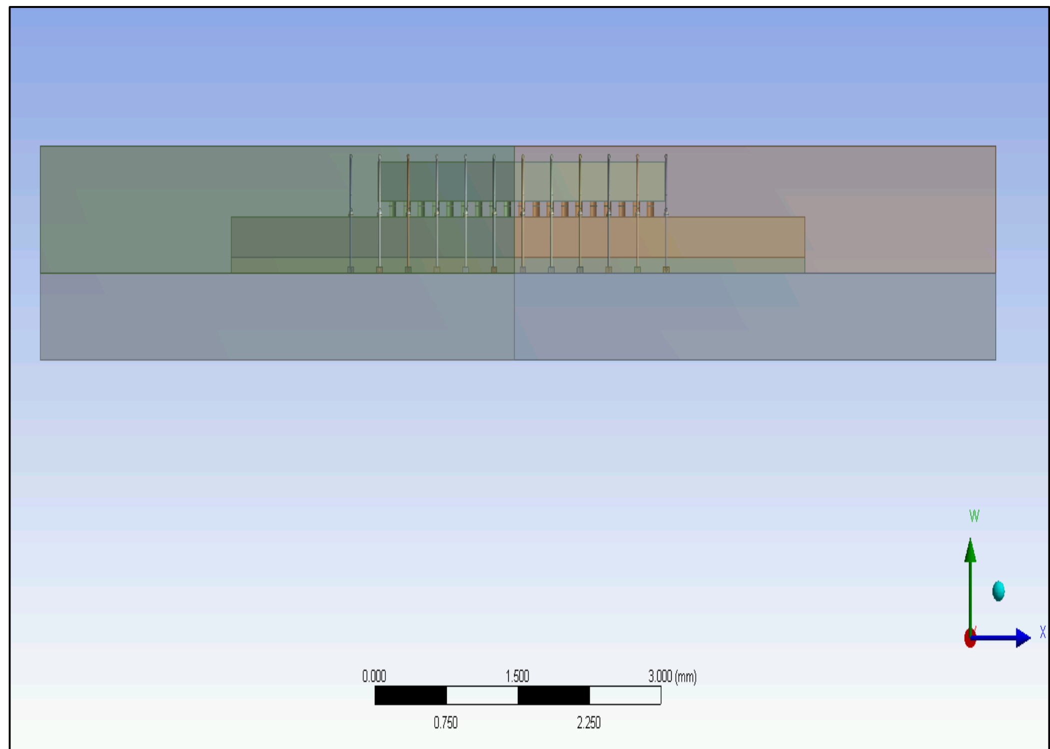


Figure 4.3 Front view of package

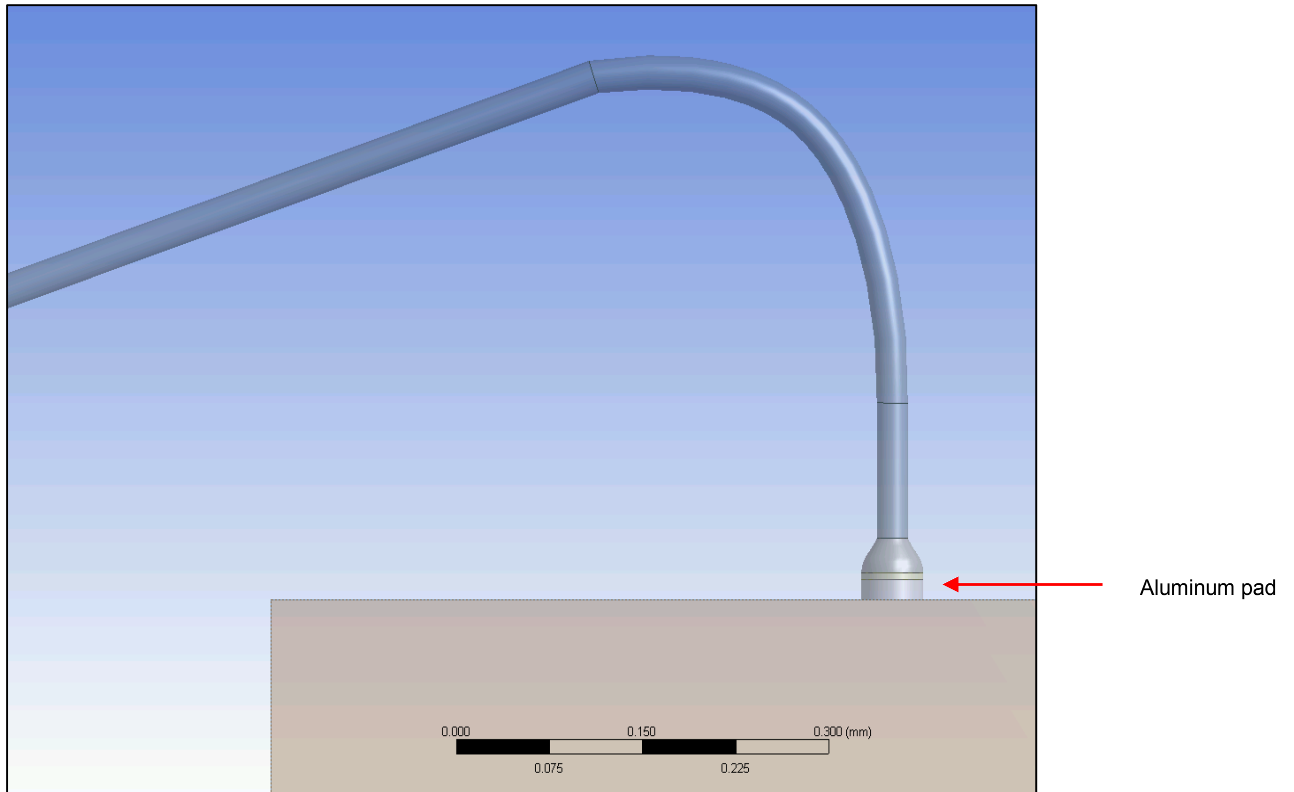


Figure 4.4 Wirebond die side

4.2 Meshing And Boundary Conditions:

The model was discretized with fine meshing option. Mesh sensitivity analysis was carried out to ensure the number of elements in the model is optimum. The geometry is simplified to reduce the mesh count and speed up the solution process. Quarter symmetry is used to again reduce the computational time. Mesh sensitivity analysis is necessary so that the quality of results is not compromised while the computational time is not too large. A base test was carried out to check the variation in results with refined mesh. Each layer in the package is assumed to be perfectly bonded to each other.

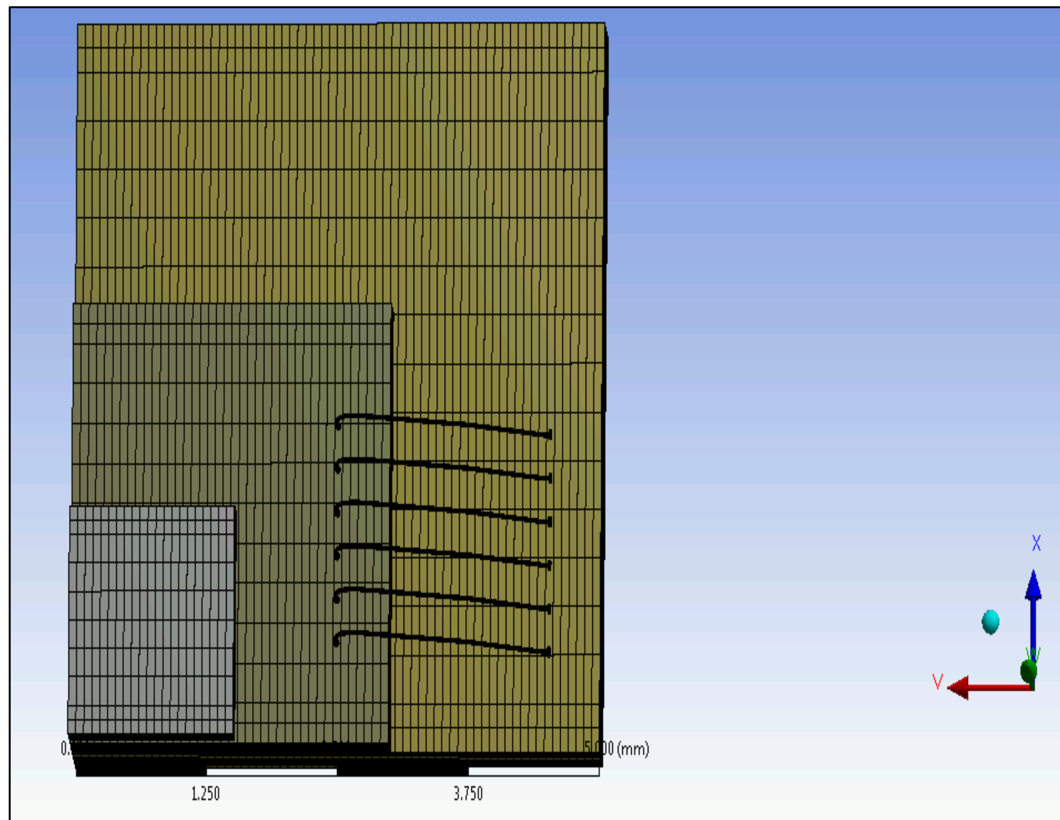


Figure 4.5 Mesh Sensitivity analysis

According to the JEDEC JESD 22-A104C temperature cycling standard for thermal shock, the model was simulated under Thermal shock loading of -55˚C to 125˚C as shown in Figure 4.6

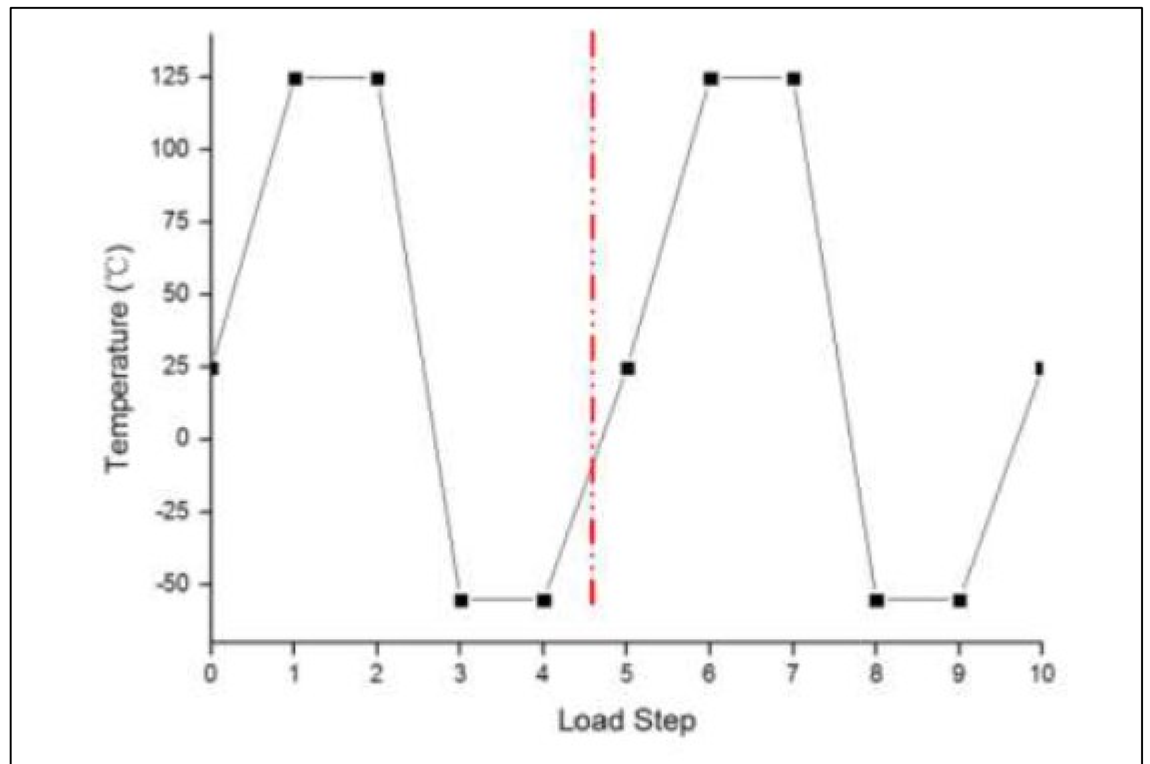


Figure 4.6 Thermal cycling profile [13]

4.3 Nonlinear Modeling

In materials science, creep is the tendency of a solid material to move slowly or deform permanently under the influence of mechanical stresses. It can occur as a result of long-term exposure to high levels of stress that are still below the yield strength of the material. Creep is more severe in materials that are subjected to heat for long periods, and generally increases as they near their melting point. Creep always increases with temperature.

There are various ways to model creep in ANSYS. Among the many models available for creep in ANSYS exponential model was chosen. Shown below is the creep strain by exponential model.

$$\dot{\varepsilon}_{cr} = C_4 e^{\left(\frac{\sigma}{c_5}\right)} e^{\left(\frac{-c_6}{T}\right)}$$

$\dot{\varepsilon}_{cr}$	= creep strain increment
σ	= stress
C_4, C_5, C_6	= Exponential creep constants
T	= temperature (absolute)

Table 4.1 Creep constants for copper [8] [9]

Temperature (˚C)	C4	C5	C6
-40	2.03E-02	12.56168	13912.73
0	1.853E-02	12.56168	13912.73
25	1.25E-02	12.56168	13912.73
75	1.22E-02	12.56168	13912.73
100	8.6E-01	12.56168	13912.73
125	8.3.03E-01	12.56168	13912.73
150	8.63E-01	12.56168	13912.73

4.3.1 Elasticity

In elastic response, if the induced stresses are below the material's yield strength, the material can fully recover its original shape upon unloading. From a standpoint of metals, this behavior is due to the stretching but not breaking of chemical bonds between atoms. Because elasticity is due to this stretching of atomic bonds, it is fully recoverable. Moreover, these elastic strains tend to be small. Elastic behavior of metals is most commonly described by the stress-strain relationship of Hooke's Law.

$$\sigma = E\varepsilon$$

4.3.2 Plasticity

When a ductile material experiences stresses beyond the elastic limit, it will yield, acquiring large permanent deformations. Plasticity refers to the material response beyond yield. Plastic response is important for metal forming operations. Plasticity is also important as an energy –absorbing mechanism structures in service. Materials that fail with little plastic deformation are said to be brittle. Ductile response is safer in many respects than is brittle response.

4.3.2.1 Plasticity Models in ANSYS

Plastic deformation is an inherently nonlinear process. Uniaxial model derived from experiments was used to for the elastic –plastic simulation.

- Bilinear Kinematic Hardening – constant slope after yielding
- Multilinear Kinematic Hardening – series of straight lines after yielding
- Nonlinear Kinematic Hardening
- Similar models exist for isotropic hardening

- Isotropic vs. kinematic determines how yield surface changes after yielding (kinematic means compressive yield increases as tensile yield increases)
- Others are more exotic; these will suffice for our needs

This data is valid in the temperature zone 22 ˚C to 175 ˚C. Figure 4. Shows the engineering stress-strain diagram.

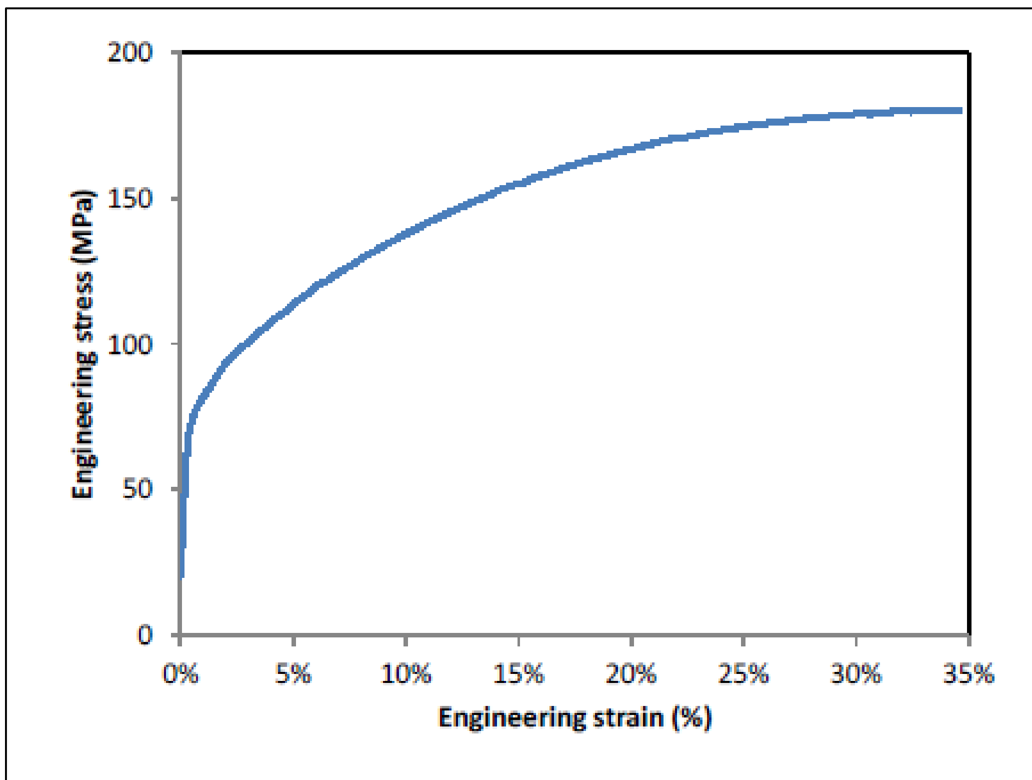


Figure 4.7 Engineering stress-strain diagram [8]

While engineering stress-strain can be used for small-strain analyses, true stress-strain must be used for plasticity, as they are more representative measures of the state of the material.

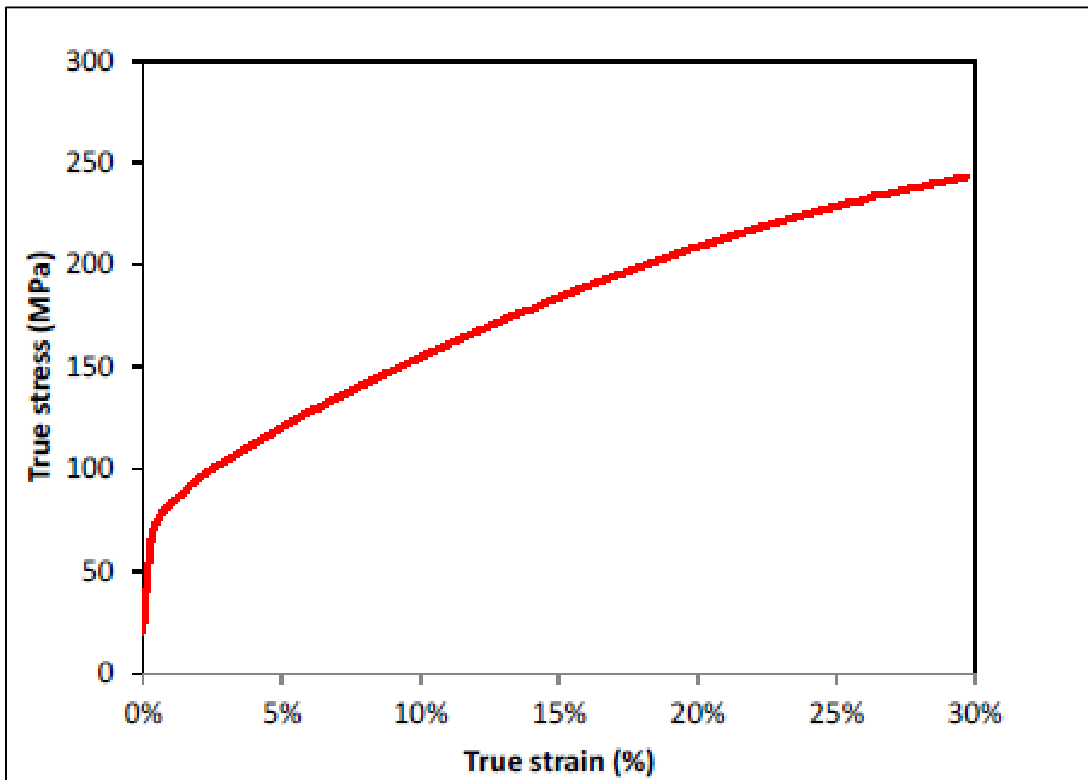


Figure 4.8 True stress-strain diagram [8]

4.3.3 Yield Criteria

The yield criteria is used to relate multiaxial stress state with the uniaxial case. Tensile testing on specimens provide uniaxial data, which can easily be plotted on one-dimensional stress-strain curves, such as those presented earlier in this section. The actual structure usually exhibits multiaxial stress state. The yield criterion provides a scalar invariant measure of the stress state of the material which can be compared with the uniaxial case.

4.4 Package Dimensions And Properties

The material properties and dimensions of various components were obtained from various sources of literature. The package dimensions and material properties are

shown in table 3 and 4 respectively. Temperature dependent properties are only used for wirebond material.

Table 4.2 Package dimensions (mm) [8] [10] [11] [13] [28]

Component	**Dimensions**
Substrate	10 x 10 x 0.55
Die attach	6 x 6 x 0.1
Bottom Chip	6 x 6 x 0.25
Top Chip	3 x 3 x 0.25
Cu Pillar	0.075 diameter
Cu Pillar height	0,075
Sn Pillar	0.075 diameter
Sn Pillar height	0.025
Overmold	10 x 10 x 0.8
Wirebond	0.05 diameter
Aluminum Pad	0.05 diameter
Aluminum Pad height	0.015

Table 4.3 Material properties [8] [9] [10] [11]

Material	E (Pa)	Poisson's ratio	CTE (ppm/˚C)
Substrate	2.4E+10	0.39	17E-06
Die attach	1.1E+10	0.3	3.3E-05
Die	1.5E+11	0.3	3E-06
Copper	1.23E+11	0.34	1.65E-05
Solder	2.4E+9	0.4	6E-05
Overmold	2.8E+10	0.3	1.6E-05
Gold	7.9E+10	0.42	1.42E-05
Aluminum Pad	6.8E+10	0.36	2.4E-05

Table 4.4 Anand’s constants for lead free solder [12]

Variable Sn4Ag0.5Cu	**Variable Sn4Ag0.5Cu**
So (MPa)	20
Q/R (1/K)	10561
A (1/s)	325
A	10
M	0.32
ho (MPa)	8.0E5
S^(MPa)	42.1
N	0.02
A	2.57

4.5 Design Of Experiments

The main objective of this study is to compare the thermal and mechanical response of gold wirebond package and copper wirebond package.

4.5.1 Comparison Of Gold And Copper Material Properties

The table 4.5 shows the properties of gold and copper. The stiffness of copper is higher than stiffness of gold. Also the CTE of copper is also higher than copper while the yield stress is lower. Copper has higher thermal conductivity and lower electrical resistivity compared to gold. Thus copper is far more superior to gold in electric current flow.

Recently the semiconductor industry has been trying to replace gold by copper because of its low cost. The superior thermal, mechanical and electrical properties give it edge over gold. In this study the thermal and mechanical response of gold wirebond package and copper wirebond package was studied. It was assumed that the wires are 100% pure gold and copper. In reality some anti-corrosion compounds are added to the wires to prevent corrosion. For the sake of simplicity in analysis the wires were considered pure copper and gold.

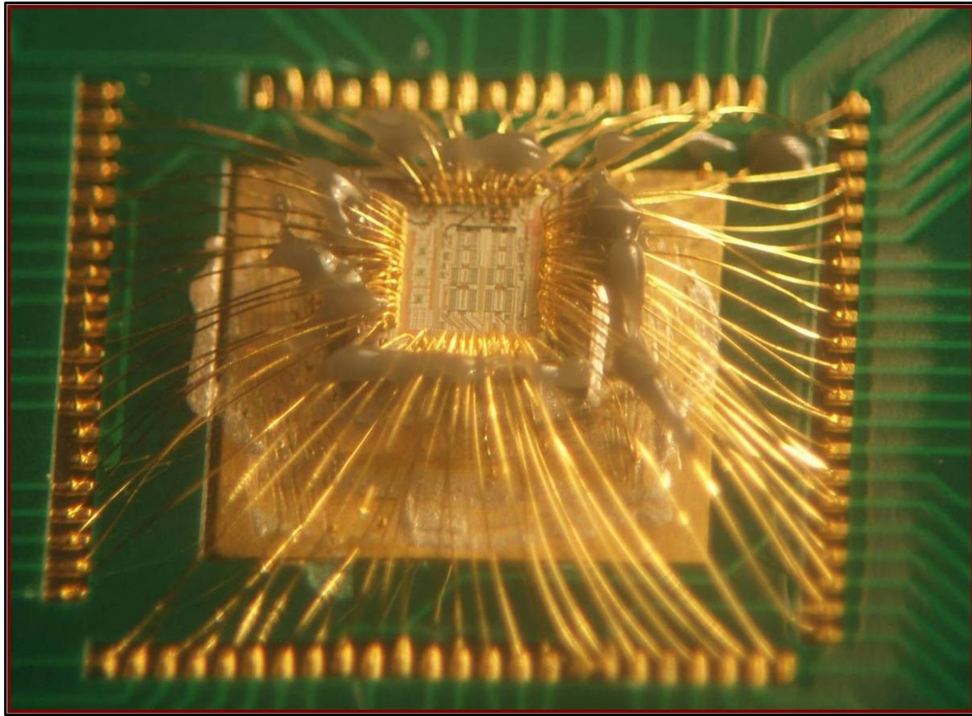


Figure 4.9 Gold wires [41]

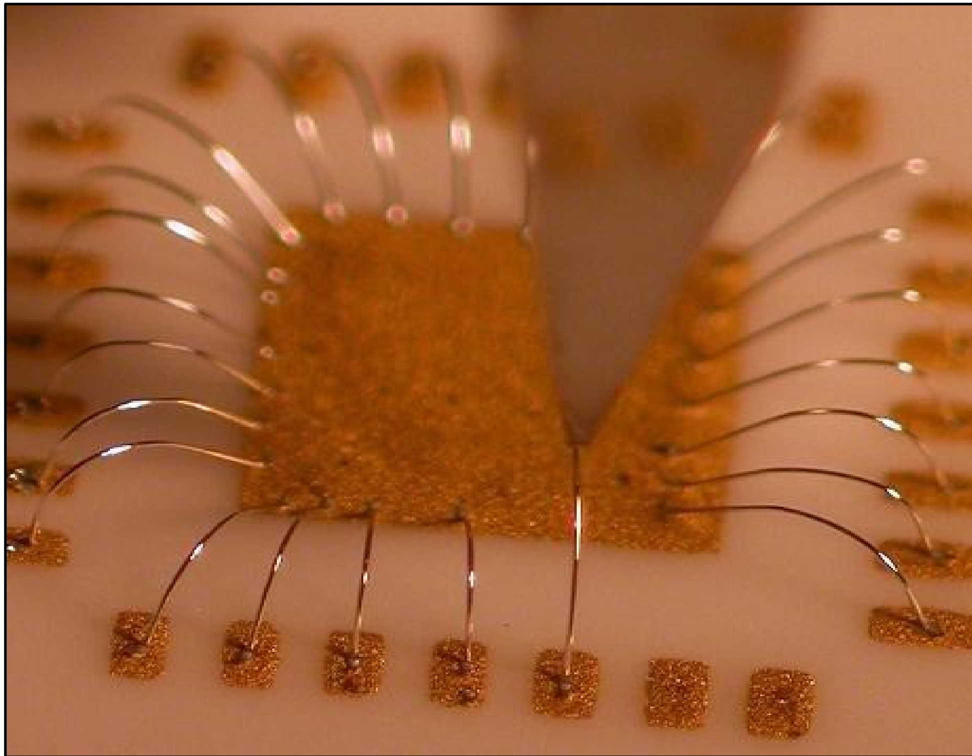


Figure 4.10 Copper wires [41]

Table 4.5 Properties of gold and copper [10] [11]

Property	Gold wire	Copper wire
Young's Modulus	79000 MPa	123000 MPa
Poisson's ratio	0.42	0.3
CTE	14.2 ppm/˚C	16.5 ppm/˚C
Yield stress	200 MPa	160 MPa
Thermal Conductivity	318 W/mK	380W/mK
Electrical Resistivity	2.2 x 10^{-8} Ωm	1.7 x 10^{-8} Ωm

Recently green mold compounds are increasingly used for electronic packages. In this study, the thermo mechanical response of same electronic package with different over mold compound has been captured (Table 4.6). The coefficient of thermal expansion of each over mold compound varies. The effect of CTE mismatch is analyzed for both copper and gold wirebond package. The CTE mismatch thermal stresses in the package. This

stresses accumulate over a period can result in plastic deformation or crack initiation in the package.

Table 4.6 Overmold material under investigation [10] [11] [12]

Case	Overmold type	CTE (ppm/˚C)	E-Modulus (MPa)
1	Overmold 1	7	30000
2	Overmold 2	8	26500
3	Overmold 3	10	24000
4	Overmold 4	12	21000
5	Overmold 5	14	18500
6	Overmold 6	16	15000

Further the effect of wirebond dimensions on the mechanical response of package is investigated. The diameter of wire bond is varied from 25μm to 100μm (Table 4.7). This will help in optimizing the wirebond design. The reliability of the package at varying wire diameters is studied.

Table 4.7 Wire bond diameter

Case	**Diameter (μm)**
1	10
2	25
3	50
4	75

CHAPTER 5

Results And Discussion

5.1 Summary Of FEA Method And Results

Finite Element Method was implemented using ANSYS Mechanical 14.5. JEDEC JESD 22-A104C temperature cycling standard for thermal shock test was simulated on a 3D wirebond package. The objective was to compare the thermo mechanical response of the packages under thermal cycling load. Electronic components and packages are put through this reliability test. This test was carried out on Gold and Copper wirebond package. A parametric study of the packages using various overmold compounds, each having different coefficient of thermal expansion and Young's Modulus was studied.

The effect of CTE mismatch is clearly evident from the results. CTE mismatch between components gives rise to stresses in the package. If the stresses are above the elastic limit it results in plastic deformation. In case of copper, the yield strength is 160 MPa. The yield strength is less than that of gold by 40 MPa. Furthermore the CTE mismatch between low CTE overmold compound and copper is very high. The glass transition temperature of low CTE overmold compound is 130˚C. The CTE of the overmold after it reaches its glass transition temperature Tg is 30 ppm/˚C.

The stiffness of copper wire is higher than gold wire by 55%, the CTE is 16% higher and its yield stress is 20% lower. Plastic deformation found in low CTE overmold copper wirebond package indicates that the stresses induced by thermal mismatch is so high that the stresses induced cross the yield stress of copper which is 160 MPa.

A parametric study off wire dimensions was carried out. The diameter of wire was varied from 10 μm to 75 μm. The critical part of wire is determined. As can be seen in the figure, the wire dimension effects the mechanical response of the package. The shear stress induced in the wirebonds were lower in 10 μm wire compared to 75 μm wire. However the plastic deformation in 10 μm wire was % while that in 75 μm wire was y%.

5.2 Feasibility Of Copper And Gold Wirebonds

Table 5.1 shows the comparison of mechanical response of copper and gold wirebond package with conventional mold material. It is evident that the maximum equivalent stress induced in copper wirebond package is higher than that induced in gold wirebond package.

Table 5.1 Stress and strain distribution in Cu and Au wirebond packages

	Equivalent von-mises stress (MPa)	**Equivalent strain (mm/mm)**
Copper	158.14	0.020811
Gold	142.28	0.02023

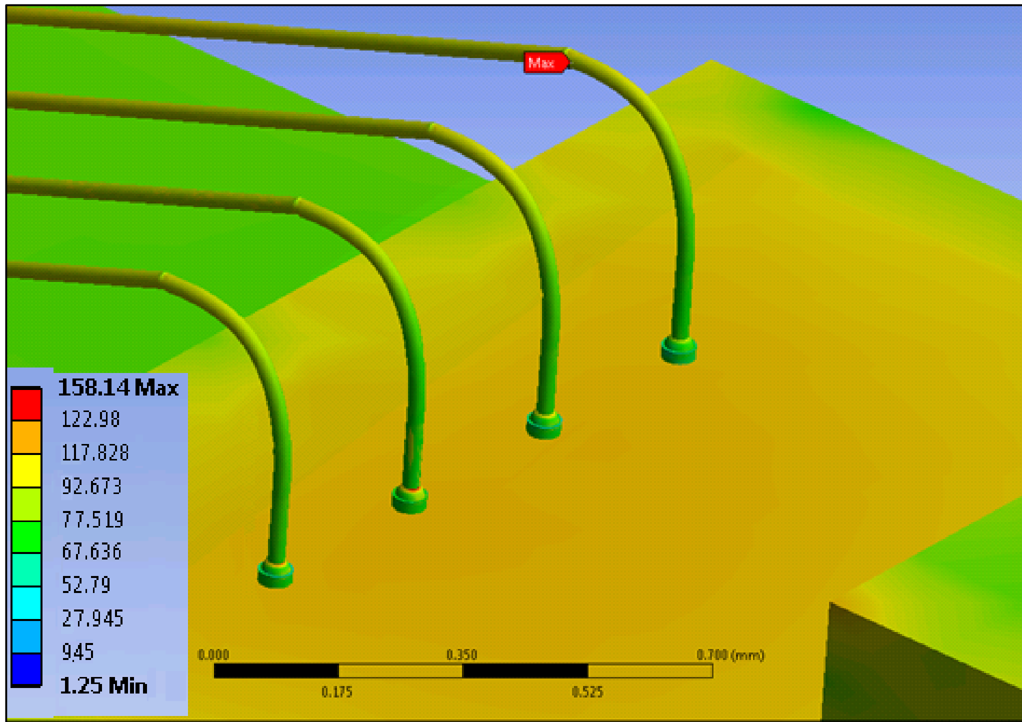


Figure 5.1 Von-mises stress in Copper wire

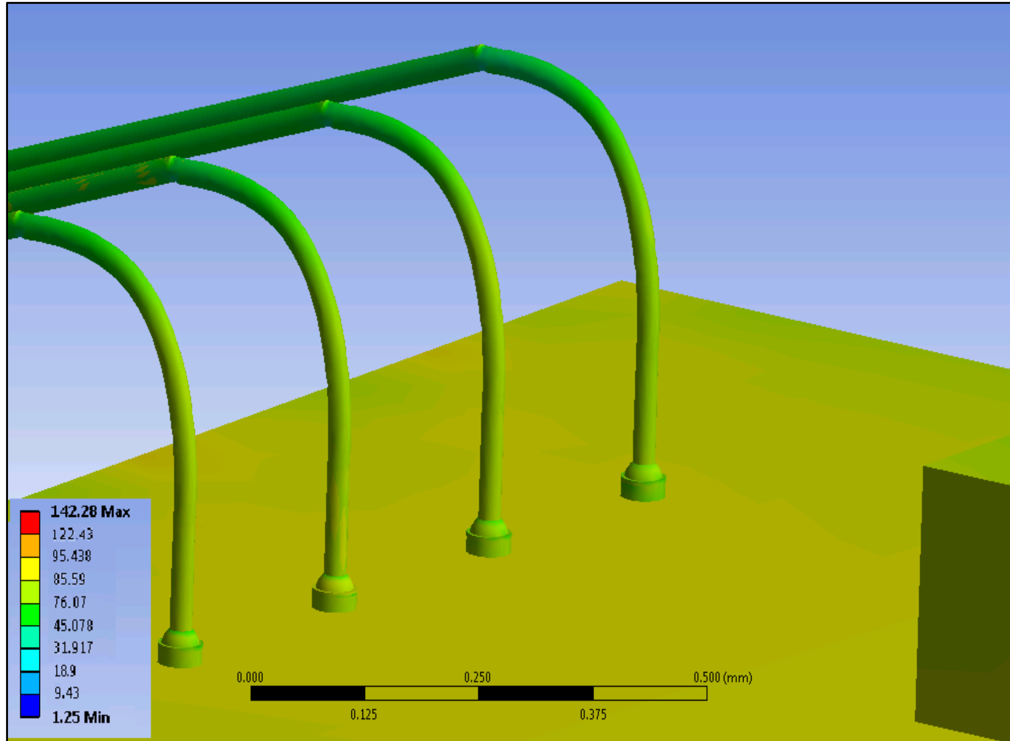


Figure 5.2 Von-mises stress in Gold wire

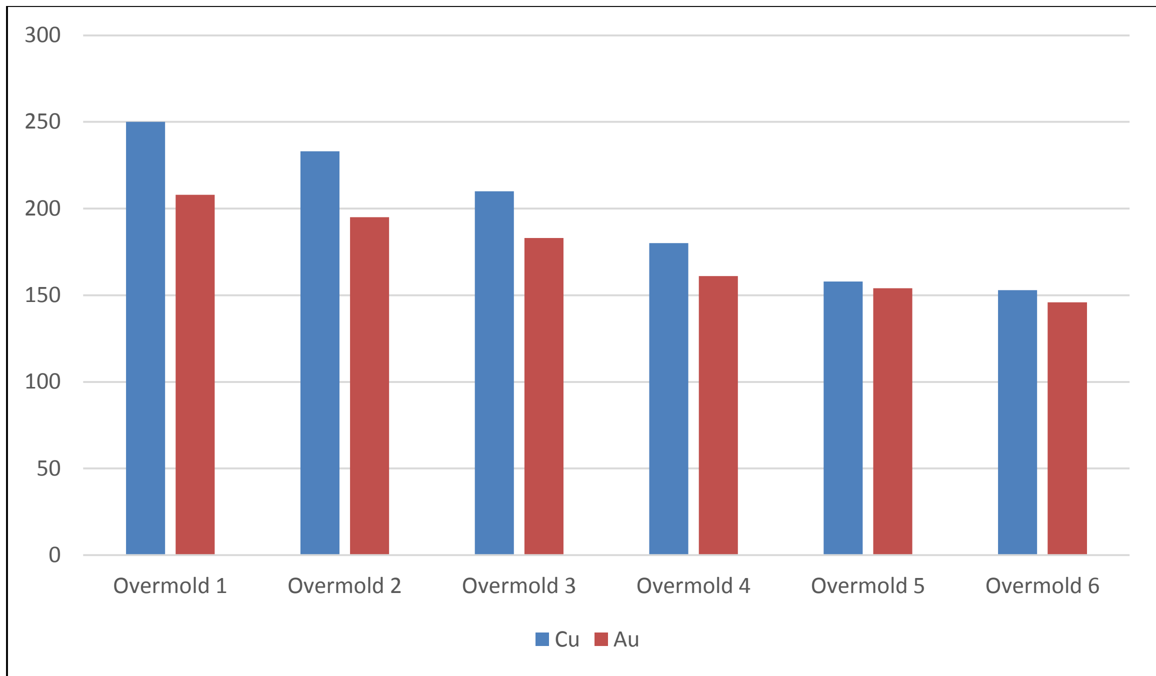
5.3 Parametric Study Of Overmold Compounds

The recent trend in electronics packaging is to use green mold compounds. The green mold compounds have low CTE. Green mold compounds. The introduction of these low CTE compounds is a result of the need for low moisture sensitivity and to reduce the CTE mismatch between die and mold compound.

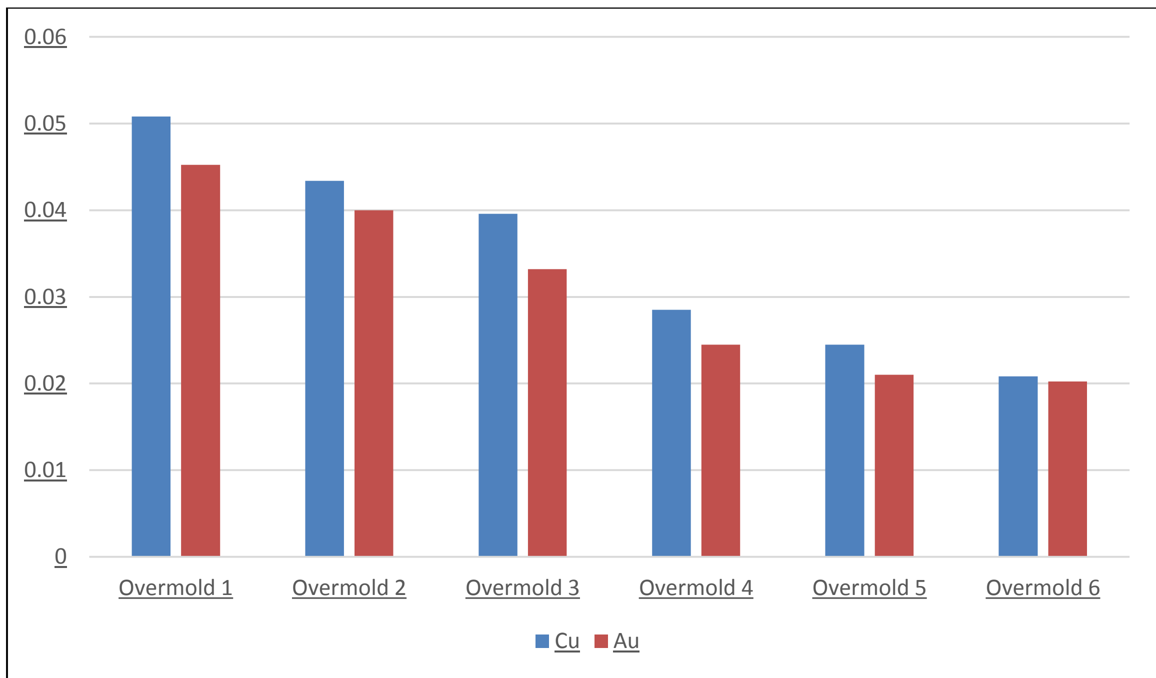
In this study a parametric study of package with different mold compounds was conducted. The mechanical response of packages was compared. The modulus of elasticity increases as CTE decreases. So to understand the effect of overmold properties on the mechanical response of package, parametric analysis using six different overmold compounds was carried out.

Parametric study of overmold compounds on gold wirebond package showed that there is no significant stress generation in the package. No plastic deformation was noticed. The maximum stress in the package was well below the yield stress of gold.

Similarly parametric study of overmold compounds on copper wirebond package showed that the stresses generated in the package are within limits for high CTE mold compounds. However the stress generated in low CTE overmold packages is very high and surpasses the yield stress of copper. Plastic deformation was observed and it can be attributed to the CTE mismatch between copper and mold.



Equivalent stress in copper and gold wirebond package for various overmold material



Equivalent strain in copper and gold wirebond package for various overmold material

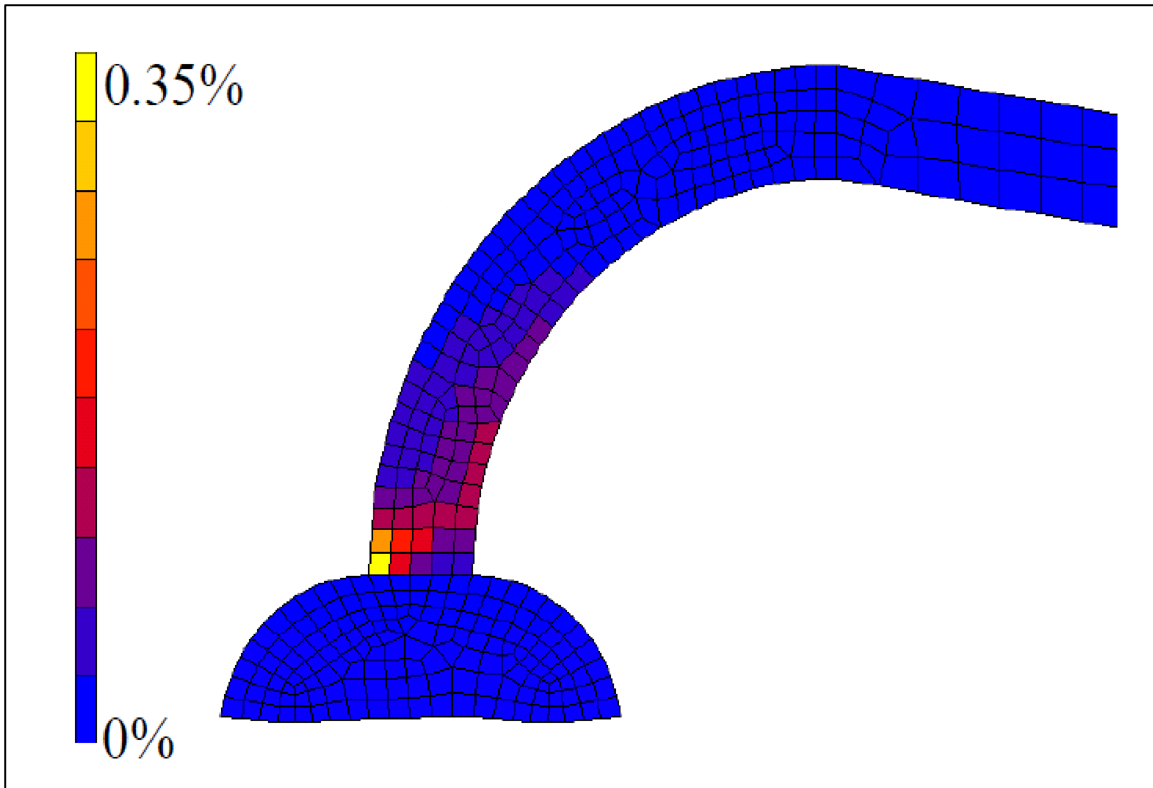
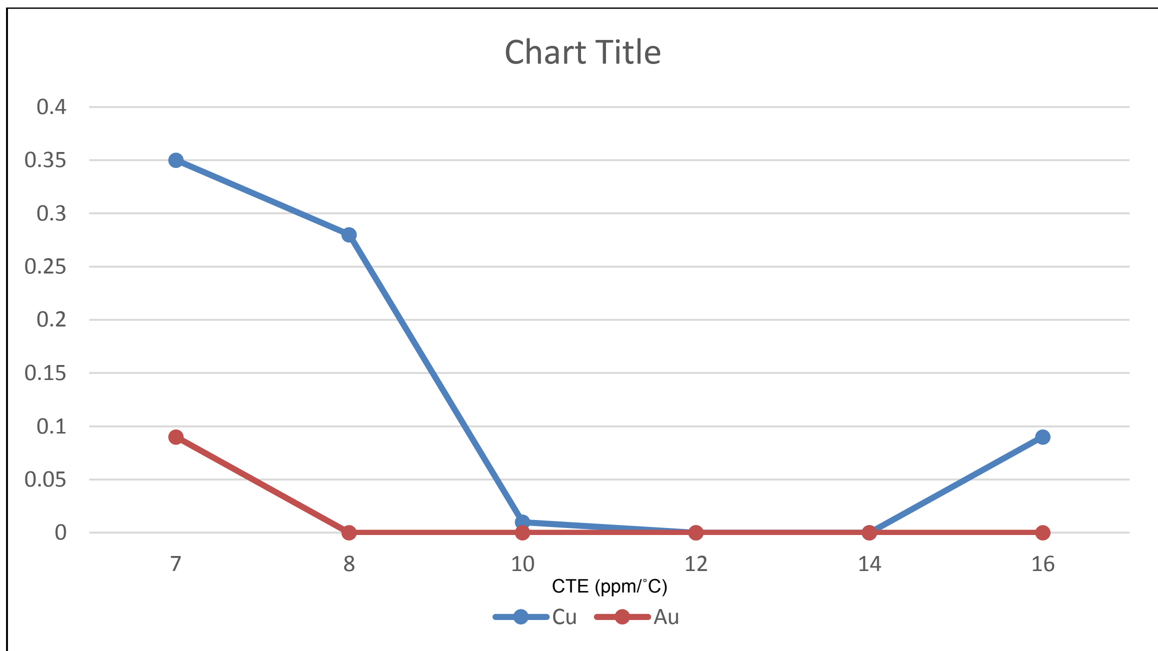


Figure 5.3 Plastic deformation in low CTE overmold copper wirebond package



Plastic strain induced for overmold compounds with different CTE

5.4 Parametric Study Of Effect Of Wire Diameter

The effect of wirebond diameter on the mechanical response of the package was investigated. The wire dimension plays a significant role in package design than one would expect. The wire is responsible for dissipating the heat generated in the package. Copper having higher thermal conductivity, the flow of heat is at a faster pace in copper wire than in gold wire thus cooling the package faster. Moreover copper has low electrical resistivity and hence has superior electrical performance. The parametric study of wire dimensions showed that the wire of diameter below 25 μm deforms. The magnitude of stresses induced in the wire decreases as the wire diameter increases. This value can be optimized my further taking into consideration the electrical performance parameters.

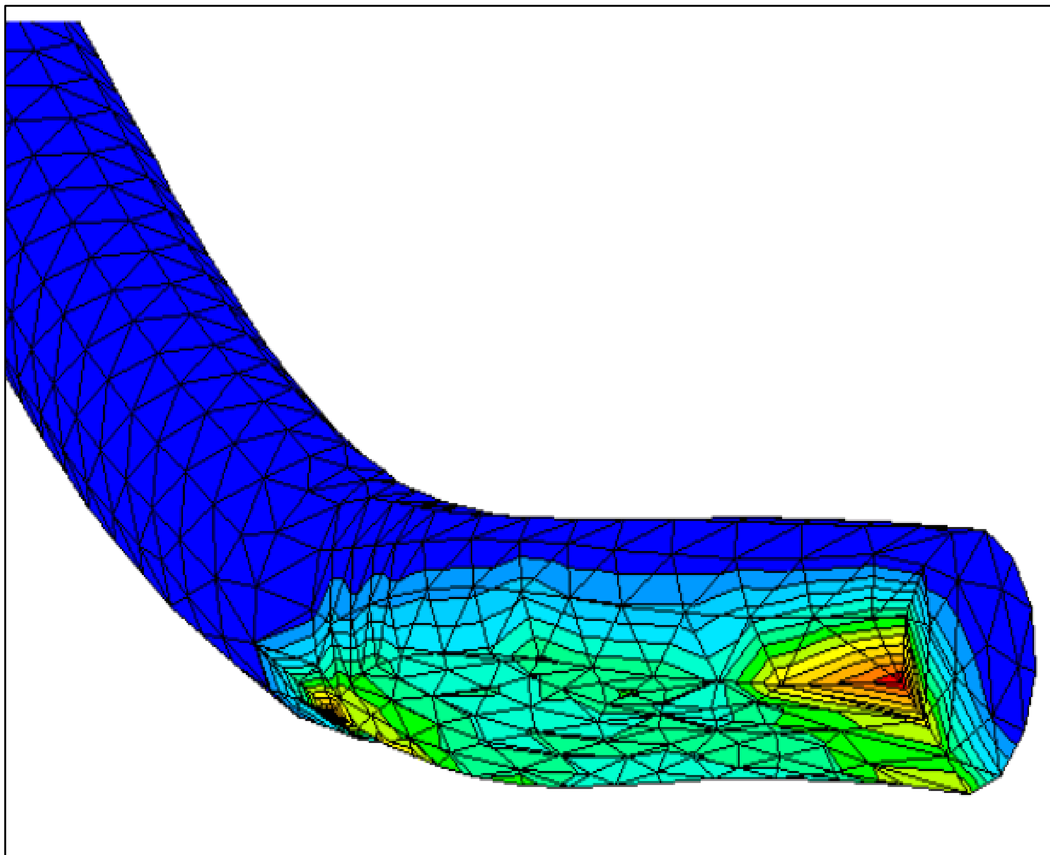


Figure 5.4 Wire of diameter less than 25 μm deforms

Chapter 6

6.1 Conclusion

Finite element model of 3D wirebond package was developed. A FEA process and method was established to accurately predict the mechanical behavior of the package. The reliability test, accelerated thermal cycling or thermal shock test was carried out. Thermo mechanical analysis was carried out on both copper wirebond package and gold wirebond package. As expected the maximum von-mises stress in copper wirebond package were higher than those in gold wirebond package. This is because of the CTE mismatch between overmold material and copper is higher compared to that between overmold material and gold. But one of the interesting observation is that copper wirebond package did not fail and hence is as reliable as gold wirebond package.

Parametric study of overmold compounds was carried out. No plastic deformation was observed in gold wirebond package for all cases. This is attributed to the high yield stress of gold. Plastic deformation was found in copper wirebond package using low CTE overmold. The two main reasons for plastic deformation are high CTE mismatch and comparatively low yield stress of copper. In conventional packages the CTE mismatch is not significant. While with low CTE overmold package the copper wire is stresses enough to cause plastic deformation. If the stresses are repeated then it can lead to cracking of wire. It is not advisable to use low CTE overmold with copper until this issue is resolved.

Parametric analysis of wire dimension was conducted. Wire with diameter less than 25 μm shows significant plastic deformation under thermal cycling load. As the diameter of wire increases the stress induced increases but does not lead to plastic deformation.

6.2 Future Work

In the future it is proposed to study the crack initiation in the low CTE overmold copper wire packages. J-integral will be used to calculate the strain energy release rate. It would be interesting to understand how the crack propagates and the number of cycles

required before it fails. Electronic packages are used in hand held devices. Reliability drop test will be conducted to study the mechanical response due to impact under gravity. Number of cycles before failure will help understand how reliable the package is.

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