EFFECT OF PCB THICKNESS ON SOLDER JOINT RELIABILITY OF QFN PACKAGE UNDER POWER AND THERMAL CYCLING

by

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Abstract

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Failure analysis and its effects are major reliability concerns in electronic packaging. More accurate fatigue life prediction can be obtained after the consideration of all affecting loads on the electronic devices. When an electronic device is turned off and then turned on multiple times, it creates a loading condition called power cycling. The die is the only heat source causing non-uniform temperature distribution. The solder joint reliability assessment of Quad Flat no-lead Package (QFN) is done through computational method i.e. Finite element analysis (FEA) under two different loads. In this paper, the power cycling and thermal cycling act as a combined load. The reliability assessment is done to check stress distribution on PCB board and solder joint. The life to failure is determined for QFN package assembly. The mismatch in coefficient of thermal expansion (CTE) between components used in QFN and the non-uniform temperature distribution makes the package deform. Modeling of life prediction is usually conducted for Accelerated Thermal Cycling (ATC) condition, which assumes uniform temperature throughout the assembly. In reality, an assembly is also subjected to Power Cycling (PC) i.e. non-uniform temperature with chip as the only source of heat generation. This work shows performance of QFN package

assembly under thermal and power cycle in combine and also the stress distribution and plastic work for the package.

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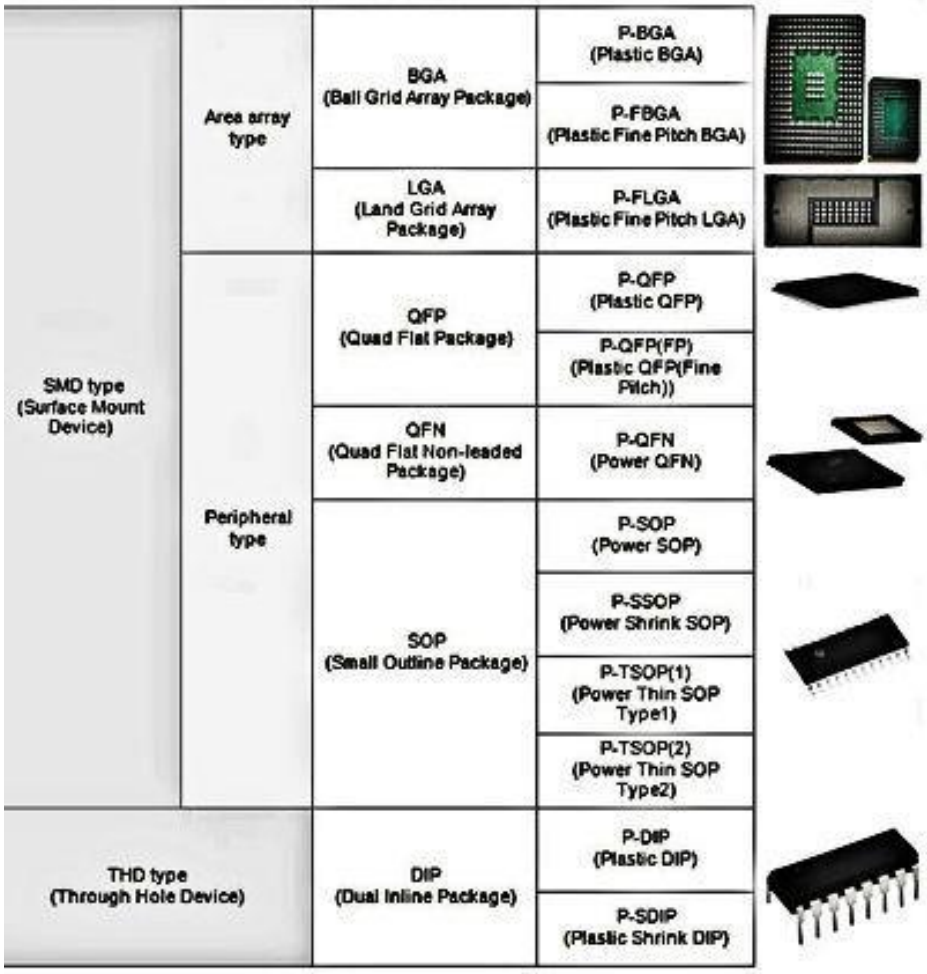
Chapter 1

1.1 INTRODUCTION

Electronic packaging is a major discipline within the field of electronic engineering, and includes a wide variety of technologies. It refers to enclosures and protective features built into the product itself, and not to shipping containers. It applies both to end products and to components. Packaging of an electronic system must consider protection from mechanical damage, cooling, radio frequency noise emission, protection from electrostatic discharge, maintenance, operator convenience, and cost. Prototypes and industrial equipment made in small quantities may use standardized commercially available enclosures such as card cages or prefabricated boxes. The same electronic system may be packaged as a portable device or adapted for fixed mounting in an instrument rack or permanent installation. Packaging for aerospace, marine, or military systems imposes different types of design criteria.

The functions of an IC package are to protect, power, and cool the microelectronic device described above and to provide electrical and mechanical connection between the part and the outside world. Each chip has its unique packaging process. For example, a generic flow for Dual-in-Line Packages (DIP). DIPs were the first complex package solution developed shortly after the invention of ICs in the 1960s. Many package solutions have been developed since, but because of its low cost and high reliability, it continues to be used even four decades after its first introduction. The package is generally fabricated independent of the ICs. [1]



Broad classification of Semiconductor Packages

Figure 1-1: Classification of Semiconductor Packages

1.2 Quad Flat No-Lead (QFN) Packages

The QFN (Quad Flat No-lead) package is probably the most popular semiconductor package today because of four reasons: low cost, small form factor and good electrical and thermal performance. Like any other semiconductor package, a QFN package functionality is to connect (both physically and electrically) silicon dies (the ASIC) to a printed circuit board (PCB) using surface-mount technology. QFN is a lead frame-based package which is also called CSP (Chip Scale Package) with the ability to view and contact leads after assembly.

QFN packages typically use a copper lead frame for the die assembly and PCB interconnection. The QFN can have a single or a multiple rows of pins. The single row structure is formed either by a punch singulation or a saw singulation process, both of these methods divides a large array of packages (for example an 18” x 24” sheet) into individual packages. The multi-row QFN uses an etching process to realise the wanted number of rows and pins; these are then also singulated, typically by saw. QFNs have an exposed thermal pad on the bottom of the package that can be soldered directly to the system PCB for optimal thermal transfer of heat from the die.

Figure 1-2 shows the outline of the QFN package.

Figure 1-1 QFN outline

The QFN package exposed pad (or paddle) offers a low thermal resistance path for heat transfer to the PCB and therefore it's recommended to solder the exposed pad to a large conductive surface such as GND plane. This path carries approximately 70% of the heat away from the Package. With the presence of metal plane the heat flow via the exposed pad can increase to 90%.

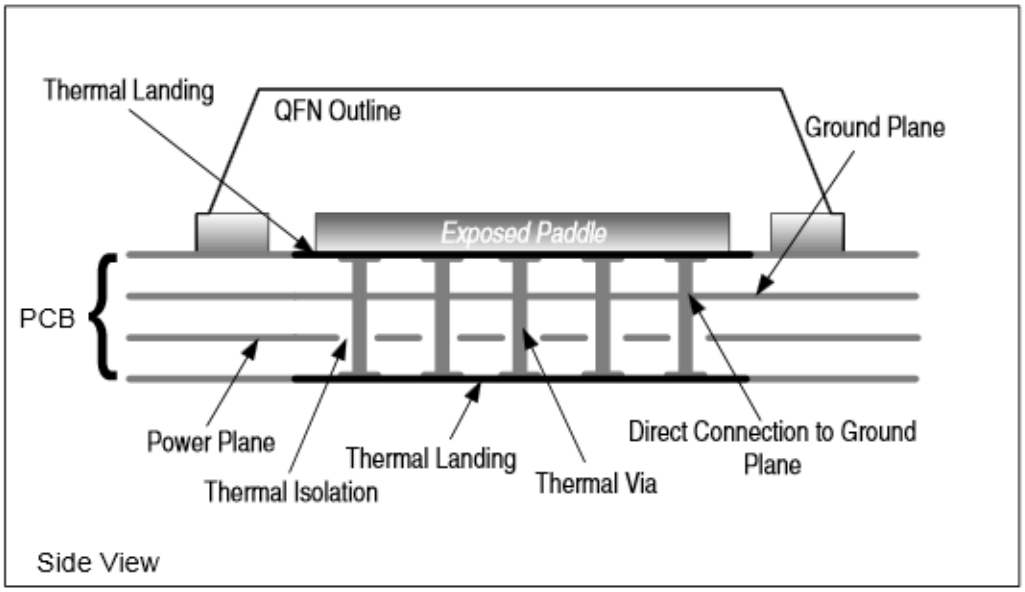


Figure 1-2: Internal Connection to the Exposed Paddle

QFN packages allows for good electrical and physical connection in between the PCB and the IC, thanks to the metal vias in the thermal pads that facilitate the heat transfer. There are different types of QFN. Two of the most common are: air-cavity QFNs (made of three parts such as: copper leadframe, ceramic or plastic-molded body, and either a ceramic or plastic lid) and the plastic molded QFN (characterised by being fully molded with no air in the package).

Thermal pad, or exposed pad, is an efficient method of drawing heat from the die to the PCB. QFN is a thermal efficient package and the exposed pad is a very cost-effective solution. QFNs can handle up to 2W-3W without forced air cooling. [2]

This work requires the use of QFN packages that were obtained from Texas Instruments (TI) for analysis. The properties of these packages are discussed in the later chapters.

1.3 Board Level Reliability (BLR) Industry Standards

Reliability can be defined as the ability of a system or component to perform its required functions under stated conditions for a specified period of time. To quantify reliability, “ability” should be interpreted as a “probability”. From this definition it is clear that all products always fail eventually. Indeed, a probability of zero failure during a certain amount of time is physically impossible, even for integrated circuit (IC) [3].

Board Level Reliability (BLR) is also known as an interconnect reliability testing. Basically, this is a method used to evaluate the quality and reliability of solder connections after mounting an IC package to a printed circuit board (PCB). [5]

To estimate the reliability of the package, environmental stress test are used to simulate the end use environment conditions and to uncover specific materials and process related marginalities that may be experienced during operational life. Few consortiums such as Joint Electronic Device Engineering Council (JEDEC) and

Institute for Printed Circuits (IPC) have adapted, documented and standardized many of the reliability tests [4].

These reliability tests are either focused on package level or board level. Package level or 1st level reliability tests are dedicated to the robustness of the package component materials and design to withstand extreme environmental conditions and does not consider the interconnects when it is mounted on board. Whereas for the board level or 2nd level reliability tests, stresses are examined on the solder joint of the surface mount package when mounted on board [12].

Table 1-1 shows different temperature ranges for various service environments for electronic products [4].

Table 1-1 Thermal environments for electronic products

Use condition	Thermal excursion (°C)
Consumer electronics	0 to 60
Telecommunications	-40 to 85
Commercial aircraft	-55 to 95
Military aircraft	-55 to 125
Space	-40 to 85
Automotive-passenger	-55 to 65
Automotive-under the hood	-55 to 160

1.4 Power Cycling and Thermal Cycling

Power cycling refers to the act of turning a device or piece of electrical or electronic equipment off, or otherwise disconnecting it from its power source, and then turning it back on again.

A power cycling test can be much more realistic than a temperature cycling test because a power cycle results in non-uniform temperature distribution as the die is the only heat source. Fatigue being the dominating failure mechanism of solder interconnects and enhancement of its life is one of the major concerns for package designers and users. Conventionally, fatigue life is obtained empirically through accelerated thermal cycling (ATC) with hundreds of parts. To reduce development time and cost, virtual qualification attempts are made using numerical simulation tools, such as finite element analysis.

Modeling of life prediction is usually conducted for ATC condition, which assumes uniform temperature throughout the assembly. In reality, an assembly is subjected to Power Cycling i.e. non-uniform temperature with chip as the only source of heat generation. This non-uniform temperature and different coefficient of thermal expansion (CTE) of each component makes the package deform differently than the case of uniform temperature [13].

Thermal cycling is one of the reliability test that has been used to evaluate the reliability of solder joint interconnect in microelectronics package. Thermo-mechanical stress is generated due to Coefficient of Thermal Expansion mismatch between board and package during temperature loading. Solder joint fatigue crack failure caused by thermo-mechanical

mechanism is one of the major failures in microelectronics package. The purpose of thermal cycling is to characterize thermo-mechanical failure mechanism on microelectronics package. [4]

1.5 Motivation and Objective

Motivation

QFN package gained popularity among the industry due to its low cost, compact size and excellent thermal electrical performance characteristics. Although QFN package is widely used in handheld devices, some customers require it for heavy industry application demanding thicker PCB. Literature suggests that as the thickness of PCB increases, the reliability and fatigue life of the package decreases since the board becomes stiffer and less flexible resulting in more transfer of stresses on the solder joint.

Modeling of life prediction is usually conducted for Accelerated Thermal Cycling (ATC) condition, which assumes uniform temperature throughout the assembly. In reality, an assembly is subjected to Power Cycling (PC) i.e. non-uniform temperature with chip as the only source of heat generation. This non-uniform temperature and different coefficient of thermal expansion (CTE) of each component makes the package deform differently than the case of uniform temperature [13].

Also, ATC is generally considered to be a conservative test method. This is generally true in the case of ceramic packages. However, it may not be true in the case of

organic packages. Hence, the effect of power cycling on board level reliability is studied in this work.

However, from the available literature we know that, as the thickness of PCB increases, there is a decrease in the reliability and fatigue life of the package. This is because the stiffness of the board increases and flexibility decreases resulting in more transfer of stresses on the solder joint. Cross-section of a typical thick PCB with 16 copper layers, is shown in Figure 1-4.[11]

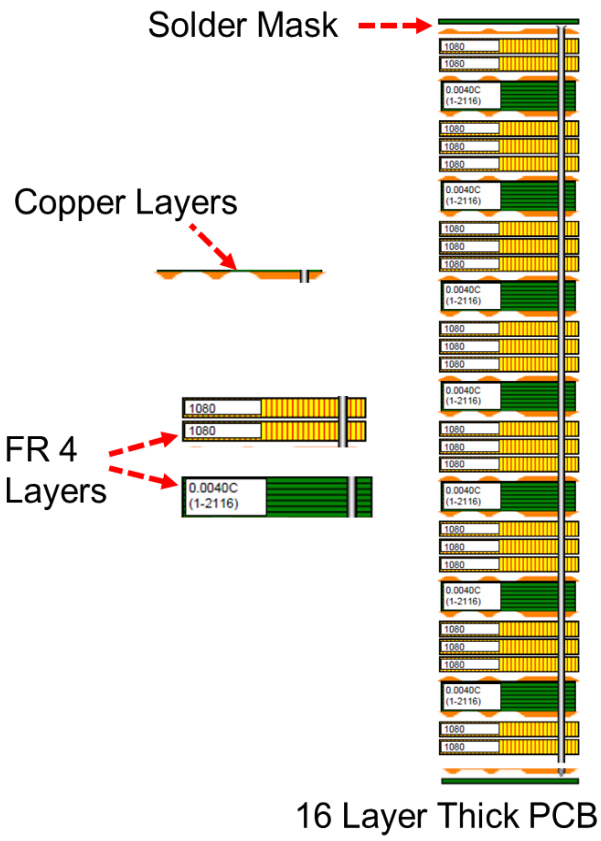


Figure 1-4: Cross-section of 16 layer Copper board

Objective

- Determine material properties of QFN board of thickness 62mil, 93mil and 134mil.
- Comparative study of solder joint reliability under power cycle and thermal cycle loading in combine.
- Obtaining plastic work, equivalent stresses and life to failure of solder join for three different thick QFN.
- Identifying critical solder joint under the combined loading.

CHAPTER 2

LITERATURE REVIEW

With great feasibility and flexibility for growing I/Os, multi-chips and system integration, the emerging fan-out embedded Wafer Level BGA (eWLB) technology is regarded as a much more favorable packaging solution compared with its traditional counterparts, i.e. fan-in WLP or BGA technology. The relentless trend of ever increasing integrated circuit chip functionality and decreasing chip dimensions for miniaturization of products have led to less chip real estate and intense heat dissipation. While eWLB technology has well addressed the routing problems associated with the former, its intrinsic ineffectiveness of reducing the spreading thermal resistance of the shrunk die has limited its application to low power devices. As a result, Quad Flat No-Lead (QFN) is often a packaging technology of choice for those applications as QFN is a lead frame based package which offers thermal and electrical enhancement with its exposed die pad on the bottom of the package surface. The exposed die pad not only provides an efficient heat path to the PCB, but also enables stable grounding with electrical connection through a conductive die attach material. To bridge the gap between the eWLB and QFN concept so that both of their advantages can be retained, STMicroelectronics has recently come up with a QFN-like eWLB package known as embedded wafer level LGA (eWLL) with low profile, high pin count and excellent thermal and electrical performance. This paper initially investigated the solder joint reliability of the eWLL packages under board level Accelerated Thermal Cycling (ATC) test through Finite Element Analysis (FEA). Experiments were then carried out to assess the accuracy of the FEA model. It was found that the predictions made by the FEA simulation correlated very well with the actual test results. The validated FEA model was then

extended to study the effect of a wide range of design variables on the board level reliability of the eWLL packages.[6]

However, most of the work considers power cycling as a pure thermos-mechanical failure problem. Typical work include Darveaux [14] (1995) published thermal and power cycling limits for plastic BGA. Ham et al [15] (2000) compared power cycling simulation to Moire interferometry measurements results, the deformation agreed well with finite element predictions. Syed [16] (2001) gave the predicting methodology within 25% accuracy for solder joint reliability in thermal, power and bend cycles. Myllykoski [17] (2002) studied and compared the thermal cycling and power cycling for BGA assemblies. Most of the above work considers the power cycling as a pure thermal-mechanical failure problem [18]**.**

CHAPTER 3

MATERIAL CHARACTERIZATION

To determine the plastic work and and stresses in the board under power cycling and thermal cycling, it is necessary to input actual material properties for each material. The thick PCBs were characterized for finding following material properties-

- Coefficient of Thermal Expansion (CTE)
- Young's Modulus.

In order to characterize the PCB, we use the following setup:

- Thermo Mechanical Analyzer (TMA)
- Dynamic Mechanical Analyzer (DMA)

While the TMA is used to determine the CTE's in each direction, the DMA is used to determine the Young's Modulus, E.

Now, let us define the two properties.

The change in length or volume of a material for a unit change in temperature is defined as The Coefficient of Thermal Expansion (CTE). The overall coefficient is the linear thermal expansion per degree Fahrenheit or Celsius. It is calculated by the change in length divided by the quantity of the length at room temperature, multiplied by the change in temperature [19].

Generally it is given by-

$$\alpha = \frac{\epsilon}{\Delta T}$$

Where,

α - Coefficient of Thermal Expansion (ppm/°C)

ϵ - Strain (mm/mm)

ΔT - Temperature Difference (°C)

Young's Modulus (E):

Young's Modulus is an elastic property of a material which can be defined as the ratio of stress to strain.

$$E = \frac{\sigma}{\varepsilon}$$

ϵ - Strain (mm/mm)

E - Young's Modulus (N/mm^2)

σ - Stress (N/mm^2)

3.1 Thermo Mechanical Analyzer

Figure 3-1: TMA-SS6000

Thermo mechanical analysis (TMA) easily and rapidly measures sample displacement (growth, shrinkage, movement, etc.) as a function of temperature, time and applied force.

Traditionally, TMA is used to characterize linear expansion, glass transitions, and softening points of materials by applying a constant force to a specimen while varying temperature. For expansion measurements, a probe rests on a sample on a stage with minimal downward pressure. Other constant force experiments include measurement of penetration, bending, tension, shrinkage, swelling, and creep (sample motion measured as a function of time under an applied load).

The concept:

Sample Chamber: The easily accessible chamber is located in the center of the furnace. Both temperature and atmosphere can be controlled. In addition an optional mass flow controller is available for purge gas regulation. The gas tight cell can be evacuated and allows you to measure under a defined atmosphere. Only such a system can provide definitive information concerning the samples sensitivity to oxidation.

Furnace: The TMA Platinum Series comes with a robust and reliable furnace. Its customized design enables rapid heat up and cool down times and an excellent heating rate control over the entire temperature range.[7]

To obtain the CTE, TMA 6600 was used as a tool. 134mil PCB was placed in the holder with a Tension probe (made of quartz) with the test settings being as follows

- Start and end limit temperatures - ~+25°C to ~+125°C
- PCB specimen size - 4 x 4 x 3.45 mm
- Ramp Input - 5°C/min
- Start and End load - 100mN

An Aluminum sample was benchmarked to gain confidence in the test before measuring the CTE of the 62 nil, 93 mil and 134 mil PCB. The CTE was measured in all the 3 directions by changing the orientation of the sample.

3.2 Dynamic Mechanical Analyzer

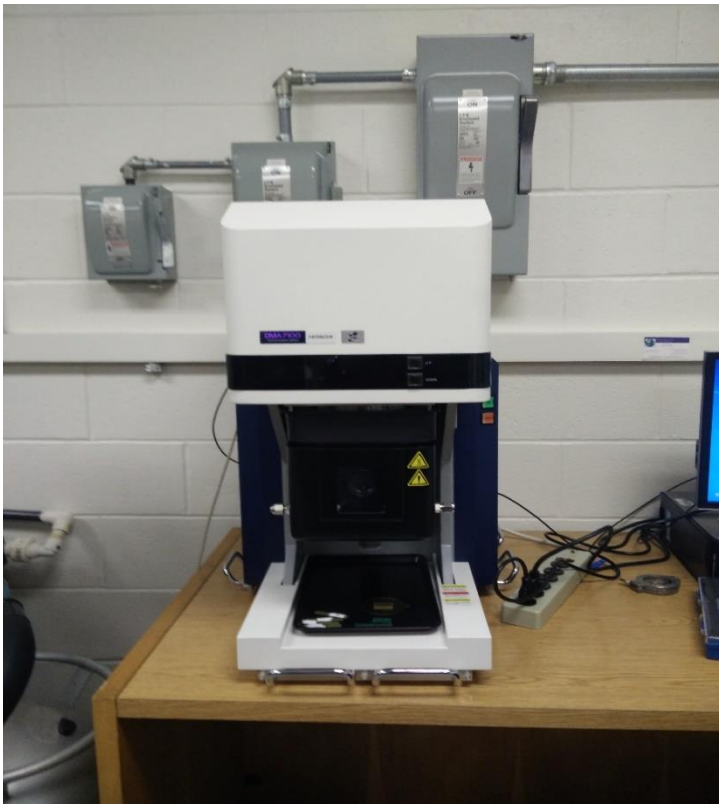


Figure 3-2: DMA7100

Dynamic Mechanical Analysis, otherwise known as DMA, is a technique where a small deformation is applied to a sample in a cyclic manner. This allows the materials response to stress, temperature, frequency and other values to be studied. The term is also used to refer to the analyzer that performs the test. DMA is also called DMTA for Dynamic Mechanical Thermal Analysis.

DMA works by applying a sinusoidal deformation to a sample of known geometry. The sample can be subjected by a controlled stress or a controlled strain. For a known stress, the sample will then deform a certain amount. In DMA this is done sinusoidal. How much it deforms is related to its stiffness. A force motor is used to generate the sinusoidal wave and this is transmitted to the sample via a drive shaft. One concern has always been the compliance of this drive shaft and the effect of any stabilizing bearing to hold it in position.

DMA measures stiffness and damping, these are reported as modulus and tan delta. Because we are applying a sinusoidal force, we can express the modulus as an in-phase component, the storage modulus, and an out of phase component, the loss modulus. The storage modulus, either E' or G', is the measure of the sample's elastic behavior. The ratio of the loss to the storage is the tan delta and is often called damping. It is a measure of the energy dissipation of a material.[8]

To obtain the out-of-plane Young's Modulus, DMA 7100 was used as a tool.

- Temperature - ~+25°C
- Frequency - 0.01 Hz (~0 Hz)

3.3 Test Results

The TMA and DMA test results are tabulated below:

Board Thickness	CTE (x) (ppm/°C)	CTE (y) (ppm/°C)	CTE (z) (ppm/°C)	E (z) (GPa)
62mil	15.5	15.5	39.4	15.37
93mil	16.3	16.3	37.8	13.7
134mil	17.5	17.5	32.8	16.1

Table 3-1: Measurement results of TMA and DMA experiment

CHAPTER 4

MODELLING AND SIMULATIONS

4.1 Introduction to Finite Element Analysis

The finite element method is a numerical method for solving problems of engineering and mathematical physics. Typical problem areas of interest in engineering and mathematical physics that are solvable by use of the finite element method include structural analysis, heat transfer, fluid flow, mass transport, and electromagnetic potential. This process of modeling a body by dividing it into an equivalent system of smaller bodies or units (finite elements) interconnected at points common to two or more elements (nodal points or nodes) and/or boundary lines and/or surfaces is called discretization. In the finite element method, instead of solving the problem for the entire body in one operation, we formulate the equations for each finite element and combine them to obtain the solution of the whole body.

Briefly, the solution for structural problems typically refers to determining the displacements at each node and the stresses within each element making up the structure that is subjected to applied loads. In nonstructural problems, the nodal unknowns may, for instance, be temperatures or fluid pressures due to thermal or fluid fluxes. [20]

FEA consists of three steps:

1. Preprocessing:
    - A geometric model is created.
    - Elements and mesh are generated.
    - Material properties are input.
2. Solution:
    - Loads and boundary conditions are applied.
    - Output control and load step control are selected.
    - Solver is selected.
    - The solution is obtained.
3. Post processing:

- Results are reviewed and listed as needed.

Assumptions:

- All materials considered linear elastic except solder.
- PCB is considered orthotropic.
- Solder is modeled as rate-dependent viscoplastic material using Anand's viscoplastic model.

4.2 QFN Package Dimensions

The package under consideration is of size 6mm x 6mm with varying thickness of 62 mil, 93 mil and 134 mil. Each of them are modeled using ANSYS 17.1 Workbench.

The figure 4-1 below shows the package configuration.[9]

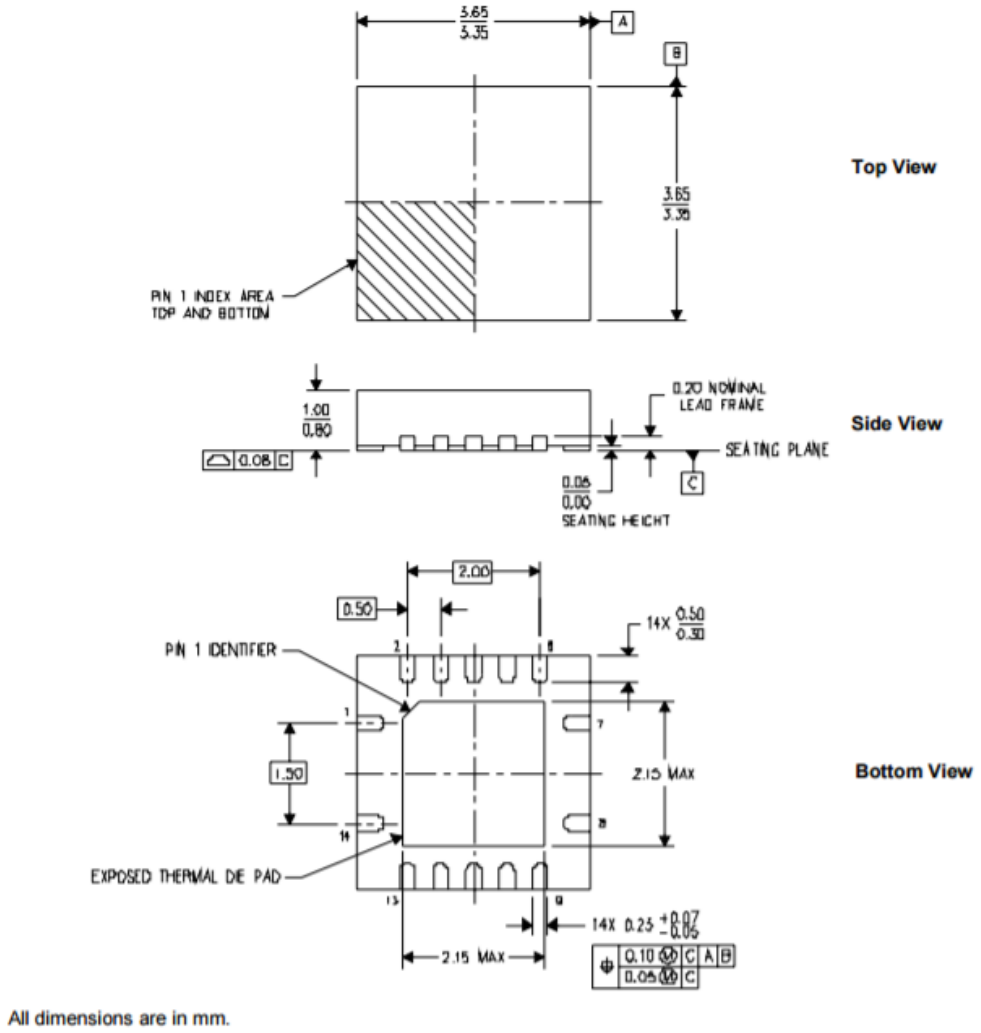


Figure 4-1: Package Configuration

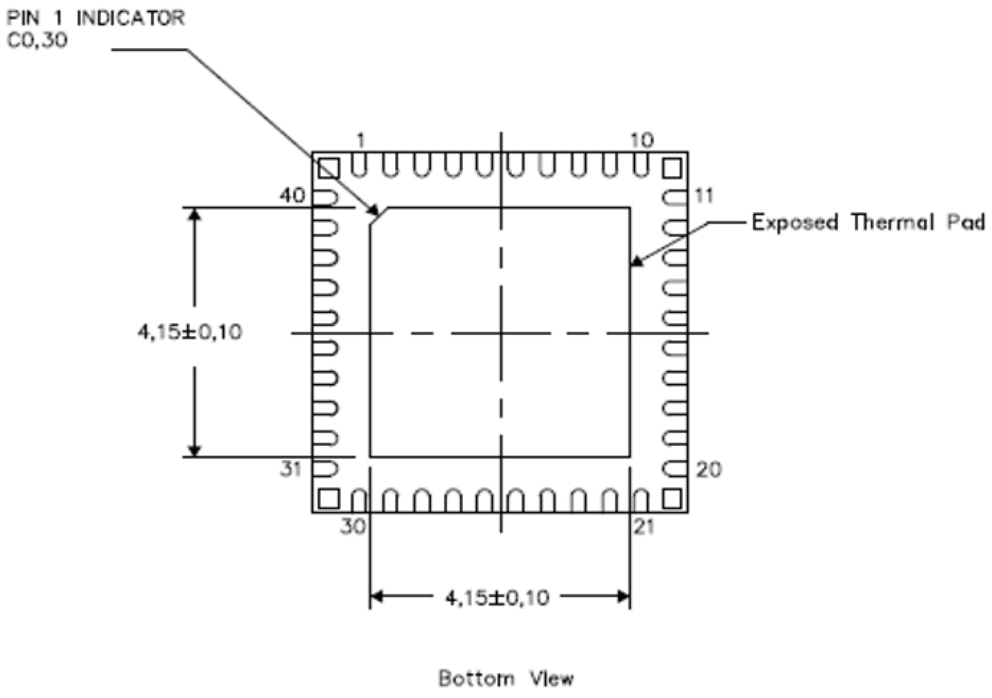


Figure 4-2: Exposed thermal die pad

The exposed thermal pad provides low resistance to the heat path between the die and the PCB. The thermal pad is soldered directly to the PCB. [21]

Table 4-1 shows each of the package dimension.

Component	62 mil Dimensions (mm)	93 mil Dimensions (mm)	134 mil Dimensions (mm)
Package	6 x 6 x 7.5	6 x 6 x 7.5	6 x 6 x 7.5
Die	4.315 x 3.245 x 0.19	4.315 x 3.245 x 0.19	4.315 x 3.245 x 0.19
Die pad	4.8 x 4.8 x 0.1	4.8 x 4.8 x 0.1	4.8 x 4.8 x 0.1
Exposed Thermal Pad	4.15 x 4.15 x 0.1	4.15 x 4.15 x 0.1	4.15 x 4.15 x 0.1
Solder Thickness	0.3	0.3	0.3
Anchor Pin	0.32 x 0.32 x 0.2	0.32 x 0.32 x 0.2	0.32 x 0.32 x 0.2
Pitch	0.5	0.5	0.5
PCB	15 x 15 x 3.45	15 x 15 x 3.45	15 x 15 x 3.45

Table 4-1: Package Dimensions

Error! Reference source not found.4-3 shows a 3D quarter geometry of a 6 x 6mm typical QFN package. A quarter model is considered for faster computation. This does not affect the results. Symmetric conditions are applied on the two faces as shown in the diagram figure 4-4.

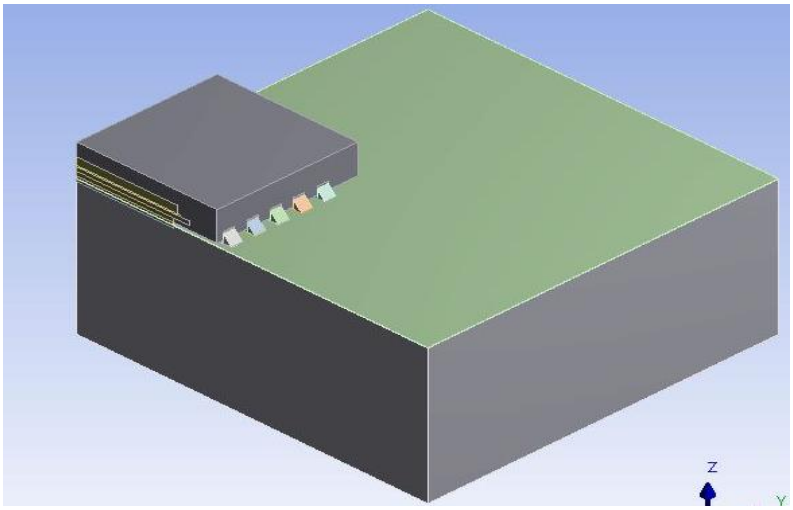


Figure 4-3: 3D quarter geometry of a 6 x 6mm typical QFN package

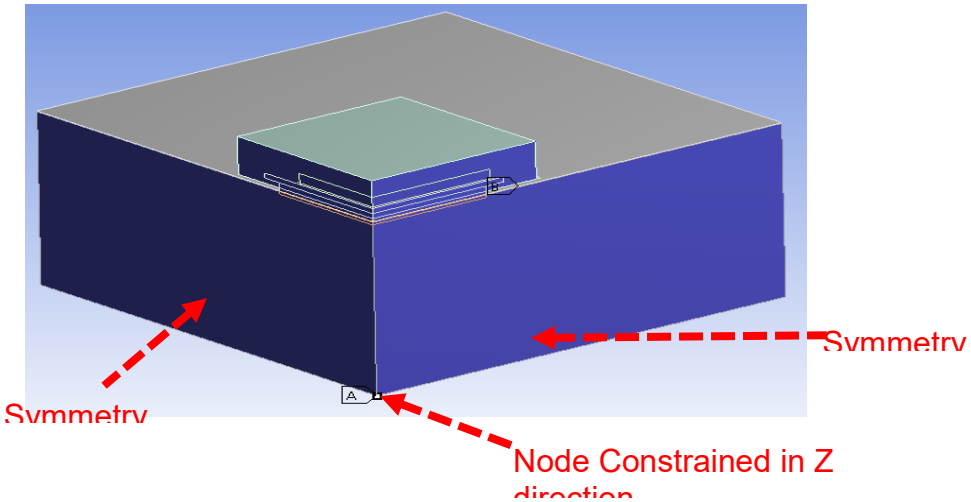


Figure 4-4: Symmetric conditions applied to the model

Table 4-2 shows the structural properties of the package components.

Material	Young's Modulus (GPa)	Poisson's Ratio	Coefficient of Thermal Expansion (ppm/°C)
Die	131	0.278	2.61
Die Attach	11.8	0.3	64
Lead frame	129	0.34	17
Epoxy Mold Compound	3	0.3	10.3
Exposed Die Pad	129	0.34	17

Table 4-2: Structural Properties of Package Components

The solder material used is SAC305 which is made of 96.5% tin, 3% silver and 0.5% copper.[11]

A simple set of constitutive equations for large, isotropic, viscoplastic deformations but small elastic deformations is the single-scalar internal variable model proposed by *Anand and Brown* ~Anand, Brown et al**.** There are two basic features in this Anand model. First, this model needs no explicit yield condition and no loading/unloading criterion. The plastic strain is assumed to take place at all nonzero stress values, although at low stresses the rate of plastic flow may be immeasurably small. Second, this model employs a single scalar as an internal variable to represent the isotropic resistance to plastic flow offered by the internal state of the material. This internal variable is denoted by s, which has the dimensions of stress, and is called to be deformation resistance. There are some reasonable considerations for the simplifications that only a single scalar is used to

characterize the internal structural characteristics of a material ~Brown et al. The set of Anand constitutive equations presented here accounts for the physical phenomena of strain-rate and temperature sensitivity, strain rate history effects, strain hardening and the restoration process of dynamic recovery. [10]

The internal variable s represents an averaged isotropic resistance to macroscopic plastic flow offered by the underlying isotropic strengthening mechanisms such as dislocation density, solid solution strengthening, subgrain, and grain size effects, etc. The deformation resistance s is consequently proportional to the equivalent stress s.

The total strain is expressed as,

$$\varepsilon_{ij} = \varepsilon_{ij}^{e} + \varepsilon_{ij}^{in}$$

where ε_{ij}^{in} is the inelastic strain tensor.

The Anand's model consists of two coupled differential equations that relate the inelastic strain rate to the rate of deformation resistance.

The strain rate equation is represented by,

$$\frac{d\varepsilon_{in}}{dt} = A\left[\sin h\left(\xi\frac{\sigma}{s}\right)\right]^{\frac{1}{m}}\exp\left(-\frac{Q}{RT}\right)$$

The rate of deformation resistance is given by,

$$\dot{s} = \left\{h_0(|B|)^{\alpha}\frac{B}{|B|}\right\}\frac{d\varepsilon_p}{dt}$$

$$B = 1 - \frac{s}{s^*}$$

$$s^* = \hat{s}\left[\frac{1}{A}\frac{d\varepsilon_p}{dt}\exp\left(-\frac{Q}{RT}\right)\right]$$

where $\frac{d\varepsilon_{in}}{dt}$ is the effective inelastic strain rate, σ is the effective true stress, s is the deformation resistance, T is the absolute temperature, A is pre-exponential factor, ξ is

stress multiplier, m is strain rate sensitivity of stress, Q is activation energy, R is universal gas constant, h_0 is hardening/ softening constant, $\hat{s}$ is coefficient for deformation resistance saturation value, n is strain-rate sensitivity of saturation value, and a is strain-rate sensitivity of hardening or softening.[11]

Anand's viscoplasticity law consists of nine material constants and is listed in 4-3. [4]

Anand's constants	SAC305
s_0 (MPa)	2.15
Q/k (K)	9970
A(1/sec)	17.994
Ξ	0.35
M	0.153
h_0 (MPa)	1525.98
$\hat{s}$ (MPa)	2.536
N	0.028
A	1.69

For the thermal properties of the package components, few assumptions were made as the material properties were not readily available.[11]

Material	Thermal Conductivity (W/m/˚C)	Density (Kg/m^3)	Specific Heat (J/Kg/˚C)
Copper Lead Frame	390	8900	390
Die attach/ fillet	2	1910	920.9
Copper exposed pad	390	8900	390
PCB	173.77 (x) 173.77 (y) 0.64 (z)	1666	1369
Epoxy Mold Compound	0.8	1910	920.9
Die	140	2330	703
Solder Mask	0.25	1910	920.9
Solder SAC305	57	9630	167

Table 4-4: Thermal properties of package components

4.3 Modelling Methodology

- The QFN package is modeled as per package dimensions in ANSYS 17.1 Workbench and the material properties are assigned.
- A transient thermal analysis is performed with the die as the only source of heat generation i.e., a power cycle is applied to the die.
- The resulting non-uniform temperature distribution of the body is then transferred to static structural.
- The non-uniform temperature distribution as load along with the thermal cycling load in static structural is applied to run the experiment with power cycling and thermal cycling simultaneously.
- The result gives the plastic work which helps us identify the critical solder joint.

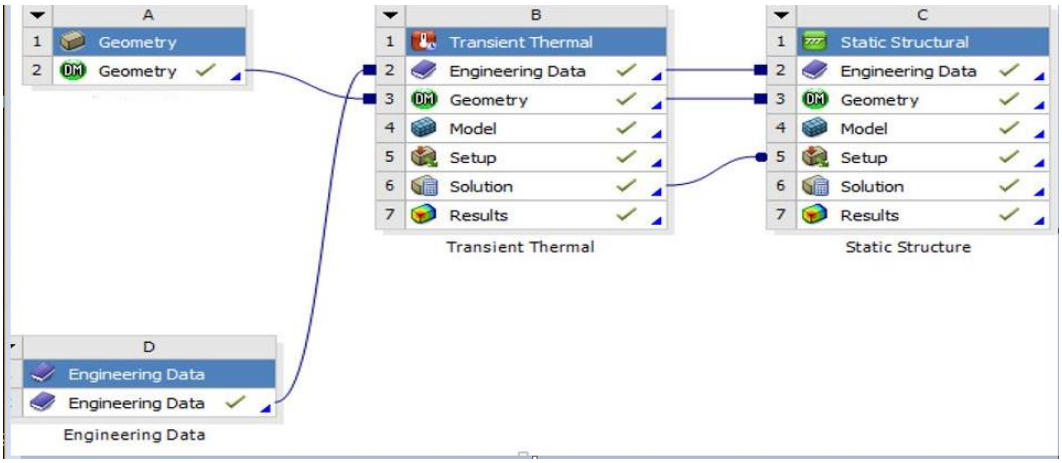


Figure 4-5: Modelling Methodology

Meshing:

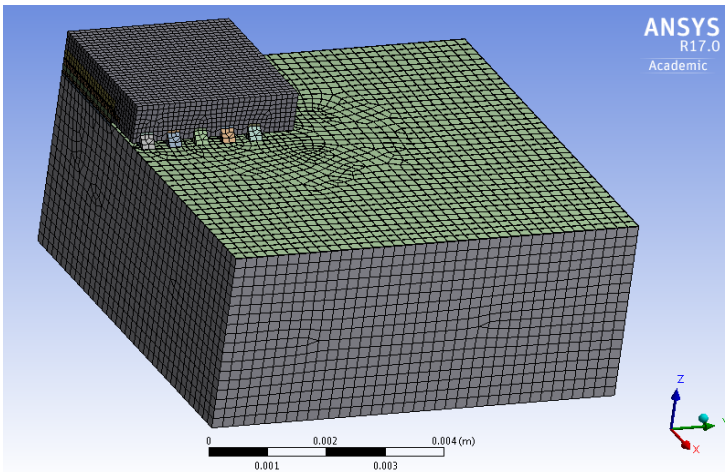


Figure 4-5: Meshed QFN Model

The mesh is Hex dominant. The model is meshed with approximately 83k elements.

Boundary Conditions:

- Symmetry at quarter symmetry cut faces.
- One center node constrained in z direction.
- Convective boundary condition on all the surfaces exposed to the environment.

Loading:

- Thermal load of three cycles is applied to whole model of temperature range -40Cel to 125Cel.

- For the same period of time, simultaneously three cycles of power cycling of 0.5W is applied to die.

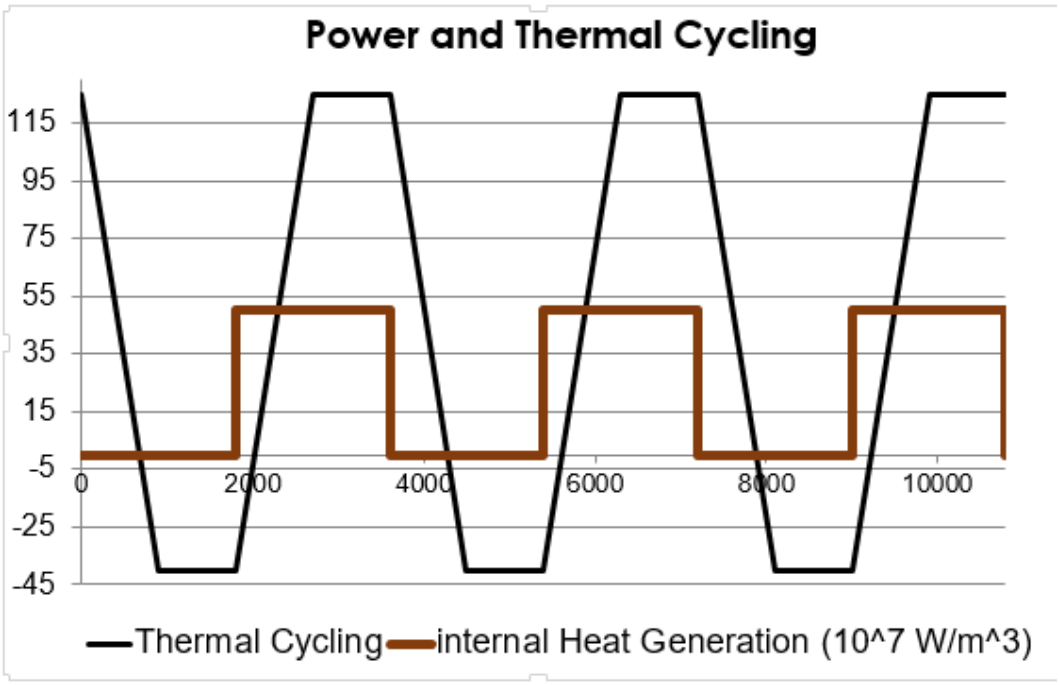


Figure 4-7: Power Cycling and Thermal Cycling applied to the setup

The convective heat transfer co-efficient is chosen such that the maximum temperature in the package does not exceed 125˚C. The convective heat transfer co-efficient considered for this analysis is 23 W/(m^2 ˚C).

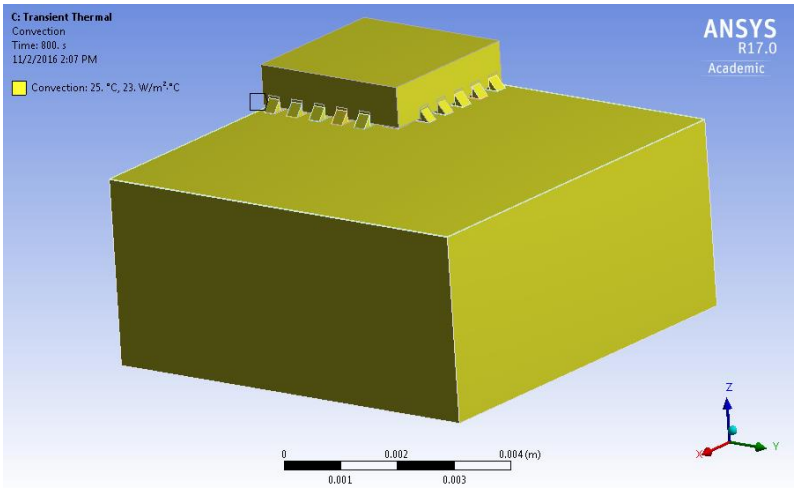


Figure 4-8 : Convective Boundary Condition

Assumptions:

- All materials considered linear elastic except solder.
- PCB is considered linear orthotropic elastic.

CHAPTER 5

RESULTS

5.1 Temperature Distribution

Three cycles of power cycling of 0.5W is applied to the die which produces a non-uniform temperature distribution in the package.

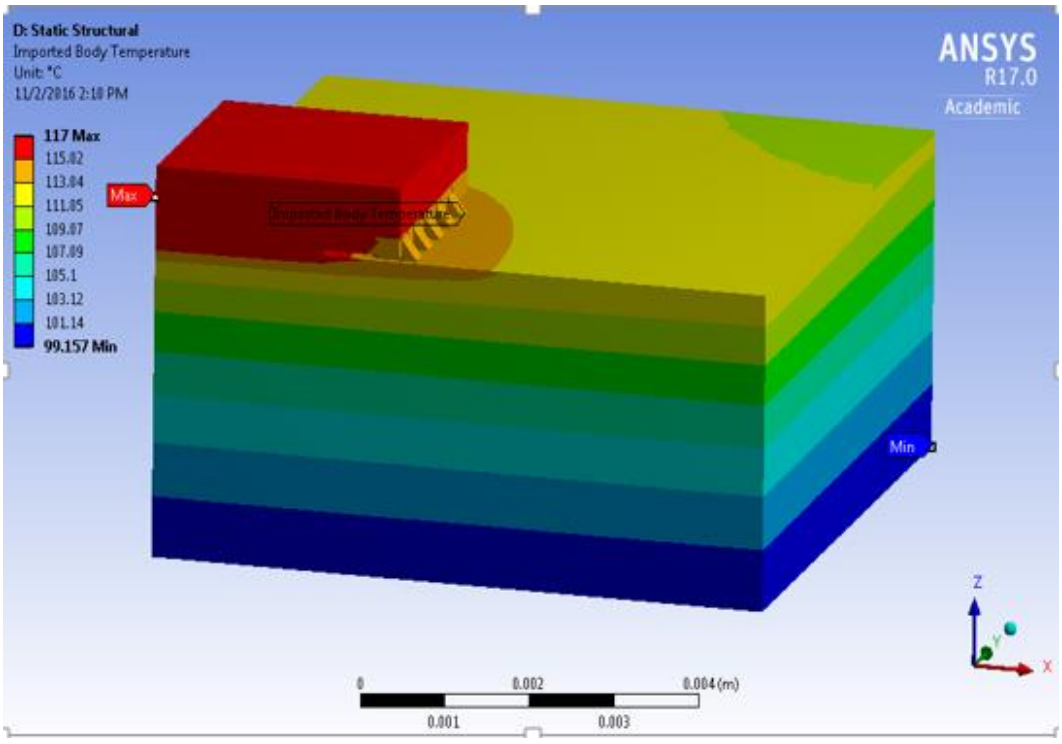


Figure 5-1: Non-uniform temperature distribution

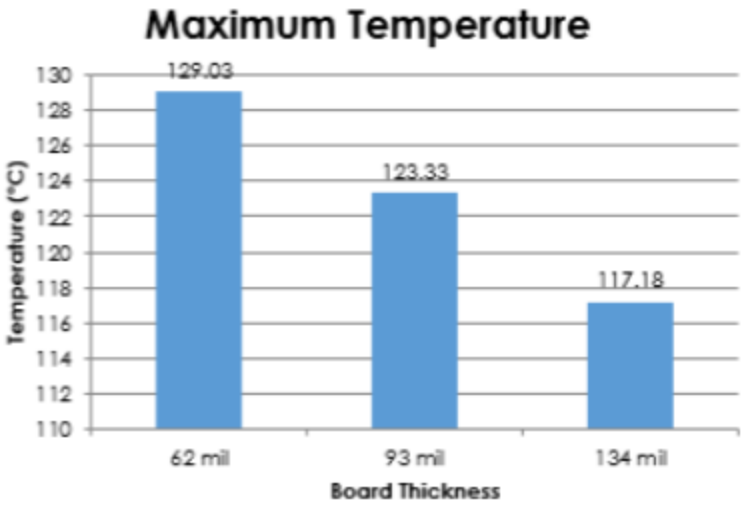


Figure 5-2: Maximum Non-uniform temperature in the QFN boards

The maximum temperature for the *62 mil, 93 mil, and 134* boards are **129.03 degree Celsius, 123.33 degree Celsius, and 117.18 degree Celsius** respectively.

5.2 Deformations

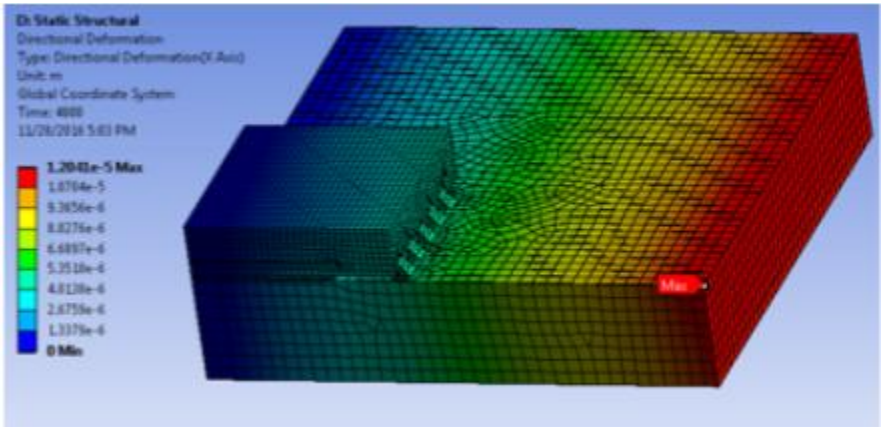


Figure 5-3: In-plane Deformation of the Board

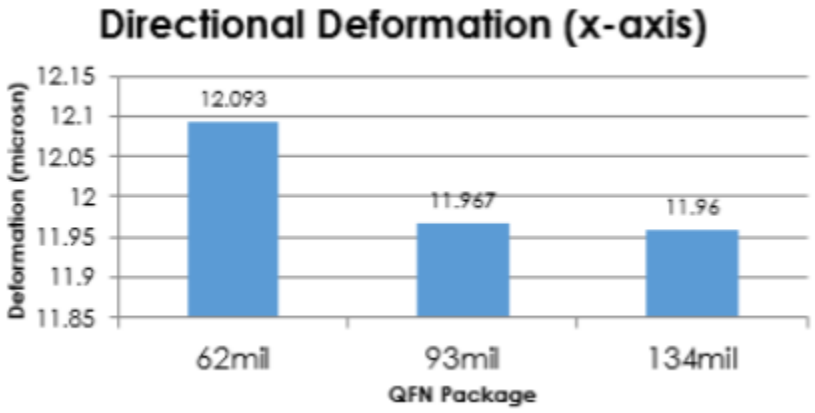


Figure 5-4: Maximum deformation in the QFN boards

Figures 5-3 and 5-4 show the in-plane deformation of the different QFN boards and are found to be **12.093 mm, 11.967 mm and 11.96 mm** for *62 mil, 93 mil and 134 mil* board respectively.

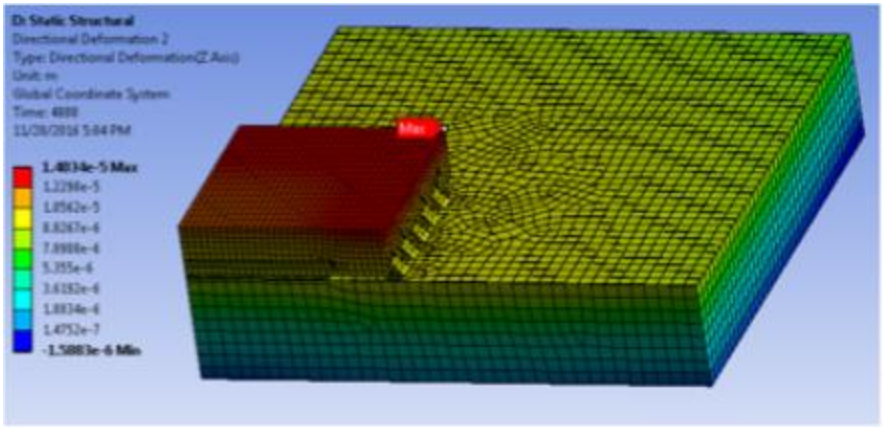


Figure 5-5: Out of plane deformation of the board

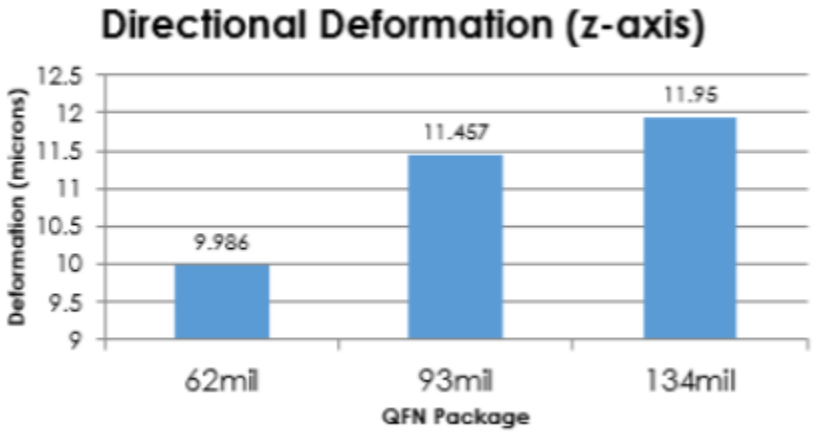


Figure 5-6: Maximum out of plane deformation in the QFN boards

The maximum out of plane deformations are found to be **9.986mm, 11.457mm and 11.95 mm** for *62 mil, 93 mil and 134 mil* board respectively.

5.3 Stress Distribution

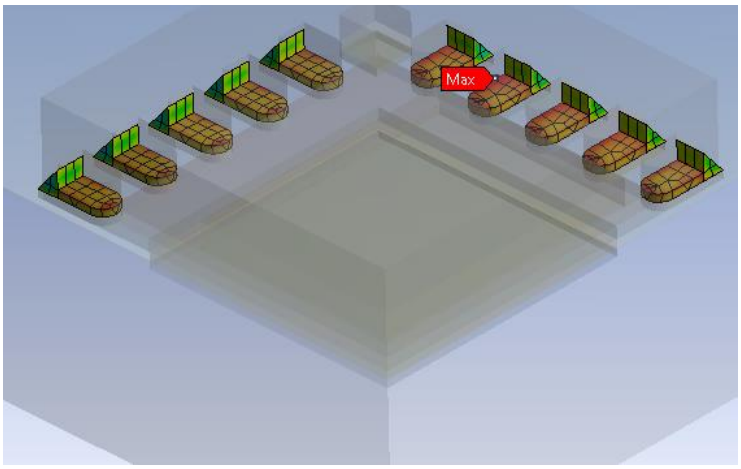


Figure 5-7(a)

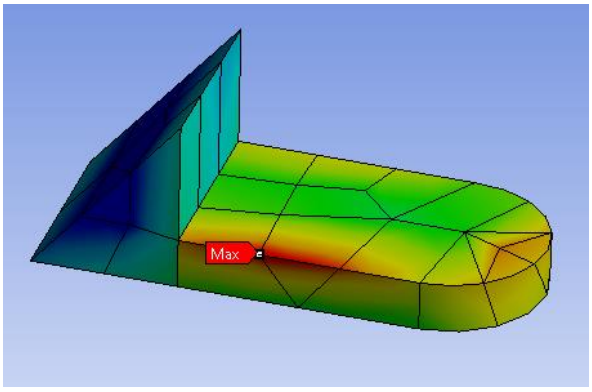


Figure 5-7(b)

Figures 5-7(a) and 5-7(b) represent the maximum stresses developed at the sharp edge of the solder joint

The maximum stresses develop at the sharp edge of the solder joint as shown in the figure.

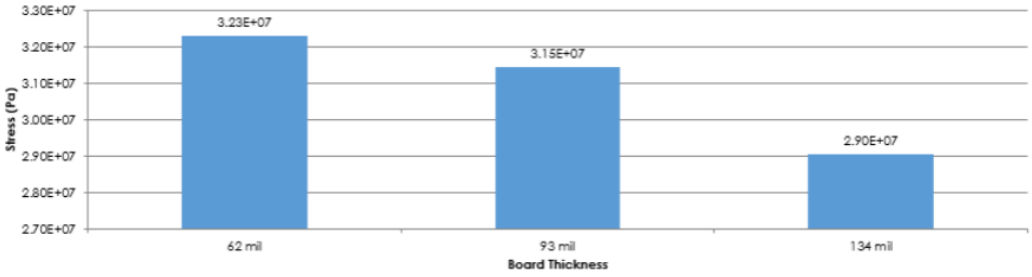


Figure 5-8: Maximum stress developed at the edge of solder joint

The maximum stresses in the *62 mil, 93 mil, and 134 mil* boards are **32.3 MPa, 31.5 MPa and 29 MPa**, respectively.

5.4 Plastic Work

Darveaux [9] and a lot other groups have shown that the increment of inelastic strain energy density per cycle can be used as a fatigue indicator. The inelastic strain energy density (inelastic strain energy per unit volume) is defined by

$$W^{in} = \int \sigma_{ij}\, d\varepsilon_{ij}^{in}$$

where σ_{ij} is the stress tensor and ε_{ij}^{in} in is the inelastic strain tensor. Since we are using Anand's constitutive law for the solder, the inelastic strain in this case is the viscoplastic strain.

Using this model, we obtain the change in plastic work in the model.

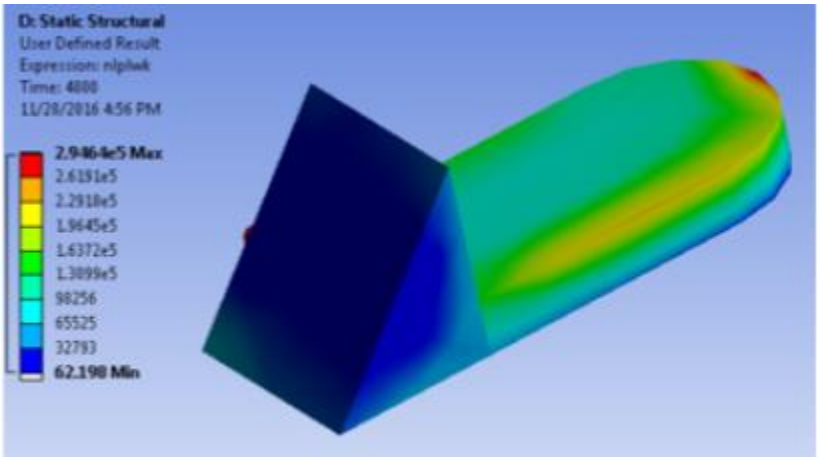


Figure 5-9: Change in Plastic Work

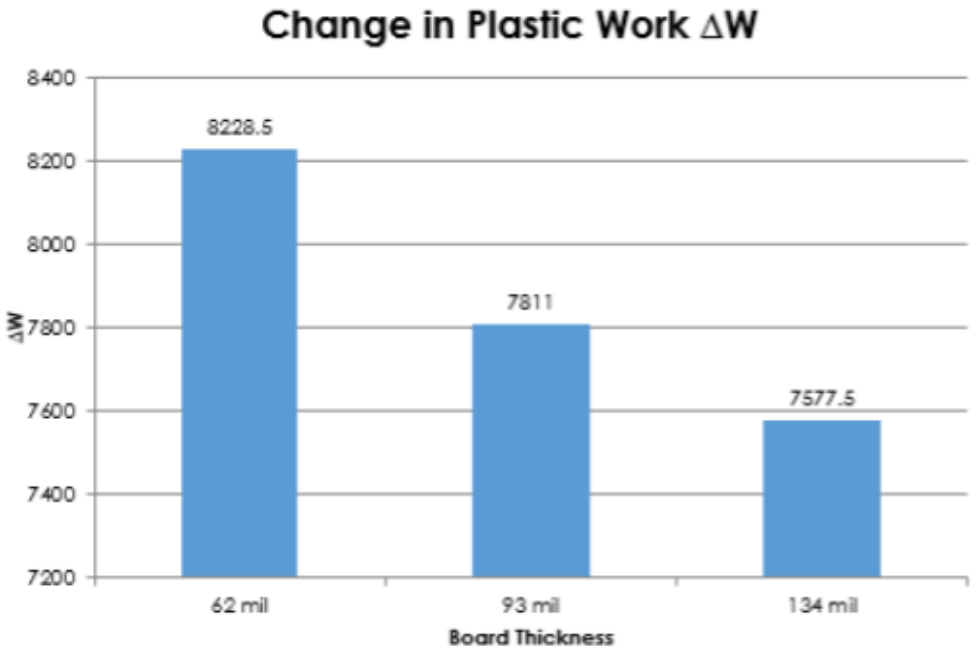


Figure 5-10: Maximum change in plastic work in the QFN boards

The change in plastic work in *62 mil, 93 mil and 134 mil* boards are found to be **8228.5, 7811 and 7577.5** respectively.

We know that thicker boards are less flexible when compared to thinner boards.

The plastic work ΔW obtained was used to calculate the number of cycles to failure using *Schubert et. al & Che and Pang* correlation: [21]

$N_f = (\frac{A}{\Delta W})^k$

Where,

N_f = Predicted life cycles to failure

A = 1.256×10^8 MPa

k = 0.4021

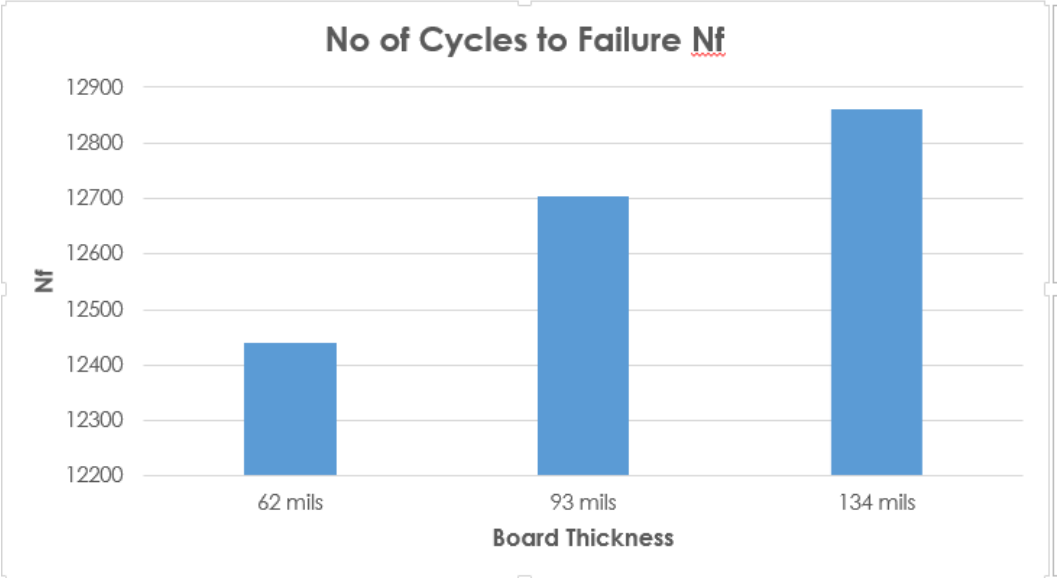


Figure 5-11: No of cycles to failure of each QFN board

Therefore, the number of cycles to failure for the *62 mil, 93 mil and 134 mil* boards are found to be **12441, 12704 and 12860** respectively.

CHAPTER 6

CONCLUSION

6.1 Summary and Conclusion

In this study, a 3D Finite Element model of QFN package is analyzed to assess the board level reliability under power cycling and thermal cycling simultaneously. ANSYS Workbench 17.1 is used for Finite Element (FE) modelling of the package under study. The orthotropic material properties of the PCB for the ANSYS model are determined experimentally using Thermomechanical Analysis (TMA) and Dynamic Mechanical Analysis (DMA). The plastic work induced in the solder joints is assessed by subjecting the package through power cycling and thermal cycling simultaneously. Plastic work can be used to estimate the number of cycles it requires to initiate and propagate the crack inside the solder joint. The analysis includes solving a model with the quarter symmetry QFN model under PC.

- The failure analysis is conducted for three different boards 62 mil, 93 mil and 134 mil.
- The 62mil board has least copper content whereas 134mil board has maximum amount copper content. The 134mil board shows maximum amount deformation due to more expansion of copper as CTE value for Cu is more compare to other.
- Life to failure increases with increase of thickness under power cycling and thermal cycling combined for the three boards.

6.2 Future Work

- The number cycles to failure under power cycling can be determined experimentally.
- Changing material properties will affect the results.
- Board level reliability also depends on copper content that can also be analyze.

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BIOGRAPHICAL INFORMATION

Srinivas Rahul Rao received his Bachelor's degree in Mechanical Engineering from Visvesvaraya Technological University, India, in the year 2011. He worked as a Design Engineer with LeeBoy Construction Equipment (P) Ltd for three years prior to pursuing his Master's in Mechanical Engineering in University of Texas at Arlington from Fall 2014. He joined the Electronics MEMS & Nanoelectronics Systems Packaging Center (EMNSPC) under Dr. Dereje Agonafer and developed a keen interest in reliability and failure analysis of electronic packages. His research interest includes reliability, fracture mechanics, thermo-mechanical simulation and material characterization. During his graduate studies, he was an integral part of the SRC funded project where he worked closely with the industry liaisons. Upon graduation, Rahul plans to pursue his career in the fields of electronic packaging, mechanical design and analysis.