PhD Dissertation

Title:

On the Enhancement of Thermo-Mechanical and Impact Reliability of Passive and Active Microelectronic Devices.

By

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Submitted to the Department of MAE of

The University of Texas at Arlington for

the Requirements for the Degree of

PHD IN MECHANICAL ENGINEERING

The University of Texas at Arlington, Arlington, TX, United States

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Summer 2016

To my beloved family:

My father Muhammad Moqsud Ali, my mother Dilruba Begum, my two sisters Tanjila and Tashrina, my daughter Shamailah and my wife Eshaba

Acknowledgement

First and foremost, I am extremely thankful to my Creator Allah Subhanahu Wa Ta'ala for providing me every opportunity to complete my graduate education in an excellent manner, while overcoming all the obstacles along the way.

I would like to acknowledge my thesis committee's chair, Dr. Ashfaq Adnan, for a lot of things; but not limited to the opportunity to start my graduate student career in UTA through his GRA funding, recommending me for Enhanced GTA fellowship, guiding me to prepare journal manuscripts and his help all throughout my graduate student life. I could not have completed my work without his utmost support and technical guidance.

I also want to thank my thesis co-advisor, Dr. Dereje Agonafer, for introducing the MLCC flex-cracking project and involving me in SRC/ Texas Instruments sponsored project. His guidance was critical for my PhD work.

I want to specially thank Dr. A. Haji-Sheikh and Dr. Wen Chan for taking out their valuable time to evaluate my thesis work and be there as members of my PhD dissertation committee.

Then, there is Dr. Fahad Mirza, to whom I am appreciative for not only being a committee member of my PhD dissertation but also for being a great mentor to me in difficult times.

I am grateful to Mr. Alok Lohia, MGTS, Texas Instruments for his support as the SRC industry liaison.

I would like to mention Sally Thompson, Louella Carpenter, Debi Barton, Lanie Gordon, Mike Baker and Kermit Beird for their help in administrative work, IT support and machine shop throughout my studies at UTA. I would also like to thank my lab mates Peter, Farzad, Fahad, Riaz of MMPL and Hassaan, Malek, Abhishek, Pavan and Sanjay of EMNSPC for being there as a support and as good friends.

Last but not least, I would like to acknowledge my family members support during this long graduate student life for bearing with me. Special thanks to my wife Eshaba for her support in my good and bad times, for all her patience and inspiration. I also have to mention my adorable little daughter Shamailah who brightens up my every day and makes me look forward to a better future.

July 26th, 2016, Arlington, TX

Contents

Dissertation Title: **On the Enhancement of Thermo-Mechanical and Impact Reliability of Passive and Active Microelectronic Devices.**

Abstract: Microelectronic devices are an essential part of human life. The idea of Internet of Things (IoT) where all the everyday devices will be connected with each other transmitting information and operating on their own is becoming very popular. A silicon chip which has millions of transistors in it, has been the heart and brain of the everyday components ranging from personal entertainment, communication to Automotive ECU (electronic control Unit), and health care management systems to home security systems. Every aspect of modern human experience is dependent on this tiny silicon chip. Microelectronic devices can be divided into two broad categories based on their functionality: active and passive devices. Active devices are capable of changing the direction of electron flow. Some of the examples of actives devices are transistors, diodes, LEDs. Passive devices cannot change the direction of the electron flow. Passive devices include resistors, capacitors, and inductors.

Essentially the chip making process is an intricate technology where bulk silicon is transformed into thin silicon wafers. After that series of surface micromachining, etching, material deposition processes are done to achieve a known good die. This tiny silicon is so delicate that it can't be placed on the Printed circuit board on its own. Due to outside heat, moisture and corrosive environment, this chip has to protected by a layer of polymer also known as mold compound. Now inside a silicon chip there are thousands of nanometer pitch interconnects. So to scale up the interconnection level on the silicon chip, wire bonds or micro-bumps are created in a semiconductor package. Even for passive devices such as Multi-layered Ceramic Capacitor (MLCC), termination end has to be connected with the outside world. Conductive terminations are soldered with the land pads on the printed circuit boards.

Active and passive devices have multiple layers of materials in them and also they are connected on the PCB through solder joint. The CTE mismatch among the component (Device, PCB and Solder) will create thermo-mechanical fatigue and eventually components fail due to breaking of interconnection between them. Drop/impact is a common reason for failure. Modern handheld gadgets are prone to repetitive drops on a rigid surface. This high strain rate loading will cause severe damage to interconnect and the device itself, causing failure of the system to meet operational expectations.

This present work focuses on the failure mitigation of the active and passive devices and interconnects. 1st part of the work involves extensive investigation of the MLCC flex cracking problem due to PCB bending, thermo-mechanical fatigue and drop. For mitigating the MLCC flex cracking problem, innovative packaging and interconnection technique are introduced. The 2nd part of the work involves thermo-mechanical reliability estimation and improvement of the active devices (QFN and BGA) on custom printed circuit board. Due to different layup of the prepreg and conductive material in the PCB, the bulk mechanical properties of changes and impacts the board level solder joint reliability of the QFN and BGA Packages. A failure mitigation technique involving tailoring the mechanical properties of the outermost prepreg layers have been proposed to enhance thermo-mechanical reliability.

Chapter 1

Introduction

1.1 Introduction:

Modern human life is all about sharing information on blog and social media, interacting with people all around the world, getting news right after major events, getting connected with friends and family no matter how far they are, using a digital map for traveling, getting real time data of the traffic to and from work. The latest driver in increase of the Internet of Things (IoT). According to Wikepedia, IoT is the network of physical devices, vehicles, buildings and other items embedded with electronics, software, sensors, actuators, and network connectivity that enable these objects to collect and exchange data.[1]. All these essential communications are integral part of life. Taking the input from an analog world, processing the information and converting back to the analog world are intricate steps. The technology that enables this, need constant improvement.

If we open up an electronic device such as a mobile phone or a gaming console we will see a green printed circuit board on which there will be many components soldered or surface mounted. This is known as a printed circuit board (PCB) or printed wiring board (PWB). Each board is basically like a city of electrical components. These electrical components are connected with each other through the underlying copper traces inside the board that allows them to collaborate with each other. Power lines and signal lines are distributed using a complex network of copper traces inside a motherboard. These components can perform many functions to get a desired job done: such as showing a movie on a TV, running a computer model on a server, storing millions of gigabytes of Data. These electronic components can be divided into two main categories: active components and passive components.

Increased functionality in a smaller handheld device creates multi-physics and multi-scale challenges that can be addressed by multi-disciplinary team of engineers and scientists. Bringing increased functionality in a system requires motion, temperature, vibration, and sensors. All these systems need to be packaged on a single PCB so that they can communicate and collaborate with each other. To shrink these devices on a PCB creates a very complex network, an example shown in Fig 1.1. Heat is being dissipated from each of the microelectronic devices during their operation and this heat needs to be removed from the system efficiently from the system. The heating of different materials will result in different expansions and creates thermo-

mechanical bending and load interconnects with stresses. Repetitive stress level creates thermomechanical fatigue and eventually the device fails. ***Understanding the failure mechanism of interconnects of these micro electronic devices during manufacturing and operation can help to establish better design rules so that the device can have better reliability.***

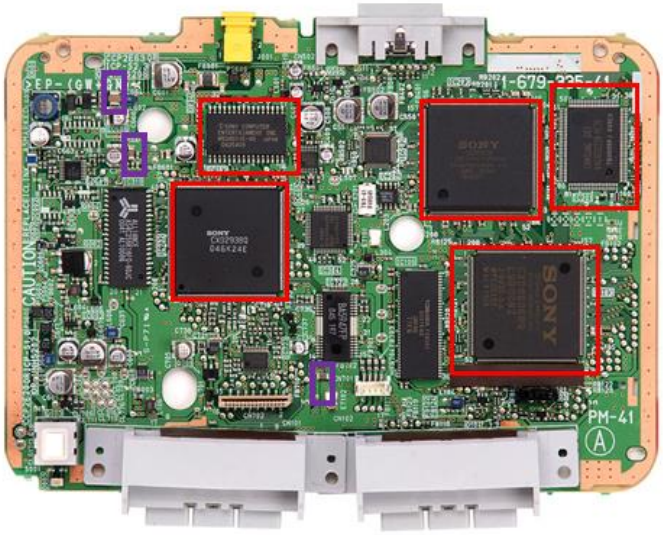


Fig 1.1: The mother board of a Sony PSone video game console. Some of the active components are identified and marked by red boxes and some of the passive components are identified and marked by purple box. [1]

1.2 Passive Devices:

Resistors, capacitors and inductors in a system are known as passive devices. They can sense, monitor, transfer, attenuate and control voltage. Passive components, however, cannot either identify the polarity of a signal nor amplify the electrical signal. Passive components store and disperse electrical energy transmitted from the active components of the system. Transformers, filters, mechanical switches and mechanical relays are also known as passive devices. [2].

Passive components are unable to add gain in the signal or change the polarity in terms of electrical functioning. Main passive components in electrical system are capacitors, resistors and inductors. These components execute various critical tasks such as bias, decoupling, switching noise suppression, filtering, tuning, feedback and termination in an electrical product. These

passive components are the most used devices in an electrical system by number. Almost 80% of electrical components are passives and they occupy 50% of the real estate of the PCB. [2]

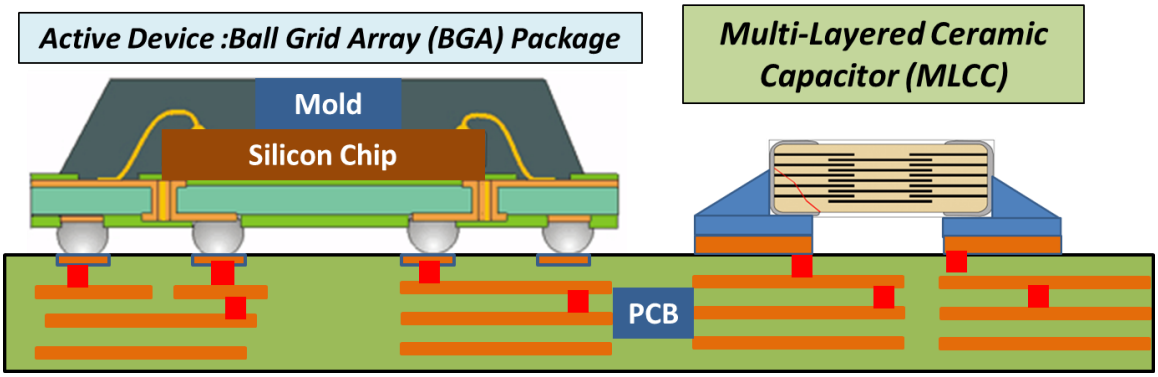


Fig 1.2: Active and passive devices on a printed circuit board.

According to NEMI 2000 roadmap [2] the ratio for active and passives are below:

Product	IC	Passive Components	Total Components	Passive/Active
Notebook Computer	53	820	900	6:01
Desktop Computer	182	1066	1285	15:01

Clearly, the number of passive components is way more than the number of active components on a system.

1.3 Active Devices:

Active components can add gain and change the polarity of the signal which is also known as switching. Transistors, PN junction diodes, bipolar Junction Transistors (BJT), Field Effect Transistors, analog integrated circuits and digital integrated circuits, displays, sensors and processors. All the critical heart and brain of any electrical system are the active components.

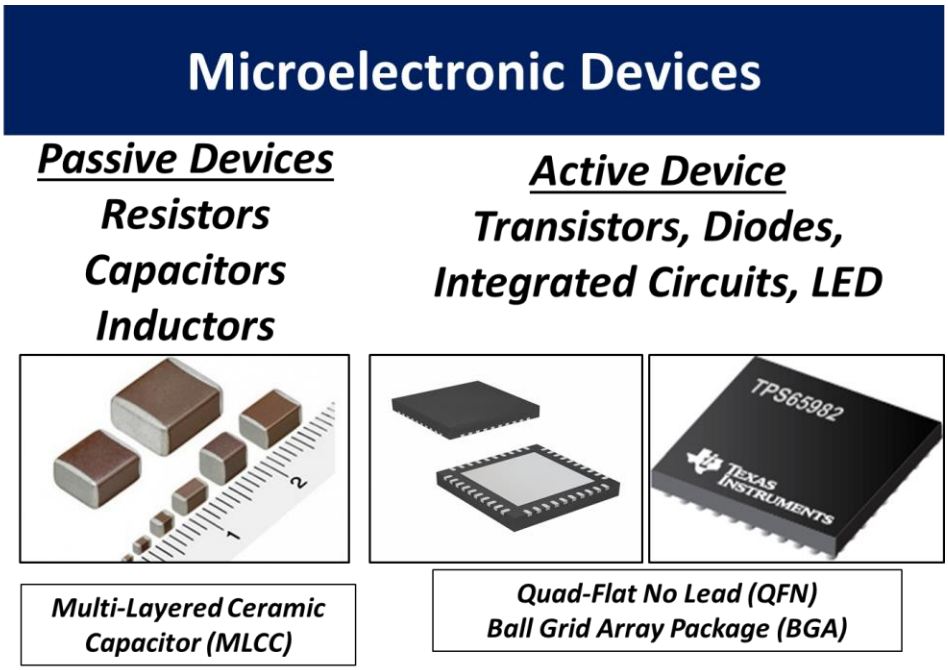


Fig 1.3: Active and Passive devices.

It all starts in the Fab, where a series of operation result in a silicon wafer containing thousands, then millions, and now billions of transistors on a single chip. These transistors, in turn, are interconnected to the outside world using packaging technology. One of the most common inter connect technology is a lead frame based technology where the bond pads on the silicon IC is fanned out using wire bonds. These wire bonds are again connected to the pads on the lead frame which can be soldered to the PCB land pads. Another widely implemented packaging technology is called Ball Grid Array (BGA) where area array interconnect is used between the substrate and board. The die in BGA can be interconnected using peripheral or wire bond from the chip to the substrate or area array from chip to substrate using flip chip technology.

1.4 Microelectronic Packaging:

The silicon IC itself is too miniscule and fragile a component to be placed on a printed circuit board. To make it work, we need to place it inside a protection so that the outside environments such as temperature, moisture, mechanical vibration do not affect its performance. At the same time it needs to be connected with the outside world so that it can communicate with other components in the system. This is done by introducing microelectronic packaging. The most important tasks of a microelectronic package are:

- Provide electrical inter-connections among the various devices in the system.
- Protect the device from outside environment. (Moisture, contaminants, temperature).
- Provide heat dissipation path for the system.
- Fan out the interconnect size from the device to the PCB (ex. BGA – wire bond to substrate, solder balls to PCB).

1.5 Scope of Present Work

Passive devices such as the capacitors, resistors and inductors are integrated in a single microelectronic device and packaged as system in package (SiP). During assembly and operation of the devices, bending, thermal loading and mechanical vibration can create failures in the solder interconnect**. This thesis concentrates on the failure mitigation of the active and passive devices and interconnects.** Extensive investigation of the MLCC flex cracking problem was carried out to understand and mitigate the cracking of the MLCC due to PCB bending, thermo-mechanical fatigue and drop. For mitigating the MLCC flex cracking problem, innovative packaging and interconnection technique are introduced. The 2nd part of the work focuses on the thermo-mechanical solder joint reliability estimation and improvement of the active devices (QFN and BGA) on custom printed circuit board. Due to different layers of the p insulated and conductive material in the PCB, the bulk mechanical properties of changes and impacts the board level solder joint reliability of the QFN and BGA Packages. A failure mitigation technique involving tailoring the mechanical properties of the outermost prepreg layers has been proposed to enhance thermo-mechanical reliability.

Reference:

[1] https://commons.wikimedia.org/wiki/File:PSone-Motherboard.jpg

[2] Tummala, Rao. *Fundamentals of microsystems packaging*. McGraw Hill Professional, 2001.

Chapter 2

Thermo-mechanical and Impact/Drop Reliability Enhancement of Multilayered Ceramic Chip Capacitor

2.1 Introduction:

Multi-Layered Ceramic Capacitors (MLCC) is indispensable part for the desired performance of electronic components. Capacitors, resistors and inductors,known as passive elements, are critical for the proper functioning of semiconductor systems. Semiconductor devices such as Microprocessors, Digital Signal Processors, Micro-Computers, and FPGAs are equipped with Ceramic Capacitor Chips. These chips act as a power storage device for the semiconductors. They eliminate noises in the signal and supply proper operating input voltages to the semiconductors. Their performance is really crucial for reliable operation of these sophisticated micro-electronic systems. There has been a rapid increase in the number of MLCCs used in electronic devices. For example, some notebook computers use about 730 units and about 230 units are present in the cellphone. Large systems like digital TVs have 1000 units or more of ceramic capacitors. It is therefore critical we address the reliability of these devices.

Cracking in Ceramic Chip Capacitor occurs in two stages during the life of the component. The first is during the manufacturing process and second is in the assembly and the handling of capacitors. To understand the different types of cracking we need to analyze the problem at both stages. During manufacturing, the capacitor brick goes through a very high temperature in the kiln furnace where the metal and the ceramic dielectric join together. Due to poor adhesion of the two surfaces, defects and voids may form at the metal-dielectric interface. Residual stresses may affect the structural integrity of the component during the soldering process. Also, during the assembly onto the PCB board, pick and place machine can cause compressive loading on the ceramic block and that enhances the propagation of the crack that already exists in the ceramic capacitor. During handling and mounting of the PCB board, the PCB can bend and the cracks inside the ceramic capacitor are subjected to tensile stresses that try to open up the crack. This mechanism of cracking is known as Flex Cracking in MLCC. In this case, stresses due to the bending load are high enough to exceed the fracture strength of the ceramic material and causes the crack to propagate in an audible snap. Optimum amount of soldering mass is crucial for the safe operation of the component. Excessive solder transfers all the stresses to the capacitor body and thus cracking happens fast. Solder shortage can also cause early fatigue failure of the solder itself.

2.2 Previous research on the MLCC cracking Problem:

Cracking in MLCC has been widely studied previously using experimental and computational technique. Park et al. [2] studied the effect of various design parameters on the developed maximum principle stress inside the capacitor using experiments and finite element methods. Two different models of the capacitor block with varying chip thickness were considered. Mode of Cracking was observed to be different for both the models. In one case the cracking started from the end point of the termination and in another model multiple cracks propagated from the interface of the termination and the chip capacitor. This variation in the cracking mode cannot be described by using maximum principle stress as a failure metric. So to have a better understanding of the cracking processes and failure mechanisms, we need to apply fracture mechanics approach.

Prume et al.[3] investigated the effect of loading profile and history on the reliability of 1206 multilayer ceramic capacitors using Finite Element Method. The variation of soldering temperature, the preheating temperature, the thickness of the nickel layer, the number of inner electrodes, and the soft solder geometry are considered critical variables in determining the reliability of MLCC. The failure probability is calculated for each parameter from preheating to bending. The failure probability increases with the decrease of solder heights. Also, the failure probability decreases as the thickness of the nickel layer in the capacitor is lowered.

Manufacturing and installation of these tiny passive elements on the PCB also put bending loads that can eventually be enough to create cracks. After surface mount assembly process depaneling process is needed to isolate each Printed Circuit Boards from tooling and fixture. This might cause severe bending of the PCB and leads to cracking of the capacitor block. Dennis et al. [4] investigated the effect of PCB depaneling on the reliability of the multilayer chip capacitor. The depaneling process is obtained by simulating a similar cantilever bending process of the PCB. The relationship between the component developed component stress and the board level strain was observed. This study could be used to see the effect of different board level configuration on

the component stresses and how the reliability of the components varies as the stiffness of the board changes.

Soldering Process generates lot of stresses in the capacitor block that eventually breaks the capacitor. Wave Soldering and hand soldering involves high temperatures at which the solder material melts and coalesces with the copper pad on the PCB side and with the termination material on the Capacitor side. The modern surface mount technology has shifted to lead free solder and it created some challenges on the reliability of the components. Blattau et al. [5] studied the effect of solder material on the flex cracking in Ceramic Chip Capacitors. Since Pb free solders are stiffer than the standard Sn37Pb solder, the probability of failure will change. Stress-strain curves of three solder material were analyzed and it was observed that the low yield strength of Sn37Pb solder can withstand more deformation of the board and do not transfer much load to the capacitor.

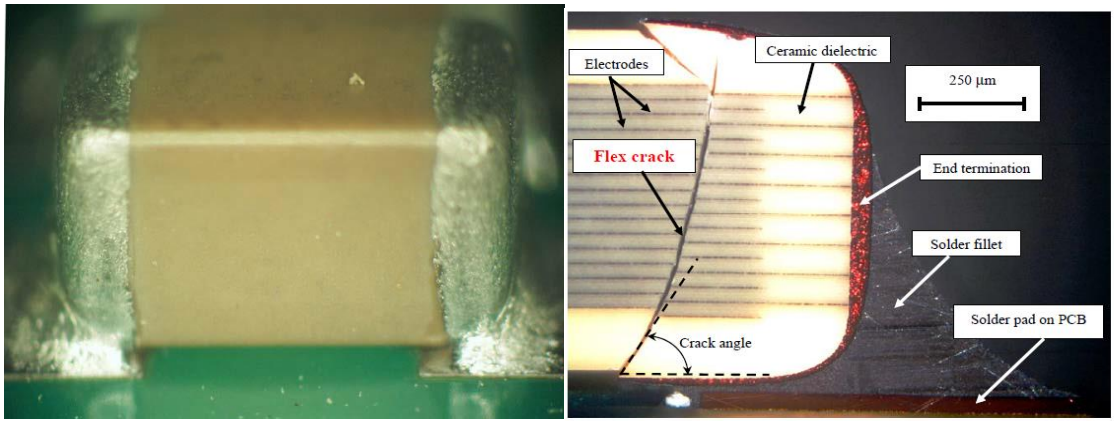


Fig 2.1: MLCC on PCB and Flex Cracking in Multi-Layer Ceramic Capacitor. [1]

2.3 Problem Statement:

Ceramic Capacitors are experiencing failure due to the excessive bending of the printed circuit board. The reasons for board flex cracking are as follows:

- Pick and place machine loading;
- Singulation of the PCB units;
- Placing other components on the PCB;
- Placing slots near MLCC on the PCB;
- PCB flexing during drop; and
- Thermo-mechanical loading due to temperature change.

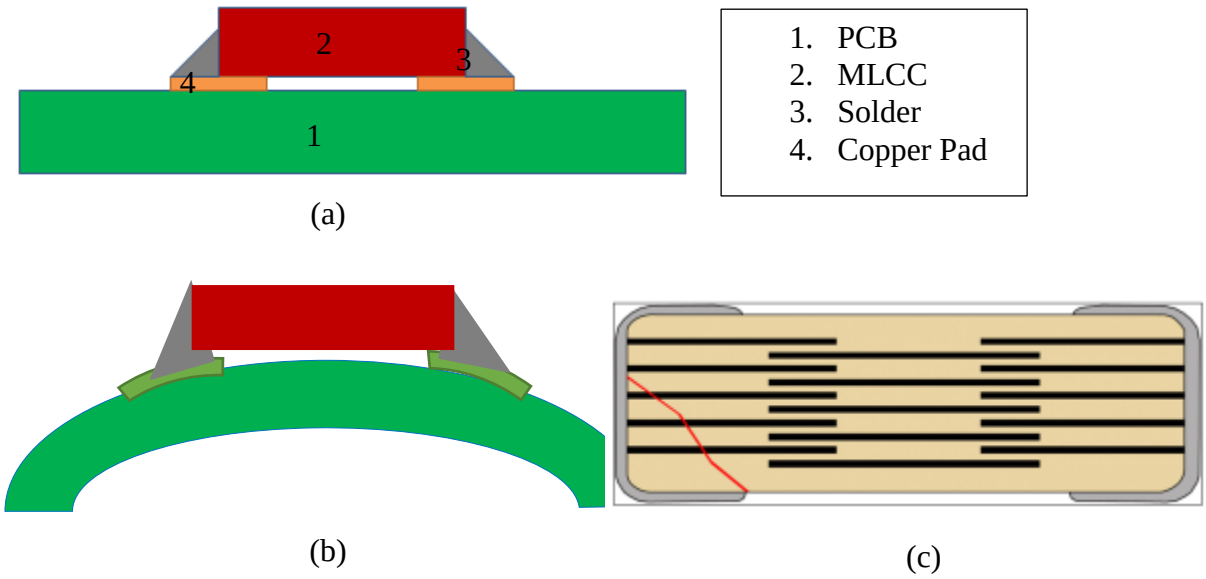


Fig. 2.2 (a): Schematic of MLCC soldered onto the PCB. (b) Schematic showing bending of the PCB and possible deformation mode of other system components. (c) Observed Flex cracking in Capacitor due to bending of the integrated system. [6]

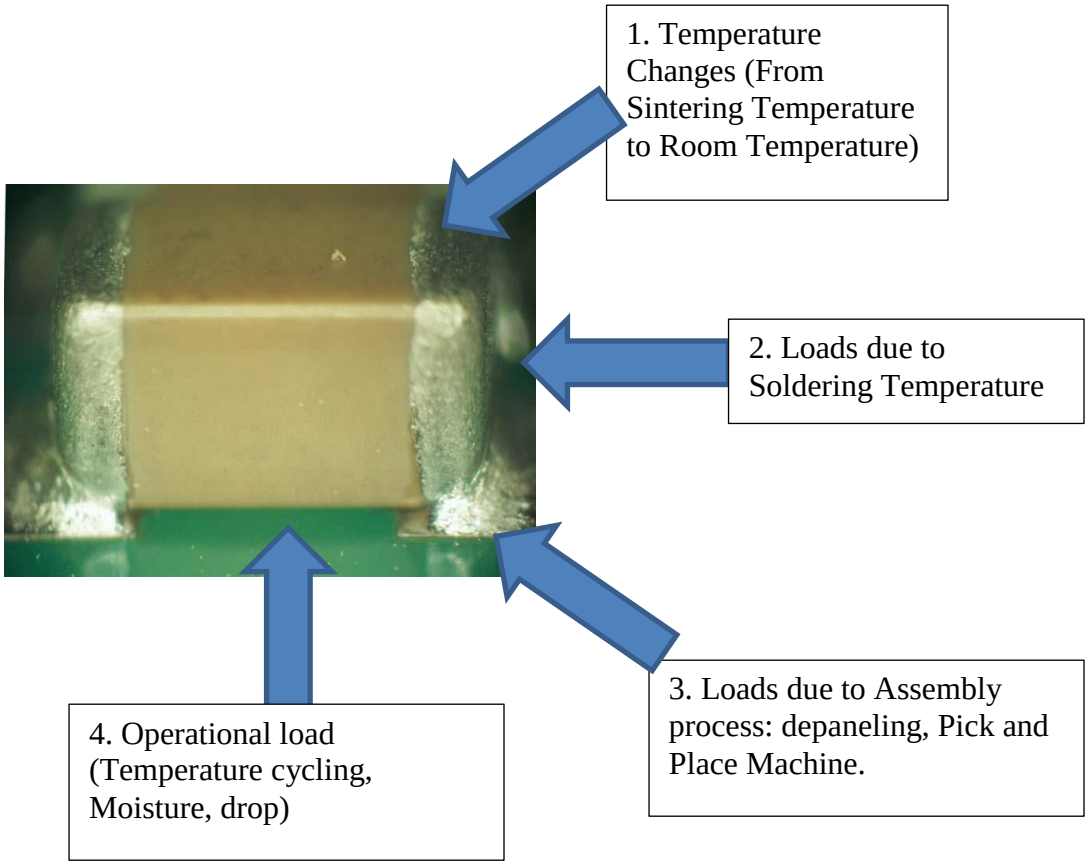


Fig 2.3: MLCC subjected to different thermo-mechanical loads generating from manufacturing, assembly and operating environments.

2.4 Research objectives and proposed studies to mitigate the Cracking failure of the ceramic capacitor:

The major research objective of this dissertation is to quantify various failure mechanisms associated with manufacturing, assembly and operational loads so that reliability issues of MLCC devices can be efficiently mitigated. **In the 1st phase of this study** the failure mechanism of MLCC and the interconnect materials are quantitatively investigated. The critical structural, design and material parameters to mitigate/minimize failure in MLCC induced by thermal, mechanical and impact/drop events have been determined.

As observed in Fig. 2.2 (c), one intriguing phenomenon is that the cracking always happens at about 70 degrees from the horizontal position. So, to understand the crack initiation propagation, one needs to understand the modes of cracking and how the cracking angle changes due to contribution of the both Mode I and Mode II stress intensity factors when the material/system is subjected to bending. Once the underlying cause of crack deflection at a particular angle has been understood, measures can be taken to suppress the cracking and reduce the angle of cracking so that the minimum number of electrodes is being cut by the crack. This will preserve the capacitance and would make it operational in a fail-safe condition. Using well-known G.C. Sih's [1] energy criterion theory, a case-specific analytical model to demonstrate the cracking mechanism of the capacitor as well as to quantify the modes of cracking has been developed.

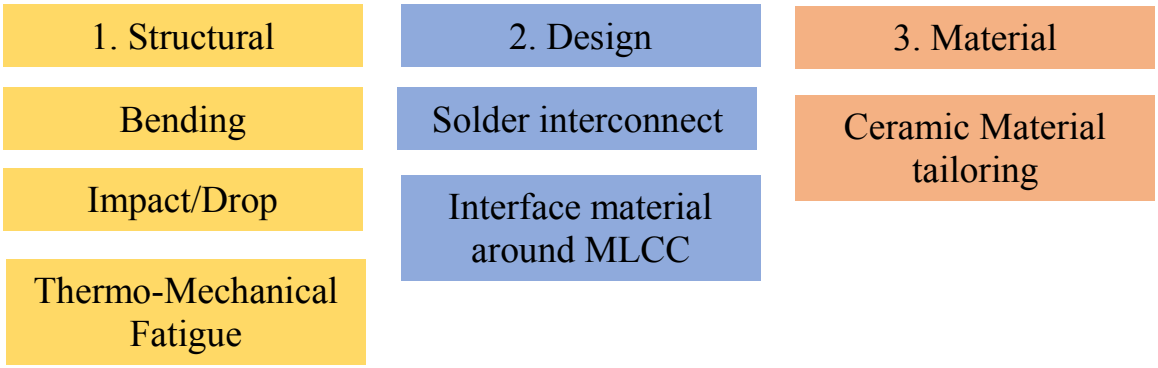


Fig 2.4: Research strategies developed for mitigating the flex cracking.

In the 2nd phase of the study, we investigated the behavior of MLCC subjected to PCB static mechanical bending. PCB is subjected to mechanical bending load due to various operational and manufacturing processes, such as installing and surface mounting other components, shipping, depaneling, installing slots on the PCBs. A 2D finite element model has been be used for analyzing the deformations and stresses in the MLCC when the MLCC/PCB assembly is subjected to bending. Crack propagation angle, stress, intensity factors developed at the crack tip has been systematically analyzed. Various design parameters such as solder joint profile: bulbous, shrunk, straight and optimum; solder joint wetting and stand-off height, termination material properties has been engineered such that the developed stress intensity factor and crack propagation are less.

In the 3rd phase of the study thermo-mechanical fatigue of the MLCC/PCB assembly has been investigated. Due to the coefficient of thermal expansion mismatch between the PCB and MLCC, the solder joint that connect the two components, would be subjected to thermal stress during accelerated thermal cycling. MLCC block is brittle and cracks will form, initiate due to the bending of the PCB/MLCC assembly. Impact of solder joint profile have been analyzed to see what type of solder joint would reduce the cracking in the MLCC and increase the fatigue life of the solder joint. The effects of PCB material properties and the PCB thickness on the solder joint fatigue life and on the developed stress intensity factors were analyzed.

In the 4th phase of the study, the effect of impact/drop of the MLCC/PCB assembly has been analyzed using 3D finite element modeling. Handheld Electronic devices are prone to dropping events. Such events induce mechanical bending of the MLCC/PCB assembly. This would create stress concentration at the interface corners of the MLCC and the terminations. After repetitive dropping events the crack will be initiated as the loads are higher than material strength. Implicit and explicit FE modeling has been used to develop the methodology for simulation drop/impact events. In implicit analysis, shock acceleration is provided to the MLCC/PCB assembly and overall response of the MLCC block and the solder joint is analyzed. In explicit dynamics method, the whole board with MLCCs will be dropped on a rigid base at a prescribed termination velocity and overall stresses in the solder joints, MLCC block have been studied.

The 5th step of the study, the various interconnect design options for Surface mount MLCC has been explored. Interconnect deign will help to sustain large deformation due to bending. This will reduce the fatigue cracking in the solder joint and also the stress transfer to the capacitor material, enhancing the thermo-mechanical and impact reliability of these components. A FEM model has been developed where MLCC is surface mounted at an angle. It has reduced stress build up in one corner of the MLCC and increases it in another corner. Another innovative idea is to create spring like interconnect so that it will absorb large deformation and do not transfer stresses to the MLCC block. Another design option includes putting resin coated copper or any other buffer material partially at the interface of the termination and the MLCC block to remove the stress concentration point thereby improving the thermo-mechanical and impact reliability of these components. That sacrificial material creates a barrier and helps MLCC ceramic material to sustain the larger stress developed at the termination corner. This methodology has been proven to reduce the maximum stress significantly. This hypothesis has been validated by performing Finite Element simulation.

Reference

[1] Sih, George C. "Strain-energy-density factor applied to mixed mode crack problems." International Journal of fracture 10.3 (1974): 305-321.

Chapter 3

Finite Element Analysis of Mechanical Bending of the MLCC

3.1 Introduction:

Manufacturing and installation of the passive elements (i.e. MLCC) on the PCB invites bending loads that can eventually lead to cracking and fracturing of the element. After surface mount assembly process de-paneling process is needed to isolate each Printed Circuit Boards from tooling and fixture. This might cause severe bending of the PCB and leads to cracking of the capacitor block. Dennis et al. [4] investigated the effect of PCB de-paneling on the reliability of the multilayer chip capacitor. The de-paneling process is obtained by simulating a similar cantilever bending process of the PCB. The relationship between the component developed component stress and the board level strain was observed. This study could be more used to see the effect of different board level configuration on the component stresses and how the reliability of the components varies as the stiffness of the board changes. Soldering Process generates lot of stresses in the capacitor block that eventually breaks the capacitor. Wave Soldering and hand soldering involves high temperature at which the solder material melts and coalesces with the copper pad on the PCB side and with the termination material on the Capacitor side. The modern surface mount technology has shifted to lead free solder and it created some challenges on the reliability of the components. Blattau et al. [5] studied the effect of solder material on the flex cracking in Ceramic Chip Capacitors. As Pb free solders are stiffer than the standard Sn37Pb solder the probability of failure will change now. Stress-strain curves of three solder material were analyzed and it was observed that the low yield strength of Sn37Pb solder can withstand more deformation of the board and do not transfers much load to the capacitor.

In this work 2D Finite Element Simulation method has been used to analyze the effect of different solder joint parameters on the Crack propagation angle, stress, intensity factors inside the Multi-layered Ceramic Capacitor. There are couples of design variables we can change to come up with the optimum setup for mounting MLCC on the PCB for improving MLCC device reliability. This will ensure that if the crack at the stress concentration region propagates then the number of electrodes cut by the crack is less. Then the overall capacitance drop will also be less. MLCC will still have operating capacitance as long as it has sufficient number of electrodes intact. In this study, the change in cracking angle, the critical stress intensity factors and the J-integral were considered as the critical factors for analysis. Solder wetting height, solder stand-off height and solder joint profile etc. are changed and corresponding change in the cracking

angle are recorded. Based on this type of detailed analysis a designer can choose optimum parameters so that the crack deflection angle is the highest and the stress concentration factor and the J integral is the lowest.

3.2 Crack mitigation Technique:

- Analytical Methods and Finite Element Simulation tool to analyze the effect of solder joint parameters on the crack propagation angle, stress intensity factors inside the Multi-layered Ceramic Capacitor.
- Solder wetting height, solder stand-off height, solder profile etc. are considered and corresponding change in the cracking angle and developed J integral have been recorded.
- This fail-safe methodology ensures that if the crack at the stress concentration region propagates then the number of electrodes cut by the crack is less.

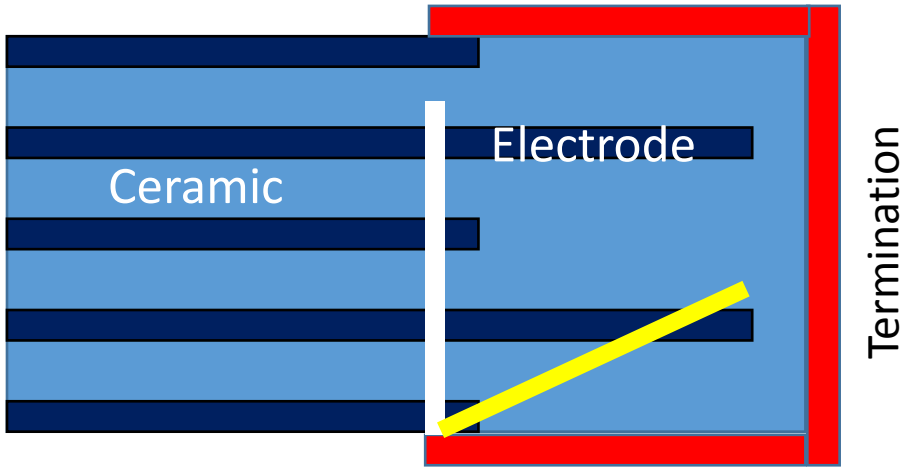


Fig 3.1: Controlling crack deflection angle by designing robust interconnects.

3.3 Maximum Hoop Stress Criteria for Cracking in Brittle Material

Erdogan and Sih [10] have developed the maximum hoop stress criterion for deteting the crack propagation angle. In their theory, they have proposed that the crack will choose the direction for

propagation in which the maximum hoop stress $\sigma_{\theta\theta}$ occurs (i.e., the shear stress $\sigma_{r\theta}$ is zero). Therefore the crack initiation angle θ_0 is obtained by solving the equation below:

$$\cos\frac{\theta_0}{2}\left[K_I \sin\theta_0 + K_{II}\left(3\cos\theta_0 - 1\right)\right] = 0 \quad \text{----------3.1}$$

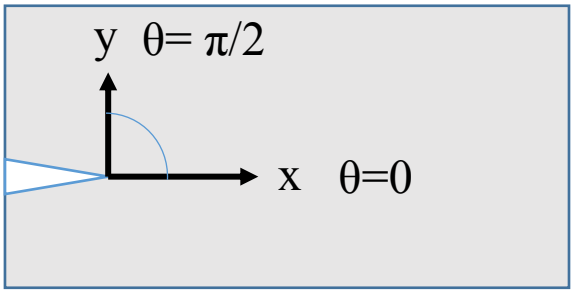


Fig 3.2 : Crack Deflection Co-ordinate system.

By providing the crack tip stress intensity factors for all the cases run in 2D Finite Element model we calculated the crack deflection angle.

- For pure Mode I cracking, K_{II} =0, so solving the above equation we get $\theta_0 = 0,\ \pi$
- For pure Mode II cracking, K_I =0, so $K_{II}\left(3\cos\theta_0 - 1\right) = 0$ and $\theta_0 = \cos^{-1}\frac{1}{3}$
- For MLCC on PCB bending with 1 mm displacement, from FEA model we got K_I = 0.315MPa√m and K_{II} = 0.060551 MPa√m
- Plugging K_I and K_{II} values into the crack propagation criteria we get $\theta_0 = -20.38°$.

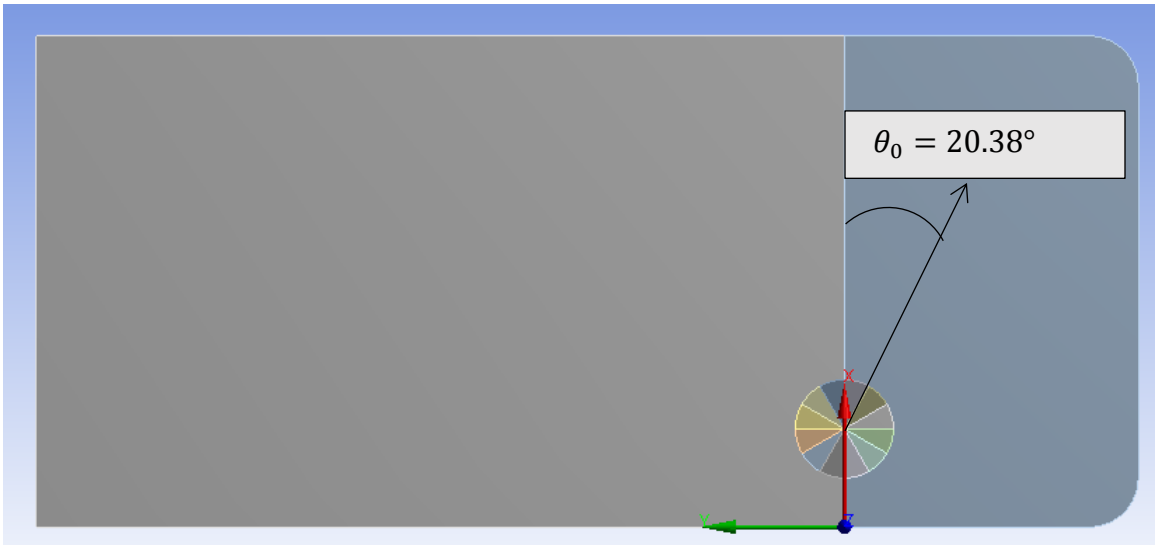


Fig 3.3: Crack Deflection from FE model.

3.4 FE Modeling Methodology

1) Base line case: solder joint height is minimal and foot print is according to the guidelines set by MLCC manufacturers. Find the cracking angle using maximum tangential stress criteria.
2) Change the solder amount (bulbous, shrunk, and straight) and find the crack angle and J integral.
3) Change the solder stand-off height: find the crack angle and J integral.
4) Effect of termination material on the developed J integral and the crack deflection angle.

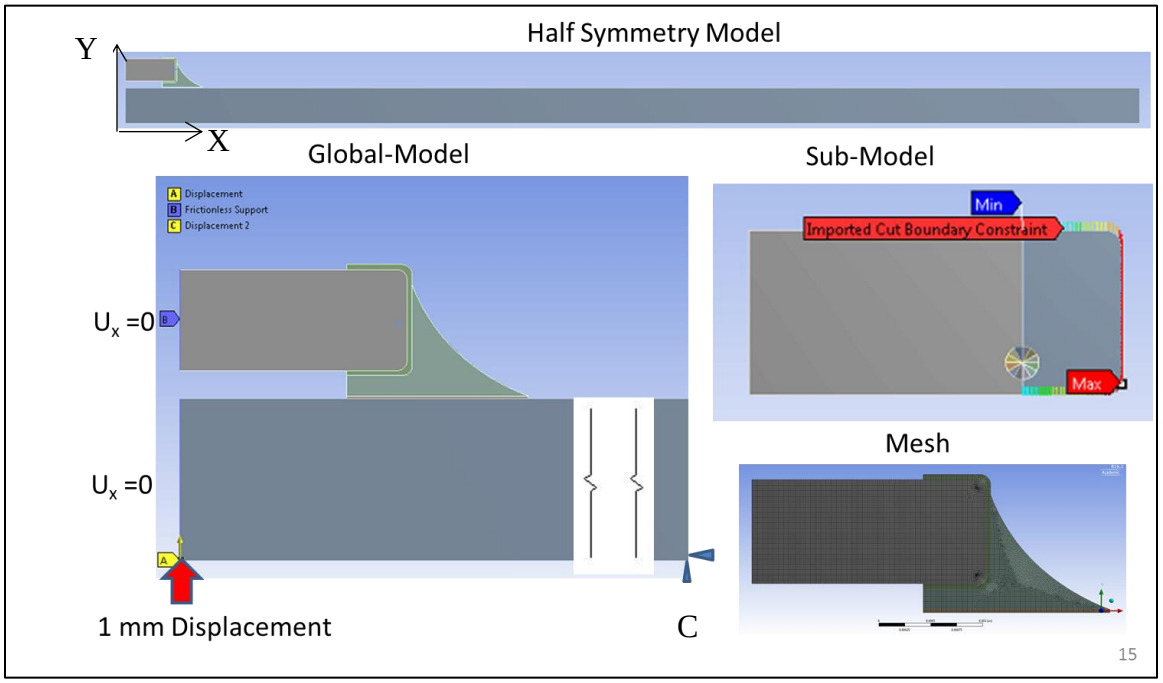


Fig: 3.4: Global Model, Boundary Condition and Sub-modeling in ANSYS Workbench

A 2D half symmetric model has been used to perform the analysis. Symmetry plane has been utilized efficiently to reduce the number of elements in the finite element model (Plane 182, 4node structural solid element). This also helps to get accurate deformation and stresses and reduce the computation time and resources. At the symmetry cutting plane, the normal deformation is constrained (U_x= 0). At the corner of the PCB, the deformation at point C has been constrained in both X and Y direction but the rotation is not fixed. As the capacitor is way smaller than the PCB itself, some measures has to be taken to accommodate the scale difference. Sub-modeling technique has been used in ANSYS workbench to address this issue. PCB, Copper

pads, termination, solder material and the MLCC have been modeled in the global model. The global model simulation has been performed and a cut boundary is specified which includes just the capacitor. The cut boundary displacements have been transferred to the local model. In the local model, a crack has been modeled at the corner of the termination and the capacitor. Local model simulation has been performed to calculate the stress intensity factors and the J integral. Mode I and II stress intensity factors have been used to calculate the crack deflection angle by using equation 3.1.

3.5.1 Impact of Solder joint wetting height on the cracking of MLCC

Surface mounting of the various passive and active components on the printed circuit boards is an important process in the IT product development. Many parameters can be changed to get the optimum solder joint that attaches the component on the PCB. Controlling the flow of solder in the reflow machine can be done to achieve the controlled amount of wetting area of the solder joint. If the solder amount is too high then the all the bending stresses will be transferred to the MLCC. That will enhance the probability of fracture failure in MLCC. In the second case if the solder amount is low then the solder joint itself will not be able to take up the tensile or compressive stress and will be susceptible to cracking. So the optimum amount of solder is very important parameter to ensure the structural integrity of the MLCC and the solder joint.

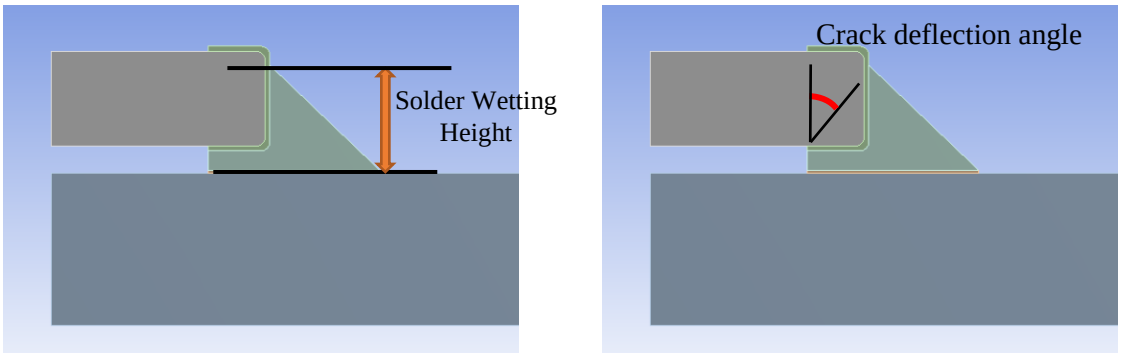


Fig 3.5: Definition of Solder Wetting Height and Crack Deflection Angle.

To find out the optimum amount of solder 1st we try to change the solder wetting height and see the developed J integral and the crack deflection angle. As the height is increased, the J integral around the crack tip is decreasing. As for the crack deflection angle, it is 1st increasing as the

wetting area is increased and then at 0.9 mm solder height is has reached at its maximum value and then further increasing the height would not affect the crack deflection angle.

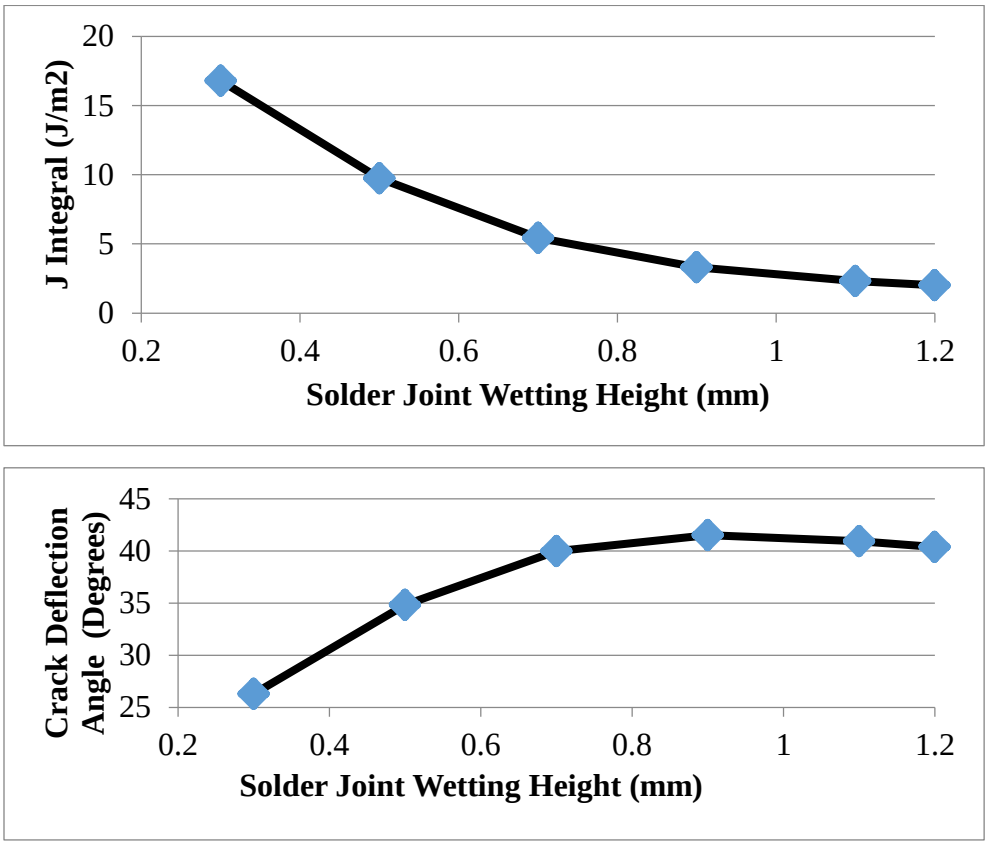


Fig 3.6: Effect of Solder wetting height on the J-integral around the crack tip and the crack deflection angle.

For 0.9 mm height of solder on the Capacitor creates highest crack deflection angle. If the crack deflection angle is more, that will help to save the electrodes being broken. The reliability of the MLCC will be enhanced if lower number of electrodes is being cut by the crack originated from the interface of the termination and the capacitor. So the more crack deflection angle is, the less probability of failure it will produce.

3.5.2 Impact of Solder joint Stand-off height on the cracking of MLCC

The stand-off height is the vertical distance of the capacitor bottom plane from the Copper pad on the printed circuit board. As the height is increased in the FE model the bending stress is more on the capacitor. Because the critical point at the termination-capacitor interface is at a higher

distance from the neutral axis of bending. This will eventually enhance the stress concentration effect the critical corner. For the increased stress concentration the ceramic material will try to break the crack will propagate along the direction perpendicular to the direction where the hoop stress turns out to be highest.

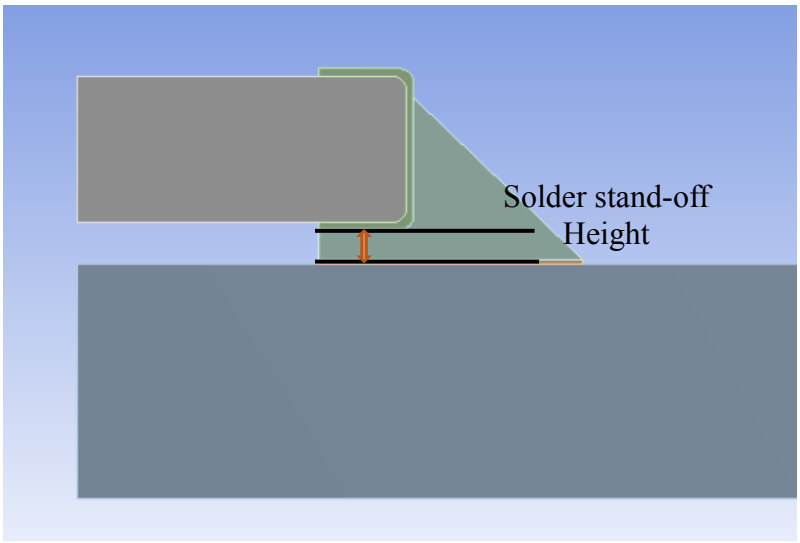


Fig 3.7: Definition of Solder Stand-off height.

As it can be seen from the FE results in Fig 3.8, as the stand-off height is increased, the J integral is also increased. It means that the crack driving energy is becoming more dominant as the capacitor is joined at a higher position from the PCB using different amount if solder underneath the Capacitor. Also at about 0.35 mm solder joint stand-off height, the crack deflection angle is the lowest. So the electrodes are prone to failure when the solder joint stand-off height is more. So the more solder underneath the capacitor is detrimental towards the crack driving energy and it also lower the crack deflection angle which cut more electrodes. So to increase the crack deflection angle and reducing the J integral lower stand-off height solder can be chosen.

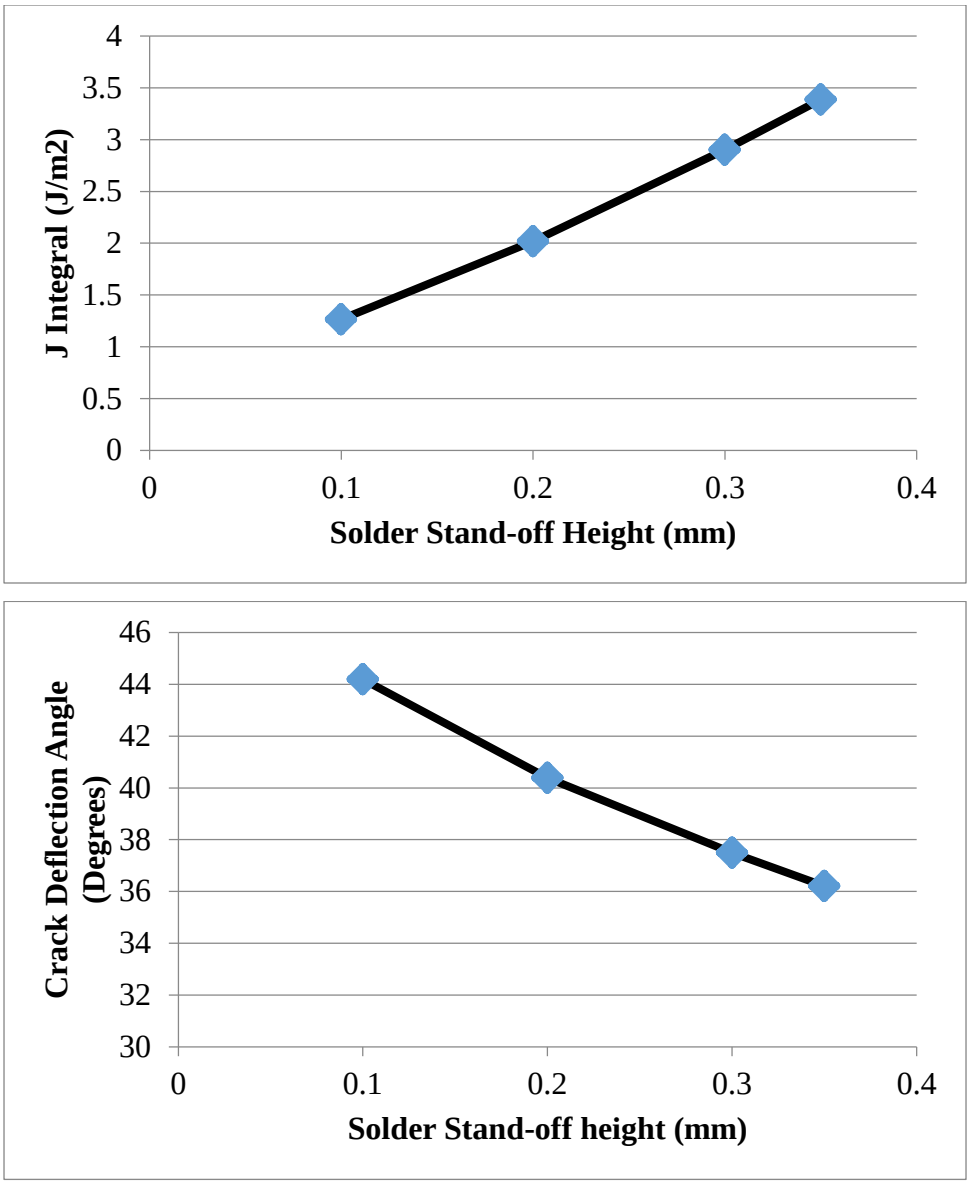
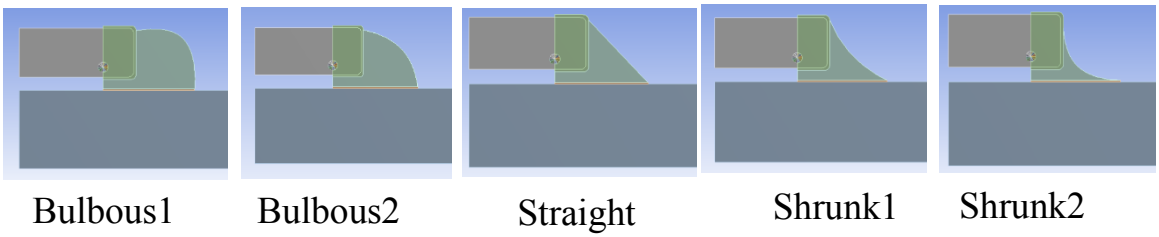


Fig 3.8: Effect of Solder stand-off height on the J-integral around the crack tip and the crack deflection angle.

3.5.3 Impact of Solder joint profile on the cracking of MLCC



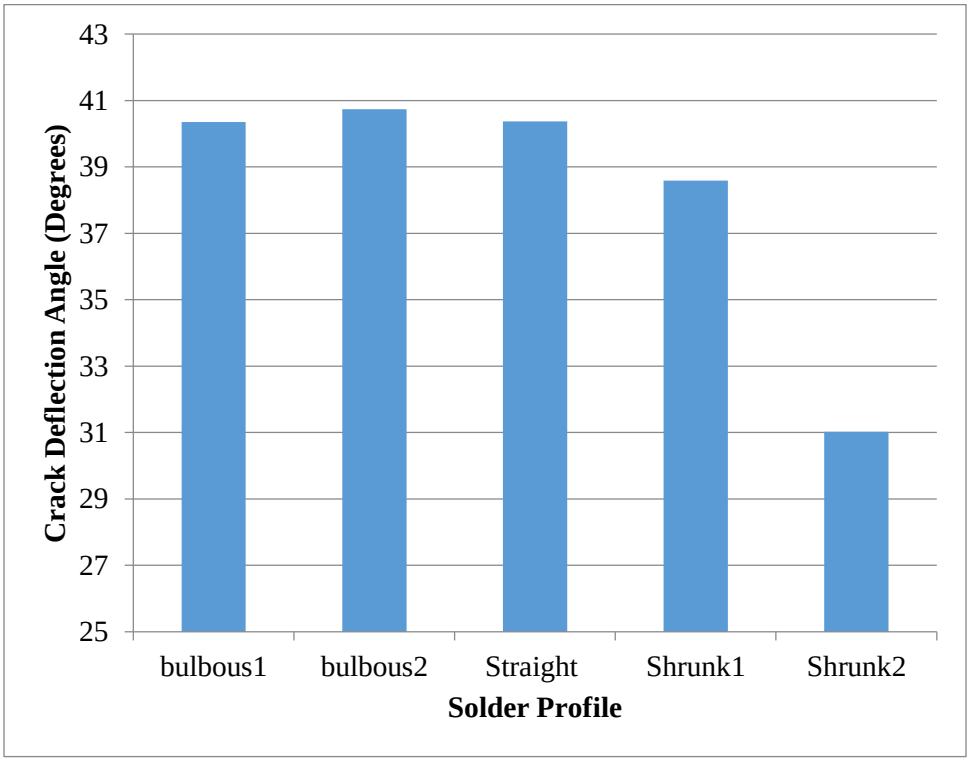


Fig 3.9: Effect of Solder Profile on the J-integral around the crack tip and the crack deflection angle.

Slight changes in the crack initiation and propagation angle can result in big impact on the number of broken electrodes inside the MLCC. So if cracking angle is increased then the number of electrodes being cut by the crack is also decreased as the crack is now propagating at a lower area then before. Amount of solder material can be controlled by the reflow parameters. So if the solder amount can be more or less there will be variation in the board level loading being applied and transferred to the MLCC through the solder material. For the case of bulbous 1 solder joint

the solder amount is the highest. So when the MLCC/PCB assembly is subjected to loading, the big chunk of solder joint will carry the bending load and save the capacitor form breaking. This enhances the MLCC reliability. In case of straight solder the solder amount is less than the bulbous solder but as the angle at which solder material is reaching on the surface of the termination material is sharp it will cause higher stresses to be developed at that spot. In case of shrunk solder amount the solder joint itself is weak when the MLCC/PCB assembly is subjected to bending loading. In this case the solder joint will be broken and there won't be any electrical connection between the device and the PCB. When designing for optimum solder profile one has to keep in mind that the solder amount must be strong enough to sustain the loading and hold the capacitor on the copper pads. And at the same time it takes up or share loads to relieve some part of the applied loading, thus saving the MLCC from stretching up.

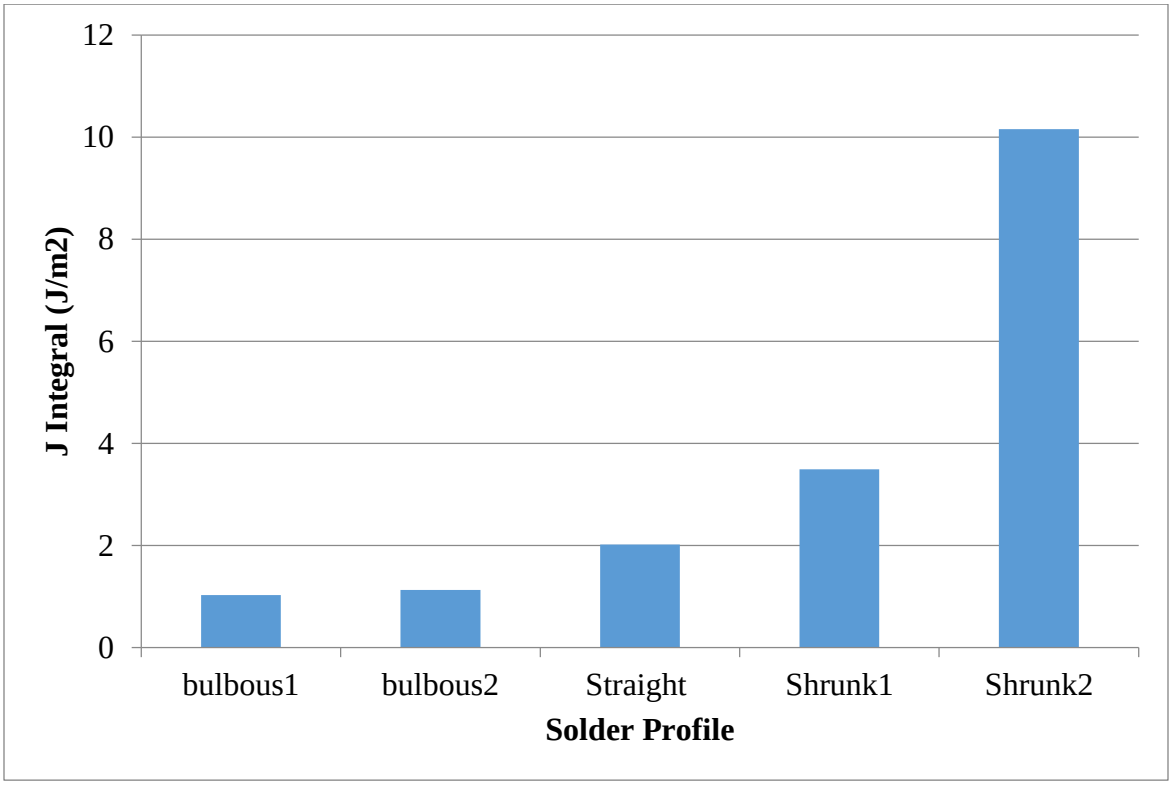


Fig 3.10: Effect of Solder Profile on the J-integral around the crack tip

From Fig 3.9, it is evident that the crack deflection angle is significantly increased when the solder amount is not starved. So by controlling the solder amount the crack deflection angle can be increased and that will also reduce the number of electrodes being cut by the crack, which reduces the loss of capacitance. From Fig 3.10, it is observed that increasing the solder amount

also suppresses the crack driving energy. The J integral is also decreased because the bulky solder joint can take up more load and deformation saving the capacitor from more stress. This will reduce the J integral developed at the crack tip. So over all, solder profile has positive role on the crack deflection and the developed J integral in the capacitor.

3.5.4 Impact of termination material on the cracking of MLCC

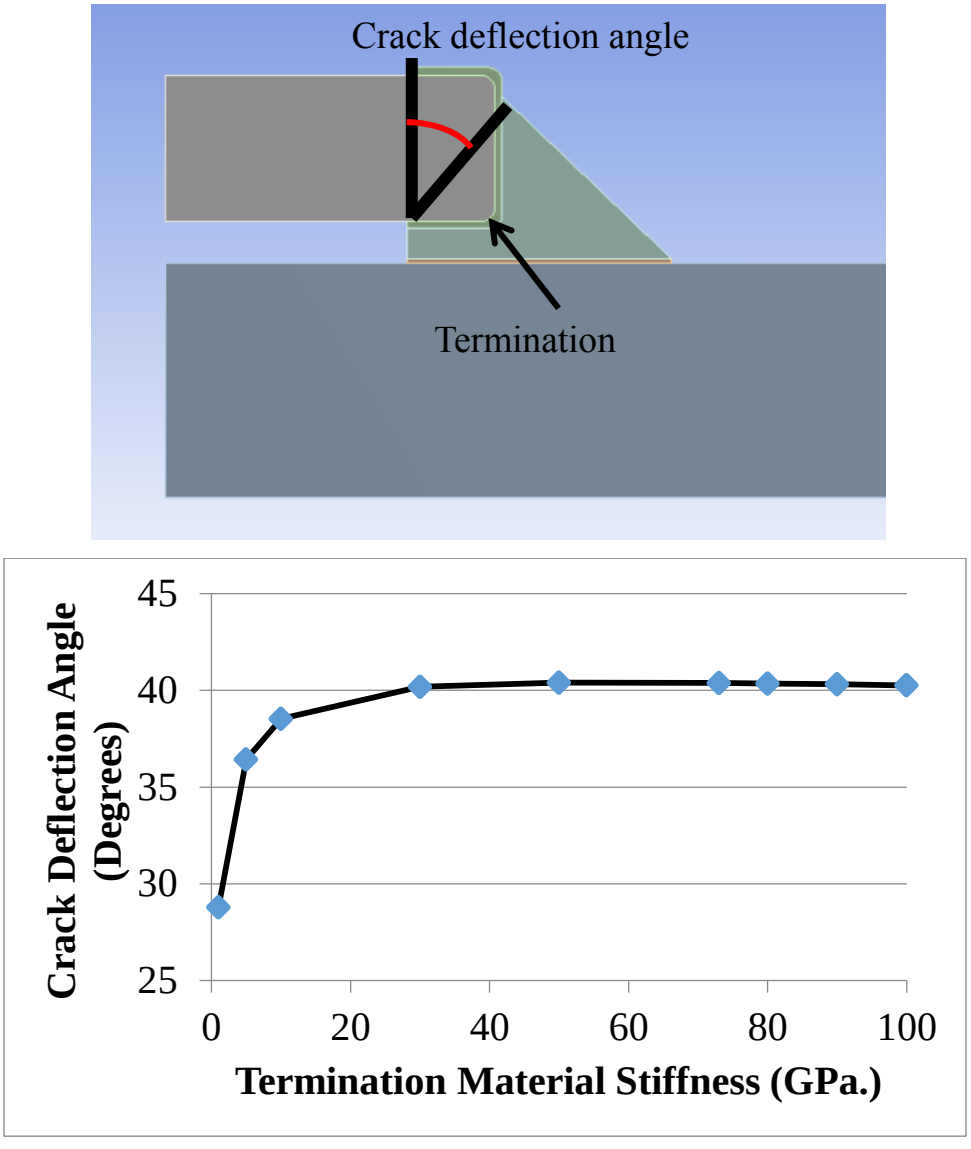


Fig: 3.11: Effect of termination material stiffness on the crack deflection angle

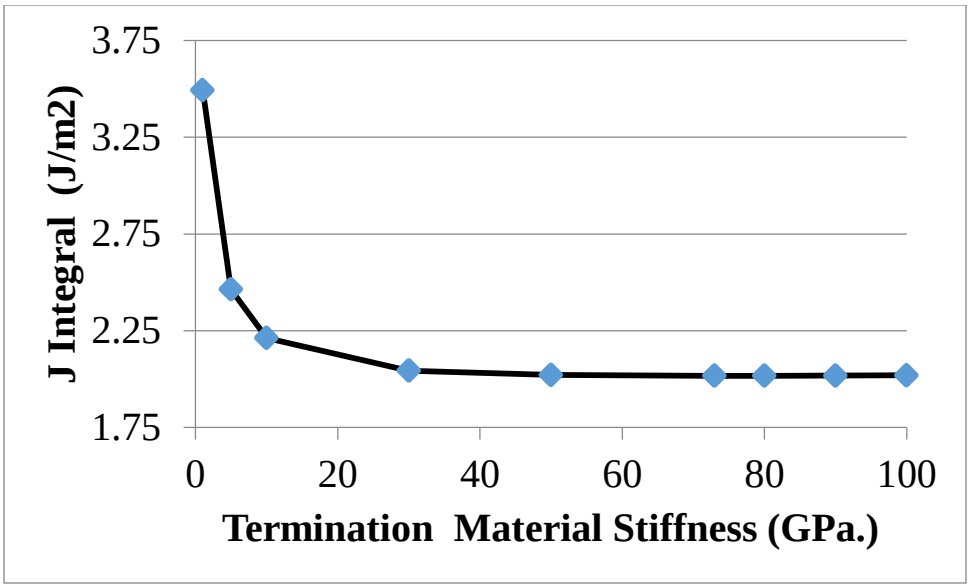


Fig: 3.12: Effect of termination material stiffness on the J integral developed in the capacitor.

Stiffer termination material can be used to increase the crack deflection angle and reducing the J integral in the capacitor. Stiffer termination can take up more loads and deform less, thus saving the capacitor from stress concentration at the critical tip. The stiffer termination is increasing the shear stress ahead of the crack tip. So the crack angle is increasing.

3.5.5 Effect of Termination End on the Cracking of MLCC

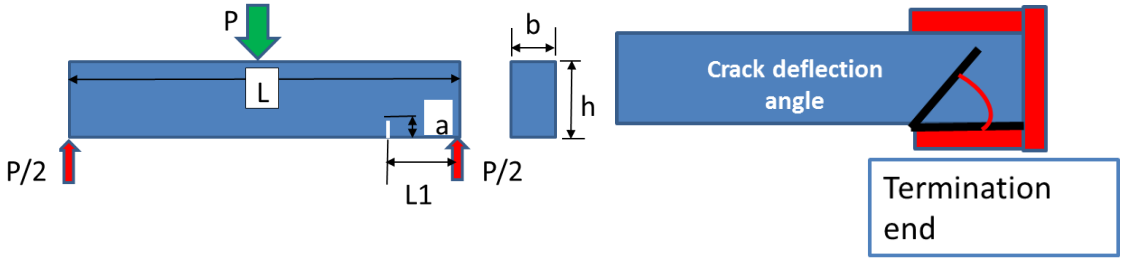


Fig 3.13: Analytical model to analyze the effect of termination end on the crack angle.

If it is assumed that the capacitor has been simply supported at the two surface mounted ends and load P has been applied on the top surface then the above boundary condition can be applied on the capacitor. The normal and shear components of the stress for simply supported beam can be used to calculate the angle of crack propagation. If we can calculate the stress distribution at the

crack tip due to bending then we can use the normal and shear stress at that point. These stress components can be used to determine the maximum principal stress direction. The crack will propagate at an angle perpendicular to the maximum tangential stress.

- $\sigma_x = \frac{MC}{I}$
- $\sigma_x = \frac{\frac{P}{2} \times L_1 \times \frac{h}{2}}{\frac{1}{12} bh^3}$
- $\sigma_x = \frac{3PL_1}{bh^2}$
- $\tau_{xy} = \frac{VQ}{It}$
- $\tau_{xy} = \frac{\frac{-P}{2} \times Q}{\frac{1}{12} \times bh^3 \times b}$

- Now, $Q = \frac{1}{2} \times (\frac{h^2}{4} - y^2) \times b$
- Here, $y = (\frac{h}{2} - a)$
- Now w, $Q = \frac{ab}{2} \times (h - a)$
- So, $\tau_{xy} = \frac{-3Pa(h-a)}{bh^3}$
- Now $\tan(2\theta_p) = \frac{2 \times \tau_{xy}}{(\sigma_x - \sigma_y)}$
- $\theta_p = \frac{1}{2} \tan^{-1} \left\{ \frac{2a(a-h)}{hL_1} \right\}$
- So for a fixed capacitor model h is fixed and θ_p= f(L_1)

For h=1, a=0.1 and L=4.5 we get the following results:

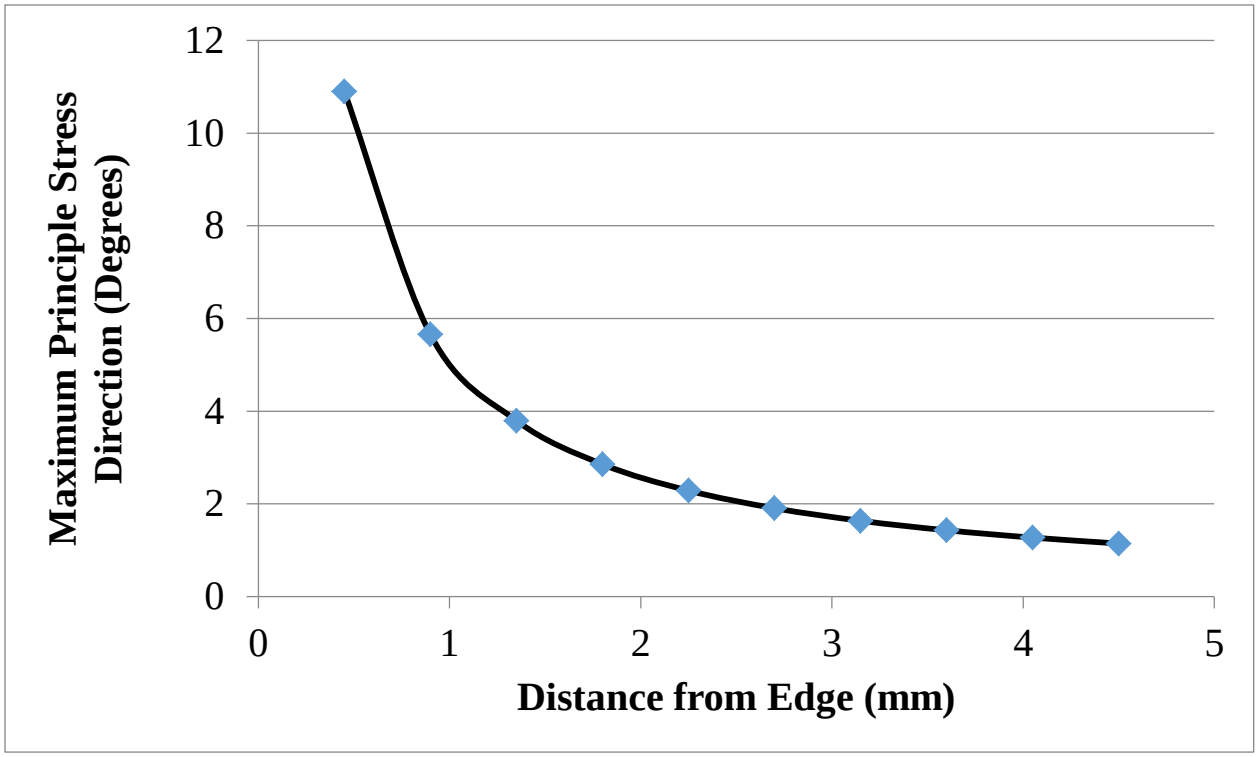


Fig 3.14: Effect of termination end on the maximum principal stress direction.

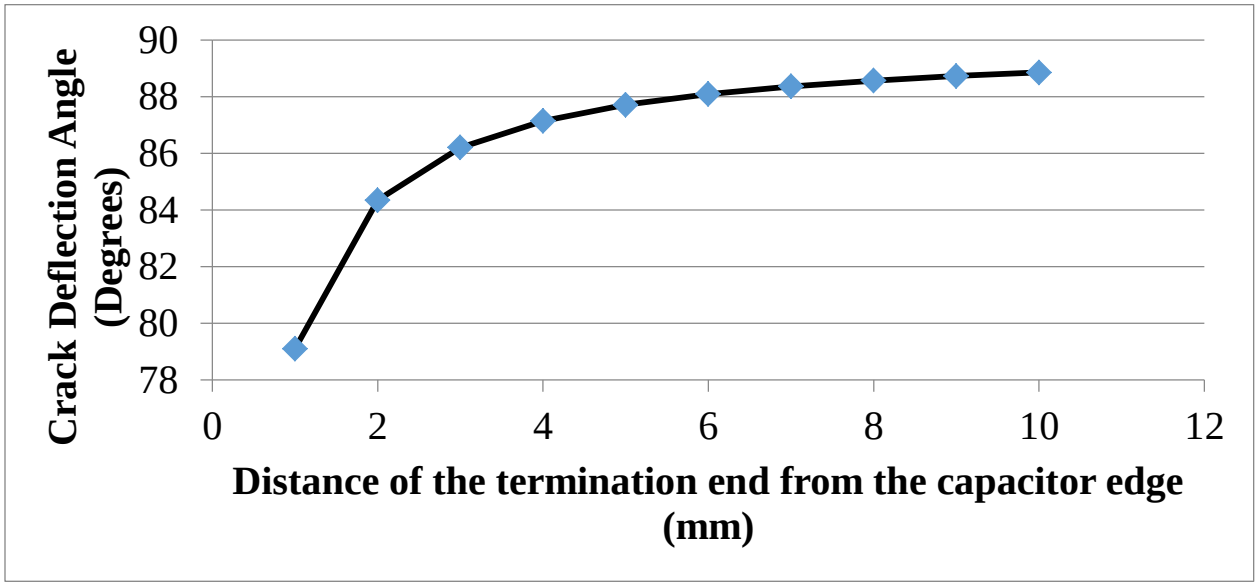


Fig: 3.15: Effect of termination end position on the crack deflection angle.

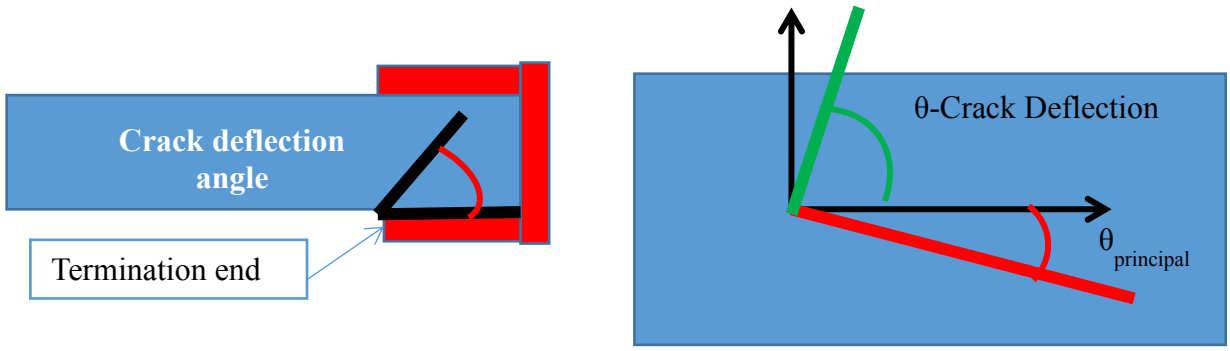


Fig 3.16: Crack deflection angle and the maximum principal stress direction

Crack deflection angle is dictated by the principal stress angle. Crack will propagate at an angle perpendicular to the direction of the maximum principal stress. And it is highly dependent on the stress concentration point which is also determined by the termination end. So the termination end can be changed such that the crack will propagate at an angle that cuts lower amount of electrode in the MLCC. From fig 3.15, it is observed that as the position of the stress concentration point is moving from the capacitor edge, the crack deflection angle is increasing. So for achieving lower crack deflection angle we can design the termination end such that it is very close to the capacitor edge.

3.6 Mesh Sensitivity Analysis:

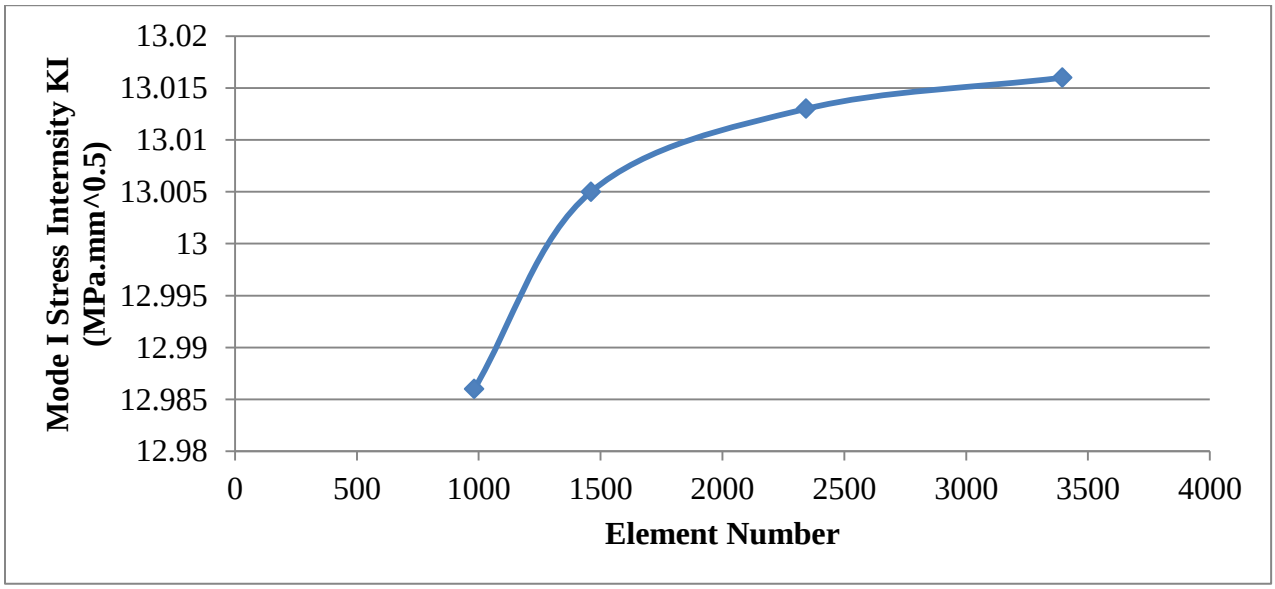


Fig 1: Effect of element number on the Mode I Stress intensity factor.

The element number ahead of crack tip has been varied to see at which mesh the results are independent of the mesh size. From the above figure it can be observed that the stress intensity factor reaches almost constant value after 2500 elements. All the subsequent simulations have been performed using this mesh to get consistent results.

3.7 Conclusion

A holistic investigation has been done on the behavior of MLCC subjected to PCB static mechanical bending. PCB is subjected to mechanical bending load due to various operational and manufacturing processes, such as installing and surface mounting other components, shipping, depaneling, installing slots on the PCBs. A 2D finite element model has been used for analyzing the deformations and stresses in the MLCC when the MLCC/PCB assembly is subjected to bending. Crack propagation angle, stress, intensity factors developed at the crack tip has been analyzed. Various design parameters such as solder joint profile: bulbous, shrunk, straight and optimum; solder joint wetting and stand-off height; can be tailored such that the developed stress intensity factor and crack propagation are less. This will help to mitigate the reduction of capacitance due to the electrodes being cut by the crack. From this study it is showed that the crack deflection can be increased by increasing the solder amount and the solder wetting height. Solder joint stand-off height has detrimental effect on both the J –integral and the crack deflection angle.

Chapter 4

Thermo-Mechanical Reliability of Multi-Layered Ceramic Capacitor (MLCC) Solder Joint and Device Using Finite Element Analysis

4.1 Introduction:

This is an era of multifunctional electronics products enabling a new horizon of human experience. Almost every year many new products with thinner profile, better performance and wider functionality have been revealed to customers. The reliability of each of these electronics have never been a important as they are used for personal communication, entertainment, healthcare, automotive ECUs, home security, military and various other applications. Multilayered Ceramic Capacitors (MLCC) are one of the most widely used components on a printed circuit boards (PCB) as they serve to reduce noise in the input signal, maintain stable input outputs. Their performance is really crucial for reliable operation of these sophisticated micro-electronic systems. There have been rapid increases in the number of MLCCs used in electronic devices. About 730 units are used in today's notebook computers; about 230 units are present in the cellphone. Large systems like digital TVs have almost 1000 units of ceramic capacitors in them. Thermo-mechanical reliability estimation is one of the most important steps in MLCC product development to make sure that the product will not fail before an expected period. MLCC and PCB assembly mainly has two critical areas of failure: MLCC solder joint failure and the ceramic component cracking due to successive PCB bending when subjected to accelerated thermal cycling.

Cracks form in the ceramic component at the corner of termination material and the ceramic block. It eventually propagates in the brittle ceramic material and cut metal electrodes into two parts creating electrical disconnection thereby reducing operating capacitance of MLCC. Due to the coefficient of thermal expansion mismatch between the PCB and MLCC, the solder joint that connect the two components, would be subjected to thermal stress during accelerated thermal cycling. MLCC block is brittle and cracks will form, initiate due to the bending of the PCB/MLCC assembly.

4.2 Mechanics of Thermo-mechanical loading

During the solder reflow process of the active and passive components solder joints are formed and the solder profile plays an important role in the thermo-mechanical reliability of these devices. In this study a Finite Element Analysis is used to identify the impact of solder joint profile and solder joint stand-off height on the fatigue life of solder joint and developed stress intensity factors in the ceramic capacitor. Thermal cycling analysis is done in global model whereas fracture analysis is done using sub-modeling technique and the prevalent mode of facture and the cracking path have been identified. This study predicts the in-elastic strain energy density in solder joint life and critical areas in solder joint that can fail during thermal cycling. Interfaces between the MLCC terminations, solder fillet region and PCB pad has been analyzed as they are the critical region for failure. At each interface a 25 micron solder layer has been considered for failure prediction and the developed in-elastic strain energy density in that layer is taken as a parameter to quantify crack initiation and propagation. Four solder joint profiles have been considered in this study: shrunk, bulbous, optimum and straight for identifying the most favorable solder joint profile that can reduce the probability of failure in the MLCC device and also in the solder joint during thermal cycling. The impact of solder stand-off height is also analyzed using the finite element method. The solder joint stand-off height will change the in-plane stress distribution due to bending as the bending rigidity will change for different stand-off heights. An optimum stand-off height will help to reduce the bending stress and thereby reducing the developed plastic work in solder joint and stress intensity factors in the Multi-layer ceramic capacitor. Sub-modeling technique has been leveraged to quantify the stress intensity factors and identify prevalent modes of cracking in the capacitors. It has been observed that the solder profile has significant effect on the solder joint reliability of MLCC device. The stand-off height has less effect on the plastic work developed in the solder joints in top, side, bottom solder layer.

4.3 Finite Element Modeling Methodology

In this study impact of various soldering parameters has been analyzed to see what type of solder joint will reduce the cracking in the MLCC and increase the fatigue life of the solder joint. Solder joint stand-off height and the profile of the solder joint, the wetting angle of the solder joint will affect the amount of solder that is being used for attaching the MLCC onto the PCB.

Solder material has time dependent material properties and it creeps at room and higher temperature. So eventually solder mass will have an impact on the developed stress inside the MLCC block. If the solder amount is too much then it is expected that solder joint will be stiff and transfer all the stress to the adjacent MLCC block, increasing the probability of higher stress concentration in ceramic capacitor. Whereas if the solder joint is too starved or shrunk then the solder joint itself will break due to repetitive thermal fatigue. The impact of optimum amount of solder joint has two effects: it will balance the stress transfer to capacitor and would be strong enough to increase the thermo-mechanical fatigue life of the solder joint. A Finite Element (FE) model of capacitor, solder and PCB assembly has been generated in commercial FE code ANSYS 16.0 [7]. The profile of the solder joints used in this study are namely: bulbous, straight, shrunk. The solder joint stand-off height was also varied to see the impact on the thermo-mechanical fatigue life of the solder joint and developed stresses in the capacitor. Three interface areas in the solder joint were chosen for estimating the plastic work as the interfaces are prone to cracking in multi-material system. . Sub-modeling technique was used to explore the developed stress intensity factors ahead of a 3D semi-elliptical crack front. The impact of solder profile and stand-off height parameters on the developed stress intensity factors in capacitor has been analyzed.

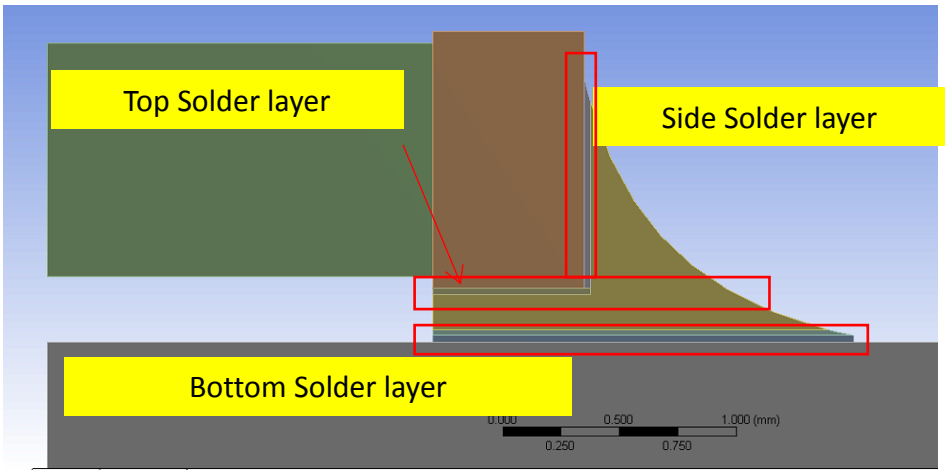


Fig 4.1: Three critical interfaces solder layer for estimating solder plastic work

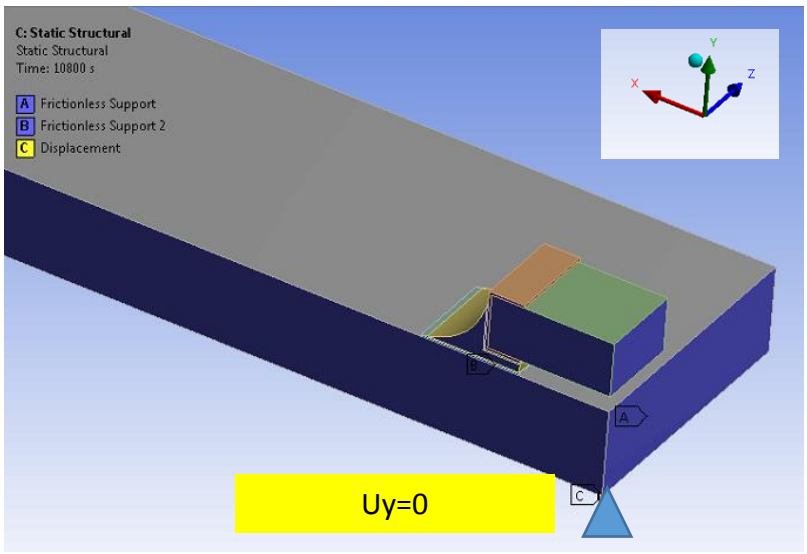


Fig 4.2: Symmetry Boundary Condition for the quarter model and Uy= 0 for preventing rigid body motion.

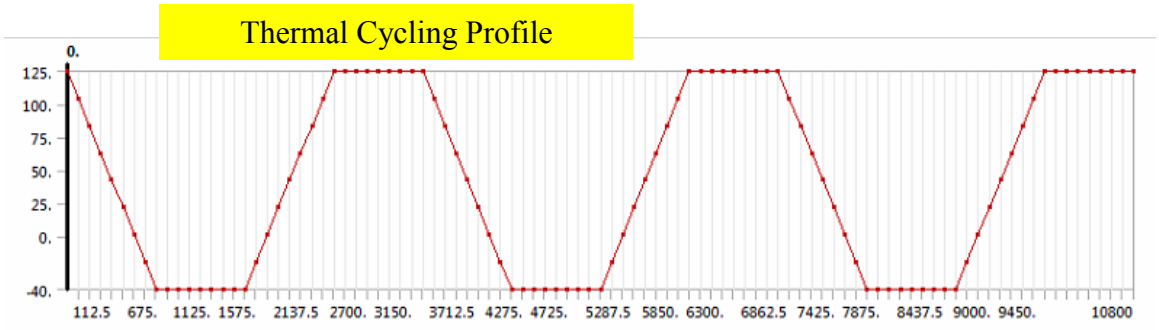


Fig 4.3: Thermal Cycling Profile

4.4 Sub-modeling technique for implementing Fracture Mechanics based study:

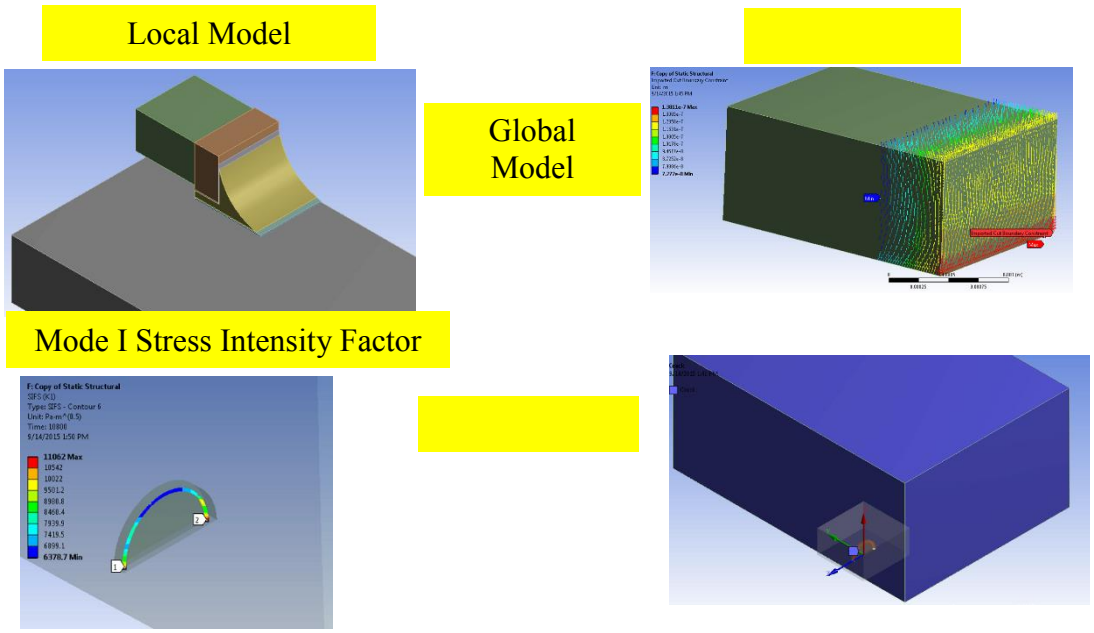


Fig 4.4: Sub-modeling technique to estimate the stress-intensity-factors.

As the capacitor is smaller than the PCB, so to capture the deformation and stresses correctly in the system a global-local modeling methodology has been used. In the global model the PCB/MLCC assembly has been subjected to -40C to 125 C temperature cycling condition. After the global simulation has been completed, a local simulation was setup such that the stresses and fracture mechanics parameters at the crack tip of the capacitor are analyzed with computational accuracy. A cut boundary was defined in the global model for the capacitor. The global time dependent displacements, around that cut boundary has been transferred to the local model. In the local submodel, a detail fracture mechanics analysis has been done by creating a penny shaped 3D crack at the stress concentration region.

4.5 Impact of Solder Profile on the developed In-elastic Strain Energy Density (MJ/m^3) in solder

Top Solder layer	0.125	0.133	0.129
Bottom solder Layer	0.046	0.046	0.044
Side Solder Layer	0.128	0.164	0.146

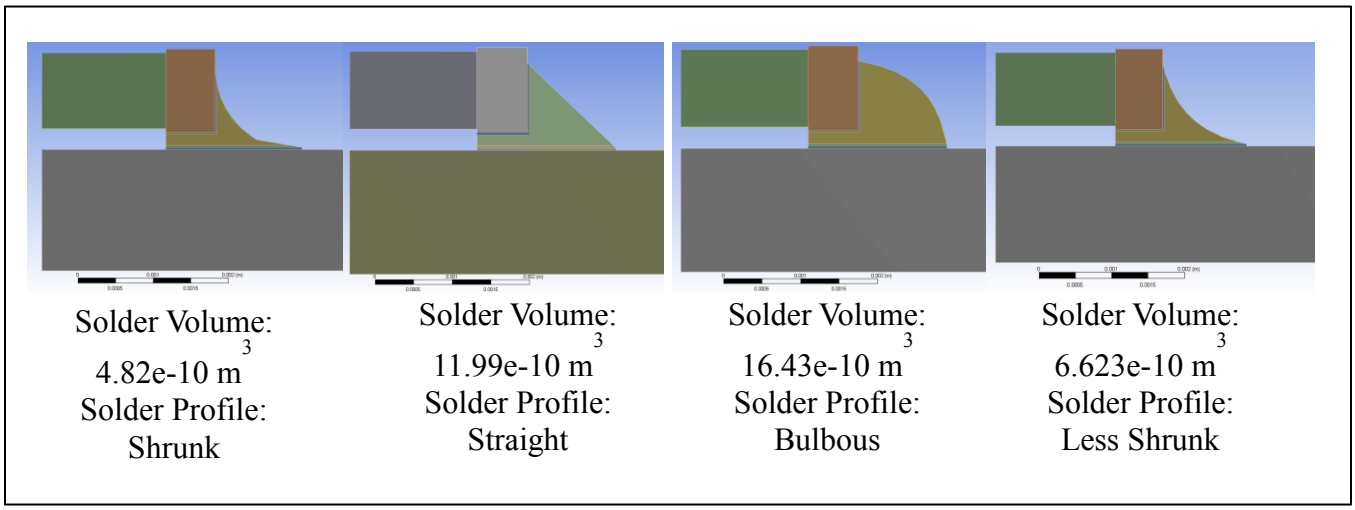
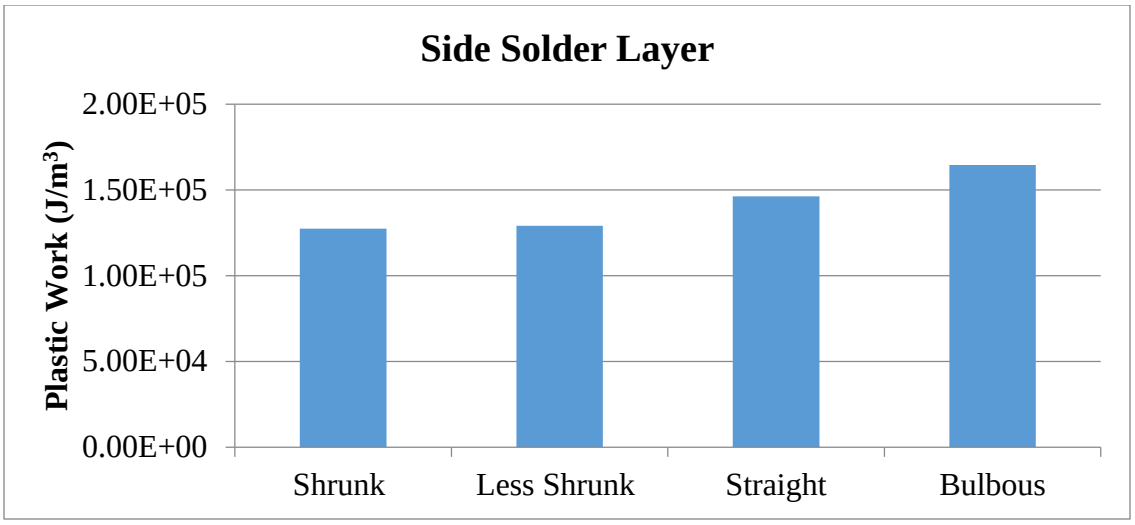
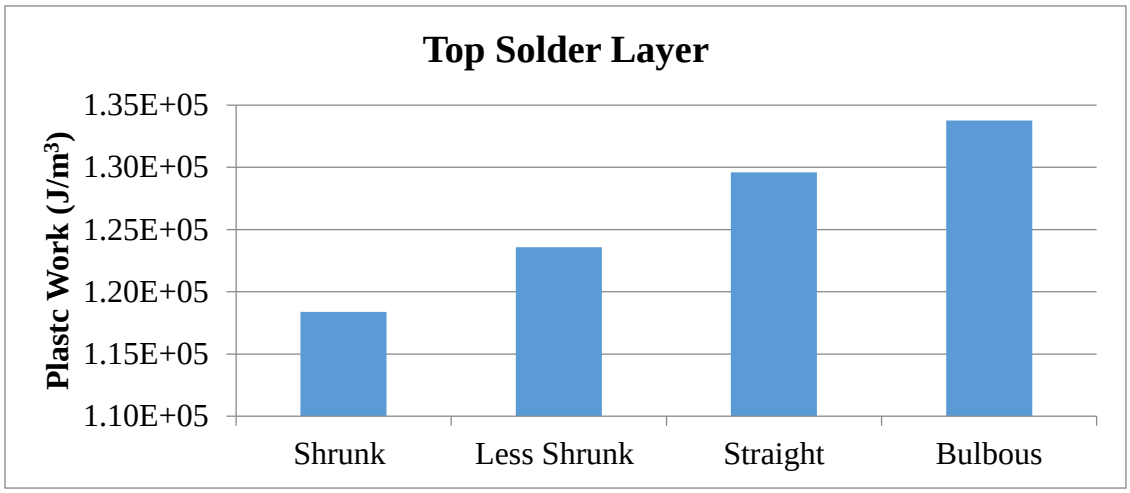


Fig 4.5: Solder volume of different solder joint profile


Side Solder Layer
Plastic Work (J/m3)
2.00E+05
1.50E+05
1.00E+05
5.00E+04
0.00E+00
Shrunk
Less Shrunk
Straight
Bulbous


Top Solder Layer
Plastc Work (J/m3)
1.35E+05
1.30E+05
1.25E+05
1.20E+05
1.15E+05
1.10E+05
Shrunk
Less Shrunk
Straight
Bulbous

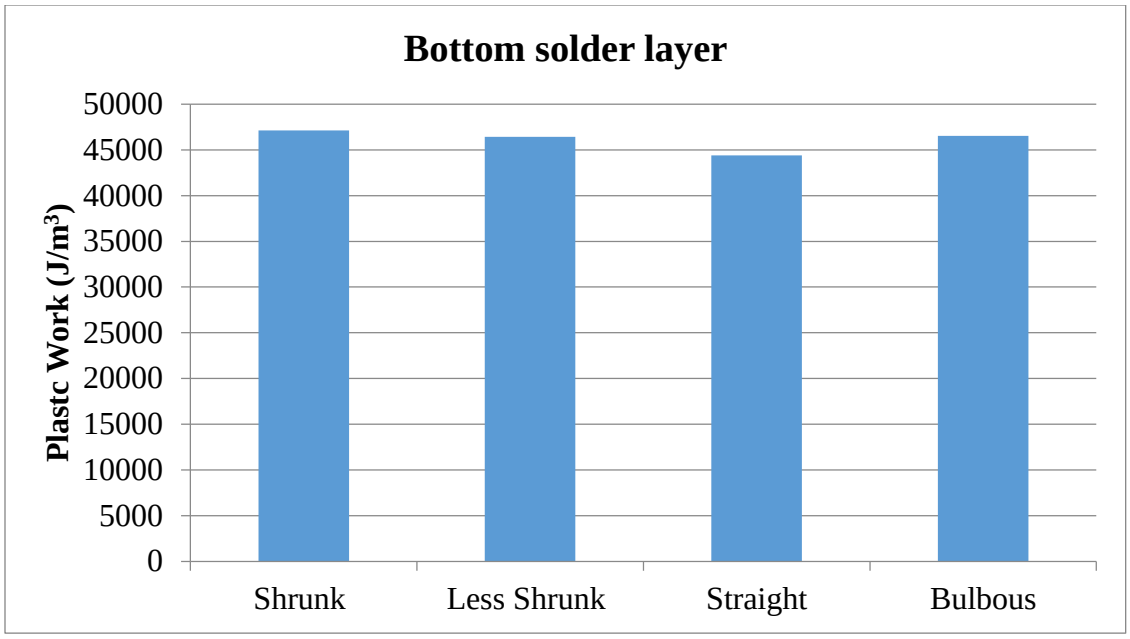


Fig 4.6: Plastic work variation in the three critical layers (a) Side, (b) Top (c) Bottom for different solder profiles.

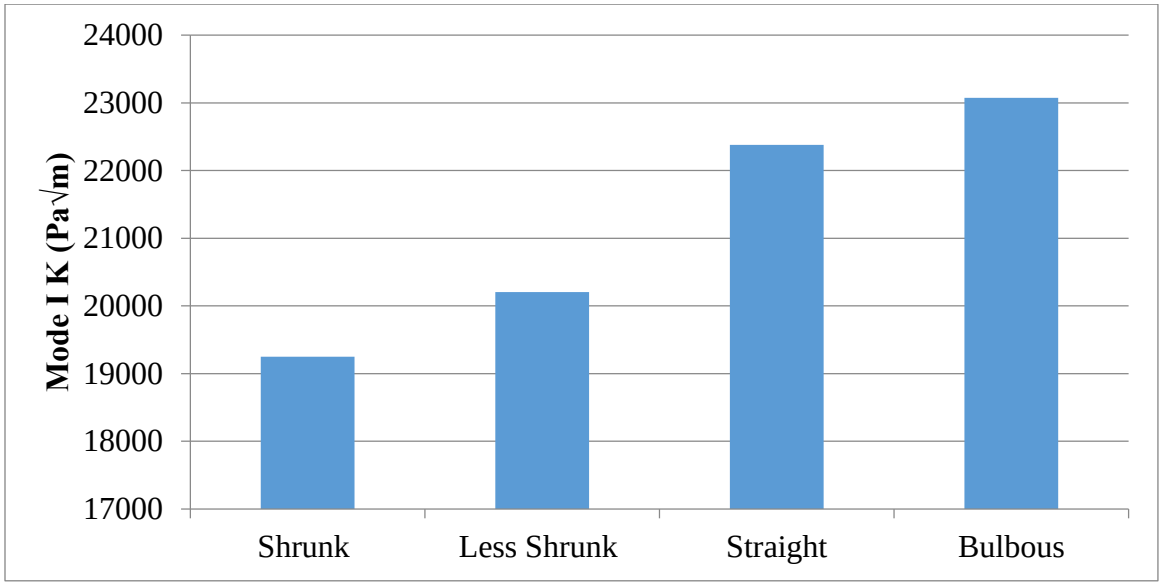


Fig 4.7: Mode I stress intensity factor variation due to different solder profile

4.6 Impact of PCB materials on the thermomechanical reliability of MLCC solder joint and device

a) Effect of PCB thickness:

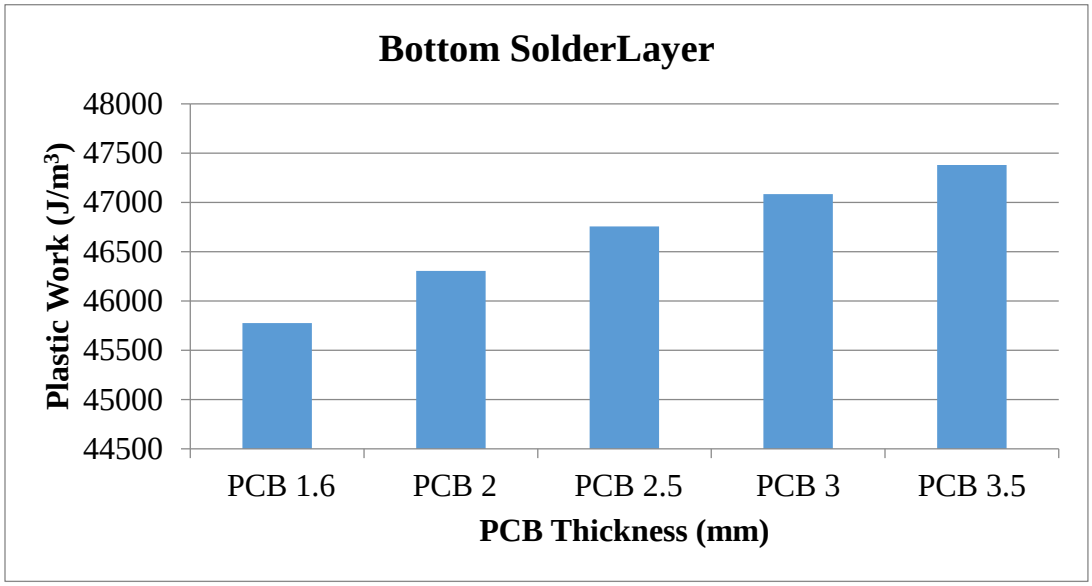


Fig 4.8a: Effect of PCB thickness on the bottom solder layer Plastic Work.

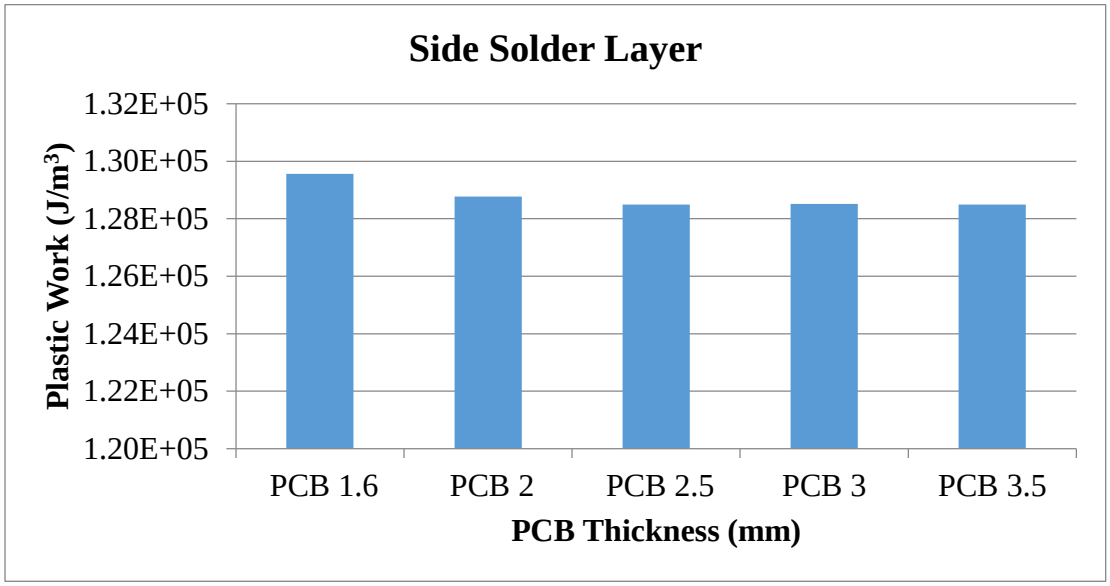


Fig 4.8b: Effect of PCB thickness on the side solder layer Plastic Work.

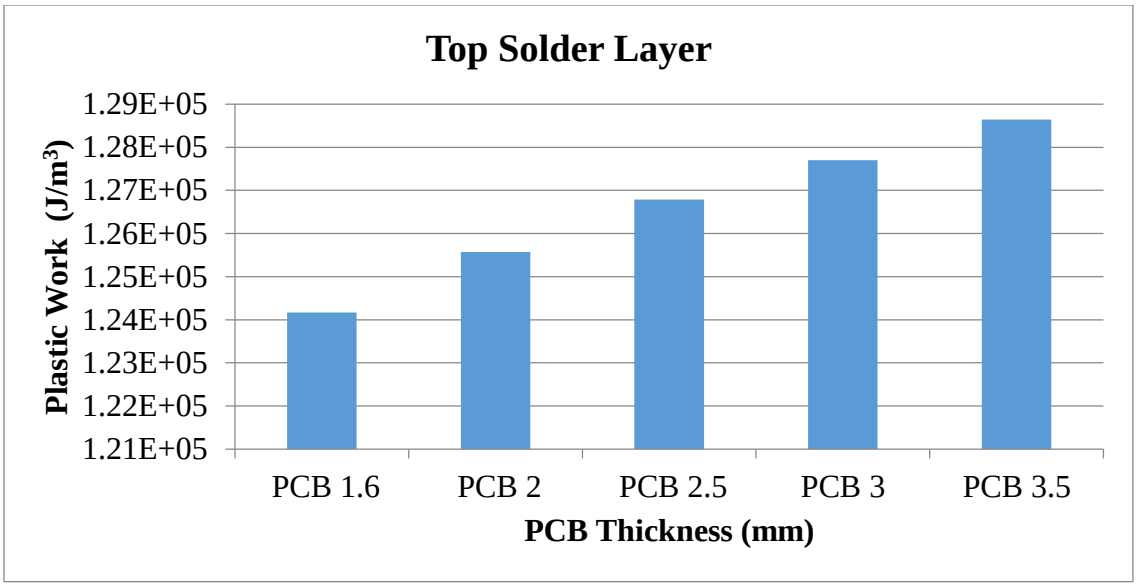


Fig 4.8c: Effect of PCB thickness on the top solder layer Plastic Work.

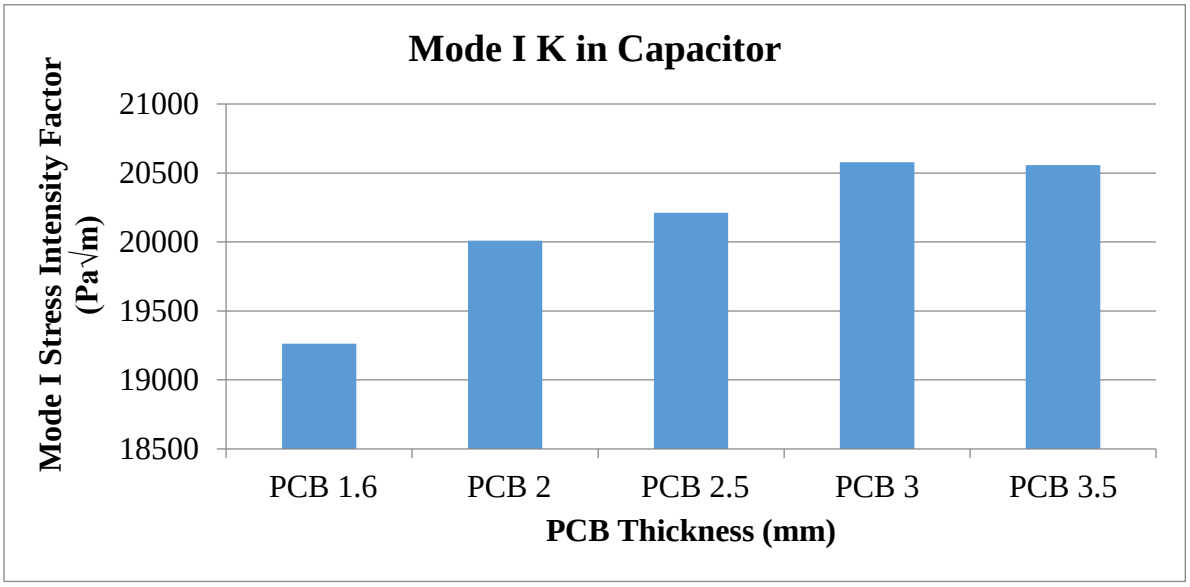
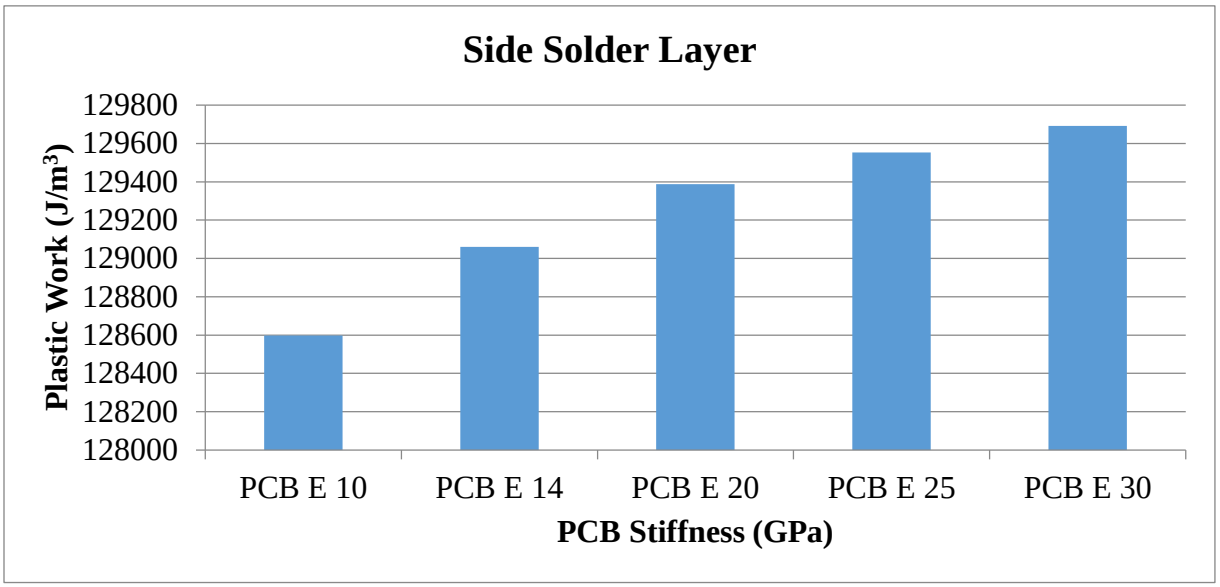
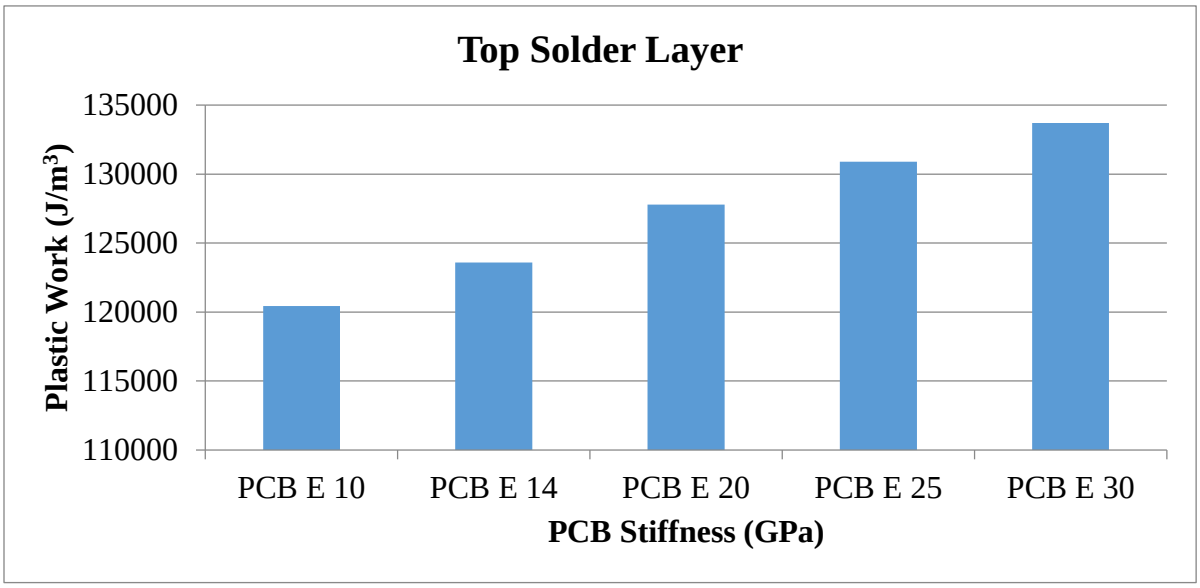


Fig 4.9 Effect of PCB thickness on the mode I stress intensity factor developed inside the capacitor

b) Effect of PCB Stiffness :





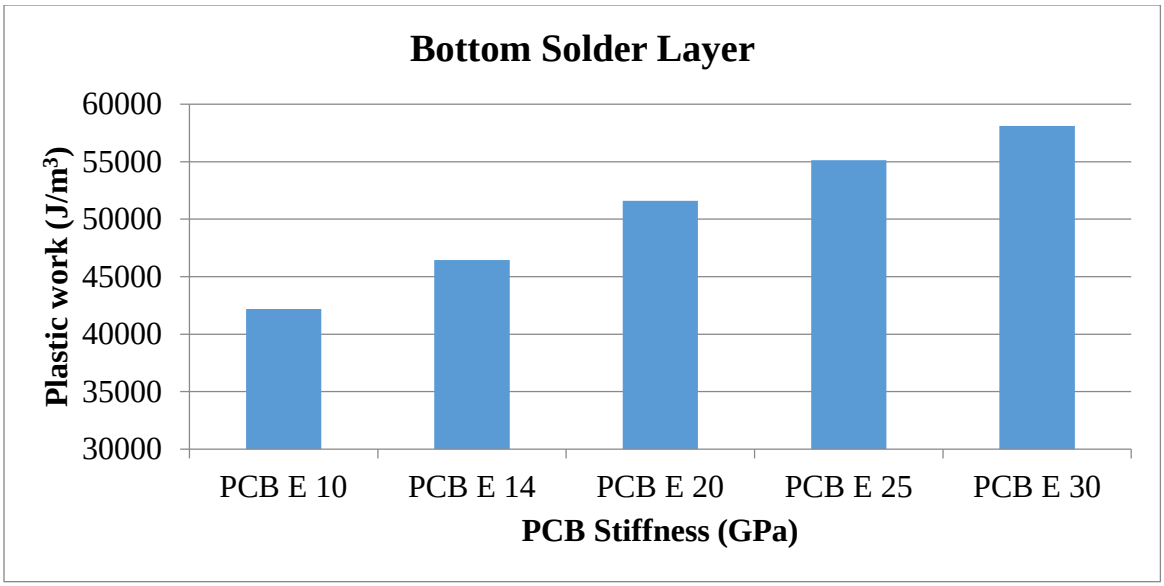


Fig 4.10: Plastic work variation in the three critical layers (a) Side, (b) Top (c) Bottom for different solder profiles.

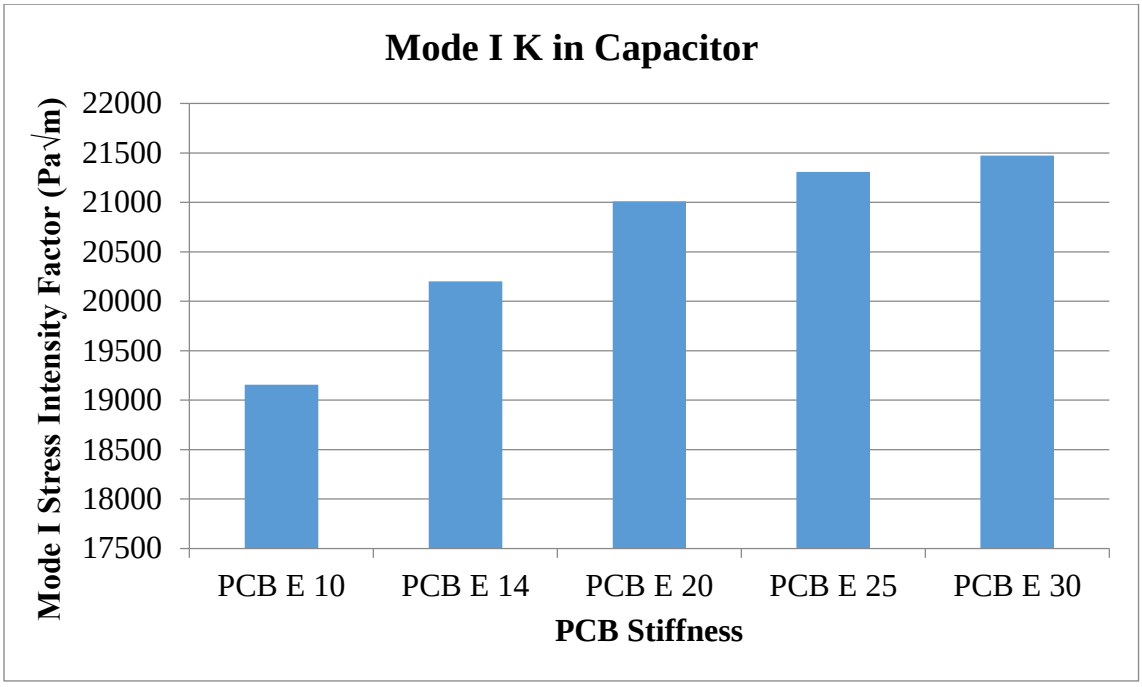


Fig 4.11: Effect of PCB stiffness on the mode I stress intensity factor developed inside the capacitor.

4.7 Conclusion

All the new microelectronic devices have to pass the certain number of thermal cycling tests before it can be qualified as a product. From this study it has been shown that the board level solder joint reliability of the MLCC device can be improved by careful choice of the solder joint profile and PCB materials. These parameters have significant effect on dictating the fatigue life of solder joint and the cracking of the capacitor during thermal cycles. Lower stiff PCB materials can conform to the deformation of the MLCC thus transferring less stress on the capacitor. Thinner PCB materials will also enhance the reliability of the MLCC device and the solder joint. If the application area of the MLCC requires the device to be subjected to higher temperature then starved or shrunk solder joint can be formed to reduce the plastic work in the solder joint and to suppress the crack driving force in the capacitor. So the MLCC design can be altered based on the mechanics of device failure and it has to be established and incorporated in the design rules such that these findings can help to design reliable devices for our gadgets.

Chapter 5

Board Level Drop/Impact reliability of MLCC using Explicit and Implicit Finite Element Method

5.1 Introduction

State of the art mobile and tablet devices are used in many applications from entertainment, healthcare systems to flight data management. These devices are dropped often. This repetitive drops during the typical service life of these devices will initiate mechanical failure in the solder interconnects and in some cases in the device itself. Therefore the estimation of drop/impact reliability is very important analysis for the design teams to make sure the operational life of the device exceeds customer expectation period. Finite Element technique is widely used method for estimating the drop/impact failure life of the solder joint and the component. In this phase of the study two FE simulation methodologies have been used for determining the critical areas of failure in the solder interconnect and the MLCC device. A sub-model is used to estimate the fracture mechanics parameters developed in the MLCC. Stiffness of the PCB is a critical factor during drop events since stiffer PCBs transfer all the loads to the MLCC device. The lay-up of the core layers and outer most layers of the PCB and the thickness of prepreg and conductive layer will play a critical role in determining the bulk PCB stiffness. The solder joint profile, solder wetting height, solder joint stand-off height will be taken as soldering parameters to analyze the effect of them on the device and interconnect stresses.

5.2 Method 1: Free falling of the Capacitor/PCB assembly on the drop table. (Done in ANSYS Explicit Dynamics module)

In this method the entire MLCC/PCB assembly is dropped on a rigid table from a prescribed JEDEC height of 1.5 m. For developing efficient simulation methodology the drop height is kept very small from the rigid table and the terminal velocity is used as an input to the MLCC/PCB assembly. This velocity is calculated from the $V = \sqrt{(2gH)}$, where H is the true drop height. Also for reducing the computational time the number elements has to be reduced and henceforth a quarter symmetric model is used for the drop simulation. Symmetric boundary condition is used on the cut faces of the quarter model for accurately predicting the stresses and strains in the critical areas of the MLCC device and the solder joints.

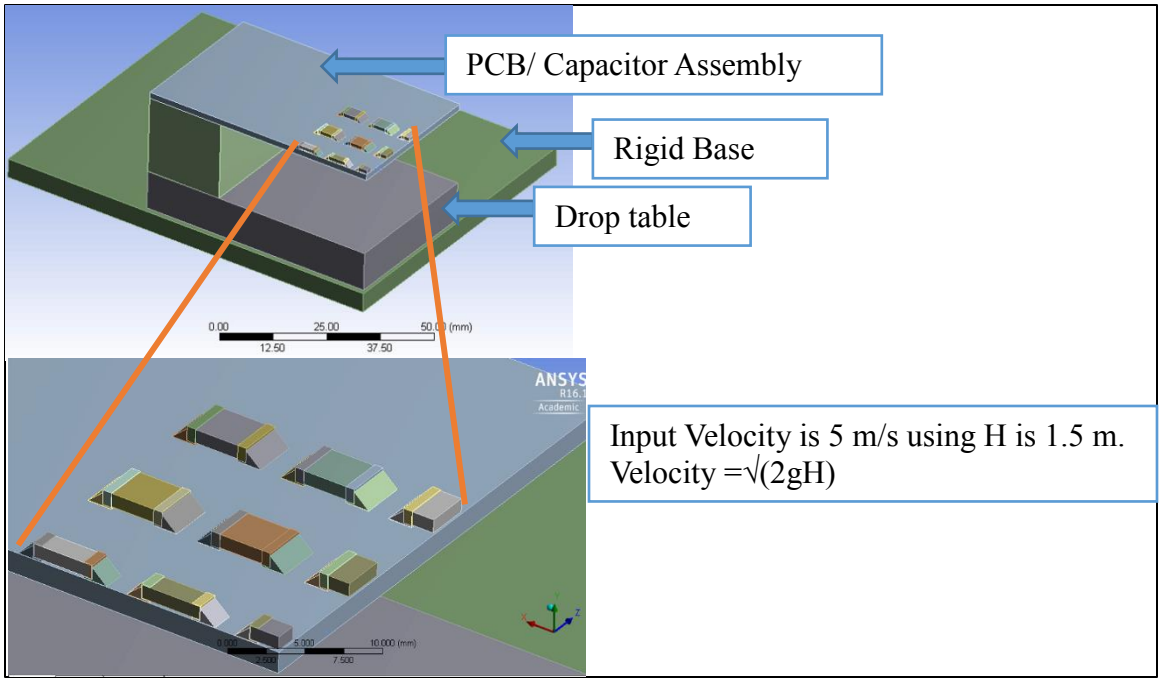


Fig 5.1: Free Fall Method using ANSYS Explicit Dynamics 16 [8]

5.3 Method 2: Acceleration impulse provided as an input to the PCB/Capacitor assembly. (Done in ANSYS Structural Transient Module)

In this method an alternative simulation methodology is used to get the drop response of the MLCC device. In the actual drop event, an acceleration impulse lasting for very few milliseconds, transfer from the rigid base to the MLCC/PCB assembly through the support screws. This acceleration impulse is a half sign wave, A sin ωT, where A is the peak acceleration and the T is the duration of the impulse. In this method, this acceleration is used as an input to the MLCC/PCB assembly and in the support screws nodal DOF will be fixed. Simulation time is specified long enough to capture the behavior of the MLCC device and the solder joint during the input acceleration pulse and after the pulse. In this case the duration of the acceleration is taken as 0.5 ms and the total time of the simulation was taken as 0.75 ms.

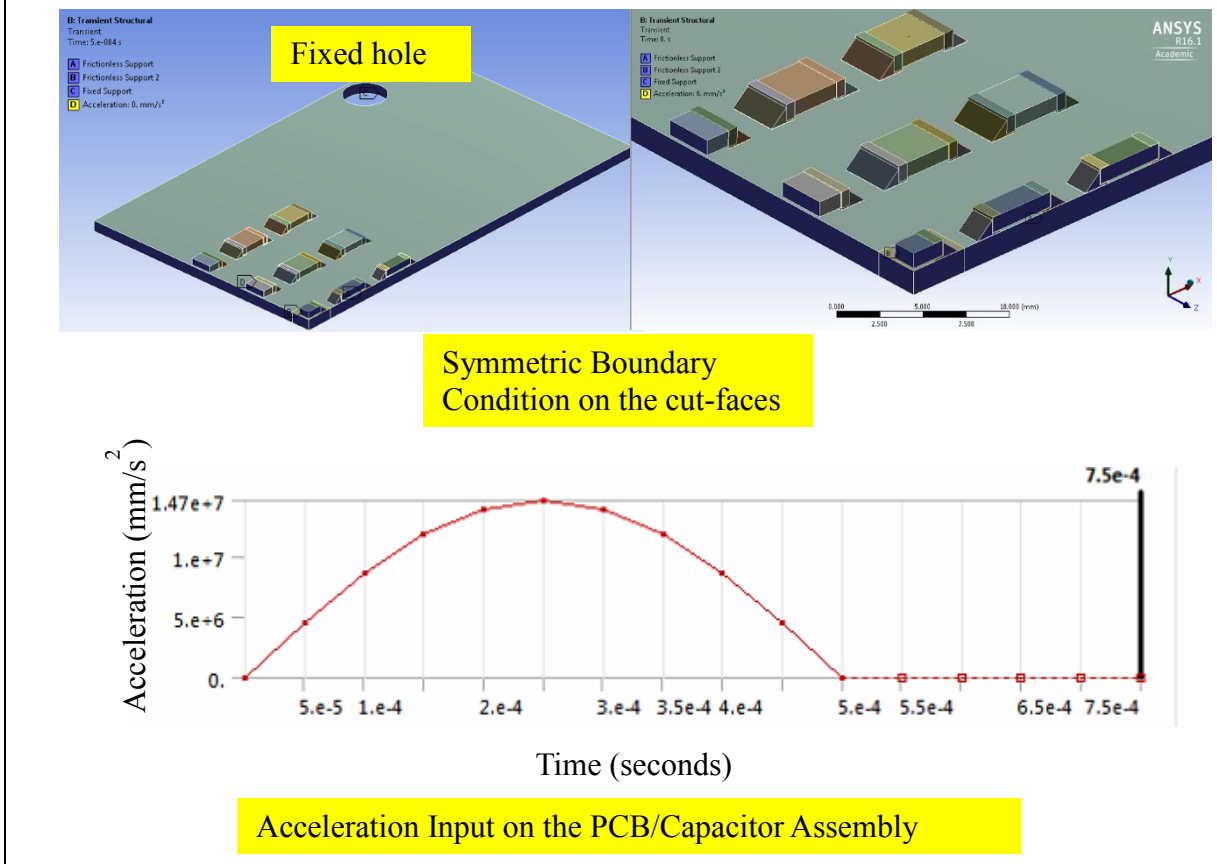


Fig 5.2: Input Acceleration Method using ANSYS Transient Structural Module. [9]

5.4 Results

a) Effect of Solder Joint Profile :

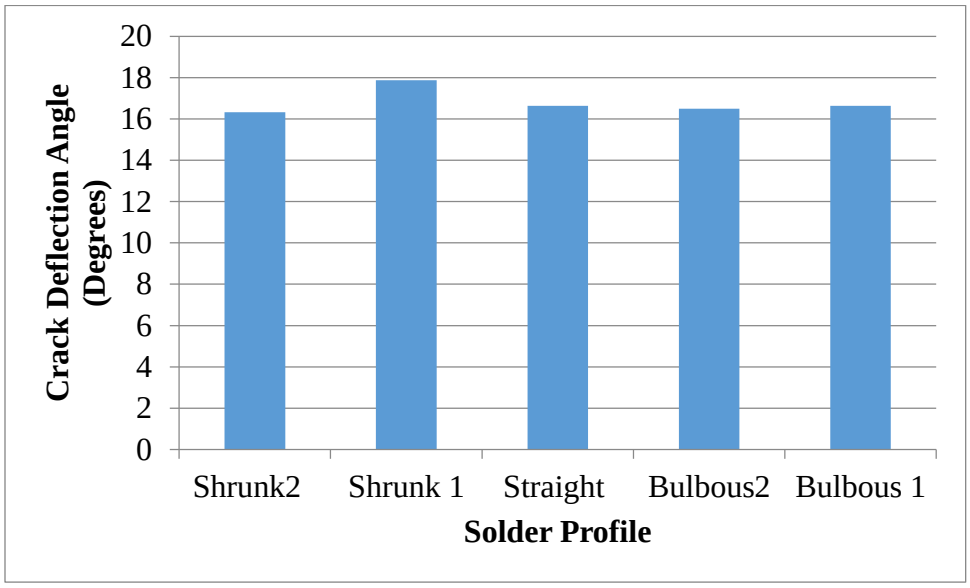


Fig 5.3: Effect of solder joint Profile on the crack deflection angle in the capacitor during drop.

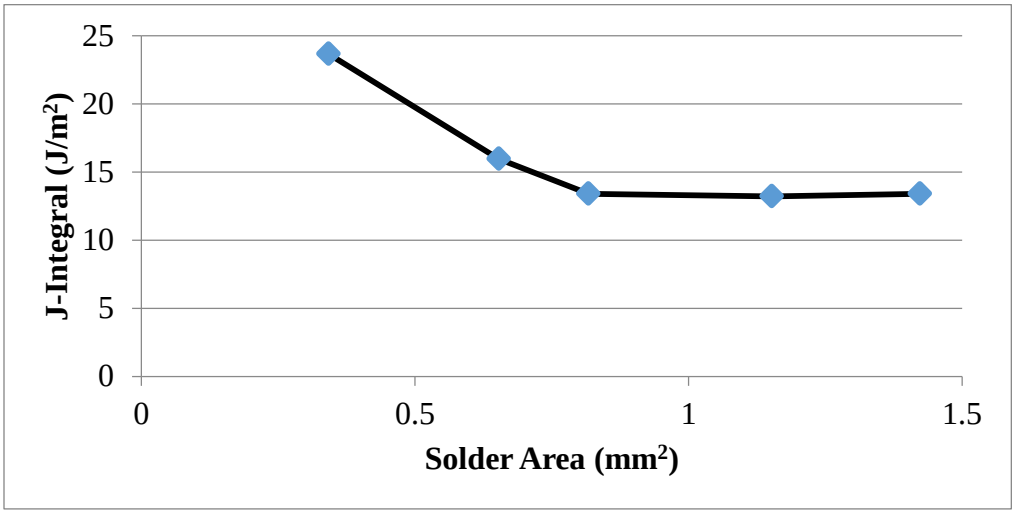


Fig 5.4: Effect of solder joint profile (Solder area) on the developed J integral inside the capacitor during drop.

Due to the change in the solder area the crack deflection is not that much significant but the developed J integral is almost cut into half from shrunk solder joint to the bulbous solder joint. Very stiff solder joint will not deform and protect the capacitor from stress concentration.

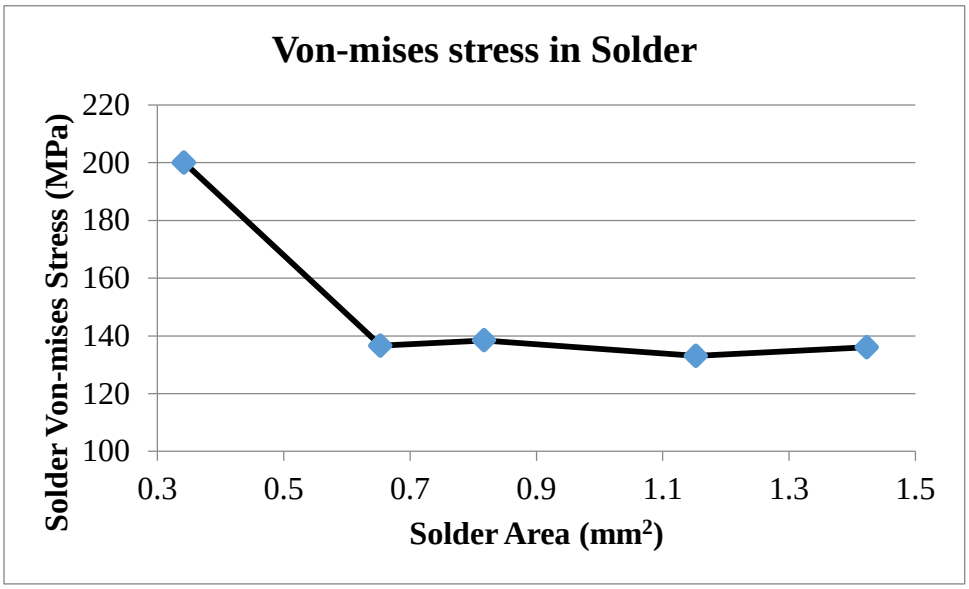


Fig 5.5: Effect of solder joint profile (Solder area) on the developed Von-mises stress in the Solder joint during drop.

By changing the solder profile, it is observed that the solder joint stress is also reduced. The bulky solder joint is resistant to the drop and absorbs lot of energy due to the increased amount of solder. That is why as more solder material will be subjected to the reduced amount of energy per unit of volume creating less stress inside the solder joint.

Over-all solder joint profile can be chosen such that the crack driving energy is lower in the capacity and the deflection angle is more. Bulbous solder joint is also helpful in terms of reducing the stress inside the solder joint.

b) Effect of Solder Joint Wetting Height:

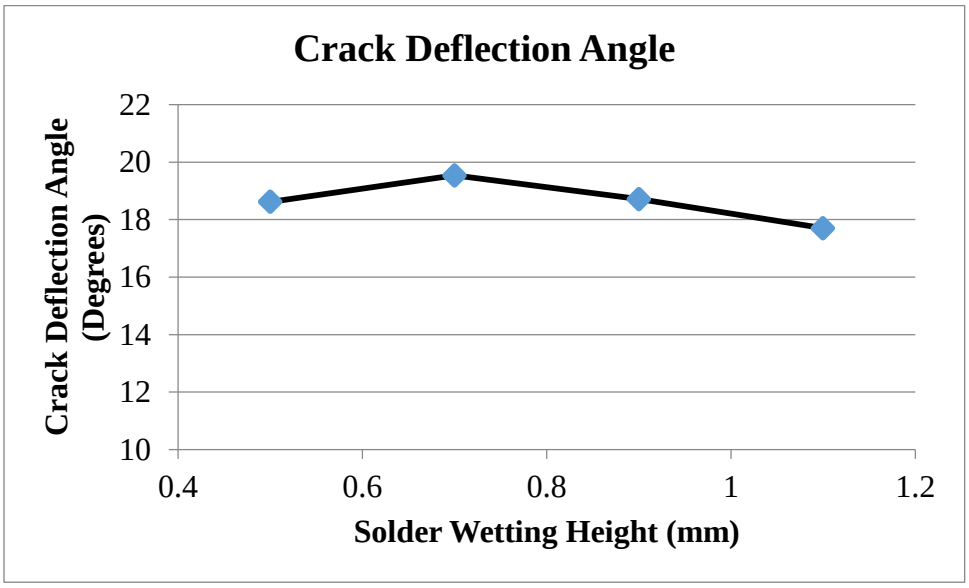


Fig 5.6: Effect of solder joint wetting height on the crack deflection angle in the capacitor during drop.

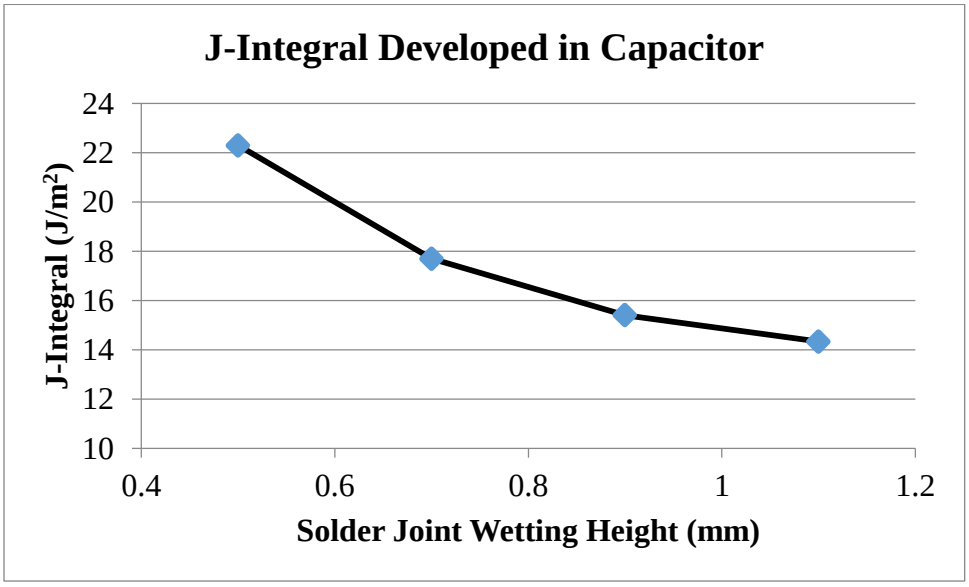


Fig 5.7: Effect of solder joint wetting height on the developed J integral inside the capacitor during drop.

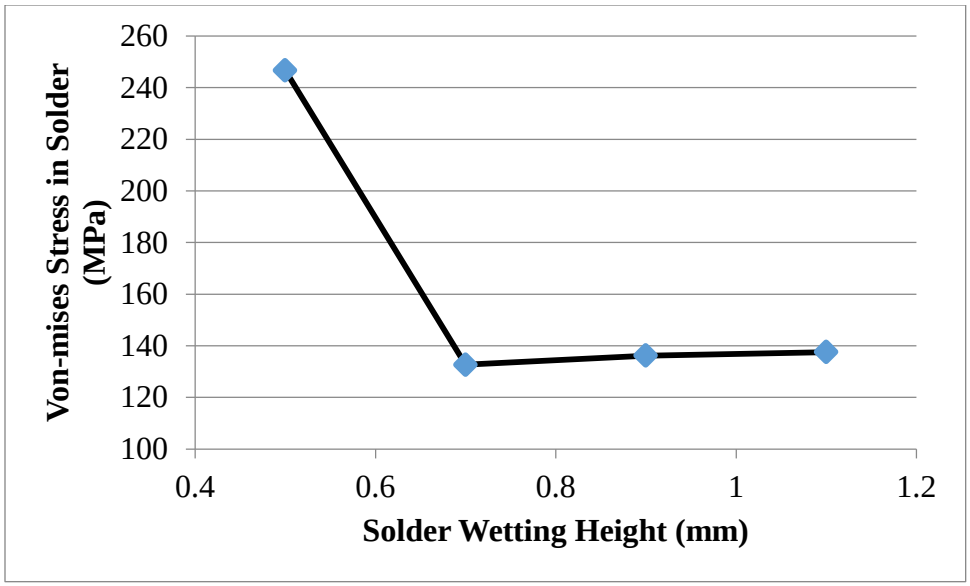


Fig 5.8: Effect of solder wetting height on the developed Von-mises stress in the Solder joint during drop.

As the Solder Joint wetting height is increased more solder amount is also increased. Increased solder amount will absorb more energy during drop event and the developed stress will be lower in solder joint and in the capacitor. As we can see from the results that both the J-integral in the capacitor and solder stress is reduced significantly by the increased amount of solder.

c) Effect of PCB material (PCB thickness and PCB stiffness)

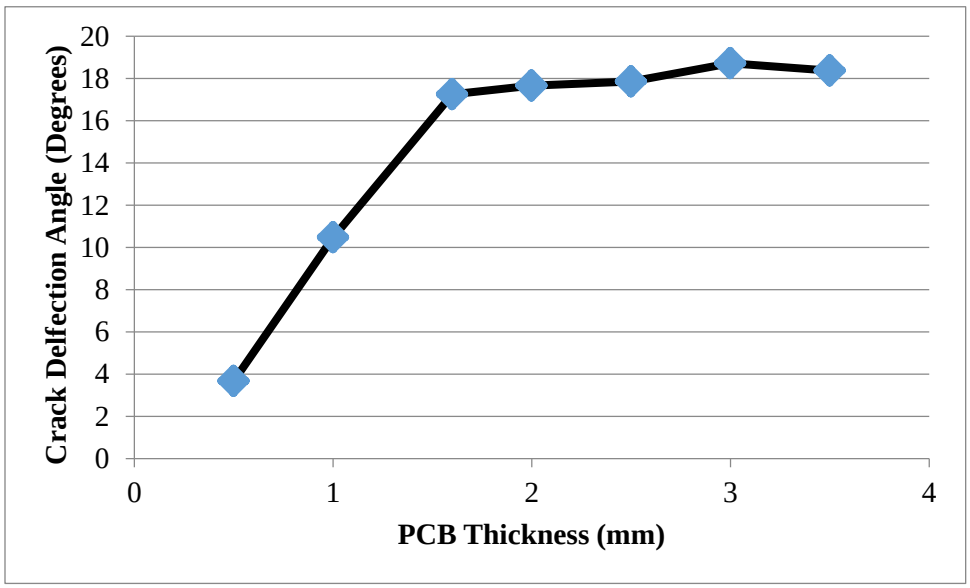


Fig 5.9: Effect of PCB thickness on the crack deflection angle in the capacitor during drop.

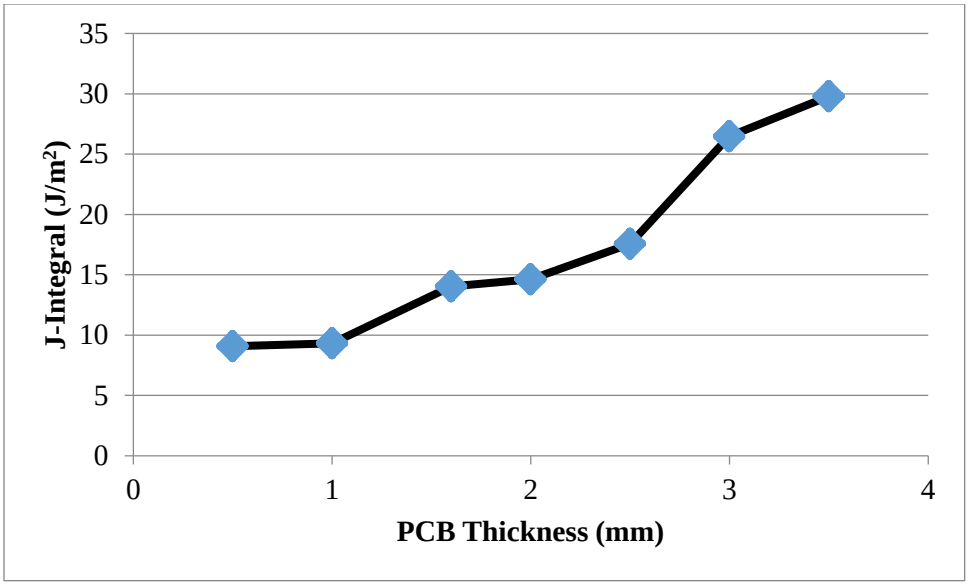


Fig 5.10: Effect of PCB thickness on the developed J integral inside the capacitor during drop.

From J integral comparison, the PCB that produces slightly more J-integral but the crack deflection is greatly changed, is 1.6 mm thick. This ensures that the crack driving force is lower in the capacitor and if crack starts to propagate then it goes at an angle deviated from the vertical line cutting lower number of electrodes.

d) Effect of PCB Stiffness:

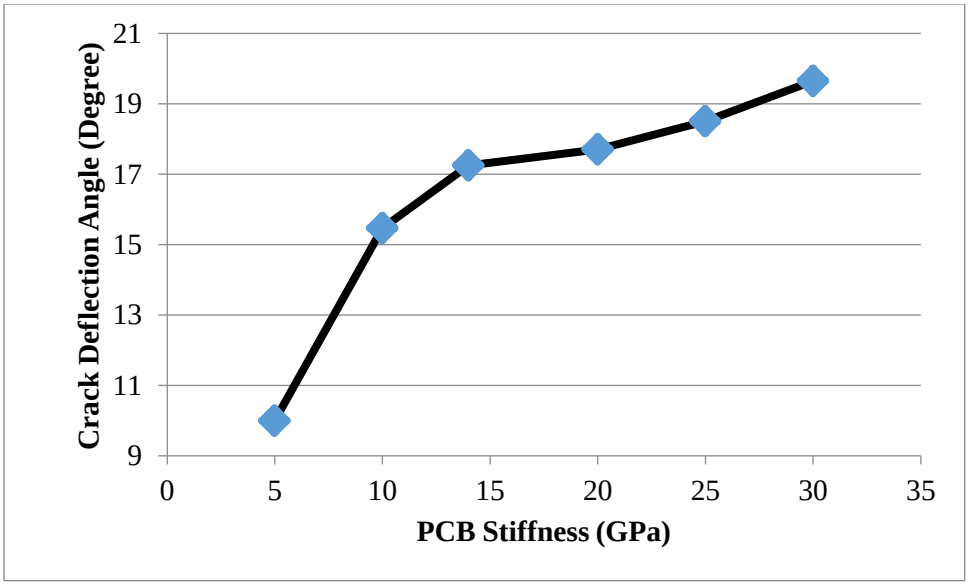


Fig 5.11: Effect of PCB stiffness on the crack deflection angle in the capacitor during drop.

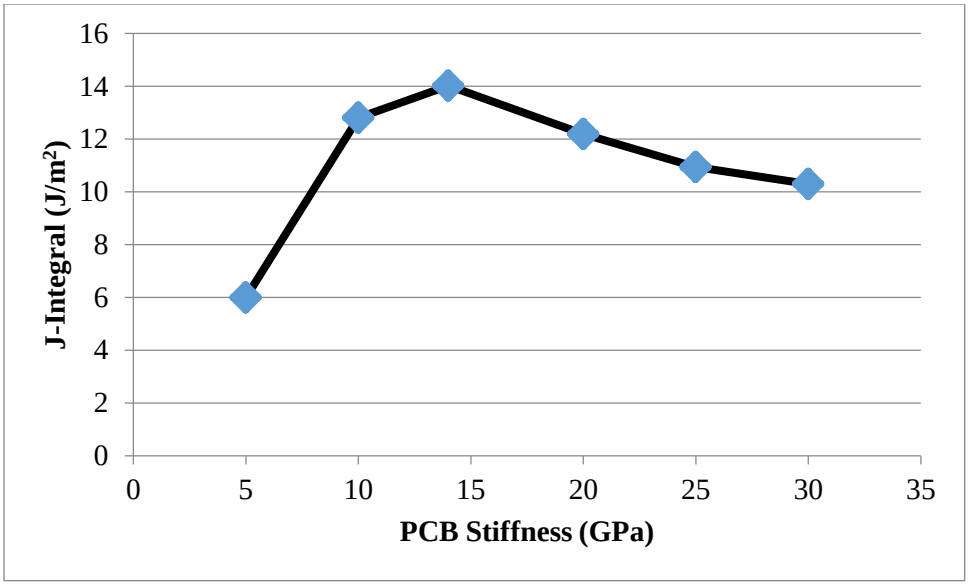


Fig 5.12: Effect of PCB stiffness on the developed J integral inside the capacitor during drop.

5.5 Conclusion

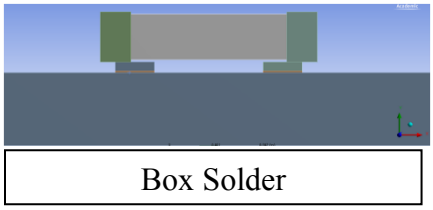
The capacitors and other passive components are now receiving renewed interest because these passives are going to be integrated in many products such as system in chip (SiP), Multi-chip modules (MCM), and intelligent power modules. So to ensure enhanced lifetime of these passive components one has to understand the application area where the capacitors are being used and what is the critical load levels that the devices will be going through. Such mechanics based approach can be implemented and subsequent design rules can be developed so that the expected device reliability can be achieved. From this study it has been shown that effectively choosing the lower stiff material for printed circuit board would reduce the failure probability during drop events. Also thin PCB material is compliant to conform to the device deformation during drop. This will reduce the induced stresses on the MLCC and on the solder joint itself. Drop/Impact reliability of MLCC solder joint and the device can be also improved by the solder joint profile. The solder joint profile can be altered through stencil selection, stand-off height modification. It has been showed in this study that higher amount of solder helps to improve the drop reliability and increases the crack deflection angle so that the crack will affect only few electrodes if it starts to propagate.

Chapter 6

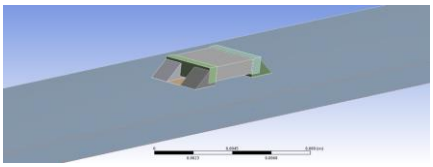
Exploring Innovative Techniques for Surface Mounting MLCC on PCB

6.1 Some innovative technique for solder attachment to mitigate flex cracking in MLCC

In this part of the thesis, different solder inter-connect material has been tailored or engineered and subsequent FE models have been built to understand if any of these artificial solder joints can help mitigate the flex cracking and improve the solder joint reliability or suppress the crack driving forces. The main hypothesis is to create a solder joint that can take up more deformation and can bend, deform, stretch without breaking or transferring more stress to the capacitor device. Box type solder reduced solder, triangular solder, copper wedge underneath the solder joint and spring like solder joint have been modeled in ANSYS.

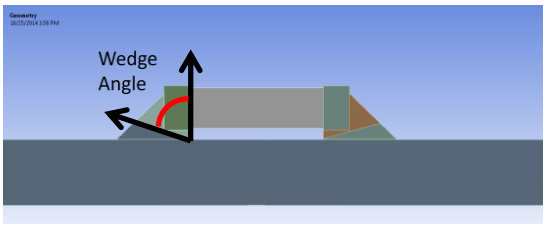


Box Solder



Reduced Solder

Triangular Solder



Putting a Copper wedge so that the load transmitting from PCB is uniformly distributed on the termination which will relieve stress concentration on the termination-mlcc corner.

Spring like interconnect to absorb the deformation during bending thus removing the stress concentration on the Capacitor.

Fig 6.1: Exploring Innovative techniques for surface mounting MLCC on PCB

6.2 Introducing the sacrificial layer to suppress the stress concentration at the tip of termination

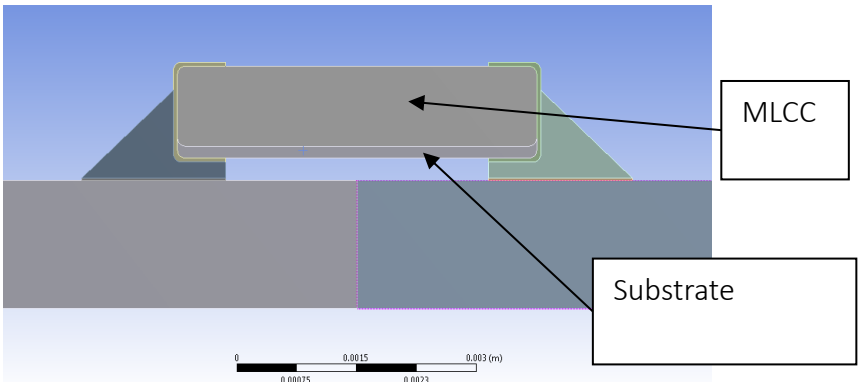


Fig 6.2: Introducing the sacrificial material to protect the MLCC

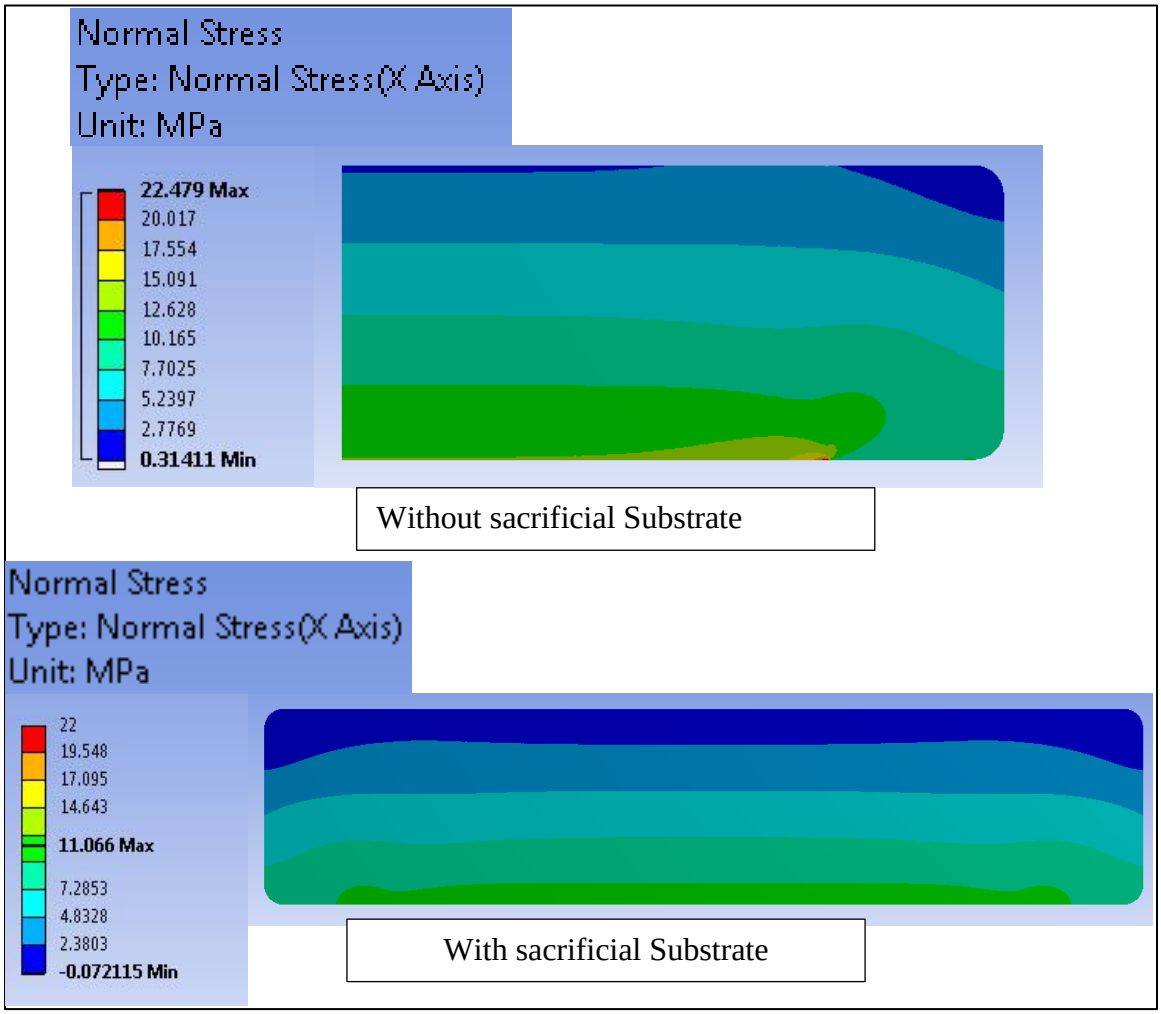


Fig: 6.3: By introducing the sacrificial layer the normal stress is reduced by half from the without sacrificial layer configuration.

If we study the stress profile in fig 6.3, we can see that there is a stress concentration point in the capacitor where there is significant amount of higher stress build up can create a crack and the capacitor can break. To remove the stress concentration point, an interface material or sacrificial layer can be introduced which can act as a barrier between the brittle capacitor and metal termination. This electrically insulated sacrificial layer can take up the buildup stress concentration and save the brittle MLCC from the higher stress. From the simulation results we can see that the sacrificial layer can reduce the stress significantly in the capacitor. The sacrificial layer can be selected such that it has compatible CTE values with the ceramic material so that the thermal stress at the interface is minimal.

6.3 Introducing copper wedge under the solder

With Copper Wedge Without Copper Wedge

Fig 6.4: Copper wedge underneath the solder joint.

	Capacitor stress Mpa	K1 MPa√m	J Integral J/m²	Solder Stress Mpa	Angle Radians	Angle Degrees
Wedge	106.1633631	0.27	1.032002207	221.4258032	0.704	40.37
without wedge	96.97908004	0.41	2.017186034	144.3876255	0.704	40.37

Fig: 6.5: Comparison of MLCC and interconnect reliability between normal and copper wedge configuration

Apparently copper wedge is not helping out much to reduce the J-integral or increasing the crack deflection angle. So this method is not an option. But copper wedge can reduce the stresses in the solder joint significantly.

6.4 Conclusion

Sacrificial layer inside the capacitor can be mounted such that the ceramic can be saved from the stress concentration corner. An electrically insulated material such as resin coated copper can be introduced as a sacrificial material. This method can help suppress the stress concentration point and reduce the stress build up in the capacitor block, thereby improving the MLCC reliability during bending. This method can be implemented with careful proof of concepts experiments.

Reference for chapters 2, 3, and 4

[1] Keimasi, Mohammadreza, Michael H. Azarian, and Michael G. Pecht. "Flex Cracking of Multilayer Ceramic Capacitors Assembled With Pb-Free and Tin–Lead Solders." *Device and Materials Reliability, IEEE Transactions on* 8.1 (2008): 182-192.

[2] Park, Jin-Woo, et al. "Thermo-Mechanical Stresses and Mechanical Reliability of Multilayer Ceramic Capacitors (MLCC)." *Journal of the American Ceramic Society* 90.7 (2007): 2151-2158.

[3] Prume, Klaus, et al. "Modelling and numerical simulation of the electrical, mechanical, and thermal coupled behaviour of Multilayer capacitors (MLCs)."*Journal of the European Ceramic Society* 22.8 (2002): 1285-1296.

[4] Lau, Dennis, et al. "Experimental testing and computational stress analysis of printed circuit board for the failure prediction of passive components under the depaneling load condition." *Electronic Components and Technology Conference, 2005. Proceedings. 55th*. IEEE, 2005.

[5] Blattau, N., D. Barker, and C. Hillman. "Lead free solder and flex cracking failures in ceramic capacitors." *CARTS-CONFERENCE-*. Vol. 24. COMPONENTS TECHNOLOGY INSTITUTE INC., 2004.

[6] http://ca.mouser.com/new/Kemet-Electronics/kemetFlexTermMLCCs/

[7] ANSYS Academic Research Release, ANSYS Static Structural Module, ANSYS Inc.

[8] ANSYS Academic Research Release, ANSYS Static Explicit Dynamics Module, ANSYS Inc.

[9] ANSYS Academic Research Release, ANSYS Static Transient Structural Module, ANSYS Inc.

[10] Fajdiga, Gorazd, and Boštjan Zafošnik. "Determining a kink angle of a crack in mixed mode fracture using maximum energy release rate, SED and MTS criteria." *stress* 1: 1.

Chapter 7

Thermo-Mechanical Reliability Estimation and Enhancement of QFN and BGA Solder Joints on Custom Printed Circuit Boards

7.1 Introduction

Active devices are the core component of any microelectronic product. Any computing device needs processor, memory and storage device. All these are silicon chips packaged in a special way so that it can be protected from outside heat, moisture and corrosion and at the same time can follow PCB interconnecting law. Essentially the PCB manufacturers always want low density interconnect on them to reduce the cost of manufacturing and assembly cost. But the Bare silicon chip has an interconnect pitch at nanometer level. There has to some intermediate medium to serve the purpose of protecting the silicon chip and fanning out the chip interconnect pitch from die to PCB level. BGA (Ball Grid Array) and QFN (Quad Flat no Lead) packages are excellent packaging technologies in terms of better electrical properties, thermal management and higher number of interconnects [1].

BGA package has higher number of solder interconnects as compared to QFN packages. BGAs utilize almost the entire package bottom to populate the solder bumps. Whereas the QFN package has interconnects coming out only from the periphery. Various application areas needs custom thinner and thicker PCBs with RCC and FR4 prepreg materials for mounting this QFN and BGA Packages. Conventionally thicker PCBs have higher stiffness and provide lower solder joint fatigue life for QFN package [2]. For BGA package thinner 1 mm boards are used with different prepreg material on the outer most layer of the PCB. This chapter of the work focuses on the estimation of solders joint reliability of QFN and BGA packages on custom printed circuit boards during thermal cycling loading.

Thicker PCBs have higher stiffness thus during thermal cycle fatigue it will not take up much deformation and will not be compliant with the deformation taking place in the package. So for QFN package the solder joint reliability will depend on the board materials, board layup, and PCB total thickness. For BGA package mounted on thinner board, the core layers are same but the outer most prepreg material is different in two boards. The hypothesis is that the softer prepreg has lower stiffness and can take up more shear deformation thus enhancing the thermo-mechanical reliability of BGA solder joints.

7.2 Evolution of IC packaging and Reliability Issues

200 years from the present time, who would have thought the human life will be so much dependent on sand. Surely sandy beaches on a coastal area with palm and coconut trees are essentially beautiful scenery. But from this very sand comes a component SILICON which in many ways changed the human life in a way no one expected 200 years back. This single piece of silicon is being transformed into millions of pieces of transistors. Transistors are the building block of today's modern electronic products. From communication to entertainment, from healthcare to military applications, every aspect of human life is now made easier, fancier and more convenient than ever before.

This single piece of silicon is so delicate that it has to be protected by the outside environment: temperature, vibration and moisture. At the same time this piece of silicon has to be connected with the outside world so that it can take inputs from the real world, process, store and transform the information back to the real world. Above mentioned activities can be achieved by providing a package/housing with interconnects to the piece of silicon.

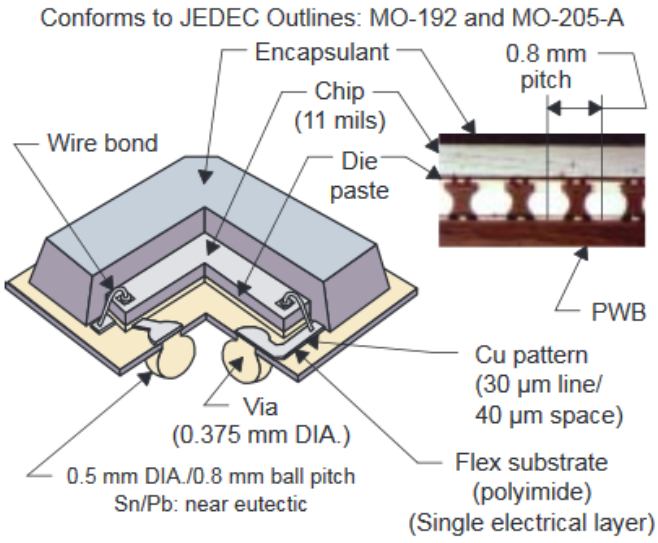


Fig 7.1: Construction of TI BGA package (http://www.ti.com/lit/wp/ssyz015b/ssyz015b.pdf)

7.3 Board Level Solder Joint Reliability Estimation for BGA Package

7.3.1 Finite Element Modeling

Detailed information from optical images is used for generating the Finite Element Model of PCB/Package assembly. Based on geometrical and load symmetry, an octant symmetry model has been leveraged to reduce computational time by reducing the number of elements in the global and local model. The FE model consists of 121 solder bumps with copper pads on the top and bottom sides. The top copper pad is T shaped which connects the die-attach. The package comprises of a 0.6 mm thick mold compound and a 0.112 mm polyimide layer. A 0.018 mm thick adhesive layer is sandwiched between the polyimide layer and the mold compound. Linear elastic material properties are used for all the materials except solder and PCB. The properties of SAC 305 are given in Table 1. Same properties were assumed for the prepreg layer as the prepreg layer is of FR4 material.

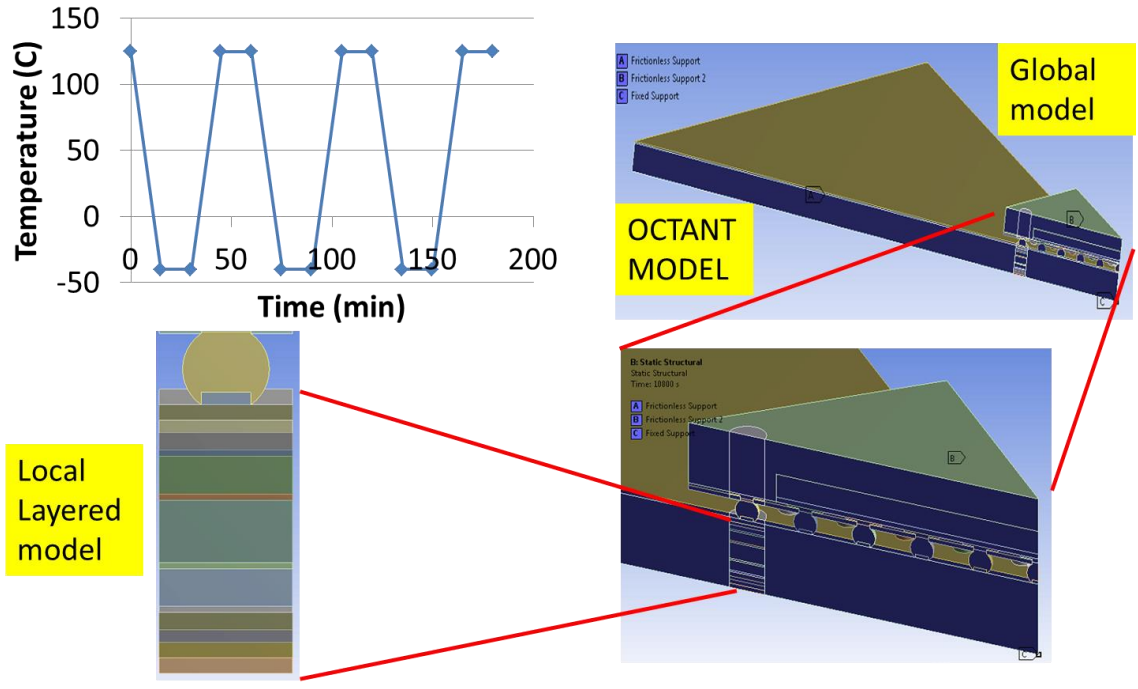


Fig 7.2: FE Modeling Methodology: BGA, global Modeling and Sub-modeling

7.3.2 Challenges in Conventional FEM analysis and the proposed Global-Local Approach

Running finite element simulation for this type of analysis can be time consuming at the same time can require significant amount of computing resources. So reducing the simulation time and computational resources and at the same time keeping the simulation result's accuracy has been a challenge for the microelectronics engineers. One method for reducing the number of nonlinear elements is to use the symmetry in the model. As the simulation domain of BGA package and the PCB board has two symmetry planes, so the number of non-linear elements can be brought down to 75% less by modeling only ¼ th of the actual PCB/package assembly. The 1/4th model can be even reduced to 1/8th model by applying octant symmetry.

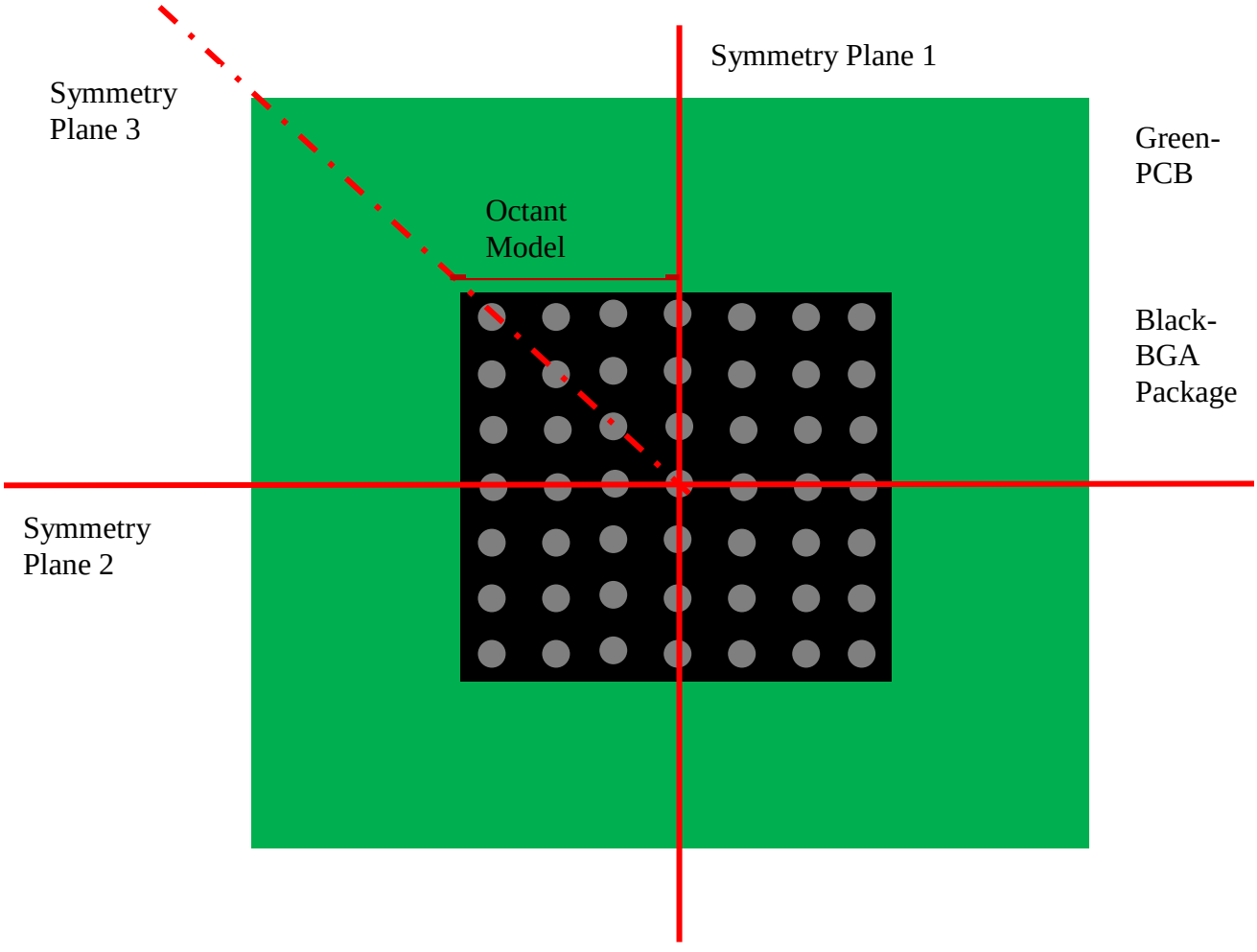


Fig 7.3: Application of octant symmetry to reduce the non-linear elements and computational times.

On the cutting plane symmetry boundary conditions are applied automatically by ANSYS Static Structural module if symmetry is mentioned while creating the geometric model. If not mentioned in the geometric model, the symmetry conditions can be even applied in the proper simulation physics window by constraining the normal displacements of the nodes at the symmetry plane.

Another challenge for creating this BLR model was to effectively creating a mesh that can capture the deformations during thermal cycling conditions. A global-local modeling methodology has been implemented to capture the local effects of the deformation at the critical solder joint. As the PCB size is significantly larger than the package, it is computationally not effective to keep a finer mesh thorough out the FE model. Instead a coarser mesh has been used for the global model and then the critical BGA ball has been identified from the global results. Essentially the corner most solder ball will be severely damaged as the distance from the neutral plane (DNP) is the largest for that solder ball. The displacements from the global model are transferred in the sub-model as boundary conditions. The PCB layer stack up with all the copper layers and prepreg layer are modeled in detail in the sub-model using a finer mesh than that of the global model.

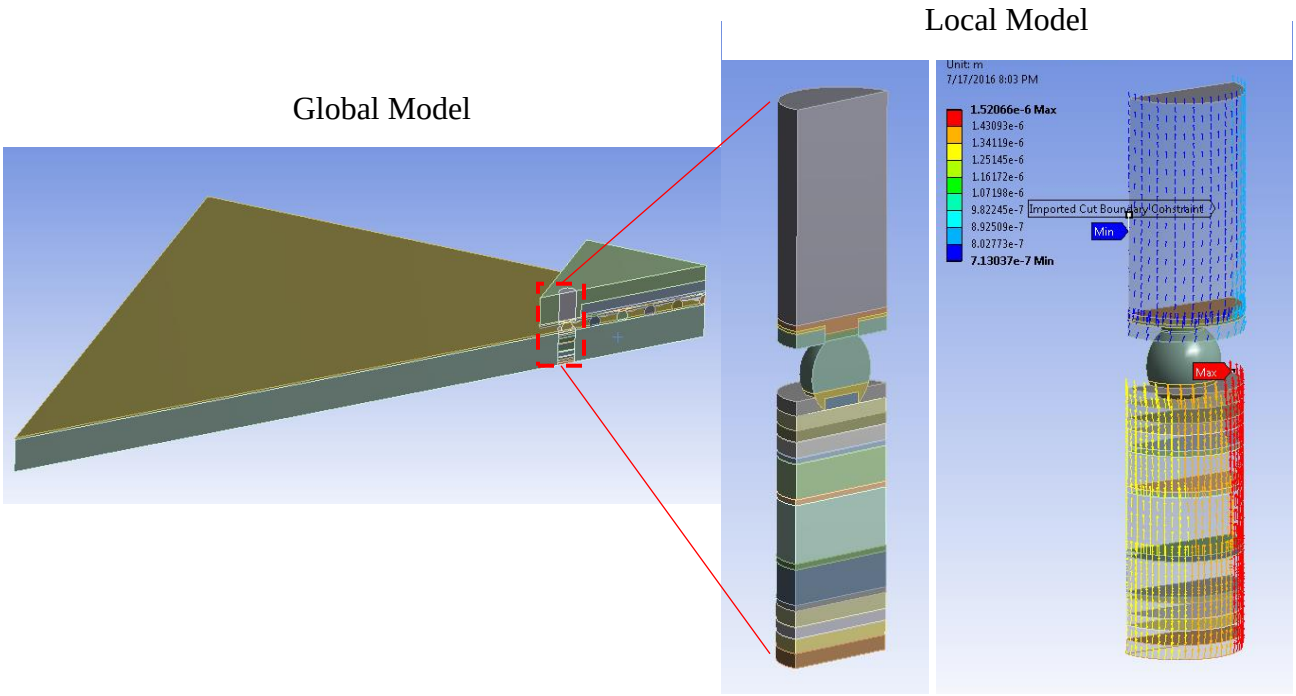


Fig 7.4: Global model and cut boundary of the local model, displacements transferred from global model to the local model.

Fig 7.5: Board Layers for BGA Package

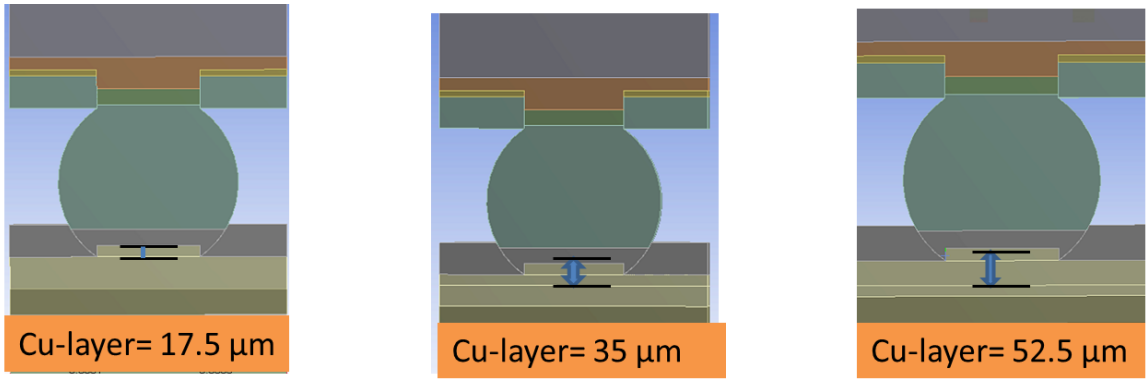


Fig: 7.6: Tailoring copper layer thickness

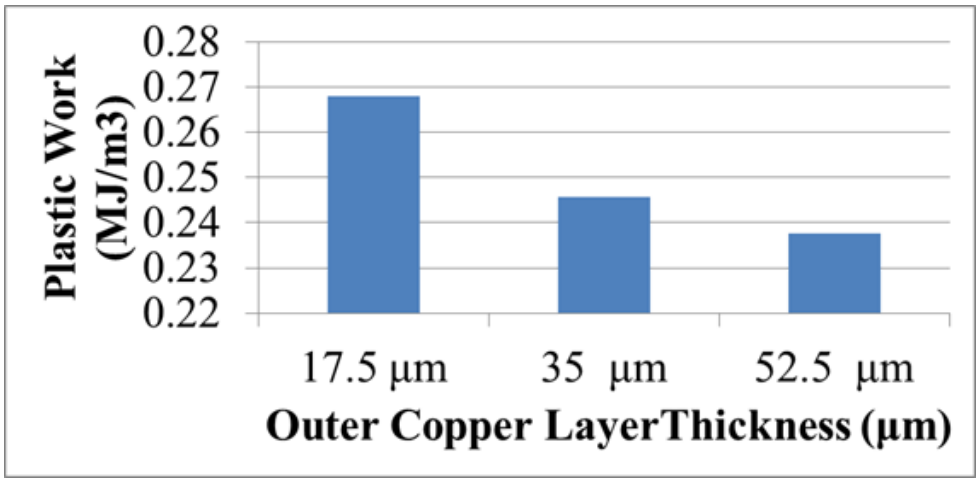


Fig 7.7: Effect of outer most copper layers on the plastic work.

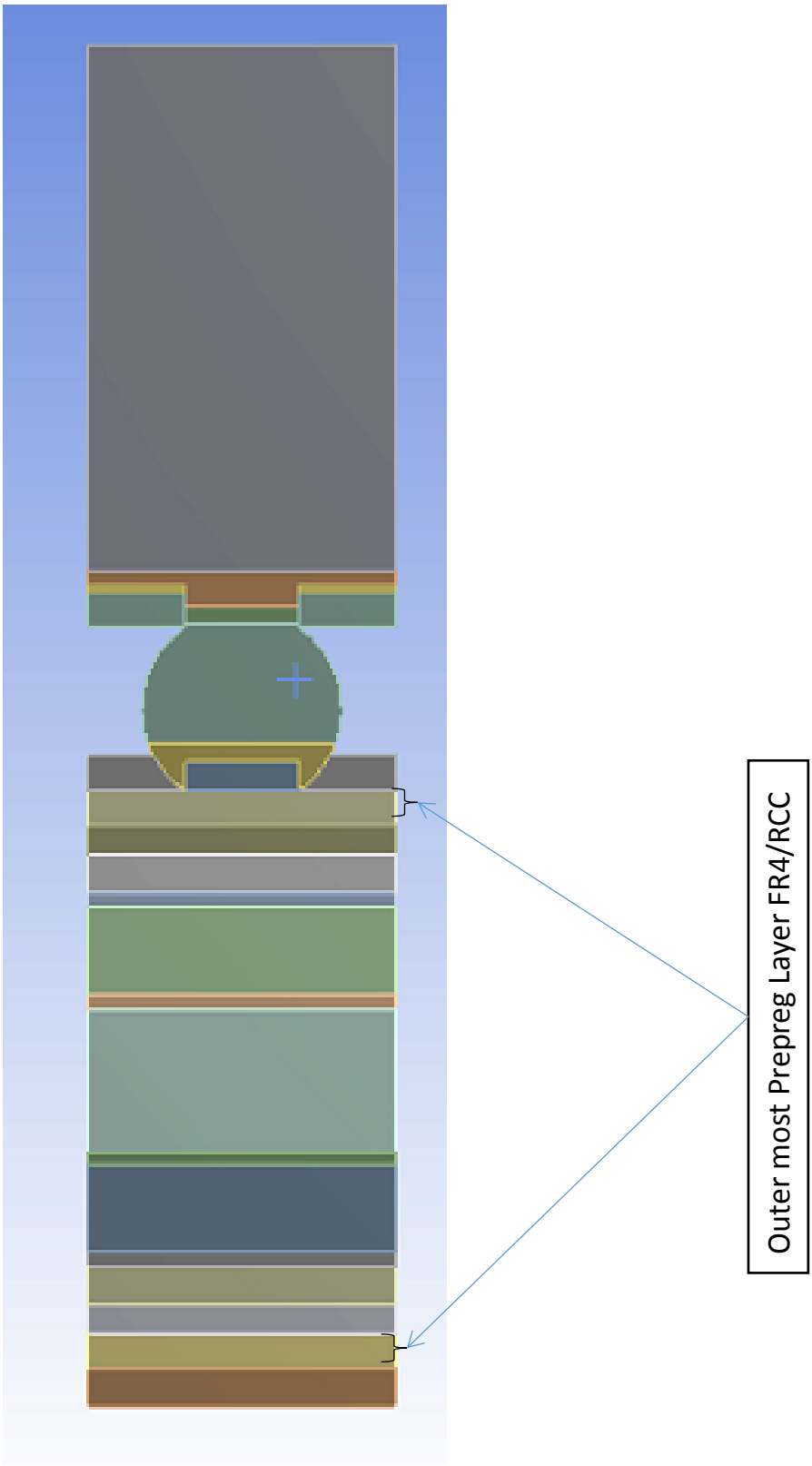
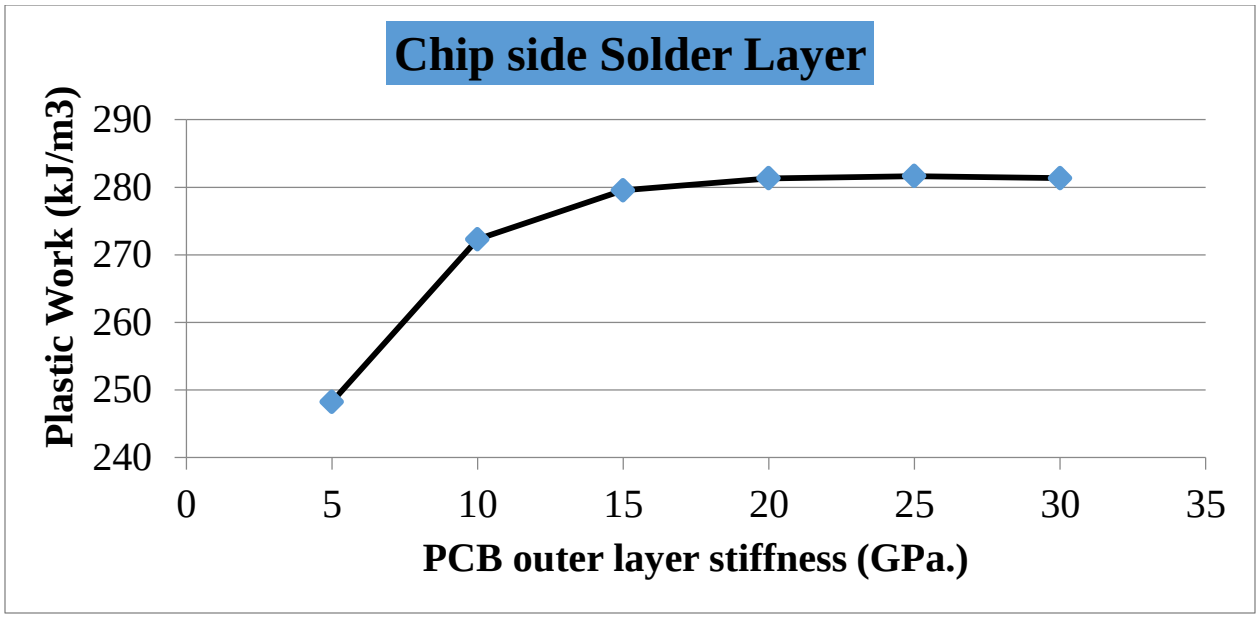


Fig 7.8: PCB outer most prepreg layers.



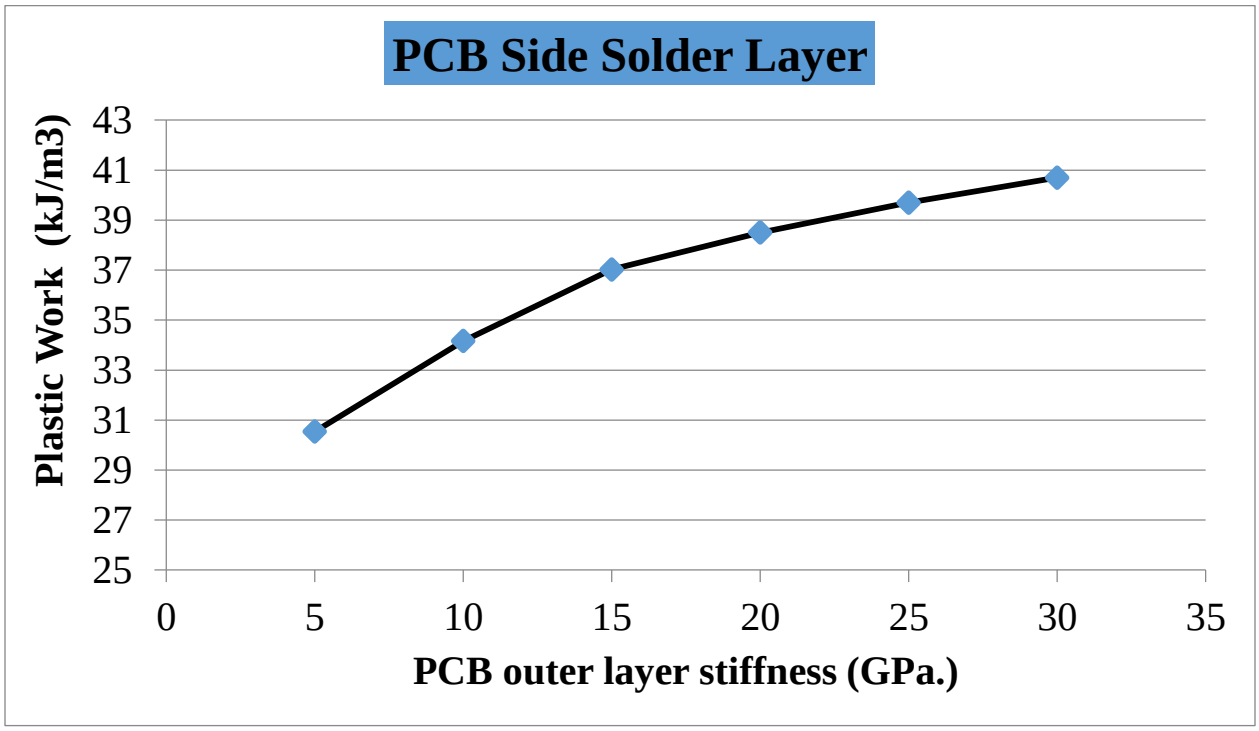


Fig 7.9 : Effect of PCB outer most prepreg layer stiffness on the BGA reliability.

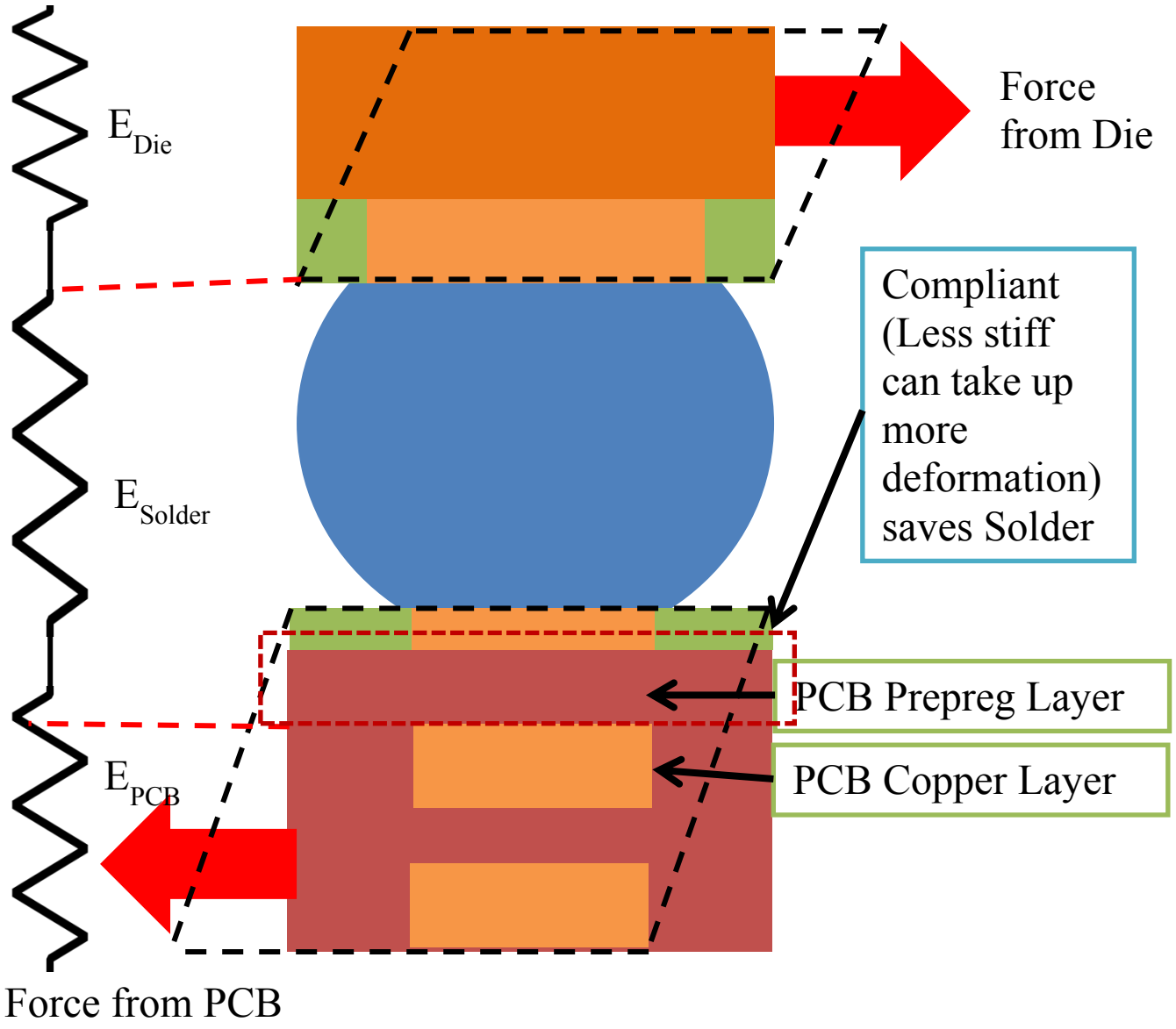
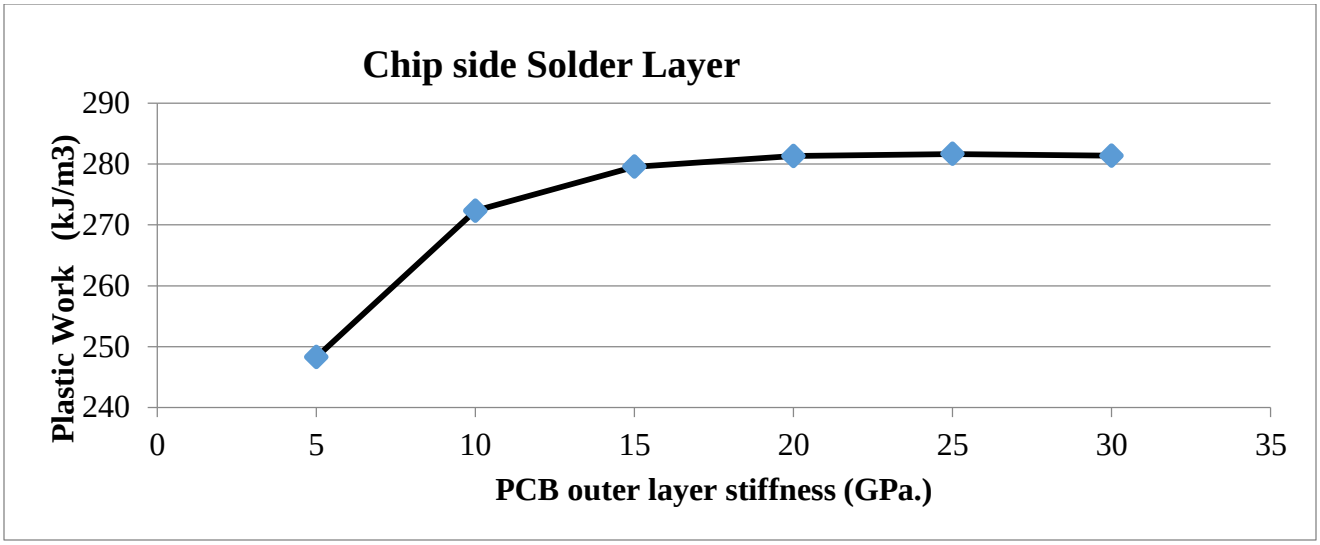


Fig 7.10 : Improving BLR by tailoring the prepreg layer stiffness.



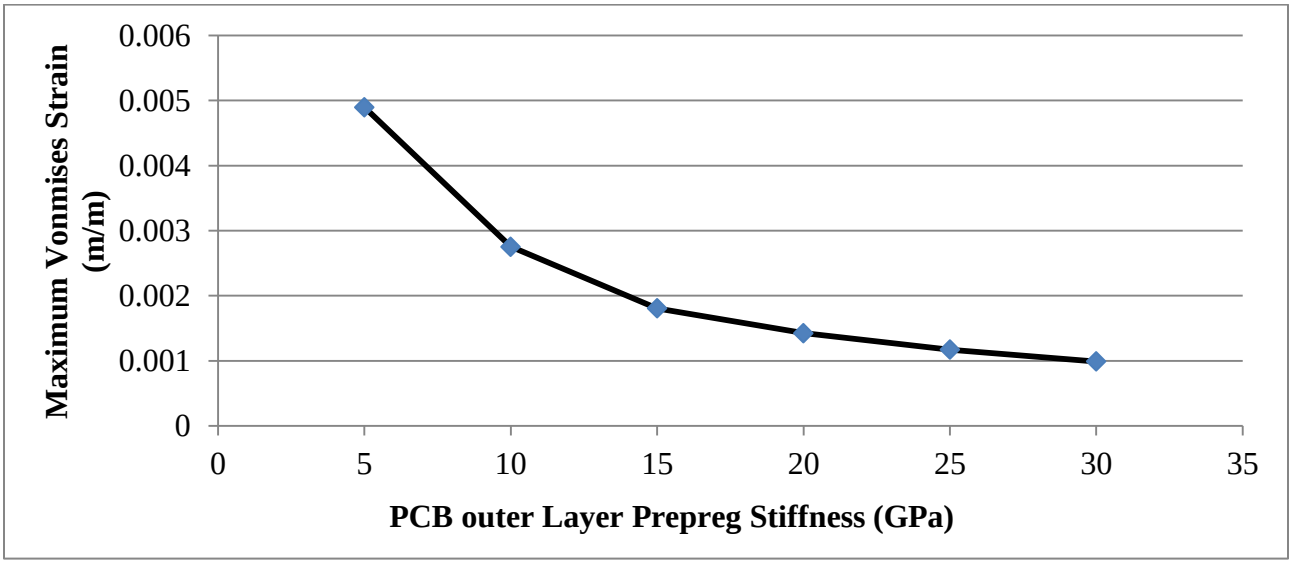


Fig: 7.11 : Effect of outer most prepreg layer of PCB on the plastic work and maximum vonmises stress in 25 microns solder layer.

7.4 Results and Discussion

During accelerated thermal cycling from -40 C to 125 C, the different components of PCB/Package assembly will try to expand due to thermal strain. But the CTE mismatch between different components in the system will enforce the individual components to bend and satisfy the strain compatibility condition. This mechanism will cause stress build up in the individual layers. Different amount of energy will be absorbed by the chip, solder layer and PCB.

Chip side solder layer is more prone to failure as the plastic work is way more than the PCB side solder layer. As the stiffness is lowered in the outermost layer, the SJR is getting better; this is in line with the TI finding: experimental ATC results. Soften outermost layer deforms more without building up stresses and thus saves the solder joint from higher stresses as the PCB/package assembly goes through thermal cycling. This way, softer polymeric material can be used as an outer most layer to improve the BLR of BGA package.

During ATC, the CTE mismatch will create bending and the external loads will be converted into internal strain energy which will deform the entire PCB, Die and Solder joint structure. During this process the internal strain energy will be absorbed by different components. The less stiff prepreg material can take up more deformation without failing thus the strain energy will be distributed more to the layer which is less resistant to the force. This mechanism will reduce the SED built up in the solder joint and thus the solder joint reliability will be improved. This is similar to the fact that the current/heat will flow through the less resistant material. So by incorporating a softer layer beneath the BGA solder layer, the solder ball can be saved from excessive stress build-up and thus the solder joint fatigue life can be improved significantly. This type of PCB material tailoring based on material deformation theory can be extended for other types of packages such as leaded or QFN type package.

7.5 Board Level Solder Joint Reliability Estimation Using Finite Element Method for QFN [3,4]

Quad Flat No Lead (QFN) package is one of the most popular packaging options for many semiconductor devices. Simpler assembly process and package structure made QFN viable solution for electronic components. Process assembly includes die attach on the lead die pad, wirebonding the die bond pads with the leadframe pads, molding and singulation. There is an exposed thermal pad which helps to remove heat from the system and may act as a ground. QFN packaging option provides better thermal path which helps to achieve higher power density. Qualifying a semiconductor product requires rigorous reliability tests prescribed by JEDEC. These packages has to be tested in accelerated environment to understand the reliability of various components such as interconnect material during its operational time. Present work investigates the effect of board thicknesses on the thermos-mechanical reliability of QFN solder joint. Fig 7.12 shows the accelerated thermal cycling profile for the FEA model. The cycle time is 60 minutes with 15 minutes dwell and ramp. The extreme temperatures are at 125C and -40C.

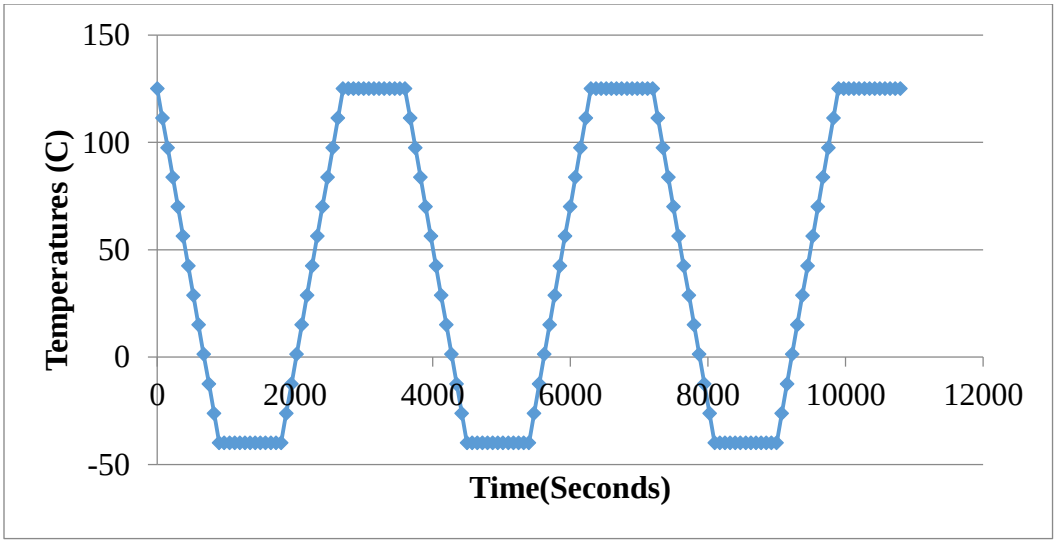


Fig 7.12: Thermal cycle profile (15 minutes dwell and ramp time)

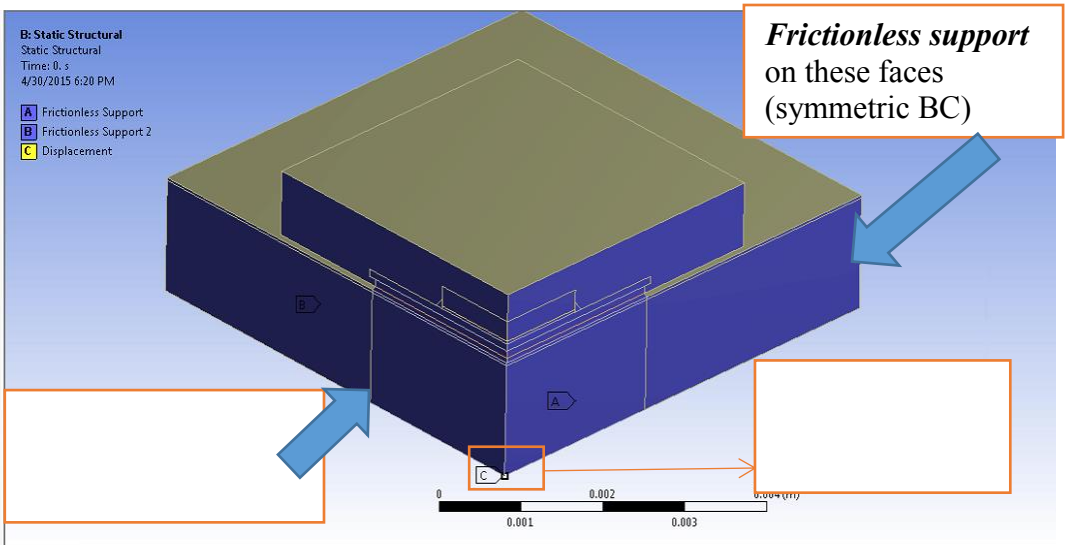


Fig 7.13: Boundary Condition for Quarter Symmetric Model

Fig 7.13 shows the quarter symmetric model and the boundary condition for the FE model. Quarter symmetric model was used to reduce the computational time and number of elements in the model.

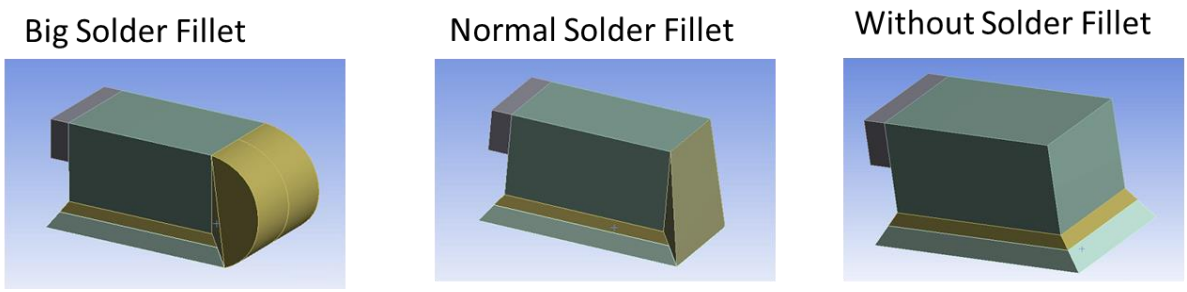


Fig 7.14: Different solder joint fillet profile.

In fig 7.14, effect of different solder joint profile on the QFN fatigue life was analyzed. The fillets formation can be achieved by careful choices for stencil design, bond line thickness and components placement parameters. From fig 7.15, it is observed that bulky solder fillet reduced the plastic work in the solder joint. This also helps to improve the fatigue life because now the crack has to propagate through a longer path.

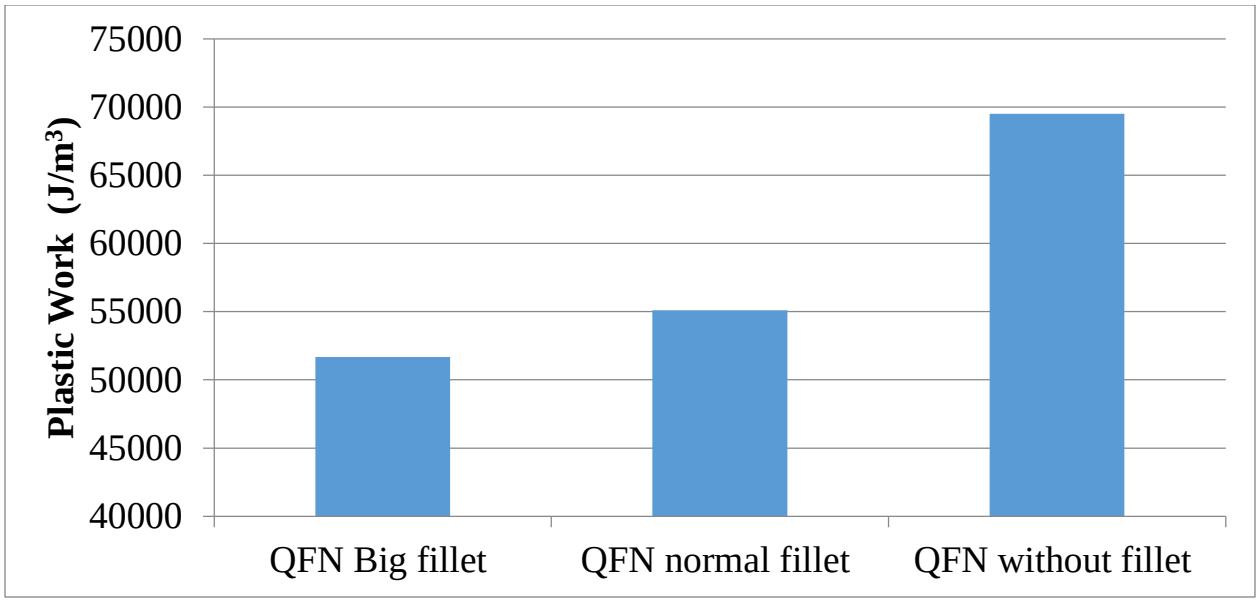


Fig 7.15: Effect of solder joint fillet on the developed plastic work in the critical solder layer.

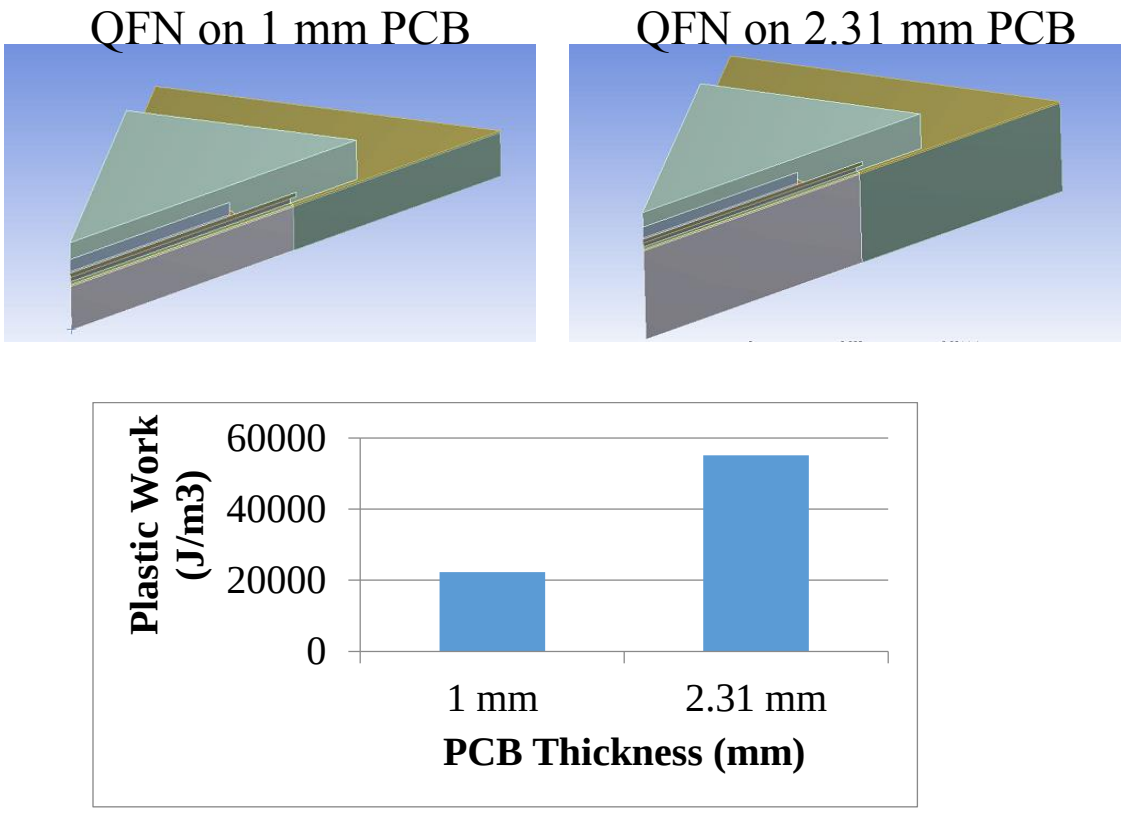


Fig 7.16: Effect of PCB thickness on the developed plastic work in the critical solder layer.

7.6 Relationship Between Board Level Solder Joint Reliability and PCB thickness

From previous studies it is evident that the board level reliability (BLR) has been affected critically by the increased PCB thickness [2]. Recent technological innovations are driven by the fact that the semiconductors in a product will have lowest real estate and has improved functionality. In the automotive industry the ECU performs several jobs such as controlling the engine systems, fuel intake systems and many other functions. These functionality improvements require many more devices such as processors, memory, control ICs, power modules integrated in one mother board which is essentially a PCB. So the number of routing copper layers inside the PCB has to be increased to accommodate all the power lines and signal lines of this system.

As the number of conductive layers and insulating layers are increased in the PCB material, the thickness will also increase. Thicker boards are stiffer thus creates more stresses on the solder joint during thermal cycling as the displacement compatibility requires the package and PCB to bend together. This is very detrimental for the solder joint. Thus conventionally thicker boards are not good for BLR.

QFN packages are widely used in the automotive industry for many different applications. At the same time automotive industry requires a certain amount of BLR on thicker boards for robust application in car's electronic control units (ECU). This requirement of BLR of different packages on thicker boards create a significant amount of challenges for the engineers in semiconductor packaging industry to understand the underlying physics that dictates and controls the failure mechanism in a solder joint. From the FE simulations performed in this study, it is shown that, QFN solder joint reliability has been degraded as the PCB thickness is increased from 1 mm to 2.31 mm. The plastic work or inelastic strain energy density is almost 147% increased as the board thickness is increased from 1 mm to 2.31 mm keeping all other conditions same.

At the same time, from the BGA solder joint reliability study we can see that the same board thickness can yield different solder joint reliability if the outer layer properties of PCB are

changed/tailored. For BGA the board thickness is 1 mm for both the cases. But for one case outer prepreg layer is FR4 and in another case the outer layer is resin coated copper. This changes the conventional relationship between the board thickness and the BLR. Based on the results of this study it is evident that there exists an inflection point after which lowering the PCB thickness can degrade the solder joint reliability.

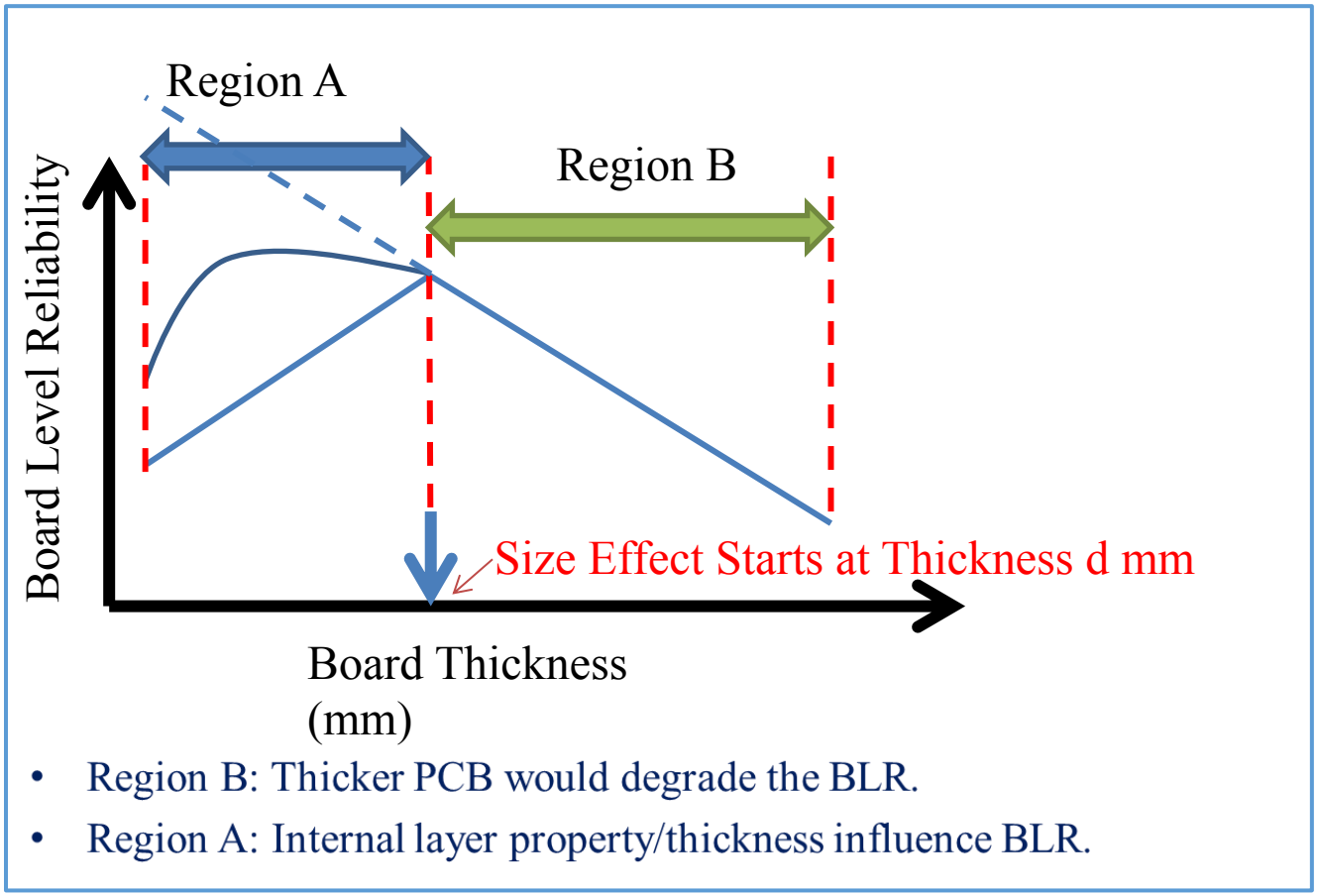


Fig 7.17: Relationship between PCB thickness and BLR.

The critical relationship between the board thickness and the solder joint reliability can be divided into two regions:

Region A: Reducing PCB thickness will improve or degrade the Board Level Reliability and it depends on the internal layer composition such as copper layer distribution and mechanical property of the prepreg material. In this case for the same board thickness the BGA solder joints

are behaving differently as the internal compositions of the layers are different in the RCC and FR4 boards. FR4 prepreg layer is stiffer than the resin coated copper layer.

Region B: If we start reducing the thickness of a PCB material by reducing the thicknesses of each individual internal layers then the BLR will improve significantly but at some point the size effect will dictate the overall BLR of Package. Then the overall PCB stiffness and CTE will be susceptible to the internal layers: mainly copper layer thickness and prepreg material's stiffness or mechanical property. We can tailor or engineer the prepreg material such a way that the outermost material layer can take up more deformation and can absorb the strain energy more. This will prevent excessive load on the solder joint and improve BLR.

Reference

[1] Plieninger, R., M. Dittes, and K. Pressel. "Modern IC packaging trends and their reliability implications." *Microelectronics Reliability* 46.9 (2006): 1868-1873.

[2] Syed, Ahmer, and WonJoon Kang. "Board level assembly and reliability considerations for QFN type packages." *Amkor Technology, Inc., Chandler, AZ*2 (2003).

[3] Zhao, Jie-Hua, et al. "Reliability modeling of lead-free solder joints in wafer-level chip scale packages." *Journal of Electronic Packaging* 132.1 (2010): 011005.

[4] Darveaux, Robert. "Effect of simulation methodology on solder joint crack growth correlation." *Electronic Components & Technology Conference, 2000. 2000 Proceedings. 50th*. IEEE, 2000.

[5] Lee, W. W., L. T. Nguyen, and Guna S. Selvaduray. "Solder joint fatigue models: review and applicability to chip scale packages." *Microelectronics reliability* 40.2 (2000): 231-244.

[6] Agrawal, Akash, et al. "Board level energy correlation and interconnect reliability modeling under drop impact." *Electronic Components and Technology Conference, 2009. ECTC 2009. 59th*. IEEE, 2009.

Chapter 8

Summary and Future Outlook

8.1 Summary

Studied the passive and active device reliability under fracture mechanics framework and investigated the roles of different design parameters to improve the device reliability.

- **Bending**
  - A Fracture Mechanics based holistic investigation has been done on the behavior of MLCC subjected to PCB static mechanical bending
  - A 2D finite element model has been used for analyzing the deformations and stresses in the MLCC when the MLCC/PCB assembly is subjected to bending
  - Various design parameters such as solder joint profile: bulbous, shrunk, straight and optimum; solder joint wetting and stand-off height; can be tailored such that the developed stress intensity factor and crack propagation are less.
  - From this study it is showed that the crack deflection can be increased by increasing the solder amount and the solder wetting height.
  - Solder joint stand-off height has detrimental effect on both the J ased by increasing the solder amount and t
- **ATC**
  - Lower stiff PCB materials can conform to the deformation of the MLCC thus transferring less stress on the capacitor.
  - Thinner PCB materials will also enhance the reliability of the MLCC device and the solder joint.
  - If the application area of the MLCC requires the device to be subjected to higher temperature then starved or shrunk solder joint can be formed to reduce the plastic work in the solder joint and to suppress the crack driving force in the capacitor.
- **Drop**
  - From this study it has been shown that effectively choosing the lower stiff material for printed circuit board would reduce the failure probability during drop events.
  - Also thin PCB material is compliant to conform to the device deformation during drop. This will reduce the induced stresses on the MLCC and on the solder joint itself.

- Drop/Impact reliability of MLCC solder joint and the device can be also improved by the solder joint profile. The solder joint profile can be altered through stencil selection, stand-off height modification
- Higher amount of solder helps to improve the drop reliability and increases the crack deflection angle so that the crack will affect only few electrodes if it starts to propagate.

- **Proposed a new packaging technique for developing MLCC capacitor with enhanced fracture resistance.**
  - To remove the stress concentration point, an interface material or sacrificial layer can be introduced which can act as a barrier between the brittle capacitor and metal termination.
  - This electrically insulated sacrificial layer can take up the buildup stress concentration and save the brittle MLCC from the higher stress. From the simulation results we can see that the sacrificial layer can reduce the stress significantly in the capacitor.
  - This method can be implemented with careful proof of concepts experiments.
  - Copper wedge is not helping out much to reduce the J-integral or increasing the crack deflection angle. So this method is not an option. But copper wedge can reduce the stresses in the solder joint significantly.

- **Proposed a design envelop relating PCB thickness and device reliability.**
  - Region A: Reducing PCB thickness will improve or degrade the Board Level Reliability and it depends on the internal layer composition such as copper layer distribution and mechanical property of the prepreg material. In this case for the same board thickness the BGA solder joints are behaving differently as the internal compositions of the layers are different in the RCC and FR4 boards. FR4 prepreg layer is stiffer than the resin coated copper layer.
  - Region B: If we start reducing the thickness of a PCB material by reducing the thicknesses of each individual internal layers then the BLR will improve significantly but at some point the size effect will dictate the overall BLR of Package.

8.2 Future Outlook

Experimental validation of the proposed solutions can be carried out to understand how the theory helps mitigate the reliability issues. The MLCC device can be surface mounted using different solder profile and failure can be observed through SEM imaging technique. Interface material can be explored to see if the sacrificial layer is helping to reduce the stress at the termination tip. Reliability of devices in SiP(System in Package) can be analyzed because the MLCC will be affected by developed IC temperature. Another idea to mitigate the problem will be to design the material such that the crack moves at a lower angle. Barium Titanate crystal direction can be changed to tailor the crack deflection angle and it can help to lower the crack driving energy.

For solving the BLR problems in custom PCBs, running ATC cycle test for same bga/qfn package with variation of board materials and board thicknesses and compiling the data for a wide range of package and PCB can help to understand the threshold thickness where the board layers actually matters. This study can be extended to incorporate the effect fo ATC cycle condition. Cycle condition: 1cph, 2cph, 0.cph, ramp rate and dwell time dependence of the BLR on custom PCBs can be analyzed to holistically tackle the BLR issue. PCB design rules that can be derived from the above mentioned investigation to achieve required BLR for different application.

Biography

A R Nazmus Sakib was born on 14th January, 1987 in the coastal city of Patenga in Chittagong, Bangladesh. He completed his Bachelor of Science in Mechanical Engineering from Bangladesh University of Engineering and Technology (BUET) in October 2009. Shortly afterwards, he started working as Assistant Maintenance Engineer in Unilever, Bangladesh. But being eager to pursue higher education, he left his job of seven months to come to USA for his PhD degree.

In January 2011, he started his graduate studies in the Department of Mechanical and Aerospace Engineering at University of Texas at Arlington. Here, he was co-advised by Dr. Ashfaq Adnan and Dr. Dereje Agonafer for his PhD work on the *Enhancement of Thermo-Mechanical and Impact Reliability of Passive and Active Microelectronic Devices.* He was a team leader in Semiconductor Research Corporation (SRC) sponsored project, focusing on *Birth-to-Death Modeling Methodology for the Optimization of Custom Board Level Reliability for different Packages QFN, WCSP, BGA.*

He is currently working as a Packaging Engineering Intern in Texas Instruments Incorporated, Dallas TX. Upon completion of his degree, he aspires to pursue a career in semiconductor industry and contribute in innovative, state-of-the-art technology for the advancement of humankind.