Power-Derived Thermal Characterization of SiGe HBTs and Design of Timing Circuit using a Phase Locked-Loop

by

VALAY DINESHBHAI SHAH

Presented to the Faculty of the Graduate School of

The University of Texas at Arlington in Partial Fulfillment

of the Requirements

for the Degree of

DOCTOR OF PHILOSOPHY IN ELECTRICAL ENGINEERING

THE UNIVERSITY OF TEXAS AT ARLINGTON

May 2016

Copyright © by Valay Dineshbhai Shah 2016

All Rights Reserved

ACKNOWLEDGEMENTS

I would like to express my deepest gratitude to my advisors, Dr. W Alan Davis and Dr. Ronald L Carter, for their excellent guidance, caring, patience, and providing me with an excellent atmosphere for doing research. I would also like to thank Dr. Howard T Russell for his valuable inputs and interest in my dissertation. I thank them for their patience and encouragement that carried me on through difficult times, and for their insights and suggestions that helped to shape my research skills. I am proud to be a part of this group. I will always cherish the time that I have spent in this group.

I would also like to acknowledge Dr. Andrew Brandt for his guidance for developing the timing circuit project. I would like to extend my sincere thanks to Dr. Jung-Chih Chiao for being on the committee and providing his inputs.

I am grateful for the support of UTA EE Department and Texas Instruments, Inc., Santa Clara for providing the SiGe HBTs for measurements.

I am greatly indebted to my parents, Dineshbhai Shah and Harshidaben Shah, for the support and love they provided me through my entire life. I would like to thank my sister, Grishma S Vora, who is always there when I need help. In particular, I would like to thank my beautiful and caring wife, Nupur, for her understanding and faith that she has put in me. Finally, I am very grateful to my extended family for their continual support and tasty food that had got me going.

ABSTRACT

Power-Derived Thermal Characterization of SiGe HBTs

and Design of Timing Circuit using a

Phase Locked-Loop

Valay Dineshbhai Shah, Ph.D.

The University of Texas at Arlington, 2016

Supervising Professor: W. Alan Davis and Ronald L Carter

Silicon Germanium (SiGe) hetero-junction bipolar transistors (HBTs) have been designed to cater the demand of high speed circuits having speed applications in wireless, optical communication and space electronics. Due to higher cut-off frequencies and high speed applications, self heating plays a significant role in the performance of SiGe HBTs. This dissertation paper does an extensive analysis on the effect of self heating and used DC measurement methods to extract the self heating parameter, thermal resistance (R_{th}). A non-linear thermal model is proposed to take into account the effects of the non-linearity in device parameters with increase in device temperature.

The HICUM (HIgh CUrrent Model) model is used for all the simulations. Simulations are performed using IC-CAP (Integrated Circuit Characterization and Analysis Program) tool. The linear thermal model attached at the thermal node of the HICUM model was replaced with a Current Controlled Voltage Source (CCVS) in order to implement the non-linear thermal model

for simulations. Measurements are done using HP 4142B modular DC source/module connected to the computer via Hewlett-Packard Interface Bus (HPIB). Texas Instruments, Incorporation's SiGe LV (Low Voltage) HBTs with varying emitter lengths are used for measurements.

The second project of this research is to design a timing circuit with an output jitter of the order of ~ 5 ps. The timing circuit was designed using a Phase Locked Loop (PLL). The basic concept of this system is based on the similar system designed at Stanford Linear Accelerator (SLAC). The input reference signal is provided by the Timing, Trigger and Control (TTC) Systems for the Large Hadron Collider (LHC) at Conseil Europeen por la Recherche Nucleaire (CERN). The frequency of the reference signal is ~ 40 MHz. Jitter content of this signal prevents it to be used as a timing signal for other electronics. In order to re-use the basic design from SLAC, this reference signal is up-converted to ~ 480 MHz using a two step up-conversion process. This up-converted signal is then stabilized using a PLL. After stabilization (jitter reduction) the 480 MHz signal is down-converted using a divider with division factor of 12. The jitter in the final output signal is of the order of ~ 2 ps.

TABLE OF CONTENTS

ACKNOWLEDGEMENTS iii

ABSTRACT iv

LIST OF ILLUSTRATIONS xii

LIST OF TABLES xv

Chapter .... Page

Chapter 1 1

INTRODUCTION 1

1.1 Evolution of silicon bipolar transistors 1

1.2 Overview of silicon-germanium hetero-junction bipolar transistors 3

1.3 Design of a timing circuit using a phase locked loop 9

1.4 Dissertation contributions 10

Chapter 2 12

DEVICE PHYSICS of SILICON and SiGe TRANSISTORS 12

2.1 Band structure of Si BJT 12

2.2 Band structure of SiGe HBT 14

2.2.1 Effects of germanium addition on the device parameters 18

2.2.2 Second-order effects 27

Chapter 3 31

SELF HEATING in HBTs 31

3.1 Introduction 31

3.2 Temperature effect on device parameters 34

3.2.1 Effect of temperature on band-gap narrowing 34

3.2.2 Effect of temperature on density of states 34

3.2.3 Effect of temperature on carrier mobility 35

3.2.4 Effect of temperature on current gain, β 36
3.3 Thermal-electrical analogy 37
3.4 Definition of thermal terms 38
3.4.1 Thermal resistance 38
3.4.2 Thermal conductivity 39
3.4.3 Proposed non-linear thermal resistance model 42
3.4.4 Thermal capacitance 43
3.5 Available models of self heating in HBTs 44
3.5.1 HIgh Current Model (HICUM) 45
3.5.2 HICUM model level 2 version 2.34 49
3.5.3 Implementation of proposed non-linear thermal resistance in the HICUM model 49
Chapter 4 51
MEASUREMENT SETUP 51
4.1 Device Under Test (DUT) setup 51
4.1.1 Hewlett-Packard 4142B modular dc source/monitor 53
4.1.2 Probe details 54
4.1.3 Preventing oscillation from the test device 55
4.2 DC measurements 56
4.2.1 Forward Gummel measurement setup 57
4.2.2 Base voltage controlled output characteristics measurement setup 57
4.3 Simulations and optimization procedures 58
4.3.1 Optimization procedure 58
4.3.2 Junction temperature estimation 60
Chapter 5 61
RESULTS AND DISCUSSIONS 61
5.1 The 20 μm Device Results 61
5.1.1 Optimized Forward Gummel (FG) plots 61

5.1.2 Base voltage controlled output characteristics (output characteristics) plots 63
5.1.3 Junction temperature plot 64
5.1.4 Current gain, β 65
5.2 The 0.8 μm Device 66
5.2.1 Optimized Forward Gummel (FG) plots 66
5.2.2 Base voltage controlled output characteristics (output characteristics) plots 67
5.2.3 Junction temperature estimation 69
5.2.4 Current gain (β) 69
5.3 Summary of results 70
5.4 Effect of error in junction temperature estimation on gain drift 75
Chapter 6 77
CONCLUSIONS AND FUTURE RESEARCH 77

APPENDIX A 80
ADDITIONAL PLOTS 80
A.1 The 0.4 μm device 80
A.1.1 Forward Gummel results 80
A.1.2 Base voltage controlled output characteristics results 81
A.1.3 Current gain, β 82
A.1.4 Junction temperature estimation 82
A.2 The 0.6 μm device 83
A.2.1 Forward Gummel results 83
A.2.2 Base voltage controlled output characteristics results 84
A.2.3 Current gain, β 85
A.2.4 Junction temperature estimation 85
A.3 The 1 μm device 86
A.3.1 Forward Gummel results 86

A.3.2 Base voltage controlled output characteristics results 87
A.3.3 Current gain, β 88
A.3.4 Junction temperature estimation 88
A.4 The 5 µm device 89
A.4.1 Forward Gummel results 89
A.4.2 Base voltage controlled output characteristics results 90
A.4.3 Current gain, β 91
A.4.4 Junction temperature estimation 91
A.5 The 10 µm device 92
A.5.1 Forward Gummel results 92
A.5.2 Base voltage controlled output characteristics results 93
A.5.3 Current gain, β 94
A.5.4 Junction temperature estimation 94

APPENDIX B 95
DESIGN OF A TIMING CIRCUIT USING A PHASE LOCKED LOOP 95
B.1 Introduction....95
B.2 Introduction to Phase Locked Loops (PLL) 96
B.3 Design of a Timing Circuit using PLL 97
B.4 Up-Conversion Circuit Design....98
B.5 Transmitter (TX) Circuit Design....100
B.6 Receiver (RX) Block Design 101
B.7 Down-Conversion Circuit Design 102
B.8 Circuit Operation....104
B.9 Circuit Components 104
B.9.1 Bias Tee....104
B.9.2 Band-Pass Filter....105

B.9.3 Circulator....106
B.9.4 Low-Pass Filter....107
B.9.5 RF Amplifier....107
B.9.6 DC Amplifier....110
B.9.7 Coupler....110
B.9.8 Attenuator....110
A.9.9 Oscillator....111
B.9.10 180° Hybrid Coupler....114
B.9.11 PID Controller....114
B.9.12 Mixer....114
B.10 Test Equipments....115
B.10.1 Digital Signal Oscilloscope (DSO)....115
B.10.2 Spectrum analyzer....115
B.10.3 Signal generator....116
B.10.4 Frequency counter....117
B.10.5 DC power supply....118
B.11 Results....118
B.11.1 Spectral purity of the signal generator....118
B.11.2 Up-conversion block output....120
B.11.3 PLL output....123
B.11.4 Frequency divider output....124
B.11.5 Frequency divider output using VCO with higher K_{VCO}....125
B.11.6 Simulation results....126
B.12 Conclusion....127
B.13 Further research....127

Appendix C 129

C.1 Bill of materials list for the timing circuit 129

C.2 Timing circuit components layout..130

REFERENCES 132

BIOGRAPHICAL INFORMATION 136

LIST OF ILLUSTRATIONS

Figure Page

Figure 1-1: A schematic of a typical first generation SiGe HBT (figure not to the scale) [11]. 3
Figure 1-2: (a) Doping and germanium (Ge) profiles of the SiGe HBT. (b) A plot of operating frequency versus the collector current of the SiGe HBT applied with collector-emitter voltage of 1 V and base-emitter voltage of 0.95 V [13]. 4
Figure 1-3: (a) A plot of cut-off frequency/transition (f_T) as a function of base width W_B [12]. (b) A plot of cutoff frequency (f_T) as a function of emitter-collector breakdown voltage, BV_{CEO} [12]...... 6
Figure 1-4: The plots of f_T and f_{max} as a function of temperature. (a) Results for a HBT with emitter width of 1.5 μm as reported by [16]. (b) Results for a 130 nm HBT as reported by [15]. . 7
Figure 1-5: The typical trend of noise figure, *NF*, with respect to the source resistance in HBTs [19].. 8
Figure 2-1: The band structure of a Si Bipolar Junction Transistor (BJT) with bias and defining major parameters [9]. 12
Figure 2-2: The three main designs for Ge base profile for SiGe HBTs. (a) A rectangular or box SiGe box, (b) a linearly graded base and (c) a trapezoidal base HBT [9]. 15
Figure 2-3: (a) Band structure for npn BJT and a rectangular Ge base profile in a npn HBT. (b) Band structure for a npn BJT with a linearly graded Ge base profile [9]. 17
Figure 2-4: Plot of forward transit time versus inverse of current density, J_C [1]. 25
Figure 2-5: Plot of f_T versus current density, J_C for a first generation SiGe HBT technology [1]. 26
Figure 2-6: (a) Temperature dependence of the collector current and the current gain of a graded SiGe HBT. The current-voltage (*I-V*) characteristics at 300 K and 85 K are shown in the inset. (b) Schematic diagram of the emitter-base (EB) depletion region and its bias dependence [25]..28
Figure 3-1: (a) Band-gap of silicon versus temperature. (b) Temperature and Ge mole fraction dependence of band-gap for a SiGe device [32]. 34
Figure 3-2: Temperature and Ge mole fraction dependence of $(N_V N_C)_{SiGe}/(N_V N_C)_{Si}$ [32]. 35
Figure 3-3: (a) The electron mobility as a function of temperature as reported by [34]. (b) The electron mobility as a function of temperature as reported by [35]. 36
Figure 3-4: The hole mobility as a function of temperature as reported by [34].........................36
Figure 3-5: (a) Temperature dependence of the current gain for a 4x20 μm SiGe HBT [36]. (b) Output Characteristics of a 4x20 μm SiGe HBT [36]. 37

Figure 3-6: Relationship of thermal conductivity of bulk silicon and thin Si films versus temperature [40]. 40
Figure 3-7: Relationship of thermal conductivity of Si for different silicon layer thickness [40]. ..41
Figure 3-8: Comparison of experimental and theoretical results for thermal conductivity of SiO_2 films and bulk SiO_2 at various temperatures [42]. 41
Figure 3-9: Comparison of measured f_T as a function of J_C with VBIC and HICUM compact models in a SiGe HBT [57]. 44
Figure 3-10: A schematic showing large signal equivalent circuit for the HICUM model [57]. 48
Figure 3-11: (a) A schematic of the thermal network as implemented in the standard HICUM model [52]. (b) A schematic of an equivalent thermal model to the thermal model shown in (a). 49
Figure 3-12: The model definition of the current controlled voltage source (CCVS) in ADS simulator that is used to implement the non-linear thermal model in the HICUM model [61]......50
Figure 4-1: Picture of HP 4142B modular dc source/monitor with High Power SMUs (HPSMUs) and Ground Unit (GNDU) connections. 52
Figure 4-2: Picture showing HPSMU connections with the bias network modules which are connected to the device under test via SMA cables. 52
Figure 4-3: Picture showing the device mounted on the probe station with probes assembly. ...53
Figure 4-4: Simplified SMU circuit diagram [62]. 54
Figure 4-5: A picture of the SG and GS Infinity probes with a vertical connector positioned on the probe station holding the wafer. 55
Figure 4-6: (a) Infinity SG and GS probes contacting the NPN device on the wafer. (b) Small contact marks on the device aluminum pads left behind by the probes [63]. 55
Figure 4-7: Example of an oscillating test device output characteristics [62]. 56
Figure 4-8: Schematic of the set up that was used for forward Gummel measurement. 57
Figure 4-9: Schematic of the set up that was used for base voltage controlled output characteristics measurement. 57
Figure 5-1: The optimized FG plot using the non-linear thermal model for a 20 μm device. 62
Figure 5-2: The optimized FG plot using the linear thermal model for a 20 μm device. 62
Figure 5-3: The plot of optimized output characteristics using the non-linear model for a 20 μm device. Here the black dashed-dot and black solid curves represents the I_C curves at V_{BE} = 560-840 mV in steps of 16 mV measured by sweeping V_C=0-2 V in steps of 40 mV. 63

Figure 5-4: The plot of optimized output characteristics using the linear model for a 20 μm device. Here the black dashed-dot and black solid curves represents the I_C curves at V_{BE} = 560-840 mV in steps of 16 mV measured by sweeping V_C=0-2 V in steps of 40 mV. 64
Figure 5-5: The plot of the junction temperature calculated using the non-linear and linear thermal models for a 20 μm device. 65
Figure 5-6: The plot of current gain, β, versus base-emitter voltage for the non-linear thermal model for a 20 μm device. 65
Figure 5-7: The plot of current gain, β, versus base-emitter voltage for the linear thermal model for a 20 μm device. 66
Figure 5-8: The optimized FG plot using the non-linear thermal model for a 0.8 μm device. 67
Figure 5-9: The optimized FG plot using the linear thermal model for a 0.8 μm device. 67
Figure 5-10: The plot of optimized output characteristics using the non-linear model for a 0.8 μm device. Here the black solid and black dashed-dot curves represents the I_C curves at V_{BE} = 560-840 mV in steps of 16 mV measured by sweeping V_C = 0-2 V in steps of 40 mV. 68
Figure 5-11: The plot of optimized output characteristics using the linear model for a 0.8 μm device. Here the black solid and black dashed-dot curves represents the I_C curves at V_{BE} = 560 mV to 840 mV in steps of 16 mV measured by sweeping V_C = 0 to 2 V in steps of 40 mV.........68
Figure 5-12: The plot of the junction temperature calculated using the non-linear and linear thermal models for a 0.8 μm device. 69
Figure 5-13: The plot of current gain, β, versus base-emitter voltage for the non-linear thermal model for a 0.8 μm device. 70
Figure 5-14: The plot of current gain, β, versus base-emitter voltage for the linear thermal model for a 0.8 μm device. 70
Figure 5-15: The plot of difference in junction temperature as estimated by linear and non-linear thermal model versus the device dimensions. 72
Figure 5-16: The plot of difference in junction temperature as estimated by linear and non-linear thermal model versus the inverse of device dimensions. 72
Figure 5-17: A plot showing the trend of R_0 and R_{th} as a function of device dimension..............73
Figure 5-18: A plot showing the trend of R_0 and R_{th} as a function of device dimension..............74
Figure 5-19: A plot showing the trend of *dRdP* as a function of device dimensions. 74
Figure 5-20: A plot showing the trend of *dRdP* as a function of inverse of device dimensions...75

LIST OF TABLES

Table Page

Table 2-1: A TABLE SUMMARIZING THE CHANGES TO THE MAIN BIPOLAR PARAMETERS FOR DIFFERENT GE BASE PROFILES [9]. 18
Table 3-1: RELATIONSHIP BETWEEN THE THERMAL DOMAIN AND THE ELECTRICAL DOMAIN 38
Table 3-2: COMPARISON OF IMPORTANT FEATURES OF THE SGP, VBIC, HICUM AND MEXTRAM COMPACT MODELS [56]. 45
Table 4-1: LIST OF DEVICES USED FOR MEASUREMENTS 51
Table 4-2: LIST OF DEVICE MODEL PARAMETERS USED FOR OPTIMIZATIONS 59
Table 5-1: SUMMARY OF JUNCTION TEMPERATURE FOR VARIOUS DEVICES USING LINEAR AND NON-LINEAR THERMAL MODEL 71
Table 5-2: SUMMARY OF THERMAL RESISTANCE AND *dRdP* FOR VARIOUS DEVICES USING LINEAR AND NON-LINEAR THERMAL MODEL 73

Chapter 1

INTRODUCTION

Electronic information in its infinitely varied forms and levels of complexity, is gathered from our analog sensory world, transformed in very clever ways into logical binary forms for ease of storage, manipulation and transmission, and subsequently regenerated into analog sensory output for our use. No matter how one perceives it, at the most fundamental level, it is semiconductor devices that are enabling this communications revolution [1].

Microelectronics is defined as the multifunctional integration of electronic devices. The goals of development of microelectronics have always been to further increase the number of devices per unit area, the integration level, the signal processing rate (i.e. the information transfer per unit time) and multi-functionality. It is an easy case to make that the semiconductor, silicon (Si), has single-handedly enabled this communications revolution because of its remarkable virtues: (i) Over 90% of the earth's crust is composed of silicate compounds, making silicon the second most abundant element in the earth's crust after oxygen [2]. (ii) The oxides of silicon are easy to form, have superior thermal and chemical properties, and are stable. (iii) Silicon is a non-toxic element. (iv) Furthermore, fabrication costs are minimized by increasing the packing density, increasing the production yield. Silicon bipolar technology has superior qualities in terms of high speed, high current carrying capability per unit area and greater transconductance compared to the Metal Oxide Semiconductor (MOS) transistors. Bipolar Junction Transistors (BJTs) hold the dominant position in high speed design application [3].

1.1 Evolution of silicon bipolar transistors

The design of bipolar transistors requires trade-offs between a number of competing mechanisms. In order to achieve a short base transit time and in turn a high value of cut-off frequency, the base width needs to be very small. The transistors fabricated using planar bipolar technology typically have a cut-off frequency, f_T, of around 500 MHz which were used to produce early transistor-transistor logic (TTL) circuits and operational amplifiers in the 1970s [4]. But the mechanism that limits frequency response is the base punch through effect which occurs when the base-emitter depletion region

intersects the base-collector depletion region in the base. Thinner base widths can be obtained by increasing the base doping concentration. But the disadvantage of heavy doping of the base is that it results in reduction of transistor gain. This trade-off between gain and base transit time is the main factor that limits the maximum achievable cut-off frequency of a silicon bipolar transistor. In practice, it is technologically difficult to achieve cut-off frequencies higher than 50 GHz in silicon bipolar transistors [3]. Further advancement led to the development of the double poly-silicon bipolar transistor with a cut-off frequency, f_T, of 38 GHz used in emitter coupled logic gates and high frequency analog circuits [5].

As wonderful as silicon is from the fabrication viewpoint, from a circuit designer's perspective, it is hardly the ideal semiconductor. Three main reasons for this are: (i) the carrier mobility for both the holes and electrons in Si is comparatively small compared to their III-V cousins, (ii) the maximum velocity that these carriers can attain under high electric fields is limited to about 1 x 10^7 cm/sec under normal conditions, relatively "slow" because the speed of the transistor ultimately depends on how fast the carriers can be transported through the device under the influence of applied voltages. (iii) Silicon is an indirect band-gap material and hence is not suitable for making active optical devices such as diode lasers. While Si Integrated Circuits (ICs) are well suited for high packaging densities, high volume microprocessors and memory application, radio frequency, microwave and even millimeter-wave electronic circuit applications, which by definition operate at high frequencies, generally place much more stringent performance demands on the transistor building blocks. Hence, the poorer intrinsic speed of Si devices becomes problematic. In other words, even if Si ICs are cheap, they must deliver the required device and circuit performance to produce a competitive system at a given frequency. The answer to the shortcomings of Si is the band-gap engineering approach where the performance of the Si bipolar transistors can be improved enough to be competitive with III-V devices for high performance applications while still preserving the enormous yield, cost and manufacturing ease [1].

Even though, the theory of hetero-junction bipolar transistors and band-gap engineering was pioneered by Kroemer in 1957 [6] it was not until the late 1980s that the growth of SiGe on pure Si epitaxy was developed providing an economical approach to building Si Heterojunction Bipolar Transistors (HBTs) [7]. Previously, HBTs were only available in compound semiconductor technologies such as AlGaAs/GaAs, because an effective hetero-junction formation requires two semiconductors with

similar lattice spacing as is the case for AlGaAs and GaAs. The lattice mismatch between Si and Ge is relatively large at 4.2%, and hence it is very difficult to form a hetero-junction between Si and SiGe without the generation of misfit dislocations at the interface [8]. One way of preventing the lattice mismatch is to dope the base with Ge in such a way that there is a gradient between the emitter edge and the collector edge. This also helps reduce the faults in the lattice and traps.

1.2 Overview of silicon-germanium hetero-junction bipolar transistors

The Silicon-Germanium (SiGe) Hetero-junction Bipolar Transistor (HBT) was first demonstrated in 1987 and has been manufactured since 1998 [9]. Ge has a smaller band-gap than Si, which can be used to create the base of a bipolar transistor and an emitter out of Si. This band-gap engineering introduces a new degree of freedom and enables design of a transistor with high base doping and reduced base width along with a reasonable value of gain. In this way, much higher values of cut-off frequency can be achieved with SiGe HBTs than silicon bipolar transistors (Si BJTs) [10]. Figure 1-1 depicts a schematic of a typical NPN type SiGe HBT. It is a vertical type device and the starting substrate is p-type doped silicon. The emitter is made up of poly-silicon with high n-type doping and the base is made up of p-type silicon with germanium doping. The emitter, base and collector contacts are highly doped in order to achieve ohmic contacts (to reduce contact resistance).

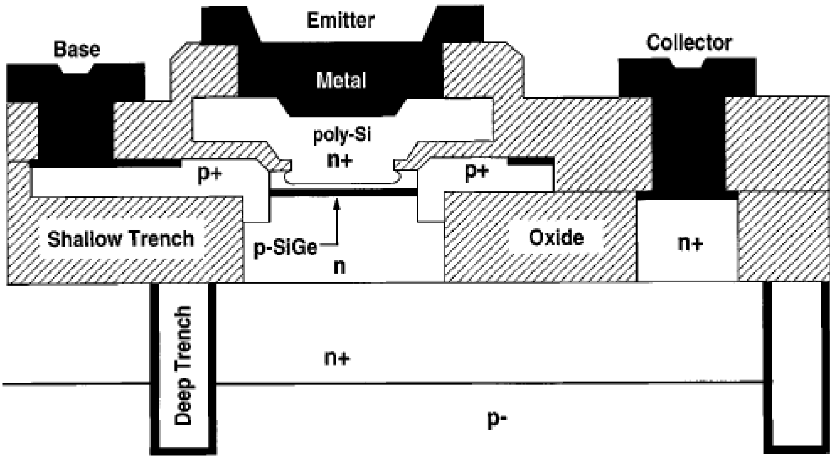

Figure 1-1: A schematic of a typical first generation SiGe HBT (figure not to the scale) [11].

In 2003, SiGe HBTs with a cut-off frequency, f_T, of 350 GHz and a maximum oscillation frequency f_{max} as high as 260 GHz, and with extremely low values of noise figure were demonstrated [8]. In 2008, HBTs designs with cut-off frequency of 508 GHz are given by [12]. Recently, simulation using the TCAD program shows design of SiGe HBT with peak cutoff frequency, f_T, of 1.2 THz [13]. The doping and Ge profiles of such a SiGe HBT are shown in figure 1-2 (a). Here, N_A and N_D represent the acceptor and donor impurity concentration with unit cm^{-3} respectively. The metallurgical base of this HBT is about 7 nm thick and peak acceptor concentration is 2.4×10^{20} cm^{-3}. The plot of peak cutoff frequency with respect to the collector current is shown in figure 1-2 (b). Here, the QS and AC represent the Quasi-Stationary and Alternating Current approaches respectively. The drawback of such a device is low collector/emitter breakdown voltage. More details of this device can be found in [13].

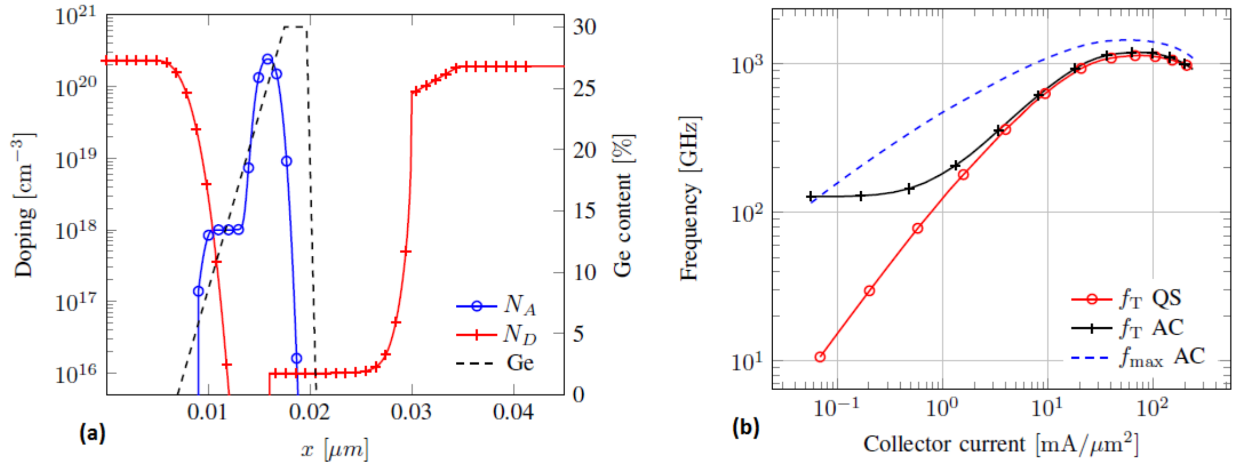

Figure 1-2: (a) Doping and germanium (Ge) profiles of the SiGe HBT. (b) A plot of operating frequency versus the collector current of the SiGe HBT applied with collector-emitter voltage of 1 V and base-emitter voltage of 0.95 V [13].

Traditionally, SiGe has been perceived as an inherently low voltage technology since it was developed for Radio Frequency Integrated Circuit (RFIC) and digital applications. However, SiGe HBTs can obtain the same breakdown voltages as Si BJTs (i.e.: VCBO > 80 V and VCEO > 26 V) for Radio Frequency (RF) applications. Additionally, performance improvements from SiGe in linearity, efficiency and gain for high voltage wireless power applications have been demonstrated. As described previously, SiGe HBTs provides an advantage to obtain high f_T and f_{max} simultaneously, which improves the gain and efficiency over conventional Si BJTs. Also, in SiGe HBTs the base doping is defined by epitaxy and the Early voltage is significantly higher than for a power Si BJT. These factors combine to provide better

linearity for a SiGe HBT compared to a Si BJT. Hence, SiGe can provide good performance at a reasonable cost for circuits such as low-noise amplifiers (LNAs), Power Amplifiers (PAs), mixers, Voltage Controlled Oscillators (VCOs) and Phase Locked-Loops (PLLs). High speed Analog-to-Digital Converters (ADCs) and Digital-to-Analog Converters (DACs) can also be implemented using SiGe HBTs. SiGe process has been also used to develop a highly integrated Digital Enhanced Cordless Telecommunications (DECT) front end, which is in production as a part of a DECT chipset. Here, the front end block includes an LNA in the receive path, a PA for the transmit path and a driver for an external PIN diode switch. In receive mode, the signal is amplified by the LNA with minimal off-chip matching. The high isolation of ~50 dB reduces the Local Oscillator (LO) leakage to the antenna and simplifies the Printed Circuit Board (PCB) design [14]. Other applications include optical communication systems domain in design of WLAN (Wireless Local Area Network) for high bit rate optical networking. RADAR applications has been enabled as well by achieving the performance of III-V devices (e.g.: GaAs etc.) at the cost of silicon bipolar/BiCMOS process. Here, SiGe HBTs are integrated with MOS transistors in a BiCMOS technology, where HBTs will be used in the RF circuits and the MOS transistors in the digital CMOS circuits. BiCMOS technologies incorporating SiGe HBTs are therefore ideally suited for producing RF systems on a single chip [8]. Lastly, the low cost space application due to its robustness with respect to gamma, proton and neutron irradiation has also been demonstrated. Some of the key figures of merit for the evaluation of circuit performance are given below:

(i) The transition frequency (f_T): The transition frequency, f_T, is basically the inverse of the time it takes for an electron to travel from the emitter to the collector contacts. The incorporation of germanium in the base of the silicon transistor has resulted in higher cutoff frequency, f_T. Figure 1-3 (a) shows a plot of the transition frequency (f_T) of a number of HBTs with different Ge base profiles as a function of base width. One of the main factors limiting the base width is the out diffusion of boron doping. This can be reduced by addition of a small amount of carbon to the transistor base region. The shortcomings of reducing the base width are: (i) reduction in breakdown voltage, BV_{CEO} across the device, as demonstrated in figure 1-3 (b) and (ii) if the base region is too thin then it can result in punch through. The advantages of

higher base doping are: (i) reduced base resistance and (ii) reduction in the noise figure of the transistor.

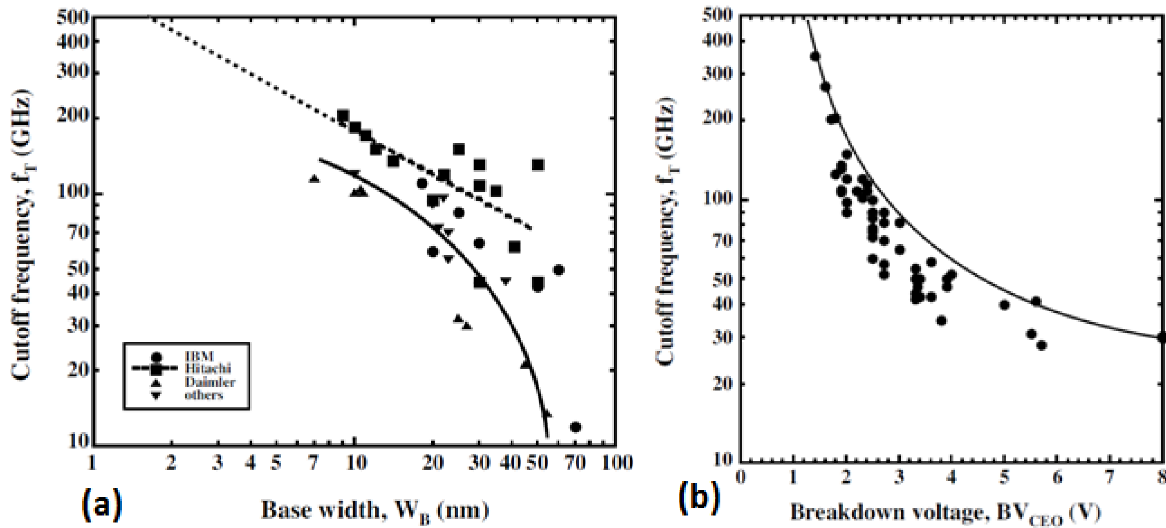

Figure 1-3: (a) A plot of cut-off frequency/transition (f_T) as a function of base width W_B [12]. (b) A plot of cutoff frequency (f_T) as a function of emitter-collector breakdown voltage, BV_{CEO} [12].

The f_T can also be improved by reducing transit delays and *RC* charging delays associated with the device. Reducing the collector region depletion width (W_{DepC}) will reduce the collector transit delay and increases the current density J_C at the Kirk-effect limit ($J_{Kirk} \sim W_{DepC}^{-2}$). This results in increased power dissipation of the device ($P = I_C \cdot V_{CE} + I_B \cdot V_{BE} \sim I_C \cdot V_{CE}$) and raises the device junction temperature. The rise in the junction temperature adversely affects the f_T of the device as shown in figure 1-4. It is apparent from figure 1-4 (a) that for a 50 K rise in the temperature from 300 K, the transition frequency, f_T, of the device degrades from 56 to 30 GHz, a drop of ~46% [15,16].

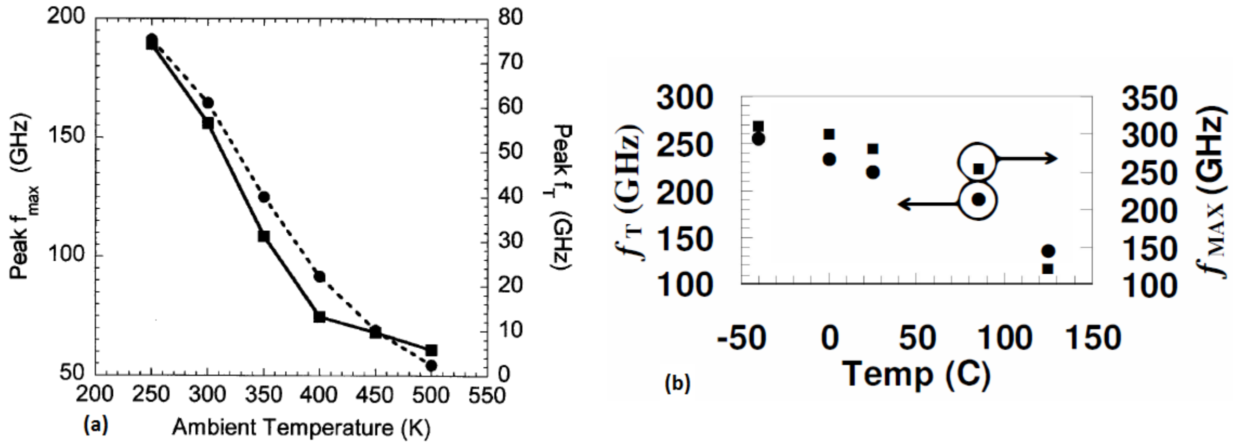

Figure 1-4: The plots of f_T and f_{max} as a function of temperature. (a) Results for a HBT with emitter width of 1.5 µm as reported by [16]. (b) Results for a 130 nm HBT as reported by [15].

(ii) The maximum frequency of oscillation (f_{max}): It is the frequency at which the device power gain equals unity. An ideal oscillator would still be expected to operate up to this frequency. Generally, transistors have useful power gains up to f_{max}, and above that they cannot be used as power amplifiers [17]. It is apparent from figure 1-4 (a) that the maximum frequency of oscillation, f_{max}, of the device degrades from 165 GHz at 300 K to 125 GHz at 350 K which corresponds to a drop of ~24% . The factors that affect the f_T of the device, also affect f_{max}. An additional factor that contributes to the f_{max} degradation is the increase in the extrinsic base resistance due to reduction in the majority carrier mobility at elevated temperatures [16].

(iii) Current gain and bandwidth product (GBWP): It is the product of current gain and frequency bandwidth of the transistor. In a bipolar junction transistor, frequency response declines owing to the internal capacitance of the junctions. The transition frequency varies with collector current as explained earlier, reaching a maximum for some value and declining for a greater or lesser collector current. As an example if the GBWP of an operational amplifier is 1 GHz, it means that the gain of the device falls to unity at 1 GHz. Further, if the maximum frequency of the operation is 100 MHz, then the maximum gain that can be extracted from the device is 10. So, if both f_T and f_{max} are decreased with the increase in temperature the GBWP will also decrease [18].

(iv) Noise performance: The thermal fluctuations of the majority charge carriers in the base induce potential fluctuations in the base, which in turn induce fluctuations of the base and

collector currents. Moreover, the base current near the base/emitter junction induces shot noise [13]. These fluctuations in charge carriers are temperature dependent through various phenomena such as variation in intrinsic carrier concentration, band-gap narrowing and variation in charge carriers' mobilities (holes and electrons). These processes will be discussed in detail in chapters 2 and 3.

Two important figures of merit specifying the noise performance of an amplifier are the Noise Factor (*F*) and Noise Figure (*NF*). The noise factor, *F*, is defined as the ratio of input signal-to-noise ratio to the output signal-to-noise ratio as shown in equation (1.1). The noise figure, *NF*, is the noise factor expressed in dB. Mathematically NF is expressed as shown in equation (1.2).

$$F = \frac{(SNR)_i}{(SNR)_o} = \frac{S_i / N_i}{S_o / N_o} \tag{1.1}$$

$$NF = 10(\log_{10} F) \tag{1.2}$$

where F is the noise factor, $(SNR)_i$ is the input signal to noise ratio, $(SNR)_o$ is the output signal to noise ratio, S_i and S_o are the input and output signal power respectively, N_i and N_o are the input and output noise power respectively and NF is the noise figure. The typical variation of the noise factor with respect to the source resistance in HBTs is shown in figure 1-5 [19]. Here, R_s is the source resistance and it is highly dependent on the device temperature.

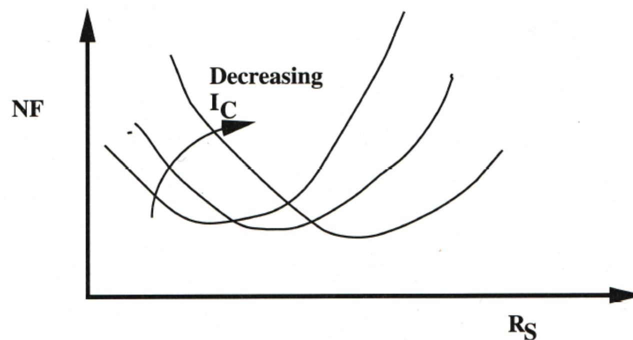

Figure 1-5: The typical trend of noise figure, *NF*, with respect to the source resistance in HBTs [19].

(v) Linearity: A system or device can be termed as linear if it satisfies mathematical conditions of superposition (i.e.: addition, $f(x+y)=f(x)+f(y)$) and homogeneity (i.e.: $f(ax)=a \times f(x)$). Linearity is required for low distortion amplifier output.

(vi) Power efficiency: Power efficiency is the measure of the output signal power, P_{out}, to the input dc power, P_{in}.

$$P_{out} = P_{in} - P_{diss} \tag{1.3}$$

$$\% P_{eff} = \frac{P_{out}}{P_{in}} \times 100 \tag{1.4}$$

where P_{out} is the output power in W, P_{in} is the dc input power in W, P_{diss} is the power lost in the system in form of heat in W and % P_{eff} (also denoted by η) is the power efficiency and since it a ratio of powers it is a unitless quantity.

(vii) Low frequency, 1/*f*, noise: It is also known as flicker noise. The origins of the flicker noise have not been conclusively determined, but a variety of physical mechanisms that can give rise to it have been reported. The possible sources of 1/*f* noise include the fundamental quantum noise generated when electrical charge carriers are scattered by an arbitrary potential. The noise may originate in the bulk material related processes such as the mobility fluctuation of the electrons and the holes. However, 1/*f* noise is more prominent to devices that have carrier conduction on the surface of the device. Any fluctuation in the occupancy of the surface states perturbs the surface recombination velocity, which in turn produce variations in the surface recombination current [20, 21].

All of the figures of merit described above are temperature dependent either directly or indirectly and hence, a thorough understanding of the device temperature is necessary to accurately estimate the device performance. The Joule heating in HBTs has been modeled using the thermal resistance. The purpose of this study is the modeling and characterization of thermal resistance for SiGe HBTs. This allows the instantaneous temperature of the device at each operating point. Thus, the temperature dependent values of all the model parameters are calculated.

1.3 Design of a timing circuit using a phase locked loop

This work is done in collaboration with Physics Department at UT, Arlington along with SLAC National Accelerator Laboratory. The objective of this work is to design a timing circuit to stabilize the ATLAS reference signal of 40 MHz. The ATLAS reference signal has a time jitter which is too large to be

used as the timing signal for the electronics and hence it needs to be stabilized. This is carried out by using a Phase Locked Loop (PLL). The system block diagram, its operation, and the results are discussed in detail in Appendix B.

1.4 Dissertation contributions

Chapter 1 gives the overview of silicon bipolar transistors and its advancement to hetero-junction bipolar transistors with the motivation of this work to perform the thermal characterization of SiGe HBTs.

Chapter 2 discusses the basic device physics fundamentals such as band structure silicon, effect of adding germanium to the silicon, band-gap engineering of SiGe HBTs.

Chapter 3 discusses the impact of temperature rise due to self-heating on the intrinsic carrier concentration, n_i, carrier mobility, μ, conductivity, σ, band-gap narrowing and the carrier saturation velocity, v_{sat}. It also presents a summary of the compact thermal models available to model the self-heating in transistors. A non-linear thermal model that is proposed to accurately model the self-heating is also discussed in this chapter.

In chapter 4 the details of the measurement setups that were used for measurements of SiGe HBTs fabricated by Texas Instruments, Inc. is presented. Also the details about the simulations and optimization procedures are given in this chapter.

The results after optimizations are presented in chapter 5. Various extracted parameters such as junction temperature, current gain, β, and thermal resistance change with respect to the device size is also discussed in this chapter.

Chapter 6 concludes the work in this dissertation with a brief summary of possible future research in this area.

Appendix A contains the additional plots of devices that are related to the chapter 5 results.

Appendix B provides the details of the timing circuit design using a PLL. Here, the block diagram of the system as well as the individual blocks is presented along with the theory explaining each of the building blocks. It is concluded with the results and discussions.

Chapter 2

DEVICE PHYSICS of SILICON and SiGe TRANSISTORS

2.1 Band structure of Si BJT

Before discussing SiGe HBTs in detail it would be useful to discuss and summarize the main parameters in a silicon bipolar transistor and also how these need to be optimized for specific applications. Practically, all the high speed bipolar transistors used in digital circuits are of vertical NPN type. Hence, transistors with this geometry only will be discussed.

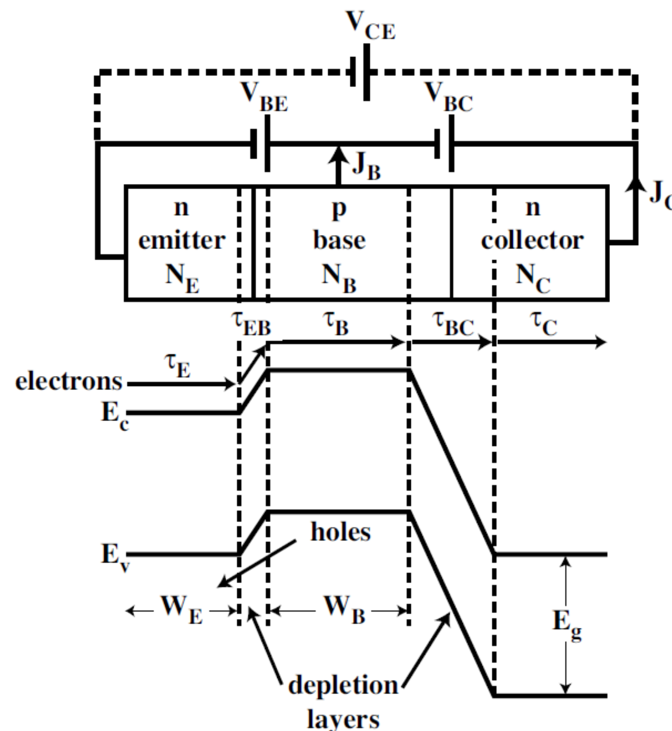

Figure 2-1: The band structure of a Si Bipolar Junction Transistor (BJT) with bias and defining major parameters [9].

Figure 2-1 shows a typical NPN bipolar transistor under forward active bias conditions. Here, the base-emitter junction is forward biased with voltage, V_{BE}, and the base-collector junction is reverse biased with voltage, V_{BC}. The forward biased base-emitter junction causes the electrons to flow (diffuse) from the emitter to the base and the holes from the base to the emitter. Those electrons which do not recombine in the base region are swept into the collector giving rise to the collector current density as given in (2.1).

$$J_C = \frac{qD_{nB}n_i^2}{W_B N_B} \exp\left[\frac{-\Delta E_b}{k_B T}\right] \exp[\frac{qV_{BE}}{k_B T} - 1] \quad (2.1)$$

where q is the electronic charge, n_i is the intrinsic carrier density, W_B is the base width, D_{nB} is the minority carrier electron diffusion constant in the base, ΔE_b is the reduction in the band-gap of the base due to the heavy doping effect for a heterojunction such as in SiGe transistors, k_B is the Boltzmann constant and T refers to the temperature. Thermal voltage, V_t is defined as $k_B \cdot T/q$ in Volts.

The base current density that flows is calculated as shown in (2.2).

$$J_B = \frac{qD_{pE}n_{ieE}^2}{N_E W_E} exp[\frac{qV_{BE}}{k_B T}] \quad (2.2)$$

where N_E is the donor concentration in the emitter of width, W_E. The common emitter current gain of the transistor is obtained by dividing the collector current density by the base current density and is given in (2.3) assuming: (i) $\exp(q \cdot V_{BE}/k_B \cdot T) - 1) \approx \exp(q \cdot V_{BE}/k_B \cdot T)$ and (ii) $n_{ieE}^2 \approx n_i^2$.

$$\beta = \frac{J_c}{J_B} = \frac{D_{nB}N_E W_E}{D_{pE}N_B W_B} \exp[\frac{-\Delta E_b}{k_B T}] \quad (2.3)$$

The Early voltage relates the collector current density on the base-collector, V_{CB}, voltage (held constant) and is defined as shown in (2.4).

$$V_A = J_C \frac{\partial V_{CE}}{\partial J_C} - V_{CE} \approx J_C \frac{\partial V_{CE}}{\partial J_C} \quad (2.4)$$

For a base with uniform doping the Early voltage reduces to a linear dependence with the base width as shown in expression (2.5).

$$V_A = \frac{qW_B N_B}{C_{BC}} \quad (2.5)$$

The parameter that affects the speed of the transistor and circuit is the transit frequency, f_T. The transit frequency, f_T, is basically the inverse of the time it takes for an electron to travel from the emitter to the collector contacts. If the transversal times for emitter, base, collector, base-emitter junction and base-

collector junction are defined as τ_E, τ_B, τ_C, τ_{BE} and τ_{BC} respectively then the transit frequency can be given as shown in (2.6).

$$f_T = \frac{1}{2\pi\,(\tau_E+\tau_B+\tau_C+\tau_{BE}+\tau_{BC})} \approx \frac{1}{2\,\pi\,(\tau_B+\tau_E)} \tag{2.6}$$

In modern day transistors it is only the emitter transit time, τ_E and the base transit time, τ_B which make significant contribution to the transit frequency. From the uniform band-gap approximation with uniform base doping, τ_B can be approximated as,

$$\tau_B = \frac{W_B^2}{2D_{nB}} \tag{2.7}$$

Hence, the easiest way to reduce the base transit time is to reduce the base width. The other parameter that also characterizes the speed of the transistor is the maximum frequency of oscillation which can be defined as:

$$f_{max} = \sqrt{\frac{f_T}{8\pi R_B C_{BC}}} \tag{2.8}$$

The capacitance term in the denominator indicates that f_{max} is susceptible to parasitic capacitances which in turn points to reducing the base-collector area in order to increase f_{max}. The other two ways to increase f_{max} is to either increase f_T or to reduce the base resistance, R_B.

2.2 Band structure of SiGe HBT

There are two methods for adding germanium, Ge, to the base of the bipolar transistor for HBTs. The first is a rectangular/box Ge base profile which was pioneered by Daimler-Chrysler and the other is a linearly graded Ge base profile which was pioneered by IBM. The linearly graded base provides a built in electric field which accelerates the electrons across the base region. In such a device construction, the Ge content near the metallurgical collector-base (CB) junction, and then rapidly ramped back down to 0% Ge. The three main designs for a Ge base profile for SiGe HBTs are shown in figure 2-2 [9]. Each of the Ge profiles changes the transistor parameters in different ways and in turn produces different enhancements. Even though the band offsets in SiGe HBTs are typically small compared to III-V

technology standards the Ge grading over the short distance of the neutral base results in large electric fields. For instance, a linearly graded Ge profile with a modest peak Ge content of 10%, graded over a 50-nm base width results in 75 mV/50 nm = 15 kV/cm electric field. This high electric field is sufficient enough to accelerate the electrons to its saturation velocity (v_{sat} = 10^7 cm/sec). Because the base transit time and parasitic capacitance (shorter base width results in higher base capacitance per unit area) typically limits the frequency response of a Si transistor, the introduction of Ge in the base results in Ge-induced drift field resulting in improved frequency response [1].

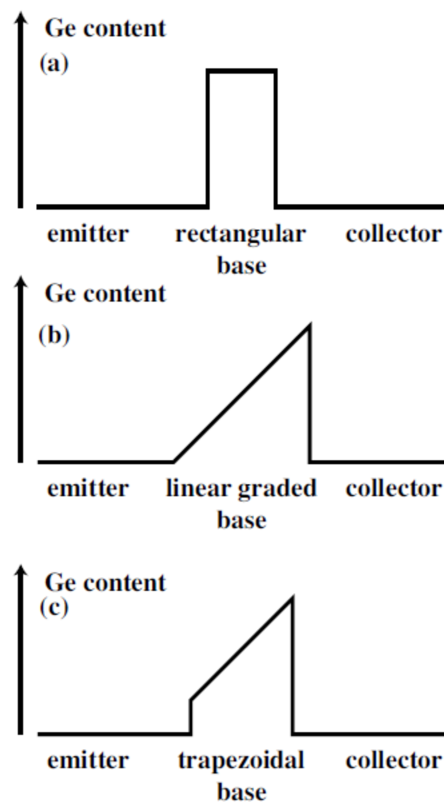

Figure 2-2: The three main designs for Ge base profile for SiGe HBTs. (a) A rectangular or box SiGe box, (b) a linearly graded base and (c) a trapezoidal base HBT [9].

For an HBT with rectangular Ge base profile, the parameters like the carrier density in the base, collector current density, gain, gain-Early voltage product and emitter transit time are all enhanced by a factor, $exp[\Delta E_g/k_B T]$ where the change in band-gap, ΔE_g as a function of Ge content, at a given distance, x (where: $0 < x < W_B$) is given as shown in (2.9) [1].

$$\Delta E_g = 0.0206x^2 - 0.43x \quad [\text{eV}] \tag{2.9}$$

It should be noted here that base transit time for a rectangular Ge base profile is not reduced as much as for the linearly graded Ge profile. The increased gain and collector current can be traded off for higher base doping to get thinner base widths and reduced base resistance for reduced base transit time resulting in an increase in f_T and f_{max}.

Each of the Ge profiles changes the above discussed parameters in different ways. For a npn-type SiGe HBT it is inferred from figure 2-3 that introduction of Ge into base region has two main consequences: (i) the potential barrier to the injection of electrons from emitter region to the base region is decreased. SiGe HBTs also provide a higher energy barrier ΔE_v to holes injected from the p-base region into the n-emitter as compared to the electrons injection from the emitter into the base [22]. This will result in exponentially more electron injection for the same applied V_{BE}, translating into higher collector current, and hence higher current gain, provided the base current remains unchanged. Of practical consequence, the introduction of Ge effectively decouples the current gain from base doping, thereby providing circuit designers with greater flexibility than in Si BJT design. For example, if the intended circuit application does not require high current gain then it can be effectively traded for a high base doping level, leading to lower base resistance and hence better dynamic switching and noise characteristics. (ii) The presence of the Ge content in the CB junction will positively influence the output conductance of the transistor, resulting in a higher Early voltage.

A rectangular base profile will have a different effect on these parameters when compared to linearly graded base profile and produce different enhancements. Figure 2-3 (a) shows the band structure modification due to rectangular base profile where the conduction band height has been reduced in the base resulting in an increase in the collector current density. As it can be seen from figure 2-3, the introduction of Ge into the base region has two dc consequences: (i) it is important to realize that the difference in the band-gap energy, ΔE_g, between the emitter and the base is almost completely absorbed by a lowering of the conduction band edge. Compared with a silicon BJT, this implies that electrons have to overcome a much lower energy barrier when being injected from the emitter into the base whereas holes will face the same energy barrier in both cases when diffusing from the base into the emitter [23].

This will yield exponentially more electron injection for the same base-emitter voltage, V_{BE}, resulting in higher collector current and gain. (ii) The presence of Ge in the base region will positively influence the output conductance of the transistor resulting in higher Early voltage.

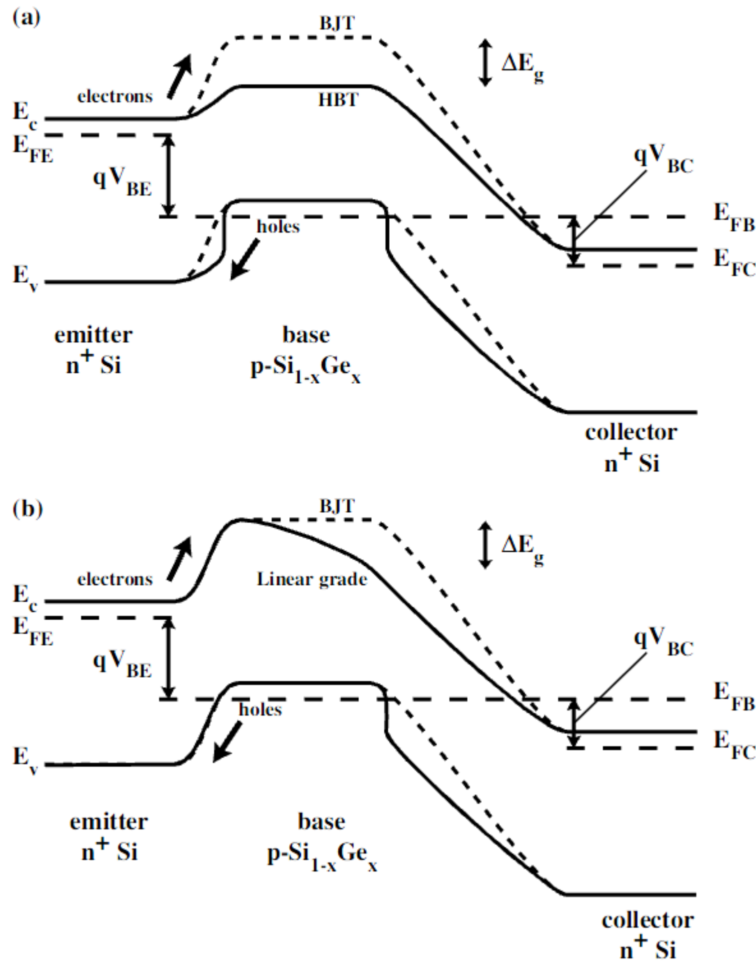

Figure 2-3: (a) Band structure for npn BJT and a rectangular Ge base profile in a npn HBT. (b) Band structure for a npn BJT with a linearly graded Ge base profile [9].

For the linearly graded base profile, the conduction band slope provides a built-in electric field that accelerates the carriers across the base and hence reducing the base transit time. A full list of all the enhancements for a SiGe HBTs compared to a Si BJT for the major device parameters are shown in table 2.1.

Table 2-1: A TABLE SUMMARIZING THE CHANGES TO THE MAIN BIPOLAR PARAMETERS FOR DIFFERENT GE BASE PROFILES [9].

Parameter	SiGe HBT	Linear graded SiGe base
$\frac{n_{iB}^2(\mathrm{SiGe})}{n_{iB}^2(\mathrm{Si})}$	$\exp\left[\frac{\Delta E_g}{k_B T}\right]$	$\exp\left[\frac{\Delta E_g}{k_B T}\frac{z}{W_B}\right]$
$\frac{J_C(\mathrm{SiGe})}{J_C(\mathrm{Si})}$	$\exp\left[\frac{\Delta E_g}{k_B T}\right]$	$\frac{\Delta E_g}{k_B T\left(1-\exp\left[\frac{-\Delta E_g}{k_B T}\right]\right)}$
$\frac{\beta(\mathrm{SiGe})}{\beta(\mathrm{Si})}$	$\exp\left[\frac{\Delta E_g}{k_B T}\right]$	$\frac{\Delta E_g}{k_B T\left(1-\exp\left[\frac{-\Delta E_g}{k_B T}\right]\right)}$
$\frac{V_A(\mathrm{SiGe})}{V_A(\mathrm{Si})}$	1	$\frac{k_B T}{\Delta E_g}\left(\exp\left[\frac{\Delta E_g}{k_B T}\right]-1\right)$
$\frac{\beta(\mathrm{SiGe})V_A(\mathrm{SiGe})}{\beta(\mathrm{Si})V_A(\mathrm{Si})}$	$\exp\left[\frac{\Delta E_g}{k_B T}\right]$	$\exp\left[\frac{\Delta E_g}{k_B T}\right]$
$\frac{\tau_B(\mathrm{SiGe})}{\tau_B(\mathrm{Si})}$	1	$\frac{2k_B T}{\Delta E_g}\left(1-\frac{k_B T}{\Delta E_g}\left(1-\exp\left[\frac{\Delta E_g}{k_B T}\right]\right)\right)$
$\frac{\tau_E(\mathrm{SiGe})}{\tau_E(\mathrm{Si})}$	$\sim\exp\left[\frac{\Delta E_g}{k_B T}\right]$	$\sim\frac{k_B T}{\Delta E_g}\left(1-\exp\left[\frac{\Delta E_g}{k_B T}\right]\right)$

2.2.1 Effects of germanium addition on the device parameters

In this section a brief comparison of the differences between a comparably constructed SiGe HBT and a Si BJT is presented in terms of various device parameters.

2.2.1.1 Current Gain (*β*)

The presence of any Ge, in whatever profile in the base of the bipolar transistor will enhance the collector current density (J_C) at fixed base-emitter voltage over a comparably constructed Si BJT. Hence current gain for a HBT will be greater than a BJT. The J_C enhancement depends exponentially on the value of Ge-induced band offset at the EB boundary and linearly on the Ge grading across the base.

2.2.1.2 Output Conductance

The dynamic output conductance ($\partial I_C/\partial V_{CE}$ at a fixed V_{BE}) of a transistor is an important design parameter for many analog circuits. A circuit designer will expect to have ideally infinite output resistance that is zero output conductance or in other words, the output current to be independent of the output voltage. But in practice this is never the case. As the collector-base (V_{CB}) is increased the neutral base boundary (x = W_b) shifts decreasing the base width. Since the W_B determines the minority carrier density on the CB side of the neutral base, a decrease in W_B results in the increase of the collector current. Thus, I_C must increase as V_{CB} increases, resulting in a non-zero output conductance. This mechanism is known as the "Early effect" expressed as V_A [1]. Mathematically it is expressed as shown in equation 2.10. The Early voltage is a simple and convenient measure of the change in output conductance with respect to V_{CB}. Early voltage for a silicon transistor can be re-written in terms of base width, W_B as [1],

$$V_{A,Si} = -W_B(0)\cdot\left\{\left.\frac{\partial W_B}{\partial V_{CB}}\right|_{V_{BE}}\right\}^{-1} \tag{2.10}$$

where $W_B(0)$ is the neutral base width at V_{CB} = 0 V. The dependence of base width on voltage and doping can be calculated using equation 2.12 [1].

$$W_B \approx W_m - \sqrt{\left(\frac{2\varepsilon}{q}\right)\cdot\left(\phi_{bi} + V_{CB}\right)\cdot\left\{\frac{N_{DC}^{+}}{N_{AB}^{-}\cdot\left(N_{AB}^{-} + N_{DC}^{+}\right)}\right\}} \tag{2.11}$$

where W_m is the metallurgical base width, ϕ_{bi} is the CB junction built-in voltage, N_{DC}^{+} is the ionized donor doping concentration in the collector and N_{AB}^{-} is the ionized acceptor doping concentration in the base.

In real Si BJT designs, circuit requirements determine the collector-to-emitter breakdown voltage (BV_{CEO}) and so the device has to be doped accordingly. To first order, BV_{CEO} sets the collector doping level. Higher values for the Early voltage can be achieved by setting the collector doping low, but this will decrease the current gain (β) considerably. Or by increasing the acceptor doping in the base to increase the Early voltage will result in a strong decrease in β. In addition, for a Si BJT, for a fixed base width, increasing base doping will degrade the cutoff frequency of the transistor (due to reduction in minority

carrier mobility and recombination in the base). Hence it is difficult in a Si BJT to simultaneously obtain high V_A, high β and high f_T. The introduction of Ge into the base of the transistor can help mitigate this constraint by decoupling β and V_A from the base doping profile. The base profile is weighted such that the Ge content on the collector side of the neutral base is higher, making it harder to deplete the neutral base for a given applied V_{CB}. If all other conditions are the same then this will effectively increase the Early voltage of the transistor. For a linearly graded Ge profile the final result is that the V_A ratio between a SiGe HBT and a Si BJT is an exponential function of Ge-induced band-gap grading across the neutral base [1].

2.2.1.3 Current gain – Early voltage product

Current gain – Early voltage product, $\beta \cdot V_A$, is a thermally activated function of two factors: (i) the Ge induced band offset at the EB junction and (ii) the Ge induced grading across the neutral base. The $\beta \cdot V_A$ in a SiGe HBT is significantly improved over a comparable Si BJT, regardless of the Ge profile in the base, although the triangular Ge profile is preferred over other profiles for both V_A and $\beta \cdot V_A$ optimizations. Due to their thermally activated nature, both V_A and $\beta \cdot V_A$ can be strongly increased with cooling, resulting in $\beta \cdot V_A$ > 104 at 77 K for a 10% Ge triangular profile [24]. The observations that can be made regarding the effects of Ge on $\beta \cdot V_A$ are:

(i) The presence of larger Ge content on the CB side of the neutral base than at the EB side of the neutral base will enhance the Early voltage at a fixed V_{BE} over a comparable Si BJT. This increases the $\beta \cdot V_A$ product.

(ii) The V_A enhancement depends exponentially on the Ge doping across the base. This behavior strongly favors the graded (triangular) Ge profile.

(iii) The Ge-induced V_A enhancement is thermally activated since it is exponentially dependent on the inverse of temperature and thus cooling will result in strong increase of the V_A.

(iv) As β and V_A have exact opposite dependence on Ge grading and the emitter-base Ge offset, the $\beta \cdot V_A$ product is an ideal win-win scenario for a SiGe HBT. Introduction of Ge into the base region of the transistor will exponentially enhance the $\beta \cdot V_A$, an important figure-of-merit for analog circuit designers.

1.2.2.4 Charge modulation effects

At the fundamental level for both the BJT and the Field-Effect Transistor (FET), the transistor action takes place by the voltage modulation of charges that in turn lead to voltage modulation of the output current. The voltage modulation of charges results in a capacitive current which increases with frequency. Various charge storage effects in the intrinsic and extrinsic device structure limits the bandwidth of the transistor. The solution of semiconductor transport equations needs to be carried out in the frequency domain in order to obtain the exact analysis of charge storage equations. Generally charge storage effects are analyzed by assuming that under the dynamic operation (i.e.: the quasi-static assumption) the charge distributions instantly follows the changes in the terminal voltages. The two important charge modulation effects in a transistor are described below:

(i) The modulation of space charges associated with the EB and the CB junctions – Voltages changes across the EB and CB junctions lead to changes of the depletion layer widths and hence the total space charge. The capacitive behavior is similar to that of a parallel plate capacitor, since the changes in charge occur at the opposite layers of the depletion region to the neutral region transition boundaries.

   a. Under high injection conditions, the modulation of charges in the depletion region becomes significant. The resulting capacitance is referred to as the "transition" capacitance and is important for the forward biased EB junction. At high injection levels the CB capacitance is a function of the collector current because of the charge compensation by mobile carriers and base push out effect.

   b. Under low injection conditions, the CB capacitance is a function of CB biasing voltage, and its value is similar to that of a reverse biased p-n junction.

(ii) Modulation effect due to injected minority carriers in the neutral base and emitter regions – In the base region, an equal amount of excess majority carriers are induced by the injected minority carriers to maintain charge neutrality. Both the minority and majority carriers respond to the EB voltage changes which contribute to the EB capacitance. The capacitance due to the minority carriers diffusing into the base region from emitter region is called "diffusion" capacitance.

High injection occurs when the minority carrier density in the base is equal to or larger than the base doping density. Any further increase in the minority carrier density will then result in an almost equal increase in the majority carrier density in order to maintain quasi-neutrality in the base. A gradient of majority carriers is caused which is equal to the gradient of the minority carrier density. This gradient causes a built-in electric field, which in turn reduces the base transit time of the minority carriers. This effect is referred to as Webster effect. In order to achieve the transistor action, modulation of output current with respect to change in input voltage is required. The modulation of charge is a way of modulating the current and it must be minimized to maintain ideal transistor action at high frequencies. For example, a large EB diffusion capacitance causes a large input current, which increases with frequency, resulting in a decreased current gain at higher frequencies. Hence, for a given output current modulation, a decreased amount of charge modulation will result in higher device operating frequency. The figure-of-merit for the efficiency of transistor action is the ratio of the total charge modulation to the total output current modulation and mathematically this is expressed as (2.12).

$$\tau_{\mathrm{EC}} = \frac{\partial Q_{\mathrm{n}}}{\partial I_{\mathrm{C}}} \tag{2.12}$$

where τ_{EC} or τ_B is called the transit time for an electron to travel from emitter to collector junctions for a NPN transistor, and Q_n is the electron charge across the whole device. The use of the relation $\tau_{EC} = Q_n/I_c$ is non-physical and incorrect, since it produces a transit time that is independent of charge modulation (i.e.: assumes constant base doping profile). Equation (2.12) can be re-written as (2.13) using the base-emitter voltage as an intermediate variable.

$$\tau_{\mathrm{EC}} = \frac{\partial Q_{\mathrm{n}} / \partial V_{\mathrm{BE}}}{\partial I_{\mathrm{C}} / \partial V_{\mathrm{BE}}} = \frac{g_{\mathrm{m}}}{C_{\mathrm{i}}} \tag{2.13}$$

where C_i is the input capacitance in Farads and g_m is the transconductance in Ampere/Volt. C_i can be divided into two components as: $C_{BE} = \partial Q_n/\partial V_{BE}$ and $C_{BC} = \partial Q_n/\partial V_{BC}$. The transit times related to the emitter and neutral base are called the emitter transit time and the base transit time respectively. The base charge modulation required to produced a given amount of output current modulation can be decreased by introducing a drift field (e.g.: Ge grading), which will in turn reduce the base transit time

thereby increases the device operating frequency. This Ge-grading induced reduction in charge reduction is the fundamental reason of SiGe HBTs having better frequency response compared to their bipolar counterparts. Base grading is a convenient way to reduce the base charge modulation [1].

2.2.1.5 Unity gain cut-off frequency and maximum oscillation frequency

For low level carrier injection, the unity-gain cut-off frequency, f_T, of a SiGe HBT can be expressed as given in (2.14).

$$f_T = \frac{1}{2\pi\tau_{EC}} = \frac{1}{2\pi}\left[\frac{kT}{q \cdot I_C}(C_{tE} + C_{tC}) + \tau_B + \tau_E + \frac{W_{CB}}{2v_{sat}} + r_C \cdot C_{tC}\right]^{-1} \tag{2.14}$$

where $g_m = qI_C/kT$ is the intrinsic transconductance at low level injection ($g_m = \partial I_C/\partial V_{BE}$), C_{tE} and C_{tC} are the EB and CB depletion capacitances, τ_B is the neutral base transit time, τ_E is the emitter region charge storage delay time, v_{sat} is the saturation velocity, W_{CB} is the width of the CB depletion region, and r_C is the dynamic collector resistance. Physically, f_T is the common-emitter, unity gain cut-off frequency, and it is measured using S-parameter techniques. In equation (2.14), τ_{EC} is the total emitter-to-collector delay time, and it sets the ultimate limit of the switching speed of a transistor. Thus, improvements in τ_B and τ_E for fixed bias current in SiGe HBT results in enhancement of f_T and f_{max} of the device. In terms of transistor power gain where the transistor is used to drive a load, the maximum oscillation frequency, f_{max}, is defined as:

$$f_{\max} = \sqrt{\frac{f_T}{8\pi \cdot C_{BC} \cdot r_B}} \tag{2.15}$$

where r_B is the small signal base resistance and C_{BC} is the total CB depletion capacitance. Physically, f_{max} is the common-emitter, unity power gain frequency and it is measured using S-parameter techniques. Since power gain not only depends on the intrinsic transistor performance (i.e.: device transit times), but also on the device parasitic capacitance associated with the process technology and its structure. The maximum operation frequency, f_{max}, is typically more of a concern to circuit designers. A larger f_T, a smaller r_B and C_{BC} are desired to obtain maximum power gain and higher circuit operating frequency [1].

1.2.2.6 Base and emitter transit times

The base transit time and the emitter transit time influence the dynamic response of the SiGe HBT. Equation (2.16) shows the comparison of base transit time of a SiGe HBT with Si BJT of identical size [1].

$$\frac{\tau_{b.SiGe}}{\tau_{b.Si}} \propto \frac{kT}{\Delta E_{g,Ge(grade)}} \left\{ 1 - \frac{kT}{\Delta E_{g,Ge(grade)}} \left[1 - e^{-\Delta E_{g,Ge(grade)}/kT} \right] \right\} \tag{2.16}$$

Several observations can be made from equation (2.16) [1]:

(i) For fixed bias current, the presence of Ge in the base region affects the frequency response of the device through the base and emitter transit times.

(ii) The grading-induced drift field aids minority carrier transport resulting in a f_T enhancement of the device.

(iii) A triangular Ge profile is better for cutoff frequency enhancement whereas a box Ge profile favors β enhancements where all other device parameters are the same. Lastly, the trapezoidal Ge profile favors both τ_b and τ_e improvement in a device. Such tradeoffs are generally technology generation dependent.

(iv) The Ge induced f_T enhancement strongly depends on temperature and for τ_b and τ_e, will produce f_T enhancement with cooling which is in stark contrast to a Si BJT.

Since, f_T is increased across a large range of collector current, substantial savings in power dissipation for fixed frequency operation compared to a Si BJT can be obtained.

2.2.1.7 Operating current density versus speed

In order to achieve high speed, high operating current density is required for SiGe HBTs. This is apparent from the figure 2-4. The operating current density dependence of f_T is given in (2.17) [1].

$$2\pi \cdot f_T = \frac{g_m}{C_{BE} + C_{BC}} \tag{2.17}$$

where $C_{BE} = g_m \cdot \tau_f + C_{tE}$, $C_{BC} = C_{tC}$ and $g_m = I_C/V_t$. Using these relationships (2.17) can be re-written as,

$$2\pi \cdot f_{\mathrm{T}} = \frac{I_{\mathrm{C}}}{V_{\mathrm{t}}} \cdot \frac{1}{g_{\mathrm{m}} \cdot \tau_{\mathrm{f}} + C_{\mathrm{tE}} + C_{\mathrm{tC}}} \tag{2.18}$$

$$2\pi \cdot f_{\mathrm{T}} = \frac{I_{\mathrm{C}}}{V_{\mathrm{t}}} \cdot \frac{1}{\frac{I_{\mathrm{C}}}{V_{\mathrm{t}}} \cdot \tau_{\mathrm{f}} + C_{\mathrm{t}}} = \frac{I_{\mathrm{C}}}{V_{\mathrm{t}}} \cdot \frac{V_{\mathrm{t}}}{I_{\mathrm{C}} \cdot \tau_{\mathrm{f}} + C_{\mathrm{t}} \cdot V_{\mathrm{t}}} = \frac{1}{\tau_{\mathrm{f}}} + \frac{I_{\mathrm{C}}}{C_{\mathrm{t}} \cdot V_{\mathrm{t}}} \tag{2.19}$$

where $C_t = C_{tE} + C_{tC}$. Since both the capacitances C_{tE} and C_{tC} are dependent on emitter area and so does the current, I_C. Equation (2.19) can be re-written as equation (2.20) where $J_C = I_C/A_E$ and $C_t = C_t^{'}/A_E$.

$$f_{\mathrm{T}} = \frac{1}{2\pi}\left[\frac{1}{\tau_{\mathrm{f}}} + \frac{J_{\mathrm{C}}}{C_{\mathrm{t}}^{'} \cdot V_{\mathrm{t}}}\right] \tag{2.20}$$

Thus, the cut-off frequency is independent of emitter area and it can be determined by the biasing current density. The values of τ_f and $C_t^{'}$ can be conveniently extracted from a plot of $1/2\pi f_T$ versus $1/J_C$ as shown in figure 2-4. The $1/2\pi f_T$ versus $1/J_C$ curve is nearly linear near the peak f_T, indicating that $C_t^{'}$ is close to constant for this biasing range at high f_T. Thus, τ_f can be determined from the y-axis intercept at infinite current ($1/J_C = 0$) and C_t from the slope of the curve. For very low J_C values the term $1/\tau_f$ is large enough to result in lower values of f_T. By increasing J_C, the effect of a first term ($1/\tau_f$) is smaller and higher cut-off frequency can be achieved [1].

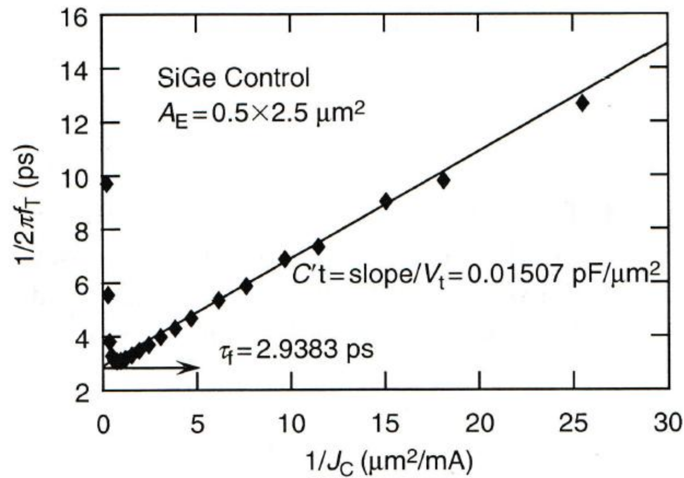

Figure 2-4: Plot of forward transit time versus inverse of current density, J_C [1].

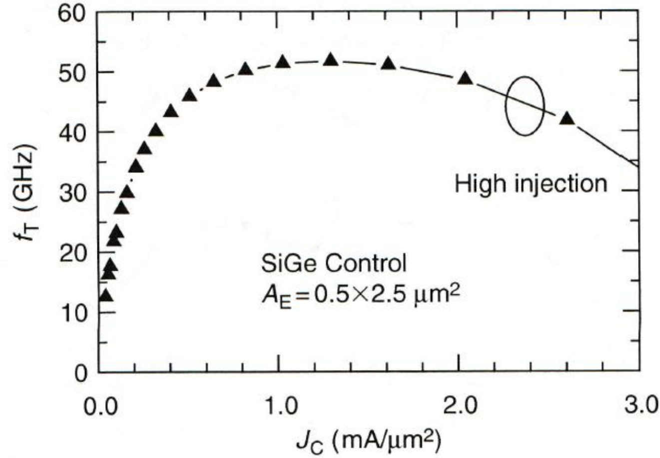

Figure 2-5: Plot of f_T versus current density, J_C for a first generation SiGe HBT technology [1].

At very high injection where J_C is very large, base push out due to the Kirk effect occurs where τ_f itself increases leading to the f_T roll-off as shown in figure 2-5. To improve f_T in a SiGe HBT, either τ_f must be decreased (by vertical profile scaling and Ge grading across the base) or J_C must be increased in proportion in order to make the second term larger compared to the first term (τ_f). Thus, to obtain high f_T for a transistor with small τ_f, sufficiently high current densities are required. This is the fundamental design criterion for high-speed SiGe HBTs. The higher the peak f_T, higher is the required current density, J_C (until the high injection effects limit the f_T). For example, for the first generation SiGe HBT with 50 GHz peak frequency, it operates at J_C of 1 mA/μm^2 while the third generation SiGe HBTs operates at 10 to 15 mA/μm^2 having a peak f_T > 200 GHz. Higher current density operation leads to more severe self-heating effects, which needs to be taken into account for compact modeling and circuit design. Electro-migration and other reliability constraints associated with very high J_C operating conditions require copper metallization [1].

The collector doping must be increased in order to delay the onset of high injection effects in order to maintain proper transistor action under high J_C conditions. This need of high doping for the collector reduces the device breakdown voltage. Hence, a trade-off between breakdown voltage and speed are inevitable for all bipolar transistors. Both C_{tE} and C_{tC} must be minimized in the device and are usually addressed via a combination of structural design and doping profile tailoring. This reduction of C_{tC} is also critical for increasing the power gain (i.e.: f_{max}). Clearly, breakdown voltage must decrease as the

transistor performance improves. Achievable f_T x BV_{CEO} product in the 350 – 400 GHz·V range are realistic goals [1].

2.2.2 Second-order effects

The first-order effects presented in section 2.2.1 are prone to deviate due to second-order effects which has impact on actual SiGe HBT devices and circuits is both profile and application dependent. In this section, second-order effects such as: (i) The effects of Ge depends on the location of the Ge in the base. The movement of emitter-base-depletion region along the graded Ge profile with increase in base-emitter voltage is responsible to influence and exemplify the Ge grading effect in SiGe HBTs. This Ge grading effect can present potential problems for circuit designs that require control over the current dependence of current gain and base-emitter voltage as a function of temperature. (ii) Neutral base recombination (NBR) is the effect that depends on finite trap density in the base region. It is assumed to be negligible in a Si BJT but it is important for a Si HBT particularly when the devices are operated across a wide temperature range. NBR can strongly affect the Early voltage (hence, output conductance) of SiGe HBTs and it is dependent on the type (mode) of base biasing (i.e.: whether the device is current-driven or voltage-driven), and hence the circuit application. (iii) Lastly, the high injection Heterojunction Barrier Effects (HBE) is the effect that takes place when the base-collector junction is operating under high current density. If this effect is not controlled then it can strongly degrade both the dc and ac performance at large current densities which SiGe HBT often have [1].

2.2.2.1 Ge Grading Effect

Parameter stability over temperature and applied bias is crucial for SiGe HBT applications. Temperature dependence of the collector current and the current gain for a typical SiGe HBT is shown in figure 2-4. For a graded base SiGe HBT, the current gain peaks at low injection and degrades significantly before the onset of high injection effects. The collapse of the current gain, β, in the medium-injection region is a result of a band-edge phenomenon. The physical origin of this bias dependent behavior of current gain in a SiGe HBT stems from the collector current dependence on bias and the Ge profile in base. The collector current at any applied bias is exponentially dependent upon the amount of Ge at the edge of the emitter-base (EB) depletion region. Physically, as the collector current density

increases, the V_{BE} must also increase, and hence from charge balance considerations the EB depletion region width contracts. This in turn reduces the Ge content at the EB boundary because depletion boundary moves which changes the band-gap from $\Delta E_{g,Ge(x)}$ to $\Delta E_{g,Ge(0)}$ as shown in figure 2-4 (b).

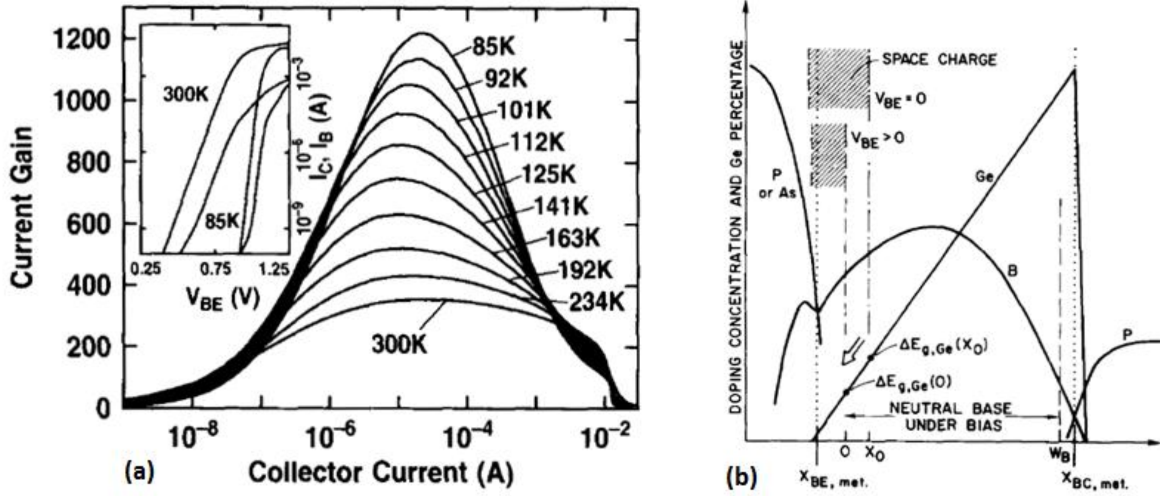

Figure 2-6: (a) Temperature dependence of the collector current and the current gain of a graded SiGe HBT. The current-voltage (*I*-*V*) characteristics at 300 K and 85 K are shown in the inset. (b) Schematic diagram of the emitter-base (EB) depletion region and its bias dependence [25].

The relationship of the collector current density with the Ge profile in a SiGe HBT is expressed in equation (2.21) [1].

$$J_{C,SiGe} \cong \frac{q \times D_{nb}}{N_{ab}^{-} \times W_b} \times \left(e^{V_{BE}/V_t} - 1\right) \times n_i^2 \times e^{\Delta E_{gb}/KT} \times \left\{\gamma \cdot \tilde{\eta} \cdot \frac{\Delta E_{g,Ge}(grade)}{KT} \cdot e^{\Delta E_{g,Ge}(0)/KT}\right\} \quad (2.21)$$

where, ΔE_{gb} is the heavy doping induced apparent band-gap narrowing in the base region, $\tilde{\eta}$ is the minority electron diffusivity ratio between SiGe and Si, γ is the position averaged "effective density of states ratio" between SiGe and Si, D_{nb} is the electron diffusion constant in the base, $\Delta E_{g,Ge}(0)$ is the Ge induced band offset at x=0, n_i^2 is the low doping intrinsic carrier density for Si and N_{ab}^{-} is the donor doping concentration in base region. Since $\Delta E_{g,Ge}(0)$ changes with increasing base-emitter bias, any changes in the amount of Ge due to EB boundary modification will have a large impact due to the exponential relationship. Hence, a more serious Ge grading effect will be observed for a more strongly graded Ge profile. Also by decreasing the $\Delta E_{g,Ge}$(grade) (i.e.: Ge grading profile), the Ge grading effect becomes negligible, resulting in a flat β versus I_C, as seen in a Si BJT. Finally, it is observed that due to the band

edge nature of the Ge grading effect, its impact on device performance is greatly magnified at reduced temperature [1]. Ge grading effects can be summarized as below:

(i) The Ge grading effect is more important in precision analog circuits compared to digital or RF/microwave circuits. Any analog circuit that depends strongly on current gain across a wide base range, or the one that requires the matching of V_{BE} between multiple devices across both the applied bias and temperature, could be potentially affected.

(ii) The Ge graded profile designs typically achieve the best ac and dc performance, and thus it is applied to the vast majority of commercially available SiGe devices. Hence, Ge grading effect should not be ignored.

(iii) The Ge grading effect is highly dependent on the Ge profile, and it will worsen with device scaling (shrinking device size). It can be partially offset by increasing the base doping with scaling.

(iv) Because temperature exaggerates Ge grading effect, it cannot be ignored for precision analog circuits that are required to operate across a very wide temperature range.

(v) It is not adequately captured using a conventional modeling methodology such as Gummel-Poon. Hence, in this work the more extensive compact model known as HIgh CUrrent Model (HICUM) has been used for device modeling.

2.2.2.2 Heterojunction Barrier Effects

The Kirk effect occurs at high current densities and causes significant increase in the transit time. The effect is due to the charge density associated with the carrier density associated with the base-collector region. As the carrier density increase near the CB junction, it increases the charge density in the CB space-charge region. When this charge density exceeds the charges in the depletion region, the depletion region ceases to exist. Now there will be build-up of majority carriers from the base in the base-collector space charge region. The dipole formed by the positively charged ionized donors and the negatively charged ionized acceptors causes the base to push out into the collector region. This results in increase of the base width and increase in the transit time reducing the f_T and f_{max} of the transistor. The collector doping (N_C) level can be increased in order to delay the onset of Kirk effect and hence HBE. Increasing N_C, however, decreases f_{max} and BV_{CEO} due to the increase in C_{CB} and the CB electric field,

causing serious design constraints. The shape and position of the Ge profile in the collector-base region of a SiGe HBT are critical in determining the characteristics of the onset of HBE and the rate of degradation in HBT characteristics with increasing J_C. While large Ge grading is desirable for increasing V_A, f_T and f_{max} of a SiGe HBT, the increased concentration of Ge at the collector-base junction increases the induced barrier which gives rise to HBE. To minimize the impact of the barrier on device performance, either the Ge concentration can be decreased at the CB region or place the SiGe-Si hetero-junction deeper inside the collector region instead of having an abrupt SiGe-Si transition at the interface. The drawback of increasing the Ge content in Si can lead to film stability constraints on the fabrication process. These design trade-offs clearly that there is no specific design rule that can completely eliminate HBE. So, the CB design can be performed depending on the application at hand and take advantage of the band-gap engineering [1].

Chapter 3

SELF HEATING in HBTs

3.1 Introduction

This chapter describes self heating process and ways to model self heating effects in SiGe hetero-junction bipolar transistors (HBTs). Earlier sections are dedicated to the origin of self-heating and the thermal domain counterparts of the self-heating parameters in the electrical domain. Section 3.4.3 describes the proposed non-linear thermal model used to characterize and model the self heating in the device as a function of its dissipated power. Lastly, the HICUM compact model is described which is used to characterize a transistor. Also the procedure to implement the proposed non-linear thermal model in the HICUM model is described.

Under the influence of bias external of semiconductor devices, the moving carriers experience successive scatterings. In most scattering events, these carriers give up kinetic or potential energy by the generation of phonons, photons and/or electron-hole pairs. Among these energy conversion modes, the generation of phonons, also known as lattice vibrations, is the most commonly observed mode and results in the generation of heat in the devices. The consequent junction temperature rise, or self-heating, significantly influences the device behavior. It modulates the device operating condition and hence performance; since the characteristics of semiconductors are inherently defined as a function of operating temperature. The raised temperature promotes most of the long-term degradation mechanisms as well as the catastrophic failures of the device which reduces the device reliability. Therefore, an accurate thermal characterization of the device is critical for the precise prediction of device operation and degradation. Historically, self heating was a major concern for high power devices in which extensive power consumption results in substantial heat generation. However, recent device scaling intended for speed enhancement and higher packing factors have made the self heating in low power, high speed devices a major concern. Self heating has become an issue for many semiconductor systems which means thermal properties need to be properly analyzed along with the electrical properties for such systems [1].

SiGe HBTs are nearly identical to Si BJTs from the thermal point of view, except. Firstly, most HBTs are made using silicon-on-insulator (SOI) technology, with low heat conduction to the heat sink. Secondly, HBTs contain either shallow trenches, deep trenches or both in order to reduce the parasitic capacitance which impedes the thermal flow out of the device. Thirdly, the base region of the HBTs contains a fractional amount of Ge which makes the thermal conductivity of the base region poorer than conventional Si BJT. The poorer thermal conductivity in the base region will not affect the self heating prominently because: the principle heat source in bipolar transistors is the base-collector space-charge region and, most of the generated heat is dissipated downward through the sub-collector, the SOI layer to the substrate. Generally, the devices are operated in the active mode where emitter-base junction is forward-biased and the base-collector (BC) junction is reverse-biased. A substantial amount of power dissipation occurs in this reverse-biased BC junction. Hence, the temperature of the BC junction will dictate the operating temperature of the device. This phenomenon of temperature rise is called self-heating. Self heating is measured in terms of thermal resistance, which represents the change in the temperature of the base-collector junction temperature for a given change in the total power dissipation in the base-collector junction. A number of geometrical parameters influence the thermal resistance of the device such as: the vertical distance of the base-emitter junction to the base-collector junction, the area and the form factor of the emitter, the number of emitter fingers and the distance between them [1].

As emitter areas of bipolar transistors grow smaller in size and power densities increase, the impact of self heating on device performance can no longer be neglected, since this thermal feedback can significantly affect the transistor behavior. The dynamic behavior self heating is characterized by the thermal resistance and thermal capacitance of the device. These thermal properties can be modeled by either a single or a multi-pole equivalent thermal *RC* network. For thermal impedance representation of a device usually a single pole *RC* network is adopted. The values of thermal resistance and thermal capacitance depend on the structural composition and dimensions of the device. The amount of self heating has to be quantified for each new generation of advanced bipolar transistors, especially when introducing Silicon-on-Insulator (SOI) substrates and deep trench isolation to reduce the collector to substrate capacitance. The side effect of this technology is that the device is packed inside four walls of

very low thermal conductivity. This aggravates the problem of self heating by trapping the heat inside the walls [1].

Self-heating may or may not affect the operation of SOI circuits depending on the application of these circuits. The self-heating effect on digital circuits is small, because in digital circuits the power is mostly consumed during transition between high and low states. Tenbroek *et. al*. [28] has demonstrated that the temperature of a partially depleted (PD) NMOS transistor with a gate length 0.7 μm during switching does not exceed a temperature change of 2.5 K [28]. Another reason for this minimal temperature rise in digital circuits is the small heat penetration depth associated with short timescale switching. The heat penetration depth is proportional to the square root of the heating timescale for semi-infinite condition and determines the device dynamic (transient) thermal resistance [29]. As a result, due to the short switching process, the dynamic thermal resistance of digital circuits is relatively small. In a nutshell, the devices which work only as digital components and are not thermally coupled to the rest of the circuit are less affected by self-heating. However, the operation of analog circuits can be significantly affected by self-heating. Tenbroek *et. al*. have demonstrated that because of the self-heating, gain of a class-A amplifier made of partially-depleted (PD) SOI NMOS transistors with a channel length of 0.7 μm can be reduced to more than 0.1 dB. The non-linear temperature change in a 7-bit Digital-to-Analog Converter (DAC), using 0.7 μm PD SOI technology, makes the step size of the DAC's output voltage to be non-linear and degrades the overall performance [28] – [30]. Precise knowledge of the temperature rise in SOI transistors and strained-Si transistors is critical in estimation of the lifetime and reliability of these devices, since the silicon layer provides an alternative yet effective thermal path to the bulk silicon substrate from the source of the heat. Physical degradation mechanisms such as electro-migration are accelerated at higher temperatures. The electro-migration process can be minimized due to lateral conduction in thin Si and SiO_2 device layers.

3.2 Temperature effect on device parameters

3.2.1 Effect of temperature on band-gap narrowing

The band-gap of a material is the difference between the conduction band edge energy, E_C, and the valence band edge energy, E_V, and is denoted by E_g. The widely accepted non-linear band-gap temperature relation for silicon is shown as shown in (3.1) [31].

$$E_{g,Si}(T) = E_{g0,Si} - \frac{\alpha T^2}{T+\beta} \tag{3.1}$$

where $E_{g0,Si}$ is the band-gap of Silicon at 0 K, and α and β are the material parameters whose values for silicon are 4.45 × 10-4 V/K and 686 K respectively. With the addition of Ge in Si the relationship in (3.1) will be modified as given in (3.2) where x_{mol} is the Ge mole fraction [32].

$$E_{g,SiGe}(T) = E_{g,Si}(T) - 0.74(x_{mol}) \tag{3.2}$$

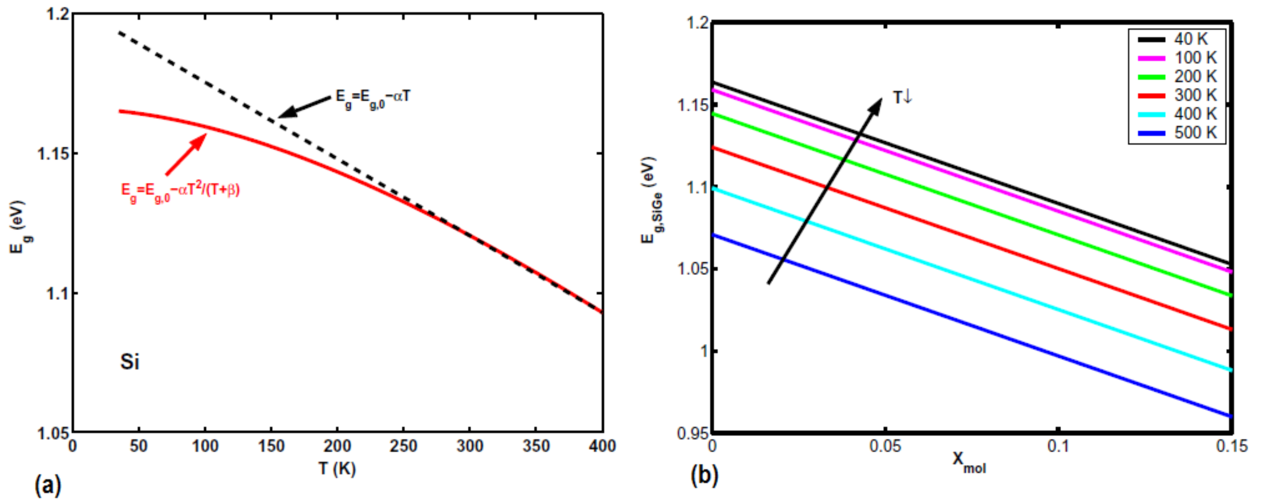

Figure 3-1: (a) Band-gap of silicon versus temperature. (b) Temperature and Ge mole fraction dependence of band-gap for a SiGe device [32].

3.2.2 Effect of temperature on density of states

Strain induced distortion in SiGe reduces the density of states product (N_CN_V) and the hole and electron effective masses [33]. The density of states, N_C and N_V, decreases with increasing Ge mole fraction and finally saturates when the band split exceeds a couple of k_BT where k_B is the Boltzmann constant and T is the temperature. Such a reduction in N_VN_C with increasing Ge content is undesirable

since it causes the reduction in collector current in the SiGe HBT. However, the same reduction in the effective masses that reduces the $N_V N_C$ product also increases the carrier mobilities, which partly offset the impact on the collector current. The temperature and Ge mole fraction dependence of $(N_V N_C)_{SiGe}/(N_V N_C)_{Si}$ is shown in figure 3-2 [32].

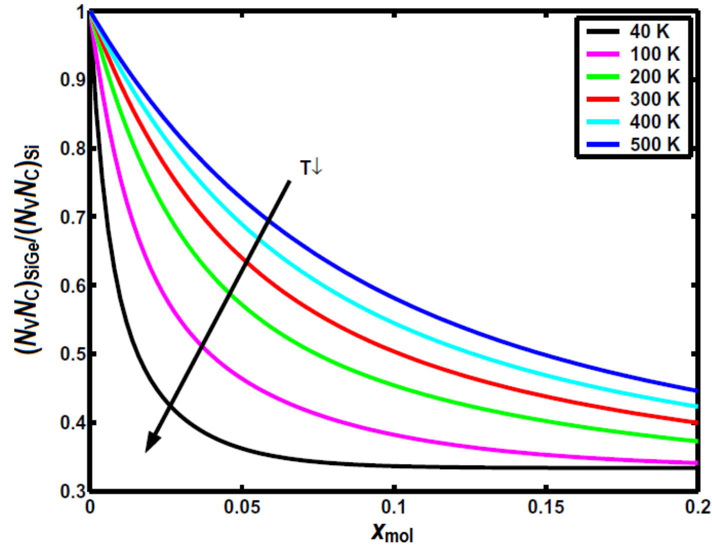

Figure 3-2: Temperature and Ge mole fraction dependence of $(N_V N_C)_{SiGe}/(N_V N_C)_{Si}$ [32].

3.2.3 Effect of temperature on carrier mobility

The electron mobility as a function of temperature for various doping densities in silicon is shown in figure 3-3. The results as reported by [34] and [35] shows that the electron mobility decreases with the increase in temperature as well as doping. A similar relationship of hole mobility as a function of temperature is shown in figure 3-4, and it is apparent from the plot that the hole mobility decreases with an increase in temperature and acceptor doping.

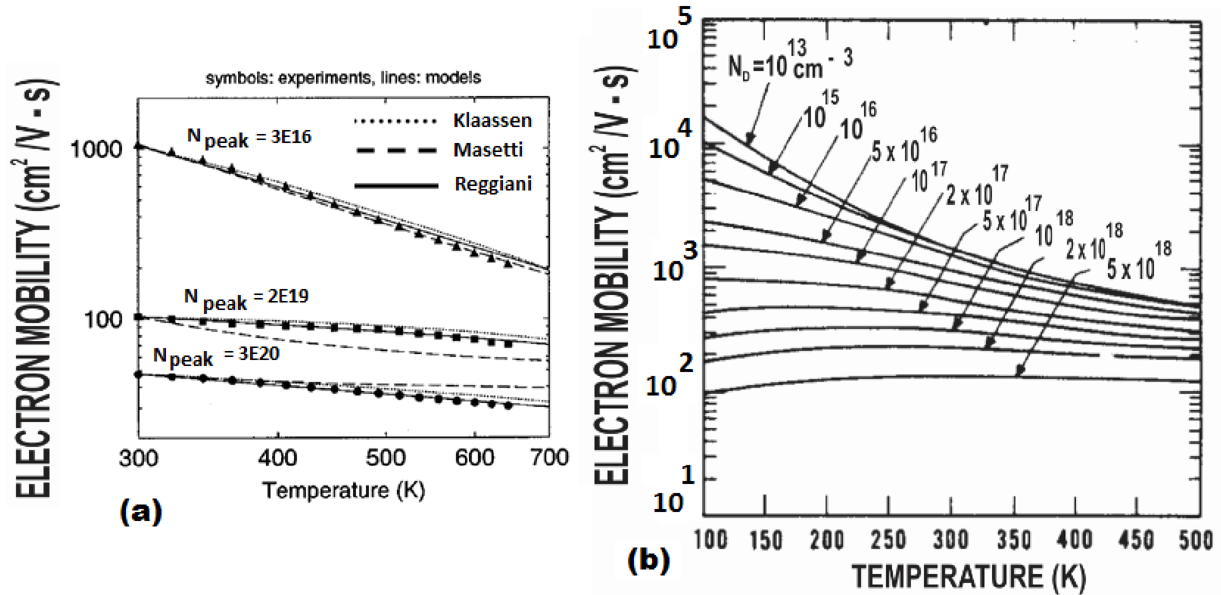

Figure 3-3: (a) The electron mobility as a function of temperature as reported by [34]. (b) The electron mobility as a function of temperature as reported by [35].

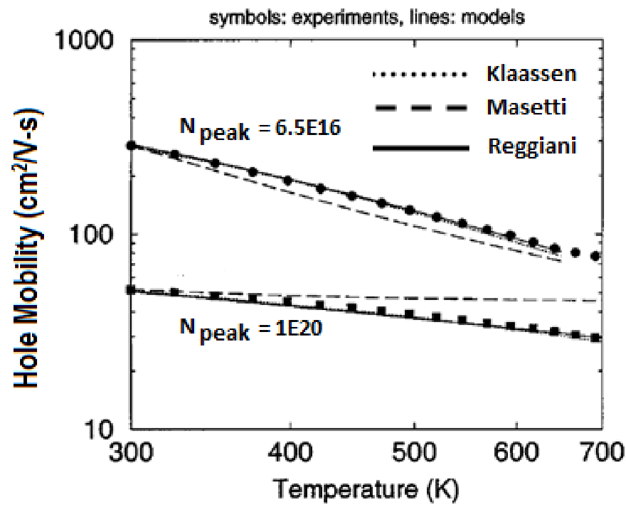

Figure 3-4: The hole mobility as a function of temperature as reported by [34].

3.2.4 Effect of temperature on current gain, β

A negative temperature dependence of the current gain, β, has been observed for SiGe HBTs as shown in figure 3-5. The collector current decreases with an increase in V_{CE} when the injected base current exceeds 1 mA. The decrease in the collector current is due to the reduction in emitter injection efficiency by a factor of $e^{\Delta Eg/KT}$ which increases with temperature. The rise in device temperature is

attributed to the internal Joule heating that in turn results in the degradation of the current gain. If carefully designed such devices can be used to design power amplifiers where the current gain can be automatically controlled to maintain stability and reliability [36].

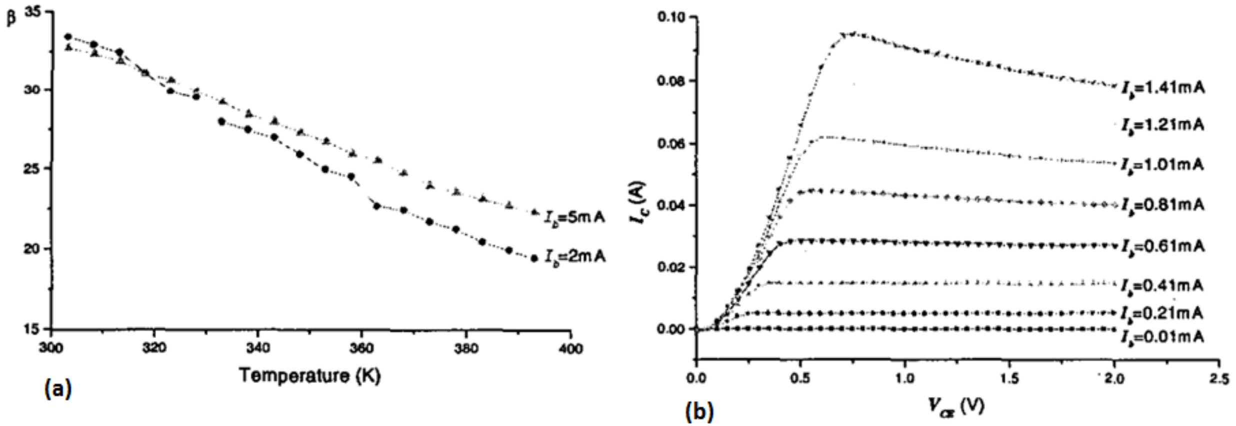

Figure 3-5: (a) Temperature dependence of the current gain for a 4x20 µm SiGe HBT [36]. (b) Output Characteristics of a 4x20 µm SiGe HBT [36].

3.3 Thermal-electrical analogy

Heat flow can be modeled by the static heat flow equation and the electrical voltage by the Poisson's equation as shown in (3.3) and (3.4) respectively.

$$\nabla \cdot (k(T)\nabla T(x, y, z)) = -g(x, y, z) \tag{3.3}$$

$$\nabla^2 V = -\frac{\rho}{\varepsilon} \tag{3.4}$$

where T is the temperature in Kelvin, k is the thermal conductivity in W-cm^{-1}-K^{-1}, g is the volumetric heat generation rate in W-cm^{-3}, ρ is the charge density in C-m^{-3} and ε is the permittivity of the material in F/m.

There exists a correspondence between the electrical and thermal domain. The temperature rise in the thermal network is analogous to the voltage rise in an electrical network. Similarly, the current, the resistance and the capacitance have their equivalent terms in the thermal domain. Table 3-1 displays this analogy between thermal and electrical networks.

Table 3-1: RELATIONSHIP BETWEEN THE THERMAL DOMAIN AND THE ELECTRICAL DOMAIN

Thermal Domain		Electrical Domain	
Temperature	T (K)	Voltage	V (V)
Heat Flow	P (W)	Current	I (A)
Thermal Resistance	R_{th} (K/W)	Resistance	R (Ohm)
Thermal Capacitance	C_{th} (J/K)	Capacitance	C (F)
Ambient Temperature	Kelvin (K)	Ground Voltage	V (V)

3.4 Definition of thermal terms

3.4.1 Thermal resistance

The heat conduction in a homogenous isotropic solid is described by following a time-dependent equation as given in equation (3.5) [1]:

$$\nabla^2 T = \frac{\rho \cdot c}{\kappa} \cdot \frac{\partial T}{\partial t} \tag{3.5}$$

where T is temperature, ρ is mass density, c is the specific heat, k is thermal conductivity and t is time. With proper initial and final boundary conditions, the temperature is determined as a function of time and position within the conducting media. The thermal resistance, R_{th} can be expressed in terms of the ratio of the final value of the temperature at a given position $\vec{r}$ and the dissipated power, P, from the heat source as expressed in (3.6). R_{th} is independent in time, t, for performing steady-state (dc) analysis.

$$R_{th}(\vec{r}) = \frac{T(\vec{r}, t=\infty) - T(\vec{r}, t=0)}{P} = \frac{\Delta T(\vec{r})}{P} \tag{3.6}$$

Even though R_{th} is a function of position most widely accepted convention to represent R_{th} is the thermal resistance at the region inside the device with the peak temperature also called the junction temperature T_j. The thermal resistance of a device can be extracted from the relation between the junction temperature and the power dissipation. Such a relation is generally obtained by exploiting the temperature dependence of an electrical parameter of the device, in which the electrical parameter is measured at various power levels and then converted into temperature variations by a careful calibration.

Typically the base-emitter voltage is calibrated as a function of temperature. The position independent formula shown in (3.7) is widely accepted.

$$R_{\mathrm{th}} = \frac{T_{\mathrm{j}} - T_{\mathrm{amb}}}{P} = \frac{\Delta T}{P} \tag{3.7}$$

where R_{th} is the thermal resistance of the entire device, T_j is the junction temperature of the device (source), T_{amb} is the temperature in the absence of power dissipation or the ambient temperature (sink) and P is the power dissipated in the device. Power dissipated in the device is calculated using power conservation relationship as shown in (3.8).

$$P = I_{\mathrm{C}} \cdot V_{\mathrm{CE}} + I_{\mathrm{B}} \cdot V_{\mathrm{BE}} \tag{3.8}$$

where I_C and I_B are the collector current and base current respectively, and V_{CE} and V_{BE} are the collector-emitter voltage and base-emitter voltage respectively of the transistor [1]. In other words, the thermal resistance is defined as the ratio of the difference in temperatures between two isothermal surfaces and the total heat flow between them. The unit for R_{th} is degree Kelvin per Watts (K/W).

3.4.2 Thermal conductivity

Self-heating and thermally induced reliability are critical issues for advanced SOI and strained-Si-on-SiGe-on-insulator (SGOI), where the devices are separated from the bulk silicon substrate by poor thermal conducting layers. Under dc (steady-state) operation, the saturation current, I_{sat}, of an SOI device is smaller than a bulk device (a device which consists of p-type or n-type substrate and no SOI). One reason is the increase in electron-phonon scattering due to an increase in temperature, which results in the decrease in the mean-free path of the carriers resulting in the reduced mobility. Hence, in practice it is observed that with an increase in temperature the thermal conductivity decreases. Mistry *et. al.* [37] has reported that for short channel devices, I_{sat}, of an SOI device is 9% smaller than I_{sat} of a bulk transistor [37]. Self-heating is responsible for 80% of this reduction and the rest is due to a larger threshold voltage (~40 to 50 mV) for the SOI devices. Degradation of I_{sat}, adversely affects the I_{sat}/I_{off}, which is an important Figure-Of-Merit (FOM) of SOI technology. The leakage current, I_{off}, when the transistor is off (V_{BE}=0) but still biased (V_{CE}>0). This leakage current increases exponentially as the lattice temperature increases. As

a result, self-heating suppresses the FOM by reducing I_{sat} and increasing I_{off}. Moreover, power consumption is increased with the increase in the leakage current. At the ambient temperature, the thermal conductivity of a single-crystal Si layer can be significantly reduced compared with the bulk silicon due to phonon-boundary scattering for silicon layers of thickness < 300 nm [29] – [30]. The impurities and the associated free carriers in the doped regions of the transistors also reduce the thermal conductivity compared to the lightly doped bulk silicon [30]. The relationship of thermal conductivity with temperature for the bulk Si and thin Si films is shown in figure 3-6 [40]. Also the relationship of thermal conductivity with the thickness of the Si layer is demonstrated in figure 3-7 [40]. The elevated temperatures also results in reduced mobility due to lattice vibrations and phonon interactions. At relatively high drain voltage, this effect is translated to negative differential output resistance [41]. Thermal conductivity variation with temperature for silicon dioxide (SiO_2) is shown in figure 3-8 [42].

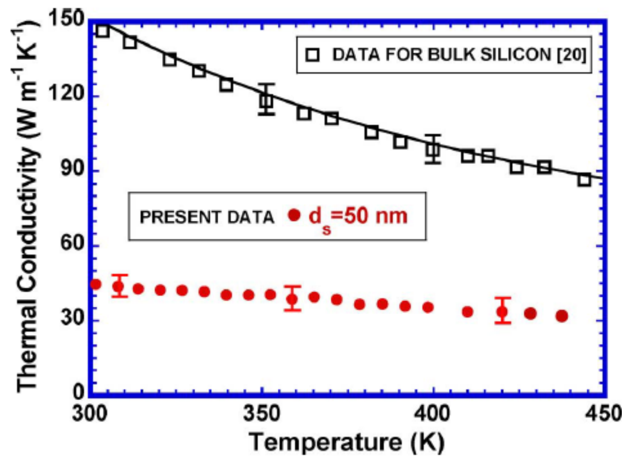

Figure 3-6: Relationship of thermal conductivity of bulk silicon and thin Si films versus temperature [40].

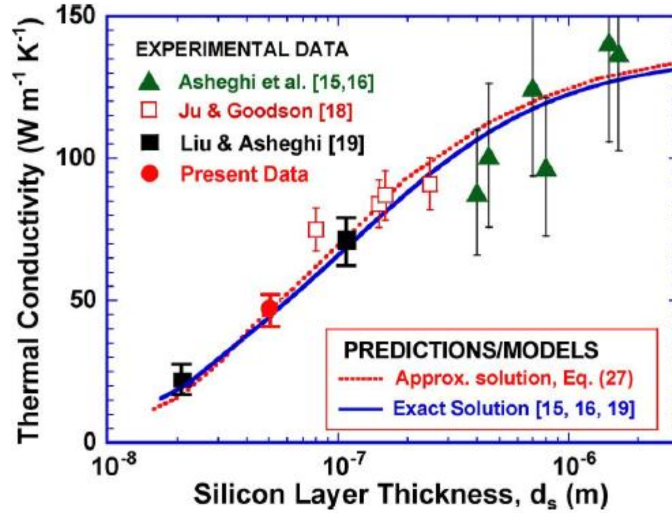

Figure 3-7: Relationship of thermal conductivity of Si for different silicon layer thickness [40].

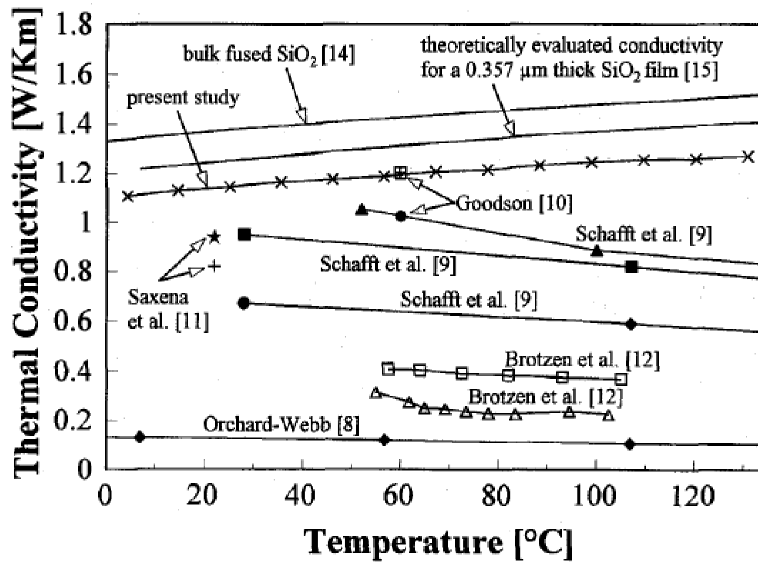

Figure 3-8: Comparison of experimental and theoretical results for thermal conductivity of SiO_2 films and bulk SiO_2 at various temperatures [42].

Although the device junction temperature is of primary concern, the metal temperature of the interconnects is also important. The metal resistance increases with temperature. If the temperature of the metal exceeds a certain value then the large value of metal resistance results in unwanted power loss in the circuit [19].

3.4.3 Proposed non-linear thermal resistance model

In order to increase the operating frequency, RF bipolar transistors must operate at very large current densities [38]. Secondly, in order to reduce the parasitic capacitances of active devices and increase the level of device integration, parasitic coupling to the Si substrate has to be reduced. This can be achieved by using silicon-on-insulator (SOI) substrates and deep trench isolation [38] – [39]. Thirdly, because of the small size of the device and deep trench isolation the heat generated from the power dissipation in the active region cannot be easily removed from the device, which results in an increase in device temperature. Since, the thermal conductivity for a device with a SOI substrate is non linear, neither Si nor SiO_2 conductivity is linear in temperature. The increase in the thermal resistance due to self-heating leads to a non-linear relation between temperature and power dissipation. Hence, equation (3.7) cannot be used to accurately estimate the R_{th} of the device. Also, expressions to describe this effect has been given in [44] for GaAs and SiGe devices, but they cannot be used for this work since the size of the SiGe HBTs used in the present work are smaller than those being used in [44]. Moreover, the details of the device geometry, such as presence of the shallow and the deep trenches, trench material, and the offset of the emitter region with respect to the trenches is also unknown. Hence results of [44] cannot be used for the present work.

The junction temperature at a given power can be calculated using a Taylor's series expansion. Equation (3.9) shows the first three terms of the Taylor's series expansion for the junction temperature as a function of dissipated power, P.

$$T_j(P) = T_j(P_0) + \frac{dT_j(P_0)}{dP}(P - P_0) + \frac{1}{2}\frac{d^2T_j(P_0)}{dP^2}(P - P_0)^2 \tag{3.9}$$

$$T_j(P_0) = T_j(P = 0) = T_0 \tag{3.10}$$

$$T_j(P) - T_0 = \left.\frac{dT_j}{dP}\right|_{T_0} \times P + \frac{1}{2}\left.\frac{d^2T_j}{dP^2}\right|_{T_0} \times P^2 \tag{3.11}$$

Using (3.9) - (3.11) the thermal resistance, R_{th}, can be written as shown in (3.12).

$$R_{\text{th}} = \frac{T_{\text{j}}(P) - T_0}{P} = \frac{\text{d}T_{\text{j}}}{\text{d}P} + \frac{1}{2}\frac{\text{d}^2 T_{\text{j}}}{\text{d}P^2} \times P \tag{3.12}$$

The thermal resistance, R_{th}, is broken into two parts: (i) the R_{th} value of the resistance when P=0 is given by R_0 having units K/W and (ii) the thermal resistance variation is denoted by dR_{th}/dP having units K/W^2. It will be symbolically denoted as *dRdP* in the rest of the document. The new expression used to calculate the thermal resistance is shown in (3.12). The second term in (3.12) takes into account the change in the thermal resistance with respect to power and is multiplied with the instantaneous power dissipated by the transistor to calculate the final change in the thermal resistance.

$$R_{\text{th}}(P) = R_0 + \left(\frac{\text{d}R_{\text{th}}}{\text{d}P} \times P\right) \tag{3.13}$$

3.4.4 Thermal capacitance

The thermal resistance, R_{th}, alone is sufficient to describe the relationship between temperature and dissipated power for steady state conditions. However, for the transient behavior, the concept of thermal capacitance C_{th} is needed. A general expression for the heat capacity (thermal capacity) in a solid is expressed as (3.14):

$$C_{th} = \rho \cdot c \cdot V \tag{3.14}$$

where c is the specific heat, ρ is density and V is the volume to be heated. The assumption being made here is that the temperature is uniform throughout the volume V. But, for practical device structures a thermal gradient always exists inside the device. Also the volume, V, is not clearly defined since the substrate around the device is partially heated. In such cases C_{th} evaluated from equation (3.14) will lead to erroneous results. The way to prevent this is to estimate C_{th} from the measured time-dependent response of the junction temperature to the power dissipation, typically applied in the form of a fast pulse function. The advantage of using fast pulse time domain techniques is; it helps to separate the device thermal spreading resistance from other components of thermal resistance [45]. Together with R_{th} values, C_{th} can be easily obtained from the estimated time delay, $\tau = R_{th} \cdot C_{th}$, of the transient response [1].

3.5 Available models of self heating in HBTs

Today's IC designs depend on circuit simulation, and circuit simulation needs compact models. Various compact models such as: SPICE Gummel Poon model (SGP), HIgh CUrrent Model (HICUM), MEXTRAM, and the Vertical Bipolar Inter-Company (VBIC) are used to model bipolar transistors. For over 20 years the SGP model has been the workhorse for circuit simulation of BJTs. There are several shortcomings of the SGP model. The SGP model shows a decrease of β with increase in dissipated power which results in a negative differential output resistance due to the self heating. The Early effect formulation for modeling output conduction. Inability to model collector resistance modulation (quasi-saturation) and parasitic substrate transistor action led to the development of new analytical models. Also the SGP model is based on integral charge control and fails to model this important self heating effect, while the VBIC and the HICUM models capture self heating with an accurate electro-thermal model. The selection of the HICUM model for the present analysis is based on its capability of modeling high-current effects and self heating [52]. A comparison of measured f_T as a function of J_C with VBIC and HICUM compact models is shown in figure 3-9 [57]. A comparison of important features of SGP, VBIC, HICUM and MEXTRAM compact models are shown in Table 3-2 [56].

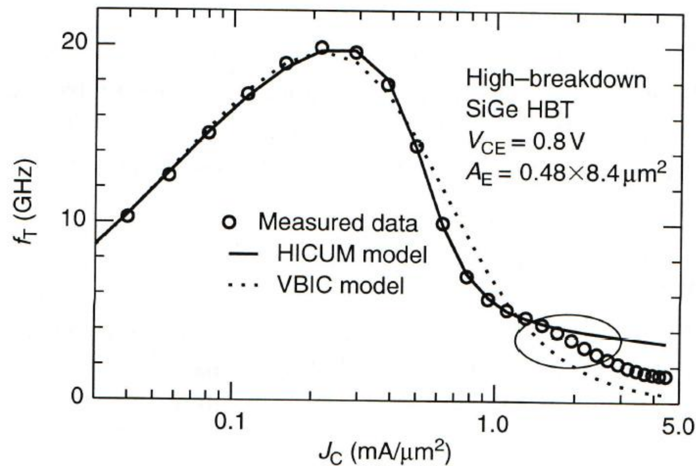

Figure 3-9: Comparison of measured f_T as a function of J_C with VBIC and HICUM compact models in a SiGe HBT [57].

Table 3-2: COMPARISON OF IMPORTANT FEATURES OF THE SGP, VBIC, HICUM AND MEXTRAM COMPACT MODELS [56].

	Feature	SGP	VBIC	HICUM	MEXTRAM
1	Separation of I_B and I_C	N	Y	Y	Y
2	Improved Early effect model	N	Y	Y	Y
3	External BE junction	N	Y	Y	Y
4	BC avalanche model	N	Y	Y	Y
5	Single piece depletion capacitance model	N	Y	Y	Y
6	Reach though capacitance model	N	Y	Y	Y
7	Quasi saturation	N	Y	Y	Y
8	HBT modeling capability	N	Y	Y	Y
9	Parasitic PNP	N	Y	Y	Y
10	Improved temperature model	N	Y	Y	Y
11	Self heating modeling	N	Y	Y	Y
12	Overlap capacitances	N	Y	Y	Y
13	Substrate model	N	Y	Y	N
14	BE breakdown	N	Y	Y	N
15	Improved f_T model	N	N	Y	Y
16	Non quasi-static effects	N	N	Y	Y
17	Current dependent BC depletion capacitance	N	N	N	Y
18	Internal nodes	3	7	5	5
19	Total number of model parameters	41	108	101	73

3.5.1 HIgh Current Model (HICUM)

The HICUM model was defined by a group of representatives from the IC and CAD industries to try to rectify the shortcomings of the SGP model. The name HICUM was derived from HIgh-CUrrent Model, indicating that HICUM was initially developed with special emphasis on modeling the operating region at high current densities. This is very important for certain high-speed applications. The HICUM model is a semi-physical compact bipolar model. Semi-physical means that for arbitrary transistor

configurations, a complete set of model parameters can be calculated from a single set of technology specific electrical and technological data. The HICUM model is based on an extended and Generalized Integral Charge Control Relation (GICCR). In contrast to the Gummel-Poon model and its variants, in the HICUM model the Integral Charge Control Relation (ICCR) concept is applied consistently without inadequate simplification and additional fitting parameters such as the Early voltage parameter. Reliable design and characterization of high speed circuits requires a compact model to accurately model the dynamic transistor behavior. Quantities such as depletion capacitance and the transit time of mobile carriers as well as associated charges that determine the dynamic behavior are considered the basis of the compact model. An accurate modeling of these basic quantities as a function of applied bias yields an accurate description of small signal, dynamic large signal, and the dc behavior. The important physical and electrical effects that are modeled by HICUM/Level 2 are listed below [52] – [55]:

- High current effects,
- Distributed high frequency model for the external base-collector region,
- Emitter periphery injection and associated charge storage,
- Emitter current crowding (through a bias dependent internal base resistance),
- Two- and three-dimensional collector current spreading,
- Parasitic (bias dependent) capacitances between base-emitter and base-collector terminal,
- Vertical non-quasi-static (NQS) effects for transfer current and minority charge,
- Temperature dependence and self-heating,
- Parasitic substrate transistor,
- Tunneling in the base-emitter junction,
- Lateral scalability,
- Bandgap differences (occurring in HBTs).

The accuracy and applicability of the HICUM model has been demonstrated for a variety of different technologies, ranging from low speed and relatively high voltage process to present SiGe production processes. The HICUM/Level 2 as shown in figure 3-9 includes many physical effects that are observed in today's silicon based processes (including SiGe technologies). As a result, its equivalent

circuit is fairly extensive and complicated and not well suited for rough analytical calculation often performed by circuit designers in the preliminary design phase. Figure 3-9 depicts the large signal equivalent circuit for the HICUM model and the thermal network is shown in figure 3-10 [56]. The HICUM/Level 2 model contains two additional circuit nodes compared to the SGP model, namely B* and S′. The node B* separates the operating point independent external base resistance component from the operating point dependent internal base resistance. This helps to take into account emitter periphery effects which play a significant role in modern highly scaled transistors. This node also helps in improved modeling of the distributed nature of the external base-collector (BC) region by separating the external BC capacitance, C_{BCx} over r_{Bx} in form of a π-type equivalent circuit. Another advantage of node B* is its ability to account for high frequency small signal emitter current crowding through the capacitance C_{rBi}. For further details on the HICUM model readers can refer to [52] – [57].

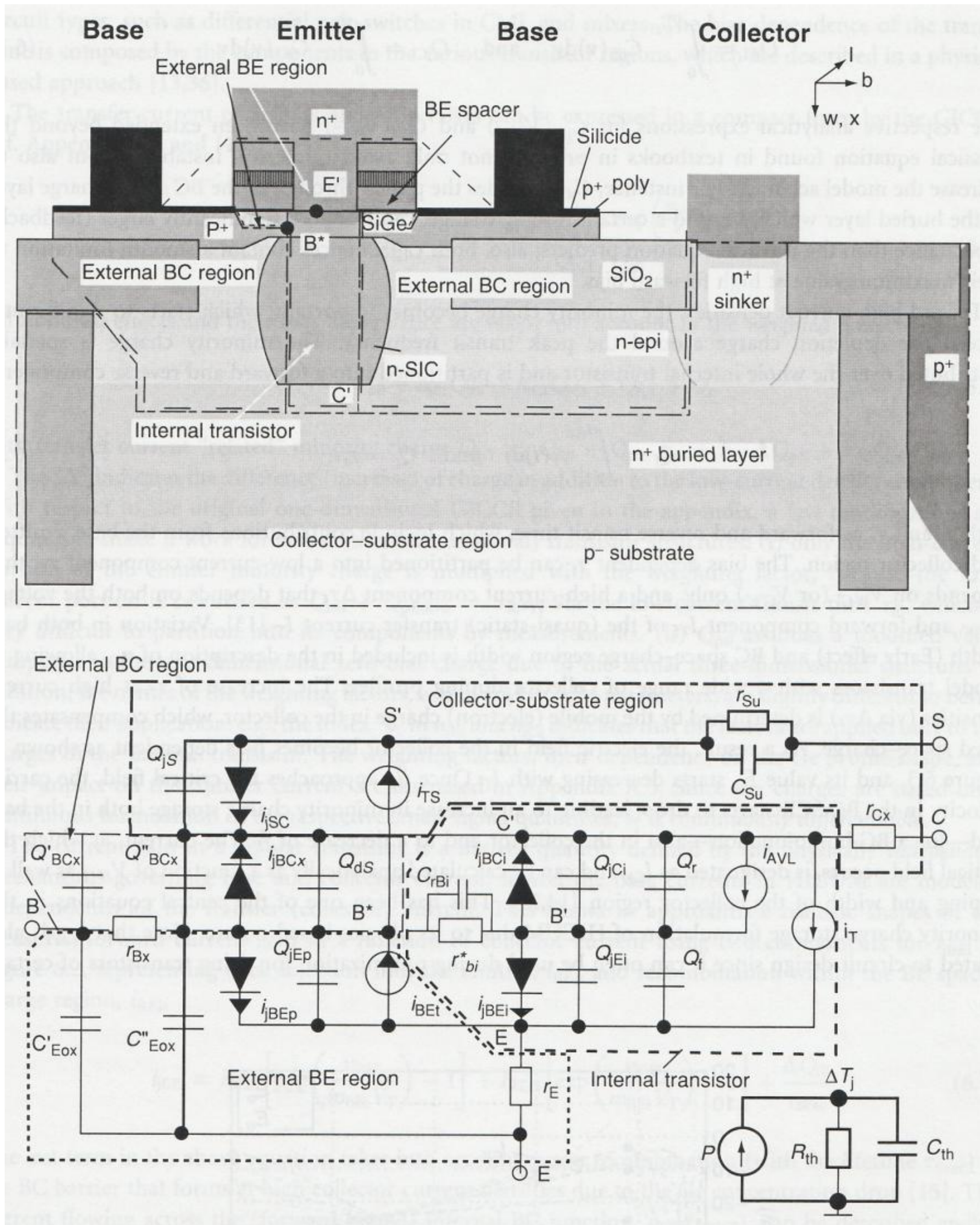

Figure 3-10: A schematic showing large signal equivalent circuit for the HICUM model [57].

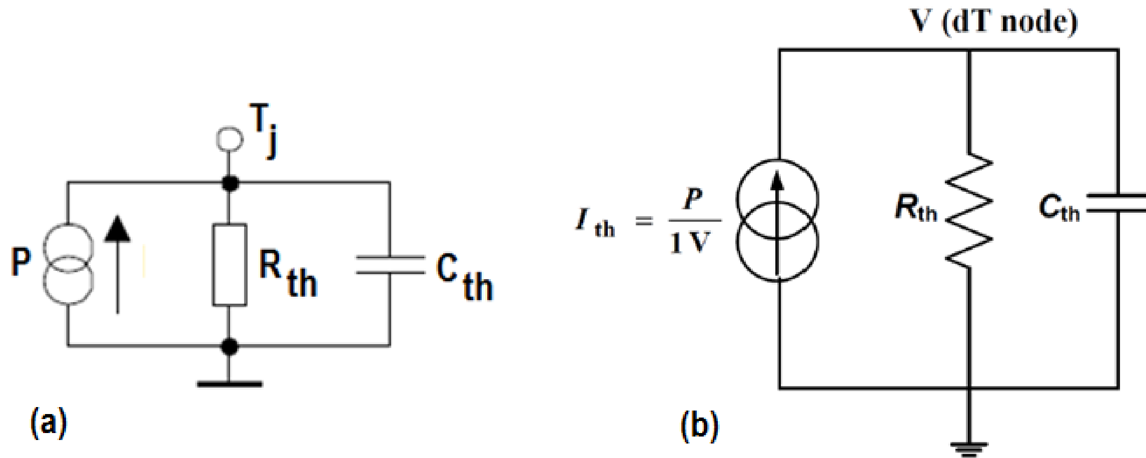

Figure 3-11: (a) A schematic of the thermal network as implemented in the standard HICUM model [52]. (b) A schematic of an equivalent thermal model to the thermal model shown in (a).

3.5.2 HICUM model level 2 version 2.34

The HICUM model level 2 version 2.34 takes into account the non-linear temperature dependence of the thermal resistance, as shown in (3.15) [60].

$$R_{\mathrm{th}}(T) = R_{\mathrm{th}}(T_0)\left[1 - \alpha_{\mathrm{Rth}}\Delta T + \left(\frac{T}{T_0}\right)^{\zeta_{\mathrm{Rth}}}\right] \tag{3.15}$$

where α_{Rth} and ζ_{Rth} are model parameters. The linear dependence on T was introduced in (3.15) to avoid a possible numerical instability, and is sufficient for practical applications. Also the last term in the square brackets in (3.15) may be dropped in the future [60]. However, optimized results given in chapter 4 shows that a non-linear term is required to model the thermal resistance accurately.

Thermal resistance is expressed in terms of power (a measured and independent quantity) as in (3.13). Expressing thermal resistance in terms of the dependent variable of temperature (as in (3.15)) does require more iteration steps to find a solution.

3.5.3 Implementation of proposed non-linear thermal resistance in the HICUM model

The non-linear thermal resistance is implemented using a non-linear current controlled voltage source in the HICUM model using the IC-CAP 2014.04 modeling tool through the Advanced Design System (ADS) simulator. The linear thermal model of the HICUM model is also attached to the thermal

node, dT, however the value of R_{th} is made very high (i.e.: 1×10^6 Ω) and the value of C_{th} is made very small so that they do not have any effect on the circuit operation. The default symbol and illustration of a non-linear Current Controlled Voltage Source (CCVS) is given in figure 3-11. The non-linearity of the circuit is defined by a non-linear equation and the node numbers 1 through 4 are replaced with the actual HICUM circuit nodes. The equation used to implement a non-linear CCVS in ADS is given in equation (3.16) [61]. The current, I_1, flows though the controlling node and V_2 is the controlled node (simulating the temperature rise).

$$V_2 = a_1 I_1 + a_2 I_1^2 \tag{3.16}$$

where a_1 and a_2 can be calculated as given in (3.17):

$$a_1 = \left.\frac{\mathrm{d}T_\mathrm{j}}{\mathrm{d}P}\right|_{T_0} = R_0 \text{ and } a_2 = \frac{1}{2}\left.\frac{\mathrm{d}^2 T_\mathrm{j}}{\mathrm{d}P^2}\right|_{T_0} = dRdP \tag{3.17}$$

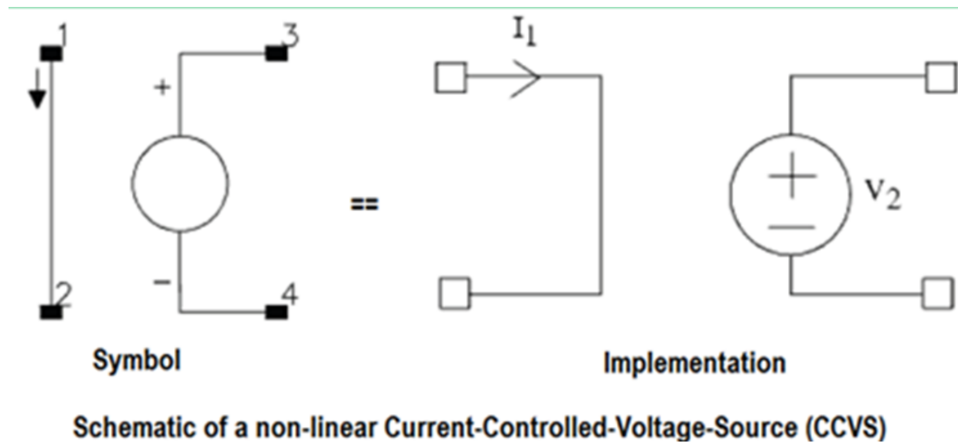

Figure 3-12: The model definition of the current controlled voltage source (CCVS) in ADS simulator that is used to implement the non-linear thermal model in the HICUM model [61].

Chapter 4

MEASUREMENT SETUP

The first part of this chapter presents the details of the measurement setups that have been used in this work. The later part of this chapter summarizes the simulation and optimization procedures that will be implemented in the IC-CAP modeling tool. The devices used in the measurements and modeling were supplied by Texas Instruments Inc. (TI). The devices are Low Voltage (LV) NPN SiGe HBTs with a single emitter configuration with shallow trench and deep trench isolation. The list of devices that were used is given in Table 4-1. The collector current was limited to the specified compliance level as given by TI. The HICUM model parameters used in this work for the optimization process for the non-linear R_{th} network were provided by TI, Inc. obtained from their extraction procedure.

Table 4-1: LIST OF DEVICES USED FOR MEASUREMENTS

	Emitter Length	**Test Structure**	**Number of Emitter Fingers**
1	0.4 µm	Low Voltage, NPN, BEC configuration	1
2	0.6 µm	Low Voltage, NPN, BEC configuration	1
3	0.8 µm	Low Voltage, NPN, BEC configuration	1
4	1 µm	Low Voltage, NPN, BEC configuration	1
5	5 µm	Low Voltage, NPN, BEC configuration	1
6	10 µm	Low Voltage, NPN, BEC configuration	1
7	20 µm	Low Voltage, NPN, BEC configuration	1

4.1 Device Under Test (DUT) setup

The Hewlett-Packard 4142B modular DC source/monitor is used to perform current-voltage (*I*-*V*) measurements on the devices listed in table 4-1. The measurement setup consists of 4 major blocks. They are: (a) A HP 4142B modular dc source/monitor (figure 4-1), (b) a combination of Source/Monitor Units (SMU) and bias network modules (figure 4-2), (c) Cascade Microtech probe station (figure 4-3) and

(d) a desktop computer installed with IC-CAP device modeling software. The measurement setup consisting of parameter (current/voltage) sweep is provided to the 4142B using the IC-CAP tool through Hewlett-Packard Interface Bus (HP-IB). The wafer level probing of the devices is carried out using the probe station using the Infinity probes. The device-under-test is connected to the 4142B using Sub-Miniature version A (SMA) via bias network and SMU unit.

Figure 4-1: Picture of HP 4142B modular dc source/monitor with High Power SMUs (HPSMUs) and Ground Unit (GNDU) connections.

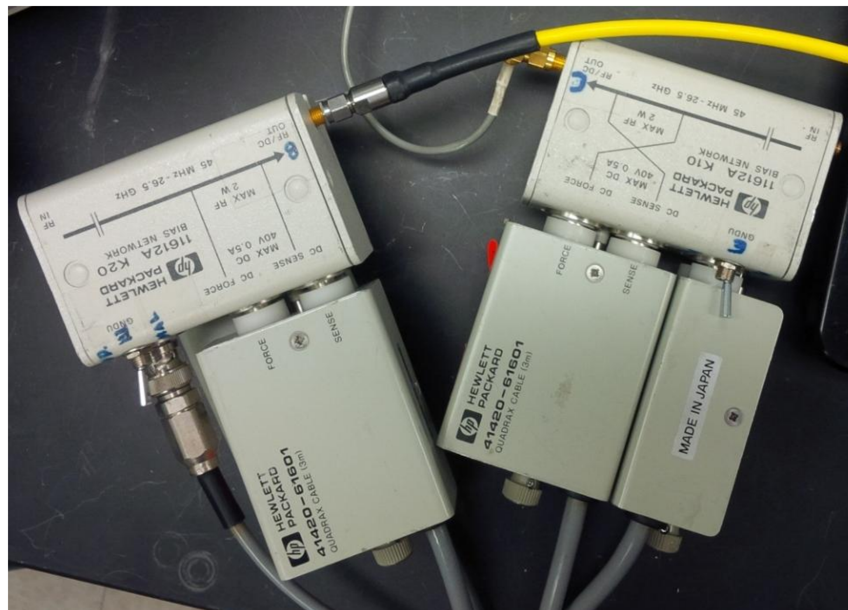

Figure 4-2: Picture showing HPSMU connections with the bias network modules which are connected to the device under test via SMA cables.

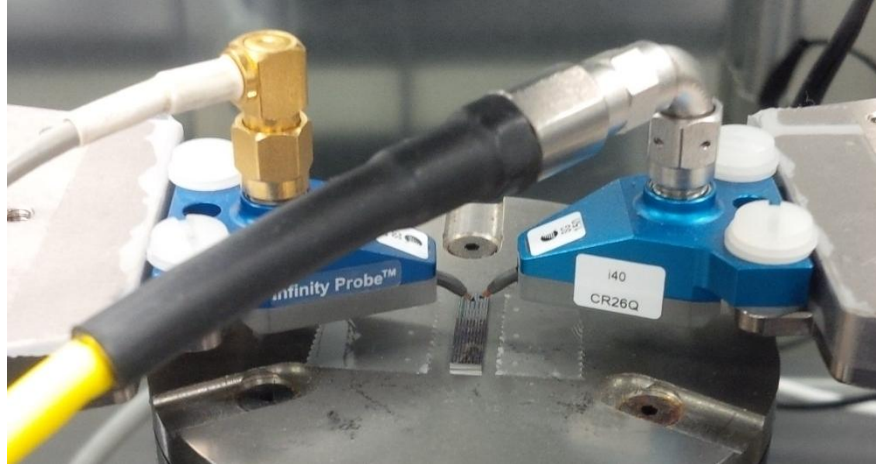

Figure 4-3: Picture showing the device mounted on the probe station with probes assembly.

4.1.1 Hewlett-Packard 4142B modular dc source/monitor

The HP 4142B is a high performance dc parametric measurement instrument with plug-in unit architecture which has: (i) a wide measurement range (i.e.: 10 A, 1000 V), (ii) high resolution (i.e.: 20 fA, 4 μV), (iii) high speed (i.e.: set/force *I* or *V*: 4 ms, measure I or V: 4 ms), and (iv) high accuracy (i.e.: V: 0.05%, I: 0.2%). All HP 4142B operations of the measurement setup, execution, and data recording are computer controlled via the Hewlett-Packard Interface Bus (HP-IB). As a measurement unit, five types of plug-in units are available in addition to a built-in, 0 V source Ground Unit (GNDU). The five types of plug-in units are: (i) HP 41420 A - High Power Source/Monitor Unit (HPSMU) and HP 41421B - Medium Power SMU (MPSMU), (ii) HP 41422A - High Current source/monitor Unit (HCU), (iii) HP 41424A - Voltage Source/ Voltage Monitor Unit (VS/VMU) and (iv) HP 41423A - High Voltage source/monitor Unit (HVU) and (v) HP 41425A - Analog Feedback Unit (AFU). For the present work HPSMUs and GNDU plug-in units will be used for the measurements. The HPSMU can force and measure up to ±200 V or ±1 A (with maximum power: 14 W). Each SMU functions in either of the two modes: (i) V source (constant or pulse) and I monitor and (ii) I source (constant or pulse) and V monitor. A simplified SMU circuit diagram is shown in figure 4-4 [62].

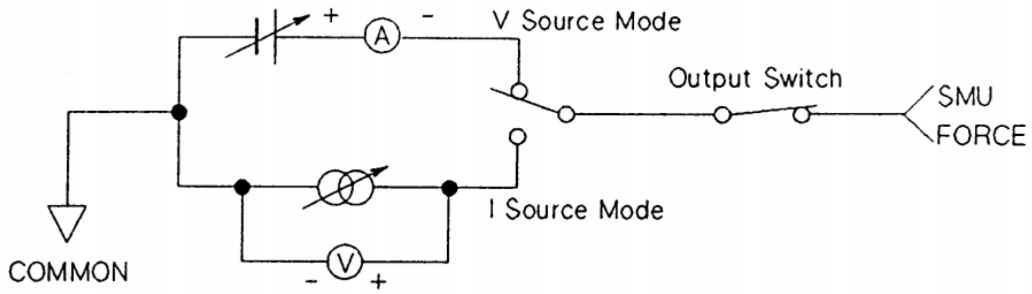

Figure 4-4: Simplified SMU circuit diagram [62].

4.1.2 Probe details

Infinity probes from Cascade Microtech, Inc. were used for probing the devices. The Infinity probes are an ideal match for device characterization and modeling because of its extremely low contact resistance on aluminum pads of the device (wafer level probing). Secondly, they are designed for on-wafer/planar surface measurements only making them the ideal choice for wafer level probing. Cascade Microtech's proprietary thin film and coaxial probe technology reduces unwanted couplings to nearby devices and transmission modes. Single vertical connector, Signal-Ground (SG) and Ground-Signal (GS) probes as shown in figure 4-5 were used for measurements. Figure 4-6 (a) shows the picture when probes are lowered to make contacts with the pads for measurements. Scuff marks are left behind due to the contact between the probes lead and the contact pads on the wafer as shown in figure 4-6 (b). Care should be taken while lowering the probes onto the wafer because over stressing the contact can result in breaking of the probe's lead.

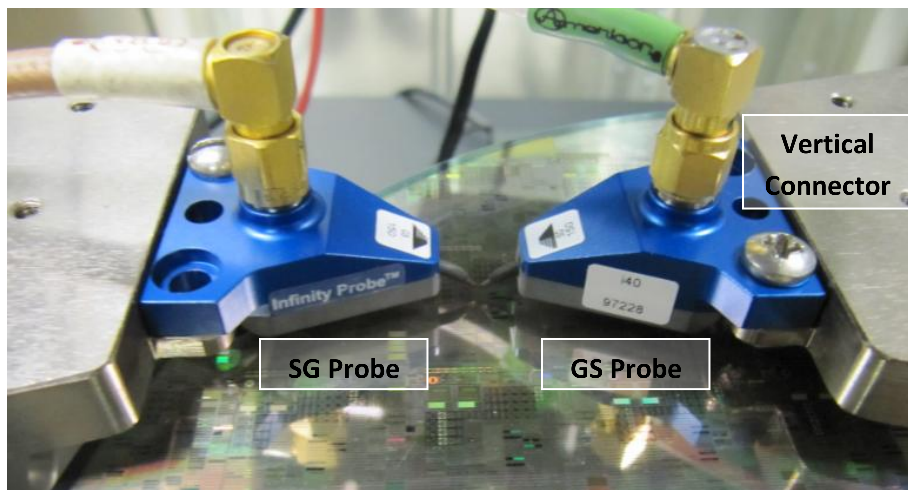

Figure 4-5: A picture of the SG and GS Infinity probes with a vertical connector positioned on the probe station holding the wafer.

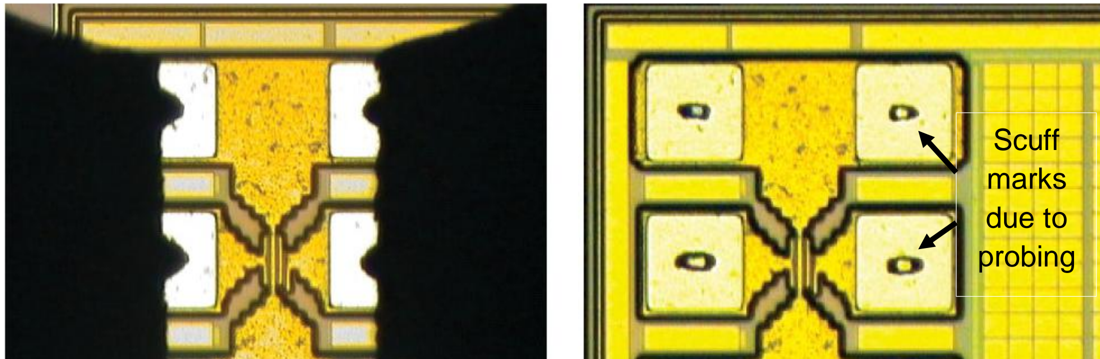

Figure 4-6: (a) Infinity SG and GS probes contacting the NPN device on the wafer. (b) Small contact marks on the device aluminum pads left behind by the probes [63].

4.1.3 Preventing oscillation from the test device

The test device itself may oscillate at high frequencies (i.e.: more than 3 MHz) due to residual inductances and stray capacitances from cables, probe card, and test fixture. Bipolar transistors which have high current gain and a wide frequency range, and Field Effect Transistors (FETs), which have high transconductance (g_m) and a wide frequency range, are likely to oscillate. An example of a current-voltage (*I-V*) plot affected by oscillations is shown in figure 4-7. The oscillation higher than 3 MHz does not come from the source and monitor units. Also an oscillation of 5 MHz or more cannot be detected by the SMU or HVU. Some of the ways to prevent test device oscillations are described below [62]:

- A ferrite bead can be installed as close as possible to the test device. One or more than one bead or change to the beads with different diameter may be needed to prevent oscillation. Installing of the ferrite bead to the base lead of a bipolar transistor and to the gate lead of a FET is generally more effective in stopping unwanted oscillations. Ferrite beads should not be shorted to the case of the device or to the other leads in order to minimize the leakage current.
- The length of the connection cable can be shortened.
- The test device can be enclosed with a shielding box.
- The “Force” and “Sense” lines of the SMU/HVU can be surrounded by a GUARD ring.

A similar oscillating result in the forward Gummel measurement setup was observed while performing measurements on HBTs. It was found that the length of the Sub-Miniature version A (SMA)

cables used to connect the probes with the SMUs is also important. At some specific length a large amount of current was recorded for both the base and the collector. The reason for the higher current values was oscillations that were caused due to the length of the cable. This problem was fixed by replacing the SMA cables cable lengths different from the previous cables [62].

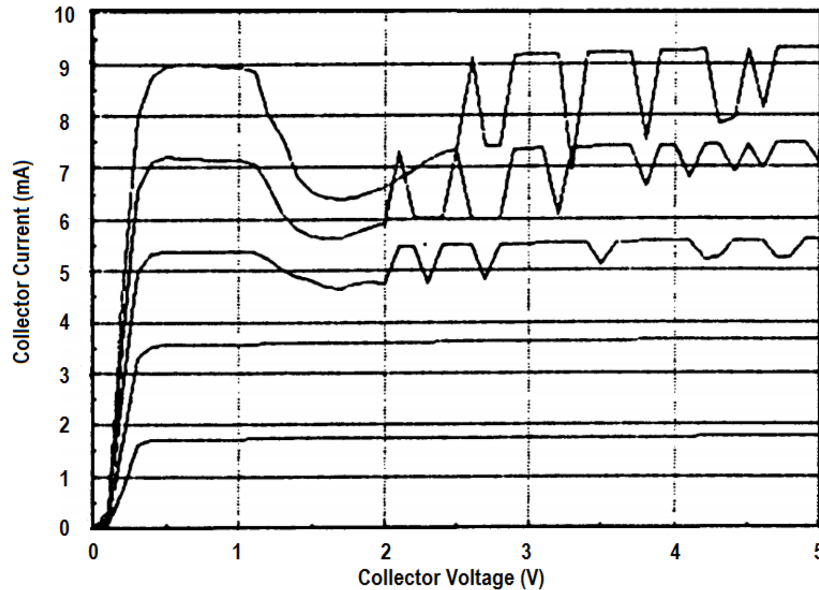

Figure 4-7: Example of an oscillating test device output characteristics [62].

4.2 DC measurements

DC measurements on the device include Forward Gummel (FG) and base controlled output characteristics (output characteristics) measurements. The FG measurement is very useful in device characterization because it reflects on the quality of emitter-base junction while the base-collector bias, V_{BC} is kept constant. The effect of Early effect on the device measurements can be reduced by keeping the V_{BC} constant. A number of other device parameters like the dc gain, β, ideality factors and leakage currents can also be extracted directly from the Gummel plot. It was ensured while taking the measurements that the devices are operated in their Safe Operating Area (SOA) limits. The SOA current limit was calculated from the maximum current density, J_C that these devices can withstand, multiplied by the emitter area of the device.

4.2.1 Forward Gummel measurement setup

The forward Gummel measurement setup is shown in figure 4-8. Here, the base voltage, V_{BE} and the collector voltage, V_{CE}, are synced together (to keep V_{BC} constant) in order to prevent the Early effect. For the forward Gummel measurement, V_{BE} was constrained to be equal to V_{CE} where both varied from 560 mV to 840 mV in steps of 10 mV.

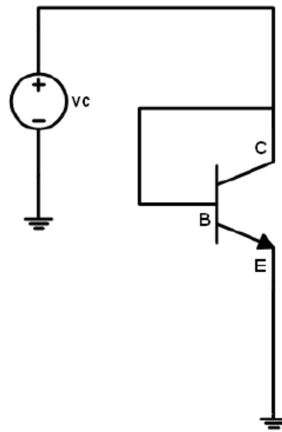

Figure 4-8: Schematic of the set up that was used for forward Gummel measurement.

4.2.2 Base voltage controlled output characteristics measurement setup

For the base controlled output characteristics, the base voltage was set at 560 mV and the collector voltage was swept from 0 V to 2 V in steps of 40 mV. Then the base voltage was incremented by 16 mV and the collector voltage was swept from 0 V to 2 V again in steps of 40 mV. This procedure was repeated until V_{BE}=840 mV. The setup is shown in figure 4-9.

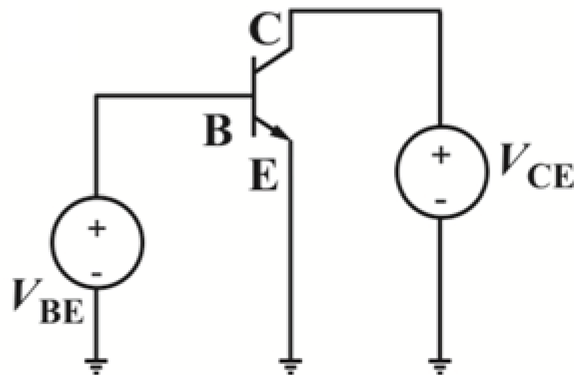

Figure 4-9: Schematic of the set up that was used for base voltage controlled output characteristics measurement.

4.3 Simulations and optimization procedures

Simulations and optimizations of the data obtained by measurement procedures as described in section 4.2 were carried out using the Agilent IC-CAP modeling software. A non-linear current controlled voltage source is used to replace the linear thermal resistance model of the HICUM/L2 version 2.31 model. The HICUM/L2 version 2.31 model was released in 2012, which was used in the model optimization process.

4.3.1 Optimization procedure

In order to model the self-heating of the device it is very important to model the junction temperature of the device. It can be inferred from equations (3.5) through (3-10) that any change in the junction temperature will directly affect the thermal resistance, R_{th}. Equations (3.4) and (3.12) were implemented in IC-CAP in the form of transforms to correctly model the rise in temperature with respect to power dissipated in the device and in turn model the correct thermal resistance, $R_{th}(P)$.

The starting values for the device model parameters were obtained from Texas Instruments Inc. except for *dRdP* which stands for *dR/dP*. The low injection parameters such as internal base-emitter saturation current and ideality factor are represented by i_{beis} and m_{bei}, respectively and the internal base-emitter recombination saturation current and ideality factor are given as i_{reis} and m_{rei} respectively. These 4 model parameters were optimized for the low level injection region. Other parameters that were optimized in the high injection region are: (c_{10}), the emitter resistance (r_e), the Early voltage parameters (h_{jci}) and (h_{jei}), the thermal resistance at ambient temperature (R_0), and the change in the thermal resistance (*dRdP*). The model parameters were optimized using the forward Gummel setup (leaving h_{jCi}, h_{jEi}, R_0 and *dRdP* constant). An upper and lower bound of 20% with respect to the starting values was used for all the model parameters. Table 4-2 lists the model parameters with the setups in which they were optimized.

The data points below V_{BE}=550 mV in the forward Gummel setup were noisy and hence excluded in the optimizations. Using the optimized values from the forward Gummel setup, the output characteristics setup model parameters were optimized to get the least percentage absolute error in the simulated curves with respect to the measured values. Thermal model parameters, R_0 and *dRdP*, along with h_{jEi} and h_{jCi} are optimized in the base voltage controlled output characteristics setup to obtain the

least percentage error in the collector current. This two step procedure was repeated until the transform used to model the junction temperature gave a constant small error for the whole range of V_{BE} values.

Table 4-2: LIST OF DEVICE MODEL PARAMETERS USED FOR OPTIMIZATIONS

Model Parameter Name	Model Parameter Definition	Optimization Setup	Unit
c_{10}	GICCR constant Related to Saturation Current as: $c_{10} = (I_S \times Q_{p0})$	FG	A×C
i_{BEiS}	Internal B-E saturation current	FG	A
m_{BEi}	Internal B-E current ideality factor	FG	-
i_{REiS}	Internal B-E recombination saturation current	FG	A
m_{REi}	Internal B-E recombination current ideality factor	FG	-
r_E	Emitter series resistance	FG	Ohm
h_{jCi}	B-C depletion charge weighting factor	Output Characteristics	-
h_{jEi}	B-E depletion charge weighting factor	Output Characteristics	-
R_0^*	Thermal resistance at T_0	Output Characteristics	K/W
$dRdP^*$	Power dependence of thermal resistance	Output Characteristics	K/W^2

* - *Ro* and *dRdP* are not the standard HICUM parameters.

The absolute error between the measured and the simulated data is calculated using the expression (4.1). This expression is used to calculate the absolute error in collector current and base current for various setups such as forward Gummel and base voltage controlled output characteristics.

$$\% Absolute_error = \left(\frac{measured_value - simulated_value}{measured_value} \times 100 \right) \quad (4.1)$$

4.3.2 Junction temperature estimation

The increase in the junction temperature using the non-linear thermal model is calculated by implementing the equation (4.2).

$$\Delta T_{\mathrm{j}} = T_{\mathrm{j}}(P) - T_0 = (R_0 \times P) + (dRdP \times P^2) \tag{4.2}$$

where ΔT_{j} is the increase in the junction temperature in K, $T_{\mathrm{j}}(P)$ is the junction temperature in K, T_0 is the ambient temperature in K, P is the power dissipated by the device, R_0 is the thermal resistance at P=0 in K/W, *dRdP* is the second order thermal resistance having units of K/W^2.

The increase in junction temperature estimation by the linear thermal model is carried out by re-arranging equation (3.5) as shown in (4.4). The dT node is not directly accessible so the junction temperature is estimated by the HICUM model. A two step approach is used in order to obtain the junction temperature as estimated by the linear thermal model. First the instantaneous power dissipated in the device is calculated by taking the ratio of the temperature at the dT node and the linear thermal resistance as shown in (4.3). The second step is to calculate the junction temperature using the power calculated in (4.3) as shown in (4.4).

$$P_{\mathrm{lin}} = \frac{v_{\mathrm{dT}}}{R_{\mathrm{th}}} \tag{4.3}$$

$$\Delta T_{\mathrm{j}} = \frac{R_{\mathrm{th}}}{P_{\mathrm{lin}}} \tag{4.4}$$

where P_{lin} is the dissipated power in W of the device as calculated using the linear thermal model in the HICUM model, v_{dT} is the voltage at the dT node which is equivalent to temperature in thermal domain measured in K and R_{th} is the linear thermal resistance in K/W.

Chapter 5

RESULTS AND DISCUSSIONS

In this chapter the results of devices listed in table 4-1 after optimizations is presented and discussed. Two sets of results for each device is presented where the first set consists the optimized Forward Gummel (FG) and base voltage controlled output characteristics (output characteristics) using a non-linear thermal model and the second set of results consists of optimized setups using the linear thermal model. The junction temperature at various powers as dissipated by the device is calculated and plotted. Always the measurements of the devices are operated in their Safe Operating Area (SOA) limits in order to avoid any device degradation. Base current data below 1 ηA is excluded for all devices due to the presence of noise and limitations in the measuring equipment.

5.1 The 20 µm Device Results

5.1.1 Optimized Forward Gummel (FG) plots

The optimized results for the FG setup for a 20 µm device using the non-linear and linear thermal model are shown in figures 5-1 and 5-2 respectively. The measured and simulated collector current, I_C and the base current, I_B are plotted versus the base emitter voltage. The measured data for both the currents is denoted by the red dotted curves and the black dashed curve represents the simulated data. The absolute error between the measured and simulated data is calculated using equation (4.1) for I_C and I_B and is plotted on the secondary (right) vertical axis. The double dashed blue curve represents the absolute error in I_B and the double dashed red curve represents the absolute error in I_C.

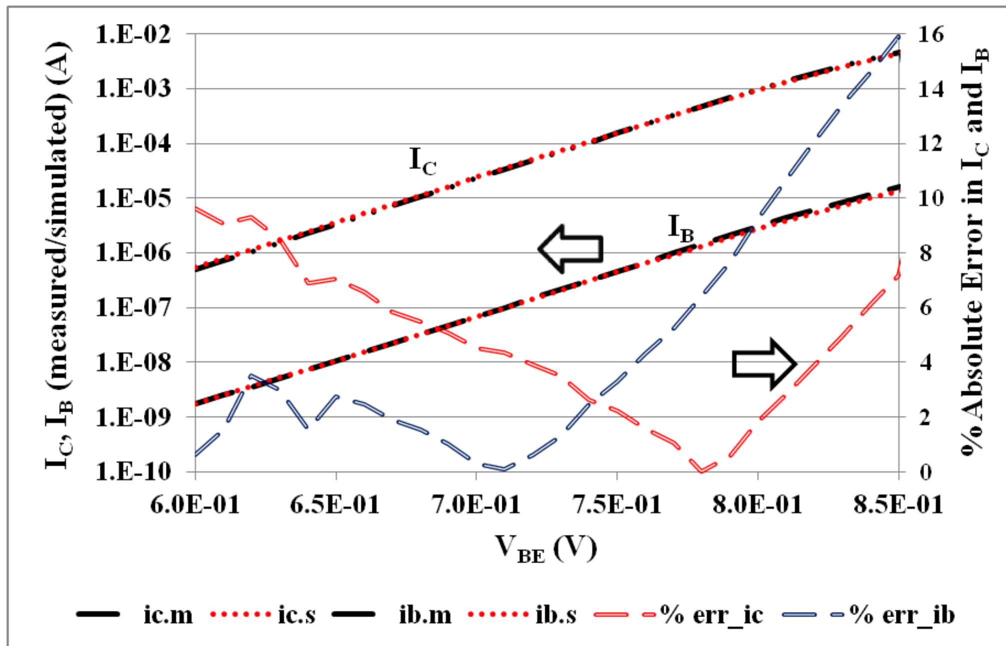

Figure 5-1: The optimized FG plot using the non-linear thermal model for a 20 µm device.

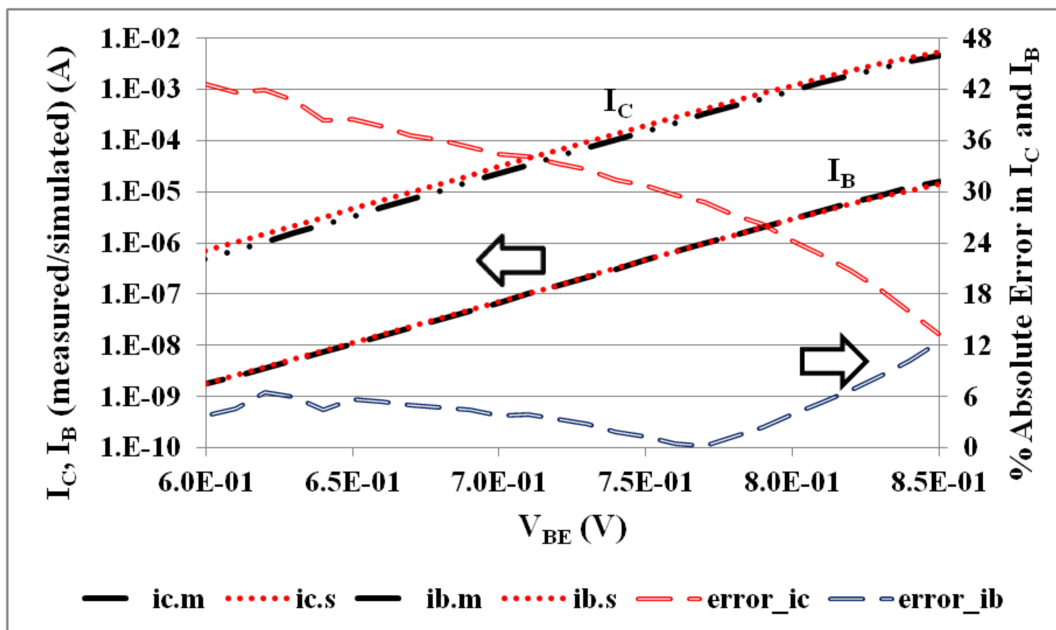

Figure 5-2: The optimized FG plot using the linear thermal model for a 20 µm device.

It is apparent from figures 5-1 and 5-2 that the absolute error in I_C for the non-linear model is substantially less compared to the linear model. The author believes the reason for the poor fit of the linear model is the model's inaccurate thermal resistance. For a larger device the power dissipation is substantial and a linear thermal resistance cannot model the thermal behavior of the device for the full

range of power dissipation. Hence, a non-linear model is needed to accurately model the thermal resistance and in turn the self-heating of the device.

5.1.2 Base voltage controlled output characteristics (output characteristics) plots

Figures 5-3 and 5-4 show the optimized output characteristics for the non-linear and linear thermal models respectively. The solid black curve and the dashed-dot black curve represent the I_C measured at different V_B while sweeping V_C from 0.2 to 2 V. The absolute error between the measured and simulated I_C values is plotted using the dotted and dashed curves. Only the maximum and the minimum absolute error curves have been displayed to reduce the clutter. For example, here the blue dotted curve represents the absolute error in I_C at V_{BE}=680 mV, the red dashed curve represents the absolute error in I_C at V_{BE}=840 mV and the lowermost red dotted curve represents the absolute error in I_C at V_{BE}=776 mV. The absolute error curves for the other V_{BE} values are between these maximum and minimum error curves.

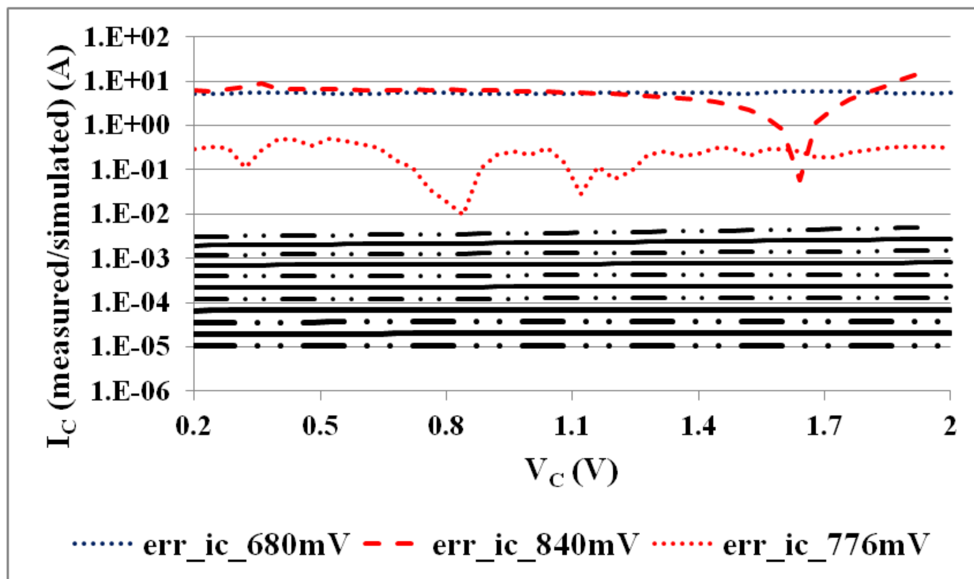

Figure 5-3: The plot of optimized output characteristics using the non-linear model for a 20 µm device. Here the black dashed-dot and black solid curves represents the I_C curves at V_{BE} = 560-840 mV in steps of 16 mV measured by sweeping V_C=0-2 V in steps of 40 mV.

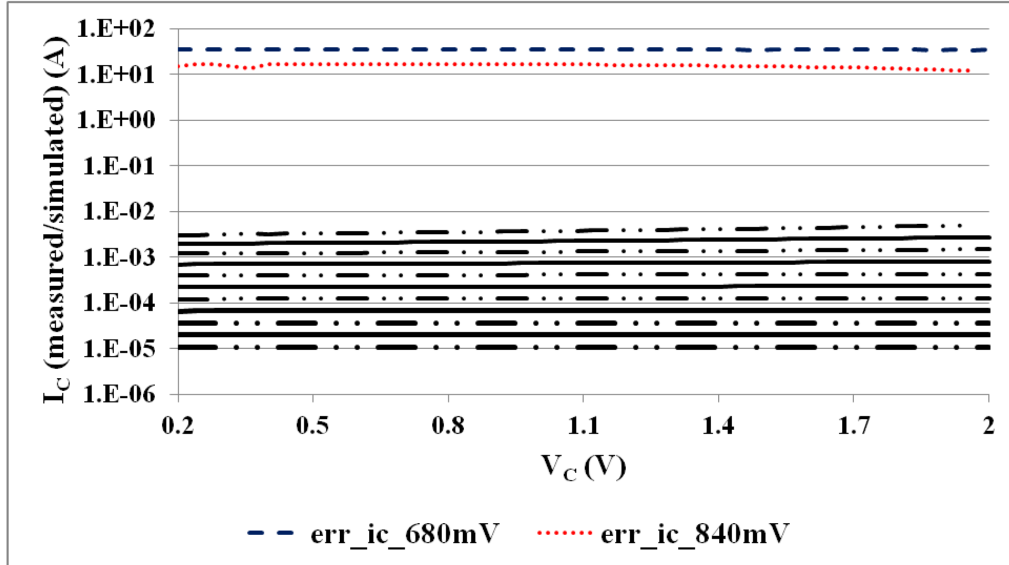

Figure 5-4: The plot of optimized output characteristics using the linear model for a 20 µm device. Here the black dashed-dot and black solid curves represents the I_C curves at V_{BE} = 560-840 mV in steps of 16 mV measured by sweeping V_C=0-2 V in steps of 40 mV.

The maximum absolute error in output characteristics, optimized using the non-linear thermal model, is substantially less compared to the linear thermal model. In this case as well the author believes the reason for the poor fit of the linear model is the model's inaccurate thermal resistance. For a larger device the power dissipation is substantial and a linear thermal resistance cannot model the thermal behavior of the device for the full range of power dissipation. Hence, a non-linear model is needed to accurately model the thermal resistance and in turn the self-heating of the device.

5.1.3 Junction temperature plot

The junction temperature as estimated by the non-linear and linear thermal models is plotted in figure 5-5. At maximum power dissipation the difference in the temperature estimation by the non-linear and the linear thermal model is 17 °C. Since the FG and output characteristics data are accurately modeled by the non-linear thermal model compared to the linear model it is apparent that the temperature estimation by the non-linear model is accurate as well.

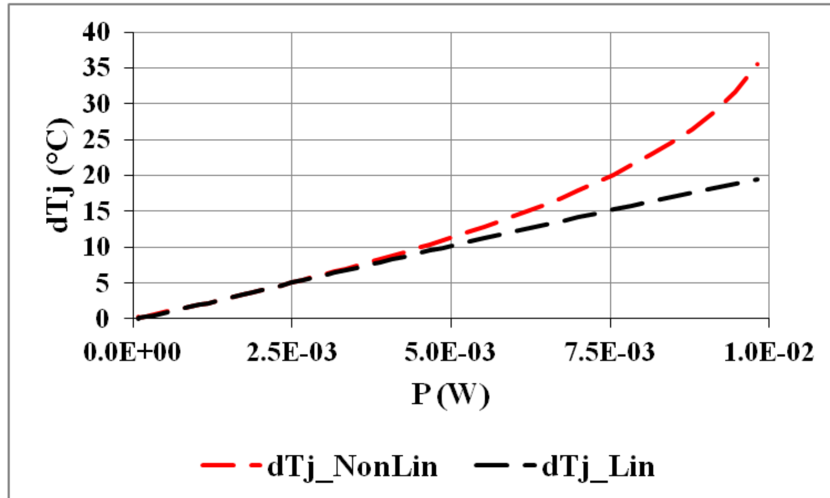

Figure 5-5: The plot of the junction temperature calculated using the non-linear and linear thermal models for a 20 µm device.

5.1.4 Current gain, β

Current gain is a critical device parameter for circuit designers. It is maximum for a range of V_{BE} values and decreases on either side of the optimum V_{BE}. This was explained in section 3.4.4. This trend is visible from figures 5-6 and 5-7 for the non-linear thermal model and linear thermal model respectively.

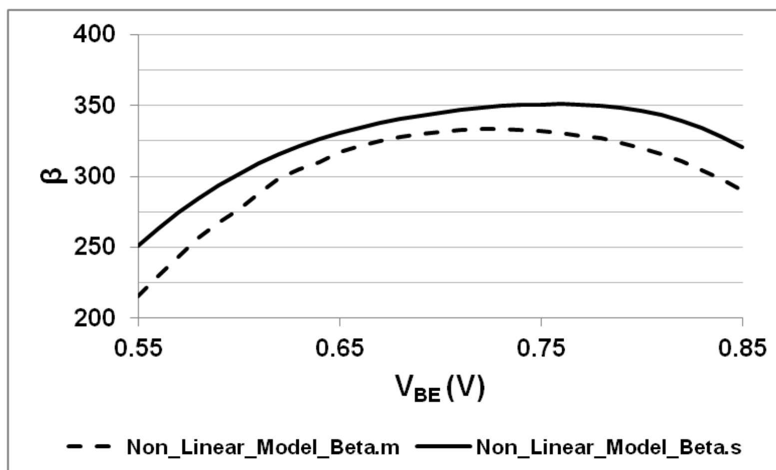

Figure 5-6: The plot of current gain, *β*, versus base-emitter voltage for the non-linear thermal model for a 20 µm device.

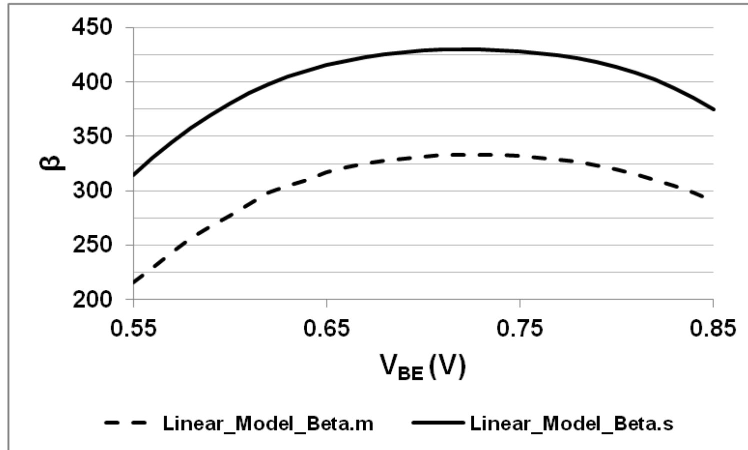

Figure 5-7: The plot of current gain, β, versus base-emitter voltage for the linear thermal model for a 20 μm device.

It is apparent from figure 5-6 and 5-7 that the current gain estimation using the linear model is inaccurate compared to the non-linear model. The linear thermal model estimates the current gain to be much higher than what it is in reality. Such a high error in gain estimation can lead to circuit designs that will not only under-perform but even fail to meet the final objective for which it is designed.

5.2 The 0.8 μm Device

5.2.1 Optimized Forward Gummel (FG) plots

The optimized results for the FG setup for a 0.8 μm device using the non-linear and linear thermal model are shown in figures 5-8 and 5-9 respectively. The measured and simulated collector current, I_C and the base current, I_B are plotted versus the base emitter voltage. The measured data for both the currents is denoted by the red dotted curves and the black dashed curve represents the simulated data. The absolute error between the measured and simulated data is calculated using equation (4.1) for I_C and I_B and is plotted on the secondary (right) vertical axis. The double dashed blue curve represents the absolute error in I_B and the double dashed red curve represents the absolute error in I_C.

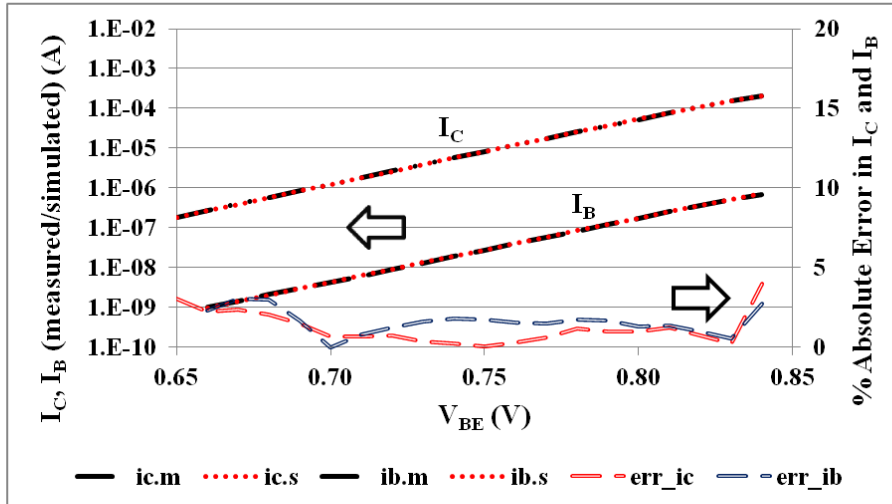

Figure 5-8: The optimized FG plot using the non-linear thermal model for a 0.8 μm device.

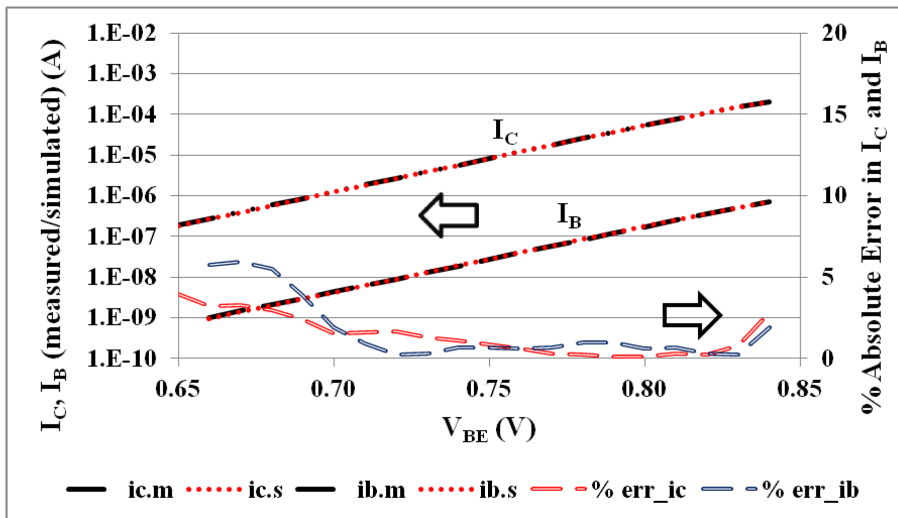

Figure 5-9: The optimized FG plot using the linear thermal model for a 0.8 μm device.

It is apparent from figures 5-8 and 5-9 that the absolute error in I_C and I_B data modeled using both the non-linear thermal model and the linear thermal model is identical.

5.2.2 Base voltage controlled output characteristics (output characteristics) plots

Figures 5-10 and 5-11 show the optimized output characteristics for the non-linear and linear thermal models respectively. The solid black curve and the dashed-dot black curve represent the I_C measured at different V_B while sweeping V_C from 0.2 to 2 V. The absolute error between the measured and simulated I_C values is plotted using the dotted and dashed curves. Only the maximum and the

minimum absolute error curves have been displayed to reduce the clutter. For example, here the purple dotted curve represents the absolute error in I_C at V_{BE}=680 mV, the red dotted curve represents the absolute error in I_C at V_{BE}=744 mV and the lowermost blue dashed curve represents the absolute error in I_C at V_{BE}=728 mV. The absolute error curves for the other V_{BE} values are between these maximum and minimum error curves.

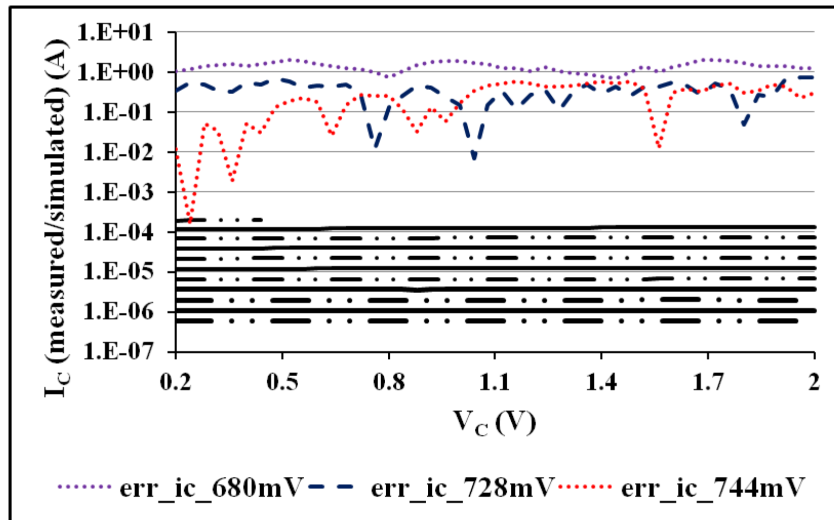

Figure 5-10: The plot of optimized output characteristics using the non-linear model for a 0.8 µm device. Here the black solid and black dashed-dot curves represents the I_C curves at V_{BE} = 560-840 mV in steps of 16 mV measured by sweeping V_C = 0-2 V in steps of 40 mV.

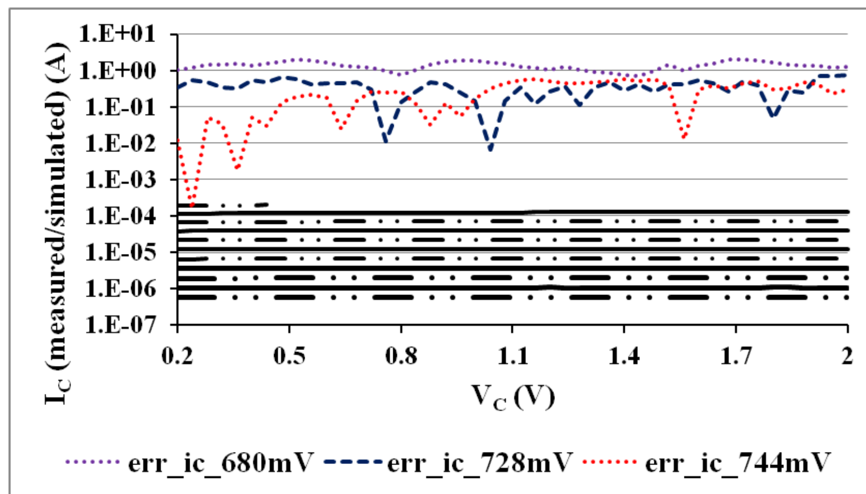

Figure 5-11: The plot of optimized output characteristics using the linear model for a 0.8 µm device. Here the black solid and black dashed-dot curves represents the I_C curves at V_{BE} = 560 mV to 840 mV in steps of 16 mV measured by sweeping V_C = 0 to 2 V in steps of 40 mV.

It is apparent from figures 5-10 and 5-11 that the absolute error in I_C and I_B data modeled using both the non-linear thermal model and the linear thermal model is identical.

5.2.3 Junction temperature estimation

The junction temperature as estimated by the non-linear and linear thermal models is plotted in figure 5-12. At maximum power dissipation the difference in the junction temperature estimation by the non-linear and the linear thermal model is ~0.23 °C. Even though the difference in junction temperature estimation by both these models is small, it constitutes an error of ~9% at the maximum dissipated power.

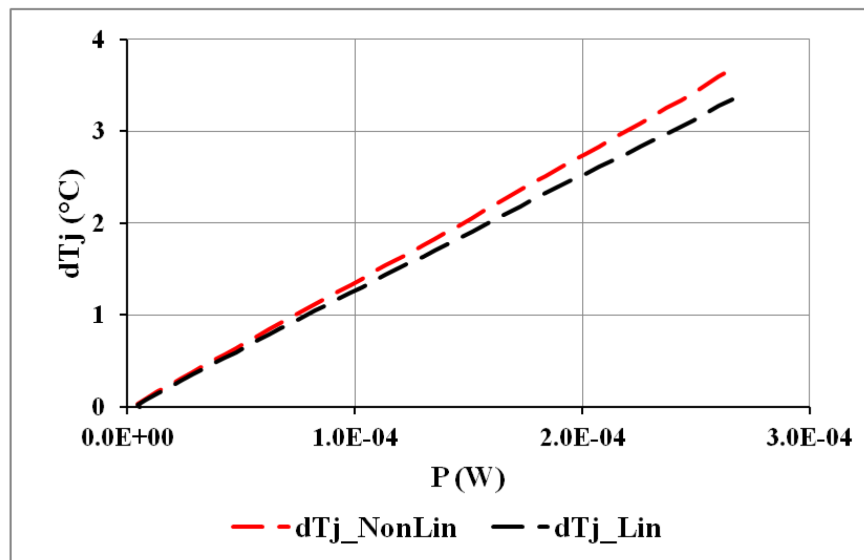

Figure 5-12: The plot of the junction temperature calculated using the non-linear and linear thermal models for a 0.8 μm device.

5.2.4 Current gain (β)

The plots of current gain, β, versus the base-emitter voltage using the non-linear and linear thermal models for optimizations are shown in figure 5-13 and 5-14. Current gain estimation performed by both the thermal models is identical. Hence, it can be inferred that for a smaller device either thermal model can be used for device optimization as far as current gain estimation is to be performed.

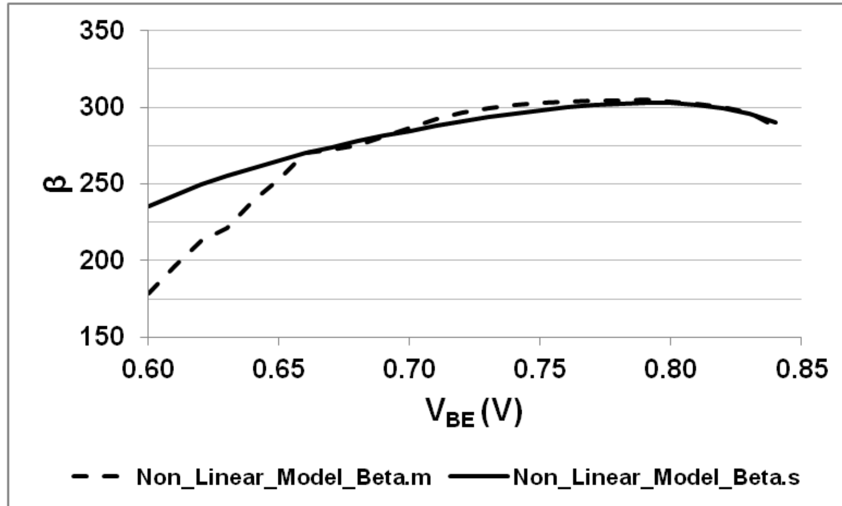

Figure 5-13: The plot of current gain, β, versus base-emitter voltage for the non-linear thermal model for a 0.8 μm device.

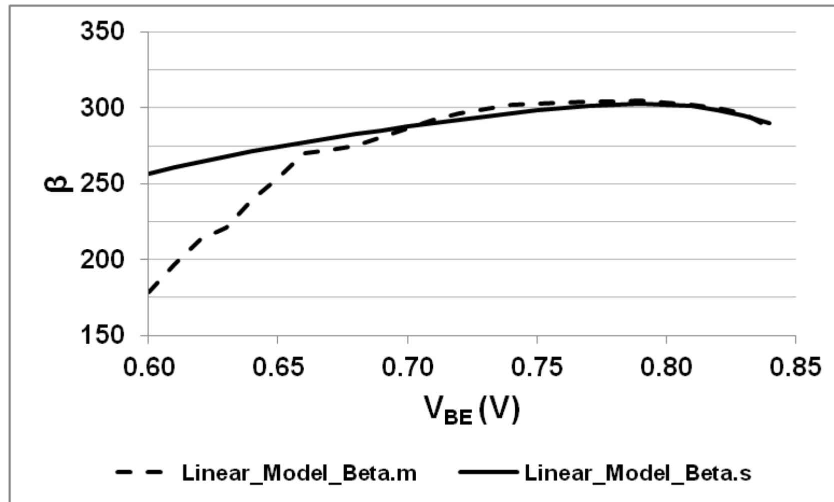

Figure 5-14: The plot of current gain, β, versus base-emitter voltage for the linear thermal model for a 0.8 μm device.

5.3 Summary of results

The maximum junction temperature of the devices estimated by both the thermal models at maximum power is listed in table 5-1. The difference in junction temperature estimation by both the models is denoted by ΔdT_{j_max}. The expression used to calculate this difference is given in (5.1). The expression used to calculate the %error in estimation of junction temperature using the non-linear thermal and linear thermal model is shown in (5.2). The %error for the smaller devices is around 9%. As the device size is increased the %error grows bigger and the 20 μm device has the largest %error. A distinction can be made between these devices based on the error in estimation of the junction

temperature based on the two thermal models. In table 5-1, the smaller devices i.e.: 0.4 µm through 1 µm can be grouped together and the larger devices i.e.: 5 µm through 20 µm can be grouped in the other. Equation (5.1) shows how the difference in temperature estimation was calculated for the two thermal models. The percentage difference between these two thermal models is calculated using (5.2).

$$\Delta dT_{\text{j_max}} = \left(dT_{\text{j_max}}\right)_{\text{non-linear-model}} - \left(dT_{\text{j_max}}\right)_{\text{linear-model}} \tag{5.1}$$

$$\%\,\text{Difference}\ _\,\text{d}T_{\text{j}}\text{_estimation} = \frac{\Delta dT_{\text{j_max}}}{\left(dT_{\text{j_max}}\right)_{\text{non-linear-model}}} \times 100 \tag{5.2}$$

Table 5-1: SUMMARY OF JUNCTION TEMPERATURE FOR VARIOUS DEVICES USING LINEAR AND NON-LINEAR THERMAL MODEL

Device	**dT_j_Max (°C) (Linear Model)**	**dT_j_Max (°C) (Non-Linear Model)**	**Δ(dT_{j_Max}) (°C)**	**Difference in dT_j Estimation (%)**
0.4 µm	2.446	2.673	0.23	8.49
0.6 µm	2.75	2.94	0.19	6.39
0.8 µm	3.35	3.681	0.33	9.05
1 µm	3.92	4.273	0.36	8.31
5 µm	13.39	16.3	2.91	17.85
10 µm	14.76	18.86	4.1	27.74
20 µm	19.49	35.51	16.02	45.11

The difference of junction temperature estimation by the two thermal models versus the device dimensions is shown in figure 5-15. A second order polynomial trend is used to perform the curve fitting. This equation can be used to predict the junction temperature difference between two thermal models for a device while performing the device scaling. The plot of junction temperature estimation by the two thermal models versus the inverse of the device dimensions is shown in figure 5-16.

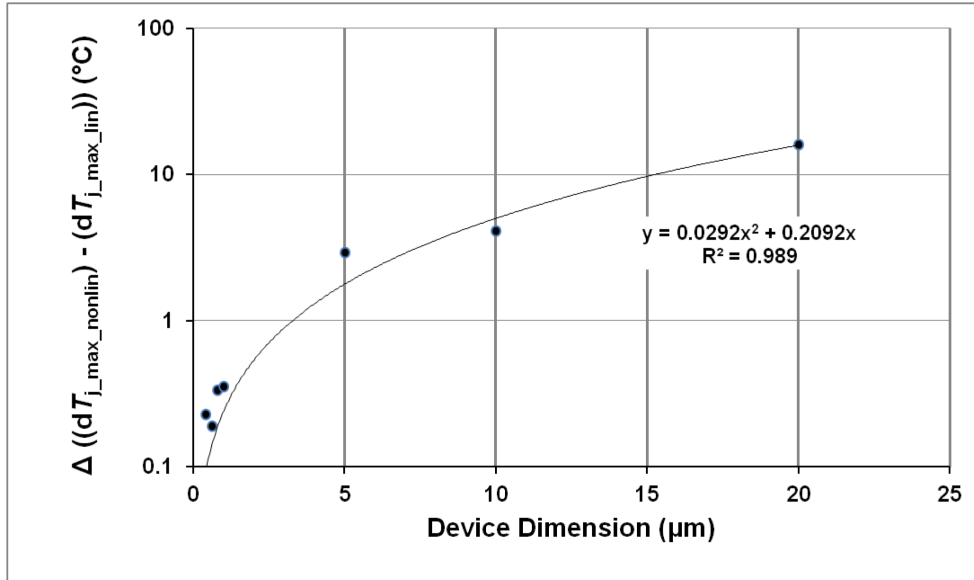

Figure 5-15: The plot of difference in junction temperature as estimated by linear and non-linear thermal model versus the device dimensions.

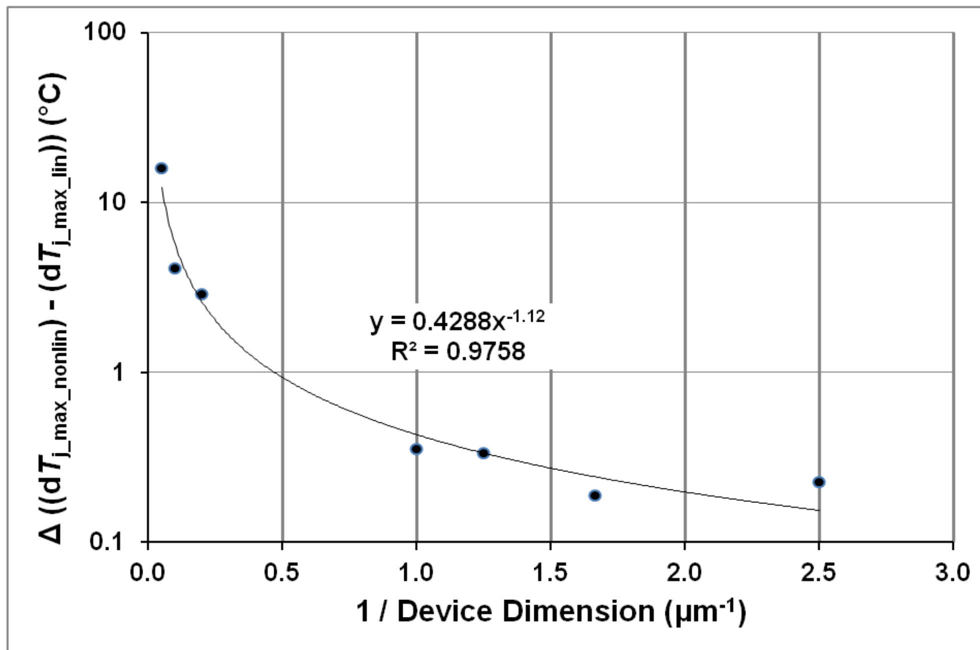

Figure 5-16: The plot of difference in junction temperature as estimated by linear and non-linear thermal model versus the inverse of device dimensions.

The summary of thermal resistance used in the linear thermal model, R_{th}, and R_0, and *dRdP* used in the non-linear thermal model for various devices is given in table 5-2. Thermal resistance is calculated at the maximum power using equation (3.13) and is denoted by R_{max}. R_{max} for various devices is also listed in table 5-2. R_0 and R_{max} together give the range of the thermal resistance variation of the device.

Table 5-2: SUMMARY OF THERMAL RESISTANCE AND *dRdP* FOR VARIOUS DEVICES USING LINEAR AND NON-LINEAR THERMAL MODEL

Device	R_{th} (K/W) (Linear Model)	R_0 (K/W) (Non-Linear Model)	*dRdP* (K/W^2) (Non-Linear Model)	R_{max} (K/W) (Non-Linear Model)
0.4 µm	17450	17880	7.315×10^6	18928
0.6 µm	14770	14790	5.067×10^6	15737
0.8 µm	13190	13160	2.216×10^6	13749
1 µm	13120	14150	0.878×10^6	14413
5 µm	6719	5070	1.206×10^6	7406
10 µm	3707	3700	0.162×10^6	4335
20 µm	1818	1955	0.089×10^6	2833

The trend of R_0 and R_{th} as a function of device dimension is shown in figure 5-17. The trend that both the thermal models show is almost identical. This trend can be used for predicting the thermal resistance for a hypothetical device fabricated using the same technology. A similar plot showing the trend of R_0 and R_{th} as a function of the reciprocal of the device dimension is shown in figure 5-18. A benefit of plotting the thermal resistance as a function of inverse of device dimensions is that it gives clearer information of the trend for the smaller devices.

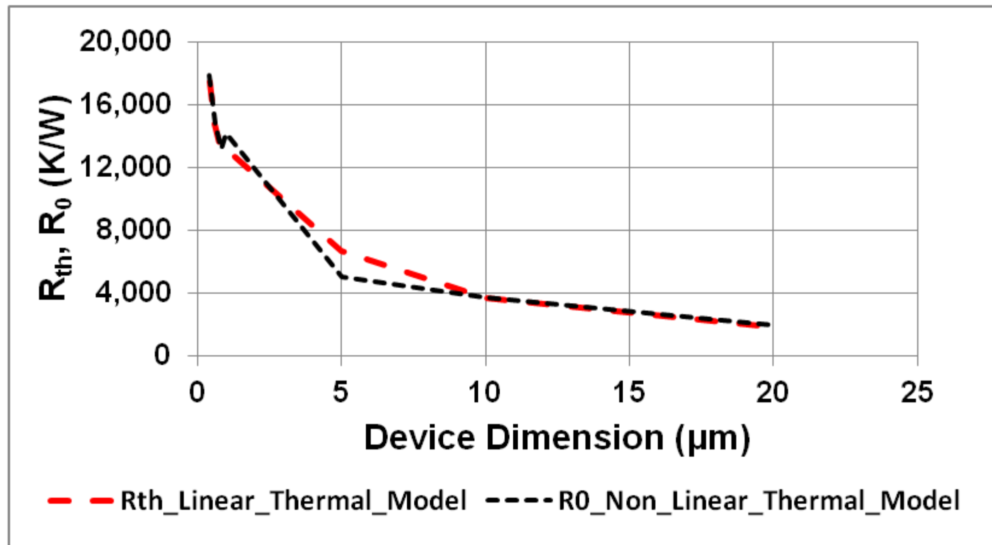

Figure 5-17: A plot showing the trend of R_0 and R_{th} as a function of device dimension.

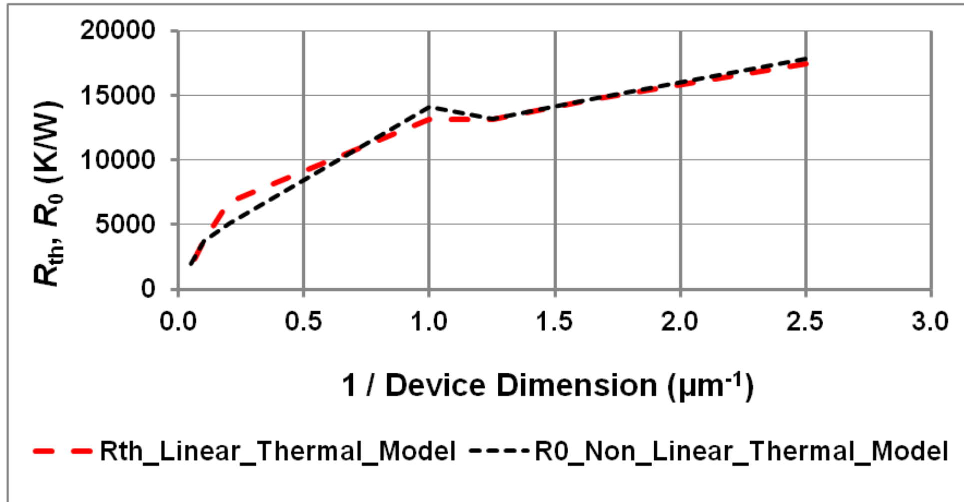

Figure 5-18: A plot showing the trend of R_0 and R_{th} as a function of device dimension.

The plot of *dRdP* versus the device dimensions and inverse of device dimensions is given in figures 5-19 and 5-20 respectively.

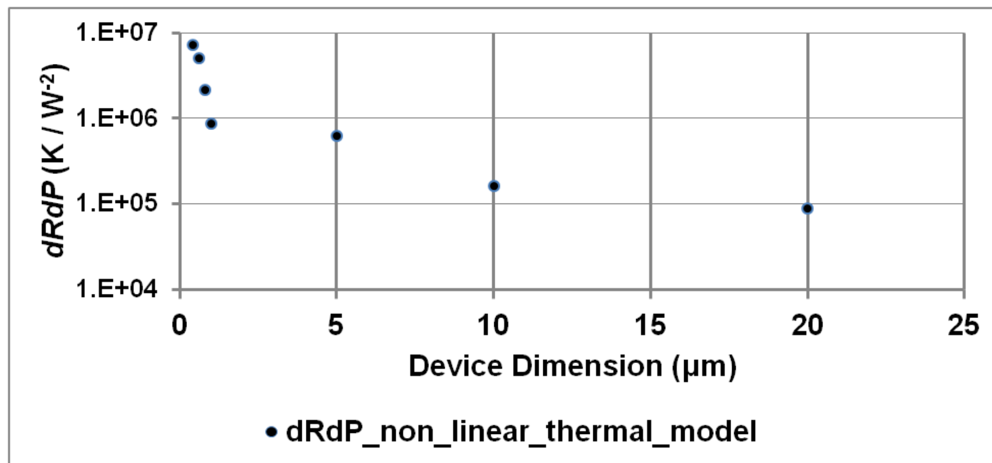

Figure 5-19: A plot showing the trend of *dRdP* as a function of device dimensions.

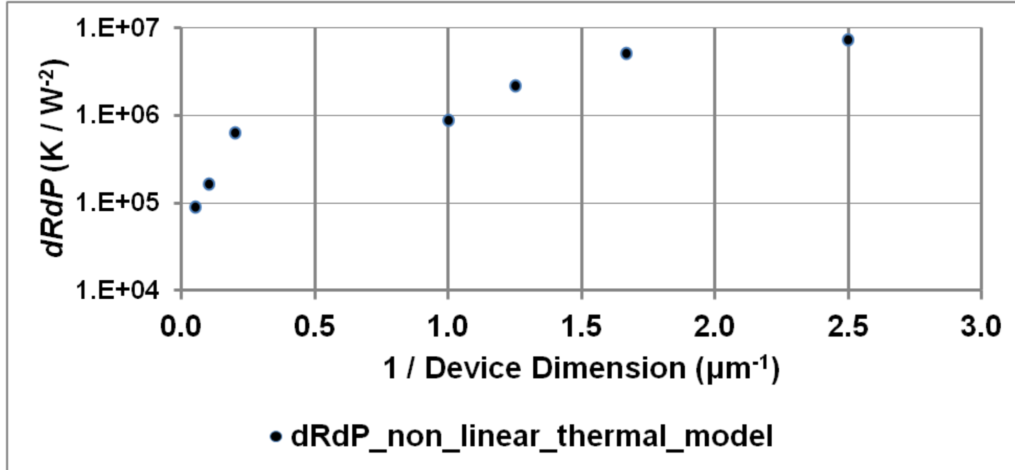

Figure 5-20: A plot showing the trend of *dRdP* as a function of inverse of device dimensions.

5.4 Effect of error in junction temperature estimation on gain drift

Gain error is a critical parameter in design of the Analog-to-Digital Converter (ADC). Gain error in ADCs is a temperature dependent parameter and the variation in gain is specified as gain drift and denoted as ppm/°C. The actual gain error at any temperature can be calculated by adding the gain drift to the gain error value calculated at the room temperature. For example, for a typical 16-bit ADC, if the gain error is (+ 4) LSB (Least Significant Bit), then it is converted to Volts as shown in equation (5.3). If the maximum voltage input to this 16-bit ADC is 5 V then the gain error in Volts for this ADC is calculated and shown in (5.4).

$$\text{Gain_Error_Volts} = \text{Error_in_LSB} \times \frac{\text{Maximum_Input_Voltage}}{2^{(\text{number_of_bits})}} \tag{5.3}$$

$$\text{Gain_Error_Volts} = 4 \times \frac{5}{2^{(16)}} = 0.000305 \tag{5.4}$$

This means the ADC code will reach 0xFFFF for an input voltage of (5.0 - 0.000305) = 4.999695 V. If the gain error is (- 4) LSB, then the device will reach 0xFFFF code for an input voltage (5.0 + 0.000305) = 5.000305 V.

$$\text{Gain_Error_(\%FSV)} = \text{Gain_Error(V)} \times (100/\text{Full_Scale_Value}) \tag{5.5}$$

$$\text{Gain_Error_(\%FSV)} = 0.000305 \times (100/5) = 0.0061\% \tag{5.6}$$

Both the offset error and gain error are usually specified at 25° C in datasheets. Also the gain error and the offset error vary with temperature. The variation in gain is specified as Gain Drift and denoted as ppm/°C. The actual gain error at any temperature can be calculated by adding the drift to gain error calculated at 25 °C (room temperature). For example, if the drift is specified as 1 ppm/°C then the gain drift can be denoted in voltage as 1 μV per 1 V (since 1 ppm of 1 V = 1 μV). Now, the error in estimating the junction temperature will result in incorrect estimation of the gain. For example, for a 20 μm device the estimated junction temperature using the non-linear thermal model is 35.51° at maximum power. The gain drifts are calculated using the junction temperature estimated by the non-linear and the linear thermal models and are shown in (5.7) and (5.8) respectively. A significant gain drift error will occur by using the linear model to estimate the junction temperature. The gain drift as calculated in (5.7) results in a + 6 LSB error compared to +4 LSB error that the ADC was designed for initially. It a 50 % increase in the LSB error.

$$\text{Gain_Drift (at } 35.51^{\circ}\text{C)} = (305\,\mu\text{V}) + [(35.51 - 25) \times 5\,\mu\text{V}] = 357.6\,\mu\text{V} \tag{5.7}$$

$$\text{Gain_Drift (at } 19.49^{\circ}\text{C)} = (305\,\mu\text{V}) + [(19.49 - 25) \times 5\,\mu\text{V}] = 277.5\,\mu\text{V} \tag{5.8}$$

Chapter 6

CONCLUSIONS AND FUTURE RESEARCH

In the first part of this dissertation, device physics and compact modeling of a SiGe HBT in the presence of self-heating were investigated. The second part of the work includes the design of a timing circuit using a phased locked loop.

Chapter 1 contrasted the Si BJT and SiGe HBT with the motivation behind this research. SiGe HBTs are deployed in high speed and high performance environments. Thorough understanding of figures of merit of a device helps in accurate circuit design. Most of the critical figures of merit of a high speed, high performance and robust system built using silicon material show strong temperature dependence. A brief overview of these figures of merit is presented in this chapter.

Chapter 2 analyzed the device physics concept that lies behind designing a hetero-junction bipolar transistor. Effects of germanium (Ge) addition to the silicon device parameters such as charge modulation in base, current gain, β, output conductance, Early voltage, device transition frequency and base transit time are discussed. It is inferred from the data as reported by several authors that addition of Ge in the base of a BJT produces positive influence on the device operation which includes higher current gain, β, larger Early voltage, lower base transit time and higher cut-off (transition) frequency.

Chapter 3 provides an overview of the self-heating effect in HBTs. It also discusses the effect of self-heating on device parameters such as band-gap, density of states, carrier mobility and current gain. It is apparent from the data that these parameters are very sensitive to temperature. An inaccurate knowledge of the device temperature will lead to error in estimation of these critical device parameters. The operating temperature of the device depends on the power dissipated in the device. For a HBT operated in the active region, the reverse-biased base-collector (BC) junction is the dominant source of power dissipation. Hence, the temperature of reverse-biased BC junction dictates the temperature of the device. Since thermal resistance of a device is not constant with respect to power, a linear model is inadequate to model the self heating effect accurately. Hence, a non-linear thermal model which is a function of power and calculated using the measured quantities (i.e.: current and voltage) is proposed to

replace the linear thermal model modeling self heating. Compact models such as Spice Gummel Poon (SGP) model, Vertical Bipolar Inter-Company (VBIC) model, HIgh Current Model (HICUM) and MEXTRAM model are used in device modeling and characterization programs to estimate the device parameters at the applied bias conditions. In this research the HICUM compact model is used for device modeling and characterization. In the HICUM model a linear thermal model as a function of power (dissipated in the device) is used to model self heating. The details of the devices used for measurements and the measurement setups are provided in chapter 4. Chapter 4 concludes with the optimization procedure used to optimize the data obtained from the measurements.

A summary of results for the devices under test is given in chapter 5. Two different trends can be seen from the optimized results. The larger devices (i.e.: 5 μm, 10 μm and 20 μm) showed one trend of thermal resistance whereas the smaller devices (i.e.: 0.4 μm, 0.6 μm, 0.8 μm and 1 μm) showed another. From the optimized forward Gummel and the base voltage controlled output characteristics plots for a 20 μm device it is apparent that the non-linear thermal model is more accurate in modeling the thermal resistance compared to the linear thermal model. The same trend was observed for the other large devices. For the smaller devices the error in the forward Gummel and output characteristics optimizations using both the thermal models was identical.

The junction temperature estimation for the larger devices by the two thermal models showed a substantial difference. A 10% error in temperature estimation between the thermal models was observed for the smaller devices. The reason for the non-linear thermal model to be accurate is that the thermal resistance for this model is re-calculated at every instantaneous power whereas in the linear thermal model it is constant. Moreover, one of the reasons for high junction temperature of the 20 μm device is its scaling. Generally, the device dimensions are scaled in x and y directions. The height or thickness (z direction) of all the layers does not change. Hence, the overall volume in which heat can spread does not increase as rapidly as the area of the device. This leads to heat confinement in a SOI based device. The trend of both R_0 and $dRdP$ is that they tend to decrease with the increase in device dimensions.

The 3D TCAD simulations can be performed and the thermal resistance values estimated by these simulations can be compared to the proposed non linear thermal model. The advantages of 3D TCAD simulations are: it can model a 3-dimentional device with actual layout of different layers of the device and each of these layers can be modeled independently with their dimensions, conductivity, doping etc. Hence, the heat spreading inside the device can be estimated which eventually leads to the rise in junction temperature.

The future research in this area also includes the application of non linear thermal model to the time domain measurements where the devices are biased in common emitter configuration. Here, a pulse input is applied to the base terminal and the output is collected from the collector terminal. At the output, a thermal tail is observed which results due to the transients that occurs during the switching. Finally, the frequency domain measurement can be performed using these devices. The application of the non linear thermal model will provide a better way to model self-heating with change in operating frequency of the device.

APPENDIX A

ADDITIONAL PLOTS

A.1 The 0.4 μm device

A.1.1 Forward Gummel results

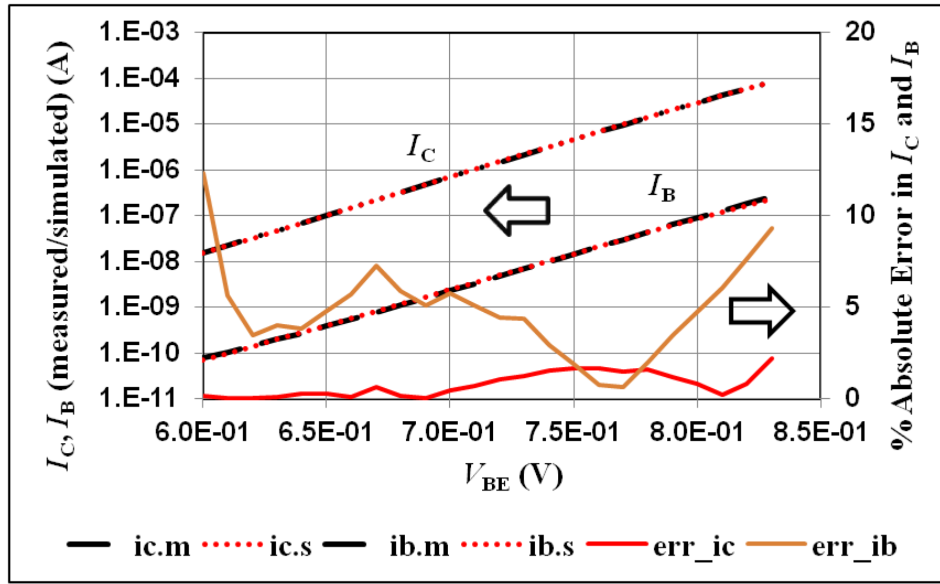

Figure A - 1: The optimized FG plot using the non-linear thermal model for a 0.4 μm device.

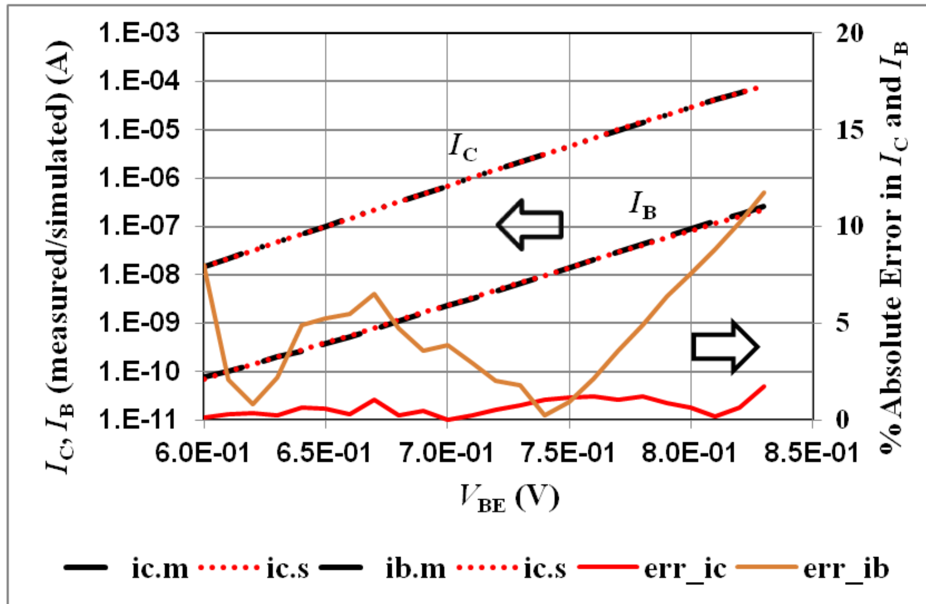

Figure A - 2: The optimized FG plot using the linear thermal model for a 0.4 µm device.

A.1.2 Base voltage controlled output characteristics results

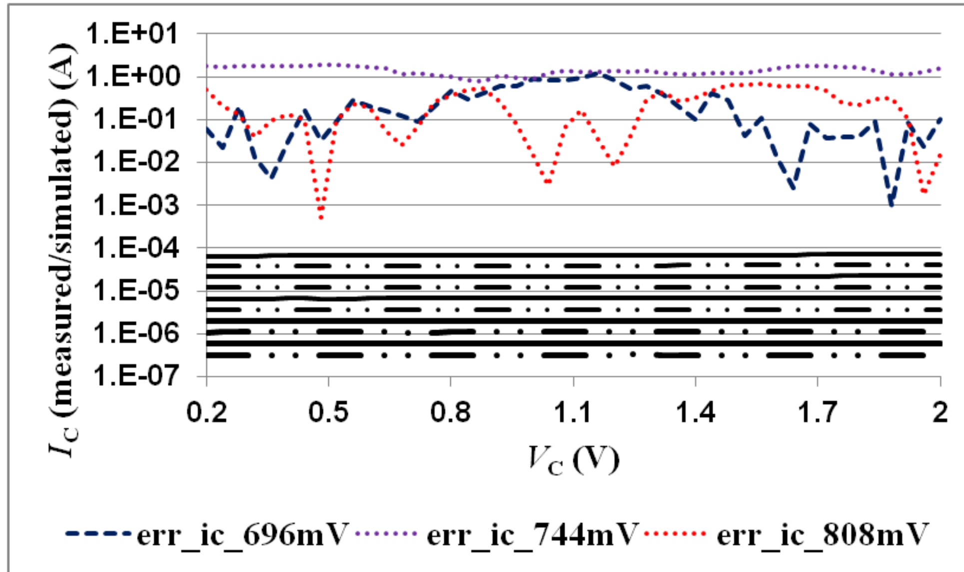

Figure A - 3: The plot of optimized output characteristics using the non-linear model for a 0.4 µm device. Here the black dashed-dot and black solid curves represents the I_C curves at V_{BE} = 560-840 mV in steps of 16 mV measured by sweeping V_C=0-2 V in steps of 40 mV.

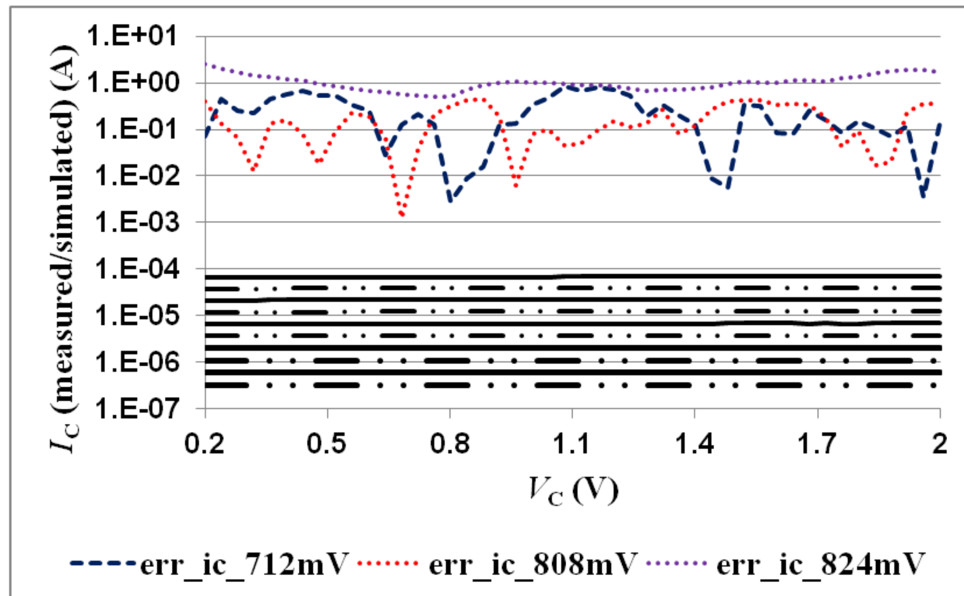

Figure A - 4: The plot of optimized output characteristics using the linear model for a 0.4 µm device. Here the black dashed-dot and black solid curves represents the I_C curves at V_{BE} = 560-840 mV in steps of 16 mV measured by sweeping V_C=0-2 V in steps of 40 mV.

A.1.3 Current gain, β

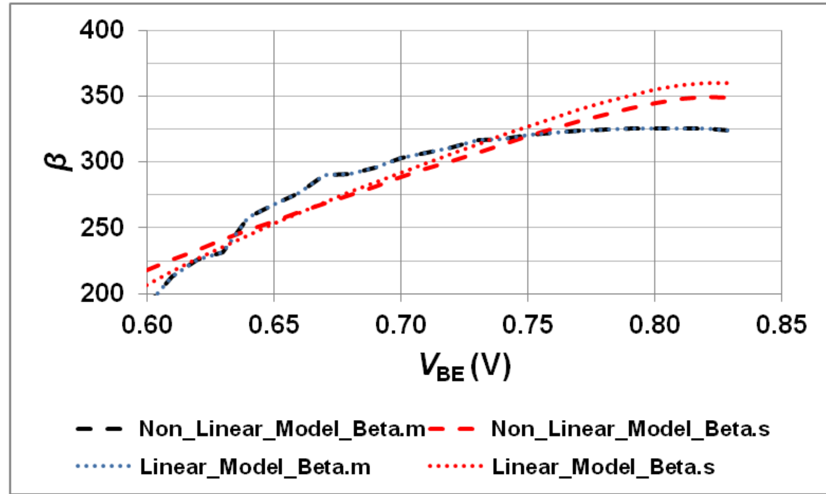

Figure A - 5: The plot of current gain, *β*, versus base-emitter voltage calculated using the non-linear and the linear thermal model for a 0.4 µm device.

A.1.4 Junction temperature estimation

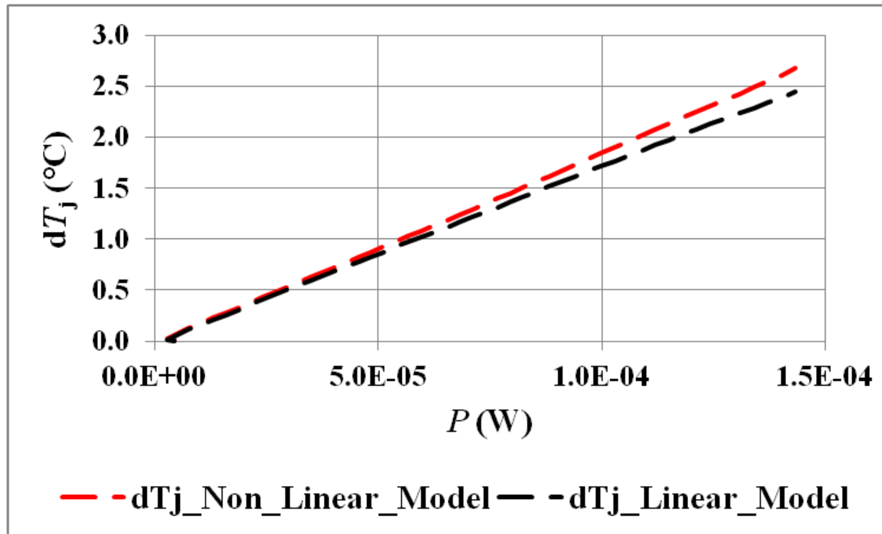

Figure A - 6: The plot of the junction temperature calculated using the non-linear and the linear thermal models for a 0.4 µm device.

A.2 The 0.6 μm device

A.2.1 Forward Gummel results

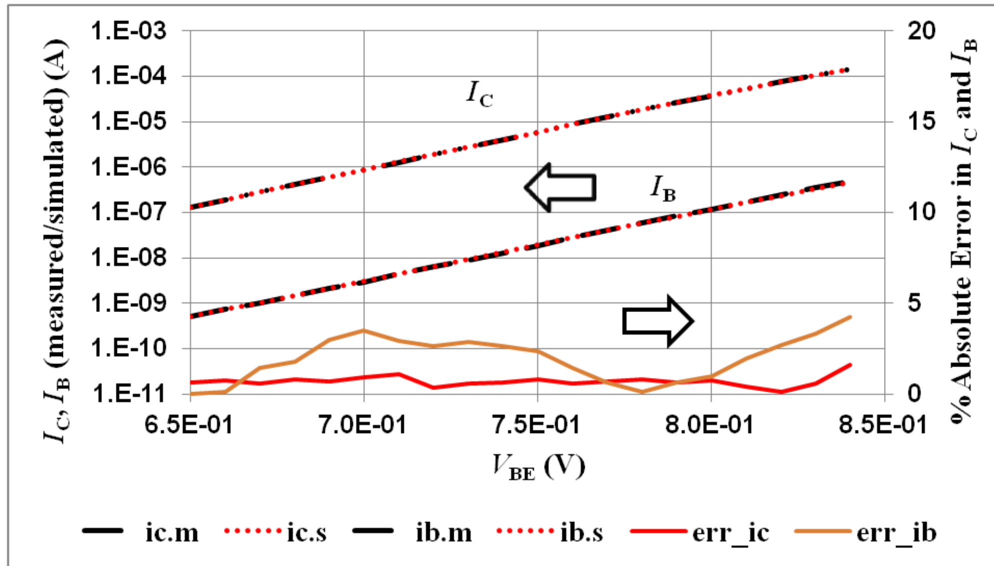

Figure A - 7: The optimized FG plot using the non-linear thermal model for a 0.6 μm device.

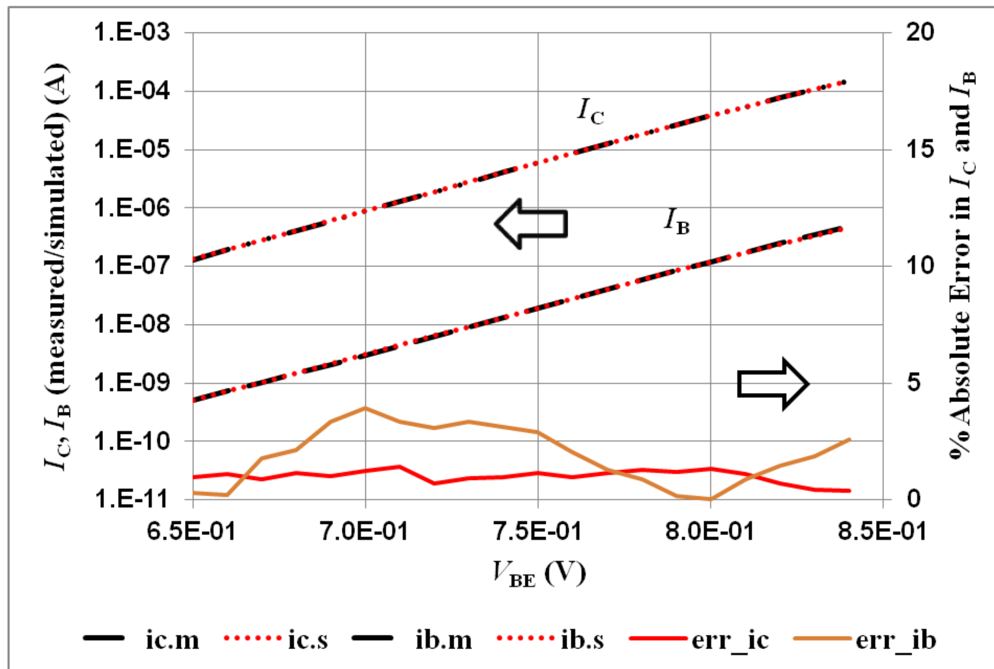

Figure A - 8: The optimized FG plot using the linear thermal model for a 0.6 μm device.

A.2.2 Base voltage controlled output characteristics results

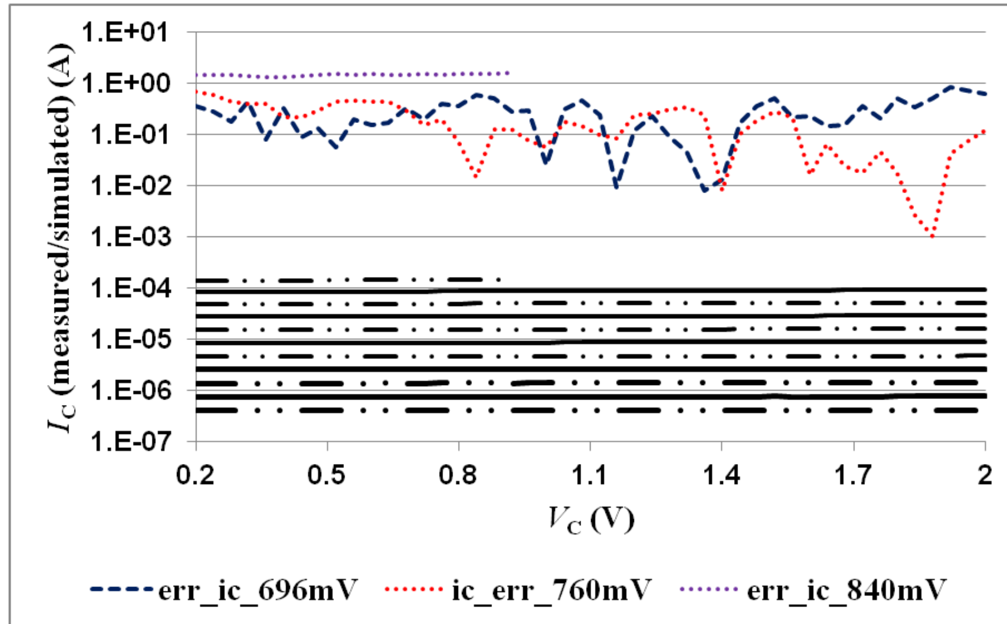

Figure A - 9: The plot of optimized output characteristics using the non-linear model for a 0.6 µm device. Here the black dashed-dot and black solid curves represents the I_C curves at V_{BE} = 560-840 mV in steps of 16 mV measured by sweeping V_C=0-2 V in steps of 40 mV.

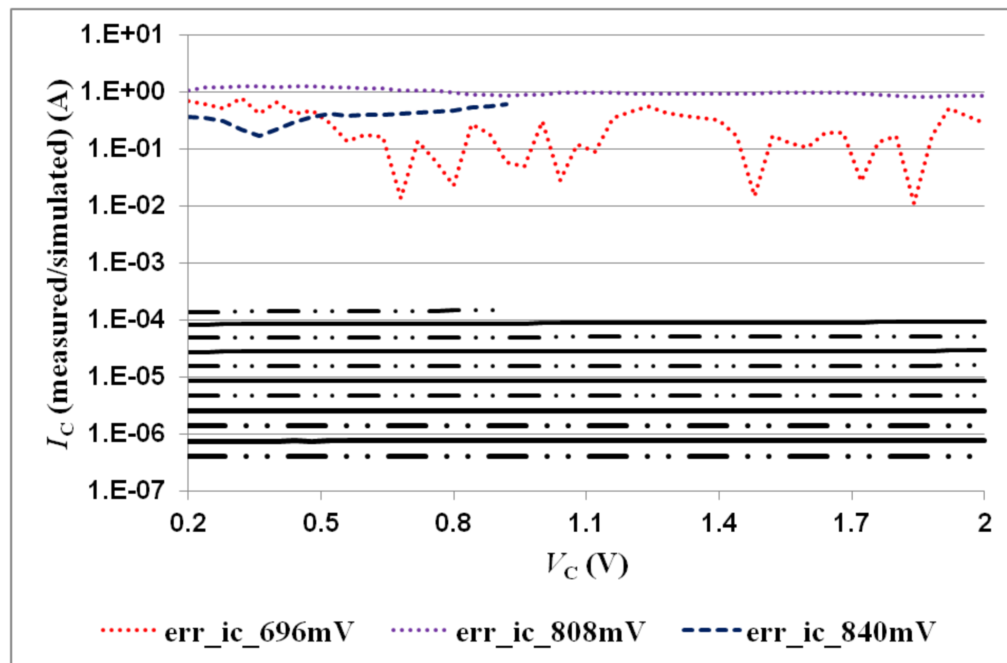

Figure A - 10: The plot of optimized output characteristics using the linear model for a 0.6 µm device. Here the black dashed-dot and black solid curves represents the I_C curves at V_{BE} = 560-840 mV in steps of 16 mV measured by sweeping V_C=0-2 V in steps of 40 mV.

A.2.3 Current gain, β

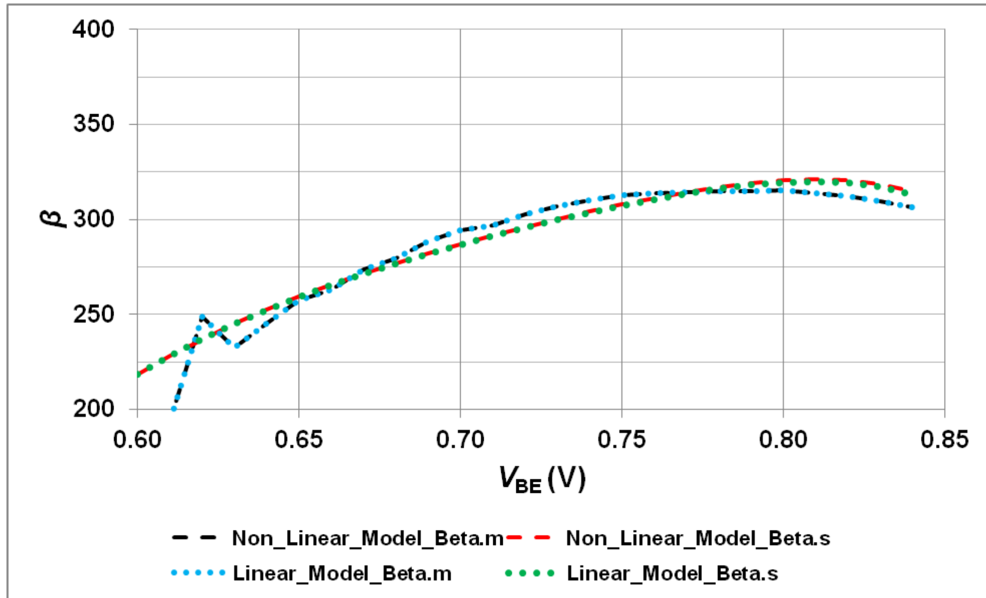

Figure A - 11: The plot of current gain, *β*, versus base-emitter voltage calculated using the non-linear and the linear thermal model for a 0.6 μm device.

A.2.4 Junction temperature estimation

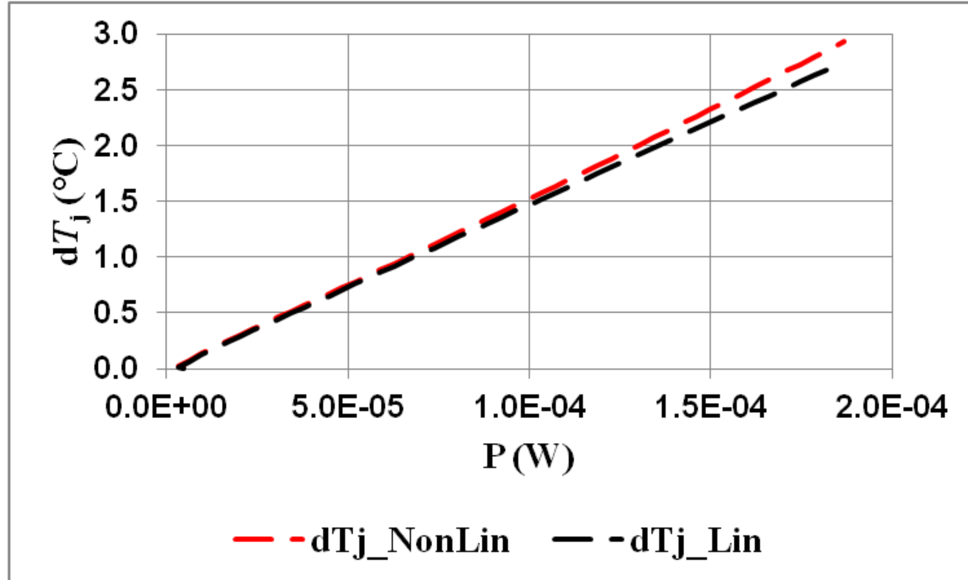

Figure A - 12: The plot of the junction temperature calculated using the non-linear and the linear thermal models for a 0.6 μm device.

A.3 The 1 μm device

A.3.1 Forward Gummel results

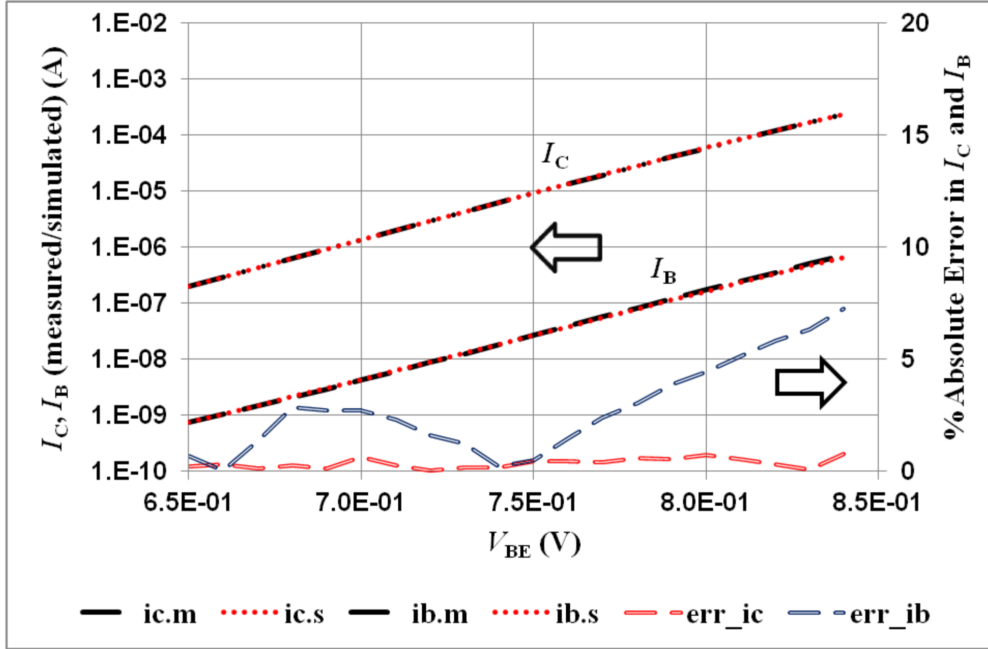

Figure A - 13: The optimized FG plot using the non-linear thermal model for a 1 μm device.

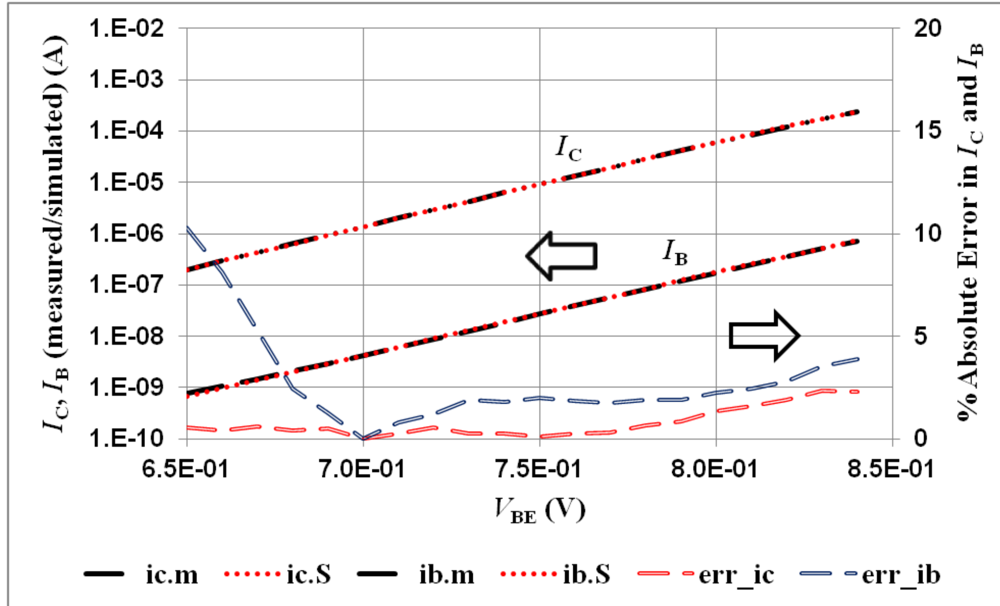

Figure A - 14: The optimized FG plot using the linear thermal model for a 1 μm device.

A.3.2 Base voltage controlled output characteristics results

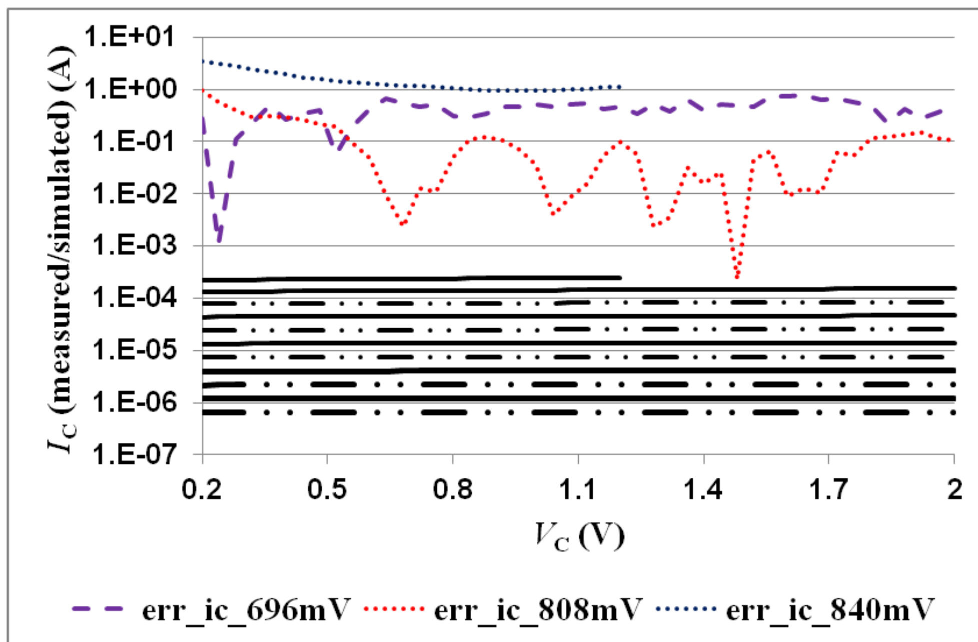

Figure A - 15: The plot of optimized output characteristics using the non-linear model for a 1 μm device. Here the black dashed-dot and black solid curves represents the I_C curves at V_{BE} = 560-840 mV in steps of 16 mV measured by sweeping V_C=0-2 V in steps of 40 mV.

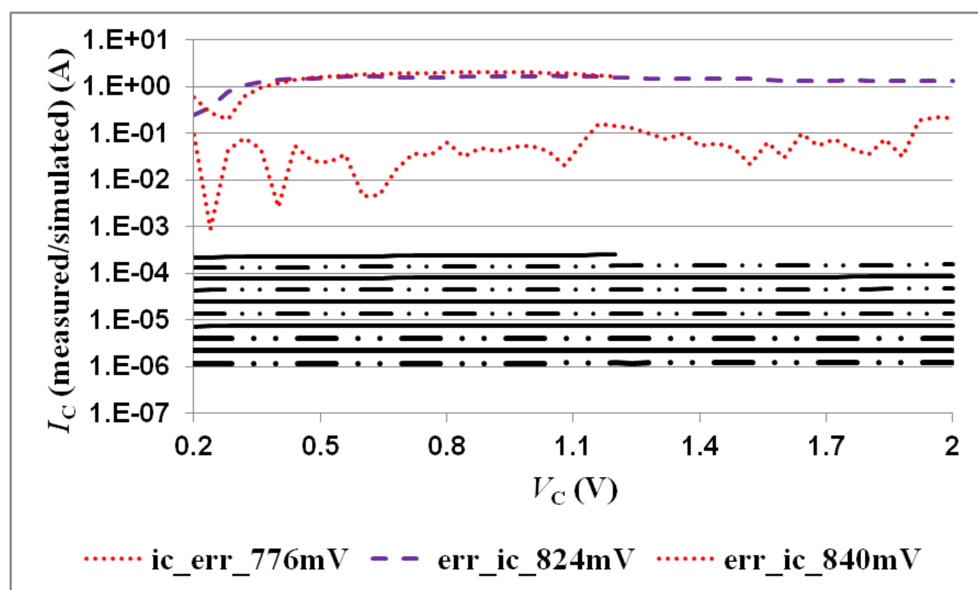

Figure A - 16: The plot of optimized output characteristics using the linear model for a 1 μm device. Here the black dashed-dot and black solid curves represents the I_C curves at V_{BE} = 560-840 mV in steps of 16 mV measured by sweeping V_C=0-2 V in steps of 40 mV.

A.3.3 Current gain, β

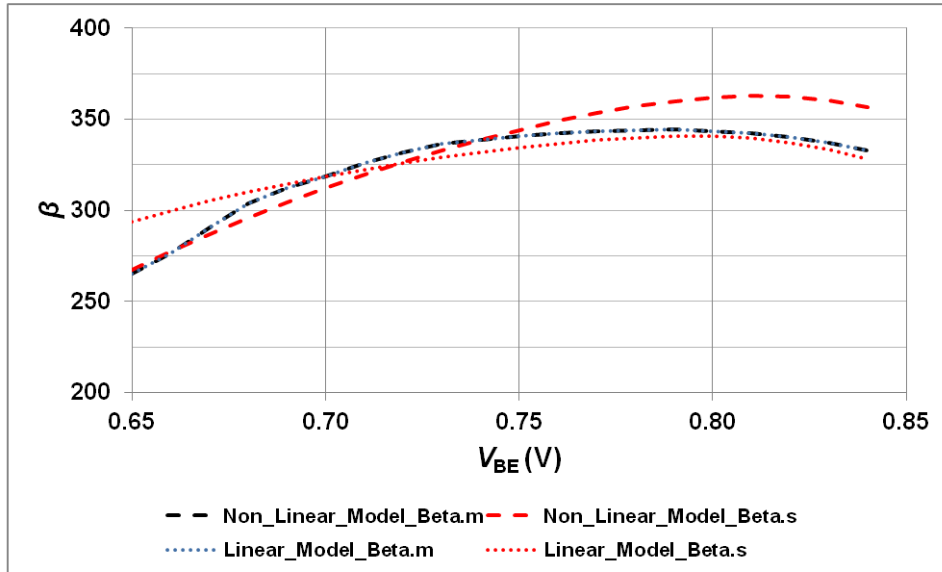

Figure A - 17: The plot of current gain, β, versus base-emitter voltage calculated using the non-linear and the linear thermal model for a 1 µm device.

A.3.4 Junction temperature estimation

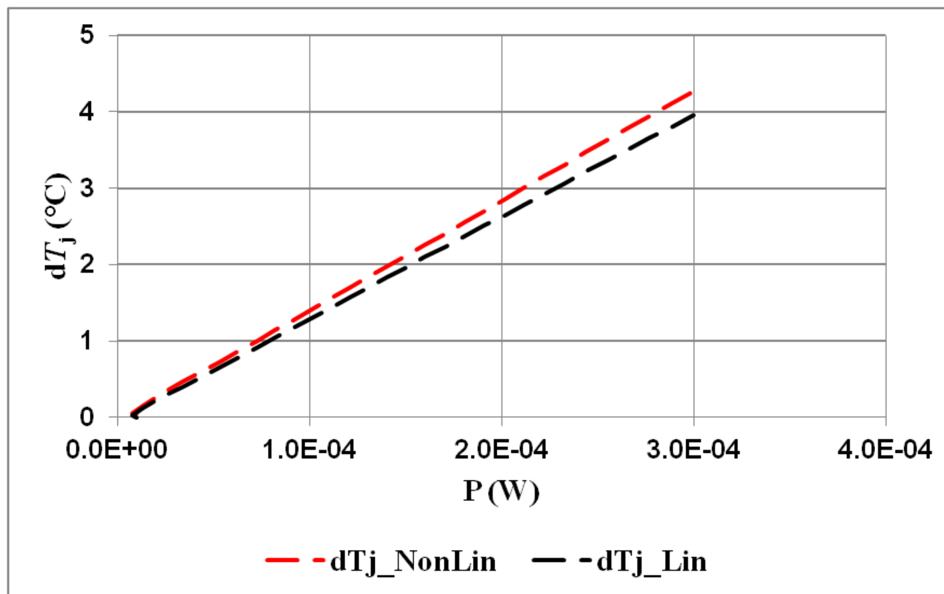

Figure A - 18: The plot of the junction temperature calculated using the non-linear and the linear thermal models for a 1 µm device.

A.4 The 5 μm device

A.4.1 Forward Gummel results

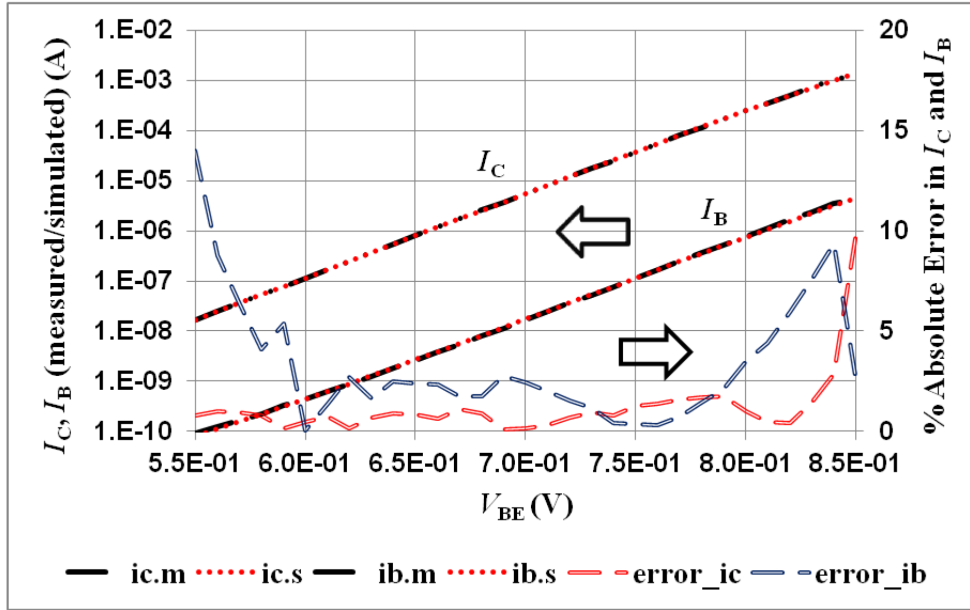

Figure A - 19: The optimized FG plot using the non-linear thermal model for a 5 μm device.

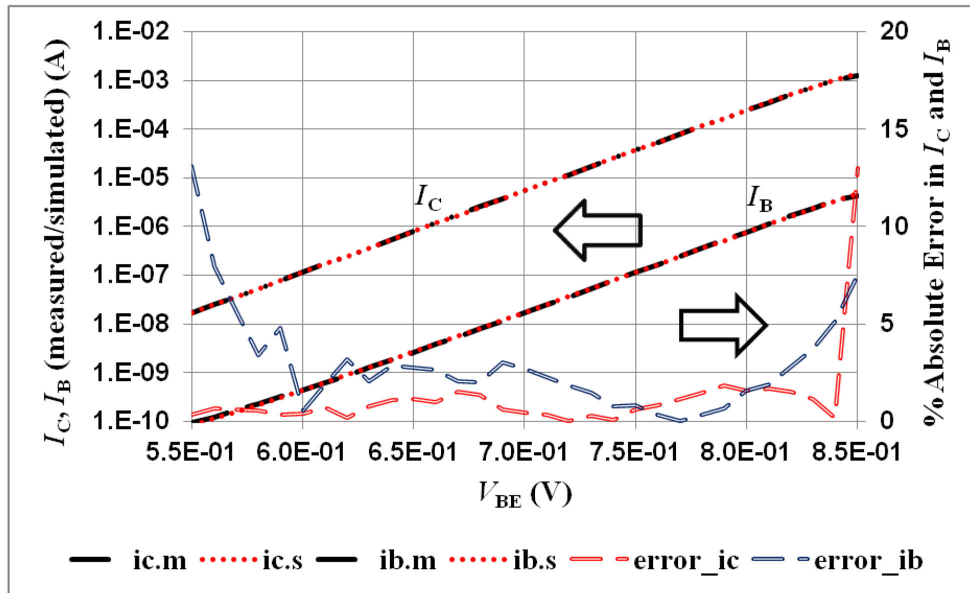

Figure A - 20: The optimized FG plot using the linear thermal model for a 5 μm device.

A.4.2 Base voltage controlled output characteristics results

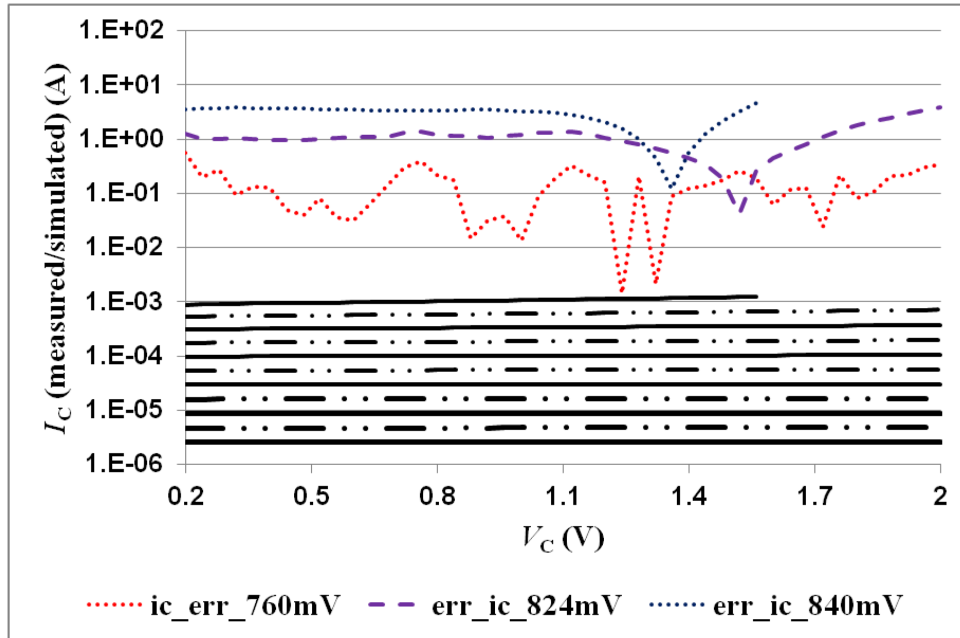

Figure A - 21: The plot of optimized output characteristics using the non-linear model for a 5 µm device. Here the black dashed-dot and black solid curves represents the I_C curves at V_{BE} = 560-840 mV in steps of 16 mV measured by sweeping V_C=0-2 V in steps of 40 mV.

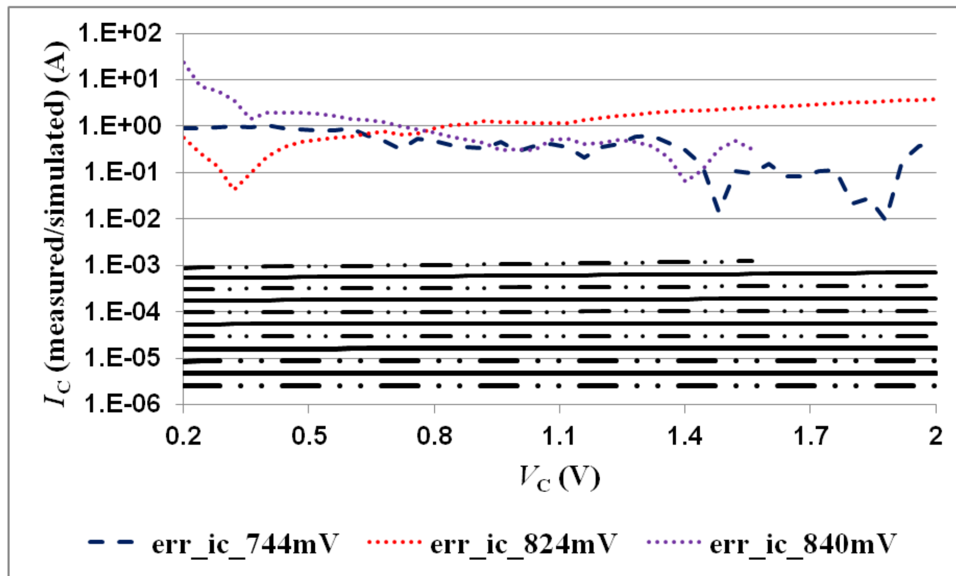

Figure A - 22: The plot of optimized output characteristics using the linear model for a 5 µm device. Here the black dashed-dot and black solid curves represents the I_C curves at V_{BE} = 560-840 mV in steps of 16 mV measured by sweeping V_C=0-2 V in steps of 40 mV.

A.4.3 Current gain, β

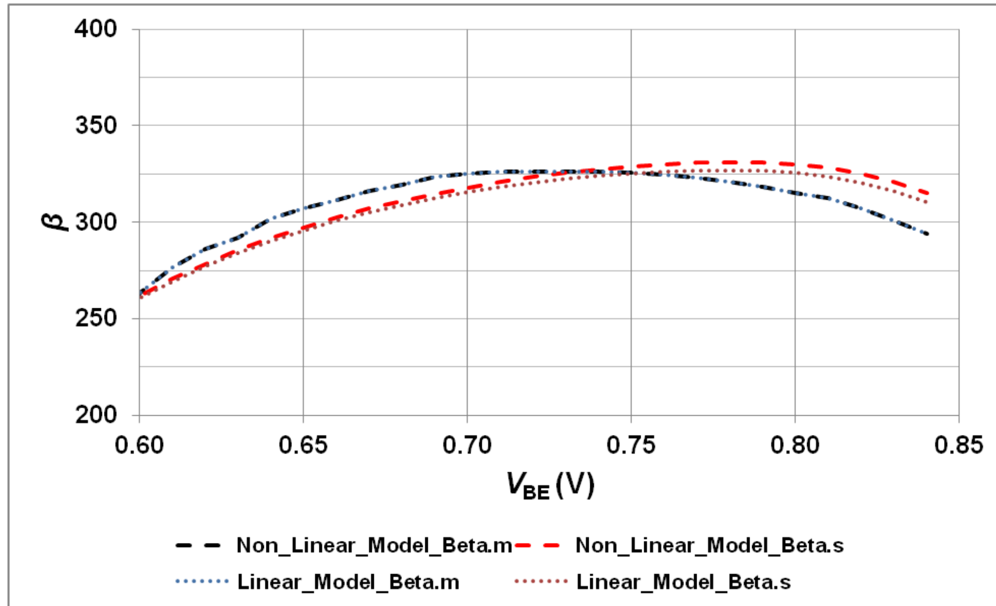

Figure A - 23: The plot of current gain, β, versus base-emitter voltage calculated using the non-linear and the linear thermal model for a 5 µm device.

A.4.4 Junction temperature estimation

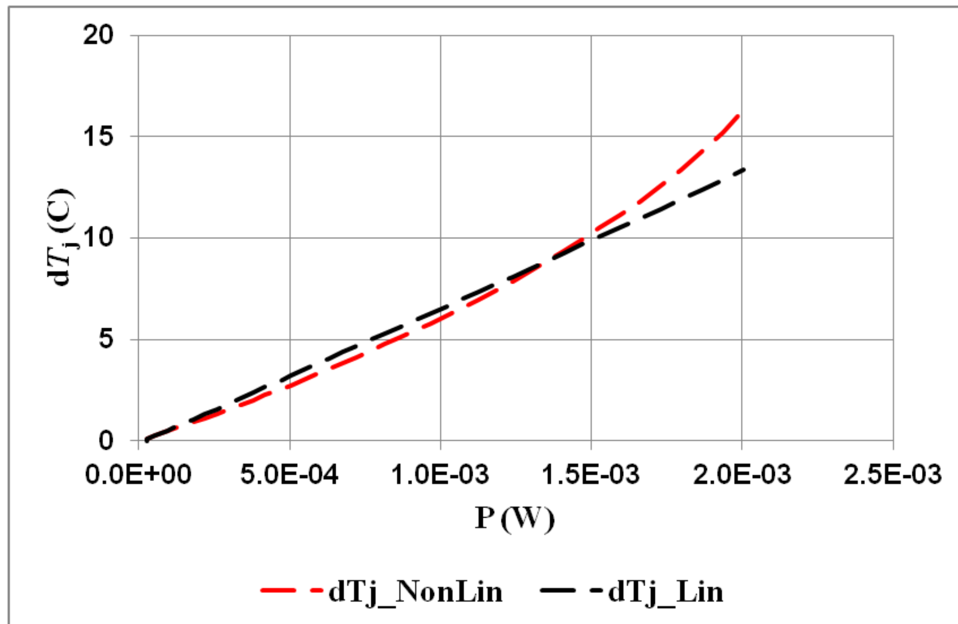

Figure A - 24: The plot of the junction temperature calculated using the non-linear and the linear thermal models for a 5 µm device.

A.5 The 10 μm device

A.5.1 Forward Gummel results

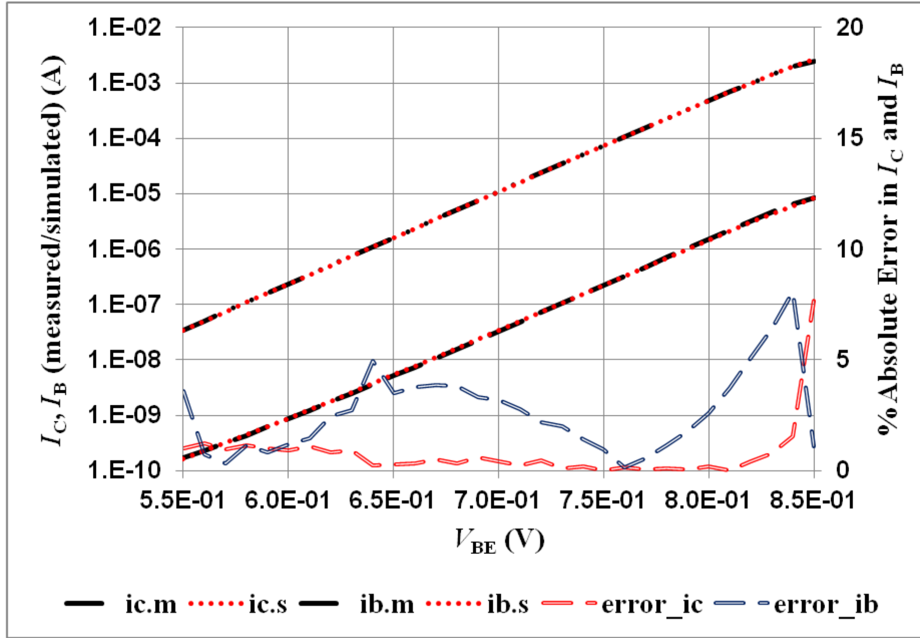

Figure A - 25: The optimized FG plot using the non-linear thermal model for a 10 μm device.

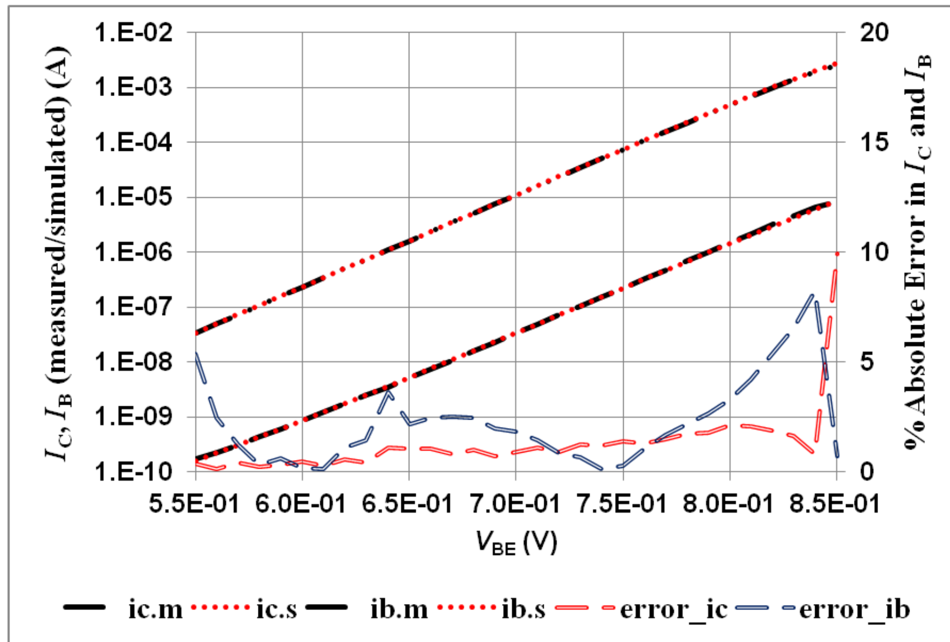

Figure A - 26: The optimized FG plot using the linear thermal model for a 10 μm device.

A.5.2 Base voltage controlled output characteristics results

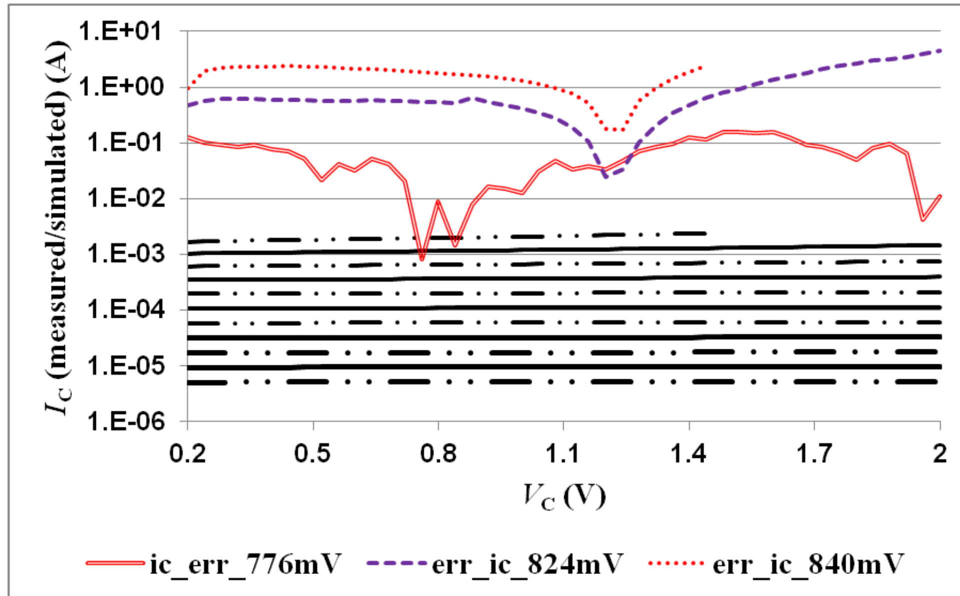

Figure A - 27: The plot of optimized output characteristics using the non-linear model for a 10 μm device. Here the black dashed-dot and black solid curves represents the I_C curves at V_{BE} = 560-840 mV in steps of 16 mV measured by sweeping V_C=0-2 V in steps of 40 mV.

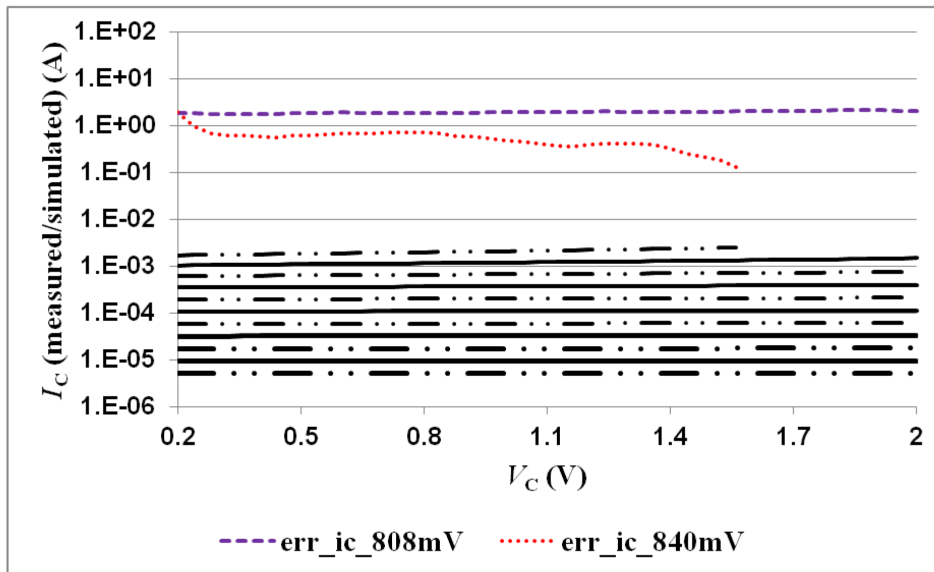

Figure A - 28: The plot of optimized output characteristics using the linear model for a 10 μm device. Here the black dashed-dot and black solid curves represents the I_C curves at V_{BE} = 560-840 mV in steps of 16 mV measured by sweeping V_C=0-2 V in steps of 40 mV.

A.5.3 Current gain, β

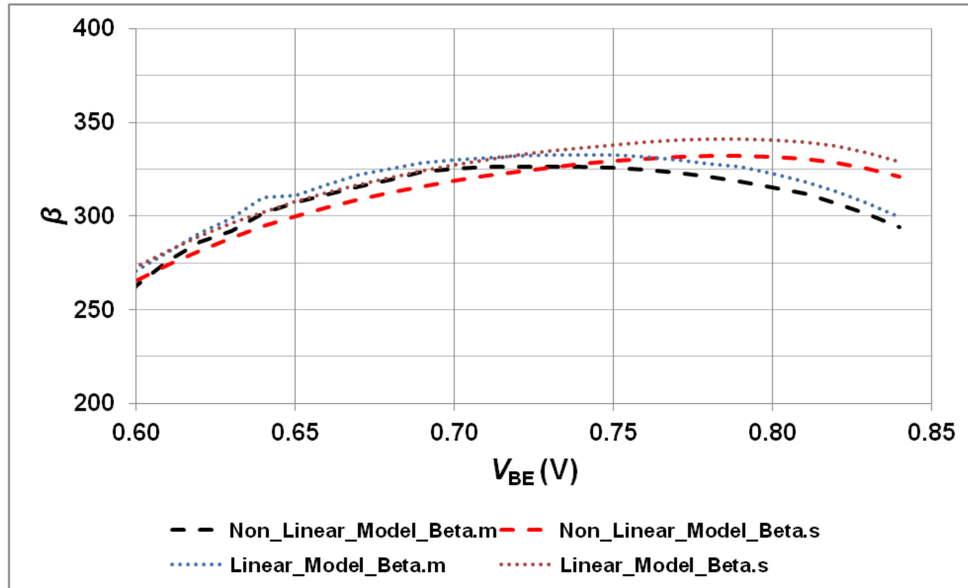

Figure A - 29: The plot of current gain, β, versus base-emitter voltage calculated using the non-linear and the linear thermal model for a 10 µm device.

A.5.4 Junction temperature estimation

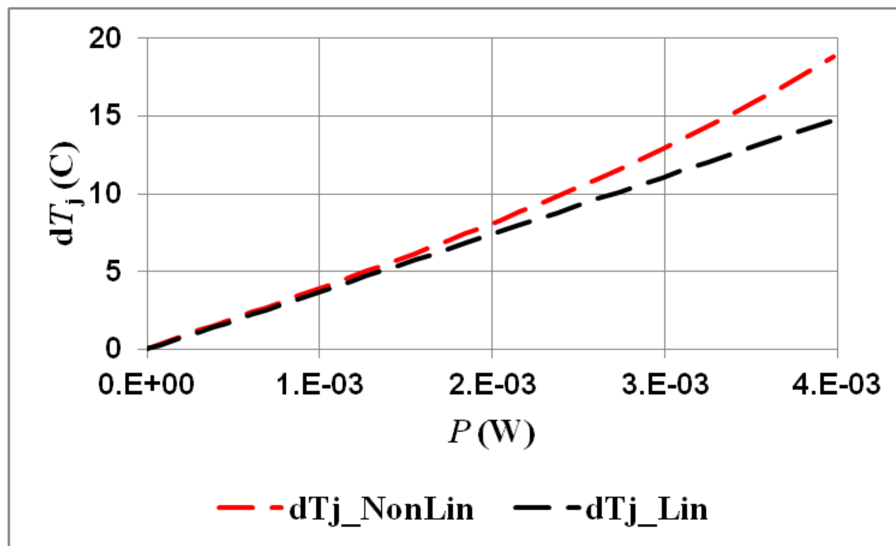

Figure A - 30: The plot of the junction temperature calculated using the non-linear and the linear thermal models for a 10 µm device.

APPENDIX B

DESIGN OF A TIMING CIRCUIT USING A PHASE LOCKED LOOP

B.1 Introduction

The European Organization for Nuclear Research also known as CERN (derived from the name "*Conseil Europeen pour la Recherche Nucleaire*") is a European research organization that operates the largest particle physics laboratory in the world. The main function of CERN laboratory is to provide the particle accelerators and other infrastructure needed for high-energy physics research. As a result, numerous experiments have been constructed at CERN as a result of international collaborations. A Toroidal Large hadron collider ApparatuS (ATLAS) is a particle physics experiment at CERN that is searching for new discoveries in the head-on collisions of protons at extraordinarily high energy. The ATLAS experiment will help people learn about the basic forces that have shaped our Universe since the beginning of time and what will determine its fate. Among the possible unknowns are extra dimensions of space, unification of fundamental forces, and the evidence for dark matter in the universe. Following the discovery of the Higgs boson, further data will allow in-depth investigation of the boson's properties.

The basic design of the timing system is adopted from the system designed at the SLAC laboratory. The differences between the two systems are: (a) The SLAC system has to be stabilized at 476 MHz whereas the ATLAS reference signal is at ~ 40 MHz provided by the TTCex system which is the clock signal. In the TTCex system, TTC is an abbreviation for Timing, Trigger and Control [71]. An up-conversion at the input end and a down-conversion at the output end is required. Also, the frequency multipliers and dividers that are available off-the-shelf provide integral multiples of the input signal. This necessitates different design requirements for the local oscillators and filters. (b) The point where the ATLAS reference signal is available is called the Interaction Point (IP) or point A in figure B-1 where the collision of the particles take place and the place where the particles after the collision are detected are at points B and C. The time interval between the successive collisions is 25 ns which is equivalent to 40 MHz in frequency domain. The distance between point A and point B is 280 m and similarly the distance between point A and point C is 280 m. Point B and point C is in the opposite directions with respect to

point A. The challenge here is that the clock signal at point B and point C has to be in synchronization. A constant offset between the two clocks is acceptable. This type of system requirement is not present at SLAC. (c) Lastly, if the system has to be designed at 40 MHz then a ferrite based circulator and isolator would be difficult to design. The size of these RF components is inversely proportional to the operating frequency. So at 40 MHz they would be very large. The distributed Phase Locked Loop (PLL) is designed to stabilize the TTCex clock signal. It is distributed in nature because all the circuit components needed to implement a PLL are not co-located at one place. A further detail of the circuit implementation is given in the following sections.

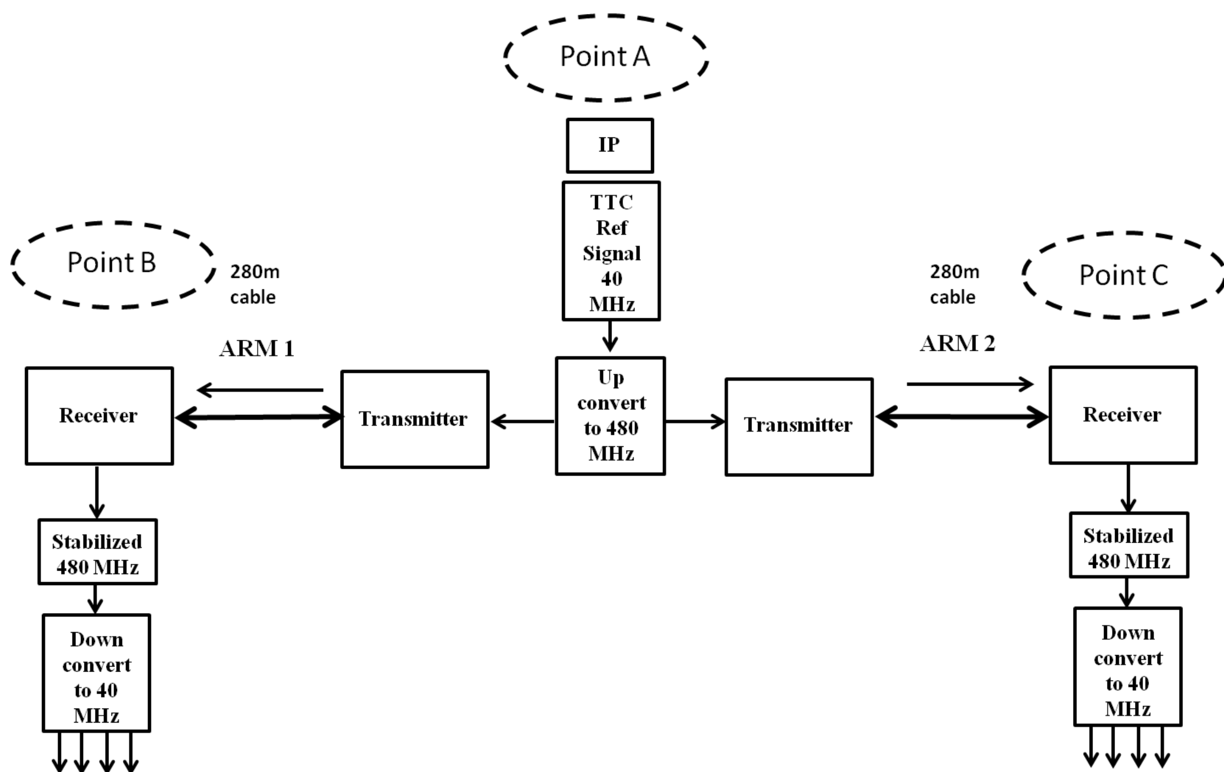

Figure B - 1: The schematic of the block diagram of the timing circuit designed to stabilize the reference signal of 40 MHz that will in turn be used as the event timing signal.

B.2 Introduction to Phase Locked Loop (PLL)

The major building blocks for a PLL are: (a) a phase detector, (b) a loop filter (generally a low-pass filter), (c) a Voltage Controlled Oscillator (VCO), (d) an amplifier (optional) and (e) a divider (if

frequency multiple is required). A block level diagram of a simple PLL circuit is shown in figure B-1. The input that needs to be stabilized is applied at the reference signal port of the phase detector as shown in figure B-2. The phase detector compares the reference signal with the free-running frequency of the oscillator and generates a voltage proportional to their phase differences. This voltage is then fed through a low-pass loop filter and into the VCO. The output frequency of the VCO is tuned by the input dc voltage. This results in a feedback loop, where the free-running frequency of the VCO will be tuned to match the phase and hence the frequency of the input reference signal. Since it takes several periods to lock on to a changed input reference, the output will not follow each small frequency shift. Therefore the output will become more stable than the reference signal. PLLs find use in a variety of different areas such as jitter cleaning (where a noisy reference signal is cleaned of jitter before entering the circuit), frequency synthesis (where one stable reference frequency source is used to create multiples of the input reference signal) and clock recovery (where data signal is sent without an explicit clock signal).

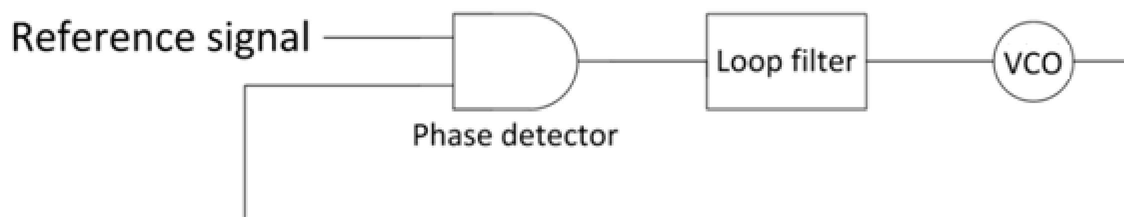

Figure B - 2: Schematic block diagram of a simple PLL circuit.

B.3 Design of a Timing Circuit using a PLL

The blocks named transmitter and receiver in figure B-1 are misnomers, since their actual circuit operation is not as it is in radio-frequency (RF) or microwave communication systems. The transmitter is named as such because the reference signal is available at this point and it is sent from this block to the rest of the circuit. The reference signal of 40 MHz is available at the Interaction Point (IP). This signal cannot be used directly as a timing signal because of the high jitter content. A PLL is designed to reduce the jitter in the reference signal to < 5 ps. The challenges that need to be accounted for in the design: (a) The reference signal is available at the interaction point from the Timing, Trigger and Control (TTC) system which is 280 m away from the electronics that needs the low jitter, stabilized clock signal. (b) The stabilized clock signal needs to be supplied to two ends, each of which are 280 m apart from the

interaction point as shown in figure B-1. Both of these stabilized timing signals need to be in synchronization. A constant offset between these stabilized signals is acceptable. (c) Also, the signal has to travel back and forth between the transmitter and the receiver blocks as shown below which requires a circulator whose size is inversely proportional to the frequency of operation. The design of a circulator operating at a frequency of 40 MHz is impractical. The solution to this problem is to up-convert the reference frequency from 40 MHz to a higher frequency. In this work the reference signal is up-converted by a factor of 12 to 480 MHz. The benefits of up-conversion are two-fold. Firstly, it will allow use of an available circulator and secondly, while down-conversion the jitter will be down-converted as well. The clock producing the TTCex standalone frequency is generating a 40.085 MHz clock at 20 °C. This clock is not sufficiently stable to be used directly as the timing signal for this experiment. Due to jitter the actual frequency ranges between ~ [40.0749 – 40.0823] MHz [71].

The design of the timing circuit is divided into four main blocks: (a) The reference signal up-conversion block, (b) the transmitter block, (c) the receiver block and (d) the signal down-conversion block. The down-conversion of the ~ 480 MHz signal by a factor of 12 yields a stabilized 40 MHz, square wave timing signal. The bill of materials (components summary) for the timing circuit is provided in Appendix C.

B.4 Up-Conversion Circuit Design

The up-converted frequency is chosen such that it is an integral multiple of the reference frequency. Here, the multiplication factor of 12 is used for up-conversion. The frequency multiplier circuit, SN65LVDS150, from Texas Instruments, Inc. has the ability to up-convert the input signal by a factor between 4 and 40 with the maximum output frequency of 400 MHz. The up-conversion is carried out in two steps: (a) The frequency multiplier circuit, SN65LVDS150, is used to up-convert the reference frequency of ~ 40 MHz to 240 MHz, and (b) a frequency doubler (×2), ZX-90-2-13+, from Mini-Circuits is used to up-convert the 240 MHz signal to the required 480 MHz. Currently a laboratory signal generator is used to provide the ~ 40 MHz TTCex reference signal.

A frequency multiplier with a multiplying factor of six and the frequency doubler are shown in figure B-3. The output of the frequency doubler as obtained in a spectrum analyzer is shown in figure B-4.

A total of 8 significant harmonics appear at the output port of the doubler. A band-pass filter with center frequency of 490 MHz is used to suppress these harmonics to a low power level (~ 20 dB down from the center frequency). A 490 MHz band-pass filter was used because it was the closest available off-the-shelf filter which matched the design criteria.

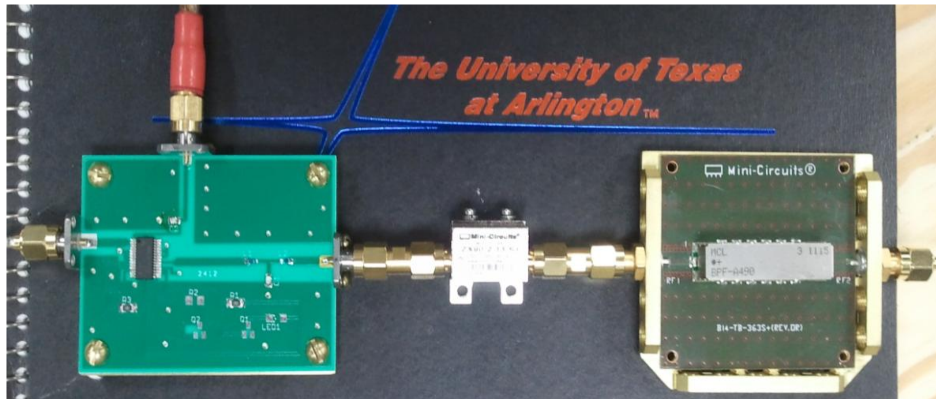

Figure B - 3: The up-conversion circuit showing a multiplier (×6), a frequency doubler (×2) and a band-pass filter.

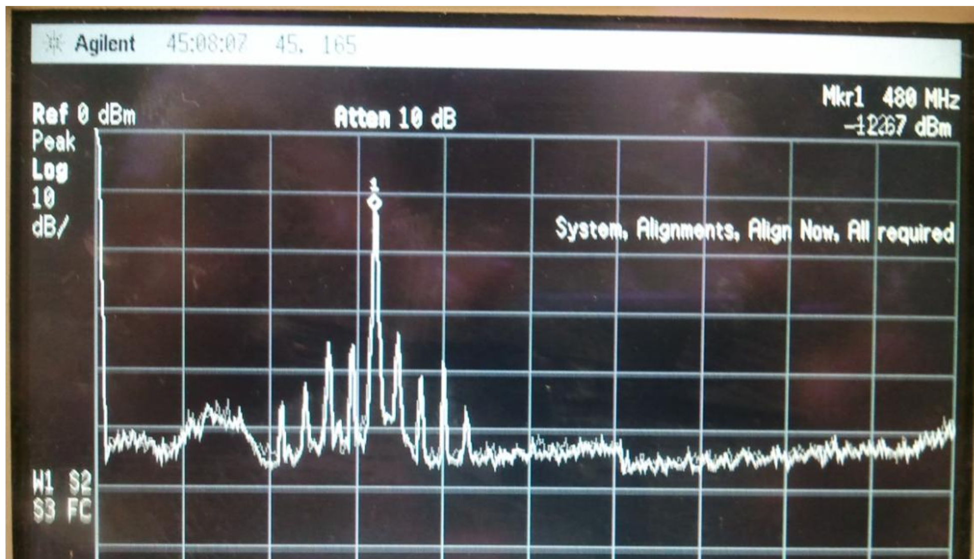

Figure B - 4: The output of the frequency doubler with the center frequency at 480 MHz and harmonics in a spectrum analyzer.

B.5 Transmitter (Tx) Circuit Design

The Transmitter (Tx) block circuit design is shown in figure B-5. It consists of RF circuit components such as: (a) a coaxial bias tee, (b) a circulator, (c) a combination of a low-pass and high-pass filter to obtain a band-pass characteristic, (d) a 2-way power splitter, (e) a RF amplifier, (f) a RF coupler, (g) a power detector, (h) a RF mixer, (i) a low pass filter and (j) a dc amplifier. The system reference block as denoted in figure B-5 consists of the up-conversion circuit components. The up-converted ~ 480 MHz signal is fed into the Local Oscillator (LO) port of the mixer as shown in figure B-5.

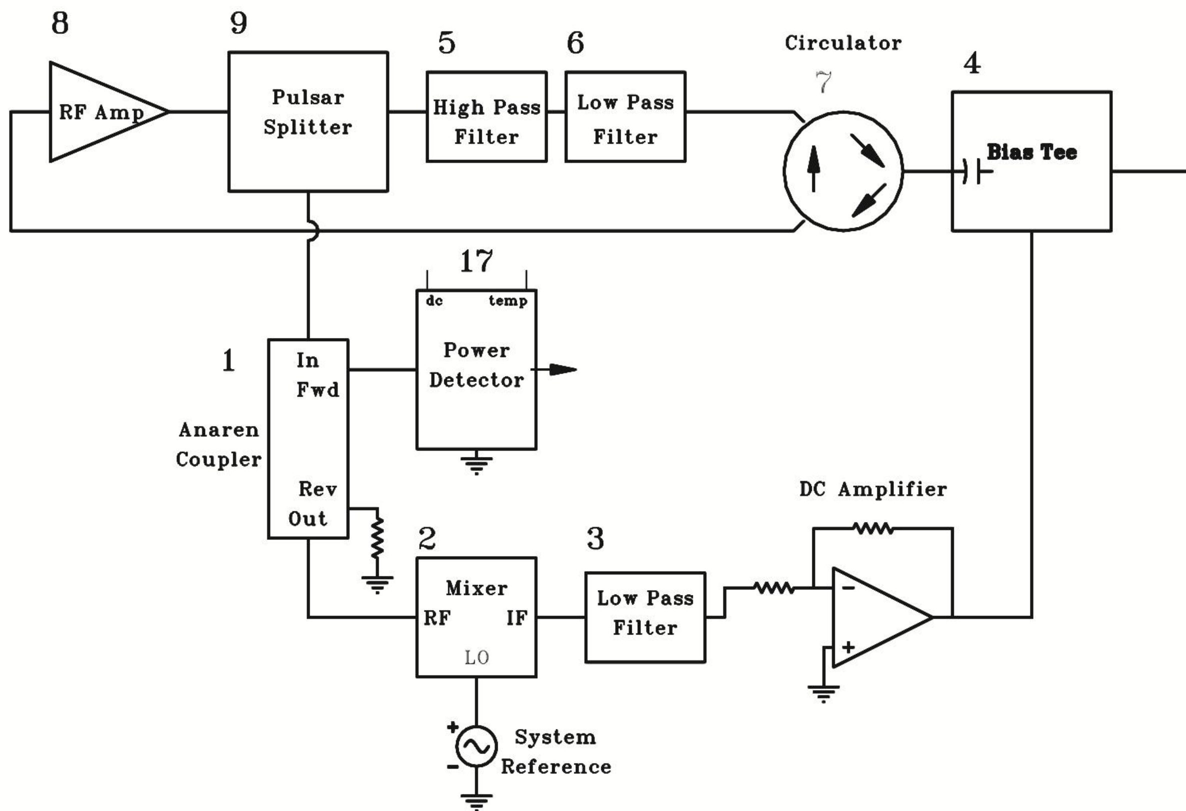

Figure B - 5: A schematic diagram of the transmitter block for the timing circuit.

B.6 Receiver (Rx) Block Design

The Receiver (Rx) block circuit design is shown in figure B-6. It consists of RF circuit components such as: (a) a dual directional coupler, (b) a coaxial bias tee, (c) an isolator, (d) an attenuator, (e) a Voltage Controlled Oscillator (VCO), (f) a Proportional Integral Derivative (PID) controller, (g) a phase shifter, (h) a 180° hybrid coupler, (i) a power detector, (j) a RF amplifier (optional) and (k) a delay line (optional). The output from the SUM port of the 180° hybrid coupler is fed into the divider circuit for down-conversion.

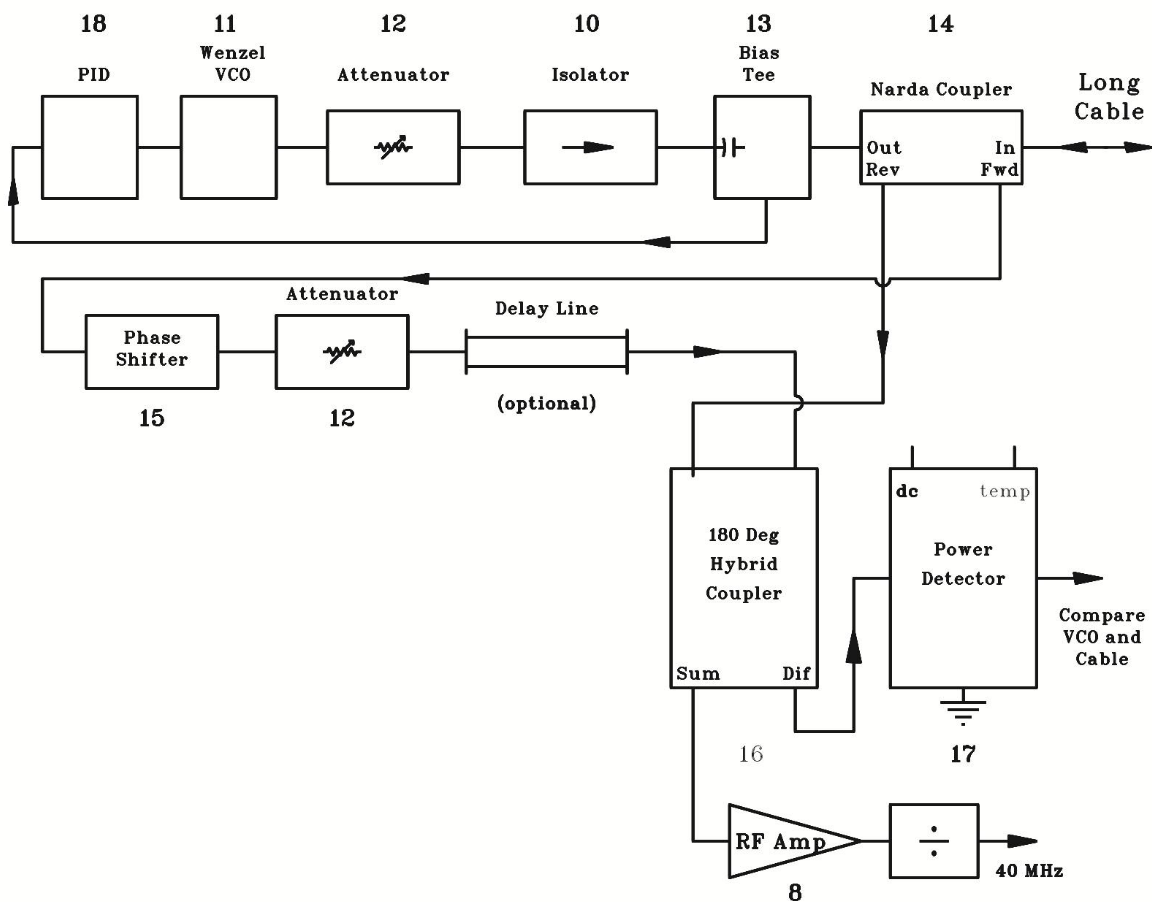

Figure B - 6: A schematic diagram of the receiver block for the timing circuit.

B.7 Down-Conversion Circuit Design

The down-conversion of the stabilized ~ 480 MHz signal is performed using the programmable divider from Hittite Microwave Corporation. The HMC705LP4(E) is a low noise GaAs HBT programmable divider in a 4x4 mm leadless surface mount package. The divider can be programmed to divide by any number from N = 1 to N = 17 up to 6.5 GHz. The functional diagram of the divider chip is shown in figure B-7. The minimum and maximum input frequencies to the divider are 0.1 GHz and 6.5 GHz respectively. The duty cycle of the output signal can be calculated using the relationship mentioned in table B-1. The division factor, N, can be selected by setting the S0, N0, N1, N2, DIV 1 and BYP pins on the chip. The truth table for selecting N = 12 is given in table B-2. These pins are visible in the functional diagram of the divider chip as shown in figure B-7.

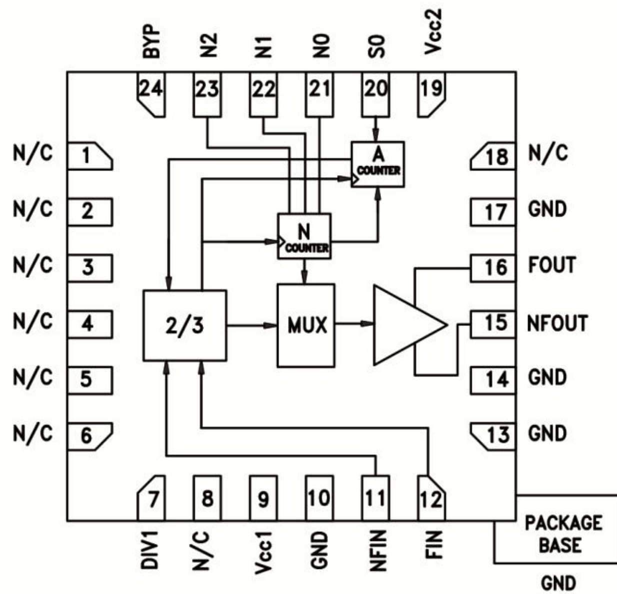

Figure B - 7: The functional diagram of the divider chip from Hittite Microwave Corporation [72].

Table B - 1: Relationship to calculate the duty cycle of the output signal for different division factor, N.

N	Output Duty Cycle (%)
1	Same as input signal
2	50
3 - 17	[1 – (2/N)] × 100

Table B - 2: Truth table to select division factor, N = 12.

Division Factor, N	S0	N0	N1	N2	DIV 1	BYP
12	0	1	0	1	0	0

An evaluation board with a pre-mounted divider chip was used for this work. The part number for this evaluation Printed Circuit Board (PCB) is 116993. The layout of the evaluation PCB is shown in figure B-8. A + 5 V power supply is needed to power up this circuit. The ~ 480 MHz stabilized sine wave is applied at the J3 (FIN) SMA input and an output signal at ~ 40 MHz is obtained at the J1 (FOUT) terminal. The output signal is a square wave with the duty cycle ~ 83 % (duty cycle is calculated using the relationship given in table B-1).

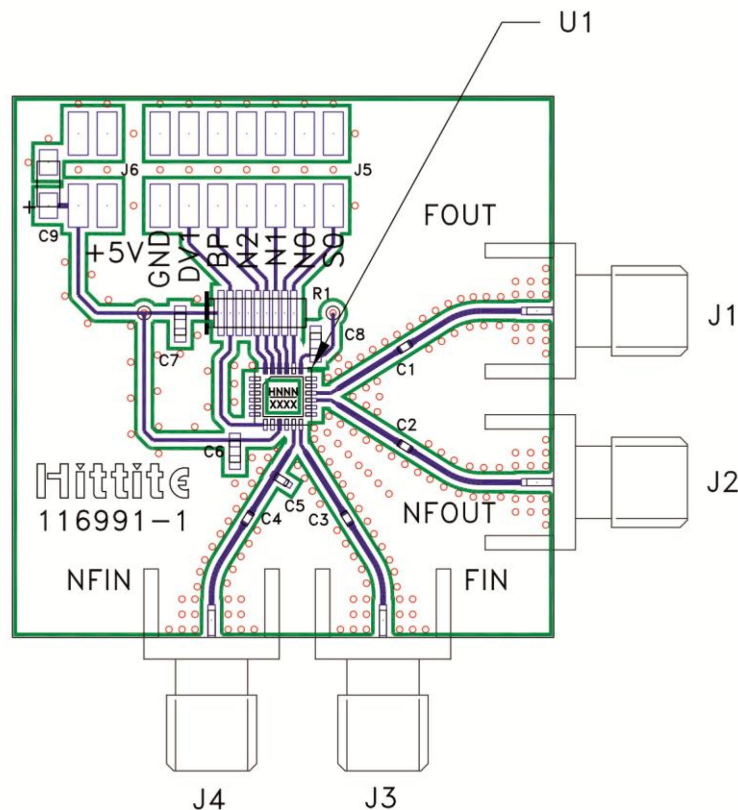

Figure B - 8: Layout of the divider evaluation PCB board from Hittite Microwave Corporation [72].

B.8 Circuit Operation

The voltage controlled oscillator (VCO) on the Rx side is initially free-running at ~ 480 MHz. This low-noise 480 MHz signal is sent to the Tx block through a 280 m long coaxial cable. This low-noise ~ 480 MHz signal is fed into the Radio Frequency (RF) port of the mixer and mixed with the up-converted ~ 480 MHz un-stabilized reference signal which is fed into the mixer at the Local Oscillator (LO) port as shown in figure B-5. The Intermediate Frequency (IF) generated by the RF mixer is filtered using a low-pass filter such that only the dc or low frequency signal is fed into the amplifier. The dc signal corresponding to this IF signal is then transmitted to the Rx to modulate the VCO output frequency. The error in the output frequency of the VCO is reduced by this repetitive process to get locked to the reference frequency. The incoming signal from the Tx block into the Rx block is divided into two parts by a dual directional coupler. The signal from the directional coupler and the VCO are internally compared at the 180° hybrid coupler which generates a SUM (addition) and DIFF (difference) signals. The null (zero) output at the DIFF port signifies the frequency of the free-running VCO is locked with the reference ~ 480 MHz signal. The phase shifter and/or delay line output can be adjusted to get a null output at the DIFF port. This stabilized, low-jitter 480 MHz signal is then down-converted using a divider with a division ratio (÷12) and a 40 MHz stabilized, low-jitter timing signal is achieved.

B.9 Circuit Components

B.9.1 Bias Tee

A bias tee is a three port network in which the input port carries both a dc and an ac signal, one output port carries the dc part and the other port carries the RF. This sets the dc bias point of some electronic components without disturbing the high frequency components. The port with no blocking capacitor is used to set the bias, the port with the blocking capacitor passes the RF signals but blocks the dc biasing levels, and the combined port connects to the device which sees both the dc bias and the RF signal. The equivalent circuit of the bias tee is shown in figure B-9. For wide-band bias tees, the inductor must be large to block the lower frequencies. A large inductor will have a stray capacitance which results in a self-resonant frequency. At high frequencies, the stray capacitance presents a low impedance shunt path for the signal, and the bias tee becomes ineffective. Practical wide-band bias tees must use circuit

topologies that avoid the shunt path. Instead of one large inductor a series of small inductors are used. In addition, there will be additional capacitors and resistors to prevent resonance.

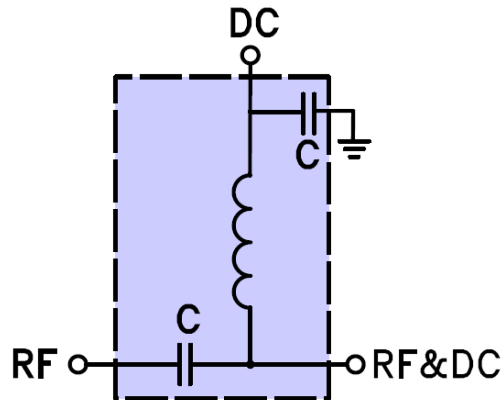

Figure B - 9: Equivalent circuit of the bias tee.

B.9.2 Band-Pass Filter

A Band-Pass Filter (BPF) is a device that passes frequencies within a certain range and reject (attenuates) frequencies outside that range. A BPF can be characterized by its Q factor. The Q factor is the inverse of the fractional bandwidth. A high Q factor will have a narrow bandwidth. The bandwidth calculation for a typical BPF is explained in figure B-10. Here, frequency is plotted on the x axis and the amplitude of the signal on the y axis. The center frequency of the filter is shown by f_0. The frequencies f_L and f_H represent the lower bound and the upper bound of the pass-band respectively and *B* stands for the bandwidth of the filter. A combination of a high-pass and a low-pass filter can be used to obtain a band-pass behavior. An ideal BPF would have a flat pass-band and would reject all the frequencies outside the pass-band. Additionally, the transition out of the pass-band would be very steep. In practice, no BPF is ideal. The pass-band consists of ripples and the filter does not reject all the frequencies outside the pass-band. Also the transition from the pass-band to the stop-band is not abrupt and is denoted by the filter roll-off factor usually expressed in dB of attenuation. Generally, the design of a filter seeks to make the roll-off as steep as possible. This can be achieved by increasing the number of stages of the BPF which adds to the design complexity. Hence, there is a trade-off between the roll-off factor and design complexity.

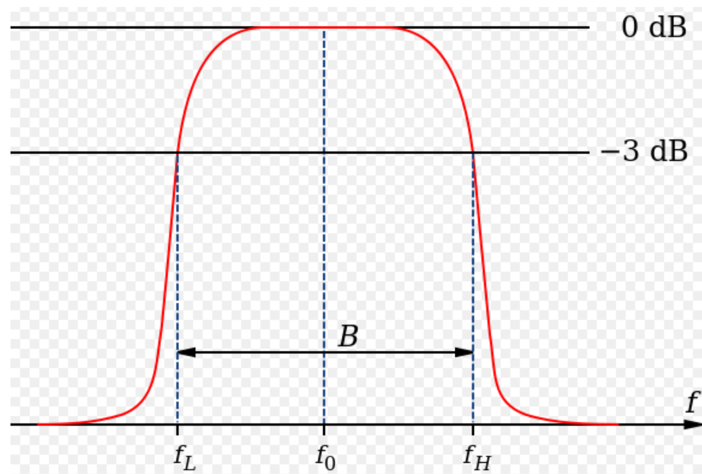

Figure B - 10: Schematic diagram depicting the bandwidth of a band-pass filter.

B.9.3 Circulator

A circulator is a ferrite device with usually three ports. Ferrite is a class of anisotropic materials that have different electrical properties (such as permeability constant) depending on which direction a signal propagates through them. In terms of S-parameters, the S_{21} is much different from S_{12} for such devices. Two types of circulators that can be manufactured are: (a) Counter Clock Wise (CCW) and (b) Clock Wise (CW). For a CW circulator the energy from port 1 predominantly exits port 2, the energy into port 2 exits port 3 and the energy in port 3 exits port 1. No energy transfer in the counter clock wise direction takes place i.e.: from port 1 to port 3. The symbols used for the two types of circulators are shown in figure B-11. The physical size of the circulator is inversely proportional to the frequency of operation. Hence, at lower frequencies (i.e.: f < 100 MHz) the circulator is bulky. Moreover, to make a ferrite circulator that can operate at dc is not feasible.

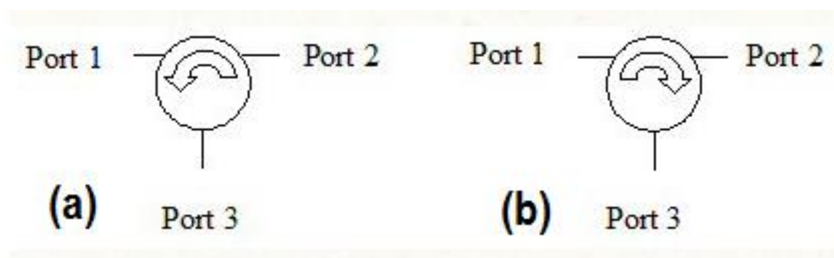

Figure B - 11: (a) Circuit symbol to represent a counter clock wise circulator. (b) Circuit symbol to represent a clock wise circulator.

B.9.4 Low-Pass Filter

A low-pass filter (LPF) is a filter that passes signals with a frequency lower than a certain cut-off frequency and attenuates signals with frequencies higher than the cut-off frequency. The amount of attenuation for each frequency depends on the filter design. The LPF is characterized by its cut-off frequency and rate of frequency roll-off. At the cut-off frequency, the filter attenuates the input power by half or 3 dB. The order of the filter determines the amount of additional attenuation for frequencies higher than the cutoff frequency.

B.9.5 RF Amplifier

Amplifiers are important building blocks for RF systems. Their typical applications includes front-end, low-noise RF amplifiers for receivers, IF amplifiers for receivers, audio, video, and other Low Frequency (LF) amplifiers, transmitter - RF amplifier chains, transmitter - output power amplifiers, buffer amplifiers for oscillators and gain stages to overcome insertion loss due to passive components such as filters, mixers and multipliers. The critical parameters for designing or describing an RF amplifier are listed below:

- Frequency range
- Amplitude transfer function (gain as a function of frequency)
- Phase transfer function (helpful for stability analysis)
- Input and output matching
- Noise Figure (mainly for preamplifiers)
- Maximum output power (critical at 1 dB compression for power stages)
- IP3 or third-order intercept point (to analyze distortion behavior)
- Power efficiency
- Gain control range or bandwidth
- Cooling (for power applications)

The front-end, RF Low-Noise Amplifiers (LNA) is a critical part of many receiver systems. Some High Frequency (HF) receivers also use LNAs. Very High Frequency (VHF) and higher frequency

receivers nearly always use front-end LNAs. At these frequencies, the receiver noise from a mixer can be much greater than the noise that is received by the antenna. Having an LNA preceding a mixer thus can greatly improve the noise and sensitivity performance of the receiver system. LNAs are constructed with either Bipolar Junction Transistors (BJTs) or Field-Effect Transistors (FETs). For each of these technologies, class A amplifiers are used. Class A amplifiers are so biased so that it is in conduction during all parts of the RF cycle. They usually consist of single-transistor gain stages. Class B amplifiers are designed such that it has a conduction angle of 180 degrees. For a class AB amplifier the conduction angle is slightly greater than 180 degrees and for class C amplifier it is much less than 180 degrees. Class B and class AB amplifiers usually are two transistor or two tube “push-pull” type power amplifiers. Push-pull amplifiers are made up of two transistors where one operates for one half cycle of the RF signal and the other transistor operates for the other half of the cycle. They frequently use transformers to combine the outputs. Class C amplifiers may be constructed by either single transistor or push-pull type power amplifiers. In most cases, class C amplifiers use resonant circuits to convert the short duration pulses into the sine waves. Class A amplifiers have a maximum possible efficiency of 50% and since they are normally used for small-signal amplification, efficiency is not very important. Whereas class B amplifiers have a maximum efficiency of 78%, with class C as high as 90% and class AB maximum efficiency slightly greater than class B amplifiers. Class B and class AB amplifiers are normally used for large-signal amplification and hence high efficiency is needed. Class C amplifiers are non-linear amplifiers that require tuned circuits on the output. Those tuned circuits are also called tank circuits [73].

Silicon BJT RF amplifiers are used at lower RF frequencies because of higher gain capability and non-linear operation. The maximum frequency is limited to ~ 8 to 10 GHz, depending on the application [73]. FET RF amplifiers made from gallium-arsenide (GaAs) typically are used at microwave and higher frequencies because of their higher frequency capability and lower noise figure. Higher operating frequencies are achieved in these devices because of the higher mobility of the carriers in GaAs compared to silicon. FETs can use either GaAs or silicon whereas BJTs use only silicon. In each case, it is necessary to bias the transistor to the desired bias voltage and current using dc bias networks. It is also necessary to provide input and output impedance matching circuits. Some matching circuits are designed to provide maximum power output whereas some are designed for flat gain over a large bandwidth. In

LNAs the matching may be to obtain the minimum noise figure. Impedance matching is done at Very High Frequency (VHF) and lower frequencies using lumped components and constant LC circuits. At Ultra High Frequency (UHF) and microwave frequencies, very small LC circuits are used in the form of monolithic and ceramic packages or distributed element designs.

In the ideal scenario, a small signal RF amplifier is linear and produces the amplified version of the input signal at the output terminal. But in practice, there will be some distortion and harmonic generation due to the non-linear characteristics of the transistor. Band-pass filters are used to suppress the signal outside the desired signal band. Due to the non-linear nature of the transfer function the amplifier output will have harmonics. The amplifier will act as a mixer if multiple frequency signals are present at the input, generating difference and sum frequencies. The mixing products form nonlinearities also called second- and third-order inter-modulation distortion. Other forms of distortion generated by a transistor amplifier are cross-modulation distortion, and composite triple-beat distortion. For example, for a three frequency signal at the input, the amplifier may generate the second-order distortion components which include 3 dc components, 6 sum and difference components and 3 second-harmonic components. The third-order distortion components include 3 third-harmonic components, 12 inter-modulation components, 4 triple-beat components, 3 self-compression components and 6 cross-compression or cross-expansion components. The third order spurious products are the most troublesome, because they may fall within the band-pass region of even moderate bandwidth amplifiers.

One of the problems that are encountered with high-gain RF amplifiers is that they are prone to oscillate. Amplifiers are always designed such that the individual stages and the overall system have stability factors greater than 1.0, and greater than 1.5 for unconditional stability. It is a common practice to place the amplifiers in metal containers or shields so that, the individual stages are shielded from each other. Such shielding can greatly reduce the unwanted coupling between the stages. Also, the use of Eccosorb or other Radar Absorbing Material (RAM) attached to covers (~20-30 mils thick) usually eliminates possible oscillations and reduces feedback. Another way to improve stability is by providing a negative feedback signal that is equal in amplitude and opposite in phase to the positive feedback signal that is causing oscillations [73].

B.9.6 DC Amplifier

Circuits that provide useful gain at zero frequency are called direct-coupled or direct-current amplifiers. Operational amplifier is an example of a dc amplifier. To obtain high gain more than one stage can be implemented. In the design and operation of dc amplifiers particular attention is paid to reducing the slow changes (drift) of the output voltage or current that occur in the absence of an input signal. Such changes are caused by a number of factors such as: aging of amplifier components, fluctuations of ambient temperature, and voltage variations of the power supply.

B.9.7 Coupler

Couplers or directional couplers are RF passive devices used to couple a specific proportion of the RF power traveling in one transmission line to another. It is a four port device. The ports are named as: (a) input or incident port, (b) transmitted or output port, (c) coupled or forward coupled port and (d) isolated or reverse coupled port. The major RF directional coupler specifications are: (a) coupling loss, (b) insertion loss, (c) directivity and (d) isolation. A schematic diagram of a typical RF directional coupler is shown in figure B-12.

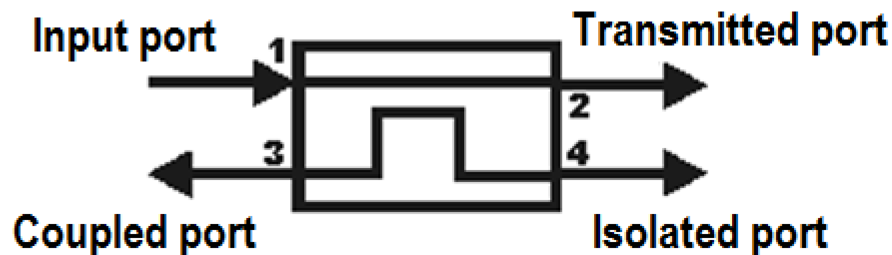

Figure B - 12: Schematic diagram of an RF directional coupler.

B.9.8 Attenuator

An ideal attenuator is a passive device that reduces the power of a signal without distorting its waveform or changing the characteristic impedance. It is effectively the opposite of an amplifier, though the working of both these components is different. They are generally passive devices made from simple voltage divider networks. Switching between different resistances forms adjustable stepped attenuators and continuously variable attenuators using potentiometers. RF attenuators are typically made from

coaxial lines with precision connectors as ports. The important characteristics of RF attenuators are: (a) accuracy of impedance, (b) low SWR, (c) flat frequency response and (d) repeatability.

A.9.9 Oscillator

The quality of an oscillator has an important effect on spectral purity. Several types of oscillators are manufactured. Fixed frequency oscillators rely on a non-tunable resonator, which often is a quartz crystal. However, since the practical upper limit of crystals only extend up to about ~ 300 MHz, PLLs and frequency multipliers are needed to achieve the higher UHF and microwave frequencies. Dielectric Resonator Oscillators (DROs) are less stable but are extensively used as microwave sources, and with a suitable multiplier they can be used in millimeter wave systems as well. In a DRO, the frequency of operation is defined by the mechanical size and shape of a small dielectric part. Tunable oscillators have a resonator that can be mechanically adjusted. Varactor-based transistor oscillators are practical up to some gigahertz (GHz) and above that yttrium iron garnet (YIG) devices can be used [74]. Important parameters that helps define an RF oscillator are described below:

- Center frequency
- Tuning range or tuning bandwidth (applicable to tunable oscillators)
- Tuning speed (if applicable)
- Output power
- Frequency stability (phase noise in frequency domain and jitter in time domain)
- Frequency pulling and pushing
- Frequency setting resolution (if applicable)
- Temperature characteristics
- Spectral purity (e.g.: spurious and harmonics)

Tunable oscillators are often called Voltage Controlled Oscillators (VCOs) because the input voltage at a specific port of the VCO determines the output frequency of the VCO. The oscillator tuning mechanism comes at the cost of its stability. The signal quality of an RF oscillator is defined by its stability, the phase noise and by the unwanted harmonics across the frequency spectrum of interest.

Apart from the actual operating frequency, odd and even harmonics (integer multiples) of the initial frequency are obtained. They can be filtered out, but for a wide band system it is tiresome. Also non-harmonic spurious signal may appear depending on the selection of components and the circuit design. Close to the carrier (center frequency of the oscillator), amplitude noise and the phase noise defined as decibels with reference to the carrier (dBc or dBc/Hz) are more critical. Here, both the actual value (for example: -70 dBc) and the distance from the center frequency (nominal frequency) (for example: 1 kHz) matter. Obviously, the lower the noise and the closer it is measured to the carrier, the better the result.

Time domain stability of the VCO is often analyzed over time spans ranging from 1 second to 1 year. Typically the fundamental frequency of the oscillator is defined above 10 seconds. Very short time frequency fluctuations are mainly caused by the PLL (if applicable). Aging is an unavoidable feature of the crystal oscillators. This is taken into account because crystals' operating principle is of mechanical nature. Sometimes reasonable stability is achieved out of a crystal oscillator after 1 year of continuous operation without any power interruptions. Drift values around 10 Parts Per Million (ppm) are common. Very high quality designs are Temperature Compensated Crystal Oscillators (TCXOs), Digitally Compensated Crystal Oscillators (DCXOs), or Oven Controlled Crystal Oscillators (OCXOs). Good TCXOs show frequency changes of 0.1 ppm, and OCXOs go down to 1 Part Per Billion (ppb). Even high quality oscillators are vulnerable to poor system level design. The supply voltages for RF oscillators must be regulated and free from transients. A PLL is sometimes incorporated within a VCO circuit making it somewhat dependent on the supply voltage [74]. The output frequency of the VCO is described by the relation given in (B.1). The locking time by the PLL can be calculated using (B.3).

$$f_{\text{out}} = f_{\text{o}} + (K_{\text{VCO}} \times v_{\text{tune}}) \tag{B.1}$$

$$f_{\text{out}} - f_{\text{o}} = K_{\text{VCO}} \times v_{\text{tune}} \tag{B.2}$$

$$\Delta t = \frac{1}{f_{\text{out}} - f_{\text{o}}} = \frac{1}{K_{\text{VCO}} \times v_{\text{tune}}} \tag{B.3}$$

A Multiplied Crystal Oscillator (MXO) with a free running frequency of 480.946008 MHz is used in the present work. It was custom manufactured by Wenzel Associates, Inc. The frequency calculation that

was used to determine the free running frequency of the VCO is presented in table B-3. The objective of these calculations is to keep the frequencies given in rows (3) and (8) to be as close as possible. The electrical tuning range of the VCO as determined from measurements is ~ 500 Hz with a negative slope. The graph of tuning range versus the tuning voltage is shown in figure B-13.

Table B - 3: Frequency calculation to determine the center frequency of the VCO

	Name	Value	Unit
1	TTCex highest frequency, f_H	40,082,300	Hz
2	TTCex lowest frequency, f_L	40,074,900	Hz
3	TTCex average frequency, f_{avg}	$(f_H+f_L)/2$ = 40,078,600	Hz
4	f_{avg} → upconverted	$f_{avg} \times 12$ = 480,943,200	Hz
5	Maximum frequency of Wenzel VCO, f_{VCO_max}	480,946,008	Hz
6	Tuning range of Wenzel VCO	~ 500	Hz
7	Minimum frequency of Wenzel VCO (after tuning), f_{VCO_min}	$(f_{VCO_max}) - 500$ = 480,945,508	Hz
8	$(f_{VCO_min}) \div 12$	480945408 ÷ 12 = 40,078,792	Hz

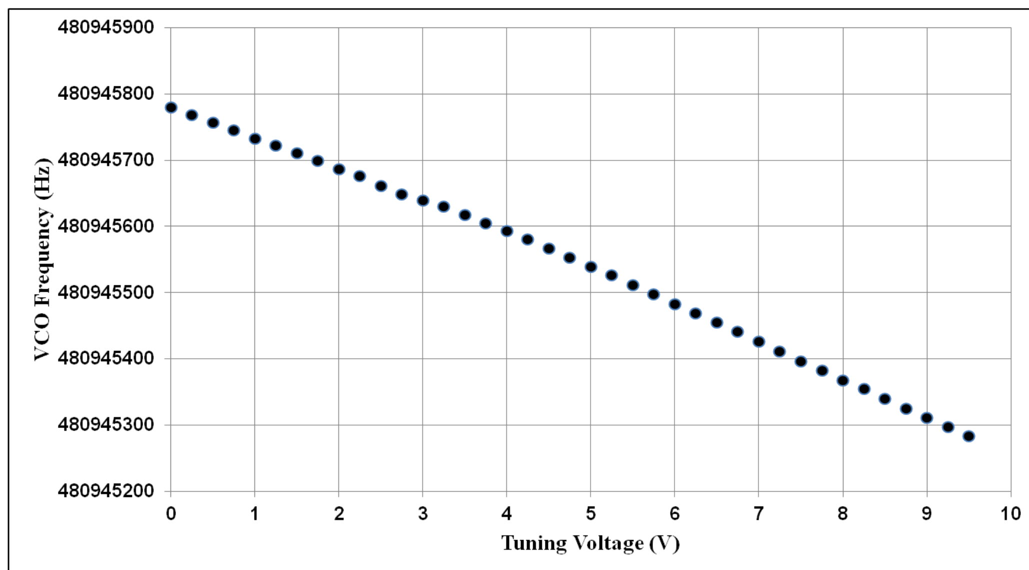

Figure B - 13: A plot of VCO frequency versus the tuning voltage.

B.9.10 180° Hybrid Coupler

The 180° hybrid coupler is a lossless, matched and reciprocal 4 port device. The power into a given port with all other ports matched is equally divided between two of the three output ports. However, the relative phase between the outputs is dependent on which port is the input. For example, if the input is applied to port 1 or port 3, the two signals will be in phase (no difference in their relative phase). However, if the input is applied to port 2 or port 4, the output signals will be 180° out of phase. An interesting application of this coupler is when two input signals are applied into the device at port 2 and port 3 (with port 1 and port 4 terminated in matched loads) then the output of the port 1 is proportional to the sum of the two inputs. Similarly, output at the port 4 is proportional to the difference between the two input ports.

B.9.11 PID Controller

A Proportional-Integral-Derivative (PID) controller is a control loop feedback mechanism used to monitor the changes in the system. A PID controller continuously calculates an error value as the difference between a desired setpoint and a measured process variable. The controller attempts to minimize the error over time by adjustment of a control variable (can be a P, I or D operation). Some instances may require using only one or two terms to provide the appropriate system control. This is achieved by setting the other parameters to zero. A PID controller is called a PI, PD, P or I controller in the absence of the respective control actions. Derivative of a signal tends to be noisy whereas integration of a signal reduces noise. The controlled process input can be unstable if the PID controller parameters are chosen incorrectly. Instability is caused by excess gain, in the presence of significant lag.

B.9.12 Mixer

RF mixers are used in systems to perform coordinated frequency changes. Additionally, a suitable mixer can be used as a phase detector or as a demodulator. Internal circuit topologies include single-ended, balanced (two-), and double balanced (four-) diode circuits. Critical performance figures used for mixer design and its selection are: (a) frequency of operation, (b) conversion and insertion losses, (c) port matching, and (d) isolation between various ports. Often times the ports do not have the same characteristics.

One of the first adverse characteristics of mixers is the IF spectrum, which tends to contain significant combination of mutual sums and differences as predicted by the common mixer equation as shown in equation (B.4). Hence, suitable filtering at the IF port needs to be performed to select the signal of interest. Sometimes, the purity of the LO signal and the RF signal at the RF input port needs to be taken into account. Using a normal BPF in the mixer ports involves the risk of mismatch because BPFs typically show very poor matching in their stop bands. Multiple reflections may cause out-of-spec conversion loss variations and yield to degraded intermodulation performance.

$$f_{\text{out}} = f_{\text{in}1} \pm f_{in2} \tag{B.4}$$

B.10 Test Equipments

B.10.1 Digital Signal Oscilloscope (DSO)

An Agilent 54855A Infiniium DSO with frequency range of 6 GHz is used to measure the jitter in the signal. The sampling rate of the DSO is 20 GSa/s on all four channels simultaneously. The trigger jitter of the scope is 1 ps RMS. Figure B-14 shows the picture of the DSO.

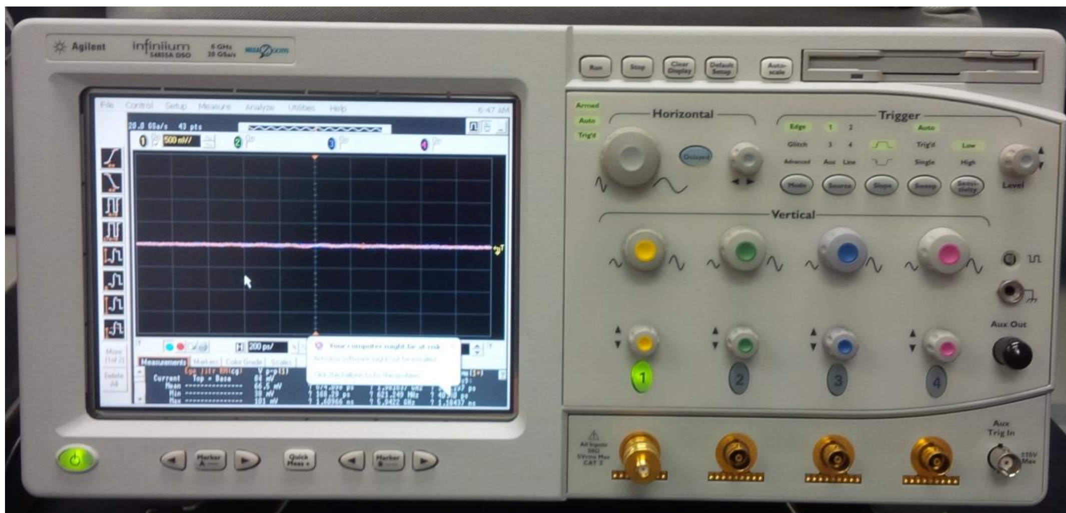

Figure B - 14: Agilent 54855A Infiniium DSO.

B.10.2 Spectrum analyzer

An Agilent E4411B ESA-L spectrum analyzer with a frequency range of 9 kHz to 1.5 GHz is used to analyze signals in the frequency domain. Basically, a spectrum analyzer is a tunable radio that shows

the magnitude (amplitude) of radio signals at different frequencies. It displays amplitude versus frequency while an oscilloscope displays amplitude versus time. Besides, center frequency it is useful to analyze power, distortion, harmonics, bandwidth, phase noise, and other spectral components of the signal that are not easily detectable on an oscilloscope. The input impedance of the spectrum analyzer is generally 50 Ω or 75 Ω and it can be made to high impedance by using an active FET probe without loading down the circuit being measured. The E4411B spectrum analyzer has an input impedance of 50 Ω. The picture of an Agilent E4411B ESA-L spectrum analyzer is shown in figure B-15.

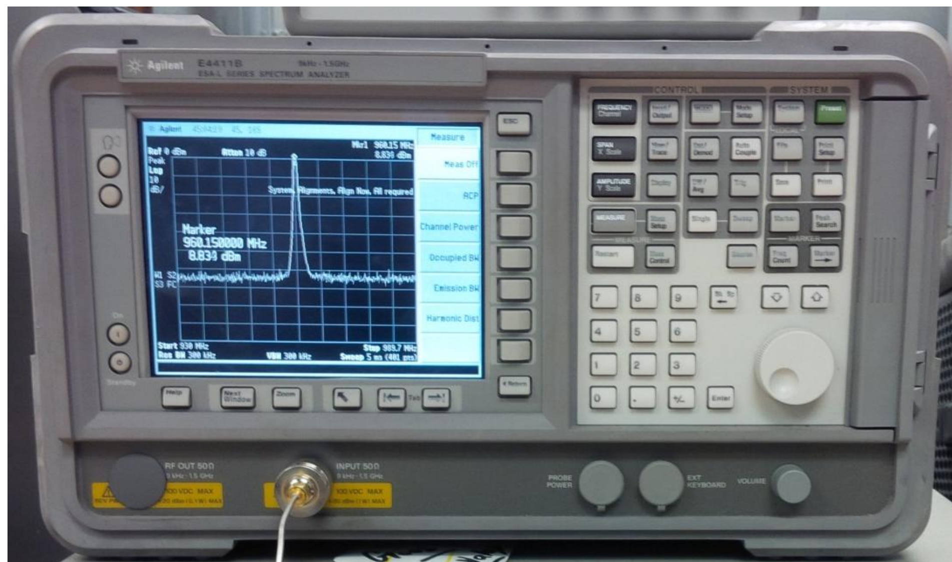

Figure B - 15: Agilent E4411B ESA-L spectrum analyzer with frequency range of 9 kHz to 1.5 GHz.

B.10.3 Signal generator

A Hewlett Packard (HP) 8657B signal generator with a frequency range of 0.1-2060 MHz is used to generate the reference signal that will eventually be replaced by TTCex signal. The 8657B signal generator provides the spectral purity and modulation versatility needed for testing the ATLAS PLL. A frequency resolution of 1 Hz is obtainable from this instrument. The picture of a HP 8657B signal generator is shown in figure B-16.

Figure B - 16: Hewlett-Packard 8657B signal generator.

B.10.4 Frequency counter

The Hewlett-Packard 5342A microwave frequency counter used to measure frequency in this work as shown in figure B-17. Two input ports are available: input port 1 can measure frequency from 500 MHz to 18 GHz while input port 2 can measure frequency from 10 Hz to 520 MHz. For measurements using port 1, the input impedance of 50 Ω needs to be selected from the front panel. If input port 2 is used then the impedance of the input port can be toggled between 50 Ω and 1 MΩ. More detailed information about the instrument can be found in the HP 5342A datasheet.

Figure B - 17: Hewlett-Packard 5342A microwave frequency counter.

B.10.5 DC power supply

Multiple DC power supplies were used to bias different parts of the circuit. The power supply models that were used in this work are the: (a) Agilent E3631A, triple output DC power supply, (b) Agilent E3620A, dual output DC power supply and (c). DC power supply requirement for various components of the timing circuit including both the arms (i.e.: arm A and arm B) is summarized in table B-4.

Table B - 4: Summary of the DC power requirement for various circuit components of the timing circuit.

	Component	**Total Quantity**	**Bias Voltage (V) Each**	**Bias Current (mA) Each**
1	Amplifier	3	+ 15	110
2	VCO - Wenzel	2	+ 12	500 @ start-up 270 @ stable operation
3	DC amplifier	2	TBD	TBD
4	Power detector	2	+ 5	
5	Divider – Hittite	2	+ 5	180
6	PID controller	2	+15, - 15, + 5	
7	Multiplier - TI	1	+ 3.3	59

B.11 Results

B.11.1 Spectral purity of the signal generator

The signal generator is used to provide the TTCex reference signal in this setup. The jitter in the signal at different frequencies is measured using a DSO and is given in table B-5. A screenshot of the jitter measurement in a DSO is shown in figure B-18. The Root Mean Square (RMS) jitter and the mean Peak-to-Peak (Pk-Pk) jitter is measured for various frequencies at different power levels. It is apparent from the table B-5 that the mean RMS jitter and the mean Pk-Pk jitter for lower frequencies are greater

compared to the corresponding jitter at higher frequencies. The reason for this behavior is that by increasing the frequency of the signal, the slope per unit time of the signal decreases and this results in a low jitter.

Table B - 5: A summary of the measured jitter in the signal generated by the signal generator at various frequencies.

	Frequency (MHz)	**Signal Power (dBm)**	**Mean RMS Jitter (ps)**	**Mean Pk-Pk Jitter (ps)**
1	40	4	111.67	667.86
2	40	7	113.17	689.75
3	40	10	134.50	807.09
4	40.0786	4	122.66	690.47
5	40.0786	7	108.59	654.67
6	40.0786	10	130.72	780.55
7	40.0786	12	116.76	696.29
8	480	4	9.82	58.94
9	480	7	12.88	76.09
10	480	10	11.65	69.71
11	960	4	5.45	31.66
12	960	7	7.02	43.26
13	960	10	5.57	34.17

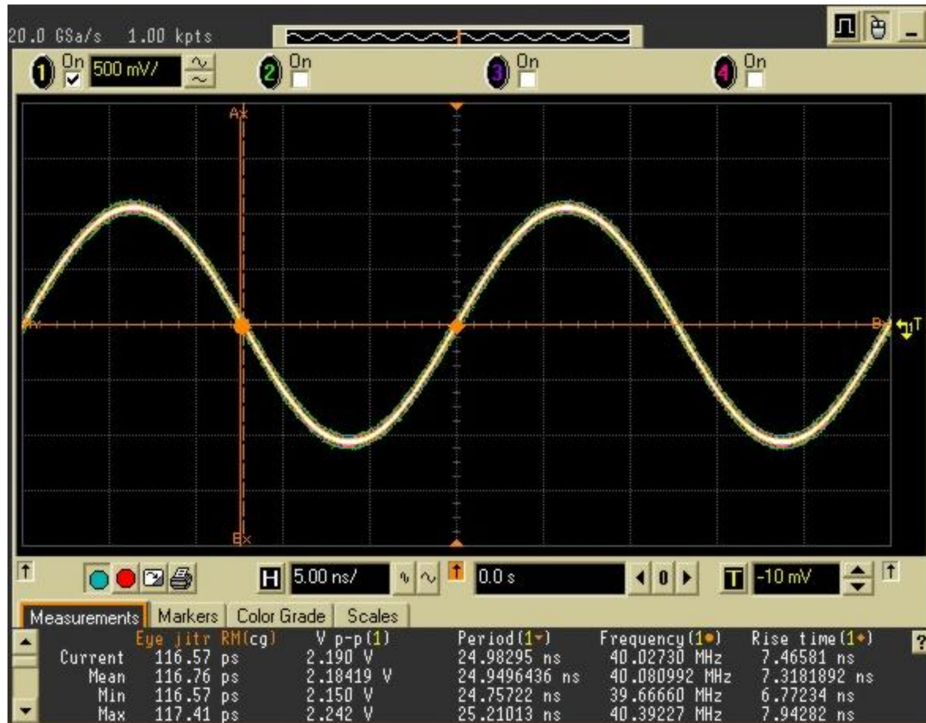

Figure B - 18: Screenshot of signal generator output signal at 40.0786 MHz at 12 dBm power as measured in a DSO.

B.11.2 Up-conversion block output

The TTCex reference signal ranges between 40.0749 – 40.0823 MHz reference. The average between the highest and the lowest frequencies of the TTCex is 40.0786 MHz. Hence, the signal generator frequency is set at 40.0786 MHz frequency which will be up-converted by a multiplying factor of 12 to 480.9432 MHz. The block diagrams of the setup used to perform the two step up-conversion is shown in figure B-19 and B-20. The output signal of frequency ~ 480 MHz from the frequency doubler contains harmonics which distorts the signal is shown in figure B-21. These harmonics are filtered out using a band-pass filter with f_C = 490 MHz and the output of the BPF is shown in B-23. The jitter measurements were performed on the output signal after each step and are summarized in table B-6.

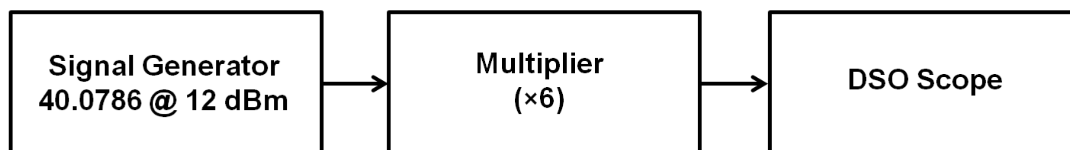

Figure B - 19: Block diagram of the setup used to measure jitter in the up-converted signal using the multiplier (×6) circuit.

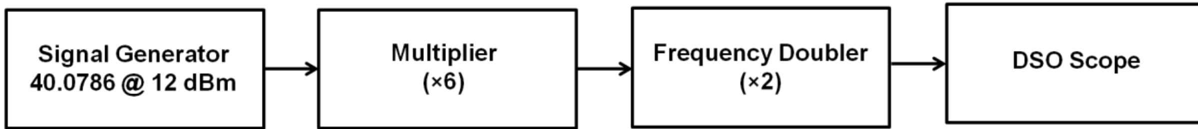

Figure B - 20: Block diagram of the setup used to measure jitter in the up-converted signal using the multiplier (×6) and frequency doubler (×2) circuit.

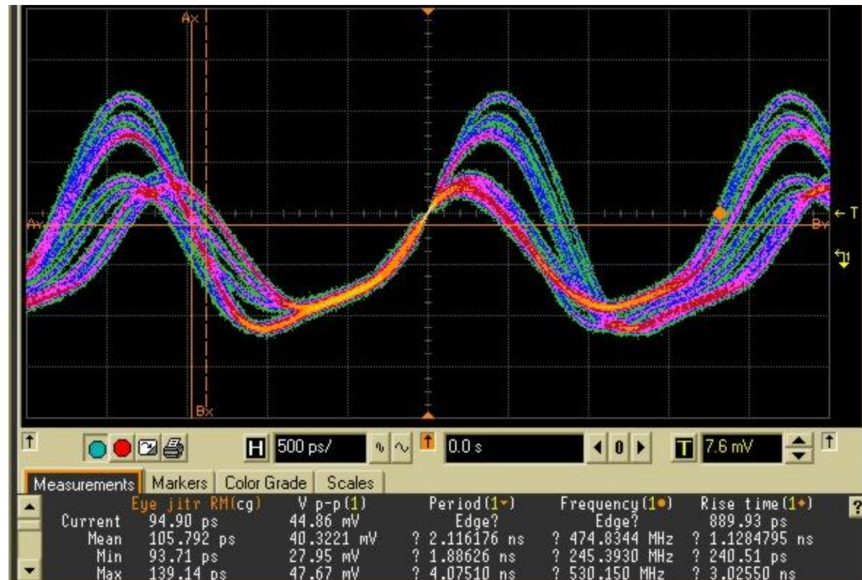

Figure B - 21: Picture of the up-converted output signal from the frequency doubler as measured in a DSO.

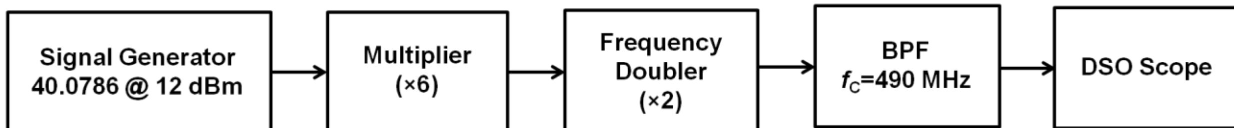

Figure B - 22: Block diagram of the setup used to measure jitter in the up-converted signal using the multiplier (×6) and frequency doubler (×2) circuit with a BPF to suppress the harmonics.

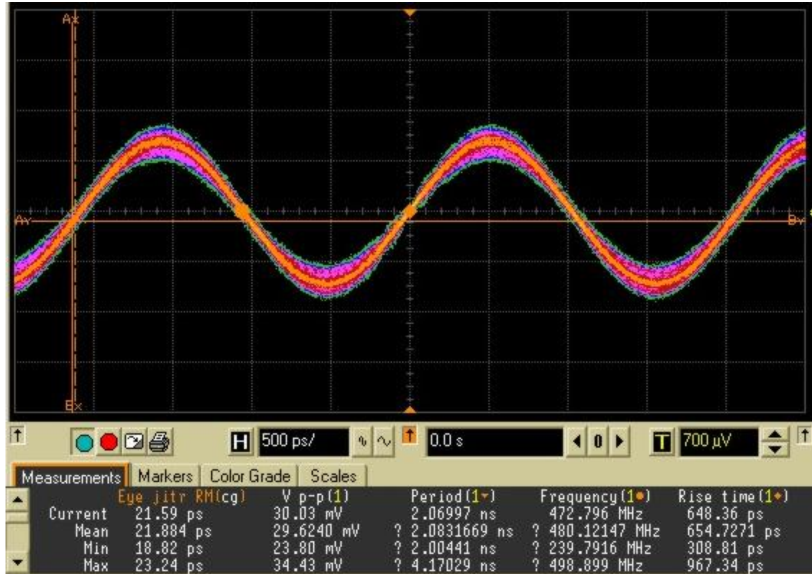

Figure B - 23: Picture of the output signal of the BPF after filtering out the harmonics caused due to up-conversion process.

Table B - 6: Summary of the jitter in the output signal due to the up-conversion procedure.

	Circuit Component Output	**Frequency (MHz)**	**Mean RMS jitter (ps)**	**Mean Pk-Pk jitter (ps)**	**Distortion due to harmonics**
1	Signal Generator	40.0786	116.76	696.29	No
2	Multiplier (×6)	~ 240	45.68	282.41	No
3	Multiplier (×6) + Frequency doubler (×2)	~ 480	105.79	344.53	Yes
4	Multiplier (×6) + Frequency doubler (×2) + BPF	~ 480	21.88	131.87	No

The frequencies that are present in the output signal of the BPF is shown in table B-7. It is apparent from the table that harmonics are spaced 40 MHz apart from the up-converted center frequency of 480 MHz. A BPF with narrow bandwidth needs to be designed in order to eliminate these harmonics. The harmonics in the BPF output are spaced at ± 40 MHz from the center frequency of 480 MHz as measured in a spectrum analyzer is shown in figure B-24.

Table B - 7: Summary of harmonics in the output frequency of the BPF of the up-conversion block.

Frequency sorted with respect to power	**Peak frequency**

1	480.9 MHz
2	521.2 MHz
3	560.9 MHz
4	440.6 MHz
5	601.2 MHz

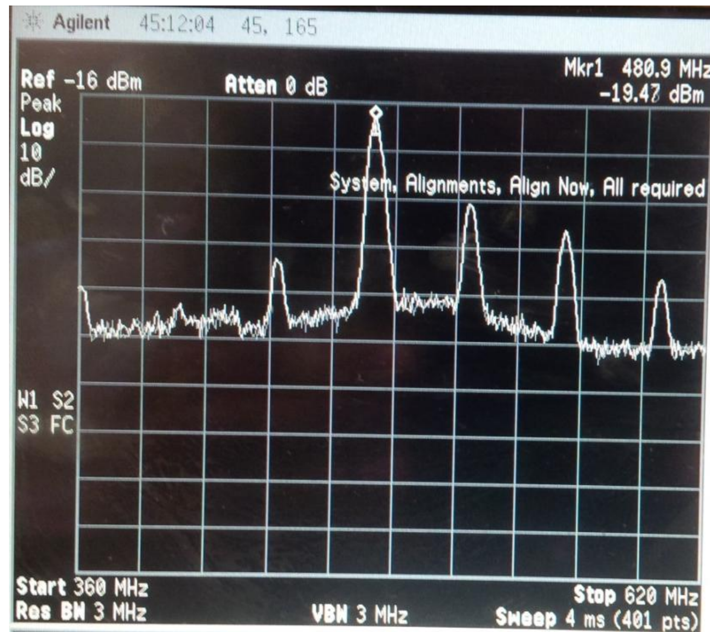

Figure B - 24: Output of the BPF of the up-conversion block showing the harmonics spaced at ± 40 MHz from the center frequency in a spectrum analyzer.

B.11.3 PLL output

The up-converted ~ 480 MHz signal is fed into the Local Oscillator (LO) port of the mixer located on the TX side of the PLL. The free-running frequency of the VCO is fed into the RF port of this mixer. The Intermediate Frequency (IF) generated by the mixer is proportional to the difference in the frequencies fed into the RF and LO port. This IF frequency is filtered using a Low-Pass Filter (LPF) and sent to the Rx side via a bias tee network to tune the frequency of the VCO. The ~ 480 MHz signal is sent back and forth between the Tx and Rx to achieve the lock. Once the free-running VCO frequency is locked to the reference frequency the phase noise (hence jitter) of the reference signal is reduced. The output signal of the PLL as captured from the sum port of the 180° hybrid coupler is shown in figure B-25.

The mean RMS jitter and the mean Pk-Pk jitter in the PLL output signal are 13.07 ps and 78.37 ps respectively.

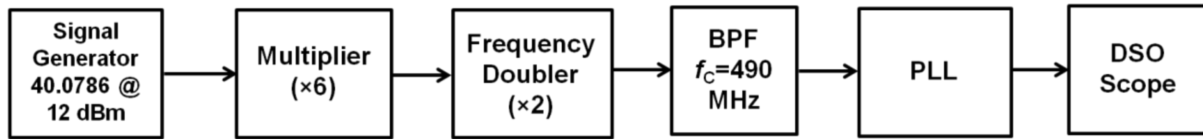

Figure B - 25: Block diagram of the setup used to measure jitter in the output signal of the PLL.

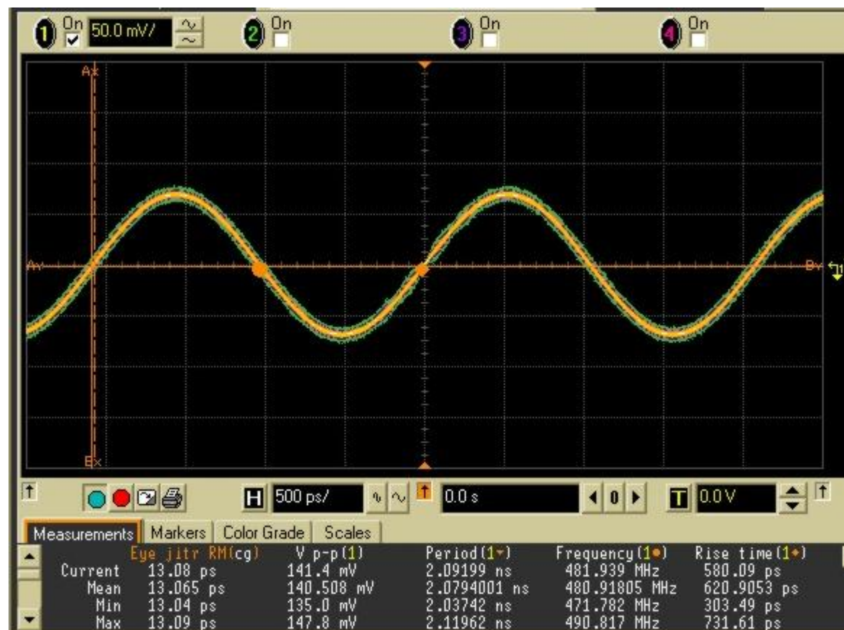

Figure B - 26: Screenshot of the output signal of the PLL captured at the sum port of the 180° hybrid coupler.

B.11.4 Frequency divider output

The output of the PLL that is obtained from the hybrid coupler sum port is fed into the frequency divider circuit to obtain the stabilized ~ 40 MHz clock signal. The frequency divider circuit that is used in this work is the HMC705LP4 from the Hitite Microwave Corporation. The block diagram of the setup used to obtain the stabilized ~ 40 MHz clock signal is shown in figure B-27. The output signal of the divider circuit board as measured in a DSO is shown in figure B-28. The mean RMS jitter and the mean Pk-Pk jitter in the divider output signal are 2.66 ps and 16.67 ps respectively.

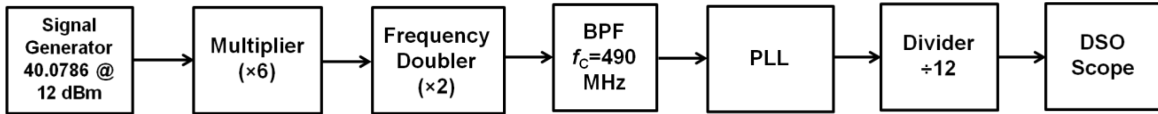

Figure B - 27: Block diagram of the PLL system with divider.

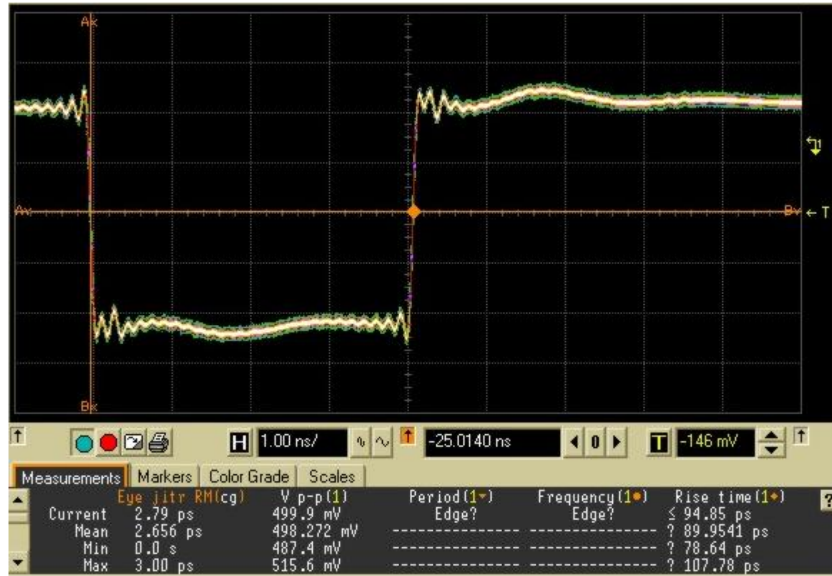

Figure B - 28: Screenshot of the output signal of the frequency divider measured in a DSO.

B.11.5 Frequency divider output using VCO with higher K_{VCO}

In section B.11.4, the jitter was measured in the PLL output using a VCO with K_{VCO} of 50 Hz/V. As a test this VCO is replaced with a VCO having a K_{VCO} of 7.5 MHz/V manufactured by Crystek Corporation. The K_{VCO} is calculated by dividing the electrical tuning range of the VCO with the tuning voltage range of the VCO. The calculation of the K_{VCO} for the Crystek VCO is shown in (B.5).

$$K_{\mathrm{VCO}} = \frac{\mathrm{Electrical_Frequency_Tuning_Range}}{\mathrm{Voltage_Tuning_Range}} = \frac{30 \times 10^{6}}{4} = 7.5 \frac{\mathrm{MHz}}{\mathrm{V}} \tag{B.5}$$

The output of the divider using Crystek VCO in the PLL loop is shown in figure B-29. It is apparent from the figure B-29 that the jitter in the ~ 40 MHz output signal is greater than the similar setup using a VCO with lower K_{VCO} value (i.e.: VCO with K_{VCO} = 50 Hz/V). The reason for high jitter is a change of 1/10 of a Volt in the tuning voltage results in a change of 750 KHz. Hence, there will be tradeoff between the locking time of the PLL and the stability of the system.

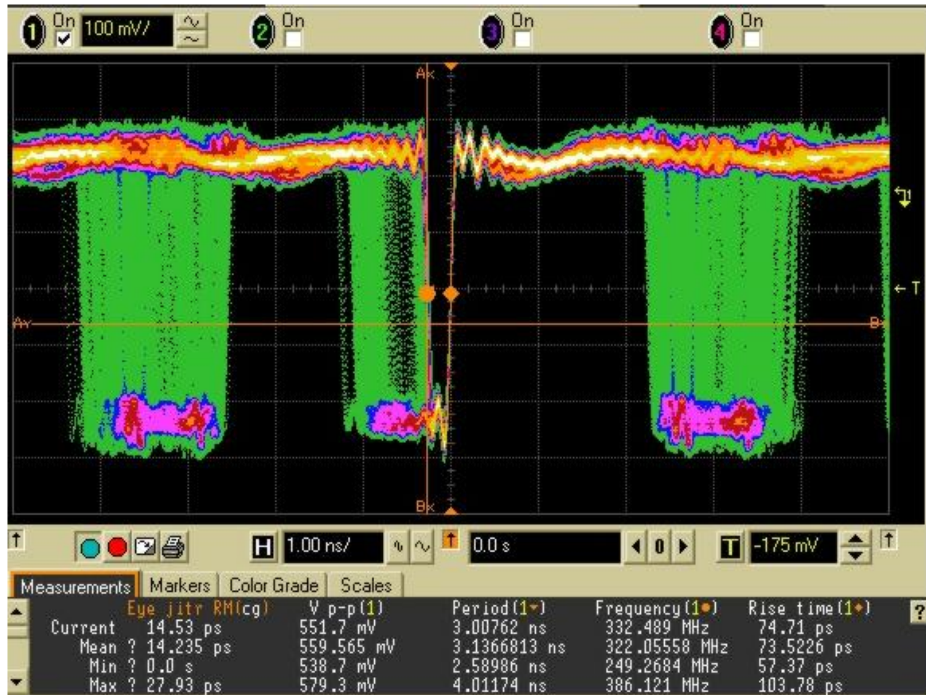

Figure B - 29: Screenshot of the output signal of the frequency divider measured in a DSO using a VCO with K_{VCO} value of 7.5 MHz/V.

B.11.6 Simulation results

Simulations were carried out to obtain the locking time of the PLL using Advanced Design Systems (ADS) 2013.06 simulation tool. A simple PLL was constructed as shown in figure B-30. Here, the unstabilized reference signal is generated using a combination of “ATLAS_Upconverted_Signal” and “Phase_Noise_Generator” blocks. This signal is then fed into the phase frequency detector (PFD1) whose secondary input is the output of the VCO (initially free-running). The output of the phase frequency detector is proportional to the difference in frequency (or constant phase) of its two input signals. This output signal is filtered using a LPF and amplified (if needed) and fed into the input port of the VCO. The output frequency of the VCO changes with the dc voltage fed into its input port. Once the loop is locked when either the output frequency of the VCO is equal to the reference frequency or the phase difference between the output signal of the VCO and reference signal is constant. The simulation results were not obtained due to computational limitation (insufficient Random Access Memory) of the author’s system at the time of this work.

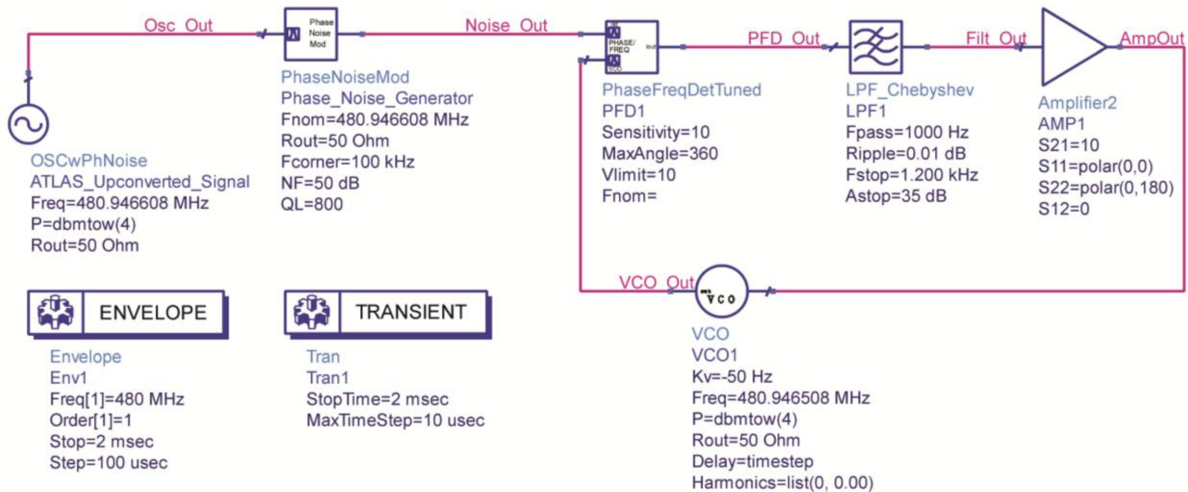

Figure B - 30: Block diagram of a PLL system in ADS simulation tool.

B.12 Conclusion

A timing circuit is designed using a PLL to stabilize the reference signal. A proof of concept is demonstrated by implementing a single arm of the system. An up-conversion circuit is designed which provides a ~ 480 MHz signal with tolerable jitter. Also a down-conversion circuit is implemented in order to obtain a stabilized ~ 40 MHz clock signal. The output jitter of the implemented timing circuit is < 3 ps RMS which meets the required specifications of the system. Currently, the system is successfully implemented using an 18 m cable.

B.13 Further research

The further research in this area includes the work mentioned below:

- Addition of the 280 m long cable between the Tx and the Rx. The addition of long cable will require a design of dc amplifier to take in to account the insertion loss in the cable. Also dispersion of the cable will need to be accurately accounted for to minimize the jitter in the output signal.
- Design of the dc amplifier to take into account the insertion loss due to the long cable
- Run test for 2 arms A and B to show it can work in CERN
- Arranging all the circuit components in a chassis for ease of handling (form factoring)

- Design of a BPF for the up-conversion circuit with narrow bandwidth (~ 50 MHz) to filter the harmonics entering the PLL system
- A phase frequency detector can be used instead of a mixer to compare the VCO output signal with the reference signal. This would prevent generation of harmonics due to mixer operation.

Appendix C

C.1 Bill of materials list for the timing circuit

Table C - 1: Bill of materials for the timing circuit for a single arm

	Component Description	Part Number	Manufacturer	Quantity	Alternate Component
1	Frequency multiplier (×6)	SN65LVDS150	Texas Instruments, Inc.	1	-
2	Frequency doubler (×2)	ZX90-2-13-S+	Mini-circuits	1	-
3	Band-pass filter	TB-122B	Mini-circuits	1	-
4	Mixer	ZX05-1MHW-S	Mini-circuits	1	-
5	Low-pass filter	SLP-100+	Mini-circuits	1	-
6	Directional coupler	ZX30-20-4-S	Mini-circuits	1	10013-20 (Anaren Microwave, Inc.)
7	Power Detector	ZX47-55LN-S+	Mini-circuits	2	-
8	Bias tee	ZX85-12G+	Mini-circuits	2	-
9	Circulator	0045CAS	Nova Microwave, Inc.	1	-
10	High-pass filter	SHP-400+	Mini-circuits	1	-
11	Low-pass filter	SLP-550+	Mini-circuits	1	-
12	2 Way splitter	ZFRSC-42+	Mini-circuits	1	PS2-03-450/1S (Pulsar Microwave, Corp.)
13	RF amplifier	ZFL-500HLN+	Mini-circuits	2	
14	Isolator	0045IAS	Nova Microwave, Inc.	1	-
15	Attenuator, continuously variable	0682-10	Arra Inc.	2	-
16	VCO	500-25329	Wenzel Associates, Inc.	1	-
17	PID controller	SIM960	Stanford Research Systems	1	-

	Component Description	Part Number	Manufacturer	Quantity	Alternate Component
18	PID controller mainframe	SIM900	Stanford Research Systems	1	-
19	Phase shifter	980-2K	Aeroflex Weinschel	1	JSPHS-661+ (Mini-circuits)
20	180° hybrid coupler	H7877	Werlatone	1	-
21	Bi-directional coupler	3020A	Narda Microwave-East	1	-
22	Divider	116993	Hittite Microwave Corporation	1	-
23	280 m long cable	-	Andrew-Heliax	1	-

C.2 Timing circuit components layout

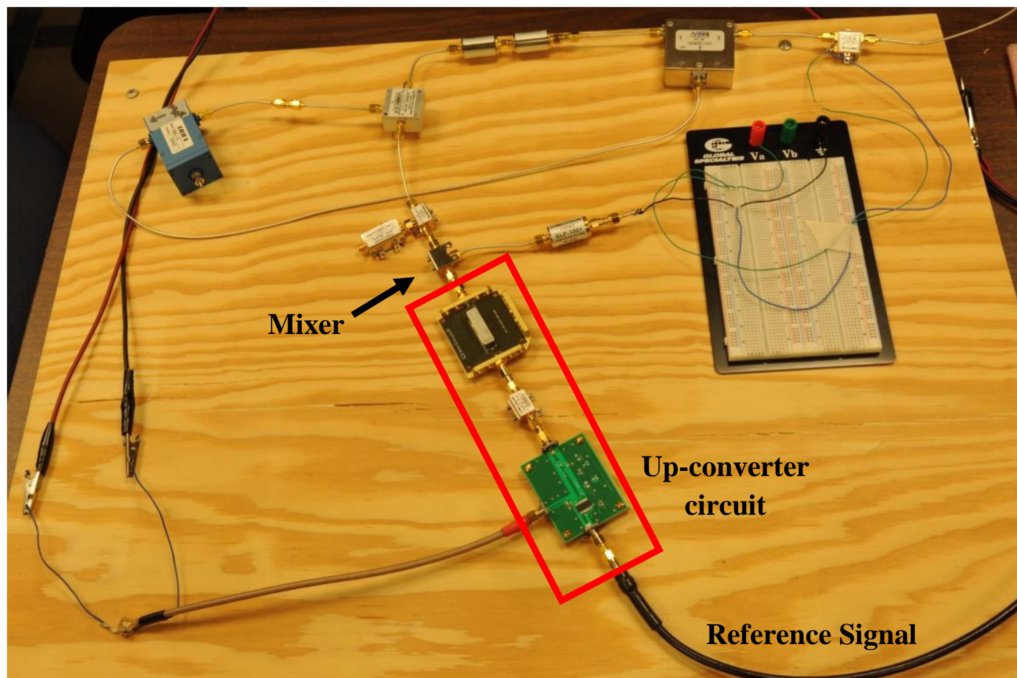

Figure C - 1: Component layout on the transmitter side (Tx) of the timing circuit.

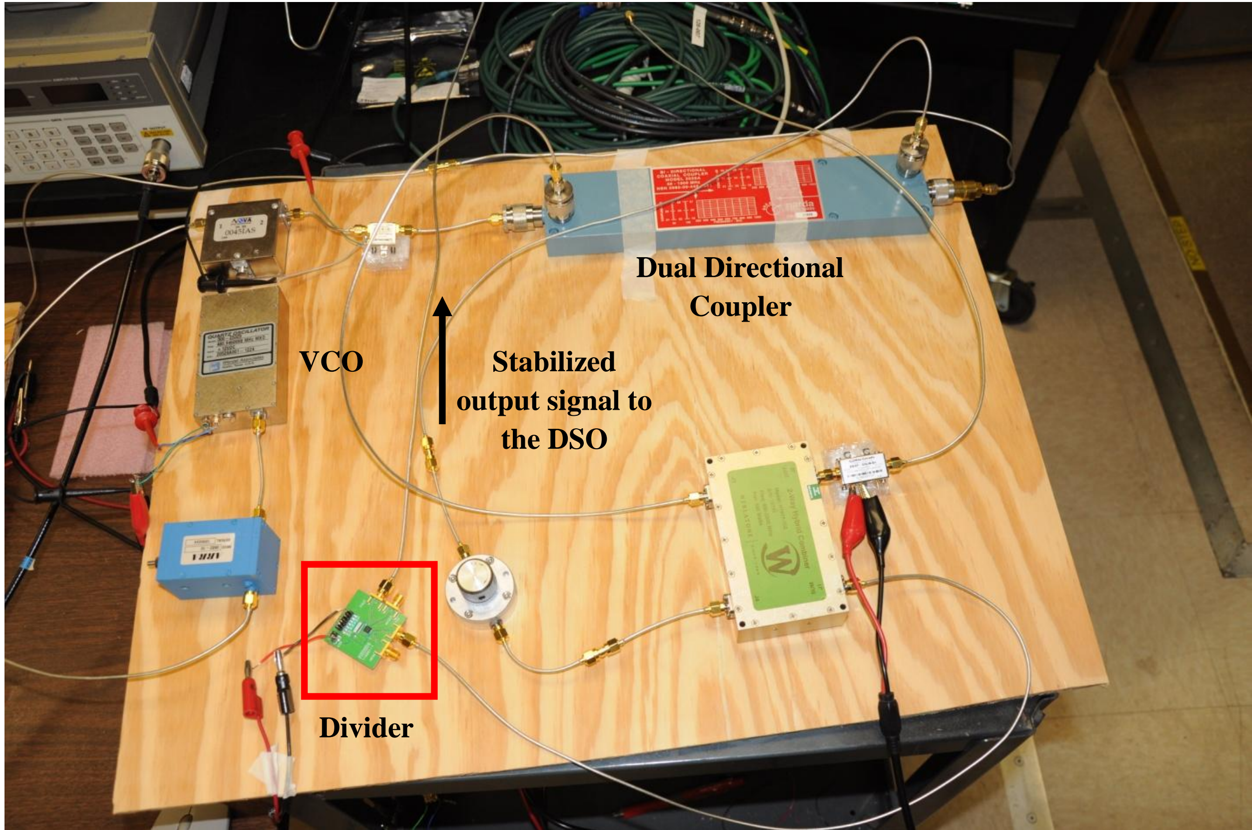

Figure C - 2: Component layout on the receiver side (Rx) of the timing circuit.

REFERENCES

[1] J. D. Cressler, "Silicon Heterostructure Devices", CRC Press, 2008.

[2] F. K. Lutgens and E. J. Tarbuck, "Essentials of Geology", 7th Ed., Prentice Hall, 2000.

[3] D. V. Morgan and R. H. Williams, "Physics and Technology of Heterojunction Devices", *IEE Materials and Devices Series 8*, Peter Peregrinus Ltd., 1991.

[4] J. L. Buie, "Coupling transistor logic and other circuits", issued 1966-11-01, assigned to TRW Semiconductors, Inc.

[5] J. Wamock, P. F. Lu, J. D. Cressler. K. A. Jenkins and J. Y. C. Sun, "35 GHz/35 PSEC ECL PNP TECHNOLOGY", *International Technical Digest on Electron Devices*, pp. 301-304, 1990.

[6] H. Kroemer, "Theory of a wide-gap emitter for transistors," *Proceedings of IRE*, vol. 45, pp. 1535-1537, 1957.

[7] B. S. Meyerson, "Low-temperature silicon epitaxy by ultrahigh vacuum/chemical vapor deposition," *Applied Physics Letters*, vol. 48, pp. 797-799, 1986.

[8] P. Ashburn, "SiGe Heterojunction Bipolar Transistors", John Wiley & sons, 2003.

[9] D. J. Paul, "Si/SiGe heterostructures: from material and physics to devices and circuits", *Semiconductor Science and Technology*, vol. 19, no. 10, pp. 75-108, September 2004.

[10] B. M. Tenbroek, M. S. L. Lee, W. R. White, R. J. T Bunyan and M. J. Uren, "Impact of Self-Heating and Thermal Coupling on Analog Circuits in SOI CMOS", *IEEE Journal of Solid-State Circuits*, vol. 33, no. 7, pp. 1037-1046, July 1998.

[11] J. D. Cressler, "SiGe HBT technology: A new contender for Si-based RF and microwave circuit applications," *IEEE Trans. Microwave Theory and Technology*, vol. 46, pp. 572-589, 1998.

[12] N. Zerounian et. al., "500 GHz cutoff frequency SiGe HBTs", *Electronics Letters*, vol. 43, issue 14, pp. 1-2, July 2007.

[13] C. Jungemann and S. M. Hong, "Investigation of electronic noise in THz SiGe HBTs by microscopic simulation", *IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, pp. 1-8, September 2013.

[14] D. Barlas et. al., "SiGe transistor technology for RF applications", *Microwave Journal*, June 1999.

[15] V. Jain et. al., "Study of mutual and self-thermal resistance in 90 nm SiGe HBTs", *IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, pp. 17-20, September-October 2013.

[16] R. Sampathkumaran and K. P. Roenker, "Effects of self-heating on the microwave performance of SiGe HBTs", *Solid-State Electronics*, vol. 49, issue 8, pp. 1292-1296, Aug. 2005.

[17] J.J. Liou and F. Schwierz, "RF/microwave transistors: evolution, current status, and future trend", *Electron Devices Meeting*, pp. 5-10, 2002.

[18] S. W. Amos and M. R. James, "Principles of Transistor Circuits", 9th Edition, Newnes, 2000.

[19] W. Liu, "Handbook of III-V Heterojunction Bipolar Transistor", John Wiley & Sons, Inc., 1998.

[20] W. Fonger, "A determination of 1/f noise sources in semiconductor diodes and transistors", in Transistor I, Princeton, NJ RCA Labs, pp.239-297, 1956.

[21] C. T. Sah and F. M. Heilscher, "Evidence of surface origin of the 1/f noise", *Physical Review Letters*, vol. 17, no. 18, pp. 956-958, October 1966.

[22] P. Narozny, H. Dambkes, H. Kibbel and E. Kasper, “Si/SiGe heterojunction bipolar transistor made by molecular-beam epitaxy”, *IEEE Transactions on Electron Devices*, vol. 36, no. 10, pp.2363-2366, October 1989.

[23] H. G. Grimmeiss, J. Olajos and J, Engvall, “SiGe: a promise into reality?”, *Semiconductor Conference*, pp. 17-26, October 1995.

[24] A. J. Joseph, J. D. Cressler and D. M. Richey, “Optimization of Early voltage for cooled SiGe HBT precision current sources”, *Journal of Physics IV*, vol. 6, pp. 125-129, 1995.

[25] E. Crabbe *et. al.*, “Current gain rolloff in graded-base SiGe heterojunction bipolar transistors”, *IEEE Electron Device Letters*, vol. 14, no. 4, pp. 193-195, April 1993.

[26] Private communications with Dr. R. L. Carter.

[27] Private communications with Dr. W. A. Davis.

[28] B. M. Tenbroek, M. S. L. Lee, W. Redman-White, C. F. Edwards, R. J. T. Bunyan, and M. J. Uren, “Measurement and Simulation of Selfheating in SOI CMOS Analogue Circuits,” *IEEE International SOI Conference Proceedings*, 1997, pp. 156–157.

[29] M. Asheghi, Y. K. Leung, S. S. Wong, and K. E. Goodson, “Phonon–boundary scattering in thin silicon layers,” *Applied Physics Letters*, vol. 71, no. 13, pp. 1798–1800, September 1997.

[30] M. Asheghi, K. Kurabayashi, R. Kasnavi, and K. E. Goodson, “Thermal conduction in doped single-crystal silicon films,” *Journal of Applied Physics*, vol. 91, no. 8, pp. 5079–5088, April 2002.

[31] W. Bludau, A.Onton, and W.Heinke, “Temperature dependence of the band gap in silicon,” *Journal of Applied Physics*, vol. 45, no. 4, pp. 1846–1848, 1974.

[32] L. Luo, “Physics, compact modeling and TCAD of SiGe HBT for wide temperature range operation”, Ph.D. dissertation, Auburn University, December 2011.

[33] T. Fromherz and G. Bauer, Properties of strained and relaxed Silicon Germanium. INSPEC, London, 1995.

[34] S. Reggiani *et. al.*, “Electron and hole mobility in silicon at large operating temperatures – Part I: bulk mobility”, *IEEE Transactions on Electron Devices*, vol. 49, no. 3, pp. 490-499, March 2002.

[35] S. S. Li and W. R. Thurber, “The dopant density and temperature dependence of electron mobility and resistivity in n-type silicon”, *Solid State Electronics*, vol. 20, pp. 609-616, 1977.

[36] Z. Deshu *et. al.*, “SiGe/Si HBTs with current gain of negative temperature dependence”, *Proceedings 6th International Conference on Solid-State and Integrated-Circuit Technology*, vol. 1, pp. 607-609, October 2001.

[37] K. Mistry, T. Ghani, M. Armstrong, S. Tyagi, P. Packan, S. Thompson, S. Yu, and M. Bohr, “Scalability revisited: 100 nm PD-SOI transistors and implications for 50 nm devices,” *VLSI Symposium Technology Digest*, 2000, pp. 204–205.

[38] G. G. Freeman, B. Jagannathan, S. J. J. Jeng, J. S. S. Rieh, A. D. Stricker, D. C. Ahlgren and S. Subbanna, “Transistor design and application considerations for >200-GHz SiGe HBTs*”, IEEE Transactions on Electron Devices*, vol. 50, no. 3, pp. 645-655, March 2003.

[39] P. S. Chakraborty, S. J. Horst, K. A. Moen, M. Bellini and J. D. Cressler, “An investigation of electro-thermal instabilities in 150 GHz SiGe HBTs fabricated on SOI”, *IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, pp. 141-144, October 2010.

[40] W. Liu, K. E. Yazdani, R. Hussin and M. Asheghi, “Modeling and Data for Thermal Conductivity of Ultrathin Single-Crystal SOI Layers at High Temperature”, *IEEE Transactions on Electron Devices*, vol. 53, no. 8, pp. 1868-1876, August 2006.

[41] Y. Chen, S. Ma, Kuo, Z. Yu, and R. W. Dutton, "An analytical drain current model considering both electron and lattice temperatures simultaneously for deep submicron ultra-thin SOI NMOS devices with selfheating," *IEEE Transactions on Electron Devices*, vol. 42, no. 5, pp. 899–905, May 1995.

[42] M. B. Kleiner, S. A. Kuhn, W. Weber, "Thermal Conductivity Measurements of Thin Silicon Dioxide Films in Integrated Circuits", *IEEE Transactions on Electron Devices*, vol. 43, no. 9, pp. 1602-1609, September 1996.

[43] S. Seth, T. Thrivikraman, P. Cheng, J. D. Cressler, J. A. Babcock and A. Buchholz, "A large-signal RF reliability study of complementary SiGe HBTs on SOI intended for use in wireless applications", *IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, pp. 133-136, October 2010.

[44] J. C. J. Paasschens, S. Harmsma and R. van der Toorn, "Dependence of Thermal Resistance on Ambient and Actual Temperature", *IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, pp. 96-99, September 2004.

[45] R. C. Joy and E. S. Schlig, "Thermal properties of very fast transistors", *IEEE Transactions on Electron Devices*, vol. 17, no. 8, pp. 586-591, August 1970.

[46] K. Etessam-Yazdani and M. Asheghi, "Ballistic phonon transport on strained Si/SiGe nanostructures with an application to strained-silicon transistors," *Proceedings in ITHERM*, 2004, pp. 424–430.

[47] F. N. Masana, "A New Approach to the Dynamic Thermal Modeling of Semiconductor Packages", *Microelectronics Reliability,* vol. 41, pp. 901-912, 2001.

[48] F. N. Masana, "A Closed Form Solution of Junction to Substrate: Thermal Resistance in Semiconductor Chips", *IEEE Transactions on Components, Packaging, and Manufacturing Technology*-Part A, vol. 19, no. 4, December 1996.

[49] P. Palestri, A. Pacelli and M. Mastrapasqua, "Thermal Resistance in SiGe HBTs on Bulk-Si and SOI substrates", *IEEE Transactions on Electron Devices*, vol. 49, issue 6, pp. 1027-1033, August 2002.

[50] K. Bastin, "Analysis and Modeling of Self Heating in SiGe HBTs", *MS Thesis*, EE Department, UTA, August 2009.

[51] A. Karingada, "Estimation of thermal impedance parameters of silicon germanium heterojunction bipolar transistors", *MS Thesis*, EE Department, UTA, August 2011.

[52] M. Schroter and A. Chakravorty, "Compact hierarchical bipolar transistor modeling with HICUM", World Scientific Publishing Co. Pte. Ltd., 2010.

[53] M. Schroter, H. Tran, "Two-/three-dimensional GICCR for Si/SiGe bipolar transistors", *Proceedings of WCM International NanoTech Meeting*, Anaheim (CA), pp. 99-104, 2005.

[54] M. Schroter, "High-frequency circuit design oriented compact bipolar transistor modeling with HICUM", (inv. paper), *IEICE Transactions on Electronics*, Special Issue on Analog Circuit and Device Technologies, Vol. E88-C, No. 6, pp. 1098-1113, 2005.

[55] A. Pawlak, M. Schröter, J. Krause, D. Céli and N. Derrier, "HICUM/2 v2.3 Parameter Extraction for Advanced SiGe-Heterojunction Bipolar Transistors", *IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, pp. 195-198, 2011.

[56] J. Berkner, "Compact Models for Bipolar Transistors", *European IC-CAP Device Modeling Workshop*, Berlin, March 7-8, 2002.

[57] J. D. Cressler, "Measurement and modeling of silicon heterojunction devices", CRC Press, 2008.

[58] K. Moebus, Y. Zimmermann, G. Wedel, M. Schröter, “Thermal Modeling of BOX/DTI enclosed Power Devices with Green’s Function Approach”, *IEEE SCD*, 4 pages, 2011.

[59] S. Lehmann, M. Weiss, Y. Zimmermann, A. Pawlak, K. Aufinger, M. Schroter, “Scalable Compact Modeling for SiGe HBTs suitable for Microwave Radar Applications", *Digest IEEE SiRF*, Phoenix (AZ), pp. 113-116, Jan. 2011.

[60] M. Schroter, A. Pawlak and A. Mukherjee, “HICUM / L2, A geometry scalable physics-based compact bipolar transistor model”, *Documentation of model version 2.34*, August 2015.

[61] Advanced Design System 1.5, circuit components nonlinear devices manual, February 2001.

[62] Hewlett Packard 4142B modular dc source/monitor operation manual, March 1992.

[63] Cascade Microtech probe selection guide, https://www.cmicro.com/files/Probe-Selection-Guide.pdf.

[64] J. Tang, G. Niu, Z. Jin, J. D. Cressler, S. Zhang, A. J. Joseph and D. L. Harame, “Modeling and Characterization of SiGe HBT Low-Frequency Noise Figures-of-Merit for RFIC Applications”, *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 11, November 2002.

[65] R. Krithivasan, Y. Lu, J. D. Cressler, J. S. Rieh, M. H. Khater, D. Ahlgren, and G. Freeman, “Half-Terahertz Operation of SiGe HBTs”, *IEEE Electron Device Letters*, vol. 27, no. 7, July 2006.

[66] D. V. Morgan and R. H. Williams, “Physics and Technology of Heterojunction Devices”, *IEE Materials and Devices Series 8*, Peter Peregrinus Ltd., 1991.

[67] R. S. Muller, T. I. Kamins and M. Chan, “Device Electronics for Integrated Circuits”, John Wiley & Sons, 3rd edition, 2002.

[68] T. Vanhoucke, H. M. J. Boots and W. D. van Noort, “Revised Method for Extraction of the Thermal Resistance Applied to Bulk and SOI SiGe HBTs”, *IEEE Electron Device Letters*, vol. 25, issue 3, pp. 150, March 2004.

[69] R. M. Fox and S. G. Lee, “Scalable Small-Signal Model for BJT Self-Heating”, *IEEE Electron Device Letters*, vol. 12, issue 12, pp. 649, December 1991.

[70] J. S. Rieh, D. Greenberg, B. Jagannathan, G. Freeman and S. Subbanna, “Measurement and Modeling of Thermal Resistance of High Speed SiGe Heterojunction Bipolar Transistors”, Silicon Monolithic Integrated Circuits in RF Systems, pp. 110, September 2001.

[71] Timing, trigger and control (TTC) systems for the LHC, http://ttc.web.cern.ch/TTC/.

[72] Frequency dividers & detectors – SMT manual, HMC705LP4/705LP4E datasheet, v03.0709, Hittite Microwave Corporation.

[73] F. A. Losee, “RF systems, components, and circuits handbook”, Artech House, second edition, 2005.

[74] P. Eskelinen, “Introduction to RF equipment and system design”, Artech House Inc., 2004.

[75] P. R. Gray et. al., “Analysis and design of analog integrated circuits”, John Wiley & sons, Inc., fourth edition, 2001.

[76] D. H. Navon, “Semiconductor microdevices and materials”, Holt, Rinehart and Winston, 1986.

BIOGRAPHICAL INFORMATION

Valay D. Shah was born in state of Gujarat, India in September 1984. He received his Bachelor of Engineering degree in Electronics and Communication Engineering from Nitte Meenakshi Institute of Technology, Bangalore, India, in 2007. The author commenced his graduate studies in Electrical Engineering department at the University of Texas at Arlington in August, 2008 to achieve expertise in the field of device modeling and fabrication. During his graduate studies he worked as Graduate Research Assistant in Analog IC Research group under the guidance of Dr. Ronald Carter, Dr. Alan Davis and Dr. Howard Russell. He received his M.S and Ph.D. degrees in Electrical Engineering in 2011 and 2016 respectively from UT, Arlington. He has worked on the analysis and modeling of SiGe HBTs, in co-ordination with Texas Instruments, Inc. (Santa Clara location). Also he has designed a timing circuit using a phase locked-loop in collaboration with Dr. Andrew Brandt from Physics Department at UT, Arlington. His research interests include device physics and modeling and device fabrication.