A COMPARATIVE STUDY OF THE THERMO-MECHANICAL BEHAVIOR OF WCSP
ASSEMBLY DUE TO DIFFERENCE IN PCBS’ LAYER THICKNESS

by

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Presented to the Faculty of the Graduate School of
The University of Texas at Arlington in Partial Fulfillment
of the Requirements
for the Degree of

MASTER OF SCIENCE IN MECHANICAL ENGINEERING

THE UNIVERSITY OF TEXAS AT ARLINGTON

MAY 2016
DEDICATION

This thesis is dedicated to my father and my sister who made everything possible. Without them I would not have been in the position I am in today. I would also like to dedicate to all the important persons in my life for their support and encouragement.
I would like use this opportunity to express my gratitude to Dr. Dereje Agonafer for giving me a chance to work at EMNSPC and for his continuous guidance throughout my time in UTA. It has been a wonderful journey working with him in research projects and an experience to learn so much from him. I also thank him for serving as the committee chairman.

I would like to thank Dr. A. Haji-Sheikh and Dr. Fahad Mirza for serving on my committee and providing numerous learning opportunities.

I want to thank all the people I met at EMNSPC and for their support during my time. Special thanks to Ms. Sally Thompson, Ms. Debi Barton, Ms. Delania Gordon for assisting me in almost everything. You all have been wonderful. Special Thanks to Mr. Kermit Beird for helping me with all the sample preparation, without him this thesis would not have been completed.

Special thanks to Dr. Ashfaq Adnan for letting me use the Shimadzu for many experiments.

May 6, 2016
ABSTRACT

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The reliability of Chip Scale Package assembly is of great concern for the electronic industry. Due to multiple function integration of the present devices there is a high demand of ultra-miniaturization of the integrated parts to build the inside circuit assembly. Wafer Level Chip Scale Packages (WLCSP) are used in the industry to meet the challenges of these miniaturization due to its form factor, not so high cost and packaging efficiency which is also very high despite the known and unknown reliability issues. WLSCPs use packaging technology at the wafer level which is an extension of the wafer fab process where the final device is a die with an array pattern of solder interconnects. This WLCSP stands out from the regular Ball Grid Array (BGA) and laminate based Chip Scale Packages as there are no bond wires or interposer used for connections, but WLCSP has issues which makes the solder life short and so concerning ourselves with their reliability should be our prime concern.

In the whole assembly a crucial part of reliability is played by the Printed Circuit Boards (PCB) which is a multi-layered structure. During Thermal cycling test, stress is accumulated in the solders due to mismatch of coefficient of thermal expansion (CTE) between the PCB and the package. In a PCB there are multiple layers and on their own possess different material properties and overall has effect on the properties of the board.
itself which is by nature orthotropic. So significant warpage also occurs in PCB which has an effect on the solder joints. By removing the layers or through different composition of the layers of the PCB changes the material properties of the board. It affects the life of the solder balls either in a good way or a bad way. The primary objective of this work is to make an effort to look into the possible effects of individual layers during thermal cycling and thermal shock, to see the effect of ramp and dwell time on the WCSP assembly by considering layer removal from the PCBs, thus changing the overall thickness of the boards.
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Chapter 1

INTRODUCTION

There are around ten trillion solder interconnections made globally for mobile devices, computers, medical, aerospace and military applications. Solder interconnections provide mechanical and electrical connections between PCB and the package. The whole system fails if failure occurs at the solder interconnections, which is why it is imperative to understand the failure methods and the reliability of the boards and solders [1]. Environmental conditions have a major impact on the durability and reliability of PCBs. Temperature fluctuations create thermal fatigue in the solder joints and a simple drop creates mechanical shock and vibration in the joints. Vibrations of moving parts can lead to failure in many applications where the PCBs may be used. To understand the behavior of the electronic packages, it is necessary to understand the background and the effect of environments on the products.

1.1 Role of Packaging

From the first diode invention in 1904 to smart watch on our hands, technological advances have been tremendous and made a huge impact on our lives. Electronics are at the heart of this advances and most of the things would not have been achieved if for the continuous efforts of the packaging engineers.

Electronics are being extensively used in our daily lives, starting from entertainment to the military and aerospace applications. As time goes by, consumers want electronic products to be cheaper, faster and lighter. They want high density information to be processed by the electronics. The first step towards the manufacturing of electronics is the integrated circuits (ICs). An IC has a substrate and many thin layers of different
thickness ranging from 100 nm and 1 μm [2]. The substrate in an IC acts like mechanical carrier during processing. Figure 1.1 shows a cross-section of a typical IC.

![Figure 1.1 Cross section of an IC](image)

The next step is packaging and it plays a vital role by ensuring that the package is handles properly. The electronic devices are protected from the environment and other factors. The packages also enhance the thermal and electrical properties. The following Figure 1.2 shows the trend in the electronic packages. Chip scale packages have led the miniaturization of packages. Wafer level chip scale packages have reduced the size even further helping the electronic products to be reduced in sizes.

![Figure 1.2 Different Types of Electronic Packages](image)
Packages can be classified as

- Through Hole Mount IC Packages
- Surface Mount IC Packages
- Contactless Mount IC Packages

Figure 1.3 Trends in Electronic Packaging [4]

The figure shows the trend in packaging and it shows that DIP or Dual In-line packages was used first. It has a rectangular house and two sets of pins on either side of the house. To meet the narrower pitch of the pins requirements QFP or quad flat package came into picture. It has leads extending from all sides of the package. To continue with the demands of increased pins, flip chip came into play. 3D packaging technology with through silicon via (TSV) is increasing researched for next generation technologies. These packaging include POP (stacked multi-chip package) and COC (chip on chip) [4].

1.2 Efficiency of the Packaging

One of the important parameters in miniaturization of electronic products is the packaging efficiency. It is defined as the ratio of die area to the IC package area. So as per the definition, bare package has an efficiency of 100%. BGA or ball grid array has an
efficiency of 30-40%. Chip scale package is something which does not have an efficiency of more than 50% and the perimeter is not more than 20% of the chip [3]. Due to the

Figure 1.4 Classification of packages

rising demand of portable and small products, the CSP has become very popular. The reason for that, CSP does not need an underfill which is an important part for flip chip
packages. The CSPs take the thermal coefficient difference well and so they are popular among the portable products. They can also be mounted on standard surfaces without major modifications. The wafer level chip scale packages, on the other hand, have better packaging efficiencies.

1.3 Wafer Level Chip Scale Packages

According to JESD30D, the definition of Chip scale Package (CSP) is “A package whose area is generally no greater than 120% of the area of the semiconductor device it contains” [5]. It has the ease of handling, testing and assembly of chips. It also has the advantage of direct surface mounting [6].

Wafer level chip scale packages are one type of CSPs where the IC is attached faced down on the boards using technologies of surface mounts. This technology does not use the traditional process where the package of each unit is assembled after wafer dicing. The package is kind of the same size as the die [7]. These devices allow the smallest possible form factor in the design. It is sometimes called the true chip scale as it has the same size as the die.

The advantages of WCSPs are:

- Space savings
- Lowest cost per I/O and lowest cost of electrical testing
- No need of underfills and have easier management of inventory [7]

According to Prismark and TechSearch International, there are four WLP technologies:

1. Redistribution Layer and Bump
2. Encapsulated Copper Post
3. Encapsulated Wire Bond
4. Encapsulated Beam Lead [7]

The most widely used WLP technology is the Redistribution Layer and Bump technology. This process deposits on the wafer a multi-layer metal rerouting and interconnection system to each device. Bonding pads are redistributed to underbump metal pads (UBM) and the solder balls are placed over these UBM pads.

Figure 1.5 Wafer Level Package Assembly

According to Yole.com, “Wafer-level-packaging market is gaining more and more significance in the semiconductor industry; it shows the greatest potential for significant future growth in the semiconductor industry.” The figure shows the prediction made by them in terms of the growth and trend in market.

![Global Wafer-Level-Packaging Demand](chart.png)

Figure 1.6 Demand of Wafer-Level-Packaging [8]
1.3.1 Overview of Package Construction

Figure 1.7 Cross-section of an WCSP [9]

Figure 1.8 Process flow of an WCSP [9]
The device has solder balls directly attached to it after processing the silicon die. The die has a passivation layer on it, followed by one polymer di-electric layer and a redistribution layer. Another layer of polymer layer is given and then UBM is deposited on top of it. The solder balls are attached on top of the UBM pads. So the whole system is actually an array of solder balls on a die. The solder balls are lead-free and it was an important transition from lead based to lead free materials.

1.4 Board Level Reliability

The reliability at the board level is usually expressed as the life of the solder joints. With the packaging, it actually means that the material movement is properly characterized. How the failure mechanisms change with the stress, is the subject matter of reliability. To understand the reliability of electronic packaging, stress and its affect should be understood first. That is, BLR shows the behavior or thermo-mechanical degradation of the assembly with time.

There are two levels of reliability, 1st level and the 2nd level. 1st level is not concerned with the solder interconnects but rather concerned about the whole package’s robustness. On the other hand, the 2nd level is concerned about the solder joint interconnects [10].

In reliability practice, one of the most important curve people follow by is the bathtub curve. It shows the total operation of devices over a period of time. That is, it shows the time dependent failure or hazard rate of the component. The curve has three distinct portion – 1. Early failure or burn-in period, 2. Random failure or useful period and 3. Wear-out period [11]. The first failures occur due to weak design, errors in the assembly or due to damaged components. After this region is done, the bad components are all taken out. The next region is a flat curve and it is the random region. The failure here mainly occurs
due to poor maintenance, accident or due to handling. That is, aside from some random failures, all the components reach their desired life and run smoothly. The third region is the wear out region and this failure occurs due to exceeding the life and fails due to wear or fatigue or corrosion.

![Bath-tub Curve](image)

Figure 1.9 Bath-tub Curve [12]

Thermo-mechanical characterization in BLR can include many conditions like thermal cycling, shock, bending or vibration. Whether mechanical characterization is done or not depending on the usage, thermal cycling is almost always done on the assembly. In reliability assessment, thermal cycling simulations is done to get a quick idea of the stress generation and its effect on the critical solder joints of the board. This approach can predict the location of the solder joint and the failure.

The prominent factors that affect the board level reliability are:

- Material of the PCB, thickness of the board and the design
- Materials of the solder balls used
- Dimensions of the die
- Mold compounds [13]
That means there are many factors that might affect the solder joint reliability in WCSP assembly but for this study only the material of the PCB and the thickness are assessed under the thermal cycling and thermal shock.

1.4.1 Thermal Cycling Test

Thermal cycling is done to see how the components resist being exposed to high and low temperatures running alternatively. Thermo-mechanical stress is generated in the solder joints due to the coefficient of thermal expansion mismatch between the board and the package during this thermal fatigue. This mismatch causes crack, delamination or warpage. The important factors to keep in mind are the temperature extremes, the ramp and dwell time, the ramp rates which indicates the frequency of the cycle. Since it is a plastic dominated cycle, significance of creep is also important to observe. Weibull distribution is used reflect the behavior of the failure rate. Here the Table 1.1 shows the temperature profile used in industries according to the applications.

Table 1.1 Temperature Profile for electronic products

<table>
<thead>
<tr>
<th>Use condition</th>
<th>Thermal excursion (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Consumer electronics</td>
<td>0 to 60</td>
</tr>
<tr>
<td>Telecommunications</td>
<td>-40 to 85</td>
</tr>
<tr>
<td>Commercial aircraft</td>
<td>-55 to 95</td>
</tr>
<tr>
<td>Military aircraft</td>
<td>-55 to 125</td>
</tr>
<tr>
<td>Space</td>
<td>-40 to 85</td>
</tr>
<tr>
<td>Automotive-passenger</td>
<td>-55 to 65</td>
</tr>
<tr>
<td>Automotive-under the hood</td>
<td>-55 to 160</td>
</tr>
</tbody>
</table>
1.4.2 Thermal Shock Test

Thermal shock test occurs when there is a sudden temperature change in the environment. Thermal shock test mimics that behavior by following certain standards. The thermal shock may occur when a hot engine goes to a cold temperature. Or when a rocket goes to outer space, there is a continuous fluctuations of temperature. According to the JEDEC standard, JESD22-A106, the temperature profile is taken as -55 to 125ºC.

1.5 Motivation and Objective

1.5.1 Motivation

It has become very important to identify the causes behind failures, as lots of time and money go into the development of the products. The failure in the products occur due to many reasons like environment, temperature, contaminants, moisture, etc. Stresses are generated in the solders due to the effect of the thermal cycling. This happens due to the big temperature difference cause different expansion/contraction in the materials of the package assembly. As the solder is not flexible, it fails to comply and ultimately starts to crack. The stress developed may cross the strength of the materials and crack starts to occur. According to literature, the reliability is inversely proportional to the thickness. That is as the thickness reduces the reliability increases. Thicker boards are not flexible enough to counter the stress generation. Whereas the thinner board is more flexible and thus reduces the stress that is generated in the components [14]. Two boards of 0.7 and 1 mm boards with WCSP were taken and it was believed that the 0.7 mm board will last longer than the 1 mm board. On the contrary, the 0.7 mm board failed faster under thermal cycling. The layer stack-ups were different but on the basis of thickness the 0.7 mm board should have lasted longer. That means, to ensure better life not only thickness but also decisions regarding material and their properties are important.
1.5.2 Goals and Objective

It is very important to determine why the thinner board is failing before the thicker board when the contrary should have happened. The primary objective of this study is to determine the causes behind the anomalies between the two boards. To achieve this, layers were removed from the 1 mm board. At first, the top copper layer was removed and the thickness of the first new board became 0.94 mm. Then the second layer is removed and the thickness of the second new board becomes 0.89 mm. As the percentage of copper and FR4 varies among the four boards (1, 0.94, 0.89 and 0.7 mm) the properties also change and so the behavior. The boards are tested for Young’s Modulus and coefficient of thermal expansion. Then the boards are observed under the ATC test using FEA simulations. The stress generation and behavior are observed under this condition. As the real time behavior of the two new boards are unknown, all the boards are also put under thermal shock test with modified ramp and dwell time to individually see the effect of time and frequency of the cycles. The simulations are performed in ANSYS 16.1. Overall, this might give an idea on which parameters are affecting which board and so ultimately what parameters are needed to be changed are the objectives of this study. This study tries to
find the trend of the change of behavior, i.e., to see if a particular design with one kind of board is better or worse.
Chapter 2

LITERATURE REVIEW

Electronic Products are getting more complex and thinner, lighter with higher density and speed. With the advancements, many researches had been conducted for many years and the products are getting better. But as more advances are being made, the issues of reliability are building up.

2.1.1 Accelerated Thermal Cycling Test

Accelerated thermal cycling was performed to observe the reliability of the solder joints and to understand the mechanism behind future failure. Accelerated tests are widely used in the electronic packaging business. The most commonly used accelerated test is the accelerated thermal cycling test. There are number of accelerated thermal cycle profile depending on the usage and the industry. At what temperature the boards are being used and the intensity determines the cycle of the ATC.

![Figure 2.1 Different Thermal Cycling Profile used in the industry [15]](image-url)
One of the most important tests is accelerated thermal cycling test and test method for temperature cycling is defined by the JEDEC standard JESD22-A104D. It applies to single, dual and triple chamber thermal cycling. Typical temperature cycle rates for component level are 1 to 3 but higher can be done if needed. For solder joints the cycles are slower with rates from 1 to 2 per hour. That is cycle times less than half an hour is not recommended by JEDEC. For Lead or Tin based solder highest temperature to exceed 125°C is not recommended. It might create dynamic recrystallization [16].

Due to thermal cycling, warpage is created in the assembly due to CTE mismatch between the materials. According to SEMI G54-93, warpage is defined as “the loss of planarity of a plastic molded surface, excluding protrusions and intrusions”. The warpage poses serious problem for packages especially chip scale packages. Electronic products are used in many applications especially in oil and gas industries, automotive, avionics, etc. They have high temperature applications along with sudden change of temperature. Operating above the $T_g$ can also cause significant change in CTE and flexural modulus and cause failure due to delamination and cracking.
The failure occurs mainly due to shear strain and due to tension and compression around the interconnections. The thermal cycling test was performed on all the package assembly with PCBs of different thickness and material properties to see how changing the thickness affected these stress generations.

Figure 2.4 Deformation observed during thermal cycles [3]
2.1.2 Thermal Shock Test

Thermal shock test is done to see how the PCBs react to a sudden change of temperature. It is the most intense thermal cycling test as the change of temperature is severe. The parts undergo test undergo exposure to very high temperature and then rapidly taken to a very low temperature. Usually it is performed in two chambers, with one chamber kept in hot temperature and the other one in a very low temperature. According to Fan et al. it was seen that failure at solder joints occurs faster for thermal shock rather than for thermal cycling. But the ramp and dwell time have different effect on the solder joint life. A temperature cycle is characterized by the end temperatures, the ramp and the dwell. So it is essential to understand the effect of these parameters to understand the behavior under thermal cycling conditions [17]. There are four temperature profile that can be followed for the thermal shock test – A, B, C and D. The fluids to be used are either water (A) or perfluorocarbon.

2.1.3 Anand’s Model and Fatigue Life Models

After the transition of solder balls from lead based to lead free, the concern for solder joint reliability has increased many fold. Extensive researches are being done on the solder joints based on the solder ball material. Many have developed life prediction models on these lead free solders. Wang et al. has applied Anand’s viscoplastic model to determine the behavior of solder alloys [18]. There are nine material parameters according to Anand. They are: A, Q, ξ, m, h₀, ̃s, n, a and s₀. The internal variable resistance, s shows the averaged isotropic resistance to flow of the plastic in the macroscopic level. The resistance is proportional to the stress.

\[ \sigma = c \cdot s \]

Where c is the material constant.

\[ c = \frac{1}{\xi} \sin h^{-1} \left[ \left( \frac{\xi}{A} e^{\frac{Q}{RT}} \right)^m \right] \]
Where, $\dot{\varepsilon}_p$ is the inelastic strain rate, $A$ is the pre-exponential factor, $Q$ is the activation energy, $m$ is the strain rate sensitivity, $\xi$ is the multiplier of stress, $R$ is the gas constant and $T$ is the absolute temperature.

Now for the formation of $s$ we have,

$$\dot{s} = g(\sigma, s, T) \dot{\varepsilon}_p$$

Where the function $g$ is concerned with strain hardening and dynamic recovery.

Simulation is an important part in the reliability assessment of electronic products. Xu et al. has showed that by using coarse mesh in the global model he located the critical solder joint and also got the same trend in the plastic work generation. It is also mentioned that the CTE mismatch between the package and the board was one of the main causes of solder joints failure. He also did not emphasize on the accuracy of the FE model as long as the design trend was close [19].

According to Tohmyoh et al., the chip size has significant effect on the reliability of the solder joints. He took three packages with dimensions of 4, 6 and 8 mm$^2$ [20]. He also observed that by changing the amplitude the plastic work generation is affected. Some have tried to optimize and tried to use plastic work increment as a measure of the thermo-mechanical performance of the PCB-package assembly. The plastic strain was maximum at top of the solder balls which was consistent with experimental results. As the thermal cycle was increased the value of the plastic strain increased. The change of plastic strain between two cycles gave the plastic strain generated due to change of temperature difference. The value of plastic strain also increased due to the increase of temperature difference. He gave the relationship between the chip size and the generated plastic strain as

$$\Delta \dot{\varepsilon}_p = A \Delta T + B$$

Where
\[
A = (-0.45 \cdot CS^2 + 10.1 \cdot CS - 5.1) \times 10^{-5}
\]

\[
B = (0.46 \cdot CS^2 - 8.73 \cdot CS + 1.00) \times 10^{-3}
\]

Syed has used double power law and hyperbolic sine constitutive equations for the thermal fatigue life prediction models [21]. There are many solder joint fatigue models and are based on different types of criteria. One of the most popular model is the Coffin-Manson Equation and is based on plastic strain.

\[
\frac{\Delta \varepsilon_p}{2} = \varepsilon'_f (2N_f)^c
\]

But since it is based only on the plastic strain, it had to be modified to let into the elastic strain in the equation. The total strain equation takes into account both the elastic and plastic strain [22].

\[
\frac{\Delta \varepsilon}{2} = \frac{\varepsilon'_f}{E} (2N_f)^b + \varepsilon'_f (2N_f)^c
\]
Chapter 3

AYER REMOVAL

To observe the layers it was necessary to do the cross-sectioning of the boards. After the cross-section is exposed, sand paper of grade 600 and 1200 was used to make the surface more polished. To see the section properly, the samples were placed under the microscope with 10 times the magnification. The images showed the number of layers present in each board. The copper layers and the FR4s were noted down. The composition of the boards are 1+6+1 which describes the copper layers. To measure the dimensions of the layers, the images from the microscope were taken into the Analyzing Digital Images software. Determining the dimensions was important as exact measurements was needed to remove the layers from the board. There layers from the one side of the 1 mm board were taken out, that means one copper and one FR4.

Figure 3.1 Sample after Cross-sectioning

Figure 3.2 Optical Microscope with the Sample
After analyzing the images, the combined thickness of the copper in the 1 mm board came out as 300 μm which is 30% of the total thickness. So the rest of the layer consist of FR4 and that is 700 μm or 70% of the total thickness. Two layers were taken out, that means one copper layer and one FR4 layer was taken out. Together they are the prepreg layers on one side of the core layers. Milling machine was used to take out the layers. Cutter was of carbide and the machining was done very carefully. The boards are very thin as it is and so removing with milling machine is difficult. So only one side was used for removing the layers. The dimension of the first layer was 0.06 mm and so the dimensions of the new board became 0.94 mm. The dimension of the second layer was 0.05 mm and so the second new board turned out to be 0.89 mm. As the first layer removed was copper, so the new copper percentage became 25.5%. After removing the second layer, overall percentage of the copper became 27%. Now if we look at the 0.7 mm board, it also has a composition of 1+6+1, the thickness of the copper layers is 180 μm with a percentage of 25.7%. So, the thickness of the FR4 is 0.52 mm which is more than FR4 thickness in 1 mm board.

Figure 3.3 Layer Stack-Ups of 1 mm under microscope
The layers are placed on top of each other in woven structure. So it is not easy to exactly know the total volume. It was a little assumptions on our part for simplification. Just from the images it suggests that, the core layers of 1 mm board are different from the core layers of the 0.7 mm board. The layers of copper are distributes and has uniform thickness.
all over. On the other hand, for 0.7 mm board, the middle two copper layers are thinner than the other layers.

<table>
<thead>
<tr>
<th>Copper Layer L1 - 60 μm</th>
</tr>
</thead>
<tbody>
<tr>
<td>FR4 Dielectric Layer - 50 μm</td>
</tr>
<tr>
<td>Copper Layer L2 - 30 μm</td>
</tr>
<tr>
<td>FR4 Dielectric Layer – 120 μm</td>
</tr>
<tr>
<td>Copper Layer L3 – 30 μm</td>
</tr>
<tr>
<td>FR4 Dielectric Layer – 120 μm</td>
</tr>
<tr>
<td>Copper Layer L4 – 30 μm</td>
</tr>
<tr>
<td>FR4 Dielectric Layer – 120 μm</td>
</tr>
<tr>
<td>Copper Layer L5 – 30 μm</td>
</tr>
<tr>
<td>FR4 Dielectric Layer – 120 μm</td>
</tr>
<tr>
<td>Copper Layer L6 – 30 μm</td>
</tr>
<tr>
<td>FR4 Dielectric Layer – 120 μm</td>
</tr>
<tr>
<td>Copper Layer L7 – 30 μm</td>
</tr>
<tr>
<td>FR4 Dielectric Layer – 50 μm</td>
</tr>
<tr>
<td>Copper Layer L8 – 60 μm</td>
</tr>
</tbody>
</table>

Figure 3.6 Layers Stack-ups of 0.7 mm with dimensions
Chapter 4
MATERIAL CHARACTERIZATION

The material properties were determined in house before giving them as inputs to the computational model. It was done so that the material properties were linked to the boards and not just generalized properties available to use. In this way it was easier to correlate if further experimentations were done on the boards. The properties that were determined are listed below followed by brief descriptions.

- Young’s Modulus, $E$ (GPa)
- Coefficient of Thermal Expansion, $CTE$ ($1/^\circ C$)
- Shear Modulus, $G$ (GPa)
- Poisson’s Ratio, $\nu$

4.1 Coefficient of Thermal Expansion

When there is a thermal stress given on the body, there is a thermal strain which changes according to a property. It is the Coefficient of Thermal Expansion ($CTE$). That means, $CTE$ measures the change in dimension with the change in temperature. It can be either a positive expansion or a contraction. When the expansion is blocked and free expansion is not there, it generates stress in the body.

$$\alpha = \frac{\Delta l}{l \Delta T}$$

Where,

$\alpha$ = Coefficient of Thermal Expansion

$l$ = Original length

$\Delta l$ = Change of length

$\Delta T$ = Change of Temperature
Keeping this in mind, the temperature difference of the cycle is 165°C and so CTE will affect the cycle. When there is a CTE mismatch between the layers, which is when all the stresses are generated in the system. So, CTE is an important parameter and determining CTE was necessary for all the boards to completely define the boards during the temperature cycles.

4.1.1 Thermo-Mechanical Analyzer (TMA)

Thermo Mechanical Analyzer (TMA) was used to determine CTE in the lab. The make and model of the TMA is TMA SS 6000 from Hitachi. The load range of SS 6000 is high, 0.01 mN to 5.8 N, and can measure sample which has single fiber to bulk compositions. The displacement range is from -500 to +500 μm. The resolution and the accuracy is also very high. That means, sample that has low expansion can be measured too. All of these makes this instrument very versatile and capable [23].

Figure 4.1 Thermo-Mechanical Analyzer (TMA)
4.1.2 Theory of Operations

There is a probe in the TMA that measures the expansion and it is made of quartz. A motor is there on top of the probe to control it and has an LVDT to measure the expansion. The probe is housed inside a quartz cylinder. A force is generated by the motor, carried by the probe and given on the sample. The probe is tightly placed on the sample and due to the expansion the probe moves up or down. LVDT measures the expansion through the movement of the probe.

4.1.3 Sample Preparations

Sample dimensions do not follow any standards but there is a limit placed by the instrument itself. The samples used are very small and is in the limit of millimeters. The samples were cut using a hand cutter so that no residual stresses get left behind in the samples. The stresses will generate unwanted effect on the samples and the results might not be valid. The cylinder limits the sample, and the sample can be of 20 mm in height and the diameter can be 8 mm. The height was cut at 10-12 mm so that the samples do not buckle as the thickness is really small. The breadth of the samples was taken at 5-6 mm so that the samples do not touch the cylinder.

Figure 4.2 Samples used in TMA
4.1.4 CTE Measurement

The quartz cylinder houses the samples and the samples are placed directly below the quartz probe. The z-direction of the board is along its thickness. So the to measure along that direction, the samples were placed flat on the plate. A sample of volume 6x6xthickness mm\(^3\) was taken. For PCBs, CTE along x or y should be the same. To measure in that direction, the samples were placed vertically on the plate. A sample of 6x12xthickness mm\(^3\) was taken. Since we only need to measure the expansion, a load of -100 mN was constantly put on the samples through the probe. The temperature was set to 250ºC from 25ºC with a ramp rate of 5ºC per minute. Since the quartz also expanded with the sample, it was necessary to do the correction and remove its influence from the results.

Some examples of CTE measurement data are shown.

![Figure 4.3 Coefficient of Thermal Expansion (0.7 mm)](image)
Figure 4.4 Coefficient of Thermal Expansion (1 mm - xy)

Figure 4.5 Coefficient of Thermal Expansion (0.94 mm - z)
4.2 Young’s Modulus

In stress strain curve, the slope of the curve before the yield strength shows the young’s modulus. It indicates the stiffness and it is the inverse of the compliance of the material. As it is the slope of the stress-strain curve, its unit is in Pa which is the same as the stress. Since it is the reverse of compliance which shows how much the material is compliant, modulus shows how much stiff the material is. That means, it is less likely to be flexible with application of load if the modulus is high. The simple equation given below is the definition of young’s modulus.

\[ E = \frac{\sigma}{\varepsilon} \]

Where,

\( E \) = Young’s Modulus  \\
\( \sigma \) = Stress  \\
\( \varepsilon \) = Strain

4.2.1 Preparations of the Sample

To measure the young’s modulus, the samples are needed to be made in dog-bone shape. This creates uniform stress distribution and needs to have higher stress density in the sample and ultimately causes necking in the sample. There are fillets to reduce the stress concentration. The complete dimensions of the sample are given in Table 4.1. Solidworks model was made and was turned to into the necessary file to use in the CNC machine to cut the samples. The samples were cut off from the board and were taken from the same position to ensure uniformity. The figure shows a general sample used in the measurement of young’s modulus.
Figure 4.6 A typical dog-bone sample

Table 4.1 Dimensions of the sample following ASTM standard E8

<table>
<thead>
<tr>
<th>Dimensions</th>
<th>Length (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Length – L</td>
<td>100</td>
</tr>
<tr>
<td>Width of Grip – C</td>
<td>10</td>
</tr>
<tr>
<td>Width – W</td>
<td>6</td>
</tr>
<tr>
<td>Length of Reduced Part – A</td>
<td>32</td>
</tr>
<tr>
<td>Length of Grip Section – B</td>
<td>30</td>
</tr>
<tr>
<td>Curvature – Dc</td>
<td>4</td>
</tr>
<tr>
<td>Radius of Curvature – R</td>
<td>6</td>
</tr>
</tbody>
</table>

ASTM standards were followed to make the samples. For this kind of boards, to make the samples E8 from ASTM was taken as reference [24]. It was necessary to keep caution so that no slippage occurs. In Instron, it is possible to provide pre-limit of the pressure applied by the jaws on the sample. The samples were aligned in both Instron and Shimadzu by following the markings on the instrument so that they are straight.

The modulus was measured by two instruments. The initial results were measured by Instron Microtester and the results were evaluated later with Shimadzu Universal Testing Machine.
4.2.2 **Instron Microtester**

Instron Microtester was very useful in determining the young’s modulus. The model of the Instron is 5848 and the software used in Bluehill. There are two jaws and the lower jaw is fixed first. To read the extension, extensometer was placed on the samples. It was important to keep the distance of the clips of the extensometer as 12 mm. The load cell used was 2 KN but 1 KN is also available. The rate of extension was given as 2 mm per minute. Before measurement, calibration needs to be done for both the load cell and the extensometer. Extension of the extensometer was directly measured and noted down.

![Instron Microtester](image)

Figure 4.7 Instron Microtester

4.2.3 **Shimadzu Universal Testing Machine**

The Testing machine was useful in many ways, especially in finding out the tensile modulus of the samples. The samples were easily placed in the machine and the readings were taken using the Trapezium software. The directions for placing the samples are given on the machine and they were placed in such ways. A force of 2 N was applied per unit length to the samples.
4.3 Results

The table shows the complete results that were obtained for the evaluation of the boards.

Table 4.2 Complete Material Properties of all the boards

<table>
<thead>
<tr>
<th>Boards</th>
<th>CTE (ppm/°C)</th>
<th>Young’s Modulus (GPa)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>x-dir</td>
<td>y-dir</td>
</tr>
<tr>
<td>1mm</td>
<td>20</td>
<td>20</td>
</tr>
<tr>
<td>0.94mm</td>
<td>14.5</td>
<td>14.5</td>
</tr>
<tr>
<td>0.89mm</td>
<td>15</td>
<td>15</td>
</tr>
<tr>
<td>0.7mm</td>
<td>13.2</td>
<td>13.2</td>
</tr>
</tbody>
</table>

Figure 4.8 Shimadzu Universal Testing Machine
Chapter 5

FINITE ELEMENT ANALYSIS

5.1 Introduction

Discretization has helped to solve many complex problems throughout the history. The value of pi was predicted with immense accuracies by discretizing a circle with polygons of many sides. This concept made its way into the aircraft industry and have not looked back since. Keeping this mind, we can classify mechanics in four different branches. They are – Theoretical, Applied, Computational and Experimental. Finite element methods fall under the computational aspects of mechanics. FEA are used in many applications:

- Aerospace
- Automotive
- Bio-mechanics
- Nuclear Engineering
- Mechanical/Civil

By taking a system as a whole, it is not possible to solve the complex problems so easily. By discretizing and turning them into elements connected by nodes, it is possible to solve many problems. That means for these problems solving them analytically is difficult. So we turn to computational methods called FEA to solve these problems in hand. Through these process of discretization, an approximate methods of solving problems are now available for engineers, scientists, etc. Local equilibrium is established at the nodes and the unknown displacements are solved solving these equations. The general equation for solving the unknowns is

\[ \{F\} = [K] \{u\} \]
Where,

\( \{F\} = \text{Forces at the nodes} \)

\( [K] = \text{stiffness matrix} \)

\( \{u\} = \text{Displacement at the nodes} \)

Here the only unknowns are displacements as the forces are externally applied. The stiffness are dependent on the geometry and the materials used. The displacements are determined at the nodes and meshes are generated to increase the number of nodes. So finer the meshes, higher the accuracy. This also means, however, that the computational time increases. So the best possible way is to optimize between the mesh and the accuracies needed for the jobs at hand.

5.2 Steps for solving FE problems

The general pattern follows some steps. They are:

- The first step is to determine the element properties from the geometric and loading data.
- The second step is to assemble all the equations. All the non-zero coefficients in the matrix can be grouped together in a band. This eliminates usage of large space while computing.
- The third step is to provide all the boundary conditions.
- The final step is to use many different methods to solve the equations [25].

ANSYS is a general purpose commercial software and can be used in many applications. Before using ANSYS few questions are needed to be answered and understood. The objectives, physical systems and mesh are some of the questions. After answering those questions, ANSYS can be used after considering the following points.
- Type of Problem
- Time Dependence
- Nonlinearity
- Modeling simplifications

![Figure 5.1 Steps of matrix formulations][25]

From the analysis standpoint this is a structural analysis where the stress/strain, deformations are determined of a solid body. The quantities evaluated are displacement, stress, strain and reaction forces. The DOF (degree of freedom) or the unknown is the displacement. From many structural problems, the problem in this study falls under static analysis. The loads that are applied and the support conditions do not change with time. Non-linear material and geometrical properties like creep, plasticity are also available.

There are many non-linear properties defined in ANSYS are:

- Plasticity: Permanent deformation but not time dependent
- Creep: Permanent deformation but time dependent
- Viscoelasticity: Non-permanent deformation but time dependent [26]
5.2.1 Considerations for Modeling

Minor details not influencing the results should not be simulated. But it is always better to have an engineering judgment on this matter. For symmetric conditions, it is better to take a portion like half, quarter or quadrant models. This saves a lot of time during simulations. But the symmetry conditions should be followed for all of the factors given below:

- Geometry
- Material Properties
- Loading
- Degree of Freedom

![Figure 5.2 An example of a quarter symmetric model](image)

5.2.2 Considerations for Meshing

Since it depends on discretization, finer mesh means better approximations. But it is not always better to have fine mesh and may cause errors in some cases. Again, engineering decisions regarding meshing is better rather than to have a firm idea. Some regions may need coarse mesh and some regions may need fine mesh. However, there
are some techniques that can be applied to have a better understanding of the mesh. They are

- Adaptive Meshing
- Mesh Refinement Test within ANSYS
- Sub-Modeling [26]
Chapter 6

FINITE ELEMENT ANALYSIS AND SIMULATION

As the two new boards, 0.94 and 0.89 mm, are imaginary and there is no board physically, FEA simulation was imperative to observe the behavior of the boards. The FEA model was developed using commercial software ANSYS Workbench 16.1. This software is commercially available and was extensively used in this project.

6.1 Modeling of Wafer Level Chip Scale Packages

The whole ANSYS procedure can be divided into three steps. They are:

- **Preprocessing**: The model is created and elements and mesh are assigned. The material properties are also given as input.
- **Solution**: The loads and the boundary conditions are given. All the control like step size, solver, etc. are given in this step. The solution is obtained.
- **Post-processing**: The results are reviewed and the desired results are evaluated and mapped.

6.2 Package Geometry

Figure 6.1 shows the cross-section and the layers used in the simulations of the WCSP assembly. All the material properties were taken according to the material shown in the figure. Here the passivation layers used were polyimide (PI-Layers 1 and 2), and the redistribution layer (RDL) is made up of copper. All of these layers and the UBM were modeled in ANSYS. The Table 6.1 shows all the material properties used in the simulations [27] [28] [29].
The properties of the boards were also determined and they are previously mentioned in chapter 3. All the properties were considered as linear elastic in nature except the solder balls and the PCB. The solder balls were considered as visco-plastic and so Anand’s model was used to explain the behavior of the solder balls. The material of solder balls was taken as SAC 396 where the material composition is 95.5% Tin (Sn), 3.9% Silver (Ag) and 0.6% Copper (Cu). The Anand’s constants are given in the Table 6.1. The PCBs were taken as linear orthotropic in nature.

In the simulations, a 2.8x2.8 mm² WCSP is taken with a solder ball array of 7x7 by following the parameters seen in Figure 6.2. The array is shown in the Figure 6.3. The distance between the solder balls was 0.4 mm and the distance between the balls from one side to other is 2.4 mm.

Figure 6.1 Cross section of WCSP assembly [30]

Table 6.1 Material properties of material used in the simulations

<table>
<thead>
<tr>
<th>Material</th>
<th>CTE (ppm/°C)</th>
<th>E (Gpa)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Copper pad</td>
<td>17</td>
<td>11</td>
</tr>
<tr>
<td>Die Attach</td>
<td>33</td>
<td>10</td>
</tr>
<tr>
<td>Mold</td>
<td>20</td>
<td>24</td>
</tr>
<tr>
<td>Pi Layer</td>
<td>52</td>
<td>1.2</td>
</tr>
<tr>
<td>Solder Mask</td>
<td>30</td>
<td>4</td>
</tr>
</tbody>
</table>
Table 6.2 Anand’s Material Constants for SAC 396

<table>
<thead>
<tr>
<th>Constant</th>
<th>Name</th>
<th>Unit</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$s_0$</td>
<td>Initial Deformation Resistance</td>
<td>MPa</td>
<td>3.3</td>
</tr>
<tr>
<td>$Q/R$</td>
<td>Activation Energy/Universal Gas Constant</td>
<td>1/K</td>
<td>9883</td>
</tr>
<tr>
<td>$A$</td>
<td>Pre-exponential Factor</td>
<td>sec$^{-1}$</td>
<td>1.57E+07</td>
</tr>
<tr>
<td>$\xi$</td>
<td>Multiplier of Stress</td>
<td>Dimensionless</td>
<td>1.06</td>
</tr>
<tr>
<td>$m$</td>
<td>Strain Rate Sensitivity of Stress</td>
<td>Dimensionless</td>
<td>0.3686</td>
</tr>
<tr>
<td>$h_0$</td>
<td>Hardening/Softening Constant</td>
<td>MPa</td>
<td>1077</td>
</tr>
<tr>
<td>$\delta$</td>
<td>Coefficient of Deformation Resistance Saturation</td>
<td>MPa</td>
<td>3.15</td>
</tr>
<tr>
<td>$n$</td>
<td>Strain Rate Sensitivity of Saturation</td>
<td>Dimensionless</td>
<td>0.0352</td>
</tr>
<tr>
<td>$a$</td>
<td>Strain Rate of Sensitivity of Hardening or Softening</td>
<td>Dimensionless</td>
<td>1.6832</td>
</tr>
</tbody>
</table>

Figure 6.2 2.8x2.8 WCSP Package [31]
Figure 6.3 2.8x2.8 WCSP Package in ANSYS

Table 6.3 Package component dimensions

<table>
<thead>
<tr>
<th>Component</th>
<th>Dimensions (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package</td>
<td>2.8 x 2.8 x 0.43</td>
</tr>
<tr>
<td>Die</td>
<td>4.315 x 3.245 x 0.19</td>
</tr>
<tr>
<td>PI Layer</td>
<td>2.8 x 2.8 x 0.02</td>
</tr>
<tr>
<td>Die Attach</td>
<td>4.15 x 4.15 x 0.01</td>
</tr>
<tr>
<td>UBM</td>
<td>.07 x 0.03</td>
</tr>
<tr>
<td>Pitch</td>
<td>0.4</td>
</tr>
<tr>
<td>PCB</td>
<td>24 x 24 x 1.00</td>
</tr>
<tr>
<td></td>
<td>24 x 24 x 0.70</td>
</tr>
</tbody>
</table>
The table shows the dimensions of the components used in the simulations. As was mentioned in the literature review it is very important to mention the dimensions of the components as they influence the results and affect the behavior of the assembly as whole.

6.3 The Boundary Conditions, Meshing and the Analysis Settings

It is always better to perform the thermal cycling test experimentally, but it has to be also kept in mind that they are expensive and time consuming. There is also the factor of that many samples and boards availability. So many tends to observe the behavior computationally to save the time and money. The package assembly can be modeled and simulated and the appropriate design and material decisions can be made up to a certain extent. As mentioned before, 0.94 and 0.89 mm boards are not physically available. So performing computational analysis on them was the only way to ensure their behavior during thermal cycling tests.

The meshing used in the simulations in ANSYS 16.1 was not too complicated and this helped to reduce a lot of computational time. Mesh sizes were taken as medium but the results did not vary too much from the coarse mesh. Special meshing operations were carried out in regions where it was needed. Edge sizing was needed for very thin sections to have at least two parts in the mesh. There was also body sizing done on the solders to match the mesh of the solders with the rest of the body. Mainly hex-dominant method was used to do the meshing of the body.

For simplicity, a 1/4th model is taken. The figure shows the quarter model used in the simulations. The quarter model has symmetric conditions on both sides. A center node is provided a fixed condition, it prevents the rigid body motion.
The package assembly is subjected to the thermal cycling condition of G (-40 to 125°C) at a dwell of 15 minutes and ramp of 15 minutes which is given at JEDEC JESD22-A104-A [16]. The cycles are done in either air to air chamber or fluid to fluid chambers. There are other thermal conditions Mil-STD-883 with conditions A, B and C.
To understand the effect of creep and the frequency of the cycles, two types of cycles were used. One cycle had a small ramp time but also long dwell time. And the other cycle had a short ramp time as well as a short dwell time. The longer the dwell time, longer the creep damage in the assembly. The faster ramp time creates more damage than a slower ramp rate [17]. So two kinds of simulations considering both long and short dwell time along with short ramp time was considered. The main objective of these profiles is not the thermal shock but the effect of frequency and the creep on all the packages involved.
Figure 6.8 Thermal shock profile with small ramp and small dwell time

The Figure 6.4 shows the thermal cycle profile used in the simulation. It has three cycles in total and it has one cycle per hour. One ramp is going down and the other is going up. There are two dwells, one in the highest temperature of 125°C and the other one is in -40°C. The ramp and dwell times are 15 minutes each. The ramps are usually given as for plastic loadings and the dwell is usually to observe the creep in the assembly. During simulations, same uniform temperature is assumed throughout the package and there is no thermal gradients in the system. It is considered in this way for making the simulations simple although in reality it may not be the case. By performing the simulations, stress, strain and deformations are observed to predict the behavior of the boards.
The strain is dependent on the thermal gradient during temperature cycling. The deformation is controlled by the CTE and other material properties of the board and the package. Figure 7.1 shows the deformation that occurred in the boards over the time of the simulation along the z-direction. It shows that for the 1 mm board the deformation in the z-direction was 13 μm and for the 0.7 mm board the deformation was 22 μm. The maximum deformation occurs for the 0.7 mm board compared to the other boards. The deformation for 0.94 and 0.89 mm boards were kind of similar. According to Chung et al. slim PCB undergoes large deformation as the bending rigidity is proportional to the cube of the thickness [32]. The deformation for the 0.94 mm was higher than the 1 mm which might indicate that as a single copper layer was removed, the stiffness of the board decreased which created more deformation upon heating indicating the influence of different layers in the board properties. There is an anomaly between the 0.94 and 0.89 mm board which indicates only the bending rigidity is not the factor over here.

![Figure 7.1 Deformation profile over time](image-url)
Figure 7.2 and 7.3 shows the deformation of the 1.0 and 0.7 mm boards at 125ºC. That means the deformation in the assembly at that temperature looks like this. The maximum deformation occurs at the centre of the package which is understandable from the beam theory. We also need to keep in mind the reference temperature was taken as 25ºC for the whole assembly. So at 125, the highest difference between the reference temperature and the applied load takes place.

After removing the FR-4 the deformation was observed again. The deformation should have been higher than 0.94 mm due to reduced thickness. But instead the 0.94 mm has higher deformation than the 0.89 mm board. Again considering only the thickness is not enough to say that it will deform more than a certain thickness.
The equivalent stresses are shown and the above figure. The stress for the 0.94 mm board is the lowest among all the boards.

The normal stress again is the lowest for 0.94 mm board compared to the other boards. It is in the range of 290 MPa whereas for 1 mm it is around 318 MPa.
As we can see that the plastic work of the 0.7 mm board is the highest among all the boards. As was previously discussed, plastic work needed to be lower for better life reliability. Hossain et al. has also mentioned minimizing plastic work is important to improve the fatigue life [33].

Now if we look at the thermal shock with two different dwell time we will see the following results.
Figure 7.8 Normal Stress with different dwell time

There is not much difference between the longer dwell time and the shorter one, might be because the ramp rate is kept constant. The dwell time would have affected if the thermal cycles was continued for a long time.

As was previously discussed, the fatigue fracture occurs due to shear developed in the region.

Figure 7.9 Maximum Shear strain in 0.94 mm board
As we can see from the experimental results, the crack starts from the top of the solder ball or the region connected to the package side. And the shear strain is also maximum at that region as seen from the computational analysis.
To see the effect of a single parameter, CTE and young’s modulus were changed to see how the stress behavior of the board changes. Since the 0.7 mm board behaves the worst, the CTE of the board were increased from its original value and the young’s modulus were kept constant. On the other hand, the young’s modulus were increased and the CTE was kept constant. That is, only one parameter was changed at a time and all the other material properties were kept constant.

Figure 8.1 Normal Stress with changing CTE

It is seen that the normal stresses keep on increasing with constant young’s modulus up to a point. Then it starts decreasing again. Higher the modulus, higher the stress at the beginning. For young’s modulus of 22 GPa, the stresses are high compared to others in the beginning. But the transition of stresses getting lower is earlier for 22 GPa than the others. The stresses for 22 GPa also come down at a higher rate.
By keeping CTE constant but changing the young’s modulus we see the stresses keep on rising. That means, not much effect it has on the stresses other than the fact that the stresses keep on rising with rising modulus.

Figure 8.2 Normal Stress with changing Young’s Modulus
Chapter 9

CONCLUSION

9.1 Summary and Conclusion

A 3D finite element model of WCSP was taken and evaluated to study how changing the layer of the PCBs affected the whole assembly. At first all the material properties were determined using TMA and UTM. The material properties were then given as inputs to the model in ANSYS. And finally the results were evaluated to give a better understanding of the boards.

Anand’s viscoplastic constants were given to the solder ball of SAC 396 and the boards were considered orthotropic in nature. These made a huge impact on the analysis as the thermal cycle goes on for a certain amount of time and the orthotropic nature of the boards gave results in all directions. The assembly was put under thermal cycling and shock to see the effect of dwell and ramp along with normal thermal cycling. It was seen that the CTE of the 0.7 mm board in the z-direction was very low compared to the other boards. It also had the highest stress generation. This indicates that only changing the thickness will not ensure better reliability. The material properties are also needed to be kept in mind. The plastic work generated in 0.7 mm is also higher than other boards. 0.94 mm board had the best behavior under all conditions.

Table 9.1 Drop Test Results

<table>
<thead>
<tr>
<th>Boards</th>
<th>Peel Stress (MPa)</th>
<th>Density (Kg/m³)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 mm</td>
<td>656.98</td>
<td>2428.99</td>
</tr>
<tr>
<td>0.94 mm</td>
<td>593.33</td>
<td>2365.32</td>
</tr>
<tr>
<td>0.89 mm</td>
<td>657.47</td>
<td>2330.1</td>
</tr>
<tr>
<td>0.7 mm</td>
<td>716.19</td>
<td>2670.7</td>
</tr>
</tbody>
</table>
If we look at the drop test results, we can also see that 0.7 mm board behaves worse than the other boards and the interesting fact is the density of the board is also higher than the other boards. This might affect other material properties relevant to thermal cycling.

If we look at the two boards we will observe that the thicker board has more evenly distributed core than the 0.7 mm board. That means the copper layers are more evenly distributed in 1 mm. The anomalies in 0.7 mm board are seen in the properties. The 0.7 mm board is highly dense and even if densities are not put into the thermal cycling simulations, it does affect other properties.

9.2 Future Work

There are many ways this study can be approved further. As it was seen that just by changing one parameter is not enough to judge the real reason of failure of the 0.7 mm board. Three or four point bend test can be done on the boards to measure the flexural stress. This can help us to understand how bending is affected by the thickness and how much it correlates with the thermal cycling warpage. The combined effect of tension/compressive loading with temperature can also be conducted to see the combined effect of both these loads. This will help us to understand the behavior of the board as we know the young’s modulus changes with temperature. We can try to pin point the effect of each changing temperature and maybe understand the behavior of the boards as they go through the temperature cycling.

We can also try to see the effect of cracks on the solder joints during thermal cycles. No components are perfectly made. How the cracks which are already present may affect the stress/strain generation and how they differ from the perfect solder balls can be
compared. The results can also be varied by putting the cracks in different positions and how changing the crack positions affect the results can also be observed.

Figure 9.1 Cracks at different positions of the solder balls
REFERENCES


[29] Sumitomo Bakelit Co. Ltd., "Sumilite APL-4901 Resin Coated Copper Foils".


BIOGRAPHICAL STATEMENT

Trina Barua received her Bachelor’s degree in Mechanical Engineering from the Bangladesh University of Engineering and Technology in the year 2012. She then decided to work for Ahsanullah University of Science and Technology, Dhaka as a Lecturer for more than a year, from 2012 to 2013. She then decided to pursue her Master’s in Mechanical Engineering in the University of Texas at Arlington in Spring 14. She joined the Electronics MEMS and Nanoelectronics Systems Packaging Center (EMNSPC) and started working as a Research Assistant. She has been actively involved in the research and her interest was reliability, material characterization, simulation and crack propagation. She also trained and motivated new members joining the group. During her time, she was an integral part of the SRC funded project with Texas Instruments and closely worked with them. Upon graduation, Trina plans to pursue her career in the direction where her experience and expertise are utilized.