PARAMETRIC STUDY OF AN IGBT COLD PLATE AND AFFECT OF DEVICE LEVEL MODELLING ON SYSTEM LEVEL THERMAL PREDICTIONS

by

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To my father Nagaraja Urs, and mother Mahalakshmi R, and my sister Pallavi S and my brother in law Satish C

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Abstract

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ABHISHEK RAJ URS K N, M.S.

The University of Texas at Arlington, 2016

Supervising Professor: Dereje Agonafer

In power electronics, as there is continuous increase in performance of the electronic devices, simultaneously the size of the components used in these devices keep on decreasing. This has resulted in increased power densities and the requirements for excellent cooling as well in order to avoid the failure of those devices. Traditionally, while designing a cooling system for a device, uniform heat flux is assumed throughout the components. In many cases this method may not be accurate for a particular model design. There are chances that the heat flux distribution around the components are non-uniform and requires a more accurate device level modelling and analysis of the system.

Since the technology is continuously improving with high power, high density electronics, it is necessary to understand the thermal stack up of the component system to avoid thermal failures. The work presented highlights the affect of device level modelling of a semi-conductor device used in power electronics. Detailed thermal analysis considering uniform flux and device level model have been performed on an Insulated Gate Bi-Polar Transistor [IGBT].

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Chapter 1

Introduction to Power Electronics

Power electronics is a branch of electronic and electrical engineering which deals with the design, control, computation and integration of nonlinear, time varying energy processing electronic systems with fast dynamics. Some of these devices are used as power conversion units. These devices can mostly found in consumer electronics like home electronics and also industrial drives, telecommunication, transport etc. Power range of these devices may vary from tens of watts to server hundred Watts. Few examples of power electronics devices include Diode, Thyristor, Bi-polar junction transistor [BJT], Power MOSFET, and Insulated Gate Bi-polar Transistor [IGBT].

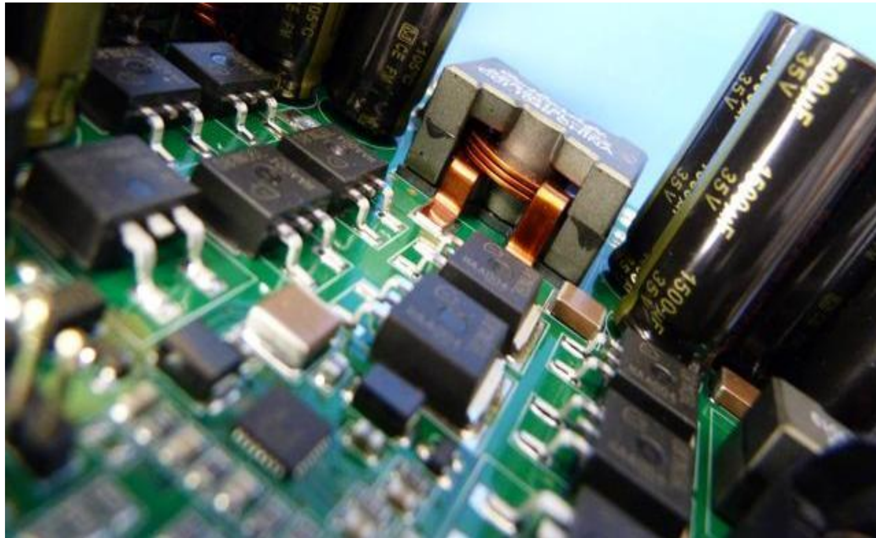


Figure 1-1 Power Electronics

Insulated Gate Bi-polar Transistor is a 3 terminal power semiconductor device which is used in switching electric signal applications. It is very highly efficient and has very high switching speeds. It is basically a combination of MOSFET and a BJT.

Chapter 2

Insulated Gate Bi-Polar Transistor

Introduction

The introduction of Power MOSFET was originally regarded as a major threat to the power bipolar transistor. However, initial claims of infinite current gain for the power MOSFETs were diluted by the need to design the gate drive circuit capable of supplying the charging and discharging current of the device input capacitance. This is especially true in high frequency circuits where the power MOSFET is particularly valuable due to its inherently high switching speed. On the other hand, MOSFETs have a higher on state resistance per unit area and consequently higher on state loss. This is particularly true for higher voltage devices (greater than about 500 volts) which restricted the use of MOSFETs to low voltage high frequency circuits (eg. SMPS). [3]

With the discovery that power MOSFETs were not in a strong position to displace the BJT, many researches began to look at the possibility of combining these technologies to achieve a hybrid device which has a high input impedance and a low on state resistance. The obvious first step was to drive an output NPN BJT with an input MOSFET connected in the Darlington configuration. However, this approach required the use of a high voltage power MOSFET with considerable current carrying capacity (due to low current gain of the output transistor). Also, since no path for negative base current exists for the output transistor, its turn off time also tends to get somewhat larger. An alternative hybrid approach was investigated at GE Research center where a MOS gate structures was used to trigger the latch up of a four layer Thyristor. However, this device

was also not a true replacement of a BJT since gate control was lost once the Thyristor latched up. [3]

After several such attempts it was concluded that for better results MOSFET and BJT technologies are to be integrated at the cell level. This was achieved by the GE Research Laboratory by the introduction of the device IGT and by the RCA research laboratory with the device COMFET. The IGT device has undergone many improvement cycles to result in the modern Insulated Gate Bipolar Transistor (IGBT). These devices have near ideal characteristics for high voltage (> 100V) medium frequency (<20 kHz) applications. This device along with the MOSFET (at low voltage high frequency applications) have the potential to replace the BJT completely. [3]

Constructional features of an IGBT

Vertical cross section of a channel IGBT cell is shown in Fig 2-1. Although p channel IGBTs are possible n channel devices are more common

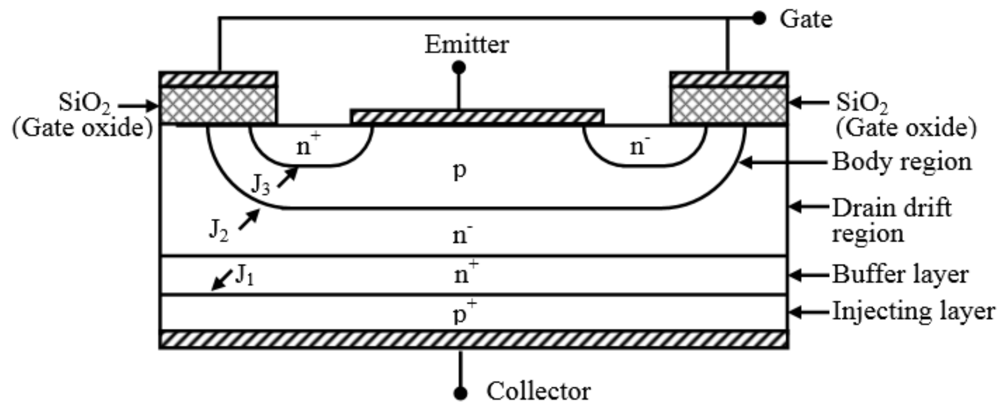


Figure 2-1 IGBT Cell

The major difference with the corresponding MOSFET cell structure lies in the addition of a p+ injecting layer. This layer forms a p-n junction with the drain layer and injects minority carriers into it. The n type drain layer itself may have two different doping levels. The lightly doped n- region is called the drain drift region. Doping level and width of this layer sets the forward blocking voltage (determined by the reverse break down voltage of J2) of the device. However, it does not affect the on state voltage drop of the device due to conductivity modulation as discussed in connection with the power diode. This construction of the device is called “Punch Trough” (PT) design. The Non-Punch through (NPT) construction does not have this added n+ buffer layer. The PT construction does offer lower on state voltage drop compared to the NPT construction particularly for lower voltage rated devices. However, it does so at the cost of lower reverse break down voltage for the device, since the reverse break down voltage of the junction J1 is small. The rest of the construction of the device is very similar to that of a vertical MOSFET including the insulated gate structure and the shorted body (p type) – emitter (n+ type) structure. The doping level and physical geometry of the p type body region however, is considerably different from that of a MOSFET in order to defeat the latch up action of a parasitic Thyristor embedded in the IGBT structure. A large number of basic cells as shown in Fig 2-1 are grown on a single silicon wafer and connected in parallel to form a complete IGBT device. [3]

The IGBT cell has a parasitic p-n-p-n Thyristor structure embedded into it as shown in Fig 2.2(a). The constituent p-n-p transistor, n-p-n transistor and the driver MOSFET are shown by dotted lines in this figure. Important resistances in the current flow path are also indicated. [3]

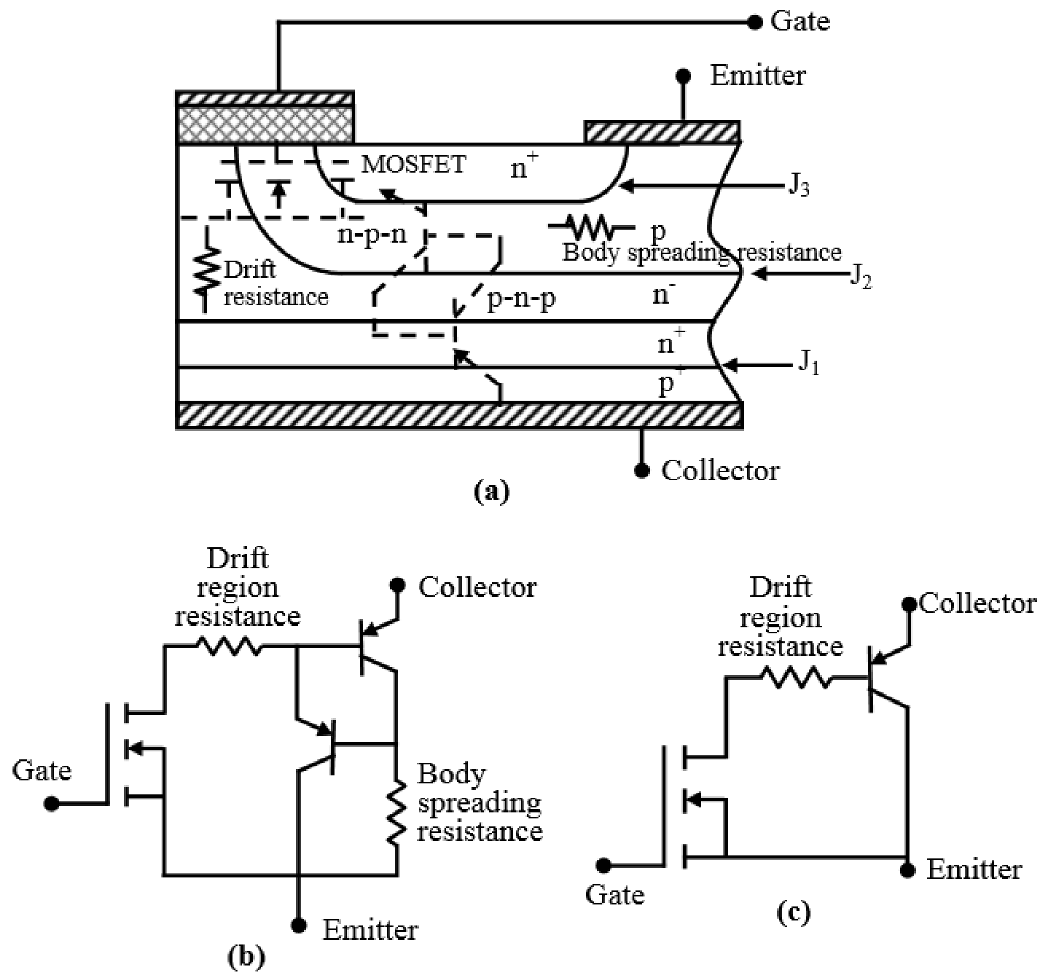


Figure 2-2 Parasitic Thyristor in an IGBT cell. (a) Schematic structure (b) Exact equivalent circuit. (c) Approximate equivalent circuit.

Fig 2.2(b) shows the exact static equivalent circuit of the IGBT cell structure. The top p-n-p transistor is formed by the p+ injecting layer as the emitter, the n type drain layer as the base and the p type body layer as the collector. The lower n-p-n transistor has the n+ type source, the p type body and the n type drain as the emitter, base and collector respectively. The base of the lower n-p-n transistor is shorted to the emitter by

the emitter metallization. However, due to imperfect shorting, the exact equivalent circuit of the IGBT includes the body spreading resistance between the base and the emitter of the lower n-p-n transistor. If the output current is large enough, the voltage drop across this resistance may forward bias the lower n-p-n transistor and initiate the latch up process of the p-n-p-n Thyristor structure. Once this structure latches up the gate control of IGBT is lost and the device is destroyed due to excessive power loss. [3]

A major effort in the development of IGBT has been towards prevention of latch up of the parasitic Thyristor. This has been achieved by modifying the doping level and physical geometry of the body region. The modern IGBT is latch-up proof for all practical purpose. [3]

Operating principle of an IGBT

Operating principle of an IGBT can be explained in terms of the schematic cell structure and equivalent circuit of Fig 2.2(a) and (c). From the input side the IGBT behaves essentially as a MOSFET. Therefore, when the gate emitter voltage is less than the threshold voltage no inversion layer is formed in the p type body region and the device is in the off state. The forward voltage applied between the collector and the emitter drops almost entirely across the junction J2. Very small leakage current flows through the device under this condition. In terms of the equivalent current of Fig 2.2(c), when the gate emitter voltage is lower than the threshold voltage the driving MOSFET of the Darlington configuration remains off and hence the output p-n-p transistor also remains off. [3]

When the gate emitter voltage exceeds the threshold, an inversion layer forms in the p type body region under the gate. This inversion layer (channel) shorts the emitter and the drain drift layer and an electron current flows from the emitter through this

channel to the drain drift region. This in turn causes substantial whole injection from the p+ type collector to the drain drift region. A portion of these holes recombine with the electrons arriving at the drain drift region through the channel. The rest of the holes cross the drift region to reach the p type body where they are collected by the source metallization. [3]

From the above discussion it is clear that the n type drain drift region acts as the base of the output p-n-p transistor. The doping level and the thickness of this layer determines the current gain "∝" of the p-n-p transistor. This is intentionally kept low so that most of the device current flows through the MOSFET and not the output p-n-p transistor collector. This helps to reduce the voltage drop across the "body" spreading resistance shown in Fig 2.2 (b) and eliminate the possibility of static latch up of the IGBT.

The total on state voltage drop across a conducting IGBT has three components. The voltage drop across J1 follows the usual exponential law of a pn junction. The next component of the voltage drop is due to the drain drift region resistance. This component in an IGBT is considerably lower compared to a MOSFET due to strong conductivity modulation by the injected minority carriers from the collector. This is the main reason for reduced voltage drop across an IGBT compared to an equivalent MOSFET. The last component of the voltage drop across an IGBT is due to the channel resistance and its magnitude is equal to that of a comparable MOSFET. [3]

Steady state characteristics of an IGBT

The i-v characteristics of an n channel IGBT is shown in Fig 2.3 (a). They appear qualitatively similar to those of a logic level BJT except that the controlling parameter is not a base current but the gate-emitter voltage [3]

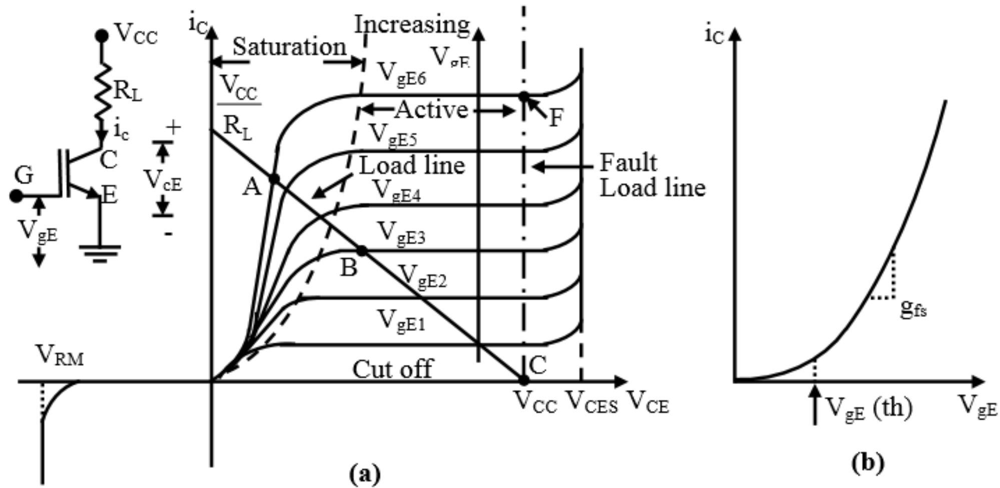


Figure 2-3 Static characteristics of an IGBT (a) Output characteristics (b) Transfer characteristics.

When the gate emitter voltage is below the threshold voltage only a very small leakage current flows though the device while the collector emitter voltage almost equals the supply voltage (point C in Fig 2.3(a)). The device, under this condition is said to be operating in the cut off region. The maximum forward voltage the device can withstand in this mode (marked VCES in Fig 2.3(a)) is determined by the avalanche break down voltage of the body – drain p-n junction. Unlike a BJT, however, this break down voltage is independent of the collector current as shown in Fig 2.3(a). IGBTs of Non-punch through design can block a maximum reverse voltage (VRM) equal to VCES in the cut off mode. However, for Punch through IGBTs VRM is negligible (only a few tens of volts) due the presence of the heavily doped n+ drain buffer layer. [3]

As the gate emitter voltage increases beyond the threshold voltage the IGBT enters into the active region of operation. In this mode, the collector current ic is

determined by the transfer characteristics of the device as shown in Fig 2.3(b). This characteristic is qualitatively similar to that of a power MOSFET and is reasonably linear over most of the collector current range. The ratio of ic to (VgE – vgE (th)) is called the forward trans conductance (gfs) of the device and is an important parameter in the gate drive circuit design. The collector emitter voltage, on the other hand, is determined by the external load line ABC as shown in Fig 2.3(a). [3]

As the gate emitter voltage is increased further ic also increases and for a given load resistance (RL) vCE decreases. At one point vCE becomes less than vgE – vgE (th). Under this condition the driving MOSFET part of the IGBT (Fig 7.2(c)) enters into the ohmic region and drives the output p-n-p transistor to saturation. Under this condition the device is said to be in the saturation mode. In the saturation mode the voltage drop across the IGBT remains almost constant reducing only slightly with increasing vgE. [3]

In power electronic applications an IGBT is operated either in the cut off or in the saturation region of the output characteristics. Since vCE decreases with increasing vgE, it is desirable to use the maximum permissible value of vgE in the ON state of the device. vgE (Max) is limited by the maximum collector current that should be permitted to flow in the IGBT as dictated by the “latch-up” condition discussed earlier. Limiting VgE also helps to limit the fault current through the device. If a short circuit fault occurs in the load resistance RL (shown in the inset of Fig 2.3(a)) the fault load line is given by CF. Limiting vgE to vgE6 restricts the fault current corresponding to the operating point F. Most IGBTs are designed to with stand this fault current for a few microseconds within which the device must be turned off to prevent destruction of the device. [3]

It is interesting to note that an IGBT does not exhibit a BJT-like second break down failure. Since, in an IGBT most of the collector current flows through the drive MOSFET with positive temperature coefficient the effective temperature coefficient of

v_{CE} in an IGBT is slightly positive. This helps to prevent second break down failure of the device and also facilitates paralleling of IGBTs. [3]

Chapter 3

Model Overview

IGBT Chip

The IGBT module was modelled in Solid Works software platform. Initially the design only consisted of a module with only a single IGBT chip. Later, the model was changed to a module that consisted of 3 individual IGBT chips. These individual IGBT chips produced a power of 50 Watts. The module is mounted on a cold plate which removes the heat generated by the semiconductor device. Fig 3-1 shows the IGBT chip.

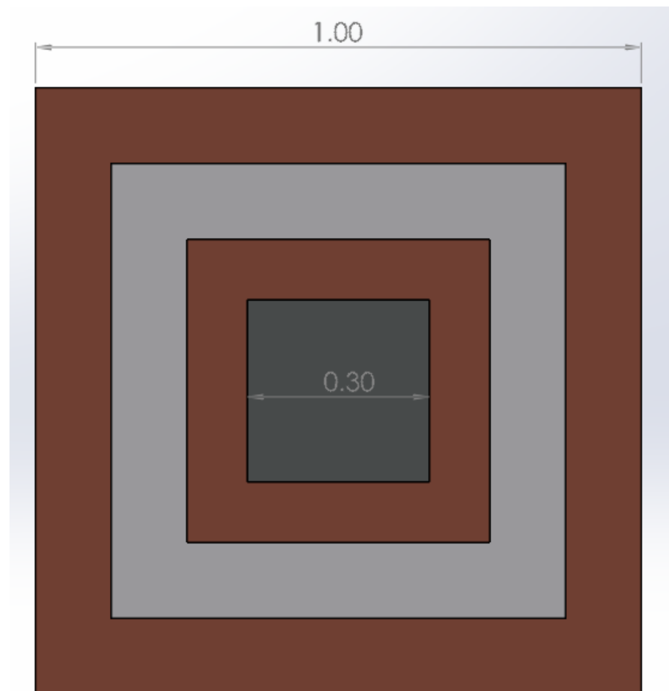
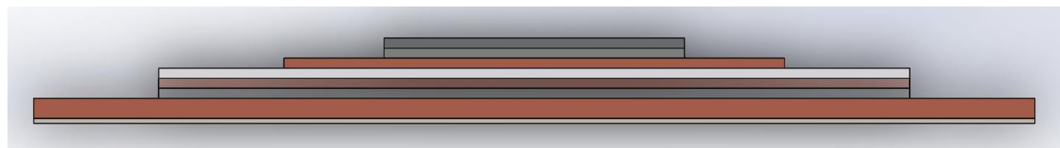


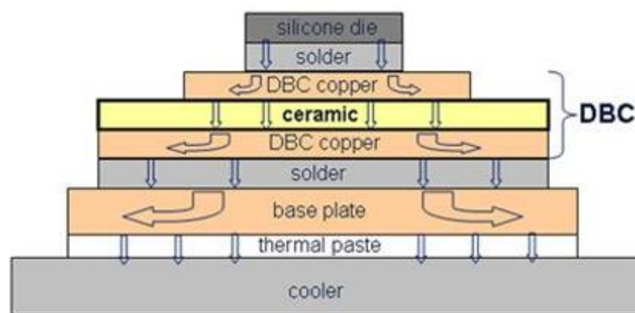
Figure 3-1 IGBT Chip.

The IGBT chips are usually made of different materials. Hence it is necessary to model the device considering different layers the heat passes through. The thermal stack

up of the IGBT chips is shown in the fig 3-2(b). Each individual layer of this device has an important role in the overall working of the module. Thermal analysis of these devices requires a proper understanding of the heat flow pattern through all the layers in order to predict the thermal stresses and failures limits and temperatures.



(a)



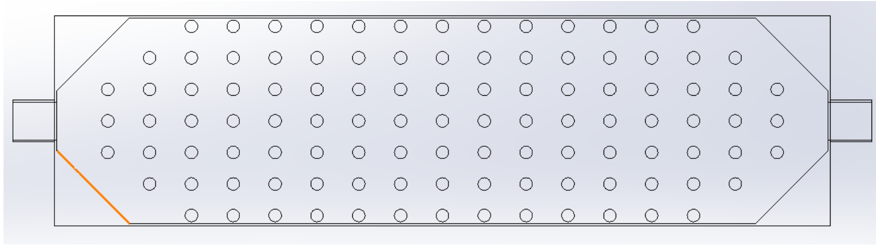
(b)

Figure 3-2 (a) IGBT Model C/S (b) IGBT Stack up.

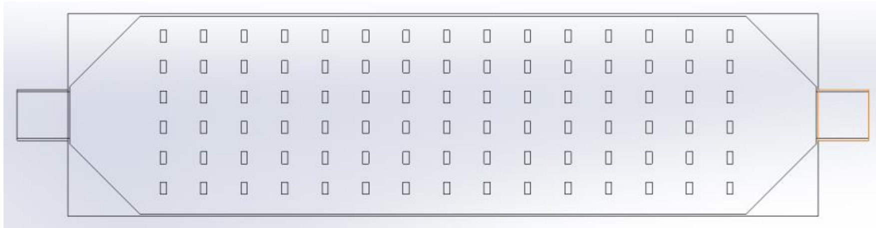
These power electronic devices can produce power range up to 1000 W/cm². Since thermal analysis can predict the effectiveness of an electronic system, it is very important to study the system before production.

Cold Plate

Cold plates are usually used to remove the excess heat generated in electronic devices.



(a)



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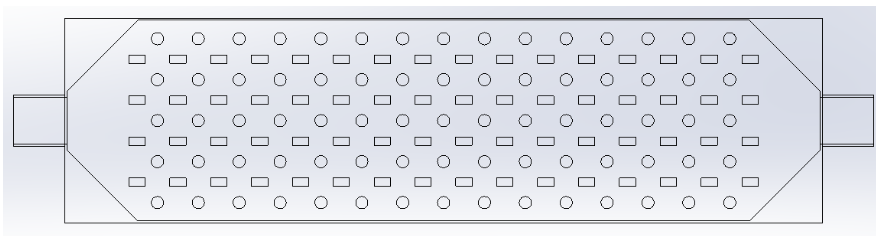

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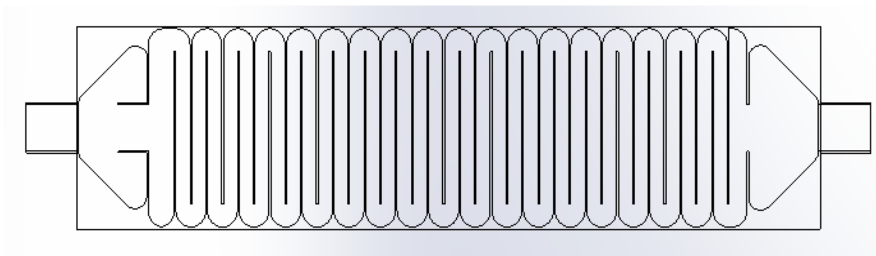


(d)

Figure 3-3 (a) Cold plate with circular pins (b) Cold plate with rectangular pins (c) Cold plate with combined pins (d) Serpentine flow cold plate.

There are different types of cold plates and are used according to the design and requirements of the electronic device. A coolant fluid is usually used in cold plate to remove the heat. Different kinds of fluids can be used based on the system application requirements.

Four types of cold plates are modeled in this application to check the affect of device modeling. The dimensions of all the cold plates are the same. They only differ by the pins/ fins used inside to remove the excess heat. Different kinds of cold plate models implemented are shown in fig 3-3.

Pins/Fins dimensions in the cold plate are altered to study the affect of the parameters. Similar tests are conducted on all the cold plate models. The cold plates used in this study are 3.7 inch in length and 1 inch in width. The cold plate models used in this application can cool an IGBT module consisting of 3 IGBT chips. The IGBT chips are mounted on the cold plate in series with each other. Fig 3-4 shows the cold plate model with the IGBT module mounted on it. The cold plate models are designed in Solid Works platform as well.

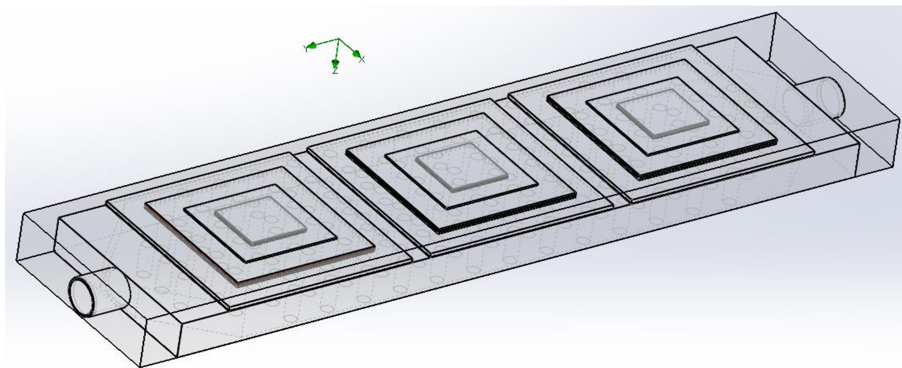


Figure 3-4 Circular pin cold plate with IGBT module.

Parametric Study of an IGBT Cold Plate

Parametric study is basically the study of effect of different parameters on the system. When designing a system it is crucial to understand the effect of all the parameters to predict the working limits of the system. A lot can change during the process and its easy to fix the problem by understanding the cause for the problem. In thermal analysis when we understand the effect of different working fluids, working temperatures, environmental conditions, we can predict thermal failures and design a system free of errors.

Different parameters used in this study are pin dimensions which include pin length, pin thickness, coolant fluid used to remove the heat from the cold plate, and material of the cold plate. Many other parameters can also be considered like fluid inlet temperature, varying the length of the cold plate, spacing and pattern of the pins/fins used in the cold plate, mass flow rate of the coolant fluid.

Parametric study is all about varying different values of the parameters and recording the values to further compare them with each other to design an optimum model.

Models were designed in solid works platform. All the models are then used in the CFD analysis to obtain results for comparison.

CFD Modelling

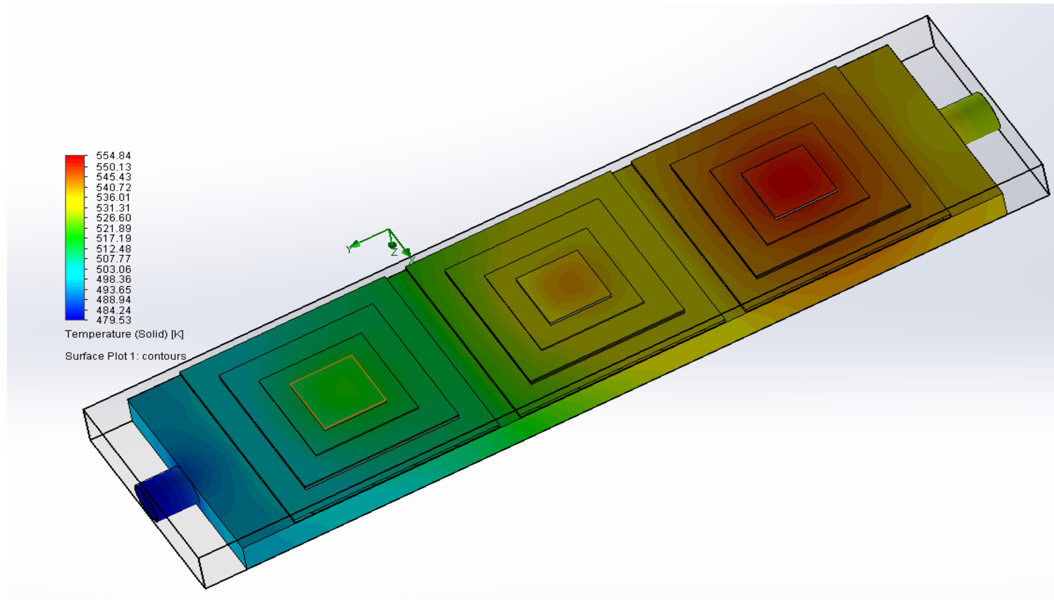
Computational Fluid Dynamics, more often abbreviated as CFD, is a branch of fluid dynamics tool that uses Finite Difference Method (FDM), Finite Element Method (FEM) and Finite Variable Method (FVM) to solve, analyze and predict complex fluid

flows. Computers are used to simulate the physics and predict time dependent results given with initial boundary conditions. [2]

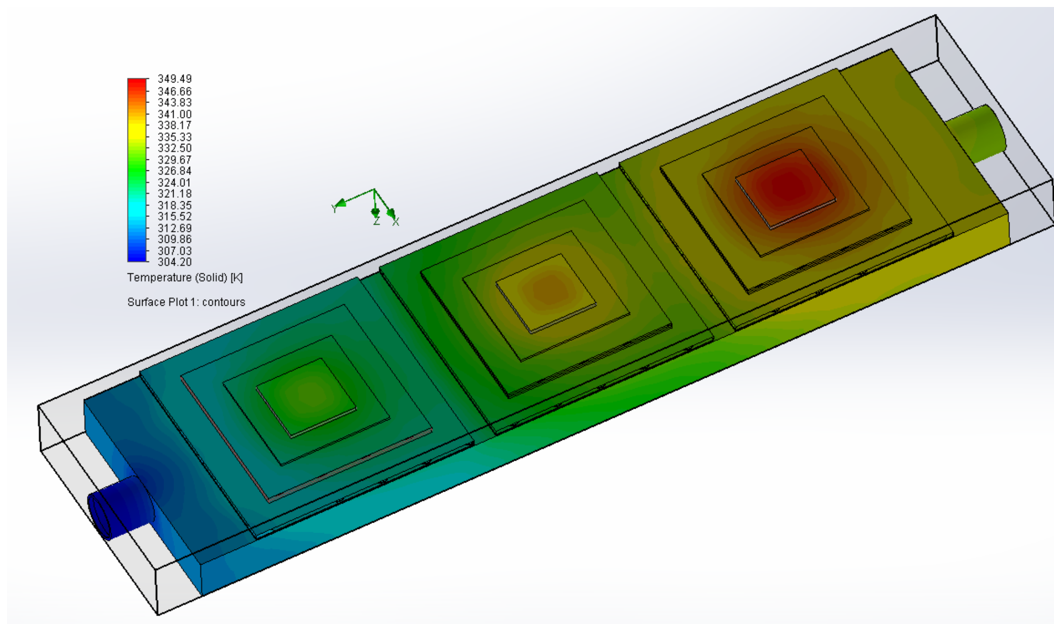
However, it seems logical to use CFD as robust and dynamic tool to model data center environments as it gained immense popularity to model cooling effectiveness within racks and aisles. It provides a 3-D analysis of hot and cold air movement within the cold plate and identify hot spots or regions that require additional cooling or areas that are excessively cooled. CFD allows the customer to predict cooling power required for his application. [2]

Although CFD is used to analyze and design thermal air flow in data centers, there is indecisiveness with respect to accuracy of thermal predictions for large data centers. CFD modeling uses computer calculations to simulate the interactions of liquids and gases with various surfaces in a defined space. [1]

Parametric Study: Coolant Study

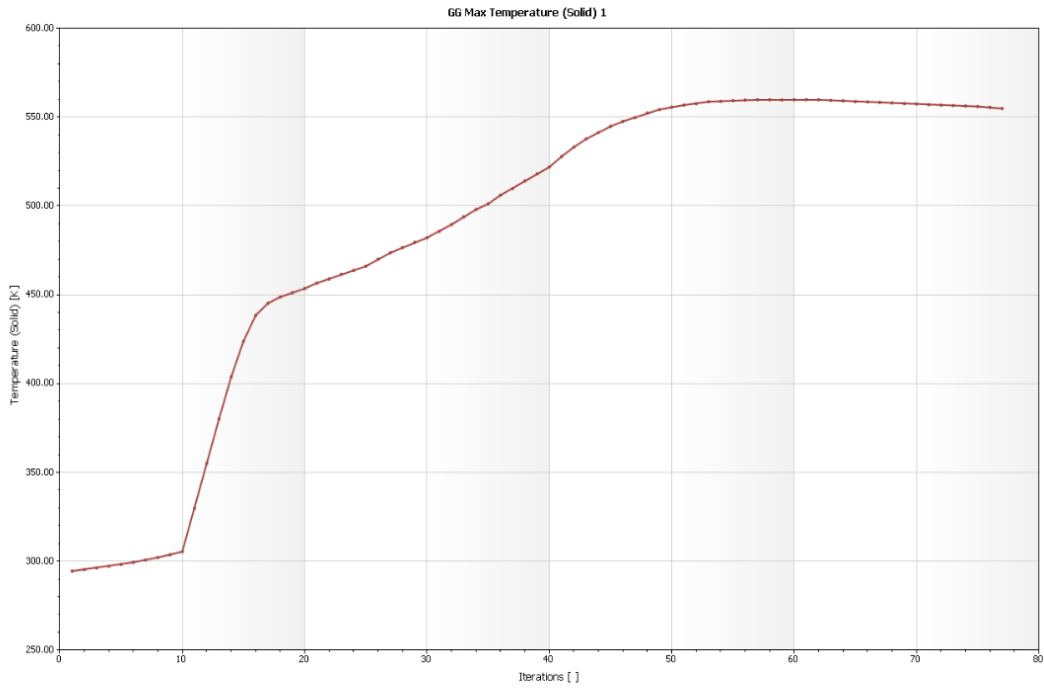


(a)



(b)

Figure 3-5 (a) CFD with Air as coolant fluid (b) CFD with Water as coolant



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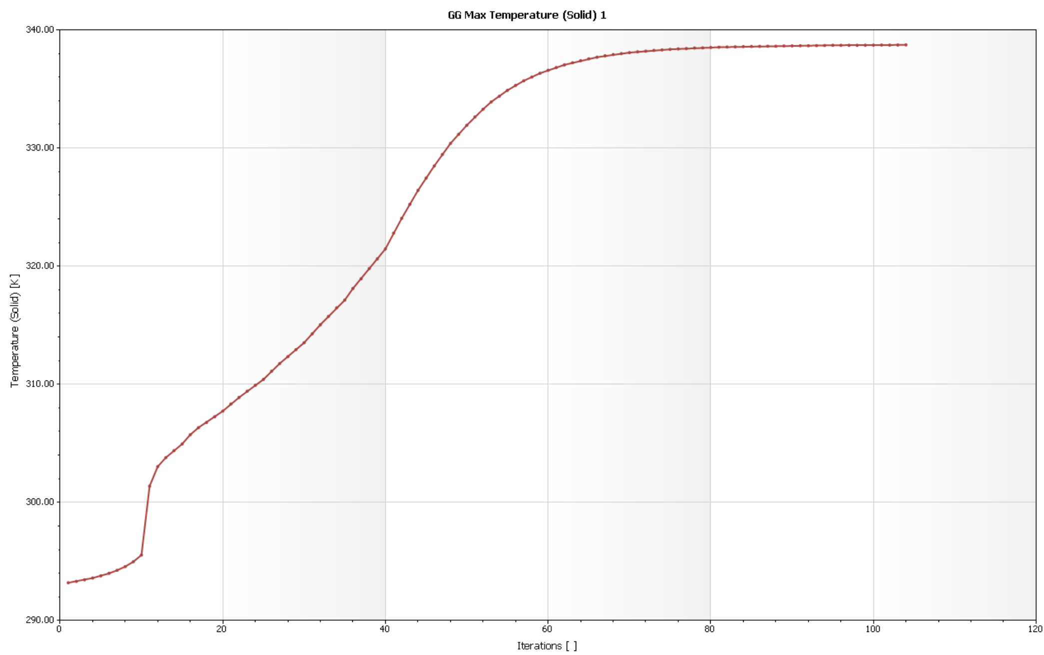
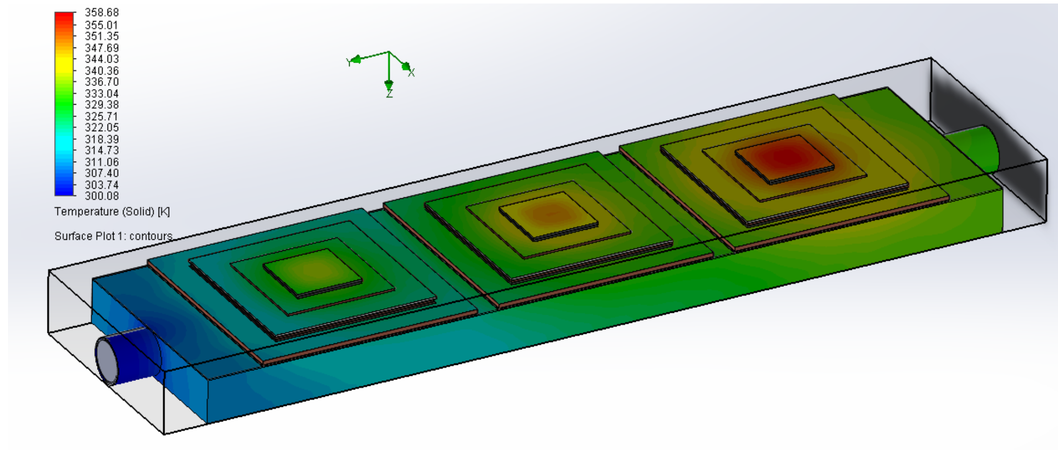


(b)

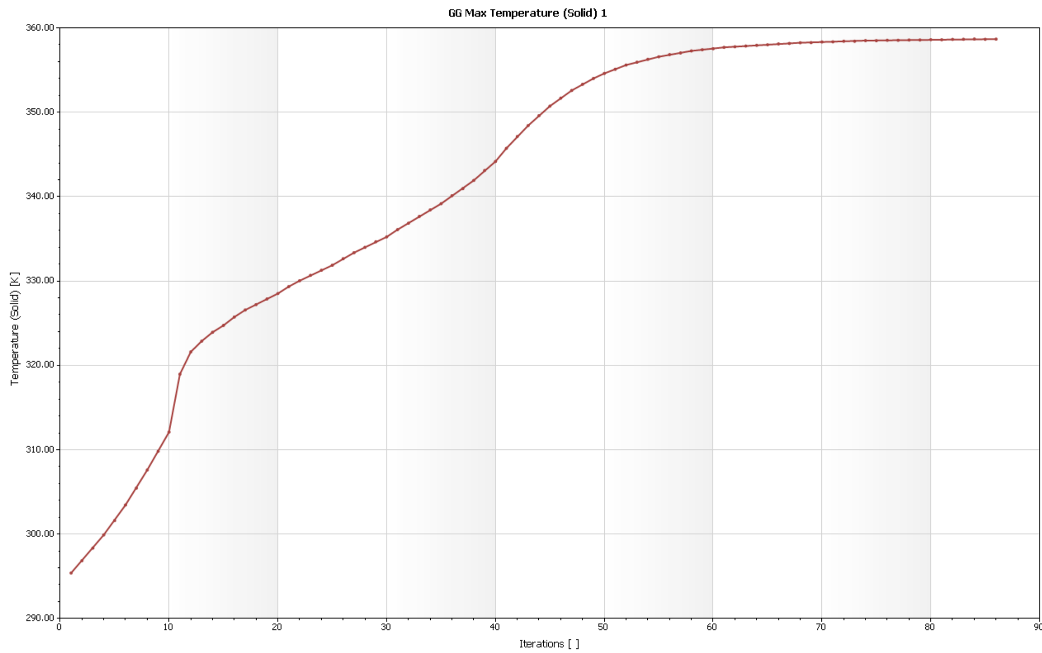
Figure 3-6 Max Temp plot of cold plate for coolant fluid (a) Air (b) Water

Parametric Study: Cold Plate Material

Material: Aluminum



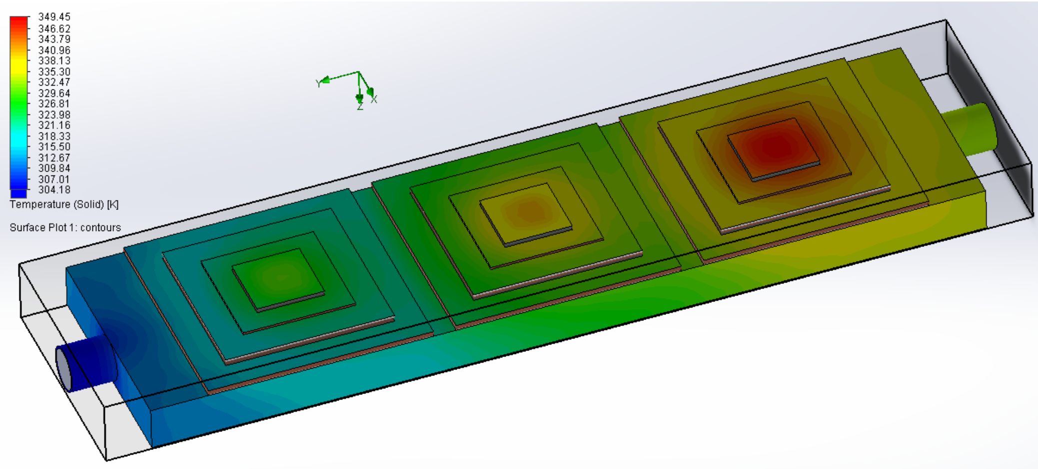
(a)



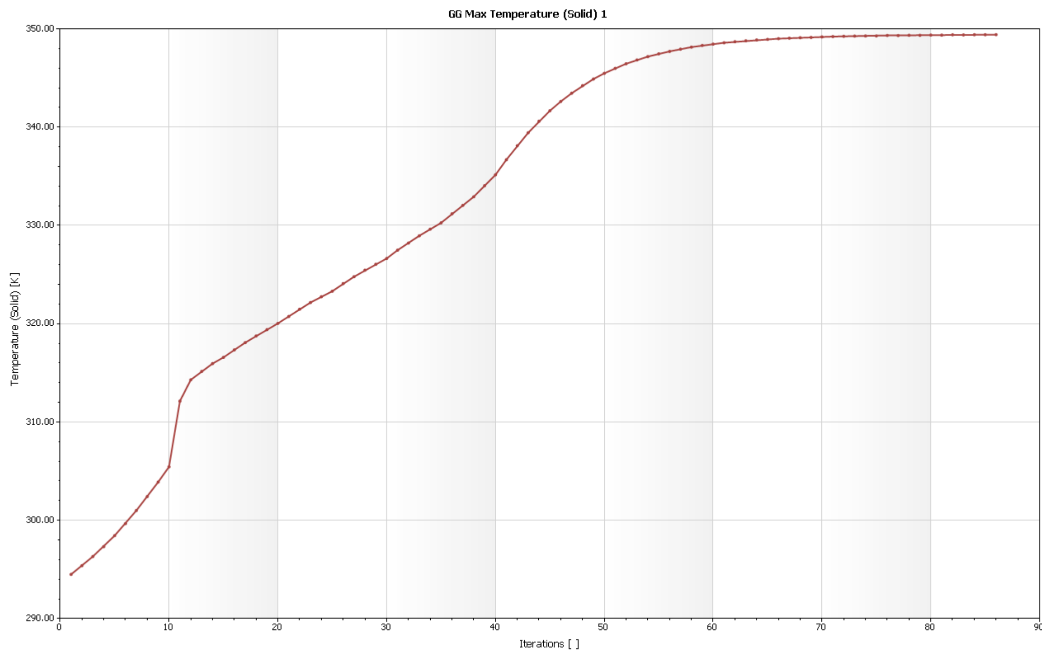
(b)

Figure 3-7 (a) CFD simulation of aluminum cold plate (b) Max Temp plot of aluminum cold plate

Material: Copper



(a)

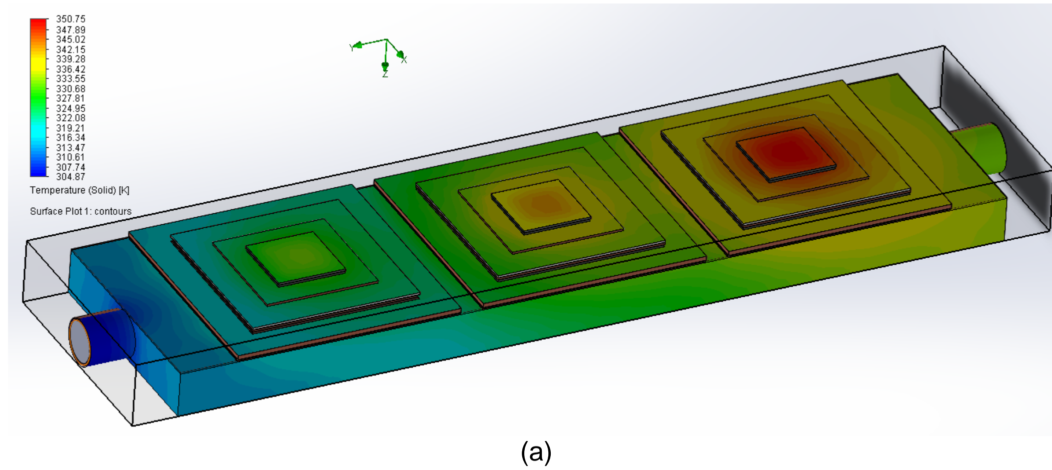


(b)

Figure 3-8 (a) CFD simulation of copper cold plate (b) Max Temp plot of copper cold plate

Parametric Study: Pin/Fin Thickness

Pin Thickness: 0.025 inch



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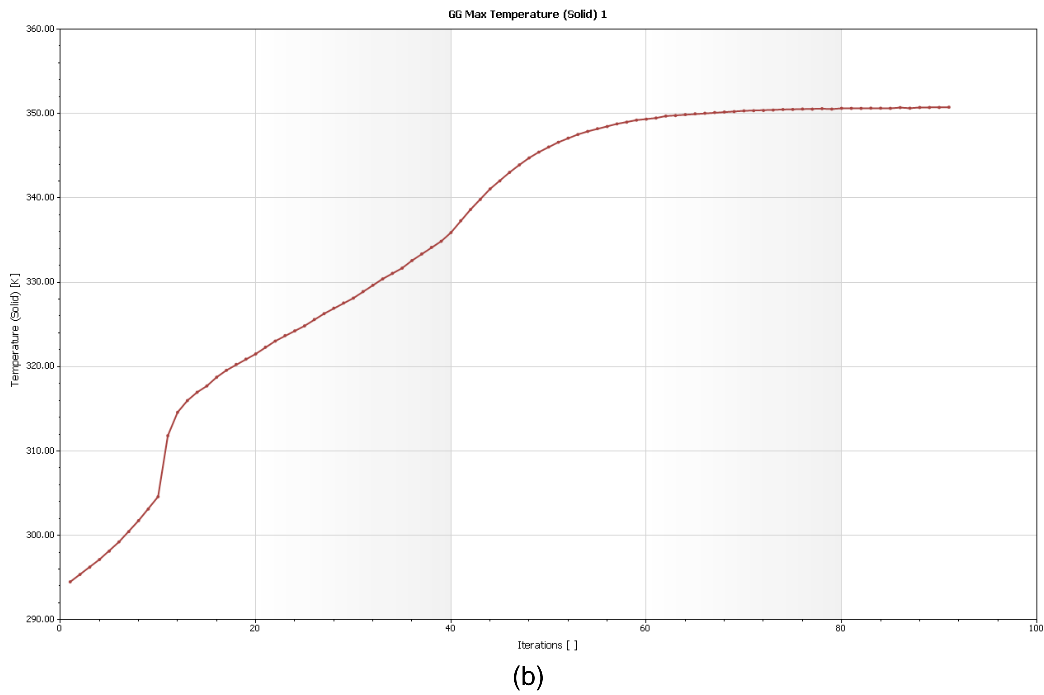
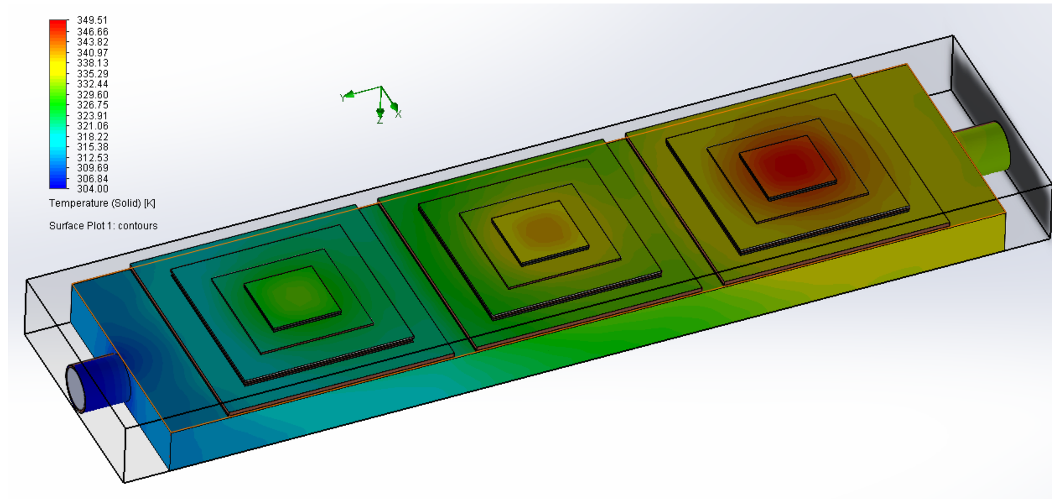


(b)

Figure 3-9 (a) CFD simulation of cold plate with pin/fin thickness of 0.025 inch (b) Max Temp plot of 0.025 inch pin thickness cold plate

Pin Thickness: 0.030 inch



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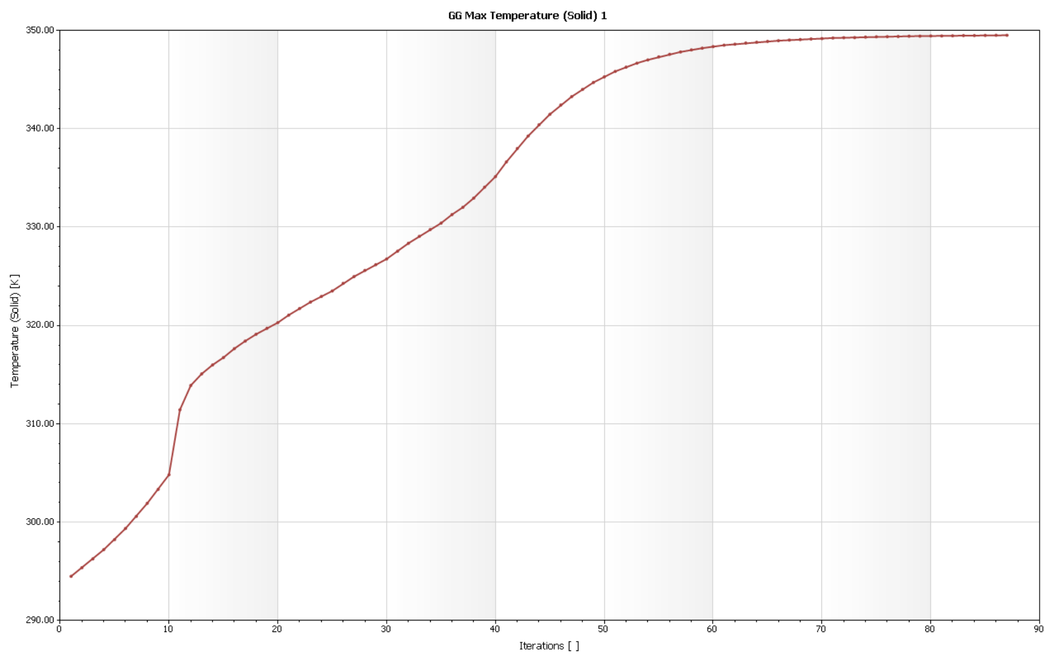
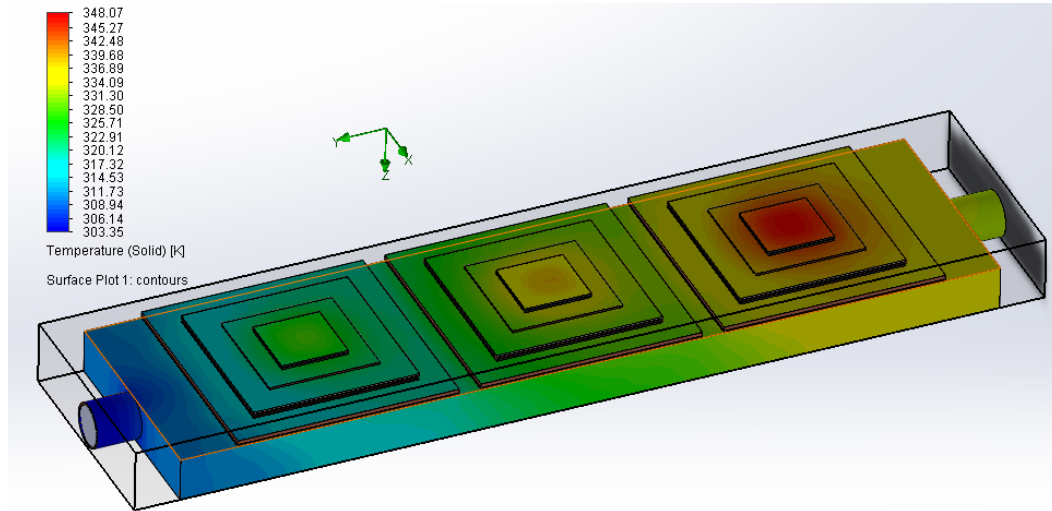


(b)

Figure 3-10 (a) CFD simulation of cold plate with pin/fin thickness of 0.030 inch (b) Max Temp plot of 0.030 inch pin thickness cold plate

Pin Thickness: 0.035 inch



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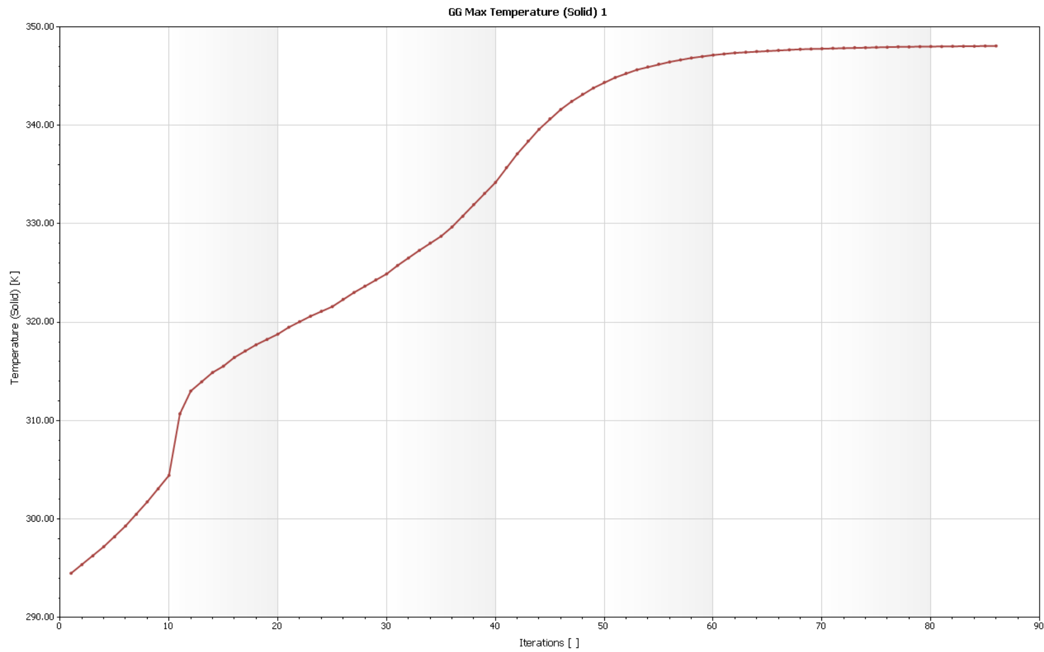
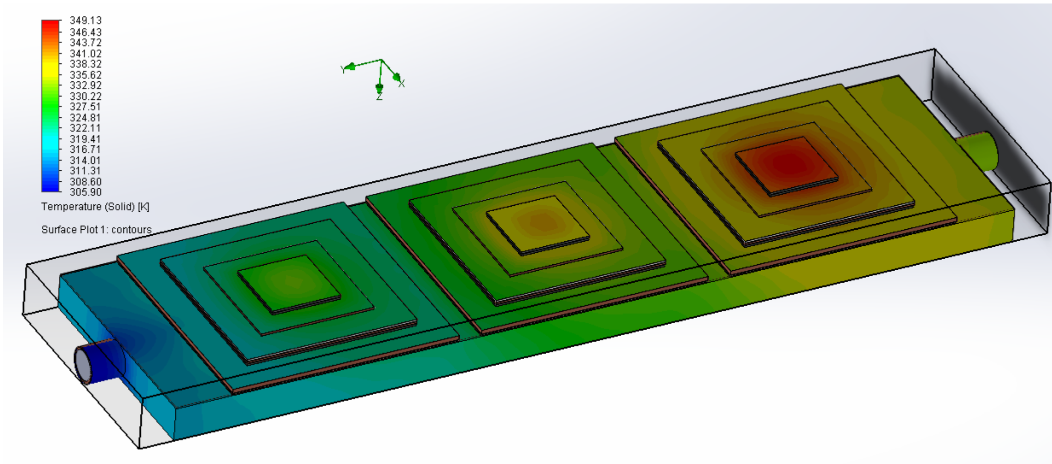


(b)

Figure 3-11 (a) CFD simulation of cold plate with pin/fin thickness of 0.035 inch (b) Max Temp plot of 0.035 inch pin thickness cold plate

Parametric Study: Pin/Fin Length

Pin length: 0.15 inch



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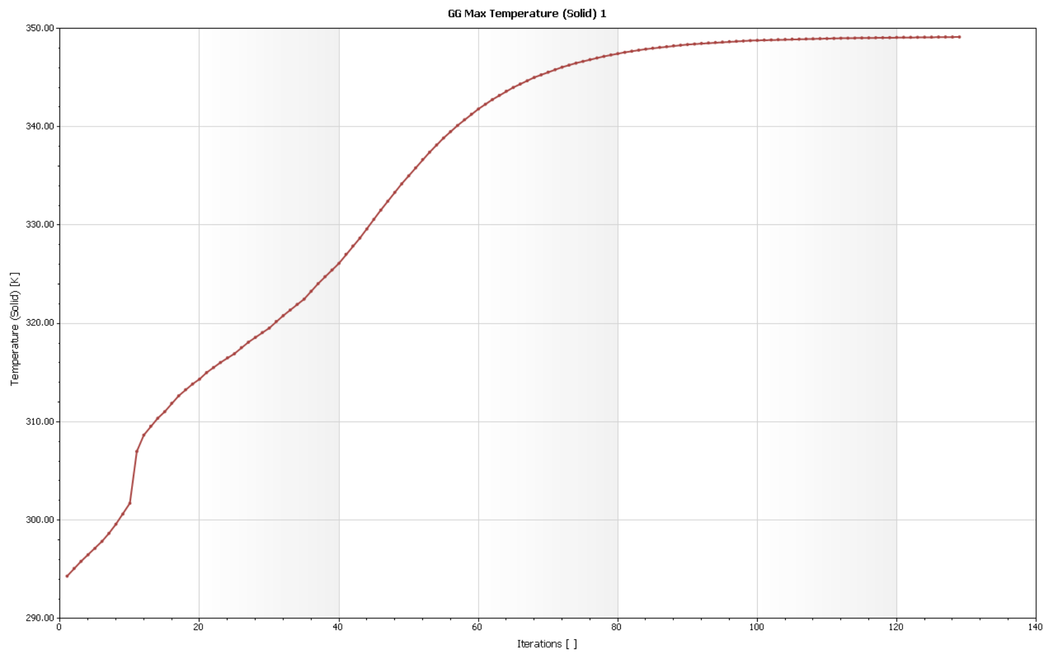
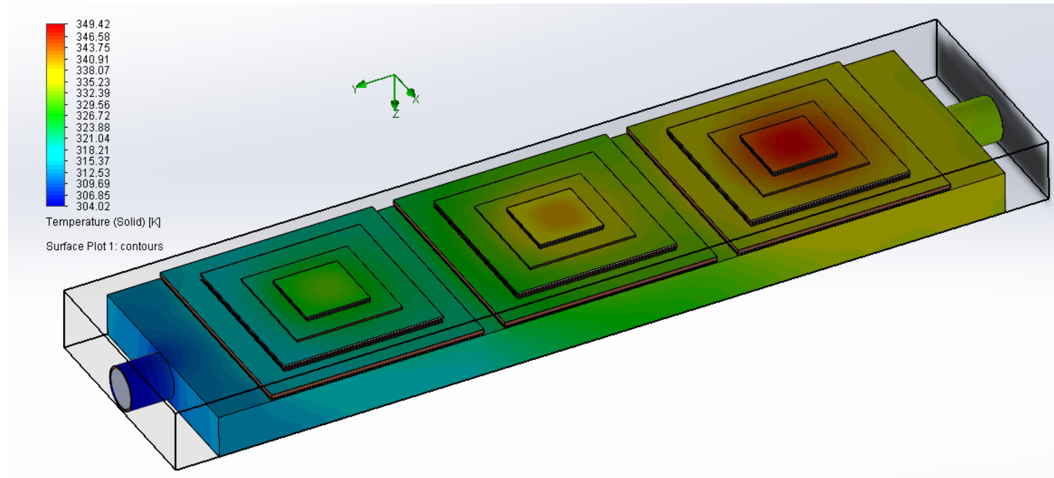


(b)

Figure 3-12 (a) CFD simulation of cold plate with pin/fin length of 0.15 inch (b) Max Temp plot of 0.15 inch pin length cold plate

Pin length: 0.20 inch



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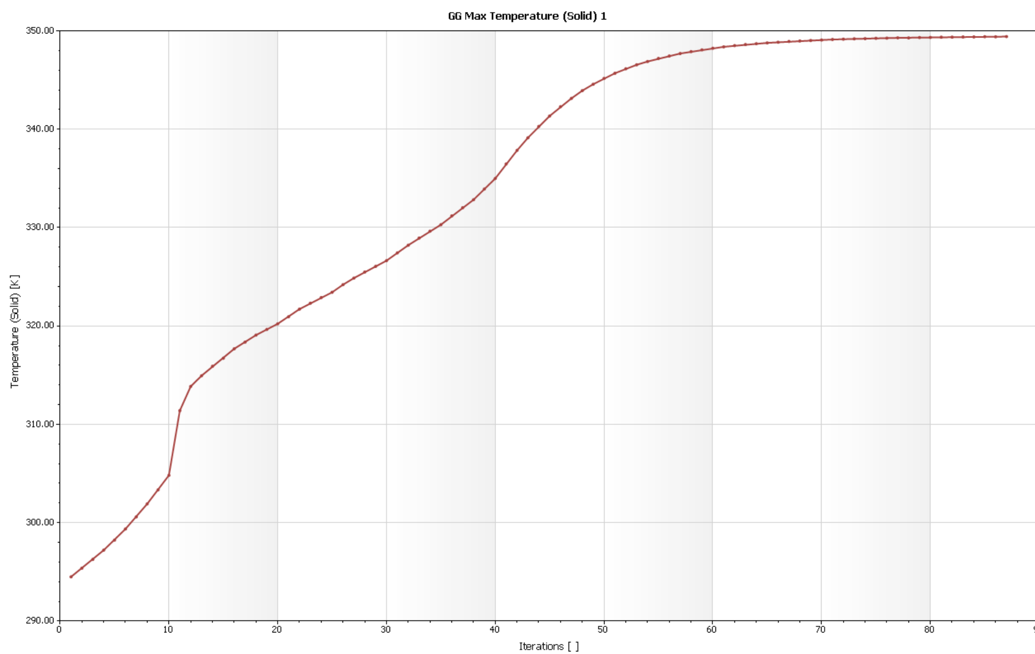
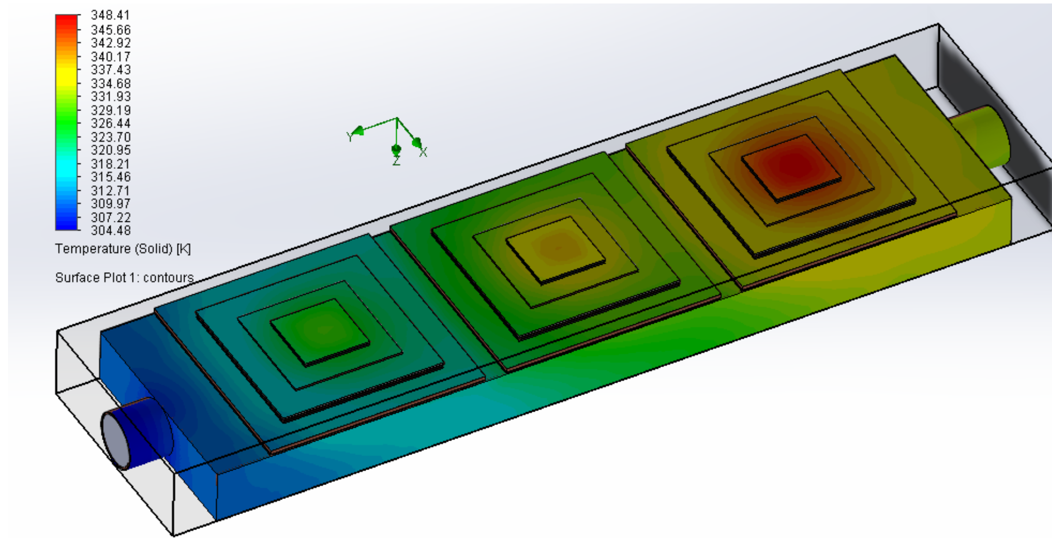


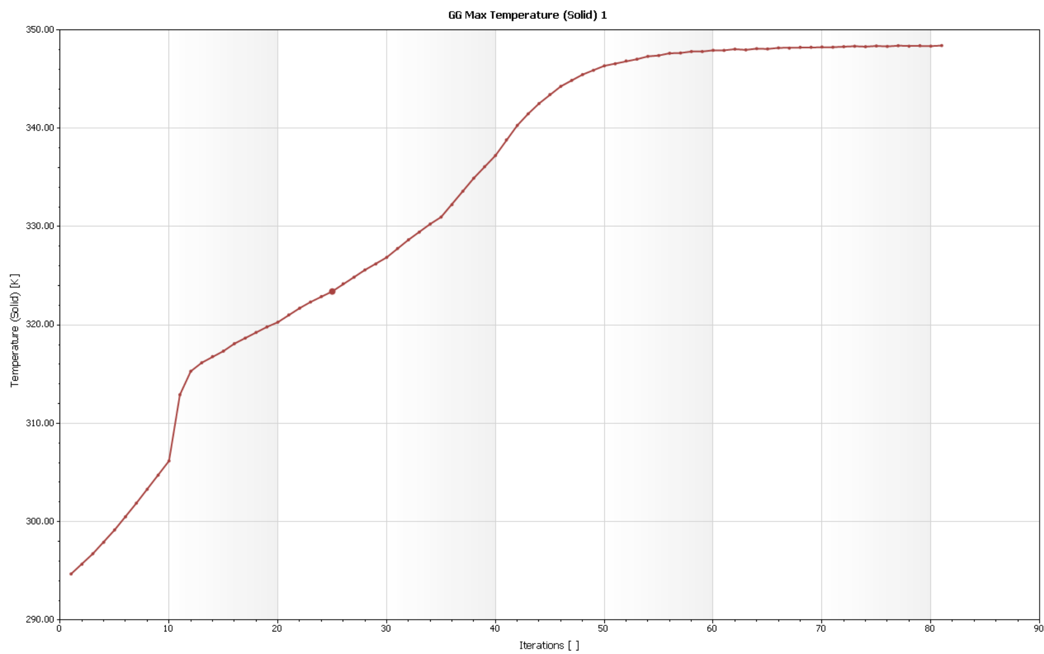
(b)

Figure 3-13 (a) CFD simulation of cold plate with pin/fin length of 0.20 inch (b) Max Temp plot of 0.20 inch pin length cold plate

Pin length: 0.25 inch



(a)



(b)

Figure 3-14 (a) CFD simulation of cold plate with pin/fin length of 0.25 inch (b) Max Temp plot of 0.25 inch pin length cold plate

Results of the Parametric Study

Table 3-1: Results of the parametric study

	Study Variable		Max Solid Temp (K)	Max Fluid Temp (K)
1	Coolant	Air	555	553
		Water	349	350
2	Material	Copper	346	348
		Aluminum	360	356
3	Fin Length	0.15 in	349	347
		0.20 in	350	348
		0.25 in	347	348
4	Fin thickness	0.025 in	351	349
		0.030 in	349	347
		0.035 in	348	346

Chapter 4

Thermal Analysis of an IGBT Module

Thermal analysis is carried out on the IGBT module containing 3 individual IGBT chips producing a power of 150 Watts each. The IGBT module is mounted on the cold plate which removes the excess heat.

The main motivation of this analysis is to show the importance of die level modelling. When thermal engineers design a cooling system for power electronic devices, in order to avoid complication in model geometry they assume uniform heat flux at the end of each component. In practical applications this can be the reason for thermal failure of the system because of the un-uniform heat fluxes from the device which in turn results in peak junction temperatures.

In this analysis two methods are implemented to check the affect of die level modelling on the system. The initial analysis will be carried out considering uniform heat flux around the device to obtain the maximum cold plate temperatures. Later, a detailed die level analysis will be performed to obtain the cold plate and temperatures and also the affect of die level modelling.

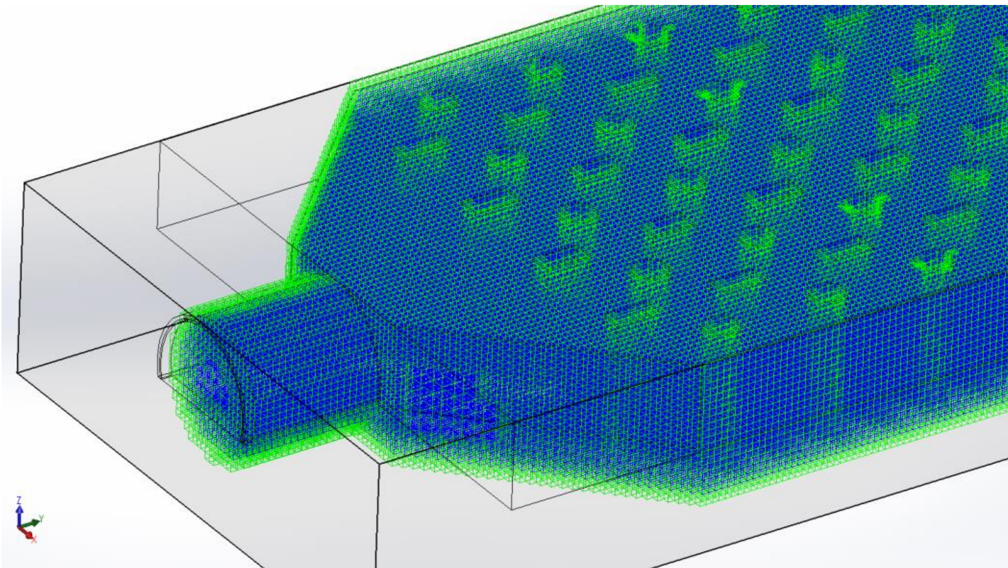
From the results obtained by the parametric study, optimum cold plate material was chosen as copper with pin length of 0.20 inch and a pin thickness of 0.030 inch. Fluid used for cooling in this application was water.

Boundary conditions

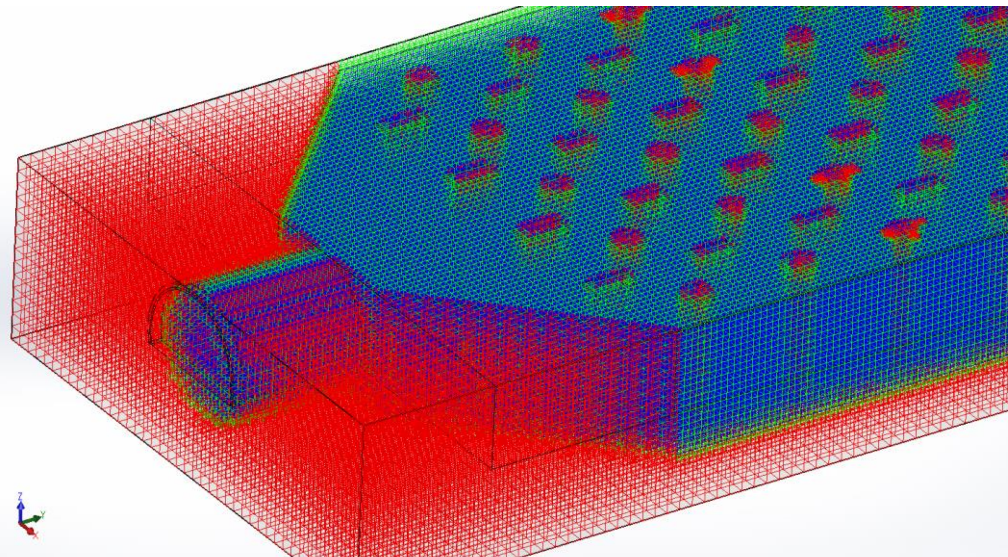
For all the simulations on different cold plate model, same boundary conditions are used to compare the results. The dimensions of the cold plate are 1 inch in width and 3.7 inch in length. Inlet water temperature was maintained at 293.15 K. Mass flow rate in to the cold plate was 0.02 GPM. Heat flux of individual IGBT chips is 150 Watts. The CFD analysis was implemented in solid works flow simulation platform. Solid Works flow simulation uses Cartesian meshing technology with immersed boundary layer.

Meshing

Meshing plays a very important role in fluid flow simulations. It is very important to have a good mesh to converge the required goals and obtain a good result. We can increase number of cells in the mesh to obtain more accurate solution. In this application, meshing was done flow simulation platform.



(a)



(b)

Figure 4-1 (a) Mesh showing Fluid and Partial Cells (b) Mesh showing solid liquid and partial cells

There are 3 different kind of cells in the mesh. Solid mesh cells, fluid mesh cells and partial cells. Partial cells are those cells which are in contact with both solid and fluid in

the model. Fluid cells are those cells which are associated with the fluid flow inside the model. This division of cells results in more accurate solution of the simulation. Fig 5-1 (a) shows the model mesh with just the fluid and partial cells, while Fig 5-1 (b) shows all the mesh cells in the model.

CFD Simulation

Simulation of Cold plate with Rectangular pins

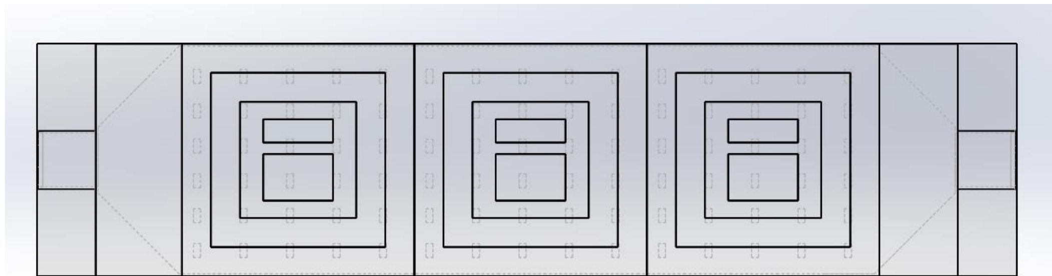
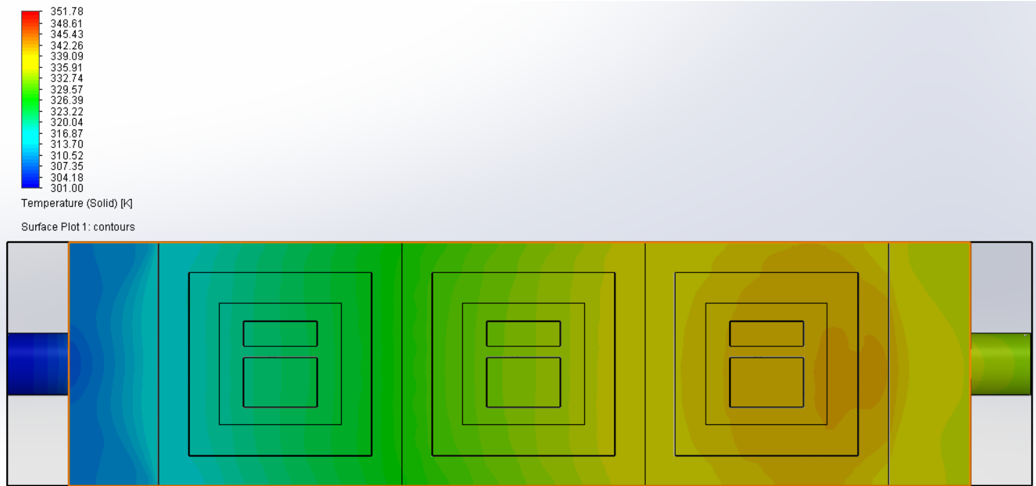


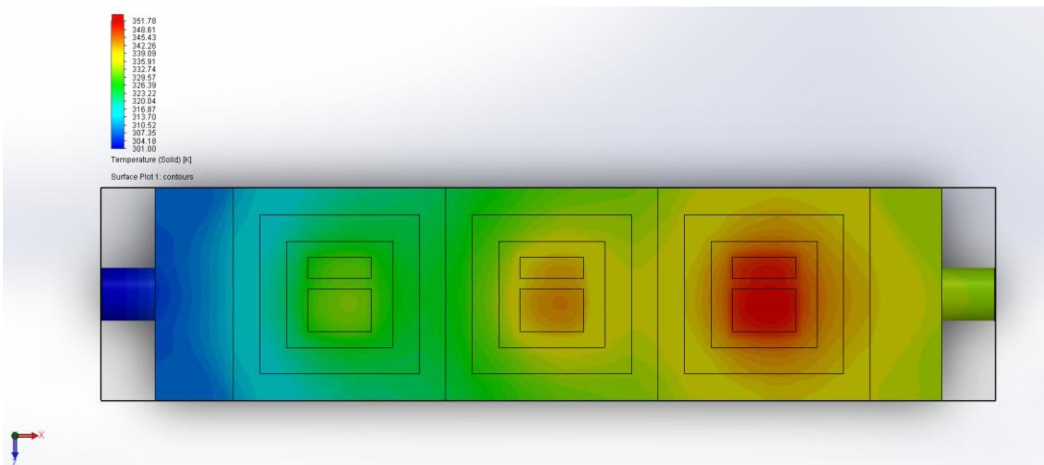
Figure 4-2 Rectangular pins cold plate model with IGBT module

Case: Uniform Heat Flux



(a)

Case: Die Level Modelled



(b)

Figure 4-3 (a) CFD simulation of rectangular pin cold plate with uniform heat flux (b) CFD simulation of die level modelling

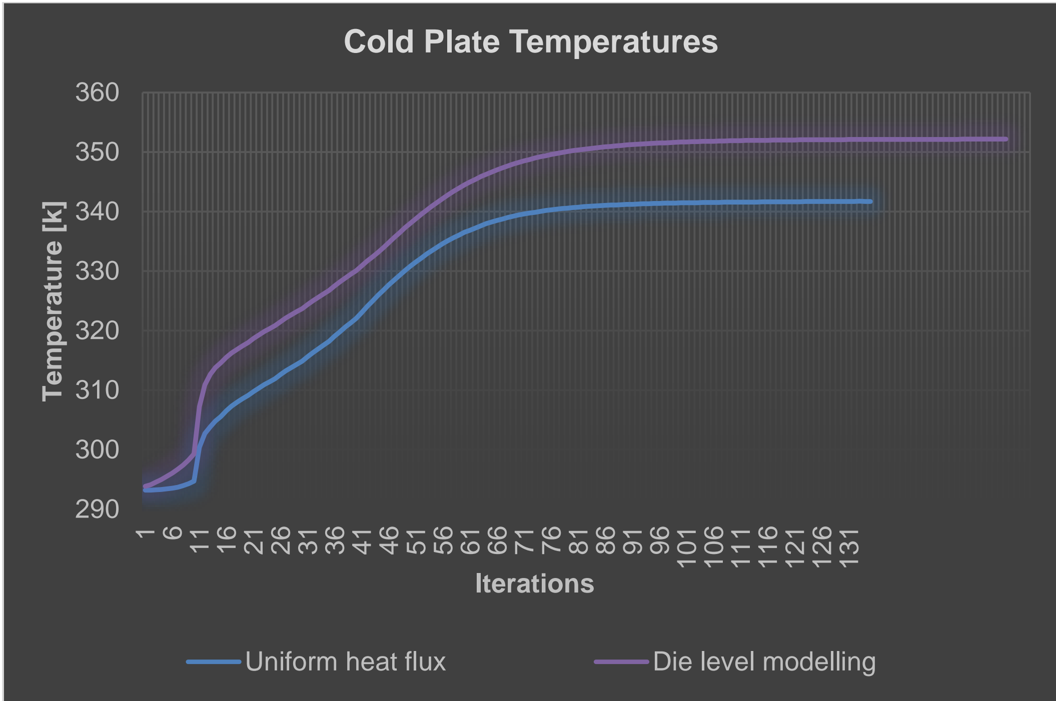


Figure 4-4 Cold plate Temperature plot for rectangular pin cold plate

Simulation of Cold plate with Combined pins

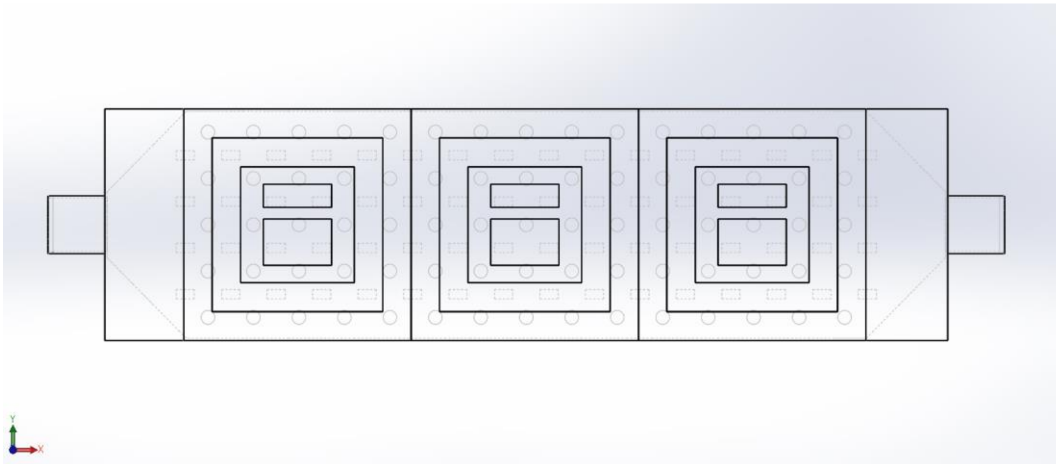
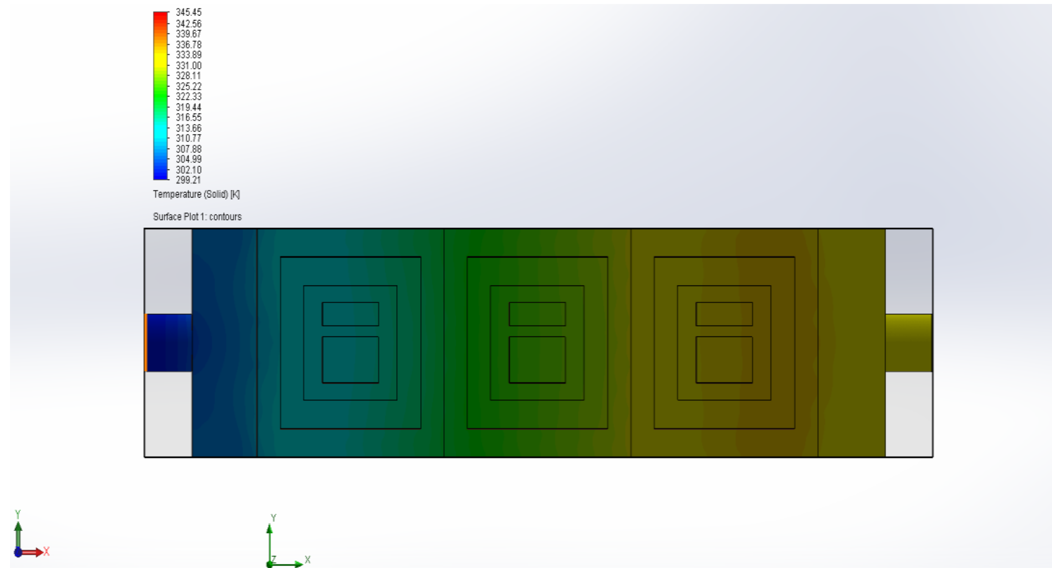


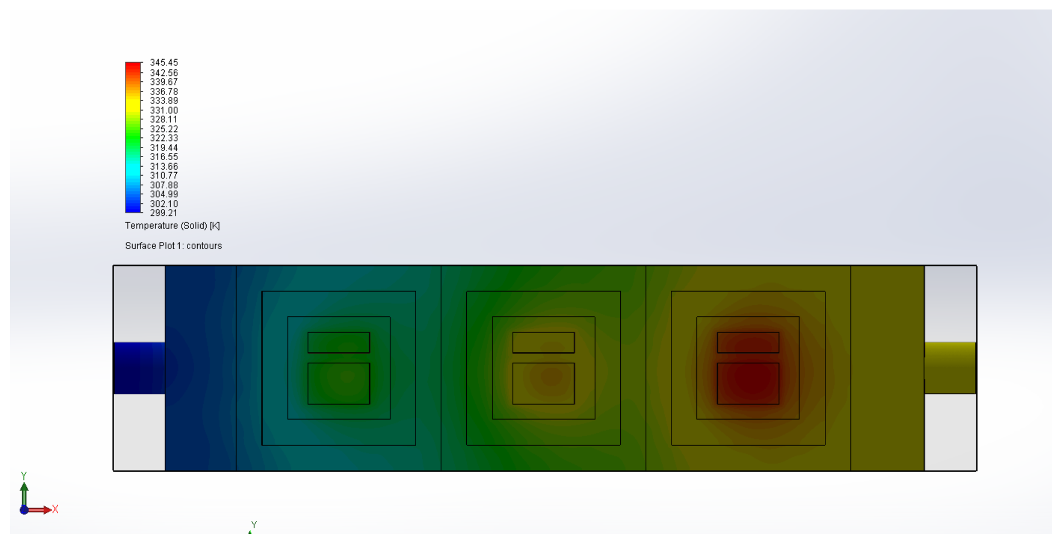
Figure 4-5 Combined pins cold plate model with IGBT module

Case: Uniform Heat Flux



(a)

Case: Die Level Modelled



(b)

Figure 4-6 (a) CFD simulation of combined pins cold plate with uniform heat flux (b) CFD simulation of die level modelling

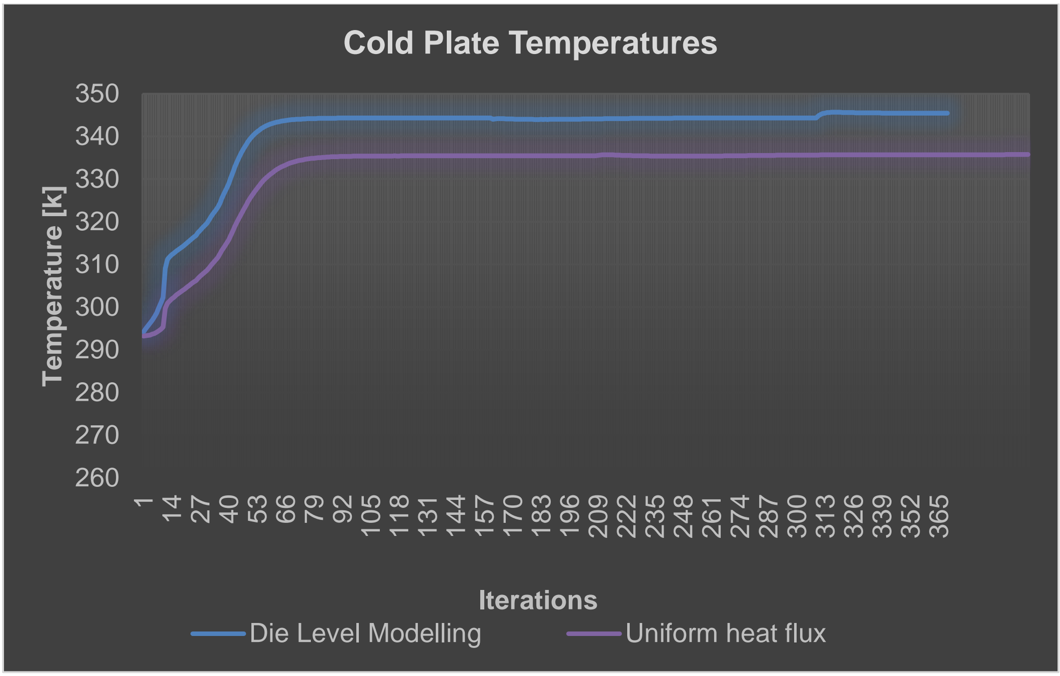


Figure 4-7 Cold plate Temperature plot for combined pin cold plate

Simulation of Cold plate with Round pins

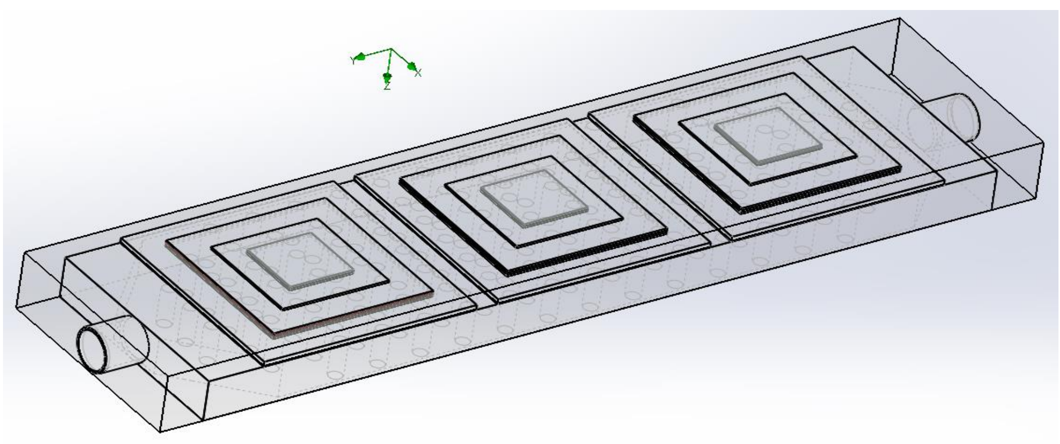
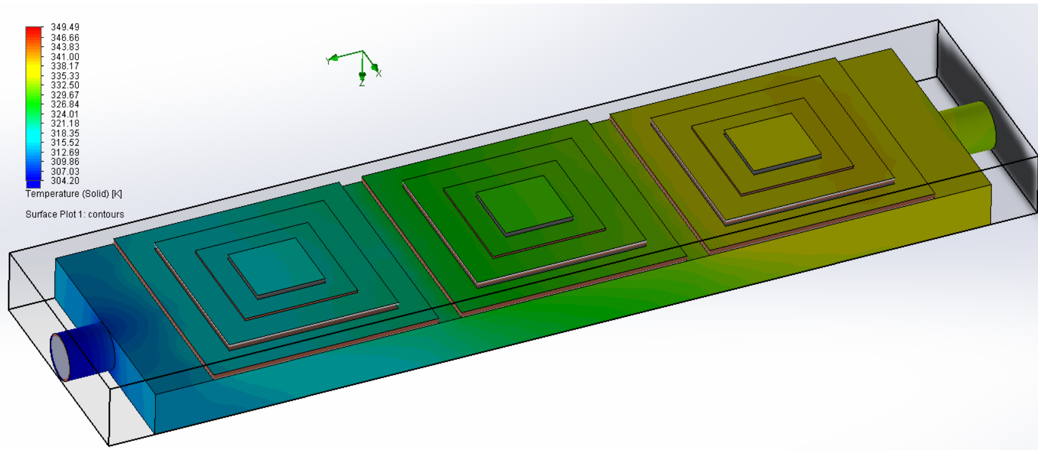


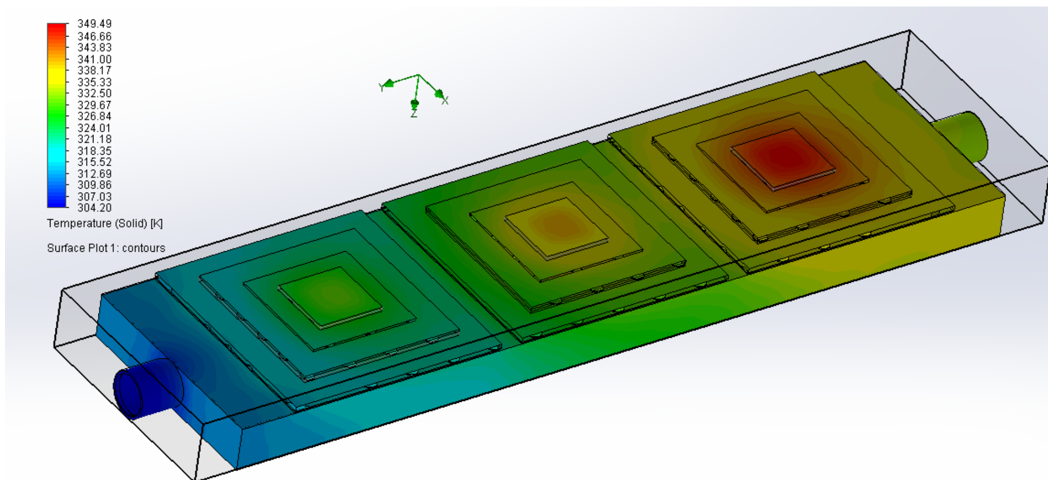
Figure 4-8 Round pins cold plate model with IGBT module

Case: Uniform Heat Flux



(a)

Case: Die Level Modelled



(b)

Figure 4-9 (a) CFD simulation of round pins cold plate with uniform heat flux (b) CFD simulation of die level modelling

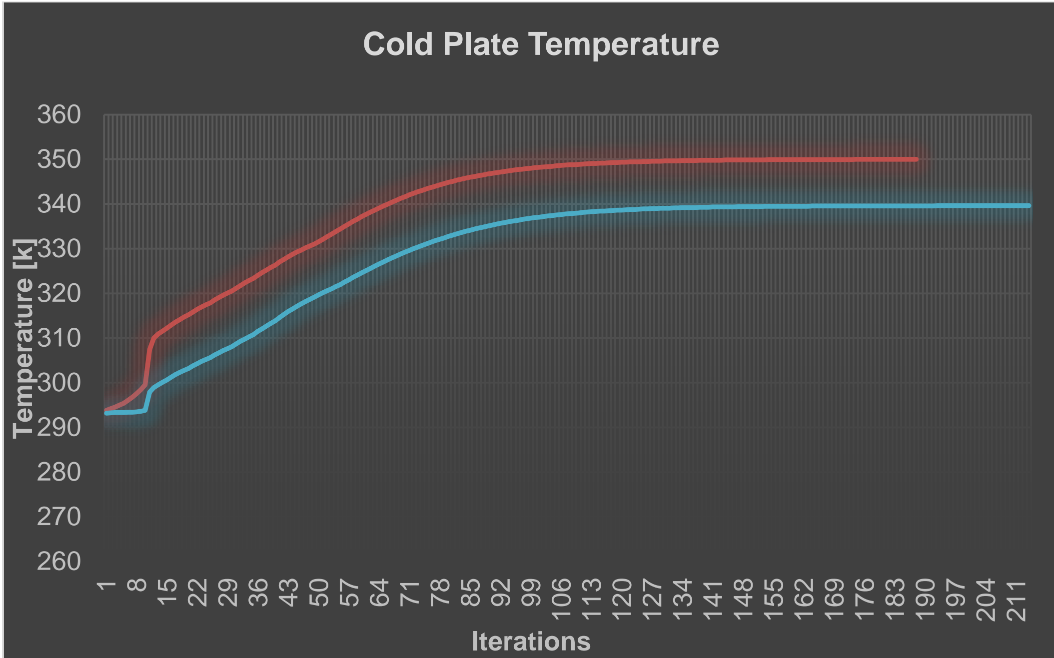


Figure 4-10 Cold plate Temperature plot for round pin cold plate

Simulation of Cold plate with Parallel Plates

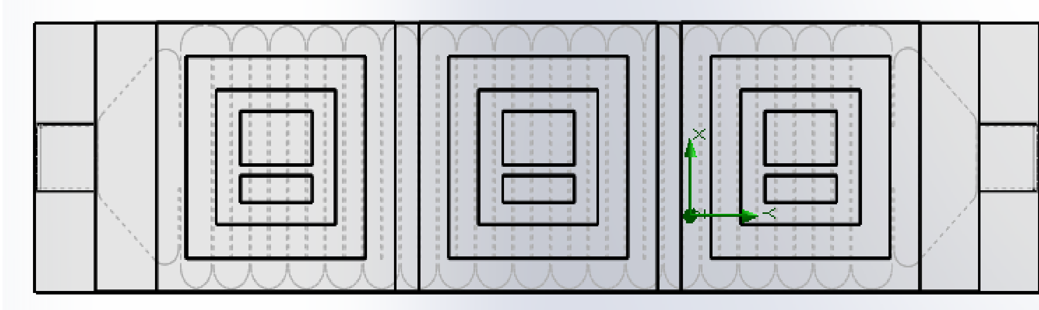
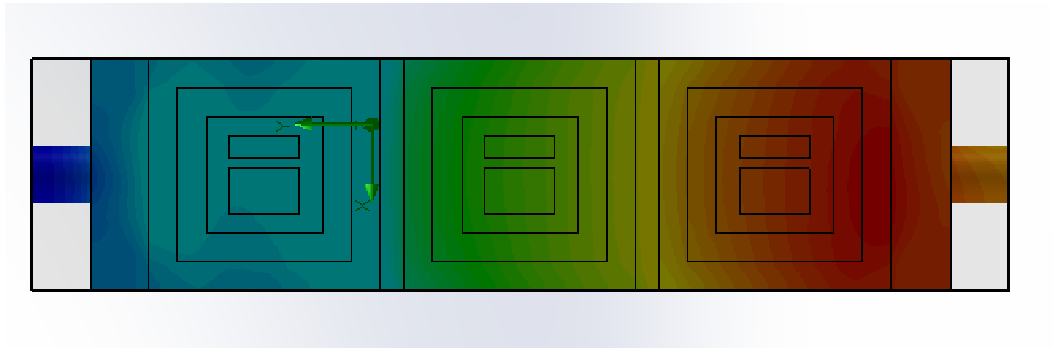


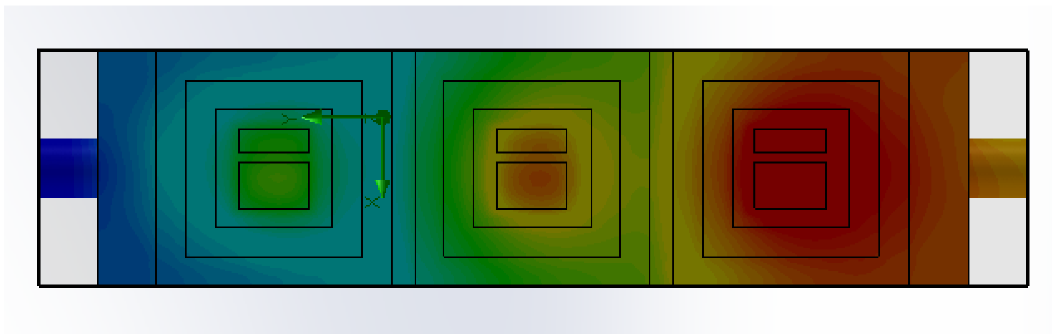
Figure 4-11 Parallel plate cold plate model with IGBT module

Case: Uniform Heat Flux



(a)

Case: Die Level Modelled



(b)

Figure 4-12 (a) CFD simulation of parallel plate cold plate with uniform heat flux (b) CFD simulation of die level modelling

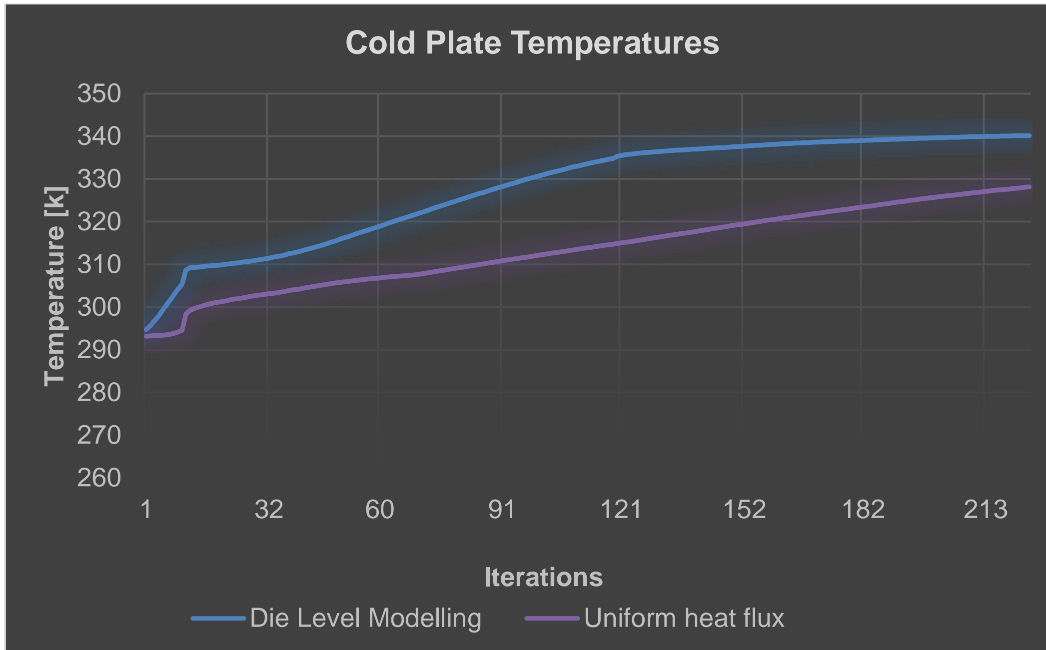


Figure 4-13 Cold plate Temperature plot for parallel plate cold plate

Summary of the CFD results

Table 4-1: Results of the thermal analysis

Cold Plate	Max Cold Plate Temperature [k] with uniform heat flux	Max Cold Plate Temperature [k] with die level modelling
Round Pins	339.6	349.4
Rectangular Pins	341.7	352.1
Combined Pins	335.7	345.4
Parallel Plate	332.8	340.1

The maximum temperatures of the cold obtained from the CFD analysis are tabulated and shown in the above table. All the CFD analysis were carried out with the same boundary conditions. Hence it is easy to compare the results and arrive at a definitive

solution. The rise in temperature of the cold plate model with die level analysis is because the heat generated at the die is not uniform and will result in peak junction temperatures. These high temperatures are not obtained when designing the model assuming uniform heat flux.

Chapter 5

Conclusion

It is evident that there is a significant temperature difference between the die level analysis and the analysis with uniform heat flux. We can see at least a temperature difference of 10 K in every cold plate model. Therefore it is very critical to design the design model from die level to have it work most efficiently and avoid thermal failures, because this increase in temperature is a result of un-uniform heat being generated across the die which in turn will result in peak working junction temperatures. If the peak junction temperature crosses the maximum limit permissible for that particular model, then the model may fail thermally.

Also, since the power requirements are continuously increasing for these electronic devices, it is necessary to obtain accurate results from the analysis and avoid the maintenance cost. Instead of simply getting the system to work, we should get it to work efficiently.

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Biographical Information

Abhishek Raj Urs K N was born in Bangalore, India, in 1990. He received his Bachelor of Engineering degree in Mechanical Engineering from Visvesvaraya Technological University, Karnataka, India, in 2012. He qualified his Master of Science degree in Mechanical and Aerospace Engineering from University of Texas, Arlington in May 2016. During his Master's program, he worked as part of the SAE F600 race car team. He also worked in the University Fab Lab as a mentor to students, faculty and public on functionality of various equipment's such as 3D printers, 3D scanners, CNC machines, Oculus Rift, Laser cutter and Electrical components. During his thesis and course work, he has gained broad experience in automotive and thermal engineering fields. He was awarded Intramural Champion in Billiards tournament held at University of Texas, Arlington in 2015.