IMPACT OF VISCOELASTIC MATERIAL CHARACTERIZATION OF PCB's ON THE THERMOMECHANICAL PROPERTIES OF QFN THICK PACKAGE UNDER THERMAL CYCLING

by

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November 24, 2015

Abstract

IMPACT OF VISCOELASTIC MATERIAL CHARACTERIZTION OF PCB's ON THE THERMO-MECHANICAL PROPERTIES OF QFN THICK PACKAGE UNDER THERMAL CYCLING

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The QFN component package is a quad flat pack (QFP) with "no-leads", where the electrical contact to the printed circuit board (PCB) is made through soldering of the lands underneath the package body rather than the traditional leads formed along the perimeter. The popularity of this device package style is primarily due to the superior electrical and thermal performance demonstrated. It is one of the most cutting-edge technologies emerged in the market, exhibiting high performance with unparalleled cost effectiveness. But using thick PCBs (>3mm) is detrimental to the package reliability. The motivation of this work is to understand and mitigate the failures associated with QFN packages on thick boards.

ANSYS workbench is used in Finite Element (FE) modelling to benchmark with the already existing literature to propose a best-known-method (BKM) for modelling. The analysis includes solving a "Global model" (relatively coarse mesh) with the quarter symmetry QFN model under Accelerated Thermal Cycling (ATC). The viscoelastic orthotropic material properties of the PCB are determined using Thermomechanical Analysis (TMA) and Dynamic Mechanical Analysis (DMA). The properties are determined in various sub-steps. Initially, the whole board level material characterization is determined which is linear elastic in nature. Sub-step involves the layer removal material

characterization of the QFN thick board which helps in determining the complex time and temperature dependent deformation due to mismatch in the Co-efficient of Thermal Expansion (CTE) of each layer. An exhaustive experimental and FE analysis is performed to validate experiment and simulation results.

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Chapter 1

Introduction

1.1 Role of Packaging in Micro-Electronics

There has been a continuous development in the semiconductor industry with the new and enhanced processes leading to highly integrated and reliable circuits. One such process is complementary metal oxide semiconductor (CMOS) process which is being extensively used for the manufacturing of integrated circuits (IC's) [1].

An IC consists of substrate and layers of thin films with their thickness varying from approximately 100 nm to 1μm. A typical CMOS process include films such as:

- Metal interconnects
- Semiconductors (as active part)
- Dielectrics (for electric isolation)
- Passive layers (for mechanical protection)
- Via plugs (for carrying current)

An IC substrate acts like a mechanical carrier during processing.

Figure 1.1 shows a cross-section of a typical IC.

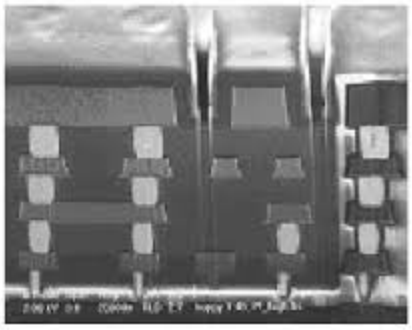


Figure 1.1 Cross section of a typical IC

An IC is manufactured in the waferfab, which is followed by packaging. Packaging plays a very crucial role in any electronic device from the performance and cost cutting view. It is the whole package that is shipped and not just the silicon; packaging significantly contributes to the total cost – equal to or greater than that of the silicon. The foremost primary functions of a package are:

- Allow an IC to be handled for PC Board assembly
- Enhance thermal and electrical properties
- Surface Mount IC packages
- Allow standardization (footprints)

Packages can be broadly classified as (refer Figure 1.2):

- Mechanical and chemical protection against the environment
- Through Hole Mount IC Packages
- Contactless Mount IC Packages

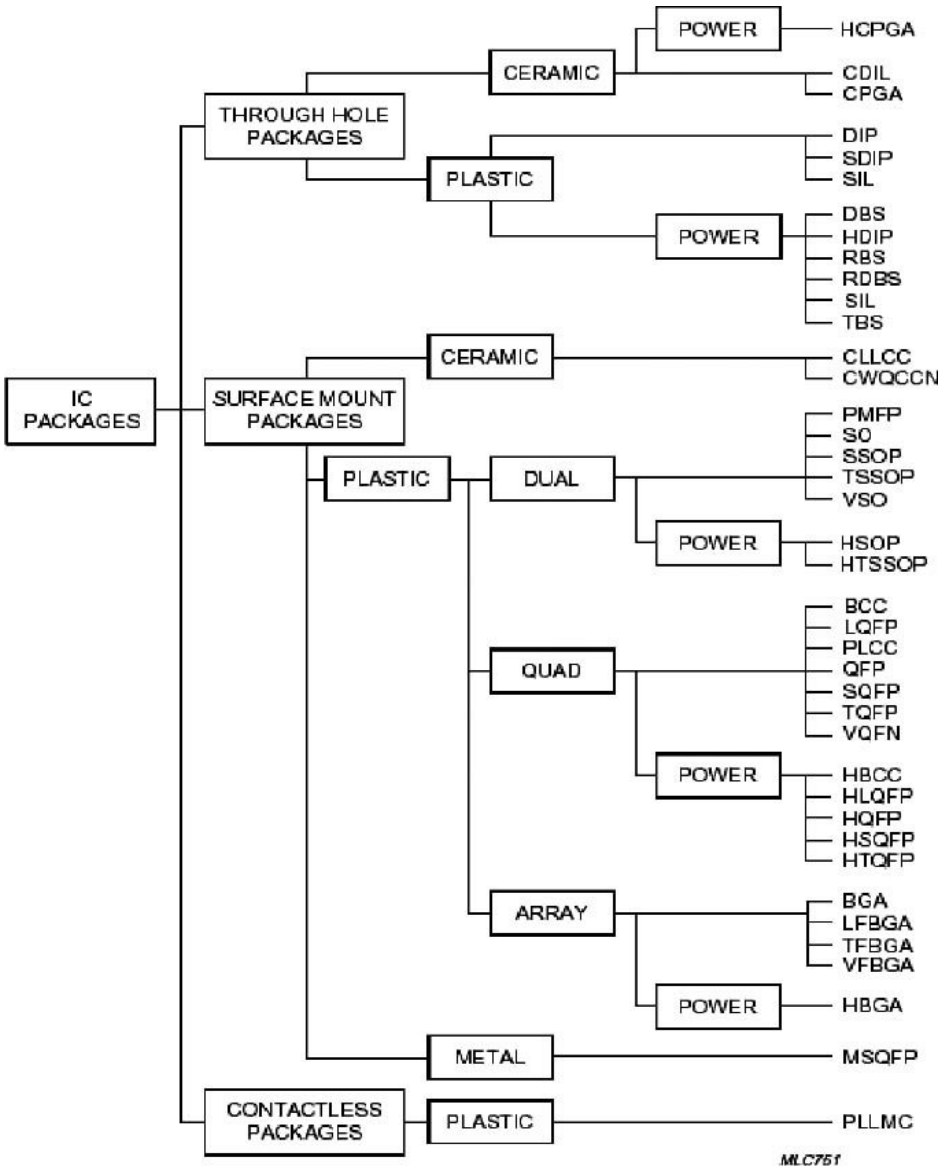


Figure 1.2 Classification of different packages

Figure 1.3 shows the schematic representation of the assembly process involving a typical lead frame package. Representation describes how packages are manufactured after a series of process using various forms of polymers.

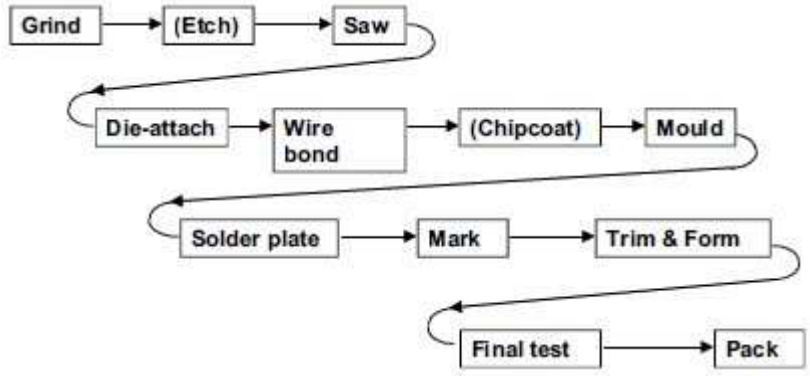


Figure 1.3 Schematic representation of the assembly process of a lead frame package (LFP)

1.2 Quad Flat No-Lead (QFN) Packages

As there is an increase in worldwide mobility, consumers have demanded for smaller and lighter products to stay connected with the exponentially growing creative market. Smaller, thinner and thermally enhanced packages help achieve product miniaturization. Numerous performance analysis have given way for Quad Flat No-Lead (QFN) packages to have better thermal performance than dual in-line surface-mount technology (SMT) packages [2]. QFN package is a thermally enhanced standard size IC package designed to eliminate the use of bulky slugs and heat sinks. QFN is a leadless package where the electrical contact to the printed circuit board (PCB) is made through soldering of the lands underneath the package body rather than the traditional leads formed along the perimeter [3]. Using PCB assembly techniques, it is easy to mount on the IC and can be replaced and removed using standard procedures. The design shows how the thermal pad (lead frame die pad) is exposed to the bottom of the IC. The efficiency of conduction of heat between the exterior of the package and the die is high due to its low resistance path.

Figure 1.4 shows the section view of a typical QFN package

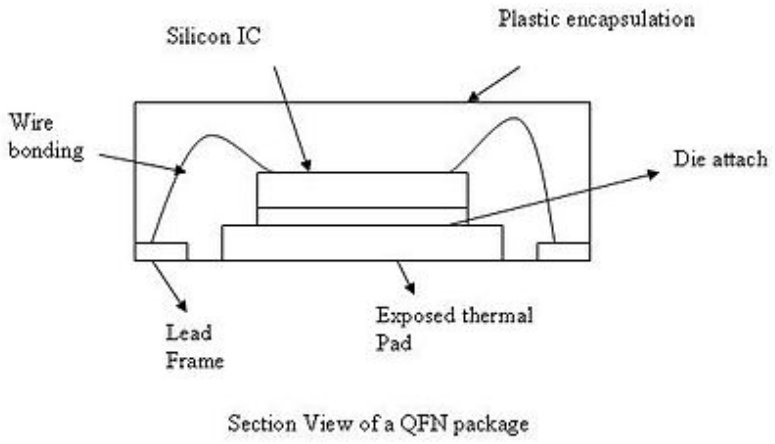


Figure 1.4 Section view of a typical QFN package

The popularity of this device package style is primarily due to the superior electrical and thermal performance demonstrated. It is one of the most cutting-edge technologies emerged in the market, exhibiting high performance with unparalleled cost effectiveness.

For the analysis of this project, Texas Instruments (TI) provided the QFN packages. The make of QFN and its detailed properties will be discussed in chapter 5.

1.3 Thermal Cycling

The majority of electronic failures are due to thermally induced stresses and strains caused by excessive differences in coefficients of thermal expansion (CTE) across materials.

CTE mismatches occur between the interconnects of die to a substrate or the substrate or the package to the PCB. This would be termed as “board level” CTE mismatch. As we know PCB consists of several layers of Copper (CU) and substrate in between, there will be CTE mismatch all along the layers as well. Due to excessive difference in the CTE between the PCB and its components, there will be a large enough strain in solder and embedded copper structures to induce a fatigue failure mode [4].

Thermal cycling is used to simulate both ambient and internal temperature changes that result during device power up, operation and ambient storage in controlled environments. The mismatch in the CTE’s between various package and board components gives rise to warp and expand unevenly resulting in generation of elastic strain, thermal stresses which results in crack propagation in dielectric, fatigue and adhesion problems. The thermal cycling tests helps in detecting these problems.

Table 1.1 shows different temperature ranges for electronic products under different service environments [1].

Table 1.1 Thermal environments for electronic products

Use condition	Thermal excursion (°C)
Consumer electronics	0 to 60
Telecommunications	-40 to 85
Commercial aircraft	-55 to 95
Military aircraft	-55 to 125
Space	-40 to 85
Automotive-passenger	-55 to 65
Automotive-under the hood	-55 to 160

These thermal cycling tests are conducted at package level and board level. Package level tests are done to test the robustness pf the package component materials and design to withstand extreme environmental conditions. It does not consider the interconnects when it is mounted on the board. Board level and layer level determines the stresses and strain on the solder joint of the surface mount package when mounted on board [5].

1.4 Objective

1.4.1 Motivation

Most often QFN package is widely used in handhled devices. But the gain in the popularity QFN package due its low cost, efficient thermal performance characteristics and compact size, some customers are demanding it for heavy industry applications for thicker PCB. According to the existing literature, as the thickness of PCB increases, the reliability and fatigue life of the package decreases as the board becomes stiffer and less flexible resulting in more transfer of stresses on the solder joint.

A RHM QFN package with 3.4mm (134mil), 16 layers thick board was tested under ATC conditions. The ATC profile was from -40°C to +125°C with 15min dwell and 5min ramp using the IPC9592 standard. The test results showed that out of 75 units on the board, 10 units showed early fails (less than 700 cycles) having insufficient joint, zero standoff or a combination of both (refer Figure 1.5 and Figure 1.6).

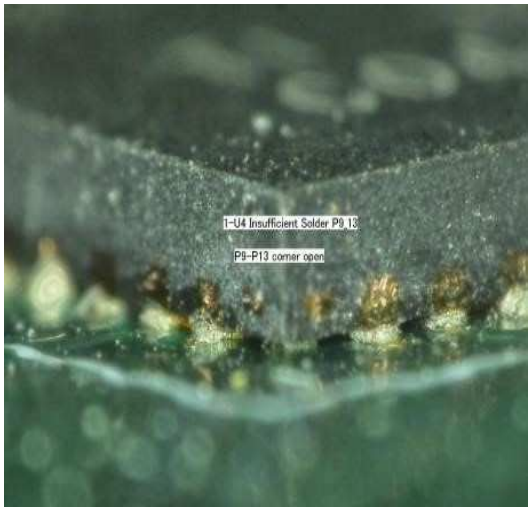


Figure 1.5 Typical fail unit showing insufficient joint

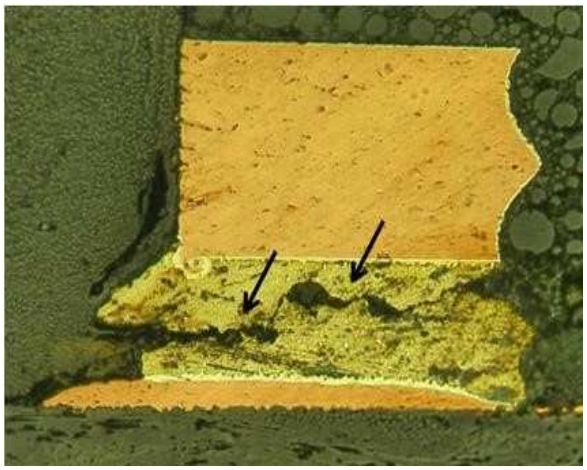


Figure 1.6 Crack propagation in a solder joint

The failures detected on the thicker board reduces the reliability and fatigue life of the package. The motivation of this thesis is to primarily determine the material characteristic properties for the board level and for the complex time and temperature dependent layer removed compound board and to find out the stress and elastic strain for the same under thermal cycling using FEA.

1.4.2 Goals

The primary objective of this work is to determine the material characteristic properties for the FR4 board at board level (repetitive similar samples) and analyze the strain energy, elastic strain and stress of the QFN package with FR4 board in the constrained direction using Finite Element Analysis (FEA) under thermal cycling. Analysis is further continued onto complex time and temperature dependent layer removed compound PCB (reducing thickness) which exhibits mismatch in CTE, Storage Modulus and Loss Modulus.

Chapter 2

Literature Review

R. Rodgers et al. [5] studied the board level reliability test for surface mount packages. The tests included for this process were based on both customer and industry requirements such as JEDEC, Mil Std, and AEC-Q100. They established a method in assessing the design for reliability of solder joint interconnects of device packages. Package level or 1st level reliability stress tests are supposed to withstand extreme environmental conditions and does not consider its solder interconnect reliability when it is board mounted. For the board level or 2nd level reliability tests, stresses are concentrated on the solder joint interconnect performance of the surface mount package when it is board mounted.

Tong Yan Tee et al. [15] studied the board level solder joint reliability for both QFN and enhanced design of PowerQFN under thermal cycling. They established a detailed solder joint fatigue model with life prediction capability within ±34% error. They also performed a comprehensive design analysis to study the effects of key variables on fatigue life and suggested to have smaller package type, more center pad soldering, smaller die size, thinner die, bigger die pad size, thinner board, longer lead length/width, smaller pitch, higher solder standoff, solder with fillet, higher mold compound CTE and smaller temperature range of thermal cycling test for enhanced solder joint reliability of QFN. Their analysis found out that the land size, mold compound modulus and die attach material has insignificant effects on reliability.

Syed et al. [16] conducted series of experiments on QFN packages and provided guidelines on board design and surface mounting of this package. They also evaluated board level reliability for temperature cycling and recommended having mold compound with higher coefficient of thermal expansion (CTE), lower die to package size ratio, larger land size, thinner board, soldered exposed pad, slower ramp rate and lower temperature extremes and greater standoff height will enhance board level reliability and increase cycles to failure.

Birzer et al. [17] performed board level stress tests of QFN packages under temperature cycling, drop, bend and power cycling tests. They observed that the QFNs on thick boards with many metal layers are critical as compared to thin boards regarding temperature cycling reliability. Also, apart from the board thickness; board design, materials and surface mount technology (SMT) process has significant influence on the board level reliability of QFN packages.

Li Li et al. [18] developed a parametric 3D FEA model of QFN for board level reliability modeling and testing having the capability of predicting the fatigue life of solder joint during thermal cycling test within a certain error range. They also performed design for reliability and assembly analyses to study the effect of key parameters and use those results to develop best practice design and assembly recommendations.

Vries et al. [19] did a solder joint reliability analysis of selected series of small, medium and large QFN packages under thermal cycling using experimental, analytical and numerical solutions. They demonstrated the importance of board parameters such as the coefficient of thermal expansion and stiffness (board thickness and Young's modulus). Also the paper established that if the glass transition temperature (T_g) of the board enters between the thermal cycling range, the mechanism of building up of stress changes effecting the board.

Chapter 3

Material Characterization

In order to accurately determine the material response generated in finite element model, it is necessary to input actual material properties for each material. Since the data on the properties of thick PCB's is inadequate, the thick PCB's were characterized for finding following material properties-

- Coefficient of Thermal Expansion (CTE)
- Glass Transition Temperature (Tg)
- Storage Modulus (E')
- Loss Modulus (E")

Equipment's and techniques used for characterization include-

- Thermomechanical Analysis (TMA)
- Dynamic Mechanical Analysis (DMA)

3.1 Coefficient of Thermal Expansion (CTE)

The Coefficient of Thermal Expansion (CTE) is defined as the change in length or volume of a material for a unit change in temperature. The overall coefficient is the linear thermal expansion per degree Fahrenheit or Celsius. It is calculated by the change in length divided by the quantity of the length at room temperature, multiplied by the change in temperature [6]. Generally it is given by-

$$\alpha = \frac{\epsilon}{\Delta T}$$

Where,

α – Coefficient of Thermal Expansion (CTE) ppm/°C

ϵ - Strain (mm/mm)

ΔT –Temperature Difference (°C)

3.2 Glass Transition Temperature

The Glass Transition Temperature (Tg) is one of the most important properties of any epoxy and is the temperature region where the polymer transitions from hard, glassy material to a relatively soft material [7].

Figure 1.7 shows a typical Tg graph

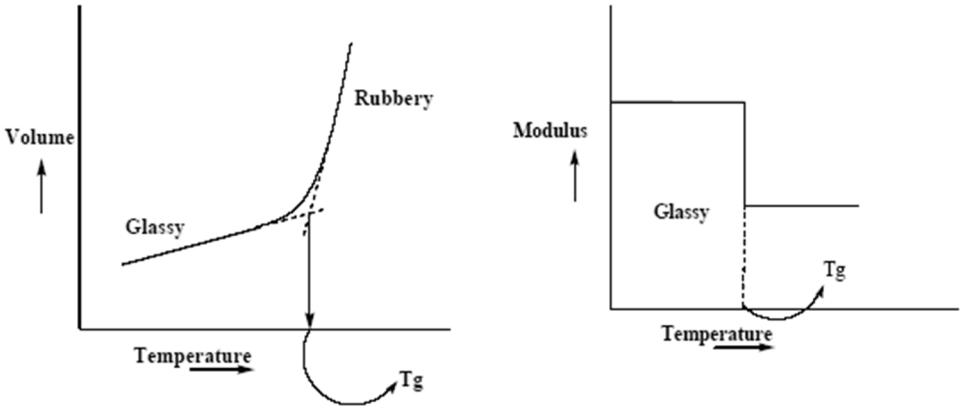


Figure 3.1 Typical Glass Transition Temperature graph

Using TMA, thermal cycling load is applied from 20°C to 150°C. Hence it is necessary to know the CTE of the package so that FEA model would replicate the actual condition as closely as possible

3.3 Thermomechanical Analysis – CTE and Tg Measurement

The need for a commercial TMA grew from hardness or penetration tests and was used in polymers in 1948 [8]. From then on it has developed into a powerful tool in the analytical laboratory. TMA measurements record changes caused by changes in the free volume of a polymer [9]. Experimentally, a TMA consists of an analytical train that allows precise measurements of position and can be calibrated against known standards. The sample is coupled to a temperature system with a furnace, heat sink and a temperature measuring device (Thermocouple). Fixtures to hold the sample during the test are commonly made of quartz due to its low CTE. The fixtures can be of expansion, three-point bending, parallel rate and penetration tests. TMA data determines the Coefficient of Thermal Expansion (CTE) and from the same set of data, Glass Transition Temperature (Tg) can be calculated. For an anisotropic material, the CTE will be different depending on which direction it has been measured. For example, a composite of an epoxy will show distinct CTE's corresponding to the x, y, and z directions [10].

Figure 3.2 TMA 6600

For this project, TMA 6600 is used as an analyzing tool. The test sample which is QFN 134mil is placed in the holder with a Tension probe (made of quartz) with the test settings being as follows

- Start and End limit Temperatures - +20°C to +180°C
- Ramp Input of 5°C/min
- Start and End load of -100mN

The measurement test was benchmarked with Aluminum sample to gain the confidence. Tests were conducted for each case with a minimum of 5 similar samples.

3.4 CTE and Tg Results

CTE and Tg measured using TMA for different cases are shown in the graphs below and is tabulated for further reference.

3.4.1 Board Level

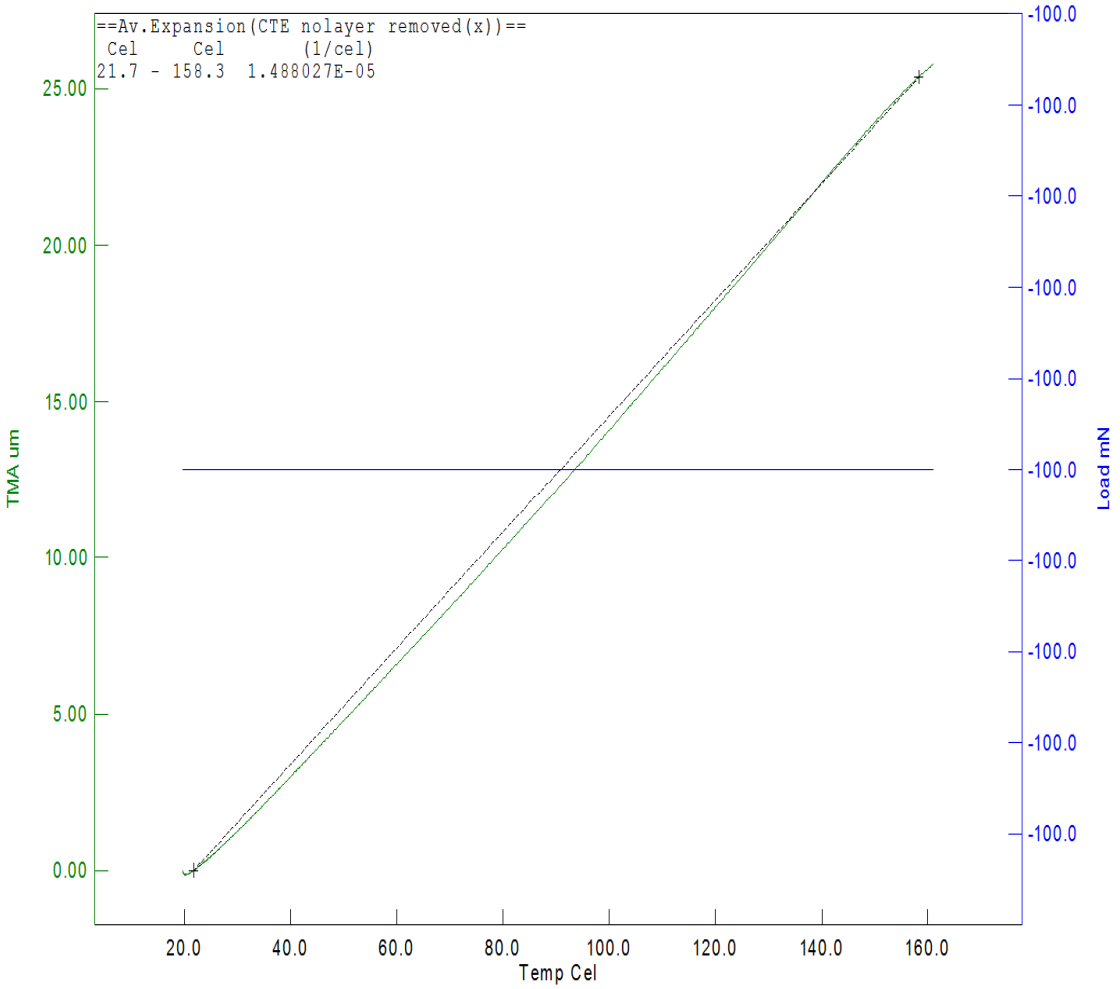


Figure 3.3 CTE in x-direction

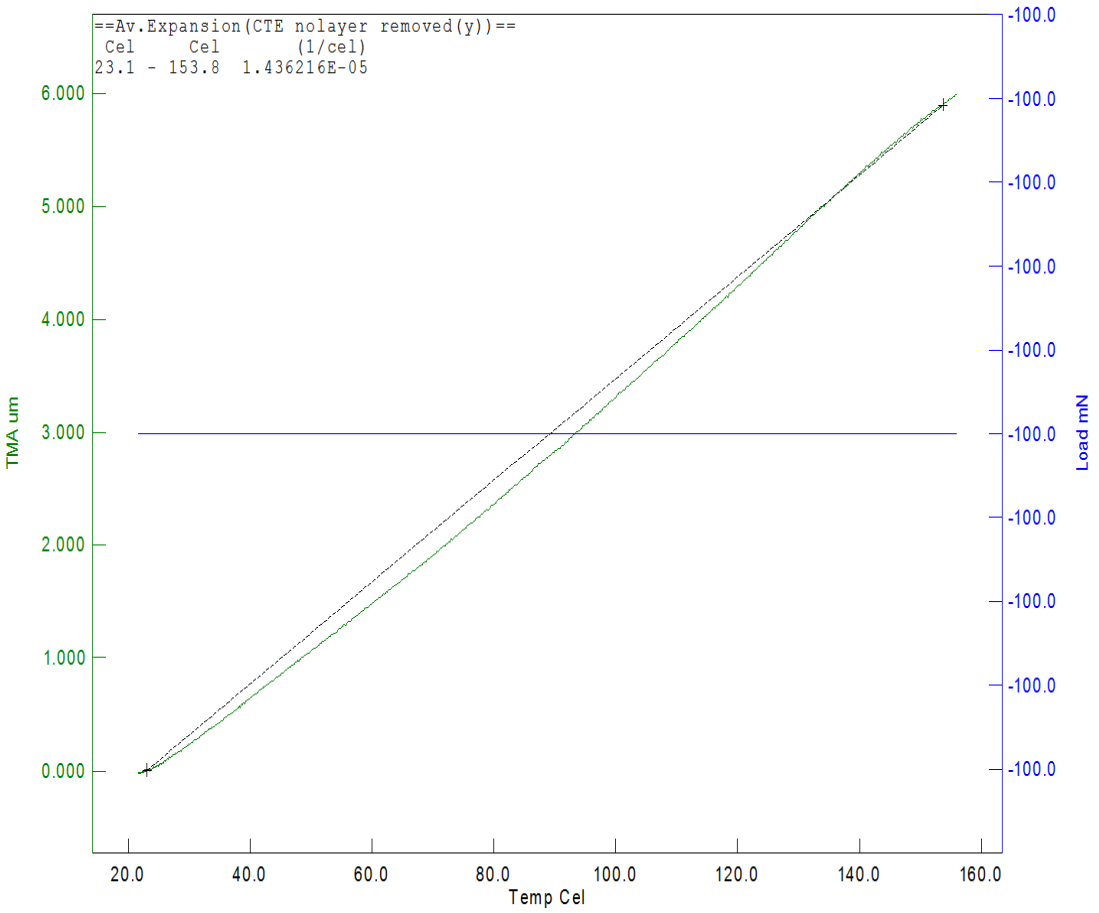


Figure 3.4 CTE in y-direction

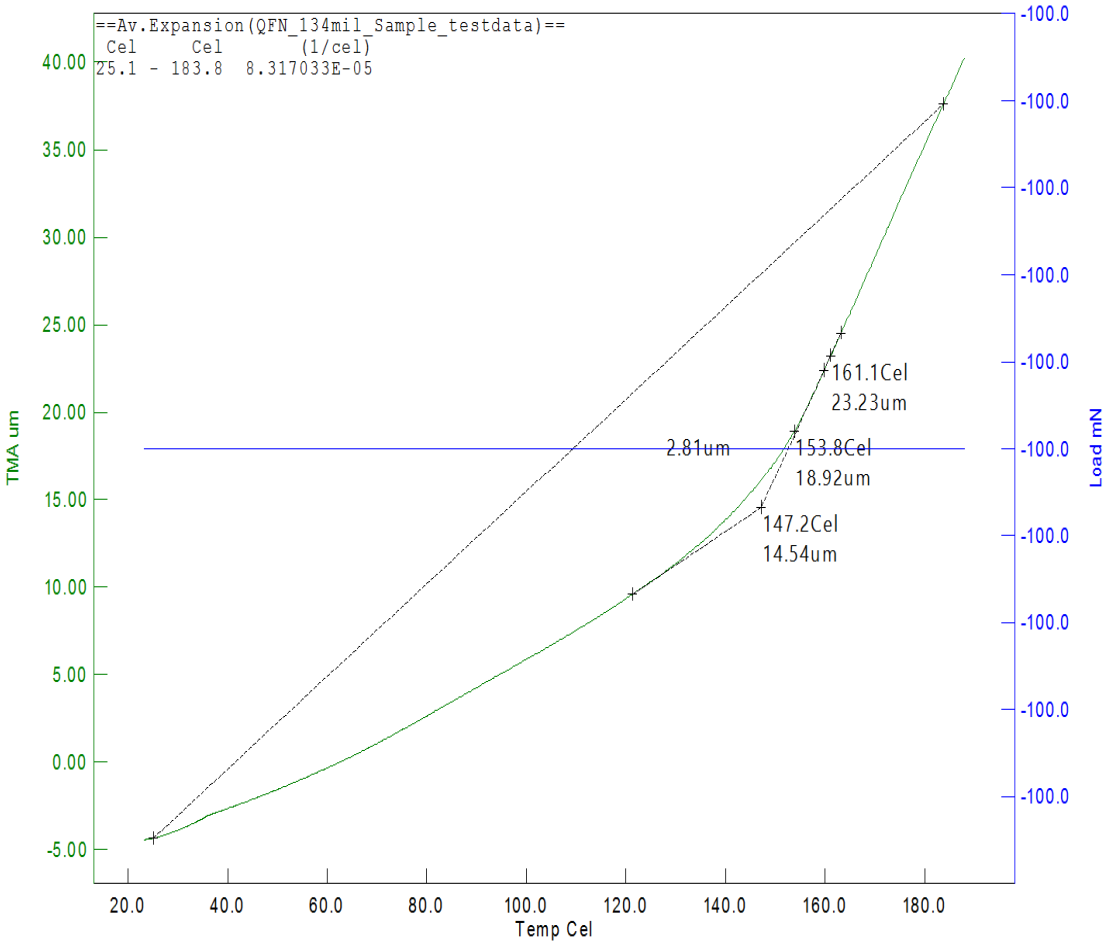
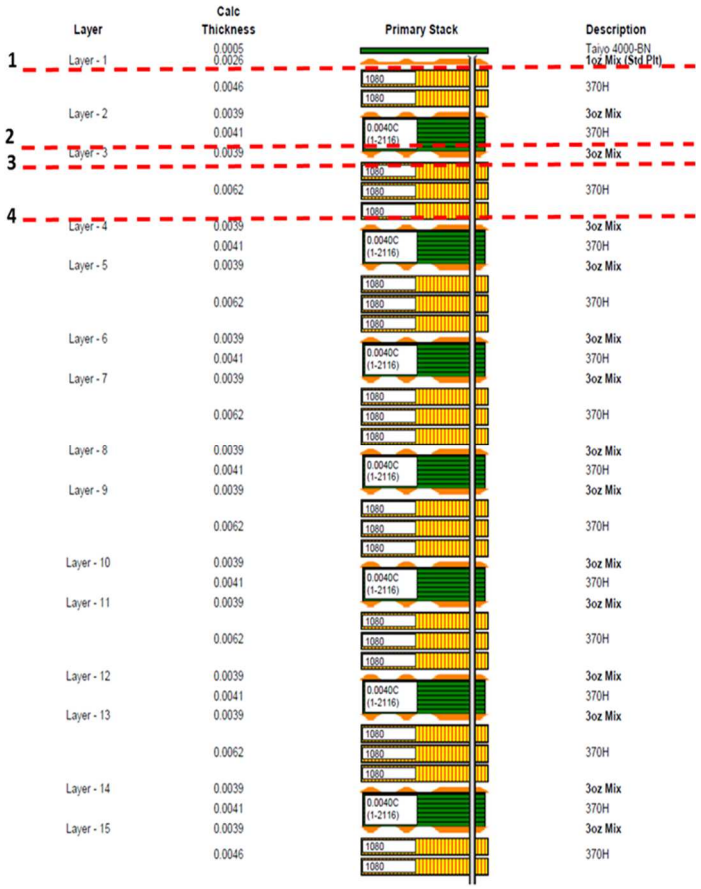


Figure 3.5 CTE and Tg in z direction

3.4.2 Layer Removal CTE Analysis of QFN 134mil



Samples Details

1	Removed SM + 1 Cu layer	70 µm	One Side (Top / Bottom)
2	Removed 2 Cu layers + 2 FR4	375 µm	
3	Removed 3 Cu layers+ 2 FR4	470 µm	
4	Removed 3 Cu layers + 3 FR4	615 µm	

a	Removed SM + 1 Cu layer	70 µm	Both Side (Top and Bottom)
b	Removed 2 Cu layers + 2 FR4	375 µm	
c	Removed 3 Cu layers+ 2 FR4	470 µm	
d	Removed3 Cu layers + 3 FR4	615 µm	

Figure 3.6 Stack-up of QFN 134 mil Board

3.4.3 Layers Removed from One side

Removed 1SM + 1CU layer

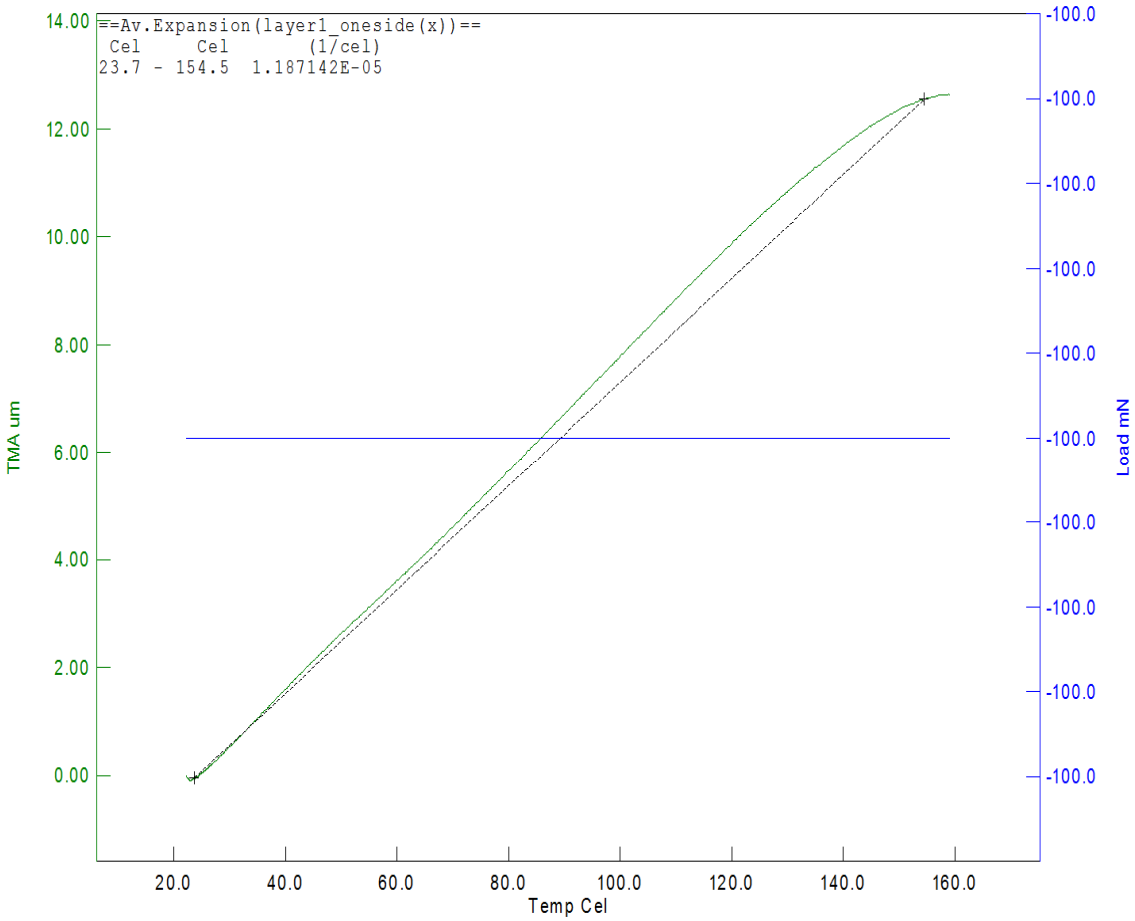


Figure 3.7 CTE in x-direction

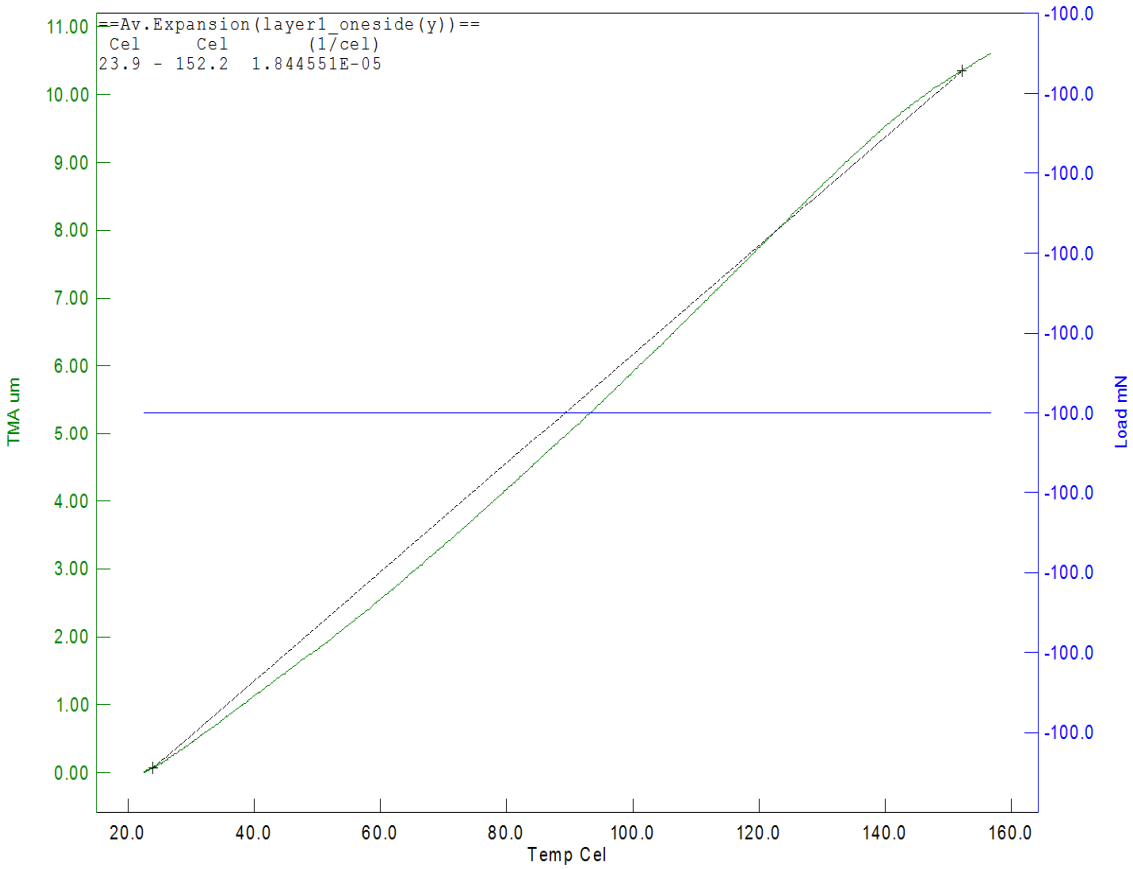


Figure 3.8 CTE in y-direction

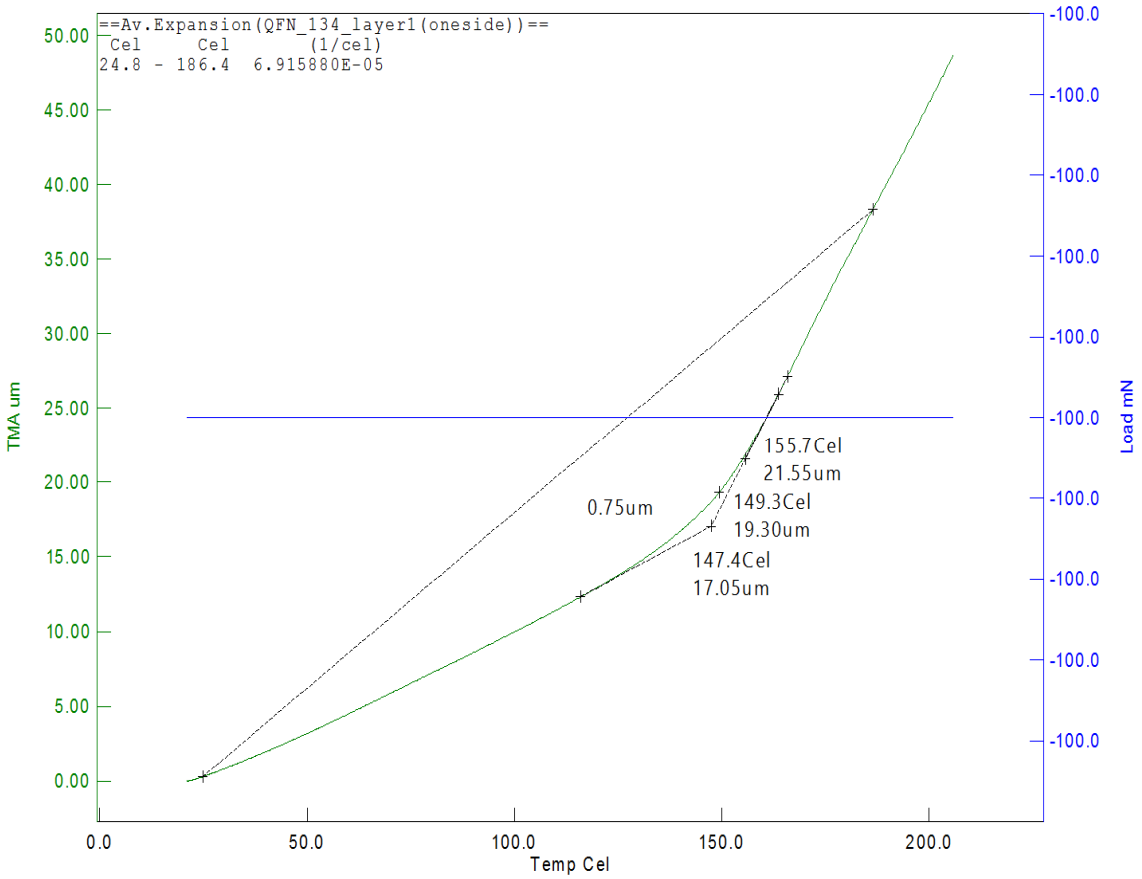


Figure 3.9 CTE and Tg in z-direction

Removed 2CU layers + 2 FR4

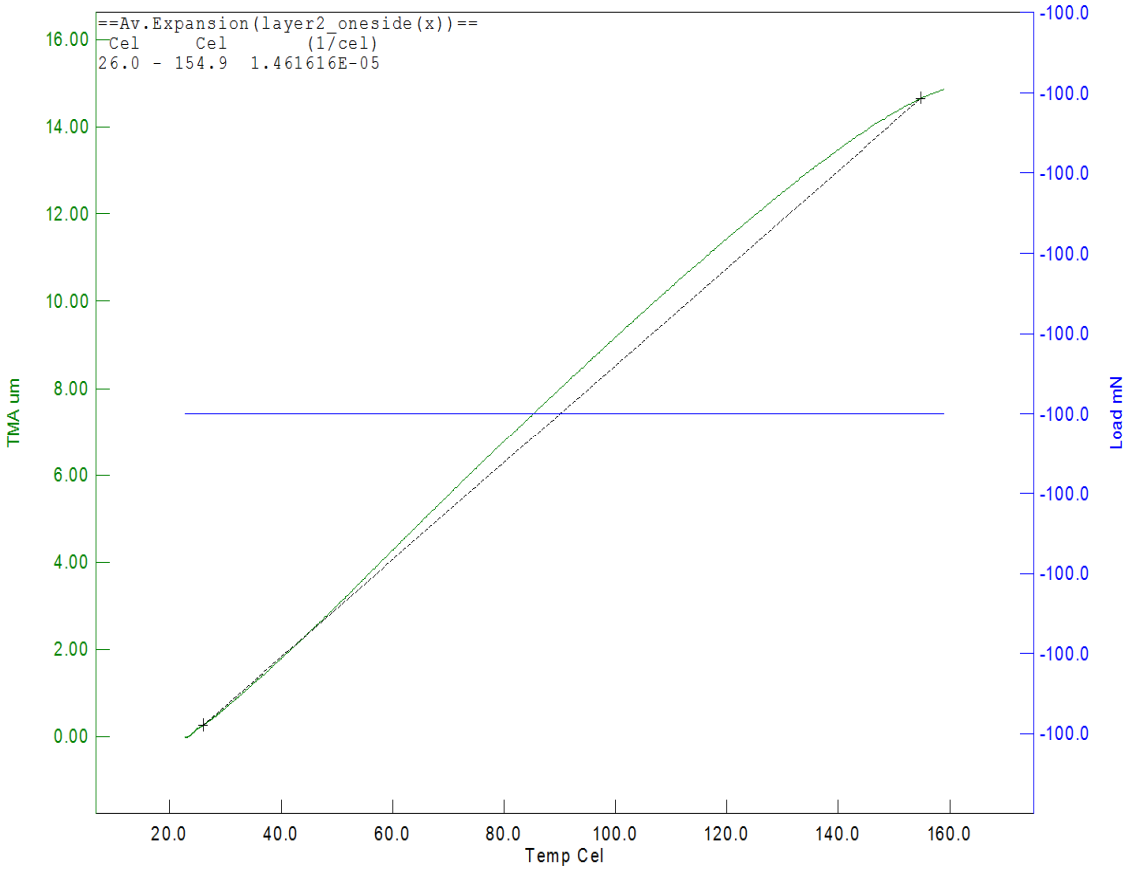


Figure 3.10 CTE in x-direction

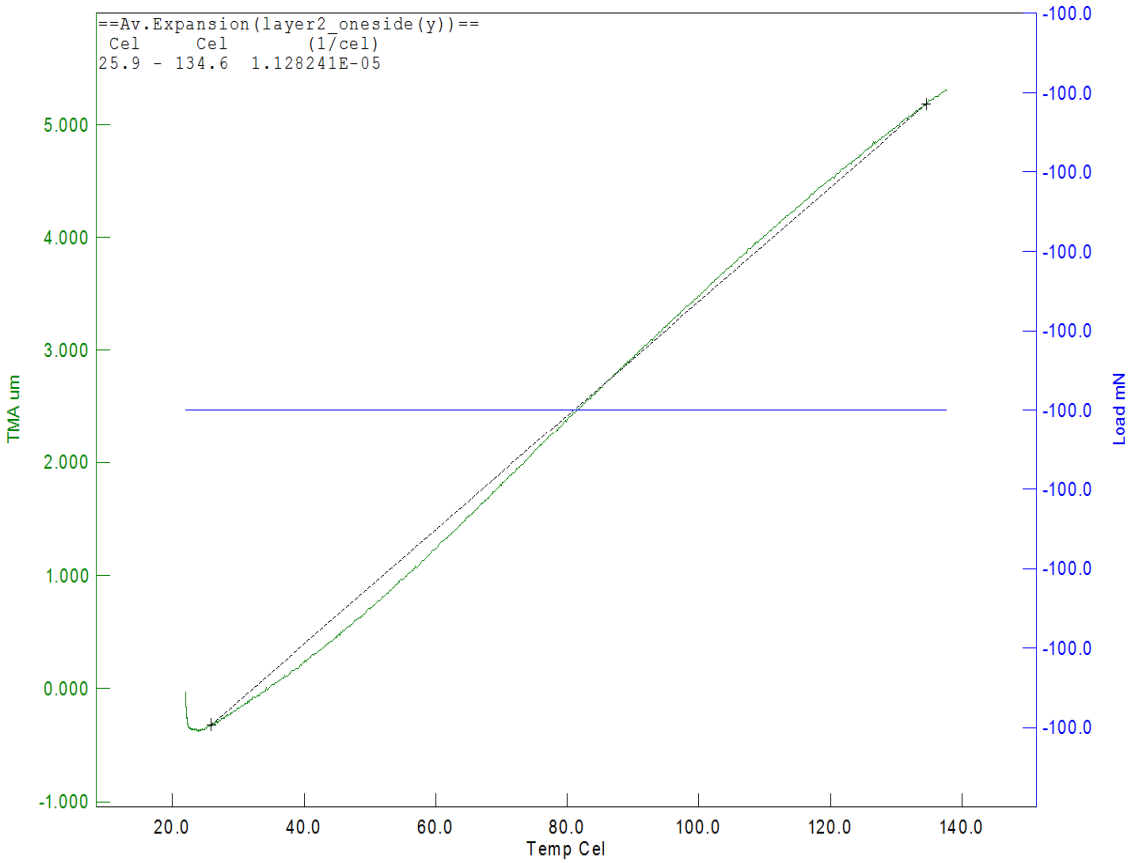


Figure 3.11 CTE in y-direction

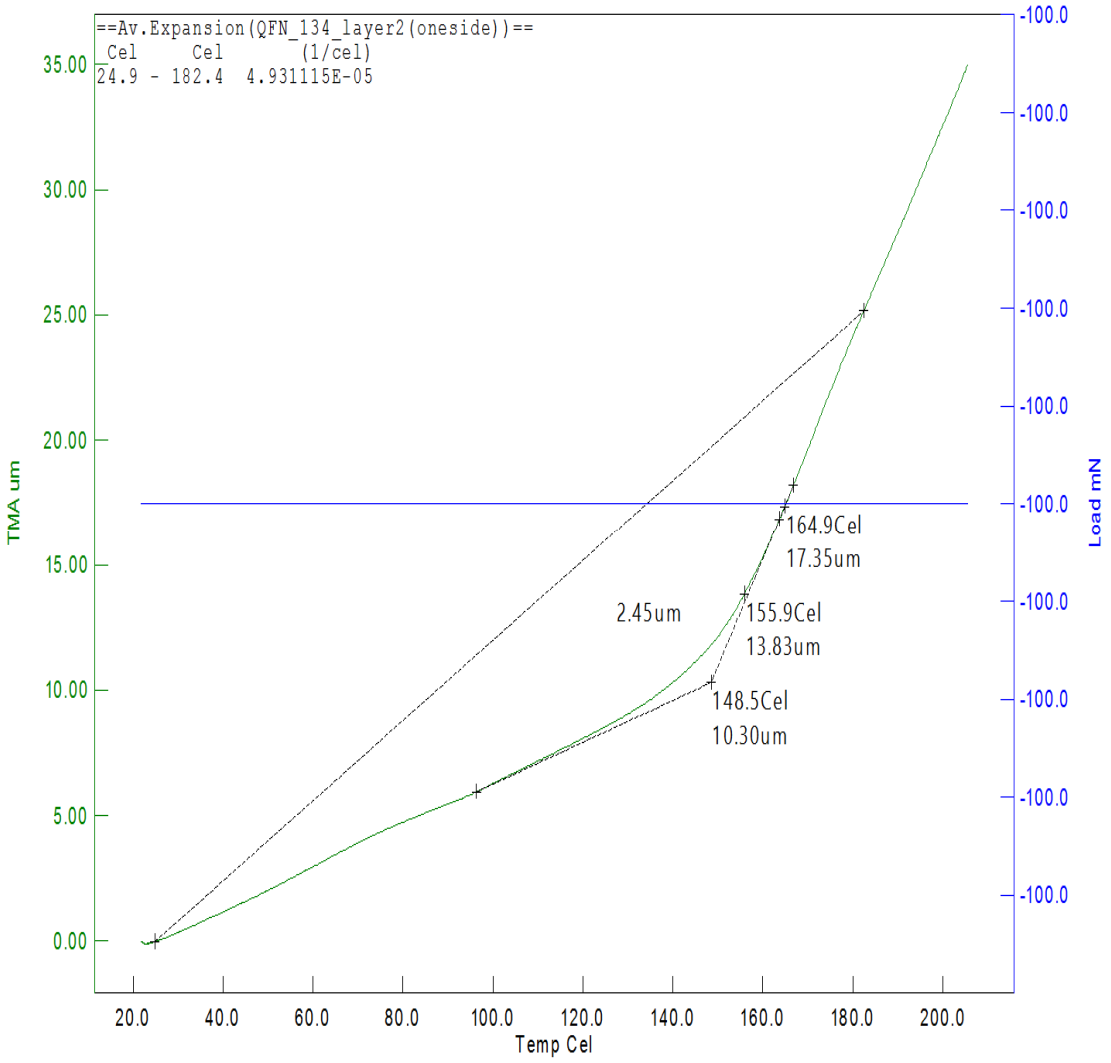


Figure 3.12 CTE and Tg in z-direction

Removed 3CU layers + 2 FR4

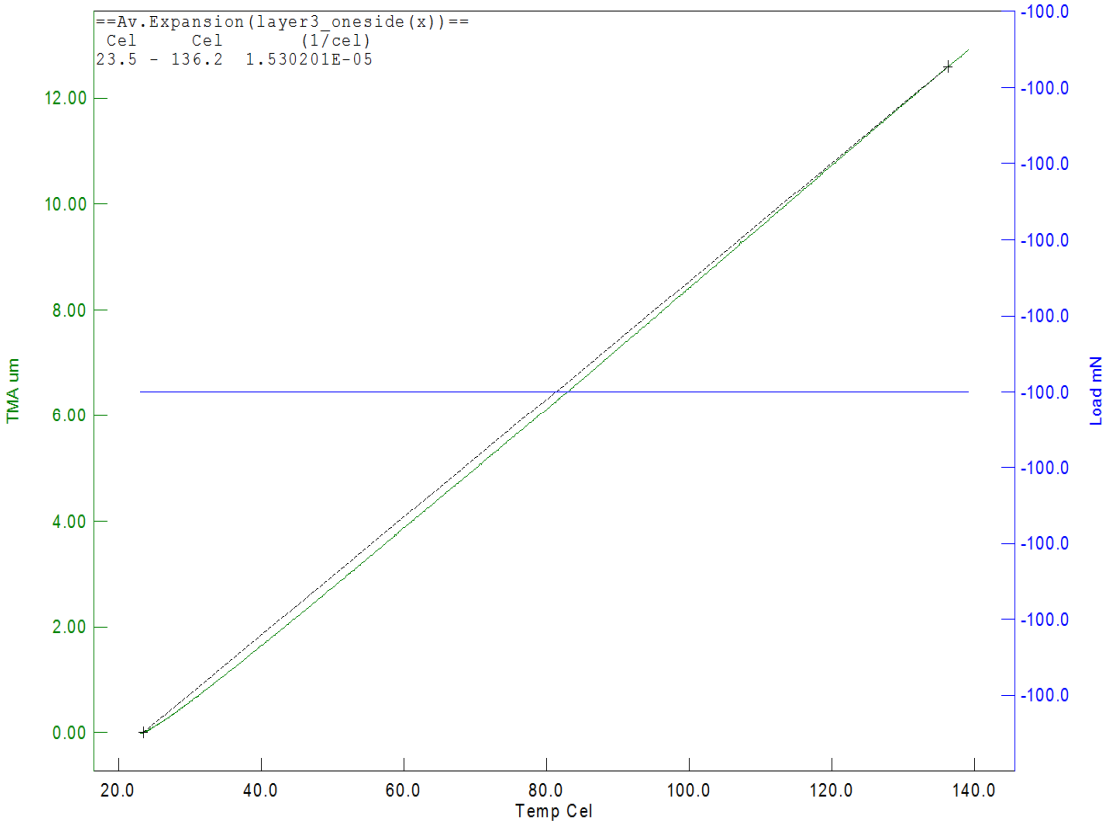


Figure 3.13 CTE in x-direction

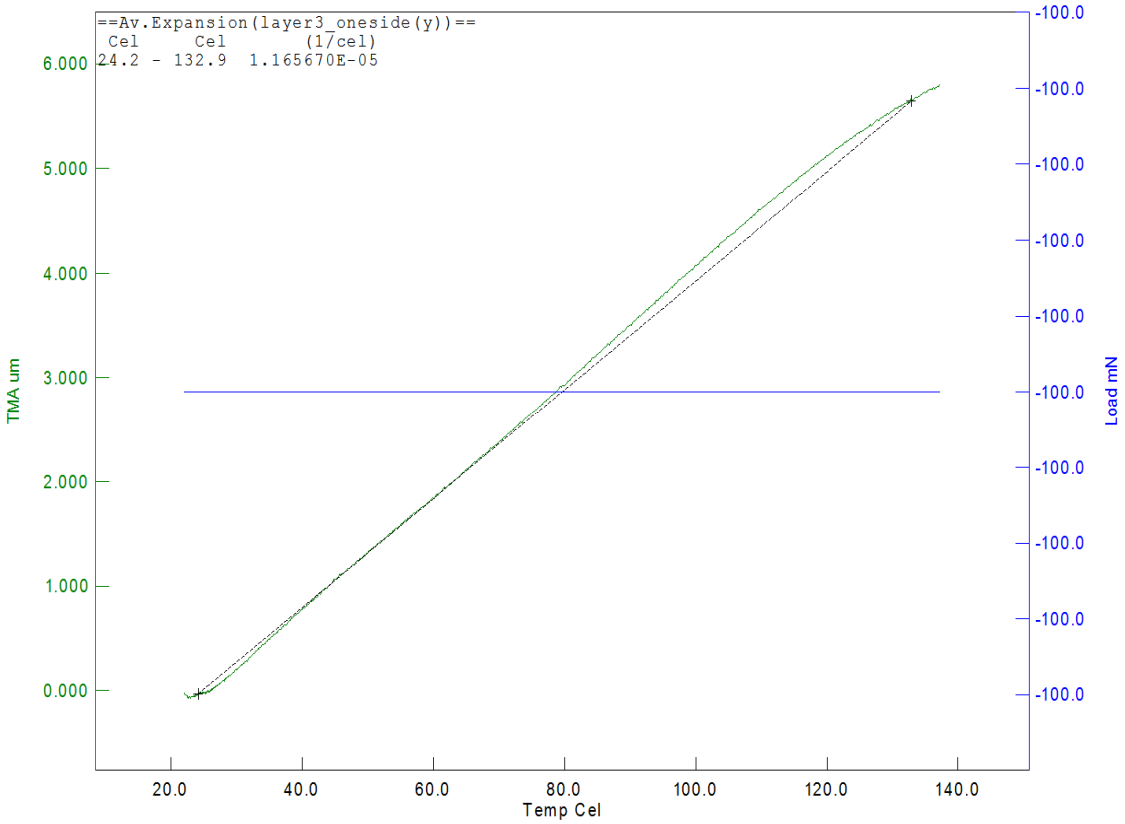


Figure 3.14 CTE in y-direction

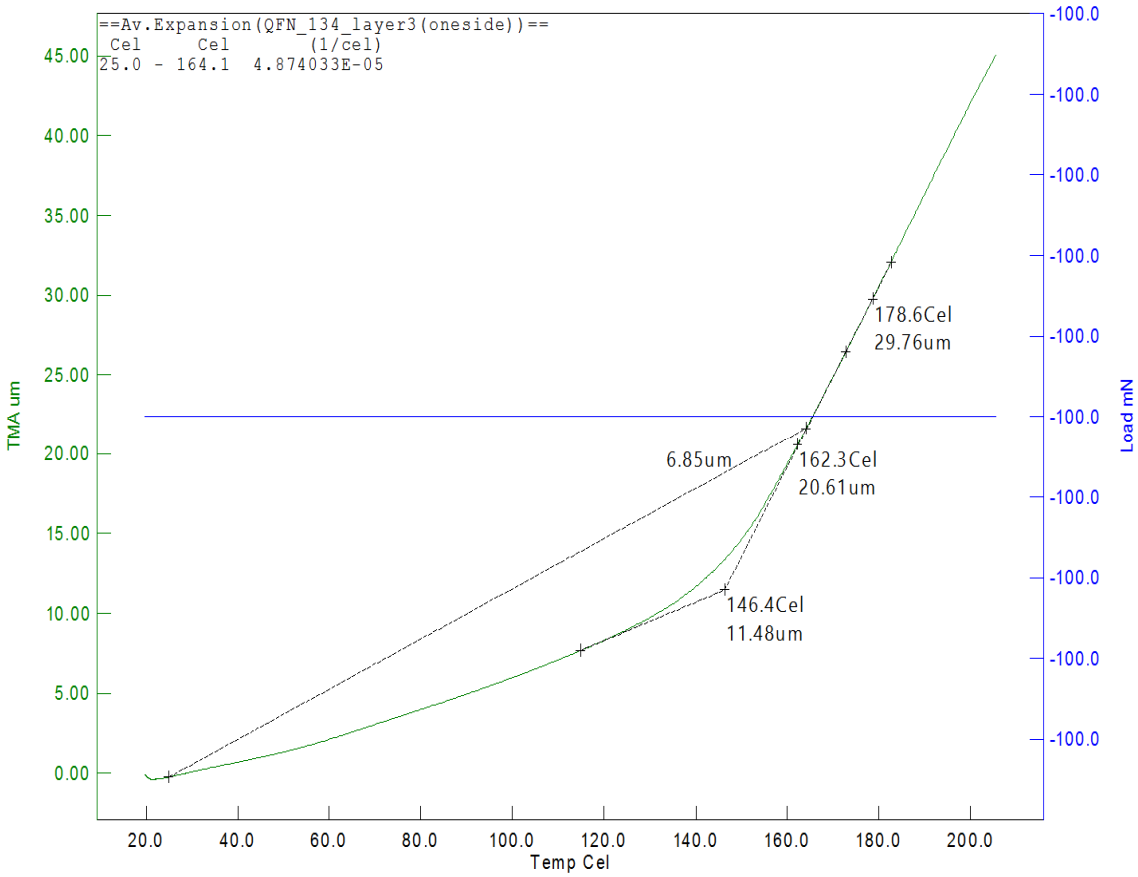


Figure 3.15 CTE and Tg in z-direction

Removed 3CU layers + 3 FR4

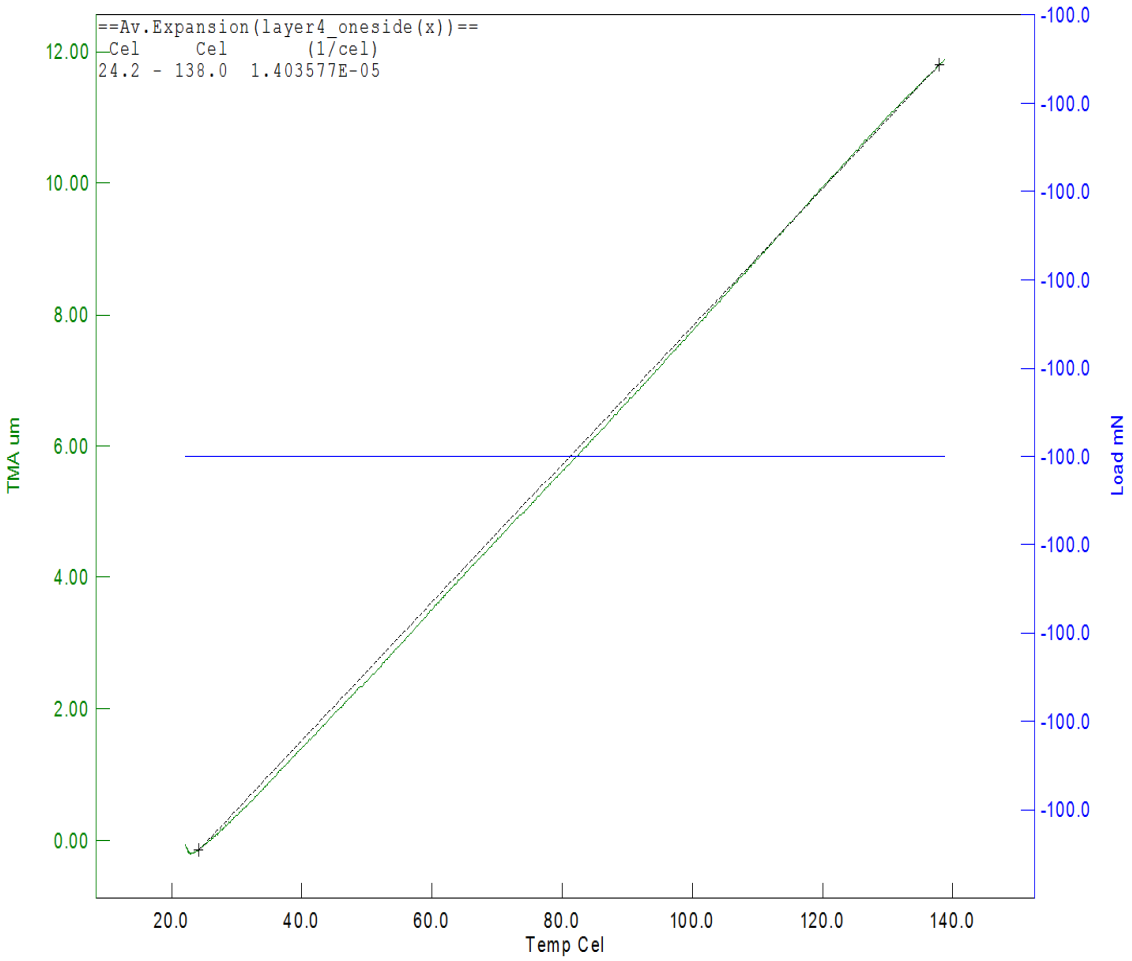


Figure 3.16 CTE in x-direction

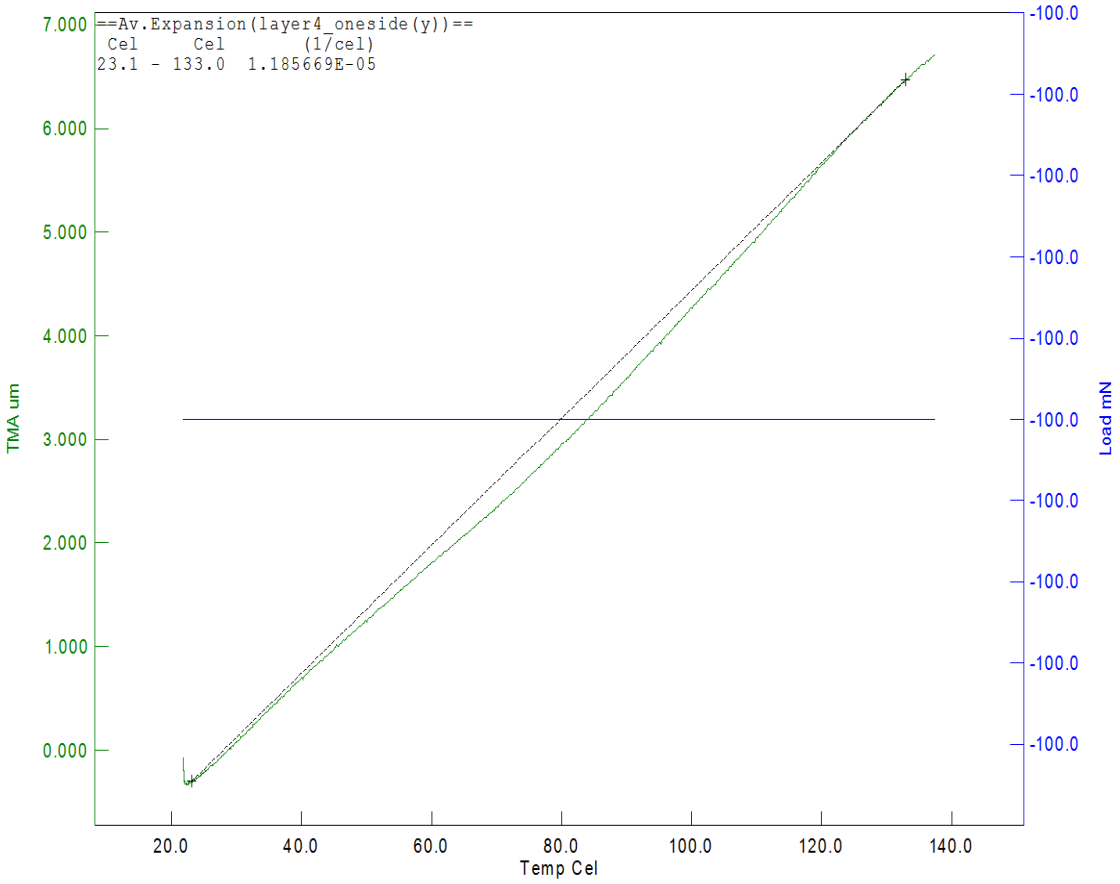


Figure 3.17 CTE in y-direction

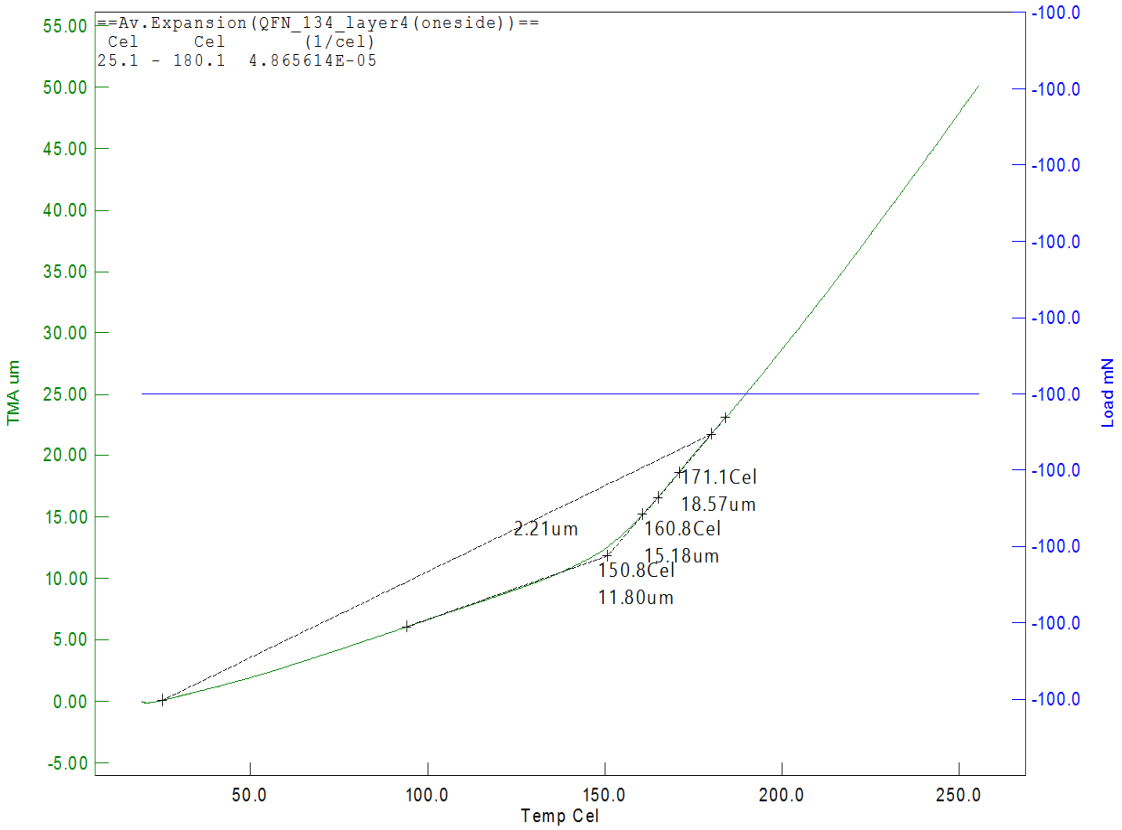


Figure 3.18 CTE and Tg in z-direction

3.4.4 Layer Removed from Both Sides

Removed 1SM + 1CU layer

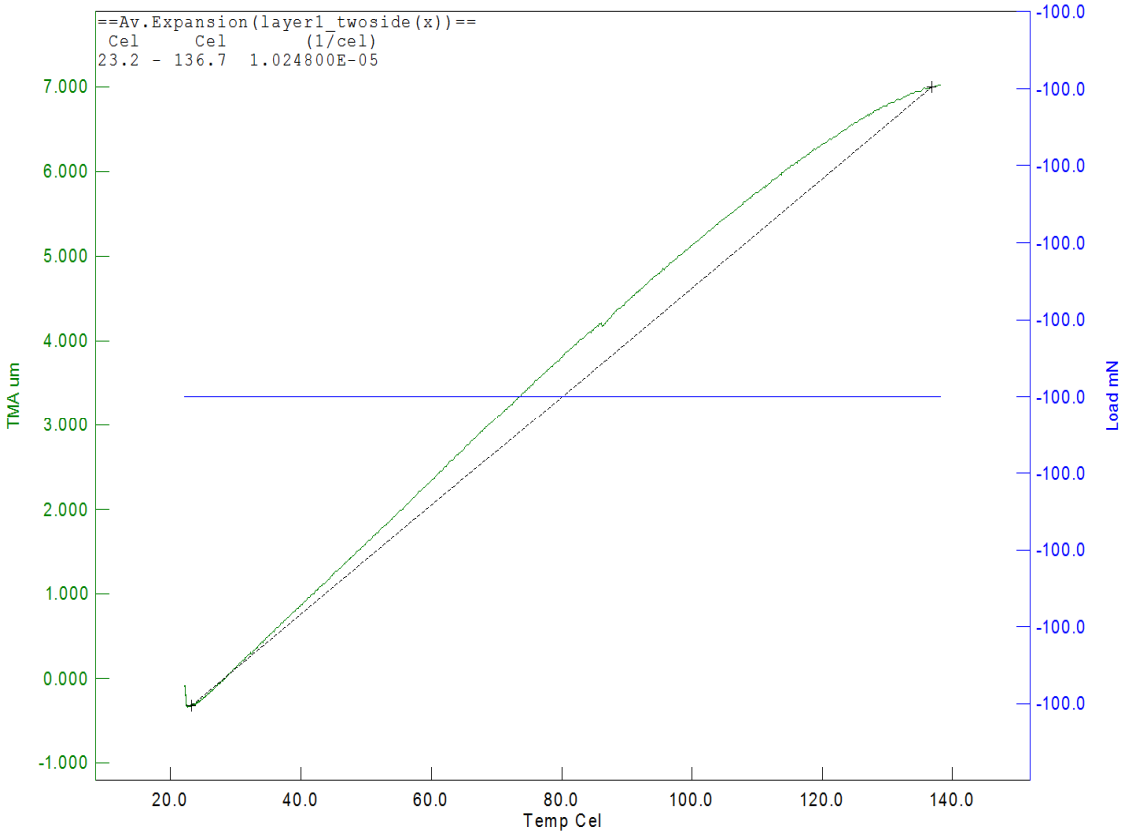


Figure 3.19 CTE in x-direction

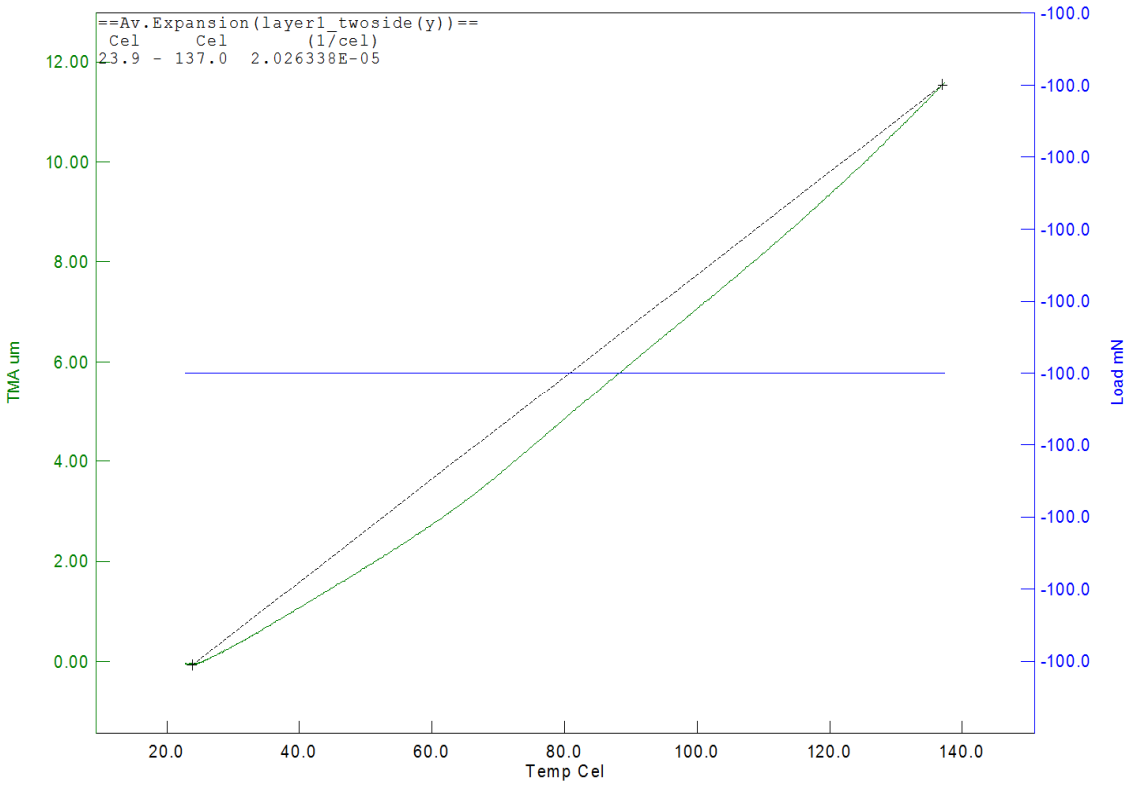


Figure 3.20 CTE in y-direction

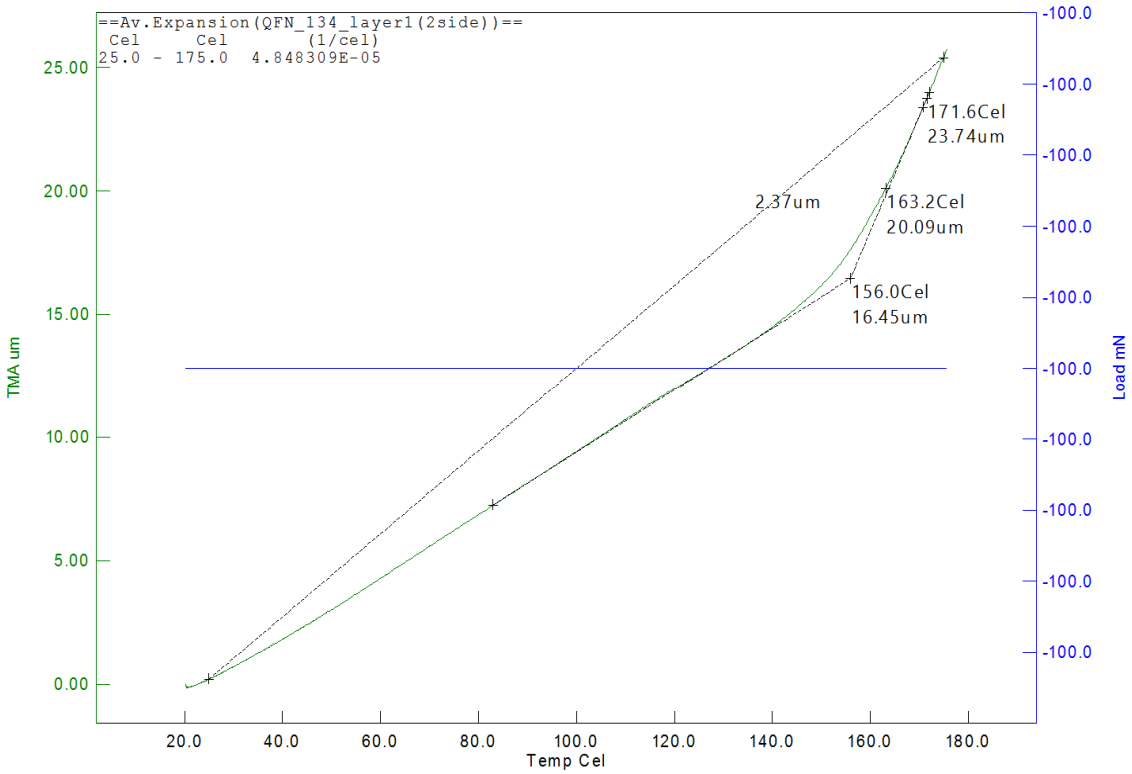


Figure 3.21 CTE and Tg in Z-direction

Removed 2CU layers + 2 FR4

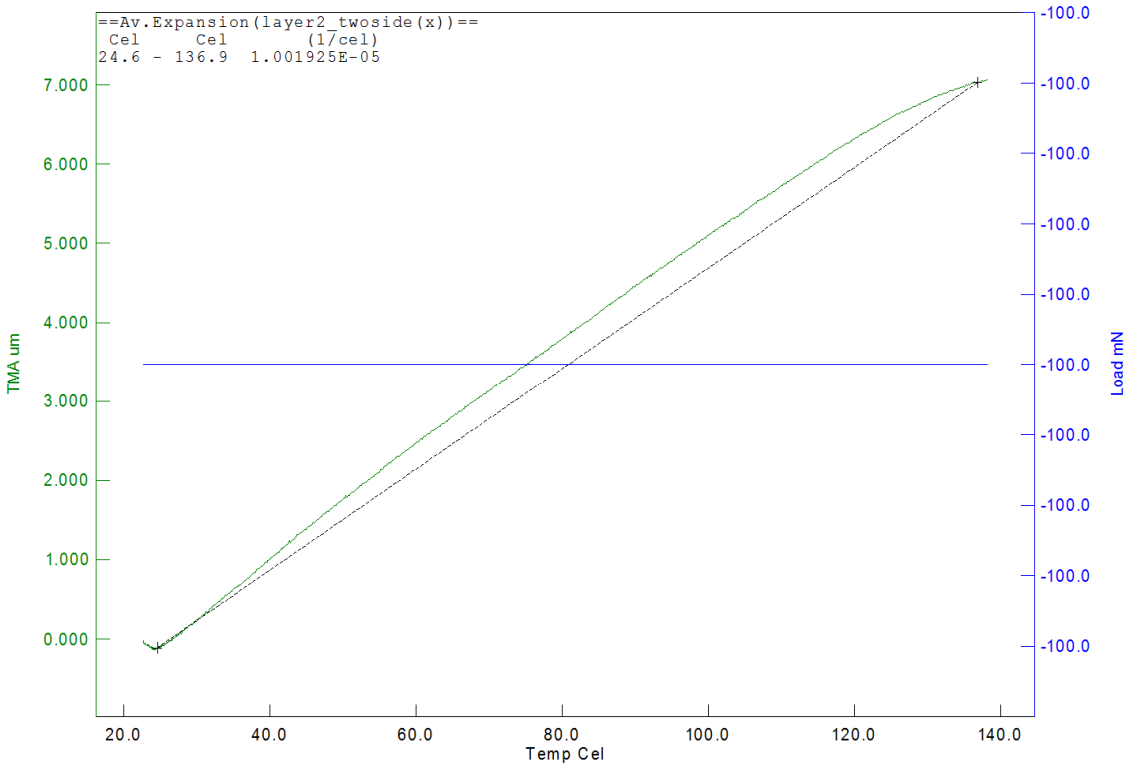


Figure 3.22 CTE in x-direction

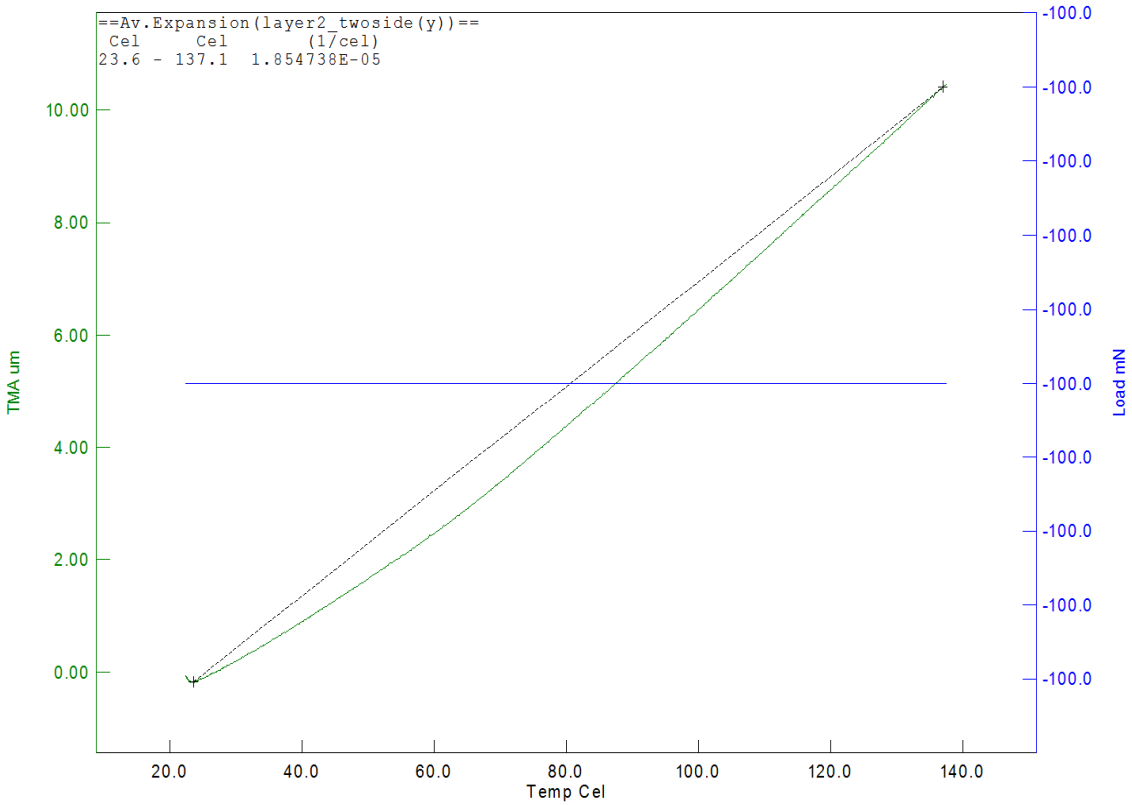


Figure 3.23 CTE in y-direction

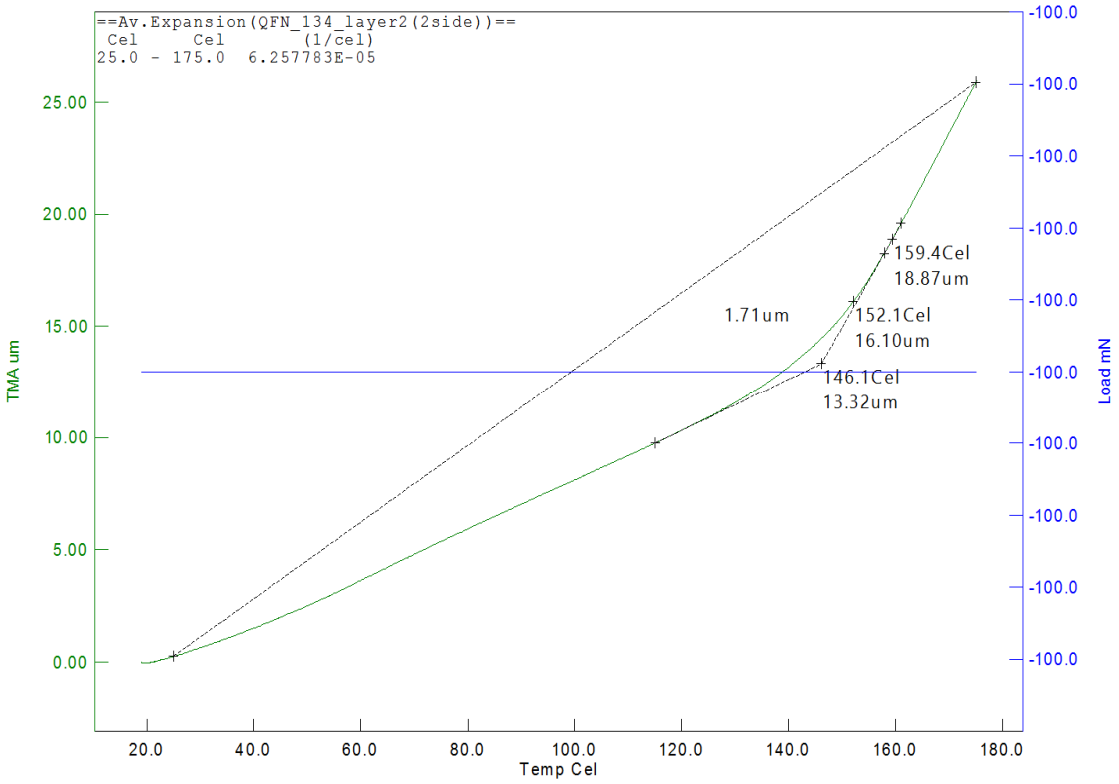


Figure 3.24 CTE and Tg in z-direction

Removed 3CU layers + 2 FR4

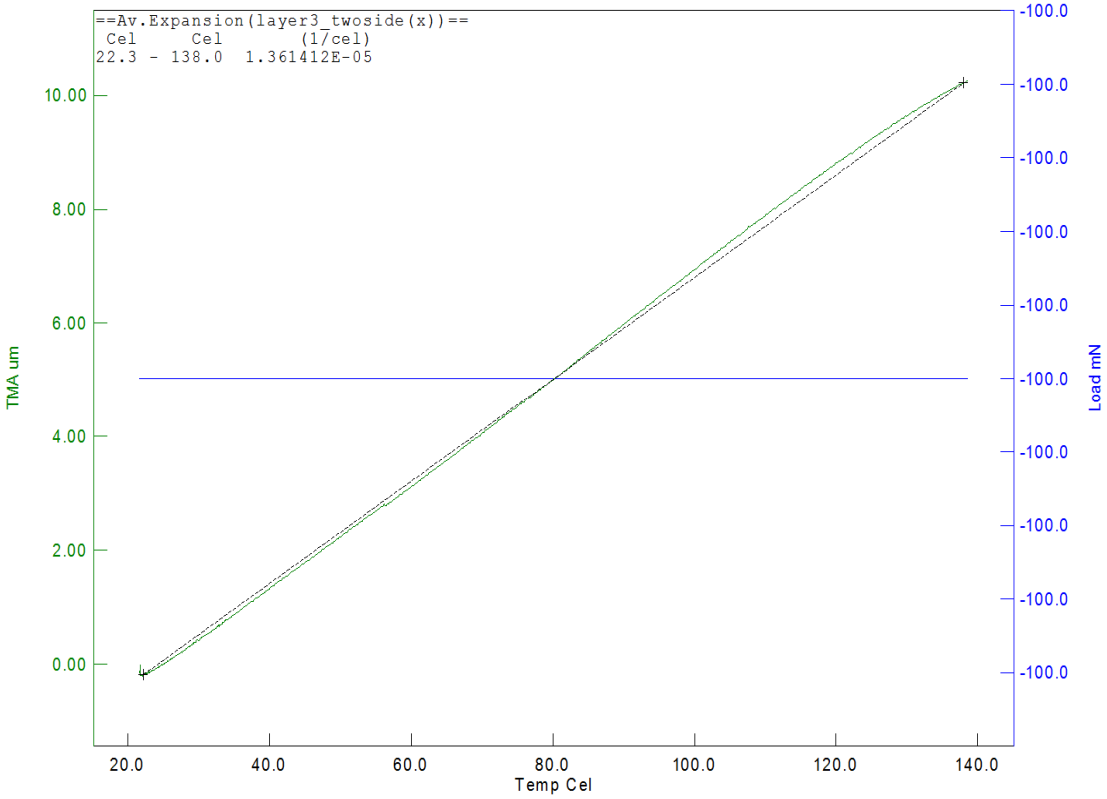


Figure 3.25 CTE in x-direction

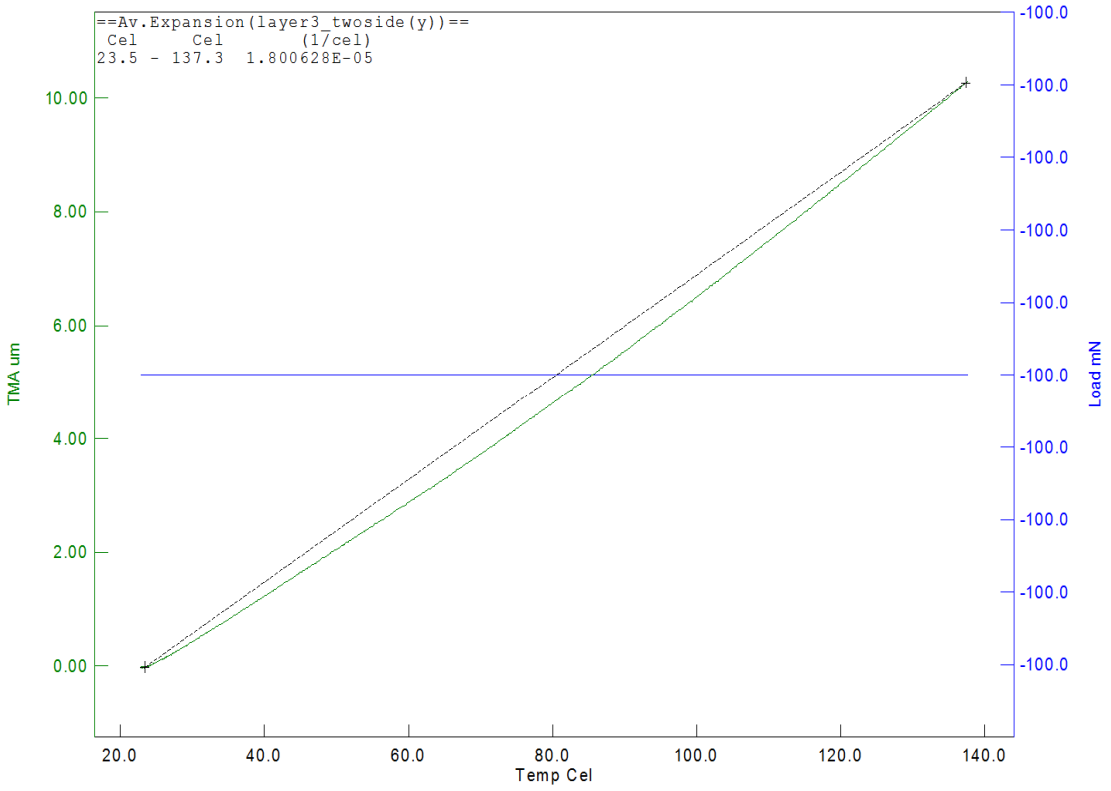


Figure 3.26 CTE in y-direction

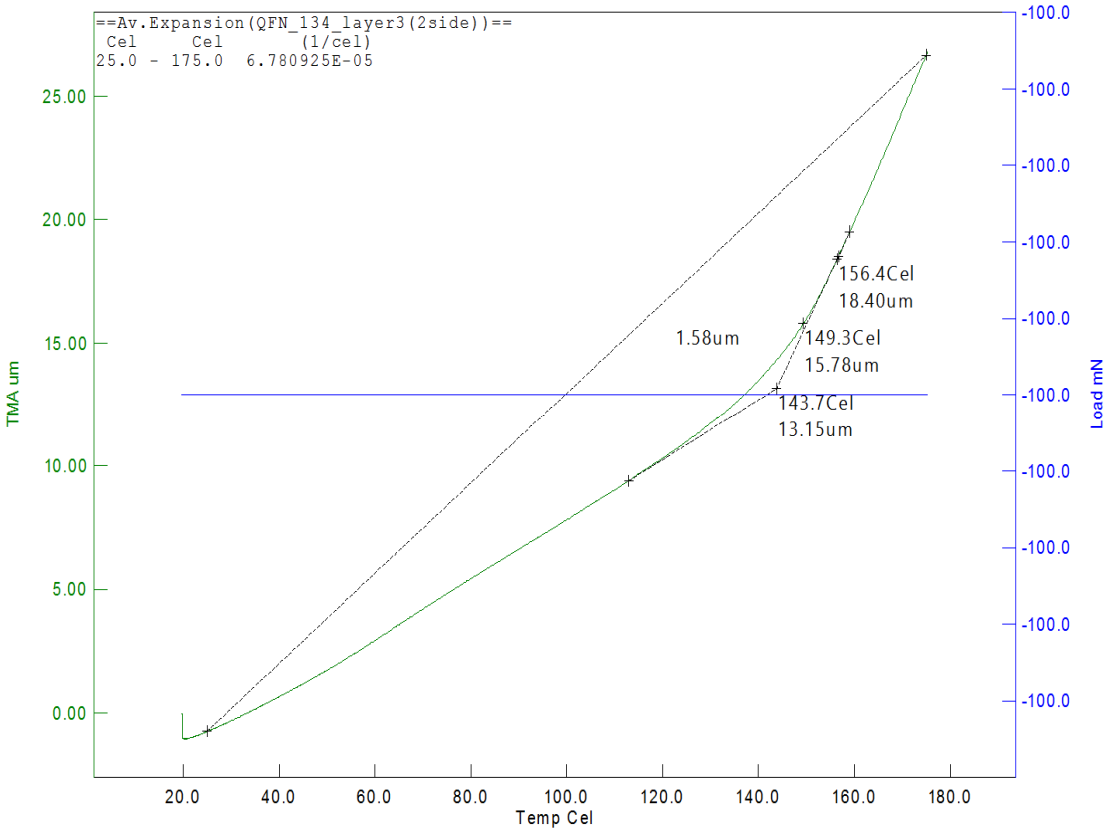


Figure 3.27 CTE and Tg in z-directon

Removed 3CU layers + 3 FR4

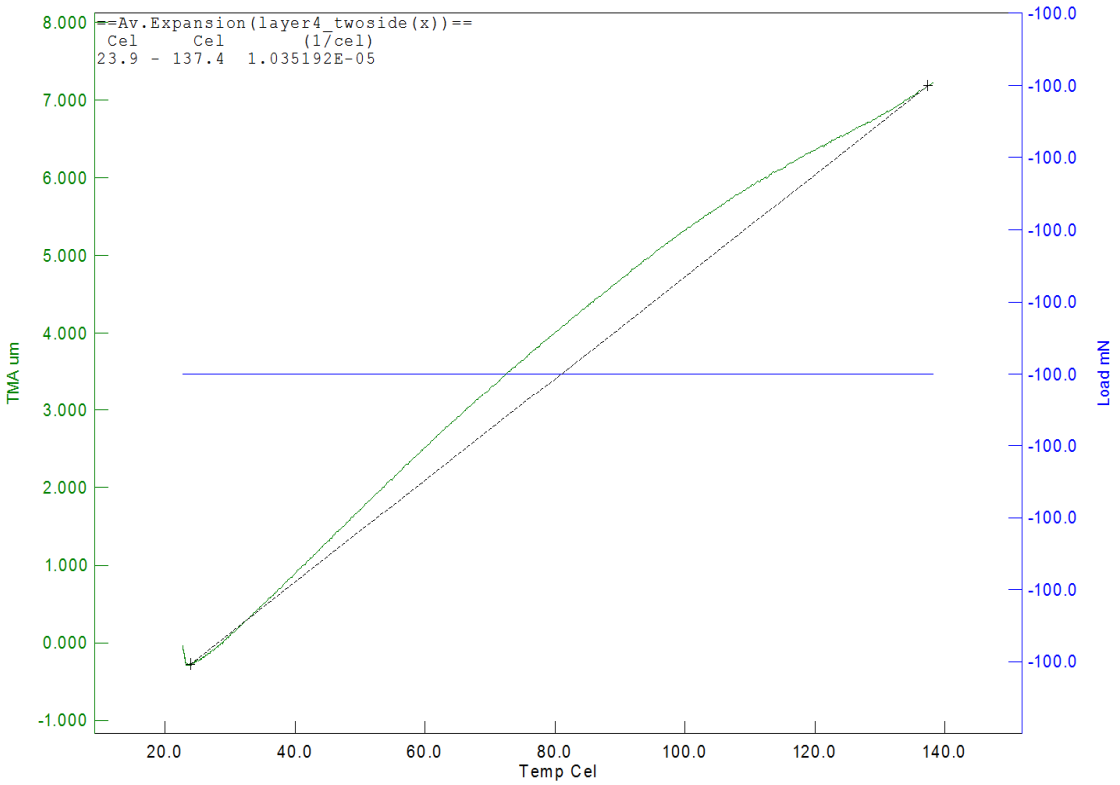


Figure 3.28 CTE in x-direction

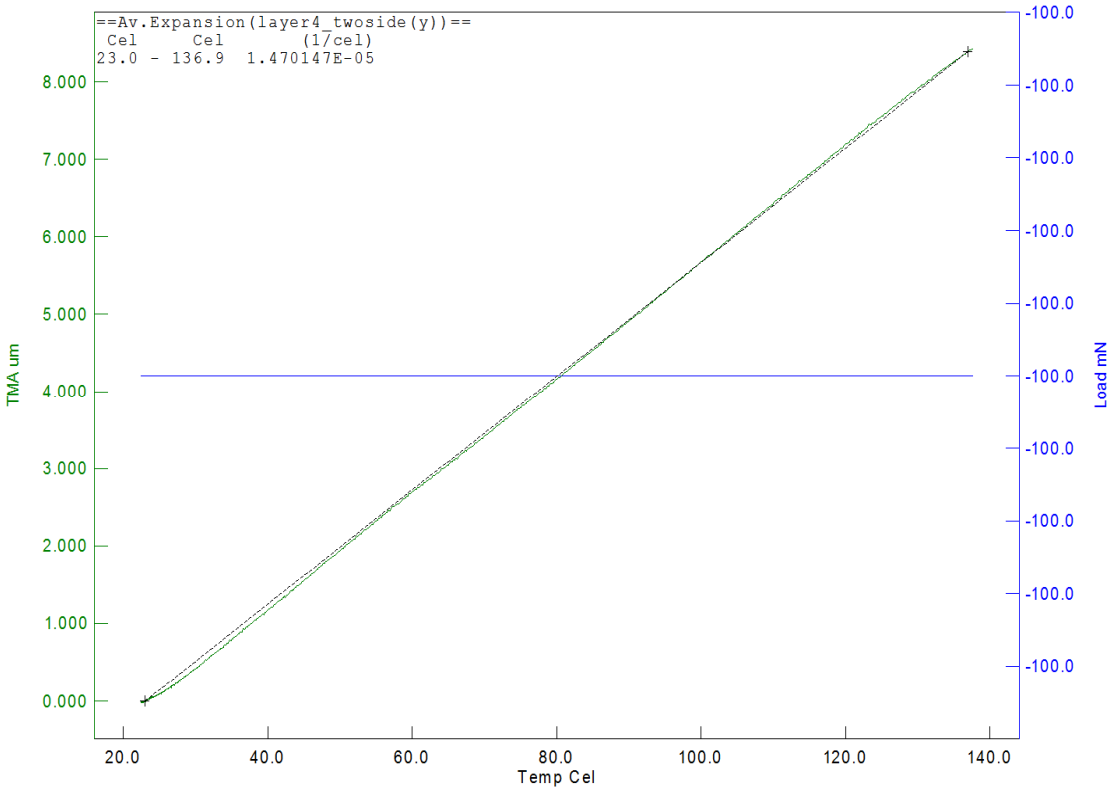


Figure 3.29 CTE in y-direction

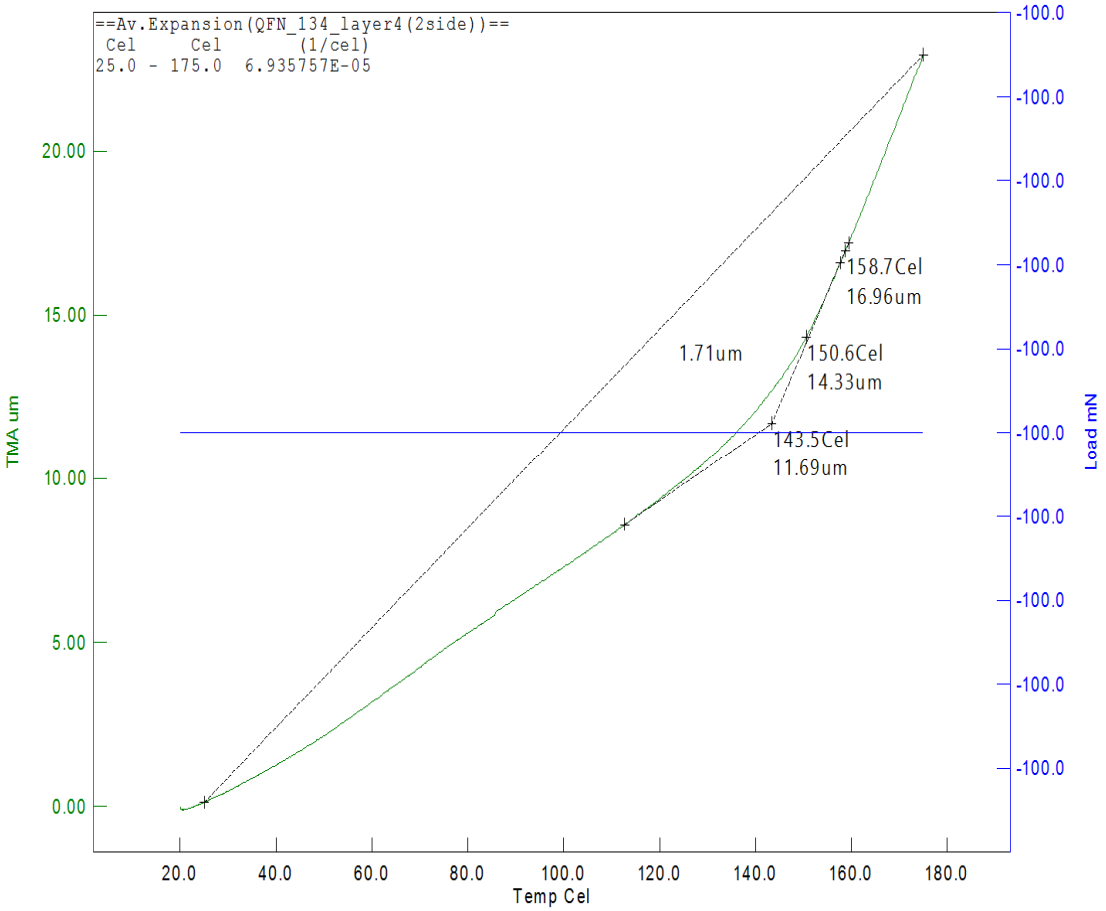


Figure 3.30 CTE and Tg in z-direction

3.4.5 Tabulated CTE and Tg Results from TMA

Table 3.1 Tabulated Results of CTE and Tg

QFN_134mil Board CTE Results from TMA				
No Layer Removed (whole board)	CTE ppm/°C			Tg °C
	x-direction	y-direction	z-direction	z-direction
	14.8802	14.362	83.17	147.2
Layers removed on one side	CTE ppm/°C			
	x-direction	y-direction	z-direction	
Removed 1SM+1CU layer	11.8714	18.4455	69.1588	147.4
Removed 2CU layers +2FR4	14.6161	11.2824	49.3111	148.5
Removed 3CU layers + 2FR4	15.3020	11.6567	48.7403	149.4
Removed 3CU layers + 3FR4	14.0358	11.8566	48.6561	150.8
Layers removed on both sides	CTE ppm/°C			
	x-direction	y-direction	z-direction	
Removed 1SM + 1CU layer	10.8400	20.2634	48.4831	156.0
Removed 2CU layers + 2FR4	10.0193	18.5474	62.5778	146.1
Removed 3CU layers + 2FR4	13.6141	18.0063	67.8093	143.7
Removed 3CUlayers + 3FR4	10.3519	14.7015	69.3575	143.5

3.5 Dynamic Mechanical Analysis – Storage and Loss Modulus Measurement

Dynamic Mechanical Analysis (DMA) is a technique which is used widely to characterize material's properties as a function of temperature, time, frequency, stress, atmosphere or a combination of these parameters. DMA works by applying a sinusoidal deformation to a sample of known geometry. A force motor is used to generate the sinusoidal wave and this is transmitted to the sample through a drive shaft. DMA measures damping and stiffness, these are reported as modulus and tan delta. Since we are applying a sinusoidal force, we can express the modulus as an in-phase component, the storage modulus (E'), and an out of phase component, the loss modulus (E"). The storage modulus is the elastic response of the sample and the loss modulus is the viscous response of the sample. Tan delta is the ratio of the loss to the storage modulus and is often called as damping [11].

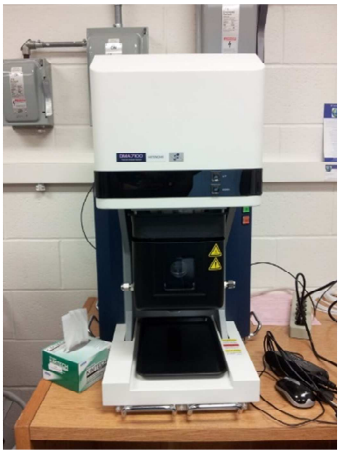


Figure 3.31 DMA 7000

The DMA 7000 which is used for this project is one of the most flexible, cost-effective instruments available in the market. The test sample which is QFN 134mil is placed in the holder with a Bending probe with the test settings being as follows-

- Start and End limit Temperatures - +20°C to +180°C
- Ramp Input of 2°C/min
- Input frequencies of- 0.5hz, 1hz, 2hz, 5hz, 10hz

The measurement test was benchmarked with Aluminum sample to gain the confidence. Tests were conducted for each case with a minimum of 5 similar samples.

3.5.1 Storage Modulus and Loss Modulus Results

The graphs of storage and loss modulus obtained from the analysis is as shown and is tabulated for further reference. For my reference I've calculated the results at 1Hz and 25°c (room temperature).

3.5.1.1 Board Level

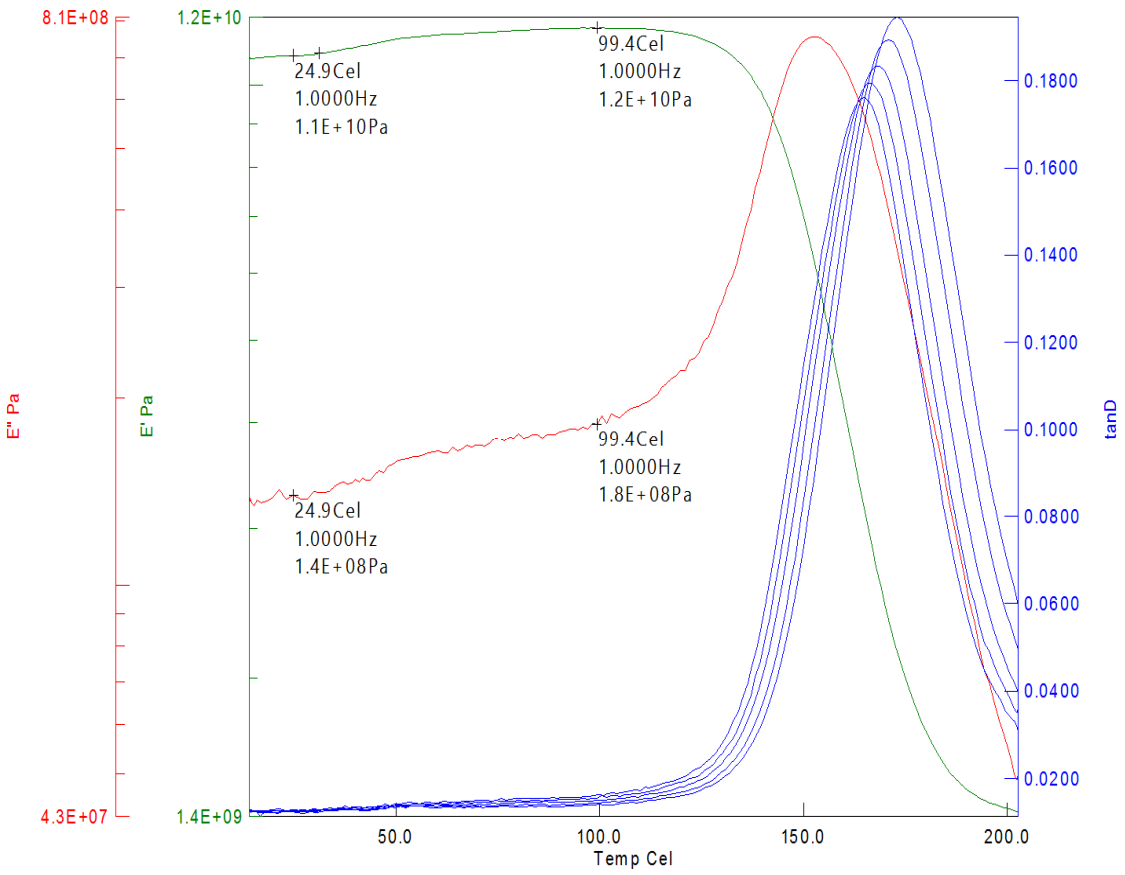


Figure 3.32 Board Level

3.5.1.2 Layer Removed from One Side

Removed 1SM + 1CU layer

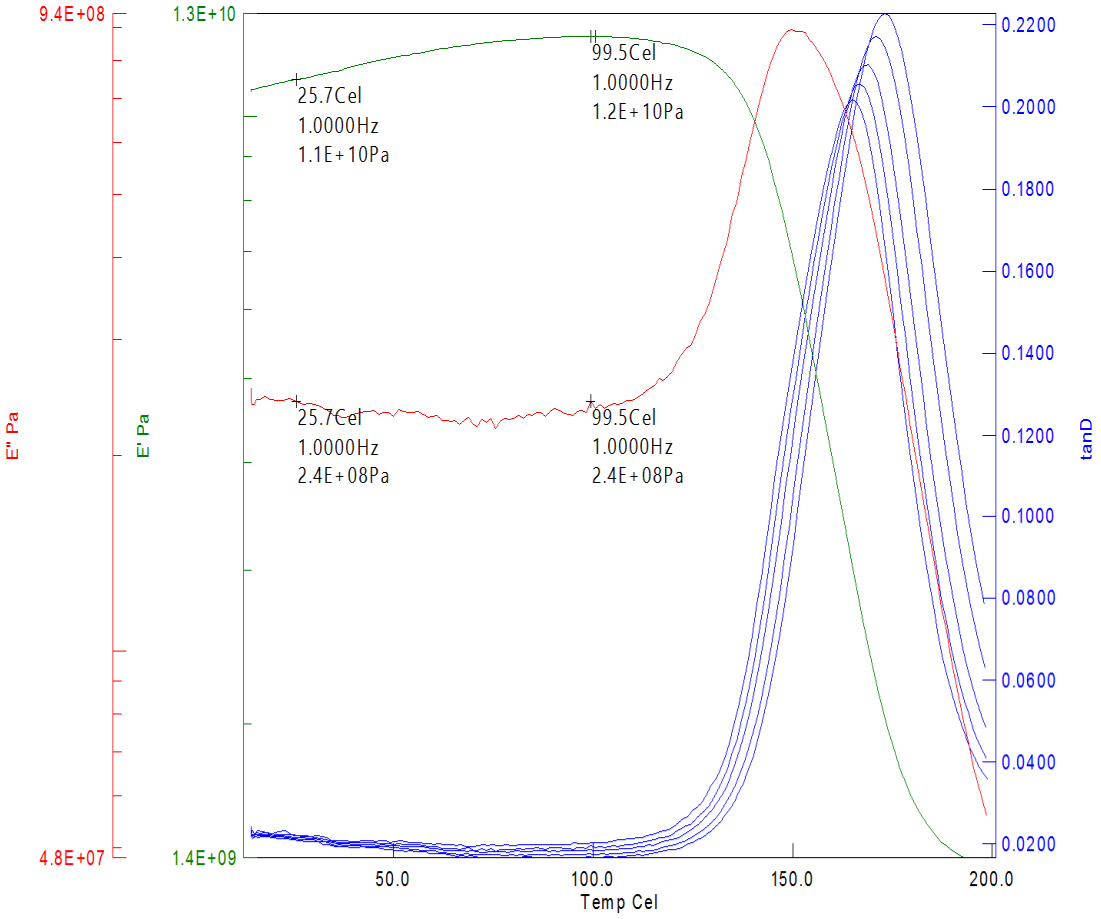


Figure 3.33 Layer-1

Removed 2CU layers + 2 FR4

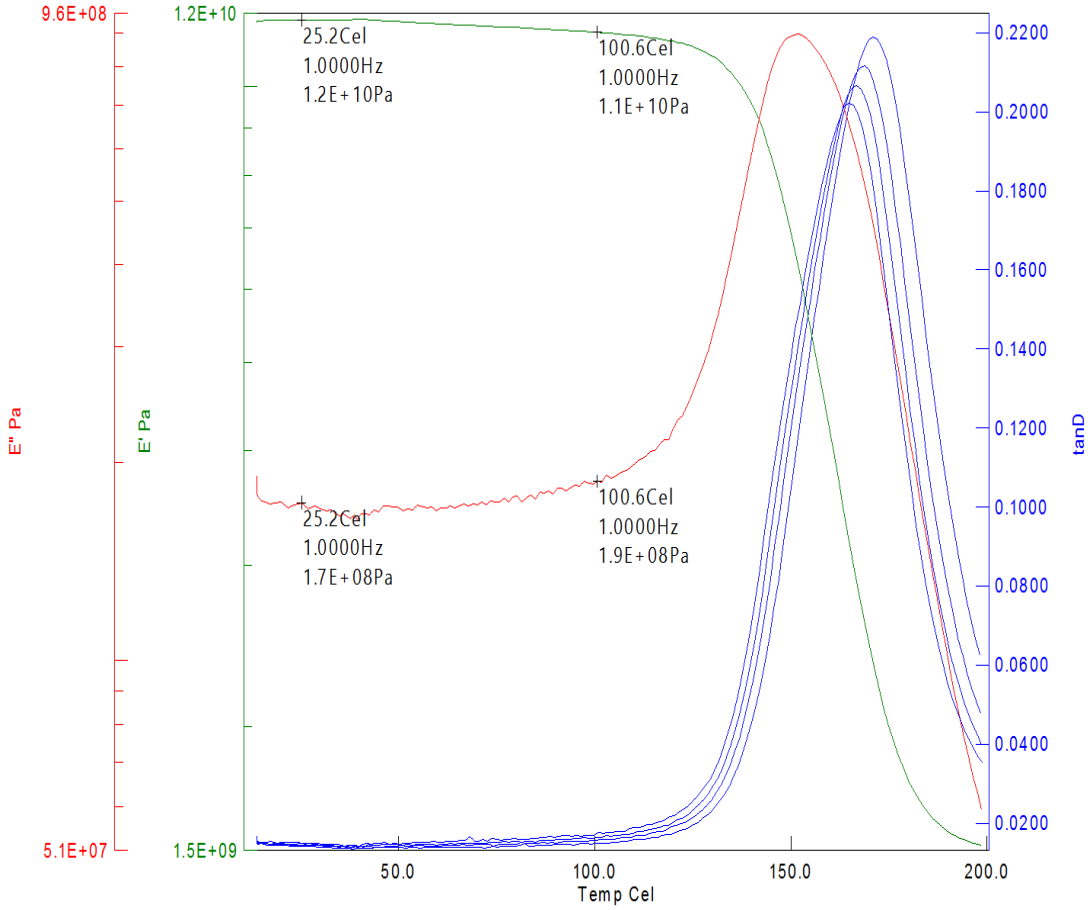


Figure 3.34 Layer-2

Removed 3 CU layers + 2 FR4

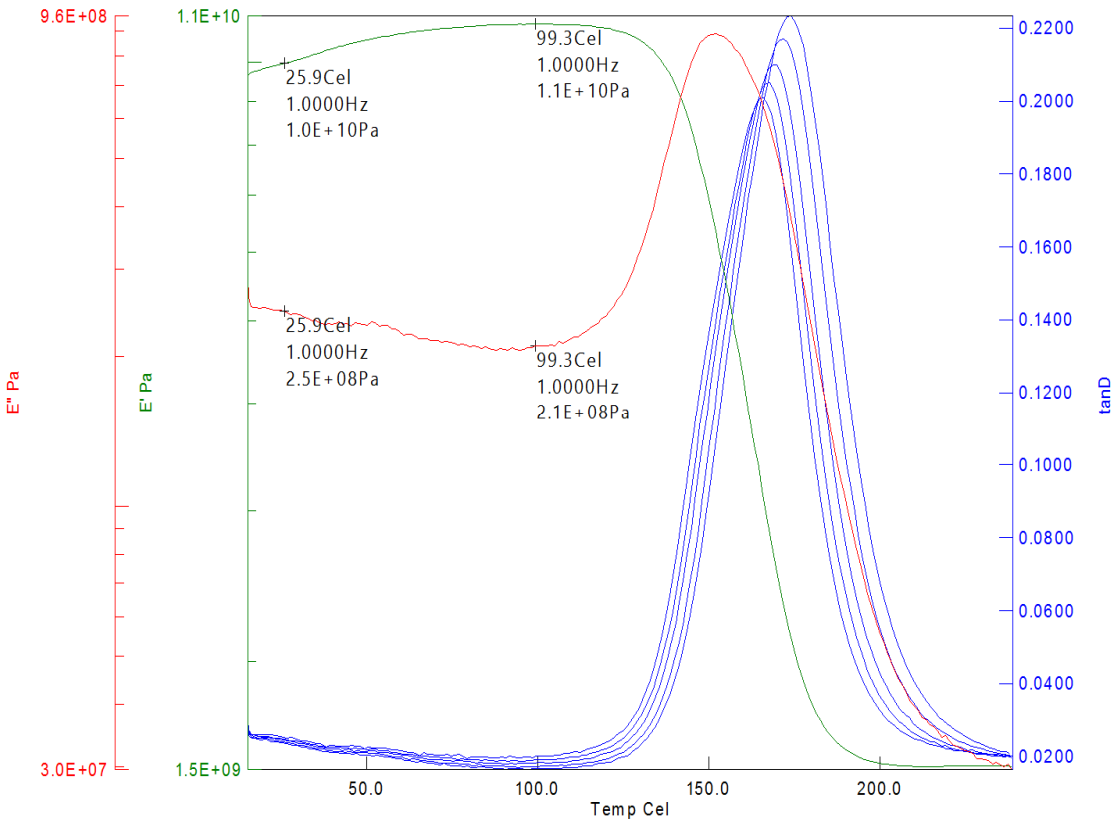


Figure 3.35 Layer – 3

Removed 3 CU layers + 3 FR4

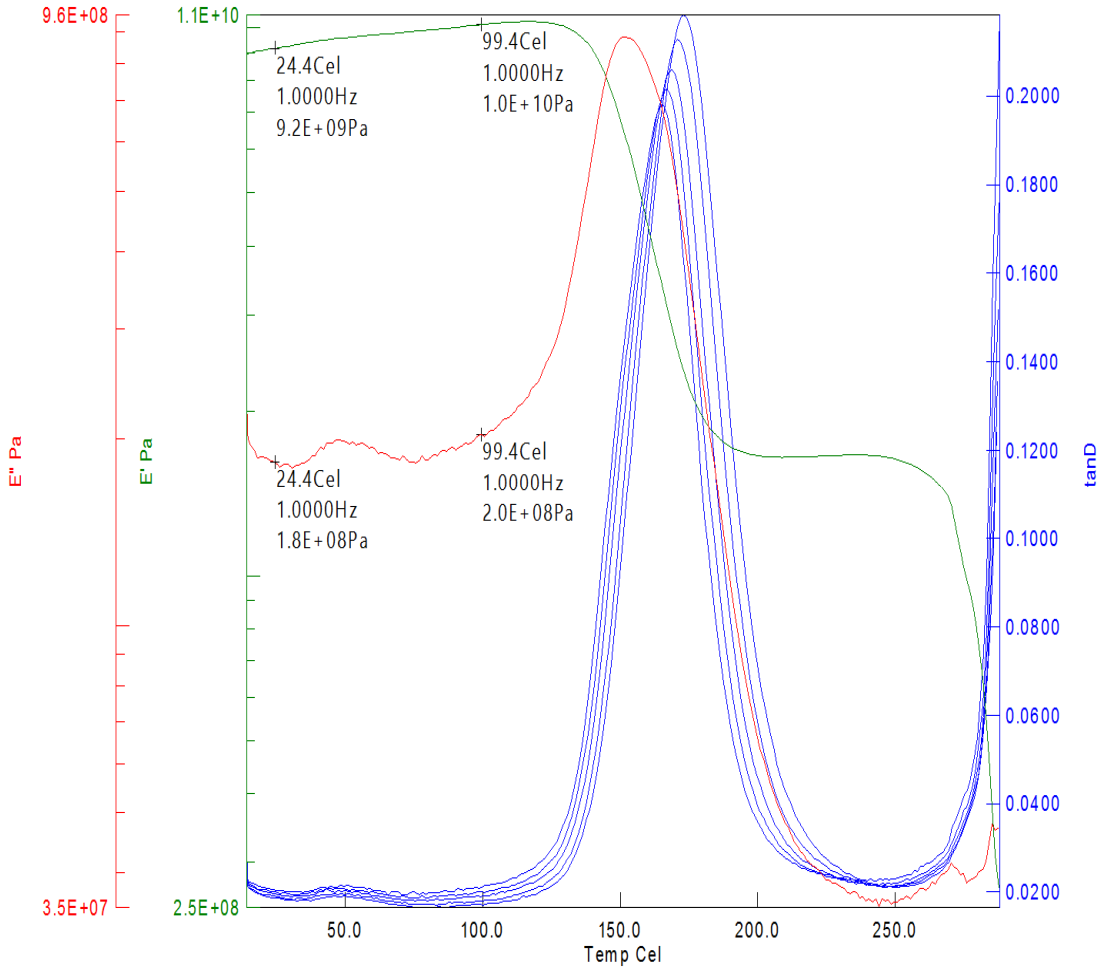


Figure 3.36 Layer – 4

3.5.1.3 Layers Removed from Both Sides

Removed 1SM + 1CU layer

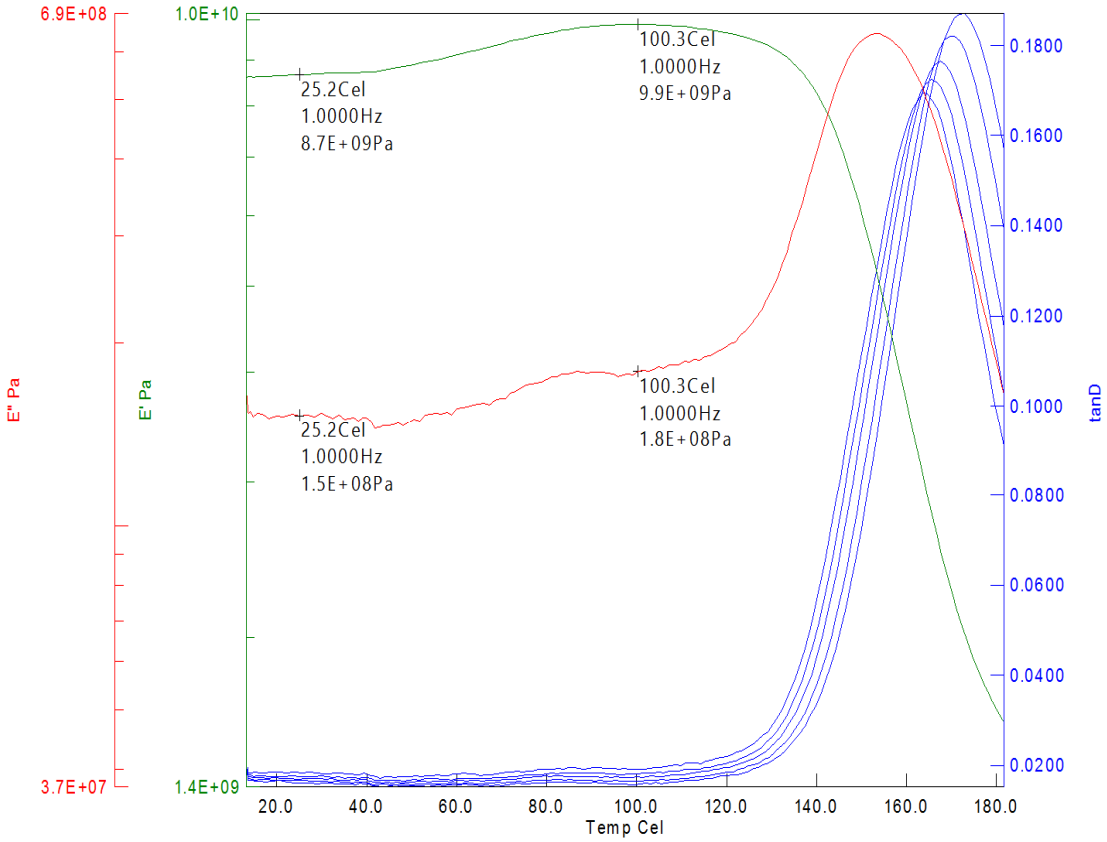


Figure 3.37 Layer-1

Removed 2CU layers + 2 FR4

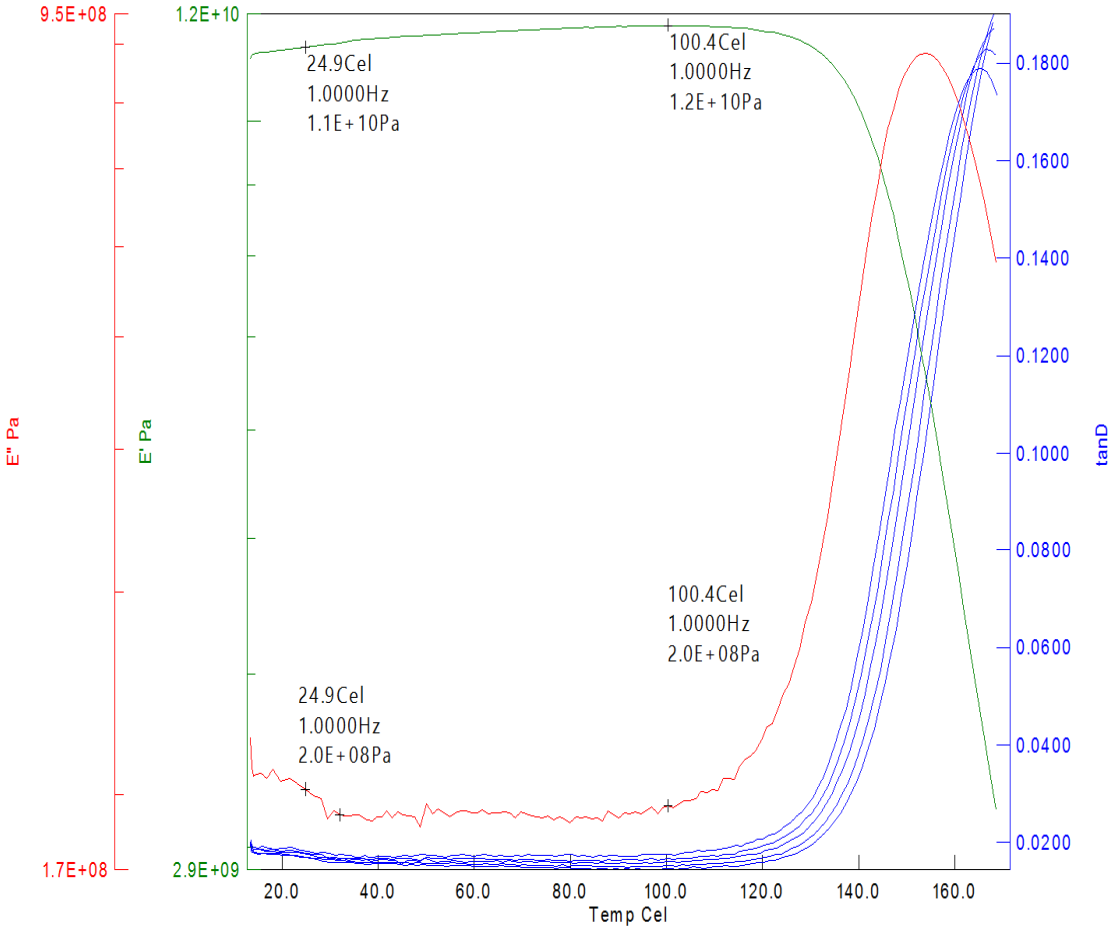


Figure 3.38 Layer – 2

Removed 3CU layers + 2 FR4

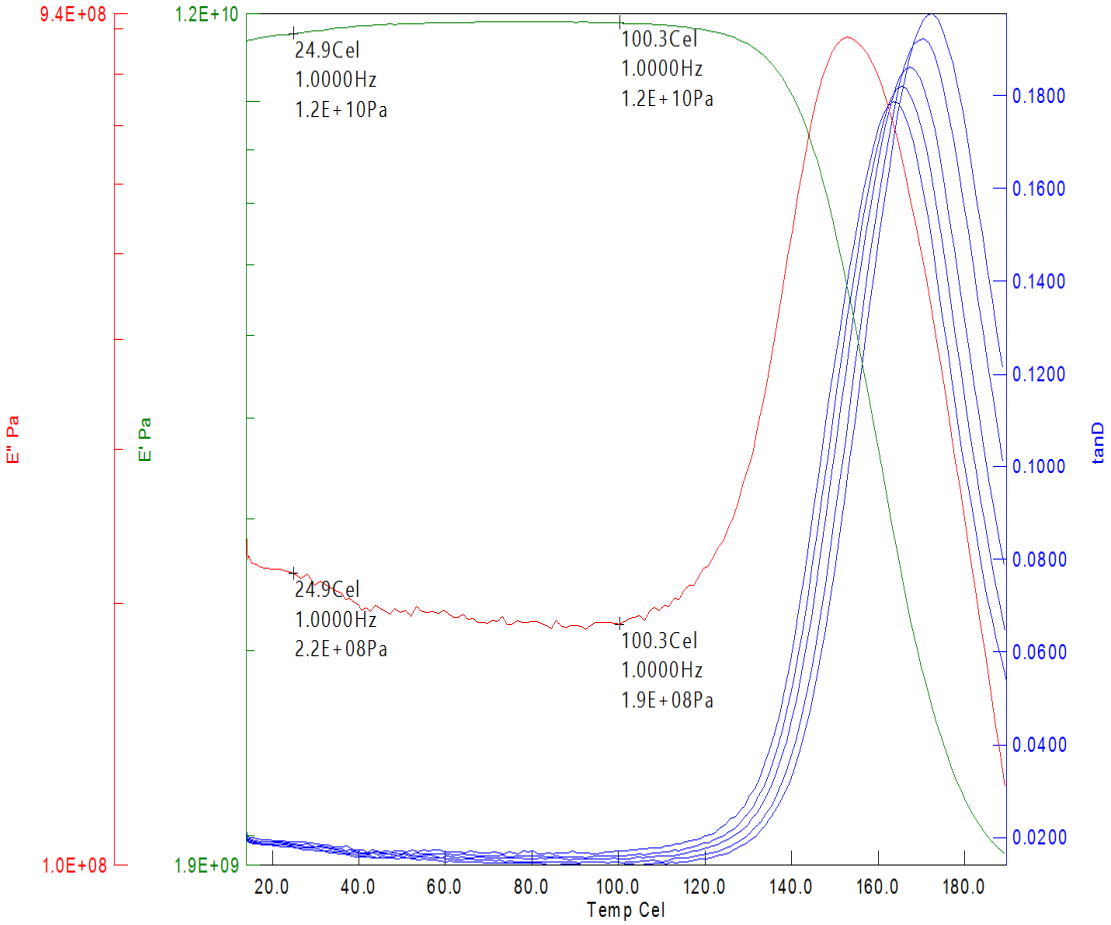


Figure 3.39 Layer – 3

Removed 3CU layers + 3 FR

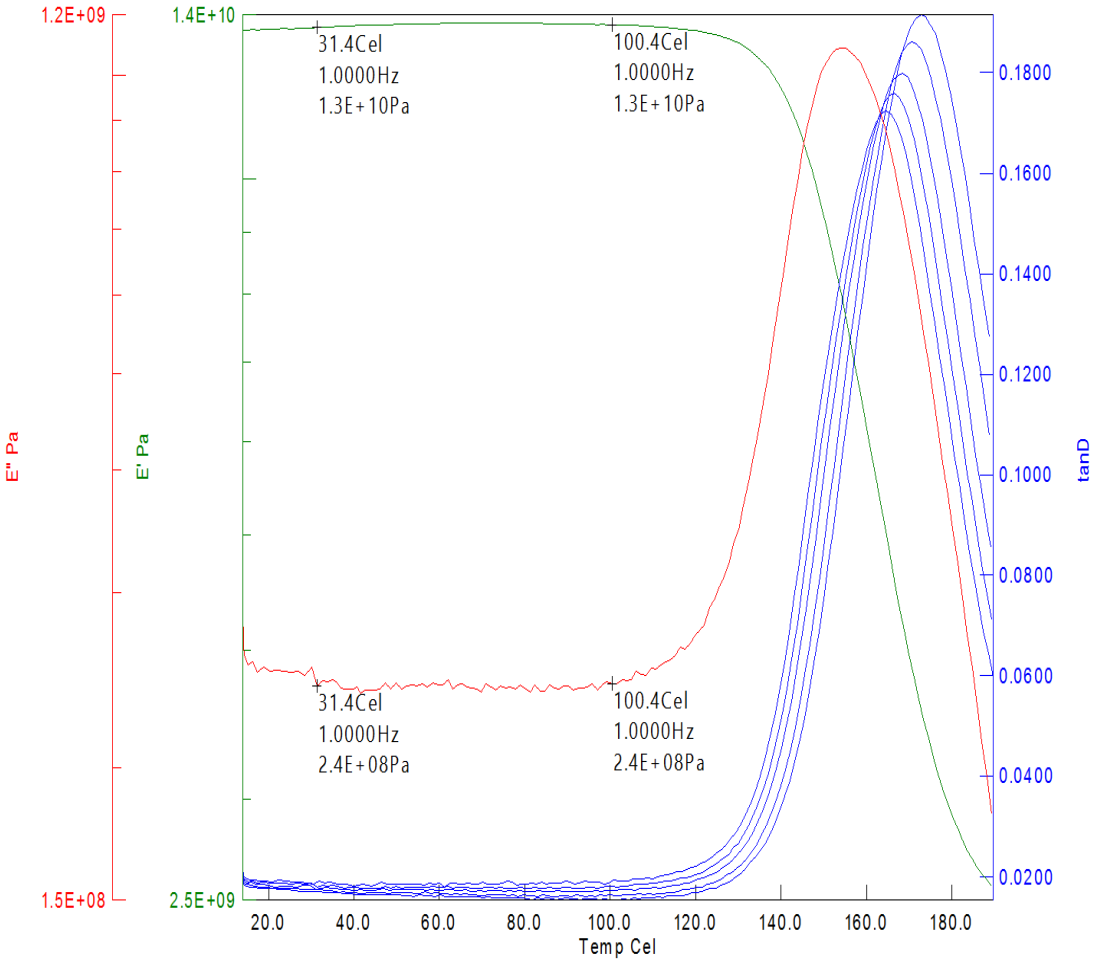


Figure 3.40 Layer – 4

3.5.2 Tabulated Results of Storage and Loss Modulus from DMA

Table 3.2 Tabulated Storage and Loss Modulus Results

QFN_134mil DMA Results			
No layers removed (whole board)	Reference Temperature – 25 °C (298.15 K), Frequency – 1Hz		
	Storage Modulus (E') Gpa	Loss Modulus (E") Gpa	Complex Modulus (E*)Gpa
	11.1	0.14	11.1009
Layers removed on one side			
Removed 1SM + 1CU layer	11.1	0.24	11.1026
Removed 2CU + 2FR4 layers	10.9	0.17	10.9013
Removed 3CU + 2FR4 layers	10	0.25	10.0031
Removed 3CU + 3FR4 layers	9.2	0.18	9.2018
Layers removed on both sides			
Removed 1SM + 1CU layer	8.7	0.15	8.7013
Removed 2CU + 2FR4 layers	11	0.20	11.0018
Removed 3CU + 2FR4 layers	12	0.22	12.002
Removed 3CU + 3FR4 layers	13	0.25	13.0024
Poison's Ratio (whole board)	XY	XZ	YZ
	0.40	0.11	0.11

Chapter 4

Finite Element Modeling

4.1 Introduction to Finite Element Method

Finite Element Method (FEM) is a computational technique used to obtain near accurate results to a boundary value problem in engineering. It uses sub division of a whole problem into simpler parts, called finite elements which minimizes the associated error function involved in the problem. FEM is vastly in almost all the current engineering industries that can be imagined. Some of the common applications are mentioned as follows.

- Thermal/Fluid Flow
- Biomechanics
- Hydraulics
- Electromagnetic
- Structural Analysis (Dynamic/Linear/Static/Non-Linear)
- Geomechanics
- Aerospace/Mechanical/Automobile/Civil Engineering
- Nuclear Engineering
- Smart Structures
- Biomechanics

"The Finite Element Method is one of the most powerful numerical techniques ever devised for solving differential equations of initial and boundary value problems in geometrically complication regions" [12]. Using analytical methods it is difficult to find the solution of problems which contains complex geometry, loading conditions and different material properties. Hence FEA is used in obtaining the solution through computational technique which determines near accurate results with all the complex conditions that can't be solved analytically. The FEA method divides the whole continuum into finite number of small elements of geometrically simple shape. These elements are made up of number of nodes. A polynomial function is used to obtain the displacement of these

nodes. External force is replaced by an equivalent system of forces applied at each node. By integrating the mentioned governing equation, results for the entire structure can be obtained.

$\{F\} = [K]\{u\}$

Where,

{F} = Nodal load/Force vector

{u} = Nodal Displacement

[K] = Global Stiffness Matrix

Load value (F) has to be inputted by the user. Structure's stiffness (K) depends on the geometry and material properties. The only unknown quantity is displacement (u). There are certain steps we need to follow during the modeling and simulation in any commercial code to reach near accurate results [13]. For this project, commercially available FEA tool, ANYSY Workbench v15.0 has been used.

4.2 FEA Problem Solving Methods

The following steps has to be carefully monitored and followed to reach any near accurate solution.

1) Geometry and Material definition
2) Defining Connection between bodies
3) Meshing the model
4) Defining load and Boundary conditions
5) Understanding and verifying results

Chapter 5

Finite Element Analysis and Simulation

5.1 Modeling of QFN Package

This chapter reviews the applications of FEA modeling and simulation technique used for the QFN package assembly. The procedures followed in ANSYS are.

1. Preprocessing: Create geometric model, elements and mesh, define and input material properties.
2. Solution Process: Apply boundary conditions and loads, output control, selecting proper solver, load step control, obtaining the solution.
3. Post Processing: Review the solution; result animation, list the result, contour map.

Certain assumptions have been made while carrying out the FEA simulation.

- All the parts in 3D package are to be bonded to each other
- Temperature change in the package during thermal cycling is even all throughout the package.
- Except solder bump, all other materials are to behave linear elastic in nature

5.2 Package Geometry

A 3D 4 x 4 mm QFN package was modeled in ANSYS v15.0 using the package drawings and optical microscope images.

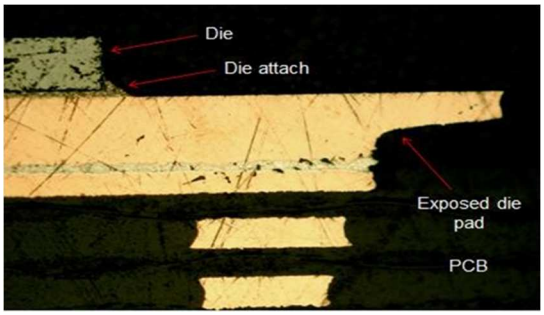


Figure 5.1 Cross section of QFN assembly

Figure 5.8 shows a 3D quarter geometry symmetry model of 4 x 4 mm QFN package with meshing. Quarter model is considered to save computational time without affecting the accuracy of the solution. Symmetry conditions are applied on the two faces as shown in the figure 6. The center node is fixed in z direction to prevent rigid body motion. The global model was meshed discretely using various meshing options and special meshing operations were carried out to make sure the continuity of meshing throughout the thickness of the package.

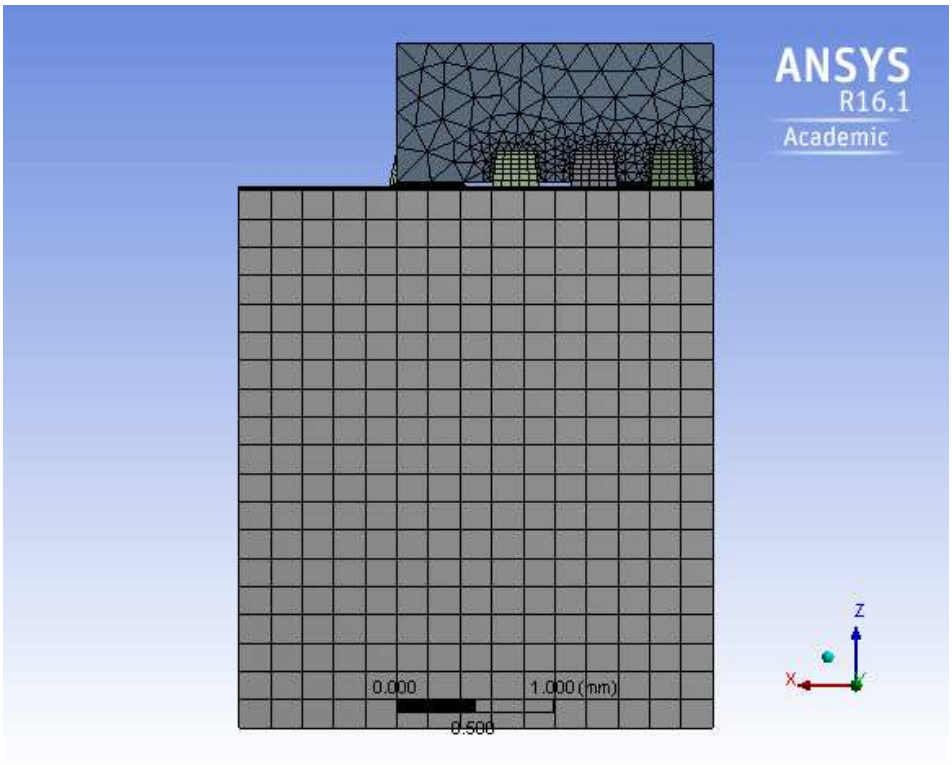


Figure 5.2 3D Quarter Global Model

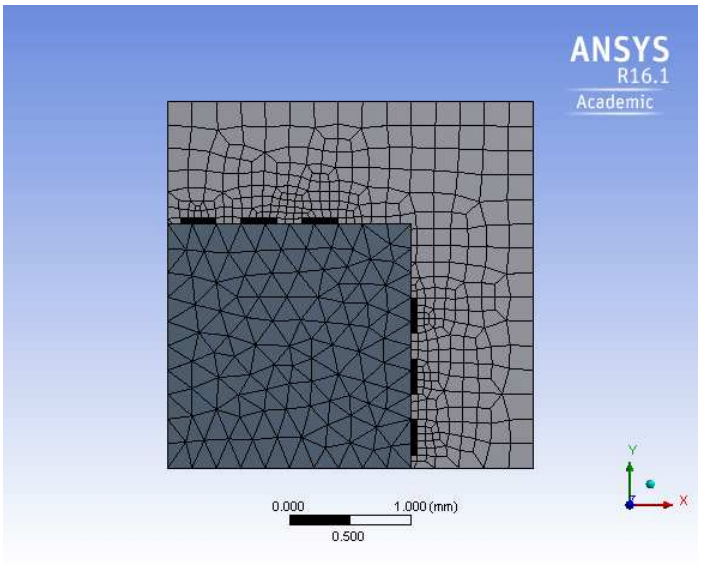


Figure 5.3 Top view of the meshed model

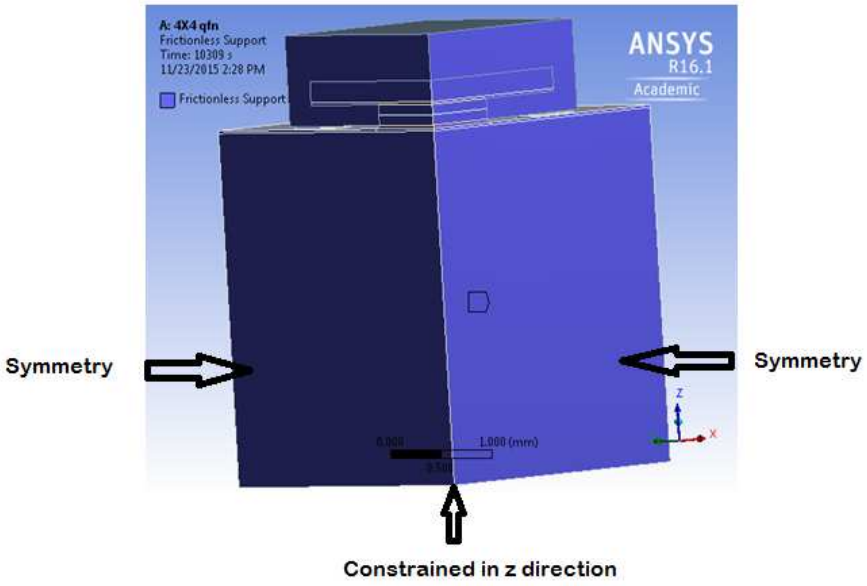


Figure 5.4 Quarter Symmetry Model

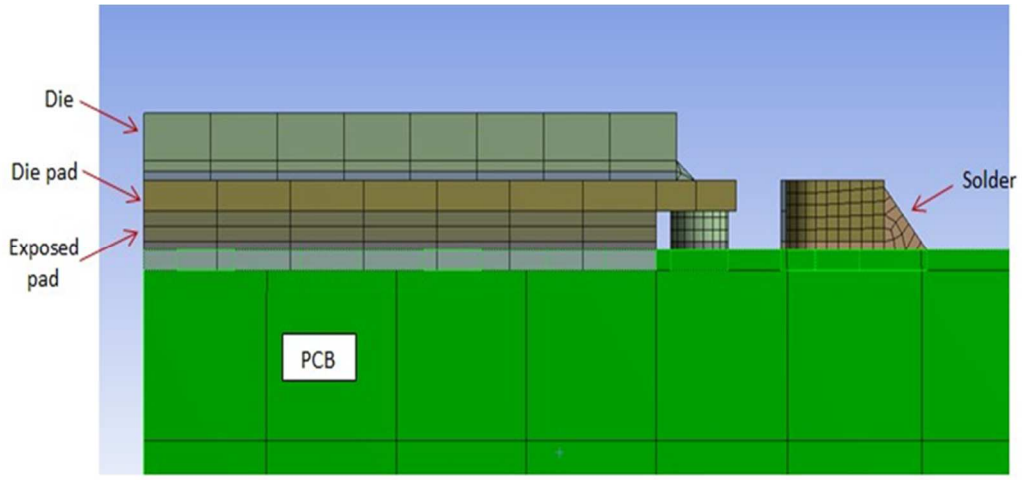


Figure 5.5 Detailed view of Global model

Table 5.1 shows the dimensions of the global model and package components.

Table 5.1 Package component dimension

Component	Dimensions (mm)
Package	6 x 6 x 7.5
Die	4.315 x 3.245 x 0.19
Die Pad	4.8 x 4.8 x 0.1
Exposed Thermal Pad	4.15 x 4.15 x 0.1
Solder Thickness	0.3
Anchor Pin	0.32 x 0.32 x 0.2
Pitch	0.5
PCB	15 x 15 x 2.38
	15 x 15 x 3.45

The simulation was done under thermal cycling load of -40°C to +125°C, 15 min ramp/dwell with 125°C as stress free temperature. By choosing the high dwell temperature of the Board Level Reliability as the stress free temperature, the system achieves stability state faster. Simulations are done over three complete cycles since most of the solder joints reach the stable state after the end of third cycle.

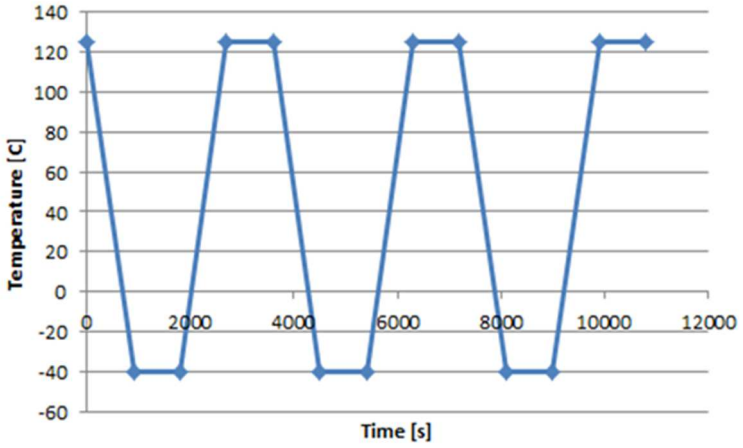


Figure 5.6 Temperature profile

5.3 Material Properties

All material properties are considered linear elastic and FR4 as orthotropic having different in-plane and out-of-plane properties. The material properties are obtained from the vendor datasheets and are listed as below. SAC305 Solder was modeled as rate-dependent viscoplaic material using Anand's viscoplasctic model. Anand's visoplastic constitutive la describes the inelastic nature of the lead-free solder which takes into consideration of both creep and plastic deformations and combines them into inelastic strain which accounts for solder's strain rate and temperature sensitivity [14].

The total strain is expressed as,

$$\varepsilon_{ij} = \varepsilon_{ij}^{e} + \varepsilon_{ij}^{in}$$

Where, ε_{ij}^{in} is the inelastic strain tensor.

The Anand's model consists of two coupled differential equations that relate the inelastic strain rate to the rate of deformation resistance.

The strain rate equation is represented by,

$$\frac{d\varepsilon_{in}}{dt} = A\left[\sin h\ \left(\xi\ \frac{\sigma}{s}\right)\right]^{\frac{1}{m}} \exp\left(-\frac{Q}{RT}\right)$$

The rate of deformation resistance is given by,

$$\dot{s} = \left\{h_0(|B|)^{\alpha}\ \frac{B}{|B|}\right\} \frac{d\varepsilon_p}{dt}$$

Where, $B = 1 - \frac{s}{s^*}$

$$s^* = \hat{s}\left[\frac{1}{A}\ \frac{d\varepsilon_p}{dt} \exp\left(-\frac{Q}{RT}\right)\right]$$

Where, $\frac{d\varepsilon_{in}}{dt}$ is the effective inelastic strain rate, σ is the effective true stress, s is the deformation resistance, T is the absolute temperature, A is pre-exponential factor, ξ is stress multiplier, m is strain rate sensitivity of stress, Q is activation energy, R is universal gas constant, h_0 is hardening/ softening constant, $\hat{s}$ is coefficient for deformation resistance saturation value, n is strain-rate sensitivity of saturation value, and a is strain-rate sensitivity of hardening or softening. Anand's viscoplasticity law consists of nine material constants and is listed in Table 5.2

Table 5.2 Anand's constant for SAC305 solder

Anand's constants	SAC305
s_0 (MPa)	2.15
Q/k (K)	9970
A(1/sec)	17.994
ξ	0.35
m	0.153
h_0 (MPa)	1525.98
$\hat{s}$ (MPa)	2.536
n	0.028
a	1.69

Table 5.3 Orthotropic properties of FR4

Young's Modulus (GPa)	Poisson's Ratio	Shear Modulus (GPa)	Coefficient of Thermal Expansion (ppm/°C)
E_x, E_y = 27.184 E_z = 11.884	v_{xz}, v_{yz} = 0.39 v_{xy} = 0.11	G_{xz}, G_{yz} = 5.792 G_{xy} = 12.266	α_x,α_y = 16 α_z = 84

Table 5.4 Material properties of package components

Material	Young's Modulus (GPa)	Poisson's Ratio	Coefficient of Thermal Expansion (ppm/°C)
Die	131	0.278	2.61
Die Attach	11.8	0.3	64
Leadframe	129	0.34	17
Epoxy Mold Compound	3	0.3	63
Exposed Die Pad	129	0.34	17

Chapter 6

Results

- Material Characterization for in-plane and out-of-plane was done successfully and has been tabulated
- Simulation at Board Level was done under thermal cycling and equivalent stress, strain energy and elastic strain in constrained direction was found and are listed as below

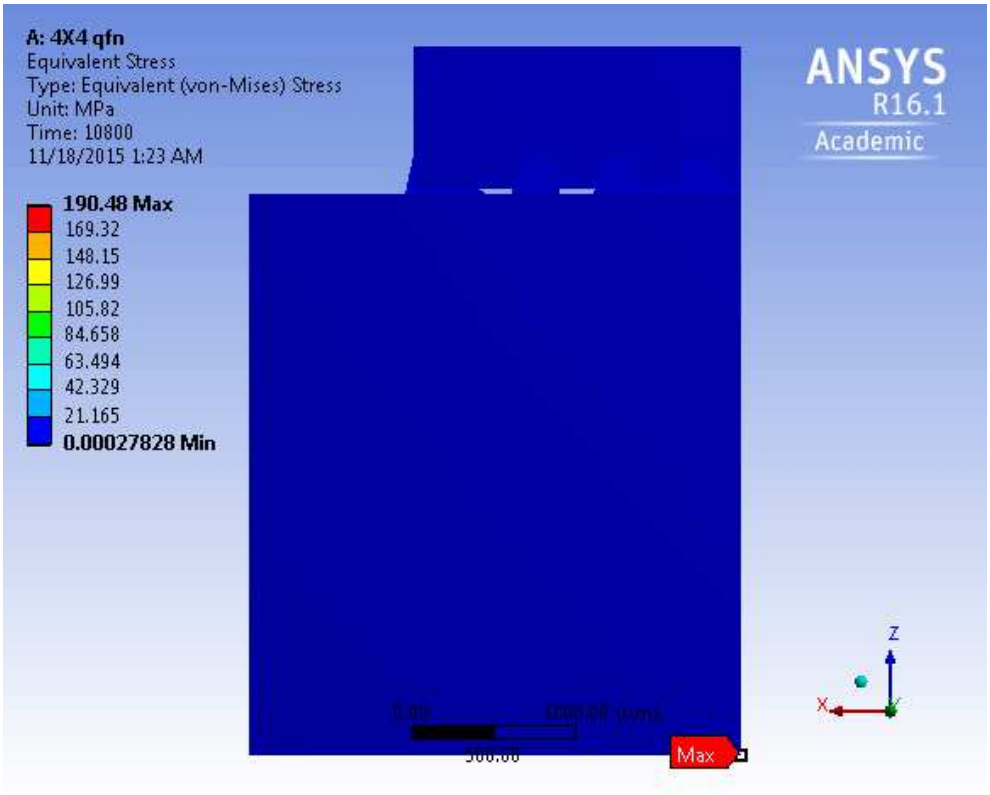


Figure 6.1 Equivalent Stress (Mpa)

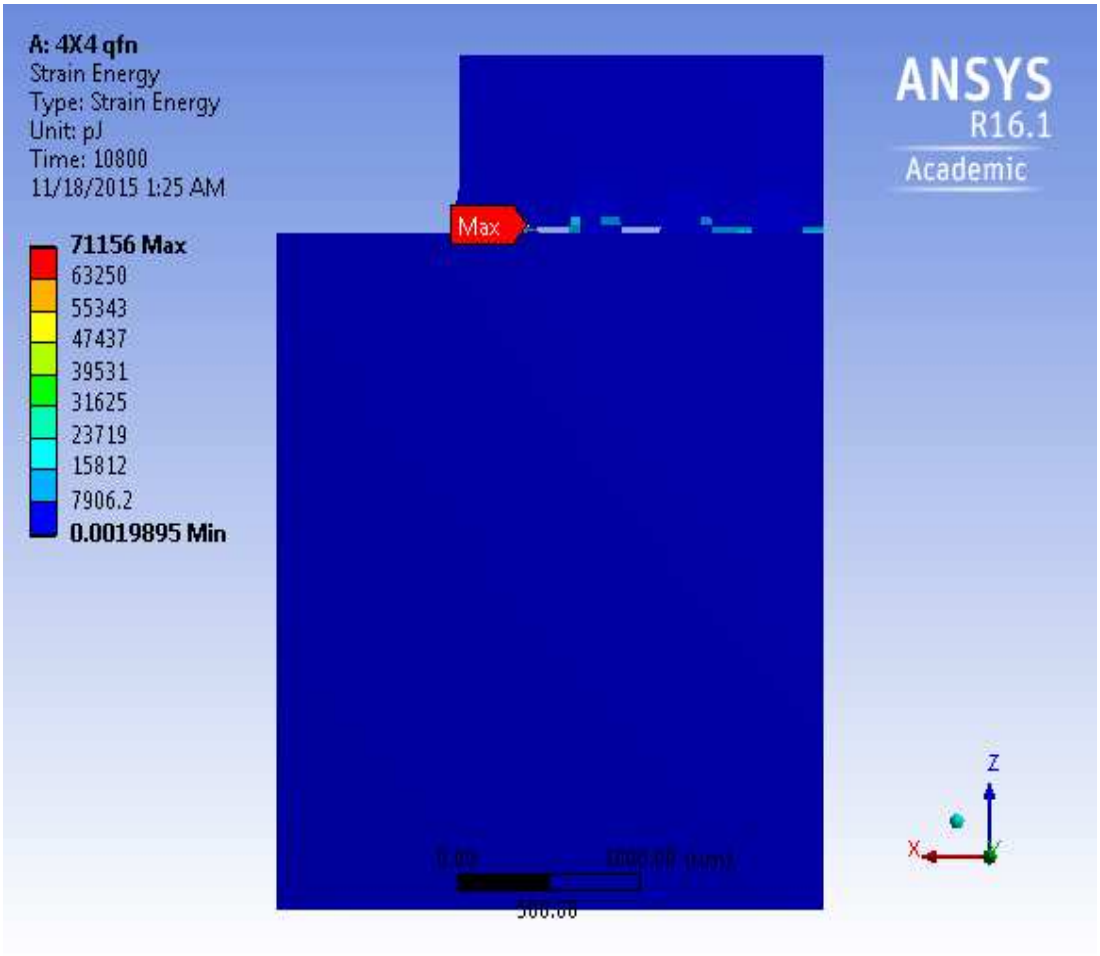


Figure 6.2 Strain Energy (pJ)

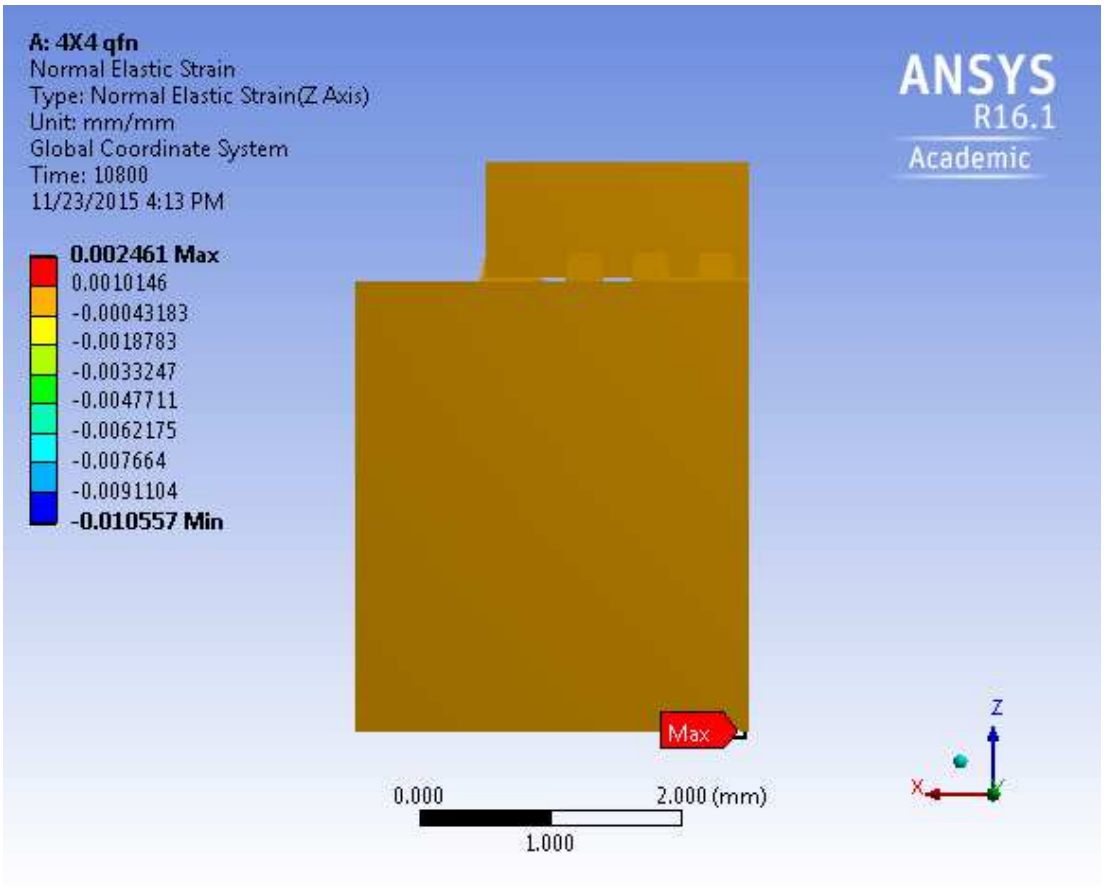


Figure 6.3 Elastic Strain

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Biographical Information

Karthik Rajashekar received his bachelor's degree in Mechanical engineering from Visvesvaraya Technological University in the Year 2012. He pursued his masters in mechanical engineering in the University of Texas at Arlington in fall 2013. He was an acting member in the Electronic MEMS &Nano electronics Systems Packaging Centre (EMNSPC) from his first semester. He was a research assistant under the supervising professor Dr. Dereje Agonafer and was into reliability team with keen interest in the failure analysis of the electronic packages. His research mainly included the Experimental Material Characterization of the Quad Flat No-Lead (QFN) PCB and thermal cycling simulation of the electronic packages. He was also a part of the research team, and an integral part of the SRC funded project where he worked closely with industrial liaisons. After graduation Karthik plans to pursue his further career in the field of electronic packaging, semiconductor industries or automobile industry.