ESTIMATION OF FRACTURE MECHANICS PARAMETERS IN 3D TSV PACKAGE DURING CHIP ATTACHMENT PROCESS

by

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Abstract

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Nowadays, the packaging of electronic products is becoming revolutionized, since the packages are becoming more and more complex, dense, thinner and lighter for greater portability. Miniaturization of packages is being taken to the next level, and hence, 3D packaging has become a hot topic in the present research area. Three dimensional chips stacking with TSV technology has gained momentum to meet such requirements of significant miniaturization and power reduction which result in increased performance. However, the unique issues related to yield and reliability of critical areas in TSV based 3D ICs need to be evaluated. Therefore, Reliability of such electronic packages has become a critical issue in today's technological scenario. In this study, the 3D package has been subjected to reflow process and the resultant modes of fracture prevalent along the length of the TSV due to the CTE mismatch between different materials has been identified. Design changes in the die and substrate thickness has been simulated to study its affect on the crack driving energy. Analysis is done using Finite Element Method (FEM) to obtain the stress intensity factor (SIF) in the TSV region as well as the stress distribution in solder joints for different die size and substrate thickness, thereby trying to address and predict the prevalent modes of fracture in TSV and assist in the design changes to reduce failure probability.

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Chapter 1

Introduction

1.1. A Glimpse in Microelectronics industry

With technological advancement, the electronics in today's digitalized industry are undergoing integration and miniaturization to become smaller, lighter and dense for greater portability while at the same time, improving in efficiency, quality with reduced cost and power loss to provide ease in seamless computing and other high-end applications for the world. This requires that effective communication be maintained between the IC's and the electronic systems without compromising with the cost and form factor owing to the increased complexity [13]. Hence, the various challenges arising due to the factors like signal processing time, heat dissipation and cooling within the devices, chemical and other reliability issues need to be dealt effectively by electronic packaging.

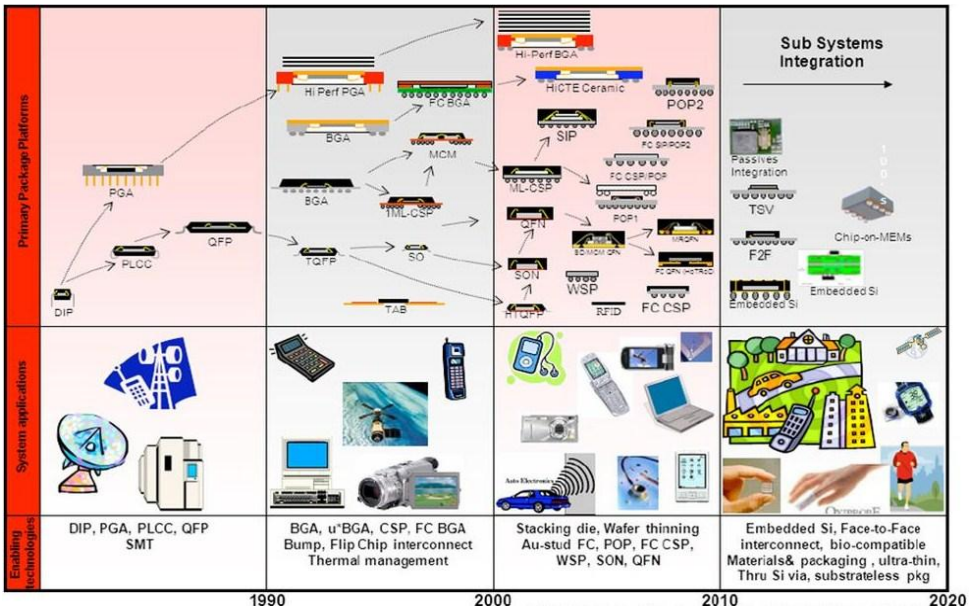

Figure 1-1 TI Packaging Technology Trends [14]

1.2. Electronic Packaging – The Basics

To begin with basic definition, Electronic packaging is a science and art of providing a suitable environment to the electronic product, as a whole, to perform reliably, over a period of time. When we use the word suitable environment, it includes thermal, electrical and other green issues. It encompasses every technology associated between IC and the system [15]. The role of electronic packaging is crucial since the performance of the IC's and the system can be properly gauged only after the electronic product has been packaged. The various levels of electronic packaging are broadly classified into:

1. Chip-Level.
2. Board-Level.
3. System-Level.

Chip-Level Packaging: The lowest level of packaging Is the chip level. It consists of steps and processes in which a bare die is conveniently handled and packaged to use on boards, etc, since we cannot directly incorporate bare dies to use, though now it has become possible as well.

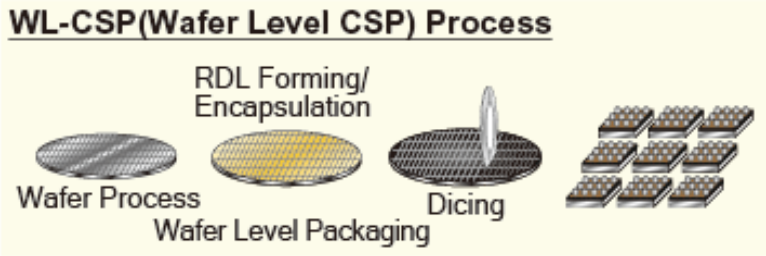

Figure 1-2 Chip Level Packaging Process [16]

Board-Level Packaging: Here, the bare dies which are packaged are mounted and assembled together on system level boards to perform system level functions.

System-Level Packaging: System-level packaging is the culmination and integration of chip level and board level packaging which come together to form a system to perform specific functions as required by the user. E.g., Computer, Hard Drive, Mobile phone, Digital Cameras, etc.

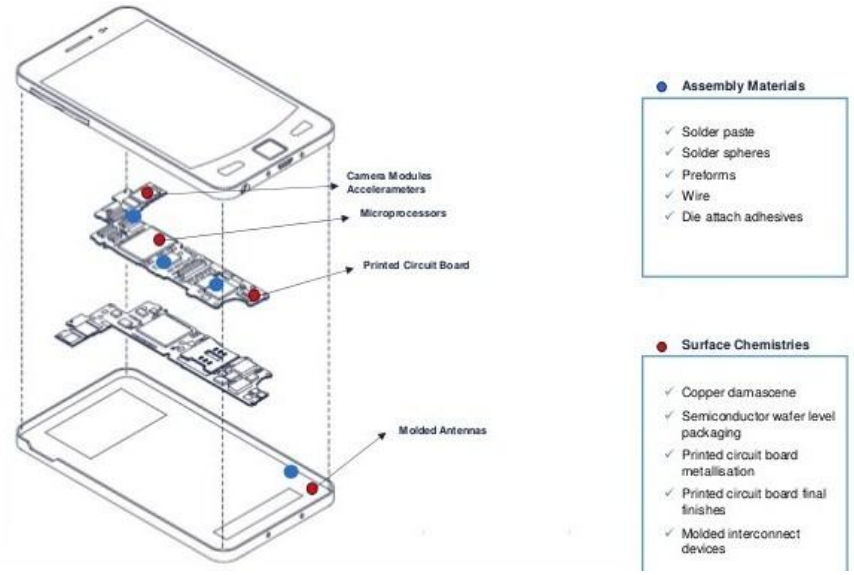

Figure 1-3 System Level Packaging Application in a Mobile Device [17]

There has always been a challenge to maintain a balance between cost, size and performance in electronic packages since the consumers require a product which costs less, has high performance and is of a size which is convenient to handle. Now with increasing the performance while reducing the form factor product, cost comes into play which tends to increase. Hence there has to be a productive and efficient trade-off between these factors to achieve and manufacture an optimum product. Also, with the miniaturization of the product, reliability and testing becomes important so that the product is thermomechanically sound, dissipates heat properly and is able to withstand real-life situations without compromising its life cycle.

1.3. Levels of Packaging

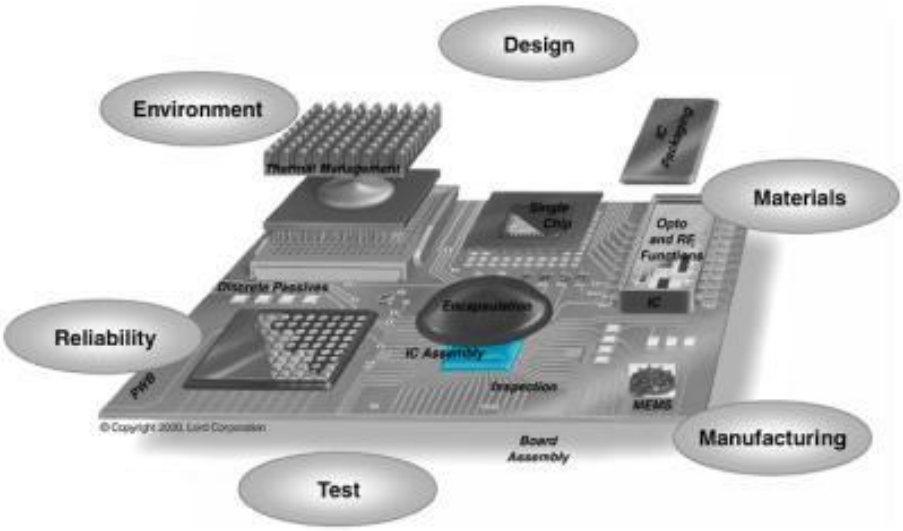

Figure 1-4 Electronic Packaging Considerations [15]

The different levels of electronic packaging are listed below:

Level 0:

- Interconnections on a monolithic silicon die.

Level 1 :

- Packaging silicon dies into single chip packages.

Level 2:

- Multi chip modules based on chip-set technologies.

Level 3:

- Printed wiring cards and boards.

Level 4:

- Complete electronic systems consisting of several subassemblies (boards, racks and frames).

Chapter 2

Trend in 3D packaging

The roadmap of electronic packaging is driven in such a direction that chips with more input/output terminals (I/Os) and state-of-the-art multifunctionality is going to take over [18]. To meet such requirements in innovation, rapid changes are being implemented with respect to the design, manufacturing methods, material selection, etc.

WLP, 3D Stacking with wire bonds and flip chips, 3D SiP (System-in-Package), PoP (Package-On-Package), 2.5D interposer are some of the emerging trends which are paving a way for new technologies.

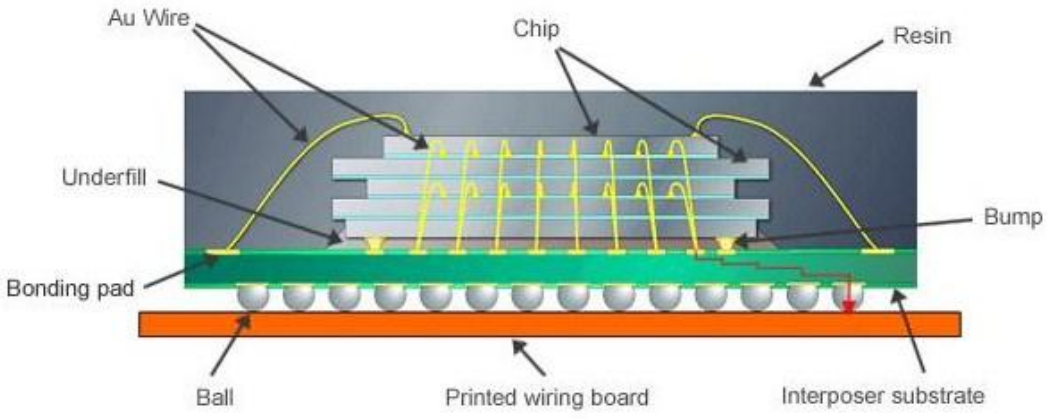

Figure 2-1 SiP Package with Stacked Chips [19]

With the trend in chip packaging technology reaching the horizontal limit, designers and engineers are constantly thinking out to find new ways and one of the steps is 3D stacking in vertical dimension. In 3D packaging, we have different type of packaging methods which enable out of plane stacking of the dies, which help us to utilize the PCB real estate efficiently.

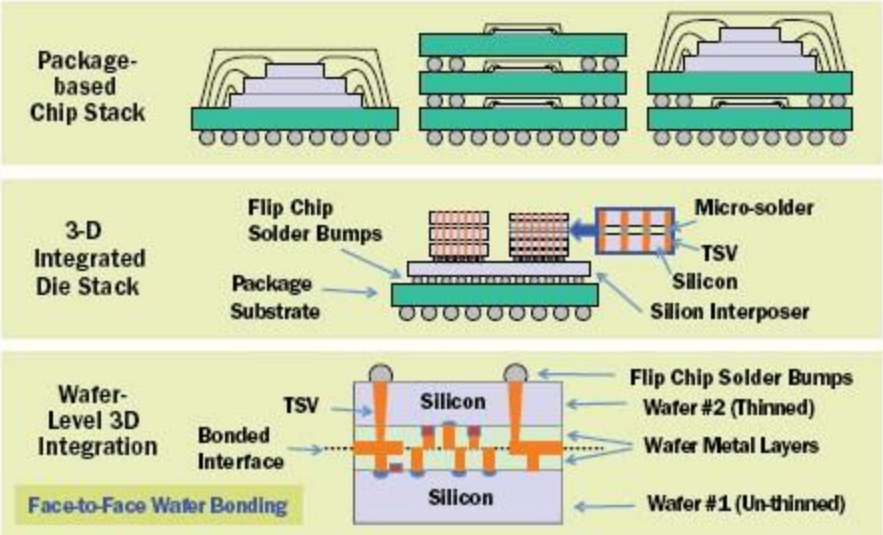

Figure 2-2 3D Packaging Technologies [20]

1. Wafer-Level Packaging (WLP): Here, the packaging of ICs is done at wafer level, where-in packaging, testing and burn-in is done after wafer fabrication [18]. Advantages for WLP packages include low cost as compared to CSP and BGA packages, smaller chip size and compatibility for hand held devices, while no requirement of underfill when assembling.

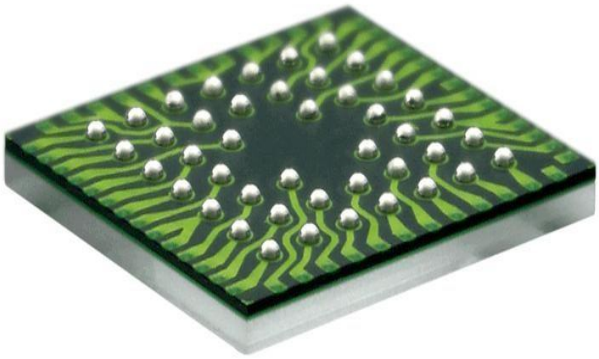

Figure 2-3 WLP Package with Ball Grid Array Interface [21]

2. System-in-Package (SiP): A system in package consists of a single module package enclosing number of integrated circuits [22]. This technology is prevalent in digital music player, portable camcorders. Interconnects are usually through wirebonding and it performs all the functions of an electronic system, with vertical stacking or horizontal tiling [23]. The disadvantage in SiP technology is that even a single defective chip can render the whole package to be non-functional.

2.1. Challenges in 3D packaging:

One of the issues with 3D packaging is the challenge of efficient utilization of CRE (Chip real estate). By using wirebonding to stack chips, only the peripheral area of silicon is being utilized.. Wire bonds create power loss issues, RC delay and only utilizes peripheral I/Os, with reduced multifunctionality. These packages are realistic solutions of 3D packaging, but more functionality and more input and output, less RC delay can be achieved through TSV.

2.2. 3D IC Technology Types

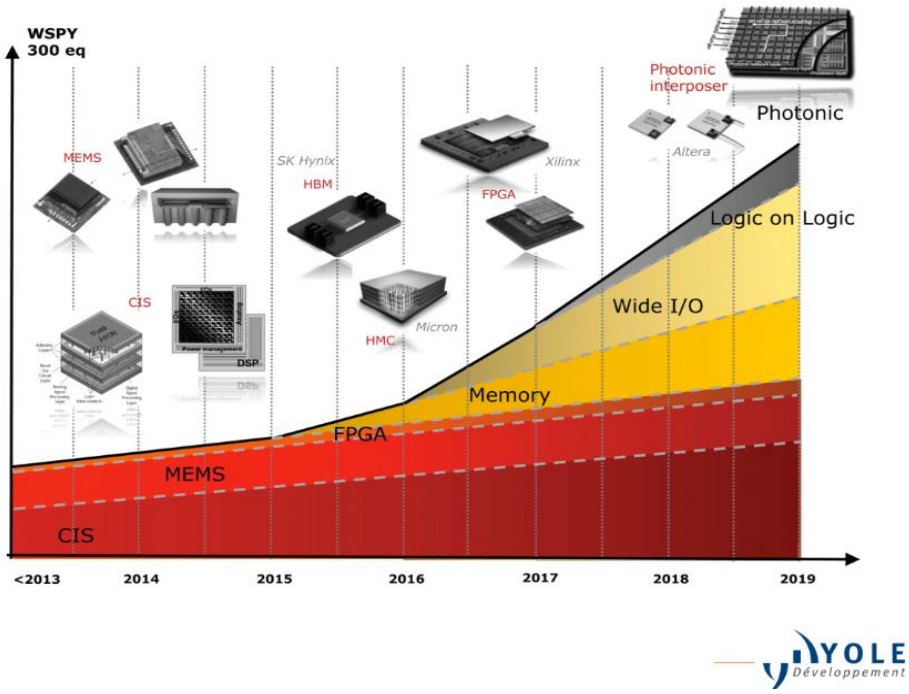

Figure 2-4 TSV Wafer Breakdown by Application [Source :Yole Development]

3D IC technology offers the advantages of design flexibility, high bandwidth, smaller footprint, efficient utilization of chip real estate (CRE), functional integration, etc, with Through Silicon Via technology posing more scope with its shorter die-to-die interconnects, low RC delay and parasitic resistance. 3D packaging has couple of other variations, i.e. 3D IC. When 2 chips using wirebonds are connected in 3D packaging, only limited number of I/Os on the periphery are utilized. Utilization of the chip area efficiently is one of the challenges faced by 3D wire bonding. Also, power loss and RC delay increases. TSV provides an alternative to such problems. 3D TSV technology is at the heart of 3D integration and stacking of dies. In a typical TSV package, a thin silicon wafer is drilled with through holes, and dielectric SiO_2 is deposited along the inside walls of the

holes, and then the hole is filled with Copper. When the length of the interconnect is less, the resistance and power loss is less with faster signal processing time. Also, there are more input and output ports in TSV which lead to improved functionality. Hence we incorporate TSV's to make 1000's of i/p and o/p in a very small area. TSV technology is the future which drives 3D packaging. However, there are some ongoing issues related to heat removal, structural integrity, chip package interaction in TSV, which are under research and development.

2.3. Limitations of TSV Technology:

One of the issues with compaction in TSV technology is the challenge of removing heat from the system (removing heat from the stacked chips). If the heat cannot be successfully removed from the system, then due to CTE mismatch of different materials like silicon, copper, there will be thermal stresses developed.

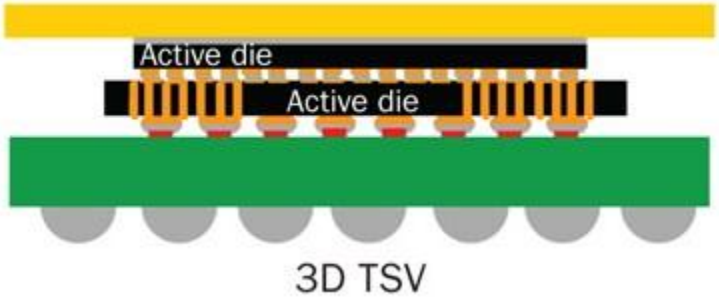

Figure 2-5 A Typical TSV Package

Around the TSV, there is a zone called 'Keep Out Zone (KOZ)' in which active transistors cannot be placed because of the developed thermal stress. This area isn't being put to effective utilization. Since the TSV's go through chips, and chips have transistors, the transistors cannot be placed in a thermally stressed area, since it won't function in that area. It is challenging to remove heat from the chips which are stacked. Due to the heat,

we have thermal stresses developed at the interfaces of different materials, which causes structural integrity issues like cracking, warpage, etc. Different materials try to expand and compress according CTE values. Also the interface of silicon/silicon dioxide is really brittle and hence crack can form at the Cu TSV and Si/SiO_2 interface. One of the methods to minimize the issue is to determine the critical areas across the length of the TSV, and fracture mechanics can be used to determine the modes of cracking prevalent along the TSV/Si interface.

Table 2-1 Material Properties of Si and Cu

Material	Young's Modulus [Gpa]	Poisson Ratio	Coefficient of Thermal Expansion (CTE) [ppm/°C]
Silicon	169	0.26	2.3
SiO2	75	0.17	0.5
Copper	117	0.3	16.7

The whole reason fracture mechanics is being used is because stress concentration equation cannot handle any flaw which has sharp corners. When you have elliptical or square holes, stress concentration is present. It is being addressed by linear elastic theory. Fracture mechanics is coming since at the crack tip, stress becomes infinity. And hence, stress intensity factor is coming into play.

This study focuses on analysis of structural integrity during chip attachment process of a 2 die 3D TSV package to gauge the stress intensity factors in TSV/Silicon interface thereby highlighting the prevalent modes of cracking in TSV. Second part of the study deals with the effects of the die and substrate thickness on the stress intensity factor arising in the TSV with respect to design changes.

Chapter 3

Fracture Mechanics Application to TSV Package

From Analysis, engineers have found that cracking is one of the primary reasons most of structures and components start to fail [24]. The relationship between fracture, stress, cracks and toughness was first introduced by Griffin in 1920. The concept of strain energy release rate was proposed by Irwin in 1950s. When the strain energy release rate reaches a critical value, crack propagates. The stress intensity factor (K) also works on a similar approach as the strain energy release rate. It can predict the state of the stress (stress intensity) near the crack tip due to the developed stresses (Remote or residual) [25]. The size, location of the crack, sample geometry and other factors affect the magnitude of stress intensity factor K.

$$\sigma_x = \frac{K}{\sqrt{2\pi r}} \cos\frac{\theta}{2}\left[1 - \sin\frac{\theta}{2}\sin\frac{3\theta}{2}\right]$$

$$\sigma_y = \frac{K}{\sqrt{2\pi r}} \cos\frac{\theta}{2}\left[1 + \sin\frac{\theta}{2}\sin\frac{3\theta}{2}\right]$$

$$\sigma_{xy} = \frac{K}{\sqrt{2\pi r}} \sin\frac{\theta}{2}\left[\cos\frac{\theta}{2}\cos\frac{3\theta}{2}\right]$$

[27]

3.1. J Integral

With the foundations of the fundamentals of fracture mechanics being established in 1960s, Rice proposed that the method of energy release rate can be extended to nonlinear materials, with energy release rate being expressed as a path-independent line integral, called J integral. It is one of the techniques to calculate the

strain energy release rate (work energy per unit fracture surface area) in a material. The equation for a cracked body with a cracked tip, under Mode-I condition is given as:

$$J = \int_{\Gamma} \left(wdy - T_i \frac{\partial u_i}{\partial x} ds \right)$$ [26]

Here, w = strain energy density with components of stress and strain tensors.

$T_i = \sigma ij * n_i$ (i^{th} components of vectors of traction and displacement) , n_j is the j^{th} component of unit outward normal to integration path, ds is the differential length along contour C, and $u_i,1 = \left(\frac{\partial u}{\partial x}\right)$ is the differentiation of displacement with respect to x_1 [26]

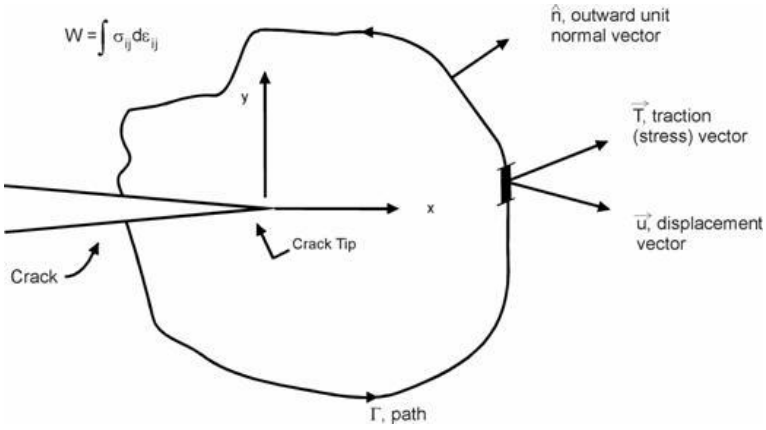

Figure 3-1 J-Integral Parameters [27]

3.2. Modes of Cracking

Fracture mechanics primarily is able to analyze a fracture phenomenon using three linearly independent cracking modes. These load types are categorized as Mode I, II, or III as shown in the figure.

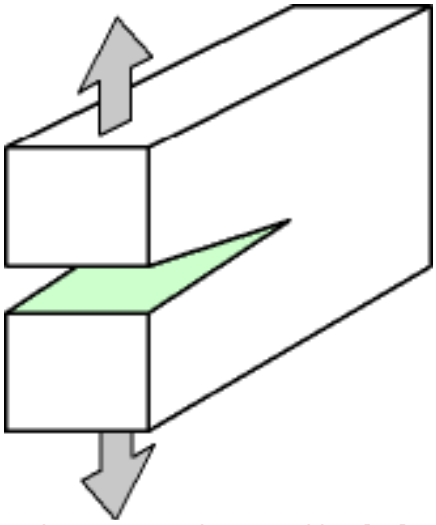

Figure 3-2 Mode 1 Cracking [29]

Mode I, shown in the figure, is an opening (tensile) mode where the crack surfaces move directly apart due to tensile load. Mode II is a sliding (in-plane shear) mode where the crack surfaces slide over one another in a direction perpendicular to the leading edge of the crack [28]. Mode III is a tearing (antiplane shear) mode where the crack surfaces move relative to one another and parallel to the leading edge of the crack. Mode I is the most common load type encountered in engineering design. Fracture is accompanied by crack and propagation.

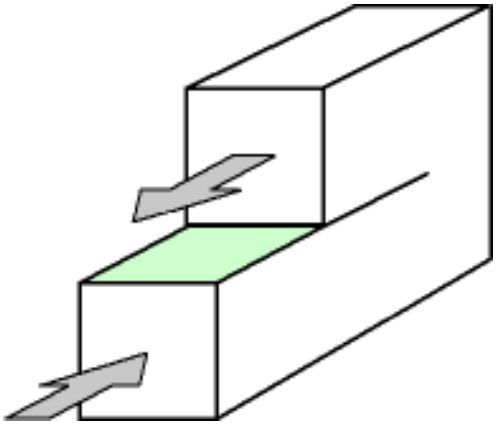

Figure 3-3 Mode 2 Cracking [29]

Significant insight can be gained about the different modes of fracture by studying the dynamics through which the crack propagates inside the material. Studies have shown that crack seems to propagate slowly with high plastic deformation rate in ductile materials and propagation of the crack continues in the material as long as the stress is being applied. Cracks in brittle materials undergo very rapid propagation with little to no plastic deformation, their magnitude growing and increasing after their initiation.

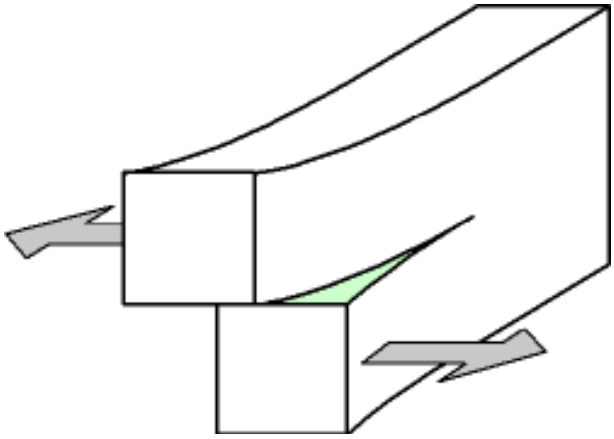

Figure 3-4 Mode 3 Cracking [29]

3.3 Fracture Toughness and Stress Intensity Factor

The critical stress intensity factor is the threshold value of stress intensity factor for a material which, when exceeded, will lead to fracture in the material [27]. It is similar to analogy of yield strength. This value of stress intensity factor at which crack propagates is known as fracture toughness which is denoted by K_c. This can be explained with the mathematical expression given below:

if $K = K_c$,

then crack propagates.

It addresses and provides information about the stress intensity field at the crack location during its propagation. Fracture toughness depends upon rate of strain and temperature, thickness of the material. The way a crack may propagate in the material is closely linked to the thickness of the material.

The designation of stress intensity factors is given by the subscripts explained below. For the crack opening mode, K_{I} is the subscript used to imply the stress intensity factor for mode I. For the shearing (crack sliding) mode, K_{II} is the subscript used to imply the stress intensity factor for mode II. For the tearing (out of plane) mode, K_{III} is the subscript used to imply the stress intensity factor for mode III. The 3 designations with their respective relations are given below:

$$K_{\mathrm{I}} = \lim_{r \to 0} \sqrt{2\pi r}\, \sigma_{yy}(r, 0)$$

$$K_{\mathrm{II}} = \lim_{r \to 0} \sqrt{2\pi r}\, \sigma_{yx}(r, 0)$$

$$K_{\mathrm{III}} = \lim_{r \to 0} \sqrt{2\pi r}\, \sigma_{yz}(r, 0)$$ [25]

Chapter 4

Modeling and Analysis Technique

Modeling of the crack has been done in ANSYS 16 and currently, only semi-elliptical cracks can be modeled. Hence, a global TSV package has been modeled, and using quarter symmetry conditions, simulated to reflow conditions to analyse the various stresses developed within the TSV package subjected to the boundary conditions of thermal reflow from 200 Celsius to 25 Celsius (room temperature). Also, submodeling technique has been used to analyse the TSV Si/Cu interface in a detailed fashion using the subsequent imported cut boundary constraints. Since the crack can be modeled only on the open face of the model (cracks cannot be modeled in the interior part of the model), the submodel has been sliced into equal halves, and one of the halves from the model is used so as to model the crack in the cylindrical silicon interposer (with imported cut boundary conditions). The behaviour of Stress intensity factor and J-integral has also been studied by varying the die and substrate thickness, and the SIF is compared with the fracture toughness of silicon.

4.1. Model Description

Global and Submodels

Crack propagation analysis has been done on a 2 die 3-D flip chip package model taken from [6] with TSV, and the response of the package when attaching the chip to the substrate has been studied. It consists of a TSV whose diameter has been kept of about 10μm, with 0.5μm die electric thickness. The TSV's occupy about 1.5% of the chip real estate (CRE) so that the efficiency of silicon isn't affected, with the TSV area limited to <4%. A novel compact modeling technique as demonstrated by Mirza et al.[8] and Chirag et al.[11], has been done so that a reasonable computational time is maintained.

Simulation is performed in 3 steps – a compact global model is formulated and solved; results from the compact global model are used as boundary conditions in the sub-model 1 which is usually the far corner region of the package (critical region) with detailed features such as actual μ-bump interconnects and the TSVs. The submodel 2 is a half model of the submodel 1 on which the imported boundary conditions are applied and the crack is formulated. Boundary conditions applied here are the constraints of the normal displacement to symmetric faces in addition to fixing the bottom center node. This has been done to prevent rigid body motions. Modeling of the materials has been done using linear elastic properties with the exception of Cu (TSVs and BEoL) metal and solders (SAC305). To take into account the creep and plastic deformations in solder so that its secondary creep is considered, Anand's viscoplastic model has been used to model solders as a rate-dependent viscoplastic material. Anand's viscoplastic constitutive law has been used to describe inelastic behavior of lead-free solder. The nine material constants of Anand's viscoplastic constitutive law, namely $\hat{s}$, A, ξ, m, h_0, a, n, s_0, Q define the solder's temperature sensitivity and strain-rate and they are determined through curve-fitting the data obtained from experiment.

In this technique, the crack propagation is intricately explained along the different locations equally spaced along the cylindrical silicon die interposer along which the TSV and copper pass through. The critical areas in TSV are found to be silicon and silicon dioxide interface, and hence, crack has been successfully modeled along the silicon die/Cu interface which is a prominent region along where the critical stresses are acting through which crack may develop.

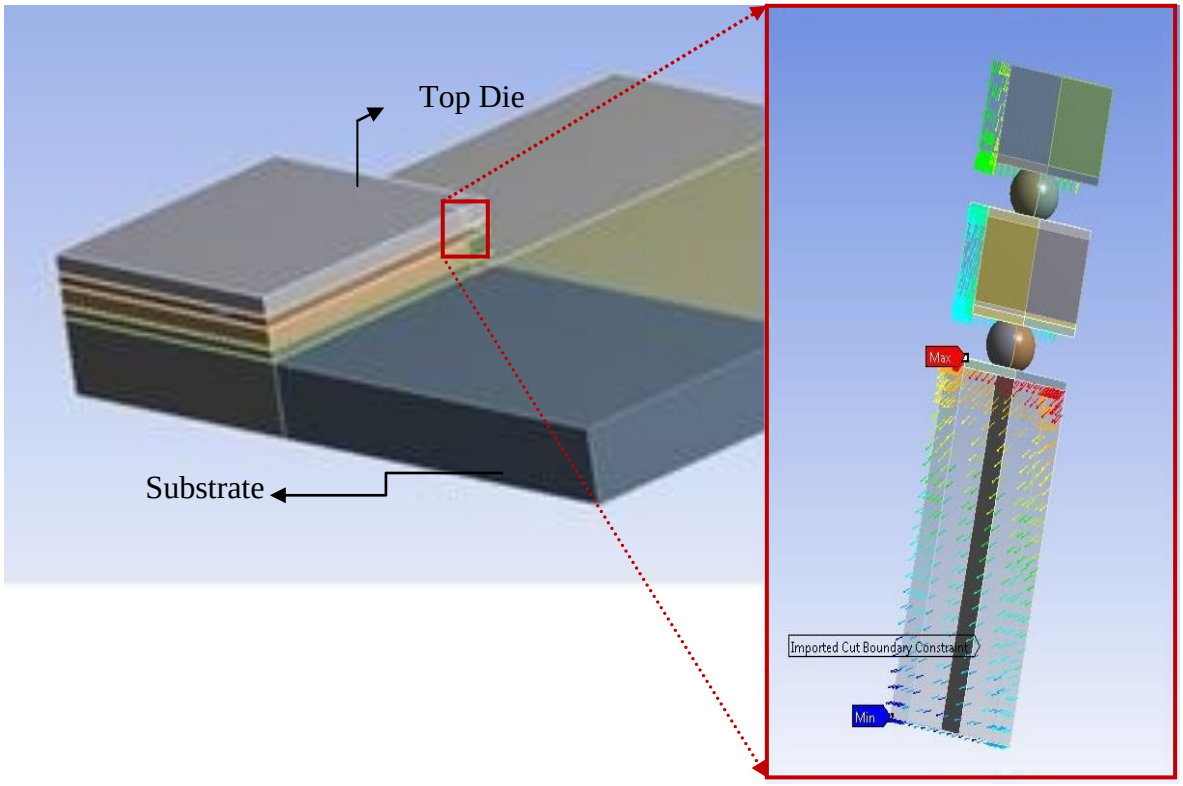

Figure 4-1 Global Model with Exploded Submodel 1

Table 4-1 Anand's Constants for SAC305 [6]

S. No.	Anand's Constant	Units	Value
1	s_0	Mpa	1.3
2	Q/R	1/K	9000
3	A	sec^{-1}	500
4	ξ	Dimensionless	7.1
5	m	Dimensionless	0.3
6	h_0	Mpa	5900
7	ŝ	Mpa	39.5
8	n	Dimensionless	0.03
9	a	Dimensionless	1.5

Table 4-2 Anand's Constant for Effective Block in the Compact Model [6]

S. No.	Anand's Constant	Units	Value
1	s_0	Mpa	0.15
2	Q/R	1/K	9000
3	A	sec^{-1}	500
4	ξ	Dimensionless	7.1
5	M	Dimensionless	0.3
6	h_0	Mpa	5900
7	$\hat{S}$	Mpa	3
8	N	Dimensionless	0.03
9	A	Dimensionless	1.5

4.2. Crack Formulation Methodology

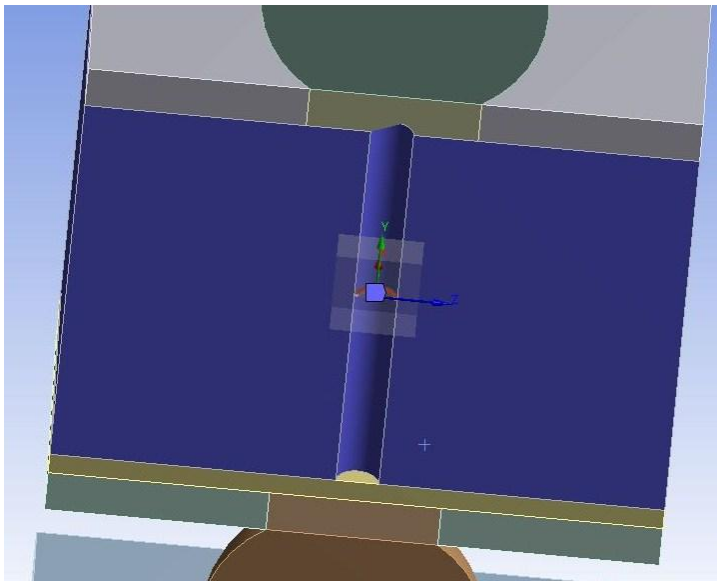

Figure 4-2 Crack formulation in the Silicon die at the mid section of Submodel 2.

In order to model and formulate radial horizontal crack for the TSV package, ANSYS 16 bundle has been used. Also, cracks can be modeled in ANSYS only with a tetrahedron mesh profile, and as of yet, only semi-elliptical cracks can be modeled on the 'exterior' surface of the model. Hence, the global model was first subjected to reflow conditions and solved, after which the submodel 1 was cut into equal halves, and simulated to same reflow conditions as a whole comprehensive model. The submodel 2, in which the crack was modeled, consists only of a single symmetrical half of submodel 1, which was again subjected to reflow conditions, with imported cut boundary constraints applied systematically from the model (Submodel1).

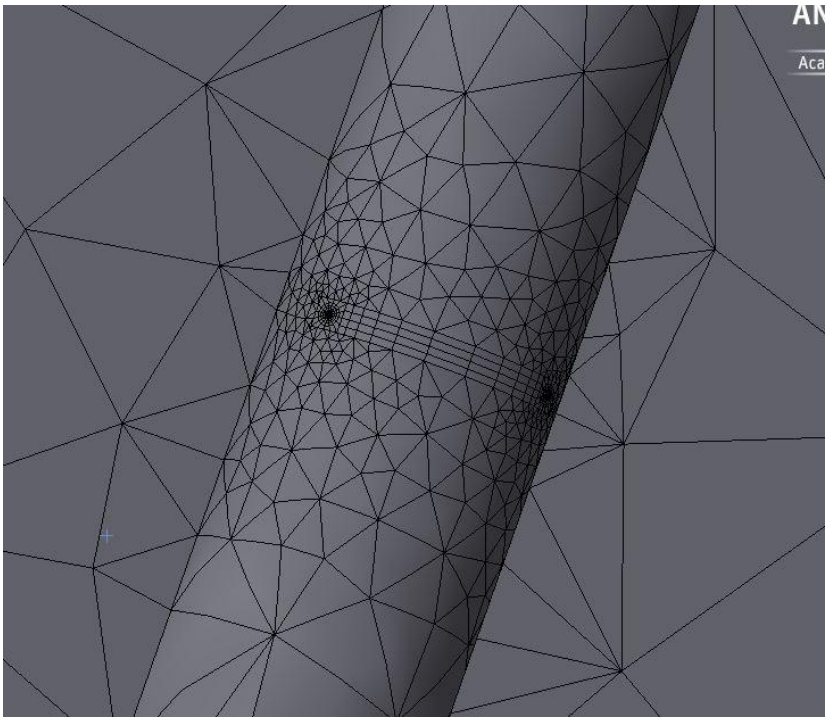

Figure 4-3 Crack Mesh on Silicon die at Si/TSV Interface

Since the total edge length of the TSV is 95μm, each simulation for the crack has been done with 10 equally spaced divisions along the TSV length in the submodel 2, with each division equal to 9.5μm. The loading was the reflow condition for the 3D TSV package when it is attached to substrate from 200°C to room temperature (for Pb-free SAC305 Alloy). The stress intensity factors (K_1, K_2, K_3) and J-Integral for different modes for different crack locations have been calculated and the parameters affecting the results have been discussed subsequently with the aid of plots and stress distribution. Analysis had been done to verify as to which area of the TSV is more susceptible to Mode 1, Mode 2 and Mode 3 cracking. Based on linear elastic fracture mechanics, the critical condition to avoid the radial crack is to satisfy $K < K_c$, where K_c is the fracture toughness of silicon.

Chapter 5

Results and Discussion

5.1. Simulation and Validation

From the stress distribution data acquired by simulating the reflow conditions, it has been analysed that the normal stress (in Z direction in our case) is positive across the middle area of the silicon/Copper interface. This has also been validated through the plot between Stress intensity factor (K_1) and crack location as shown in Figure 4. The trend in the plot infers that the middle area of TSV is susceptible to Mode 1 fracture. The value of K_1 is positive across the middle region. The Mode 2 crack propagation is more prevalent in the top portion of the Silicon/TSV interface (Figure 5). Similarly, in Figure 6, the plot between K_3 & crack location infers that the top & bottom portions of the TSVs are more susceptible to Mode 3 fracture since K_3 is higher in those regions & minimum in the middle region.

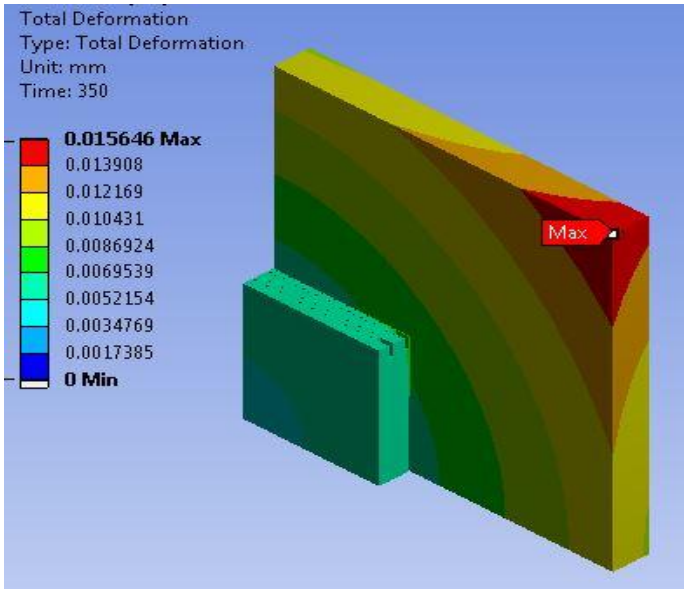

Figure 5-1 Deformed Global Model.

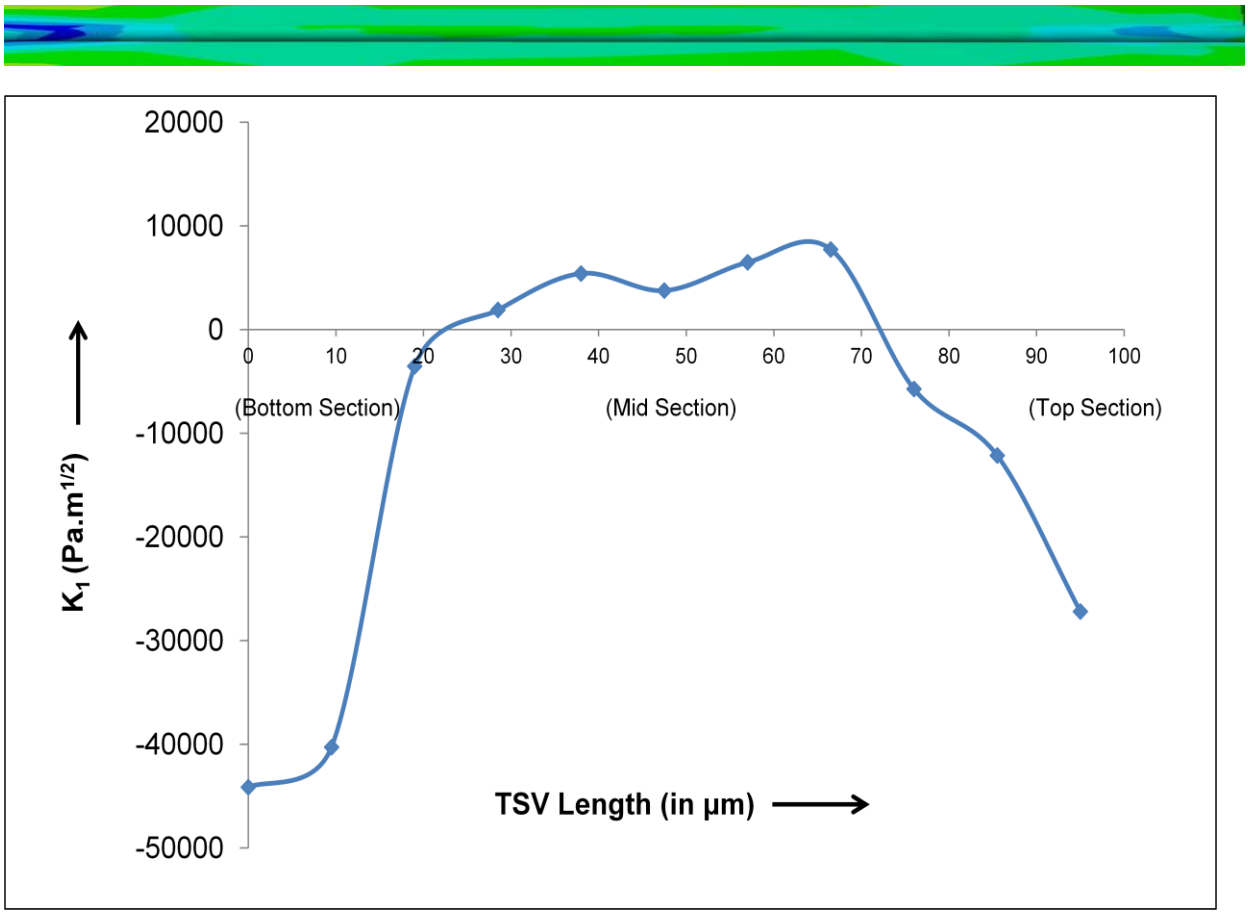

Figure 5-2 Silicon die/Cu stress distribution with K_1 plot.

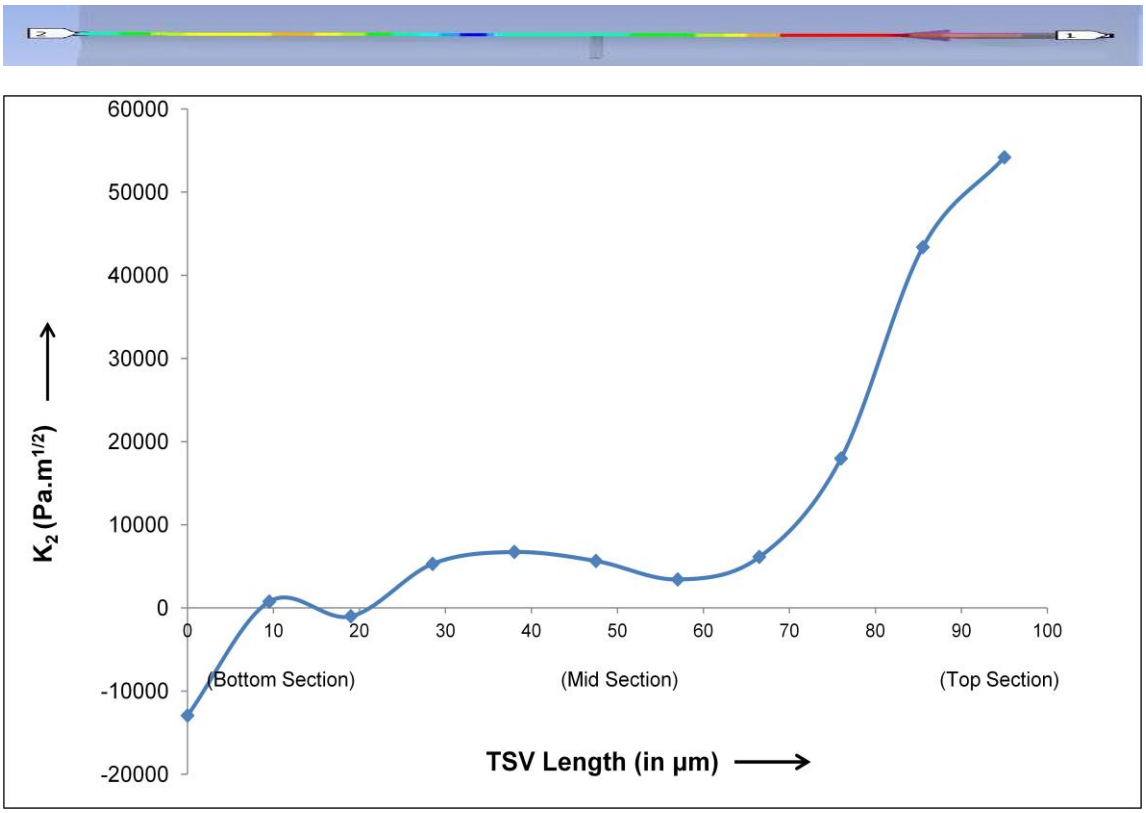

Figure 5-3 K_2/Crack location plot.

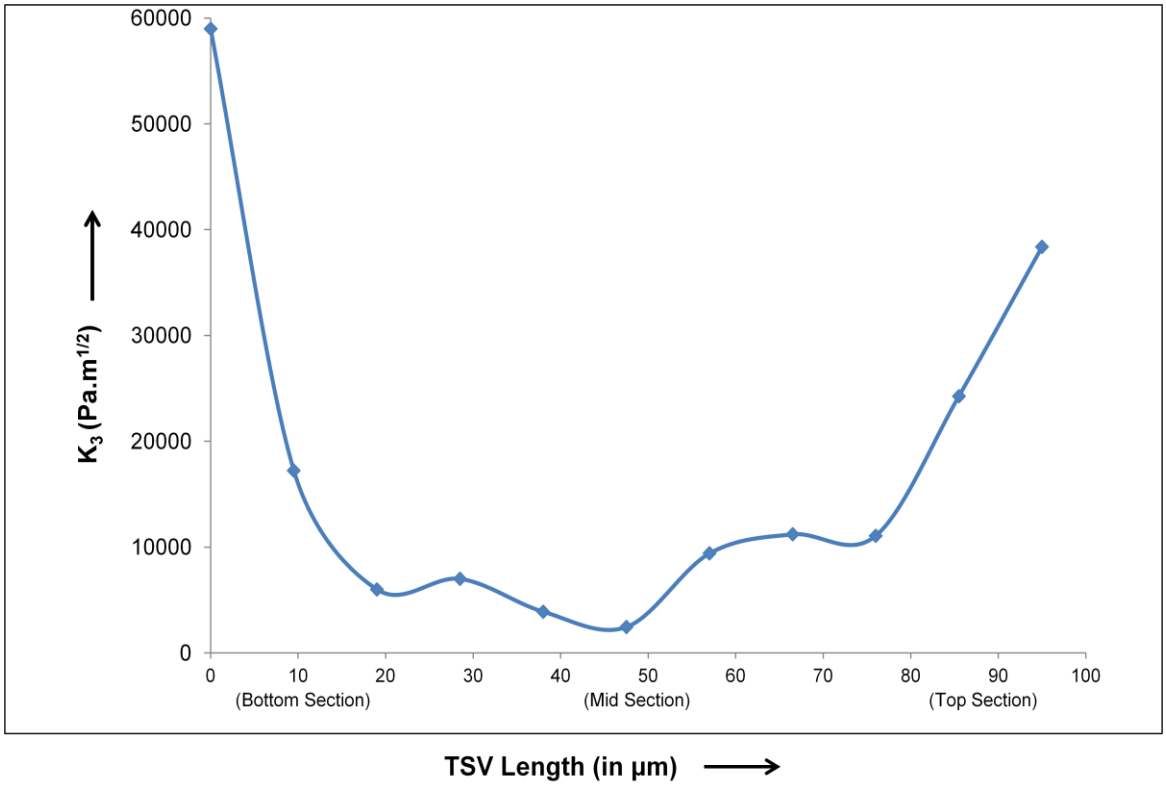

Figure 5-4 K_3/Crack location plot

5.2. Variation of Die and Substrate Thickness

The crack behaviour in the TSV region has also been studied by incorporating variation in the die and substrate thickness to analyse whether any significant change is caused in the strain energy release rate with respect to die and substrate thickness variation. It is to be noted that in this case, the crack propagation was analysed only in the middle section of the TSV region and the substrate thickness was varied from 0.2mm to 1mm, with increments of 0.2mm. The change in the substrate thickness has been done in all the models (global model, submodel 1 and submodel 2), so as to maintain consistency in the imported boundary conditions.

The J-integral does seem to have a relationship with respect to substrate thickness which can affect the crack formation. Initially, as the thickness of substrate is increased, the J-integral tends to follow a steep downward curve which signifies a decrease in crack driving force. As the substrate thickness is further increased, the J-integral's takes on a progressive positive slope, signifying constancy in crack driving force (Figure 7).

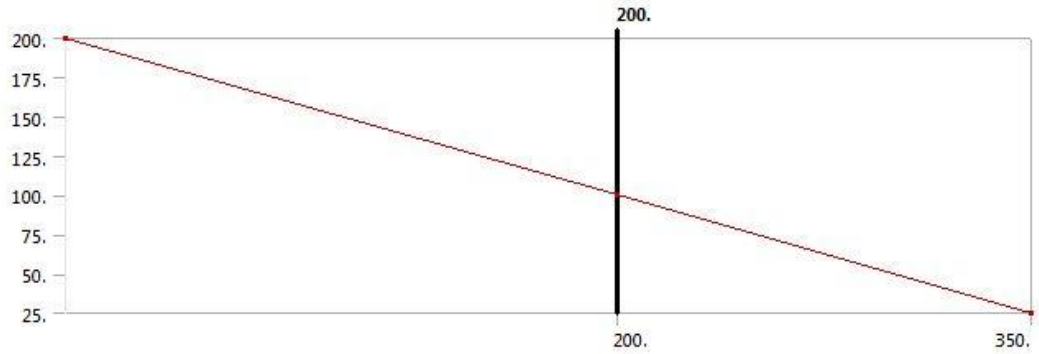

Figure 5-5 Thermal Reflow profile

The top die variation has been done by varying the thickness in equal increments of 0.1mm. The J-Integral decreases upto a certain limit with respect to die thickness, and eventually starts to increase with the increase in top die thickness.

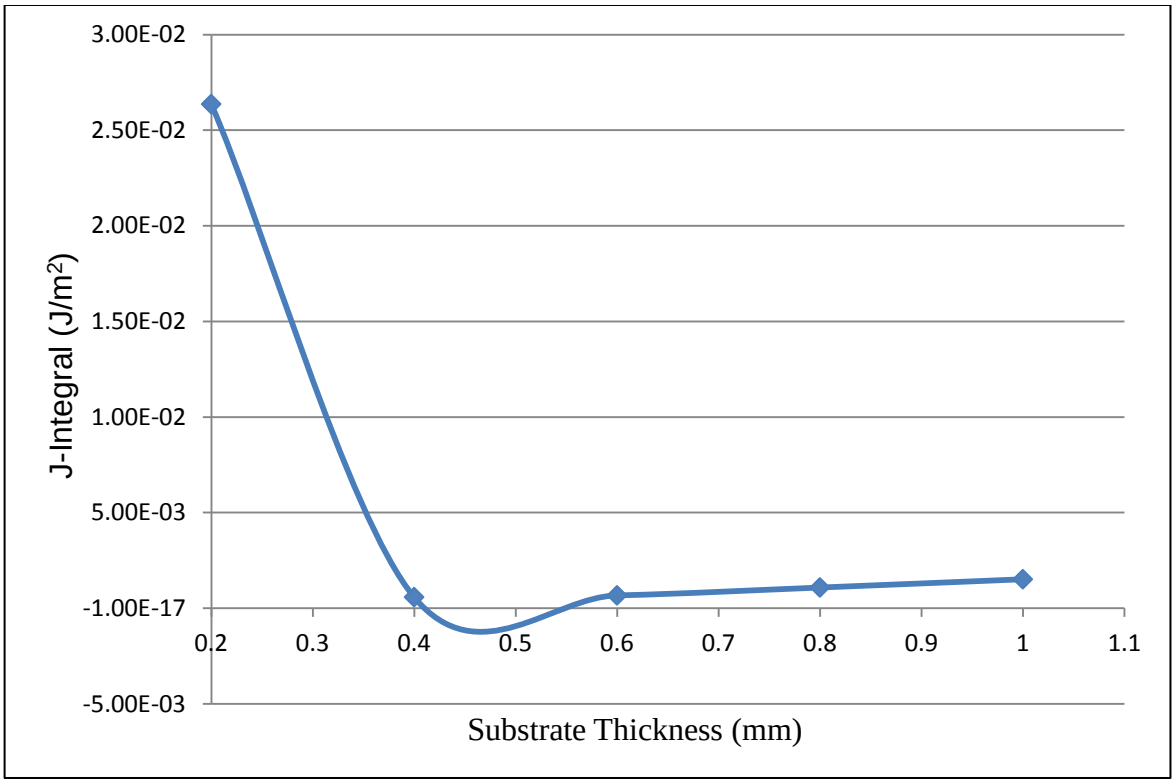

Figure 5-6 J-Integral vs Substrate Thickness Plot

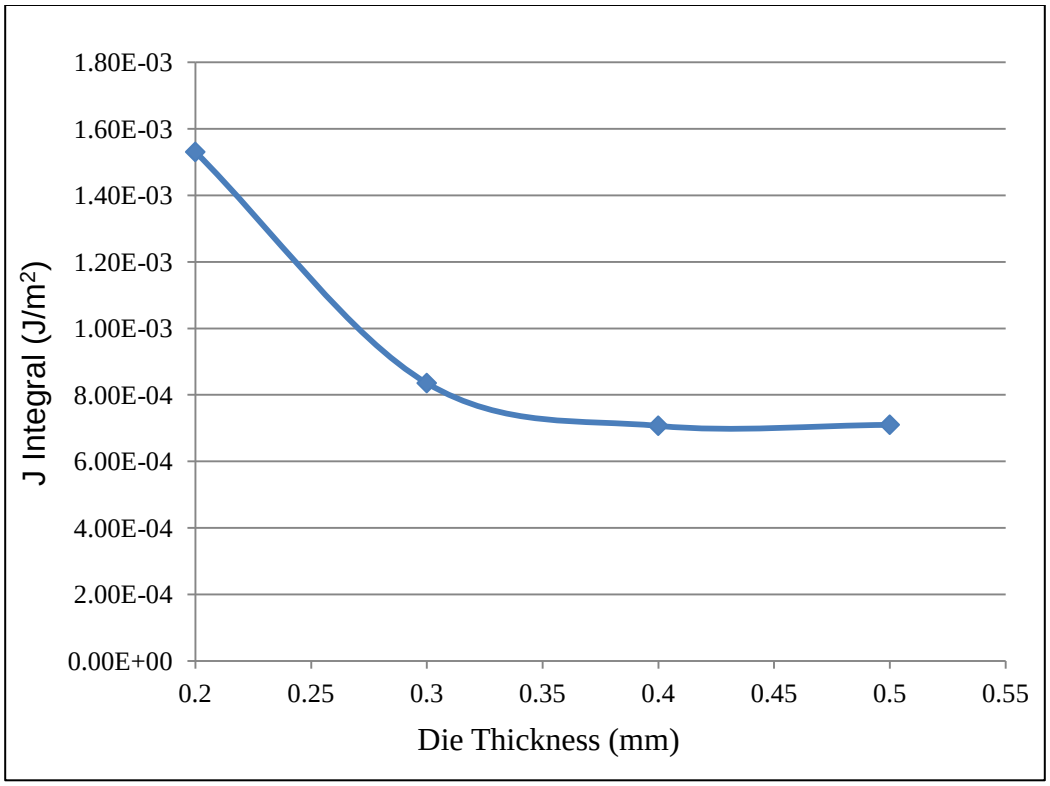

Figure 5-7 J-Integral vs Die Thickness Plot

5.3. Effect of Die and Substrate Thickness Variation on Solder Joints

Since the solders also play an important role in the reliability of TSV packages, study has been done as to whether the change in the die and substrate thickness induce any appreciable amount of stresses (Von Mises) in solder joints. From simulation analysis of variation of substrate thickness, the equivalent stresses in top and bottom solders when the substrate thickness was 0.2mm was found to have a maximum value of 33MPa. When the substrate thickness was increased to 0.8mm, the stresses induced in solders had a minute increase of 0.3MPa.

When the die thickness was increased from 0.1mm to 0.5mm, the equivalent stress in the bottom solder joint increased by 0.2MPa, resulting in a new value of about 33.2MPa. This signifies that the solder joint stresses doesn't get much affected with the variation of die thickness.

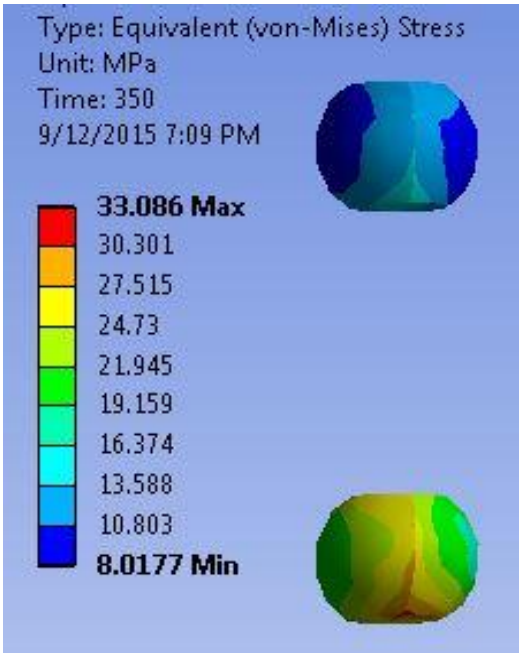

Figure 5-8 Equivalent stress distribution in solder joints with 0.2mm substrate thickness in Submodel 1.

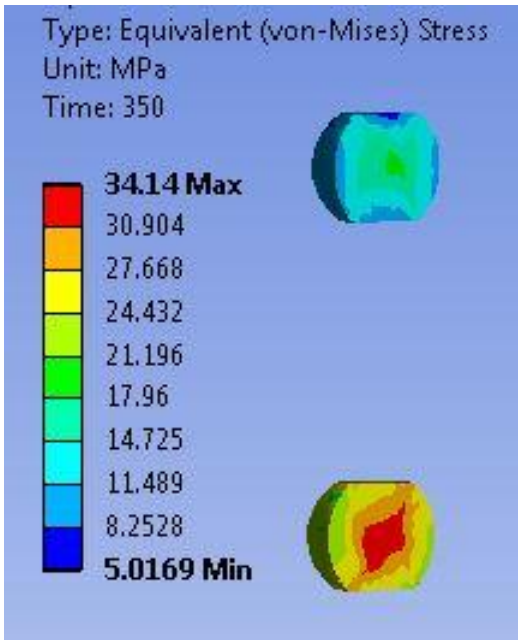

Figure 5-9 Stress distribution in top and bottom solders with 0.1mm die thickness in Submodel 1.

Table 5-1 Equivalent stress in solder joints at different die and substrate thicknesses.

Substrate Thickness (mm)	Equivalent Stress (MPa)
0.2	33.086
0.4	32.961
0.6	33.527
0.8	33.373

Die Thickness (mm)	Equivalent Stress (MPa)
0.2	32.929
0.3	33.561
0.4	33.363
0.5	32.903

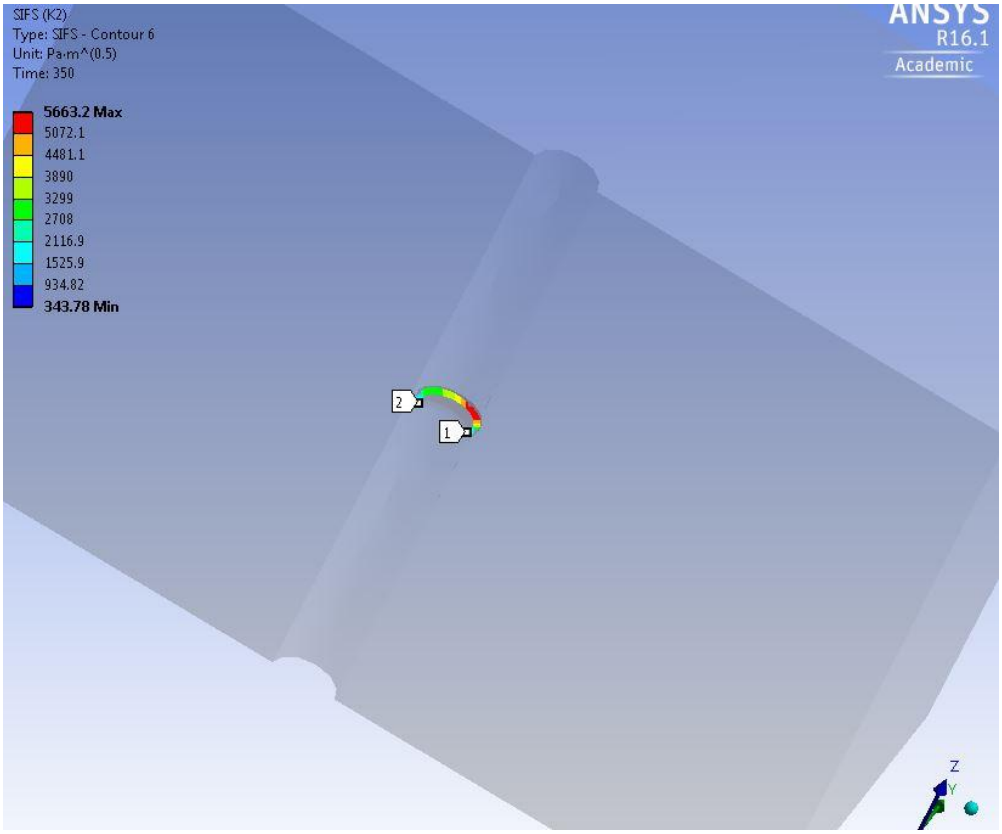

Figure 5-10 Stress intensity factor distribution K_2 at crack location in Submodel 2.

In dealing with thermo-mechanical reliability issues in TSV during the attachment of chip to the substrate in reflow conditions, tensile hoop stress and axial stress is generated due to CTE mismatch causing stress concentration to increase in the interface between Cu/SiO_2, the dielectric and TSV. Failure of silicon occurs along <111> cleavage planes. From empirical data, the fracture toughness of Silicon is 0.83 to 0.95 along <111> plane, 0.91 along <100> plane, 0.94 along <110> plane, 0.94 for polycrystalline silicon. From our analysis, it has been found that the fracture toughness of silicon near the crack susceptible region is well below the limits. Although, there is a significant probability that the mismatch may cause the crack to propagate in the critical areas where the

magnitudes of K_1, K_2, K_3 are higher. From the trend acquired in the plots discussed above, it is possible to predict and track the behavior and methodology of crack propagation, which, in our case, was the study of silicon die surrounding the TSV region subjected to thermo mechanical stresses. Since this is a preliminary study where the focus has been mainly analyzing radial horizontal cracking along the length of silicon die, further work can be done in this area to evolve and have a breakthrough in TSV technology, where improvised software bundles help us to simulate different types of cracks within the silicon and/or TSV/Cu interface. (This might improvise and be updated in the future versions of ANSYS). When you increase the substrate thickness, your J-integral goes down, which is favorable. Also with increase in die thickness, crack driving energy decreases. J-integral is the crack driving energy and its taking care of all the SIF. It incorporates the total picture of the system incorporating all the SIF.

So here, when the substrate thickness is increased, the developed J-integral is reducing. There's the critical value of J-integral. When the developed J-integral reaches that value, crack will propagate. When it is lower, the better.

Chapter 6

Conclusion

6.1. Concluding Remarks

To conclude, radial crack propagation along the length of silicon die through which TSV passes has been successfully studied, and crack has been successfully modeled in a half cut submodel and simulation has been done by importing cut boundary conditions from global model and submodel 1 to highlight the areas susceptible to different modes of cracking in silicon die/Cu/TSV interface where the magnitudes of stress intensity factors are higher and Identified which modes are prevalent in the different areas of TSV along the length. This has been validated with the aid of various plots discussed in this study which substantiate the results. The values have been compared with the fracture toughness of silicon. The variation of die and substrate thickness has also been successfully leveraged to investigate its effect on stress distribution in solder joints. The die and substrate thickness variation signifies some design changes so that the crack driving energy is lowered and is under safe limits.

6.2. Future Work

A series of new techniques in terms of TSV oriented research is possible and it does seem to have good scope for extensive study related to the reliability of 3D TSV packages. A Multi-physics study to predict crack driving forces in TSV region of 3D IC package during drop events using Finite Element Method will be investigated. In case of a drop/impact event, crack can initiate at the interface and the bulk silicon region. With repetitive drops, crack starts to propagate and electrical connection can be broken. 3D IC with TSV interconnects will be analyzed for predicting the crack driving forces when the IC is subjected to JEDEC drop. Input-G method and free falling will be implemented in

ANSYS Explicit and Transient module. A Sub-model of the critical TSV will be further used to analyze the developed J integral in the TSV region. Effect of TSV die thickness, top die thickness and substrate thickness will be analyzed using the Finite element method to come up with the best design parameters which will help to reduce the probability of cracking in the TSV region during drop events. In all the cases prominent modes of fracture will be identified so that the design parameters can be altered to reduce the crack opening, sliding and out of plane shearing modes. Crack orientation with respect to the chip plane will be also analyzed to identify the most critical crack location in the TSV. For each case vertical and horizontal crack orientation will be studied. This will help to find out better design parameters which will reduce the cracking in TSV region during drop or impact loading.

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