CHIP PACKAGE INTERACTION STUDY TO ANALYZE THE MECHANICAL INTEGRITY OF A 3-D TSV PACKAGE

by

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I also would like to mention, without all my friends' constant annoyance, I would have completed my thesis much earlier.

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ABSTRACT

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The convergence and miniaturization of computing and communications dictates building up rather than out. As planar device miniaturization continues to its ultimate limits, the complexity of circuit interconnections for 2-D devices becomes a limitation for performance and drives up power dissipation [1]. As the consumers demand more functions on their hand-held electronic devices, the need for more devices such as memory, CPU and GPU in hand-held type footprints is increasing. Chip-stacking (3-D) is emerging as a powerful tool that satiates such IC package requirements. A 3-D FPGA would overcome the interconnect limitations, resulting in greater silicon efficiency per function (number of used gates/total number of gates), faster signal/data throughput, and faster switching of the gate-level configuration. 3-D through-silicon-via (TSV) technology is being termed as the "***next big thing***" in the semiconductor arena and has the potential of revolutionizing the packaging industry but it has some inherent issues that need to be addressed before it could be implemented in the mainstream electronics industry. TSV fabrication process, thermal management of 3-D TSV packages, TSV joule heating, and

chip package interaction (CPI), are some of the key issues in this technology [2, 3, 4, 5, 6].

In this paper, the thermo-mechanical chip-package-interaction (CPI) analysis is carried out and a full field compact 3D modeling methodology has been leveraged to assess the mechanical integrity of a 2 die 3D TSV package during attachment to substrate. This modeling methodology would provide damage predictions caused due to global and local CTE mismatch between the different package components. Mechanical interaction at the Si/TSV regions, back-end Cu/low-k stack, and the inter die µ-bumps during chip attachment is demonstrated in this paper.

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INTRODUCTION

1.1 Electronic Packaging

Electronic Packaging is a multi-disciplinary subject which needs knowledge of all field i.e. Mechanical, Industrial and Electrical Engineering, Chemistry, Physics and Material Science Department. All these disciplines are equally important in Packaging. Electronic packaging provides housing and interconnections of integrated circuits to form electronic system.

Electronic Packaging must provide:

- Circuit support and protection
- Heat dissipation
- Signal distribution
- Manufacturability and serviceability
- Power distribution

Figure 1-1 shows Hierarchy of interconnections levels and the details are explained below:

Level 0

- Gate-to-gate interconnections on the silicon die

Level 1

- Connections from the chip to its package

Level 2

- PCB, from component to component or to external connector

Level 3

- Connections between PCBs, including backplanes or motherboards

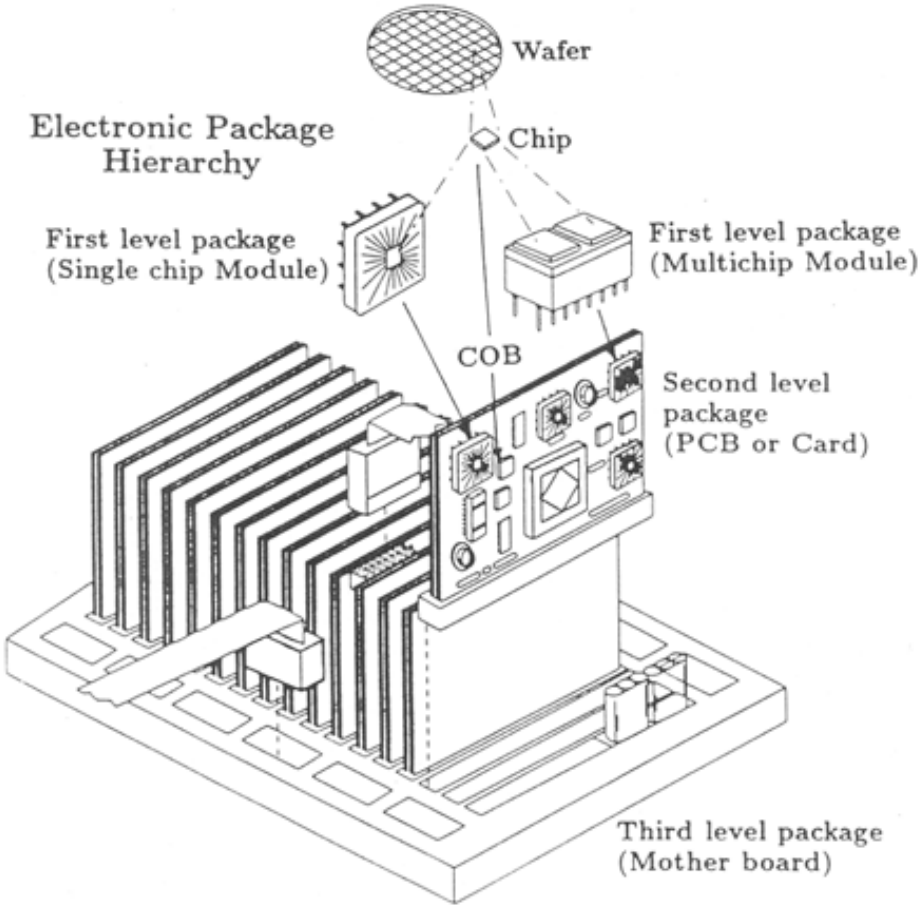


Figure 1-1 Hierarchy of Interconnections levels

Level 4

- Connections between subassemblies, for example a rack

Level 5

- Connections between physically separate systems, using for example an Ethernet LAN

1.2 Packages Classification and Assembly

Packages can be broadly classified as-

- Through Hole Mount IC Packages
  - Dual in-line Package(DIP)
  - Pin Grid
- Surface Mount IC Packages
  - Quad Flat Package(QFP)
  - Thin small outline package(TSOP)
  - Small outline J-leaded package (SOJ)
  - Ball Grid Array (BGA)
- Chip Scale IC Packages
  - Chip Scale Package (CSP)
  - Wafer Level
  - Stacked Die (2.5D & 3D Packages)

Figure 1-2 below shows a schematic diagram of the assembly process involving a typical lead frame package. Packages are manufactured after a series of process one at a time using polymers in various forms.

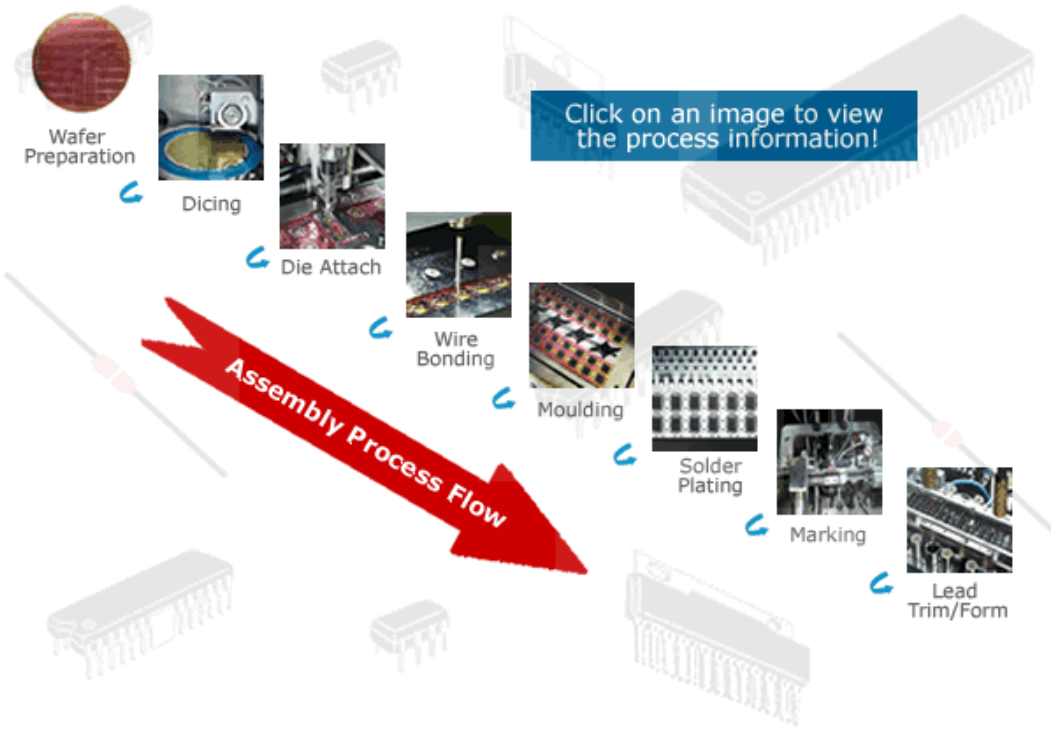


Figure 1-2 Package Manufacturing Process

1.3 3D TSV Packages

Consumer electronic products such as digital cameras, personal digital assistants, cell-phones etc., require high functional integration in small footprints with low cost. Multi-chip packaging (chips packaged on the same plane) is one of the solutions. But, due to miniaturization, coupled with the requirements of high memory density, performance, and more features per cm^2 of Printed Circuit Board (PCB), engineers have been forced to think vertically. Stacking dies and interconnecting them vertically accomplishes all of these goals. 3-D stacking of the processor and memory components in high computing applications reduces the communication delay in a multi-core system owing to reduced system size and shorter interconnects [7]. High-density-interconnects (HDI), necessitates area array packaging with much higher number of interconnects as well as

reduced footprints leading to 3D TSV technology. Hybrid-memory-cube (HMC) is one such development [8]. HMC is a small, high-speed logic layer that sits below vertical stacks of DRAM die that are connected using through-silicon-via (TSV) interconnects. 3-D IC technology is a promising approach to reduce interconnection power, increase communication frequency, improve design flexibility and enable seamless system-level integration of heterogeneous technologies. The GLOBALFOUNDRIES 3D innovation roadmap for high- performance computing is shown below in Figure 1-3 [9].

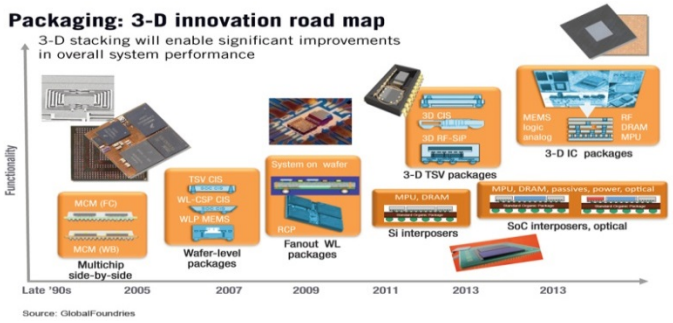


Figure 1-3 3D Innovation Roadmap - GLOBALFOUNDRIES

In this paper, the thermo-mechanical chip-package-interaction (CPI) analysis is carried out and a full field compact 3D modeling methodology has been leveraged to assess the mechanical integrity of a 2 die 3D TSV package during attachment to substrate. This modeling methodology would provide damage predictions caused due to global and local CTE mismatch between the different package components. Mechanical interaction at the Si/TSV regions, back-end Cu/low-k stack, and the inter die µ-bumps during chip attachment is demonstrated in this paper.

1.4 Literature Review

Zheng et al. [10] introduced the development trends of 3-D stacked packages. The advantage of 3-D over the traditional 2-D or planar packaging (Multi-Chip-Module, MCM) and challenges faced by the 3-D technology have been discussed. Selvanayagam et al. [2] demonstrated the nonlinear stresses and strains in the µ-bumps between the silicon chip and copper filled TSV interposer (with and without underfill) for a wide-range of via sizes and pitches, and various temperature conditions. Selvanayagam [2] results were useful for making a decision if underfill is necessary for the reliability of µ-bumps and selecting underfill materials to minimize the stresses and strains in the µ-bumps. [3] et al. developed an analytical model for the three-dimensional state of stress in a periodic array of TSVs. The model accounts for Cu plasticity and predicts the out-of-plane protrusion that occurs in the TSV due to differential thermal expansion with the surrounding Si.

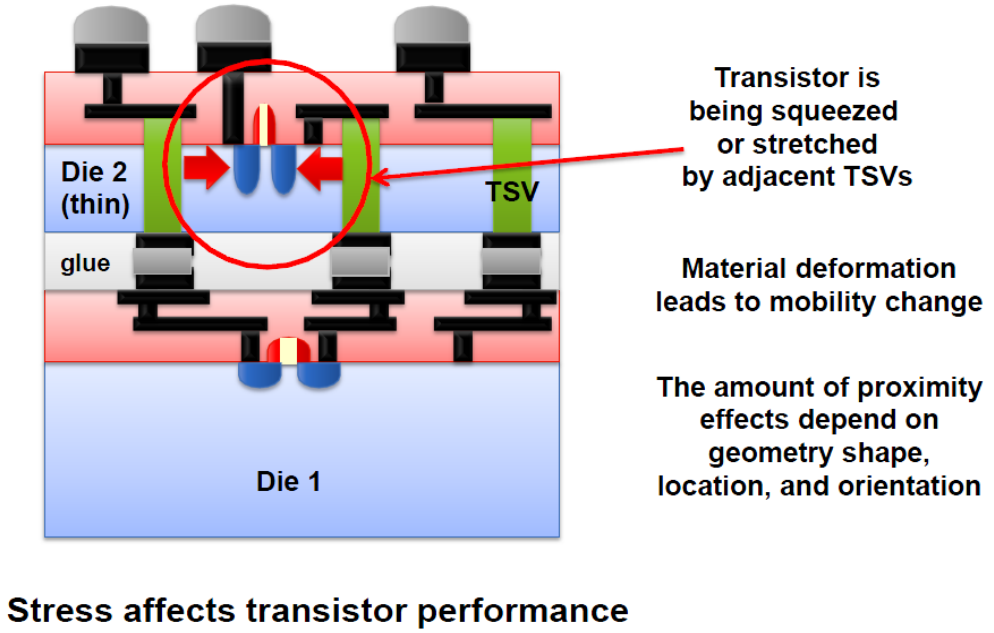


Figure 1-4 Stress Affects Transistor Performance

Excessive out-of-plane deformation of the top surface of the via has the potential to induce fracture causing stress in the brittle dielectric layers that lie above the via. Kawa et al. [4] studied the TSV related performance and reliability issues due to thermal-mechanical stress using Fammos TX. He showed that the localized TSV/Si stress significantly affects the BEoL mechanical response/reliability and the transistor performance (see Figure 1-4 and Figure 1-5). Alam et al. [11] analyzed the parasitic characteristics of inter-die bonding techniques and materials.

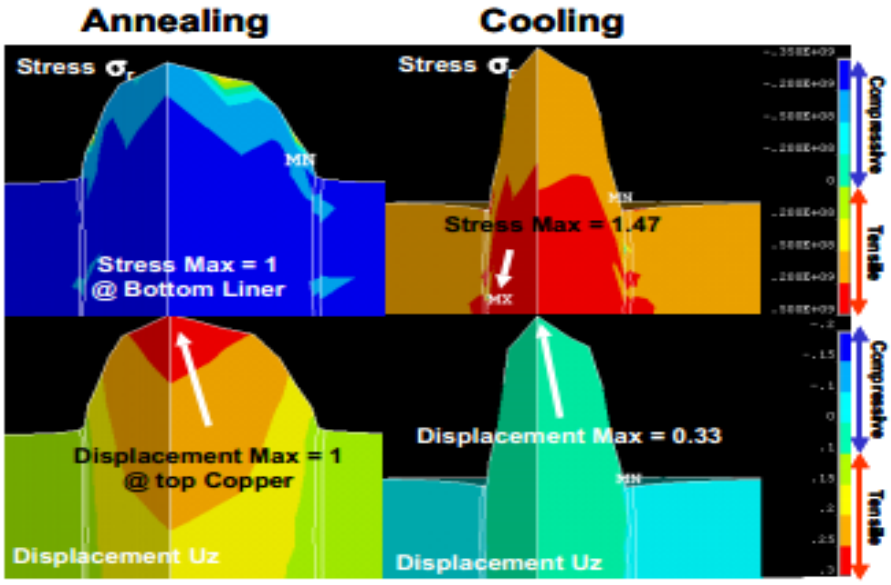


Figure 1-5 TSV Cu Protrusion

Chapter 2

MATERIAL CHARACTERIZATION

As an engineer it is very important to know about the material that we are use or study. Material characterization is the important aspect of material science department by which we determine different properties and structure of material. In this study the work is limited to determine properties of material. To predict more accurate results through ANSYS workbench, it is necessary to provide more accurate inputs. To characterize the material following parameters were considered:

- Coefficient of Thermal Expansion (CTE)
- Young's Modulus (E)
- Poisson Ratio (υ)

To determine these properties the equipment and techniques used are given below:

- Sun Microsystems Oven
- Instron Microtester with 2kN Load Cell
- Digital Image Co-relation technique (DIC)
- Thermo-mechancial Analysis
- Dynamic Mechanical Analysis

Sample preparation and test procedures for all the tests conducted for material characterization will be explained in this section.

2.1 Coefficient of Thermal Expansion (CTE)

Coefficient of Thermal Expansion (CTE) is defined as the tendency of a material which defines the amount by which it expands or contracts when heated or cooled

$$\alpha = \frac{\epsilon}{\Delta T}$$

Where,

α – Coefficient of Thermal Expansion (CTE) ppm/°C

ϵ - Strain (mm/mm)

ΔT – Difference in Temperature (°C)

Since we will be analyzing the package under reflow process i.e. 200^0C to 25°C (room temperature) , it was necessary to know the CTE of the package so the FEA model of the package would complement the actual condition as closely as possible.

2.1.1 Heating/Cooling Oven

The oven used for heating the package was a Sun Microsystems Oven with a door for easy access to place and remove packages in the oven. The oven has a 12”x4” borosilicate glass at the top wall for the cameras to view the package clearly. The purpose of using a borosilicate glass is to avoid any reflection caused due to illumination from glass surface into the camera eye. There are two openings on each side wall of the oven which are covered by rubber corks. Thermocouple wires are connected to the sample through these openings which are closed with the rubber corks after the wires have been carefully passed through them.

Figure 2-1 Sun Microsystems Oven

2.1.2 Digital Image Correlation Technique – CTE Measurement

Digital Image Correlation (DIC) is a non-contact, non-destructive technique to measure in-plane and out of plane displacements of speckles by which software can determine strain. A pair of 5MP cameras was used to capture the images. The cameras were positioned at an angle from the vertical to have a view of package's in-plane as well as out of plane deformations. The cameras were connected to software VICSnap to view the image clearly on the screen and select area to be analyzed.

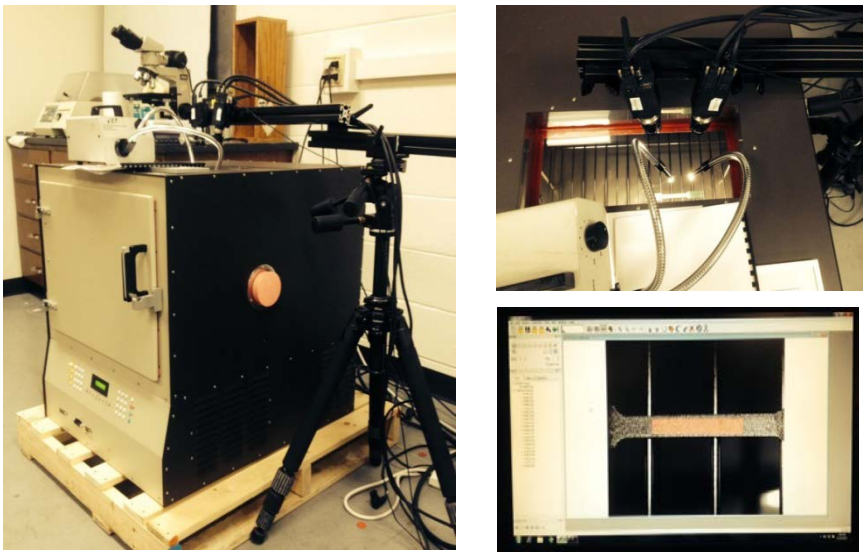


Figure 2-2 Sun Microsystems Oven & DIC Experimental Setup

2.1.3 DIC Calibration

It is of utmost importance that before using DIC, the cameras have been calibrated properly so they can measure the smallest deformation correctly. To calibrate the DIC, a calibrating panel with white base and black dots was used. The pitch between the dots was 4mm/5mm/6mm and the total number of dots was 108. First the sample is focused so that the image on the software is clearly visible and sharp, then the calibrating panel is kept at the same height as of the sample and images are taken by the software at different angles of the calibrating panel. The panel is tilted in all directions to get a good focus of the DIC cameras from all directions and angles. The software is then used to analyze the images of the panel and once the software is able to view the dots on calibrating panel clearly, the DIC is ready for testing.

Sample Preparation

Since the DIC works on the principal of tracing movements of small dots during heating or cooling, it is very important to prepare the testing sample in such a way that it

has clearly visible dots on its surface. To achieve this, samples of 15mmx51mm were cut out from PCB and painted using matt enamel paint. First, a layer of white paint is applied on the sample and left to dry. Once it has dried, black paint is sprinkled on the white layer carefully in such a way that the surface neither gets very large blots nor very few dots. There should be enough dots on the surface for the DIC to trace their movement during expansion. This sample is then kept inside the oven and thermocouples are then connected to it at 3 different locations to measure temperature during the test and avoid any temperature difference within the sample due to thermal mass.

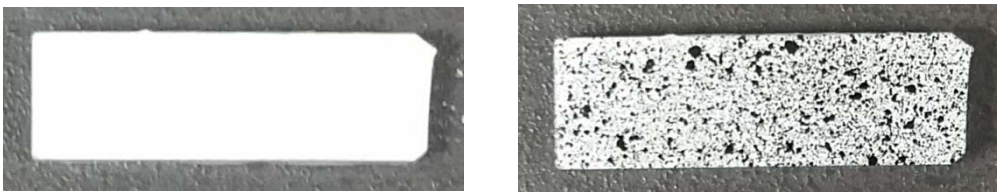


Figure 2-3 Sample For CTE Measurement

2.1.4 CTE Results

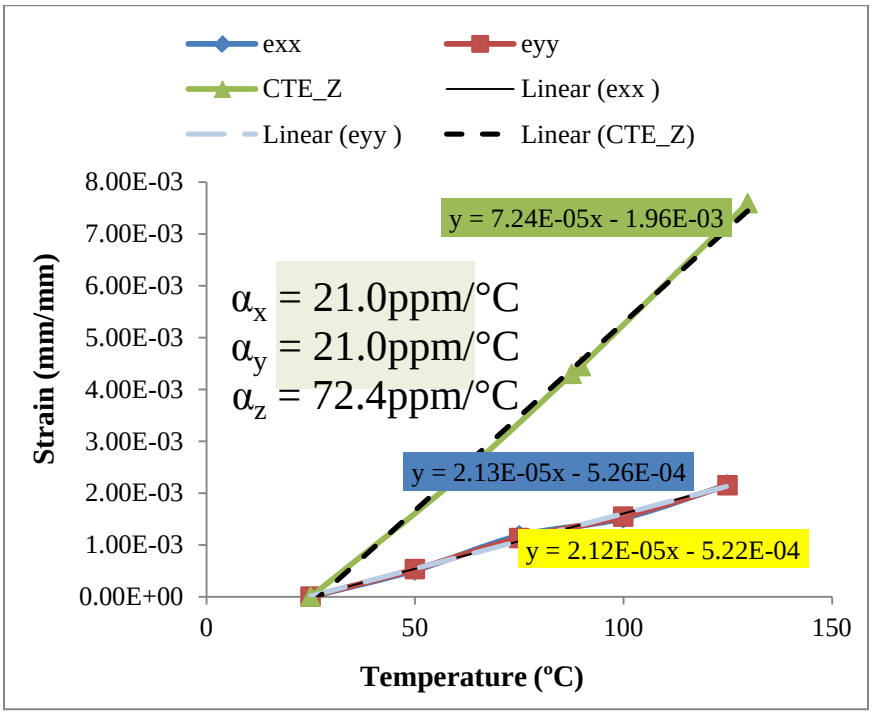


Figure 2-4 In-Plane & Out-of-Plane CTE Plots

2.2 Young's Modulus Measurement

Young's Modulus or Elastic Modulus defines the stiffness of compliance of a material when subjected to tensile or compressive loading. Materials that deform by a small amount when tensile load is applied to them are said to be stiffer as compared to the materials that deform by a considerable amount when tensile or compressive loading is applied to them. Mathematically, Young's Modulus is defined by the stress produced in a material when some strain is applied to it.

$$E = \frac{\sigma}{\epsilon}$$

Where,

E – Young's Modulus (MPa)

σ – Stress (MPa)

ϵ - Strain (mm/mm)

2.2.1 Instron Microtester – Young's Modulus Testing

To conduct Young's Modulus tests, an Instron Microtester of 2kN load cell was used to apply tensile loading to the samples. An extensometer is placed on the sample to measure strain during sample extension. The extensometer is connected to a software to while the instron is also connected and it gives in-situ force-displacement graph during the test. Stress is calculated by dividing the stress from the cross-sectional area of the sample and strain is measured using the extensometer. From the stress and strain, Young's Modulus is calculated for a sample.

Sample Preparation

ASTM standard was followed to prepare dog bone samples for Instron test. The reason for preparing dog bone samples is to make sure there is enough grip section

available for the instron grips to hold the sample tightly during the test. The final shape of the sample is shown in the fig below

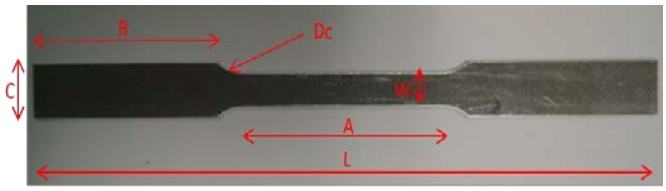


Figure 2-5 Dog Bone Sample

The dimensions of the sample as referred from the ASTM standards is given below

Table 2-1 Dog Bone Dimension

Dimensions	Value (mm)
L - Overall Length	100
C – Width of grip section	10
W – Width	6
A – Length of Reduced Section	32
B – Length of Grip Section	30
Dc – Curvature Distance	4
R – Radius of Curvature	6

2.2.2 Experimental Setup

To measure the Young's modulus of PCB samples, Instron MicroTester 5848 with a max. load cell of 2kN was used to apply force. The grip section of dog bone sample is clamped vertically between the two jaw faces of the instron tester and an extensometer is placed on the samples with its pins gripping the sample tightly. The extensometer pins have an initial gap of 12mm between them. When tensile force is applied on the specimen, the extensometer pins which are tightly gripping the specimen open accordingly and the change in length is measured from where strain is calculated using Instron software.

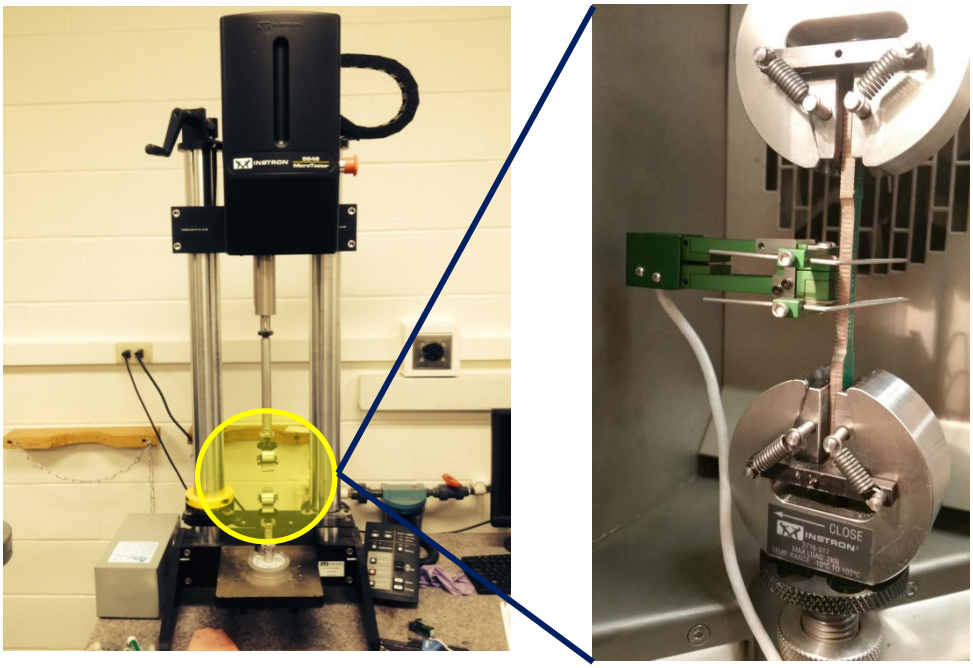


Figure 2-6 Instron Experimental Setup

The test setup and procedure as shown in fig 4 was benchmarked by testing an aluminum sample and calculating the Young's Modulus. The experimental result was compared with the theoretical result and was found to be in complete agreement with the theoretical value. The results are as Follow:

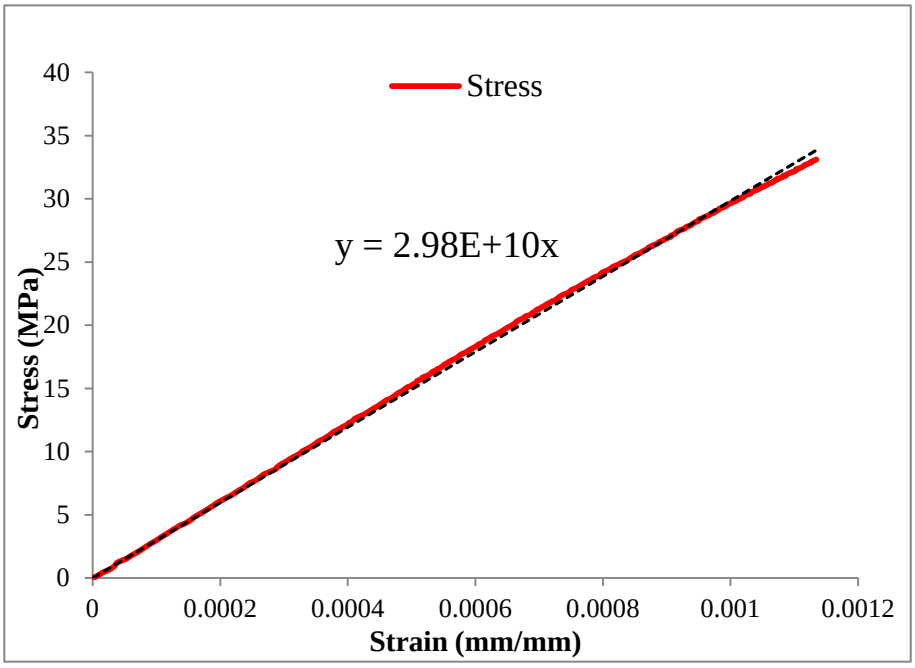


Figure 2-7 Young's Modulus

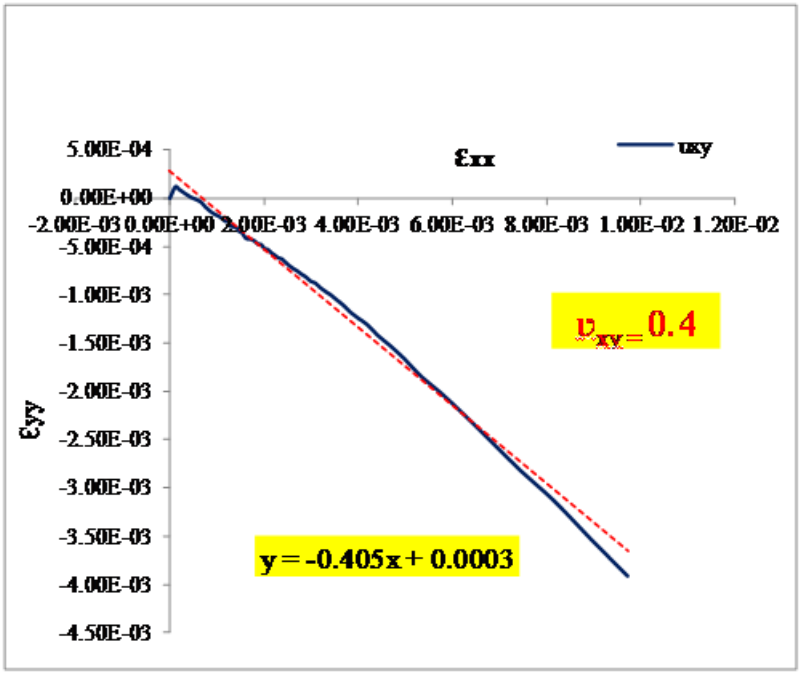


Figure 2-8 Poison's Ratio

Chapter 3

MODEL DESCRIPTION

Full field CPI analysis of a 2 die 3-D flip chip package with TSVs is performed to study the thermo-mechanical response during chip attachment to the substrate. TSVs occupy approximately 1.5% of the chip real estate (CRE) and the TSV diameter is 10µm including the 0.5µm thick dielectric around it. We limited the TSV area to <4% so we don't inadvertently affect the silicon efficiency. Since there is a huge scale difference among the different package components and the full model size is big (~8000 TSVs and µ-bumps) a novel compact modeling technique has been implemented to maintain reasonable computational time. Simulation is performed in 3 steps – a compact global model is formulated and solved; results from the compact global model are used as boundary conditions in the sub-model 1 which is usually the far corner region of the package (critical region) with detailed features such as actual µ-bump interconnects and the TSVs. The sub-model 2 is a section of the far corner unit cell with detailed BEoL stack (metal/via layers). The proposed compact model has the corner region modeled in detail and replacing the inner region of Si/TSVs with an effective Si block (with volume averaged material properties) [12]. A similar effective block for the 1st level interconnects (µ-bumps) has been modeled for the inner region while the corner µ-bump is modeled in detail. The concept of effective block is similar to that demonstrated by Chirag et al. [12] & Mirza et al.[13]. Thermo-mechanical response of the inter-die bond layer (µ-bumps) is analyzed and the "effective block" model is compared and validated with the "full array" version for a smaller footprint. The package footprint is based on a mobile application package (memory-on-logic) footprint (see Figure 3-1)

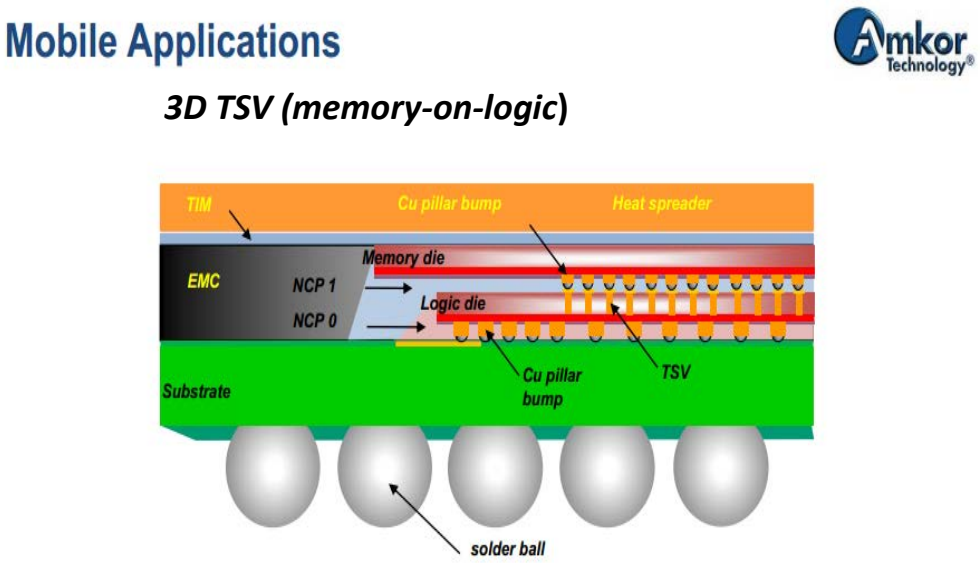


Figure 3-1 Package Footprint

Figure 3-2 and Figure 3-3 show the ANSYS model for a Full Array 3D Package with the BEoL layer in the highlighted region and Quarter Symmetry of Full Array Model respectively. As a part of symmetry boundary conditions, normal displacement to symmetric faces are constrained and center node of bottom is fixed to prevent rigid body motions. All materials in this work except solder (SAC305) and copper (TSVs and BEoL) metal are modeled using linear elastic material properties. Solder is modeled as rate-dependent viscoplastic material using Anand's viscoplastic model, which takes into consideration both creep and plastic deformations to represent the secondary creep of solder. Anand's viscoplastic constitutive law has been used to describe inelastic behavior of lead-free solder. Anand's law accounts for solder's strain-rate and temperature sensitivity through its nine material constants A, Q, ξ, m, n, h0, a, s0, ŝ which are determined by curve-fitting the experimental data. For SAC305 solder, the nine material constants used for SAC305 and modified Anand's block (effective solder block in the

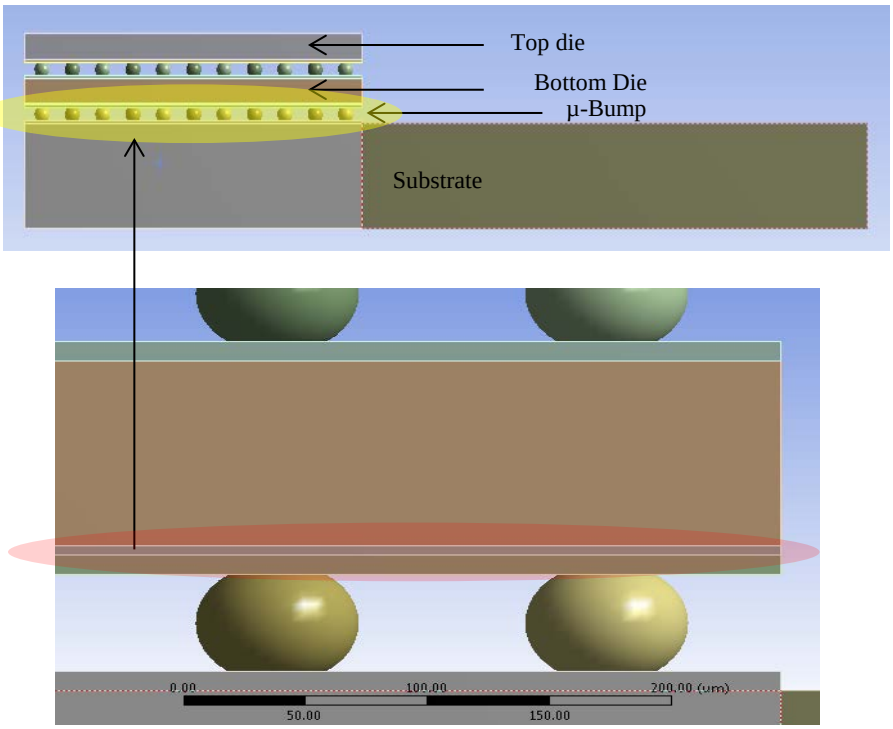


Figure 3-2 Package Cross-section

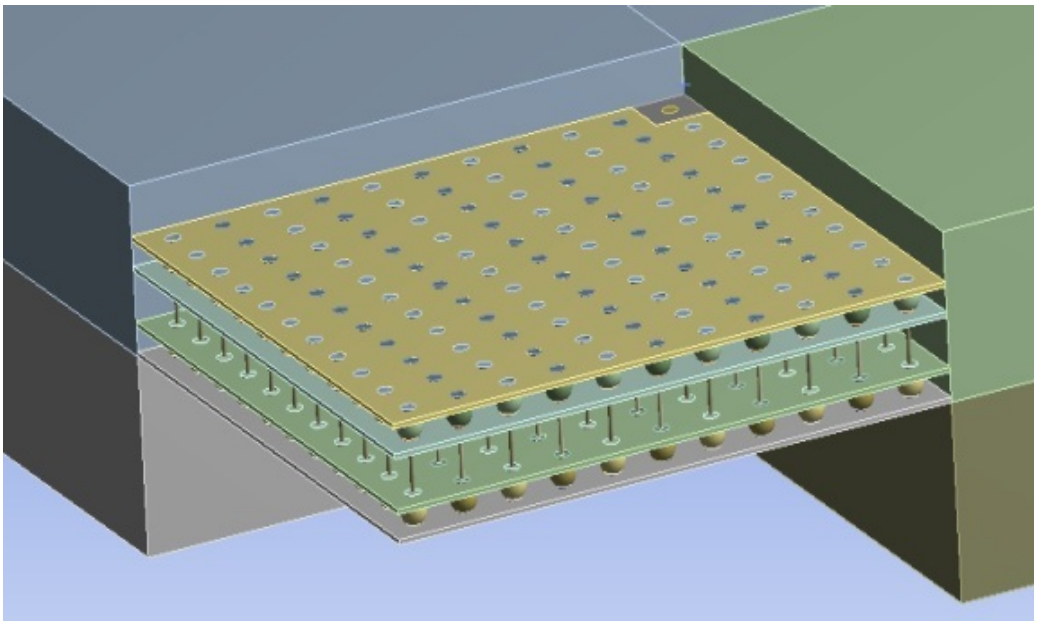


Figure 3-3 Quarter Symmetry Model – Internal View

compact model) are listed below in Table 3-1 and Table 3-2 respectively. Anand's viscoplasticity for solder can be described as follows [14].

$$\frac{d\varepsilon_p}{dt} = A \sinh\left(\xi \frac{\sigma}{s}\right)^{\frac{1}{m}} \exp\left(-\frac{Q}{kT}\right)$$

With the rate of deformation resistance equation

$$\dot{s} = \left[h_0(|B|)^{\alpha} \frac{B}{|B|}\right] \frac{d\varepsilon_p}{dt}$$

where,

$$B = 1 - \frac{s}{s^*}$$

and

$$s^* = \hat{s}\left[\frac{1}{A}\frac{d\varepsilon_p}{dt} exp\left(-\frac{Q}{kT}\right)\right]^n$$

Table 3-1 Anand's Constants for SAC 305

S. No.	Anand's Constant	Units	Value
1	s_0	MPa	1.3
2	Q/R	1/K	9000
3	A	sec^{-1}	500
4	ξ	Dimensionless	7.1
5	m	Dimensionless	0.3
6	h_0	MPa	5900
7	ŝ	MPa	39.5
8	n	Dimensionless	0.03
9	a	Dimensionless	1.5

Table 3-2 Anand's Constant for Effective Block in the Compact Model

S. No.	Anand's Constant	Units	Value
1	s_0	MPa	0.15
2	Q/R	1/K	9000
3	A	sec^{-1}	500
4	ξ	Dimensionless	7.1
5	M	Dimensionless	0.3
6	h_0	MPa	5900
7	$\hat{S}$	MPa	3
8	N	Dimensionless	0.03
9	A	Dimensionless	1.5

As shown in Figure 3-4 sub-modeling has been leveraged to assess the mechanical integrity of the Si/TSV region. In the global model – the TSVs are modeled as one volume (10µm diameter). To minutely study the CPI damage at the BEoL region, a 5µm layer was modeled in the bottom die (sub-model 1). The results of the full model were imported as the cut boundary conditions for sub-model 1 shown in Figure 3-5.

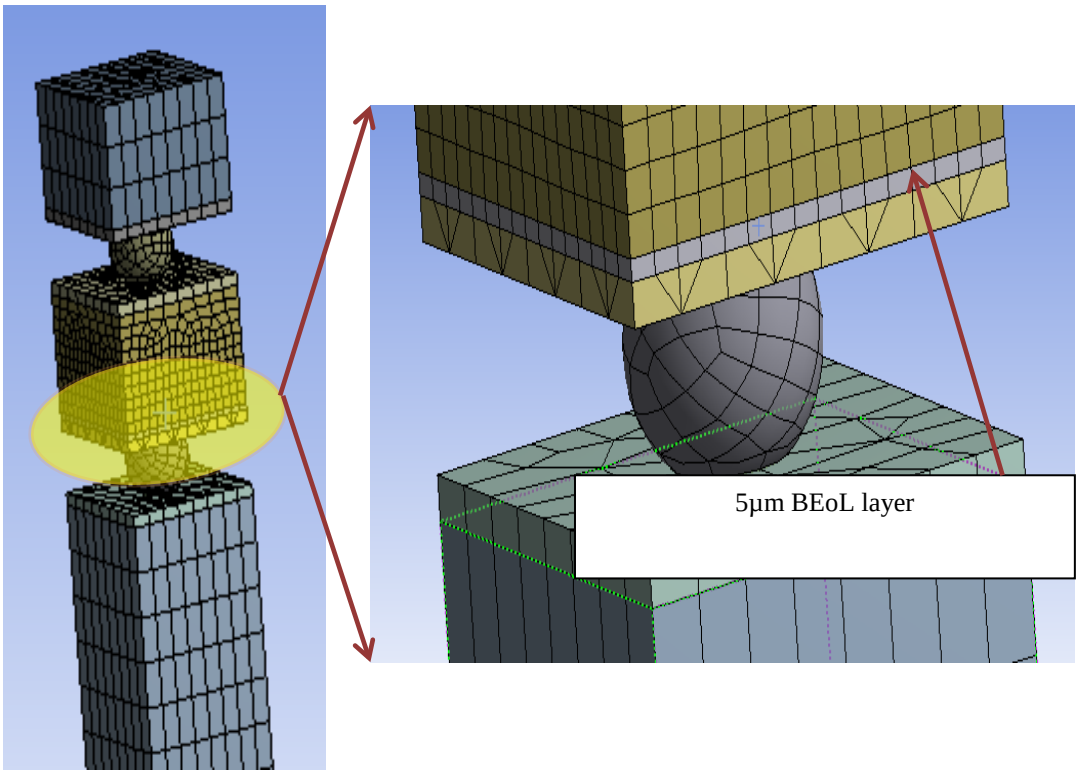


Figure 3-4 Sub-Model 1

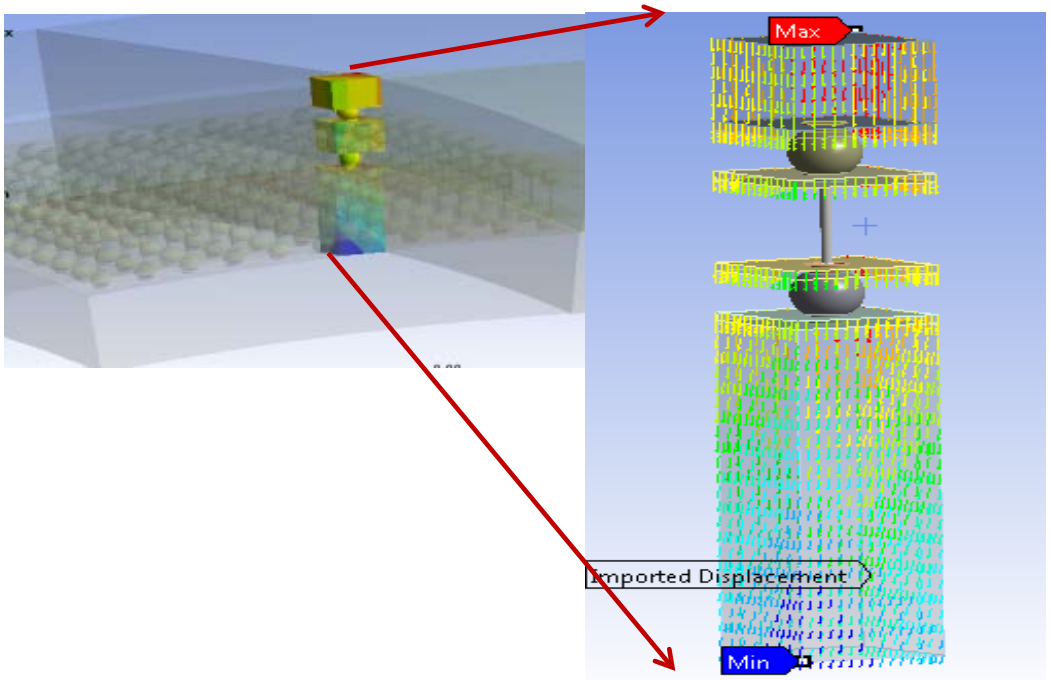


Figure 3-5 Sub-Model 1 Cut Face Boundary Condition (Corner Region)

To determine the failure location precisely in the BEoL region, sub-model 2 was leveraged which has a detailed layup of metal and low-k dielectric layers. It incorporates the BEoL stack (metal/dielectric layers) to study the localized TSV/BEoL CPI interaction. Starting from the bottom of the 5µm layer in sub-model 1, 11 more layers of cumulative thickness of 1.4µm were sliced inside the chip. The 11 layers consist of 5 metal and 6 dielectric layers alternatively stacked on top of each other with the dielectric layers on top and bottom as shown in Figure 3-6.

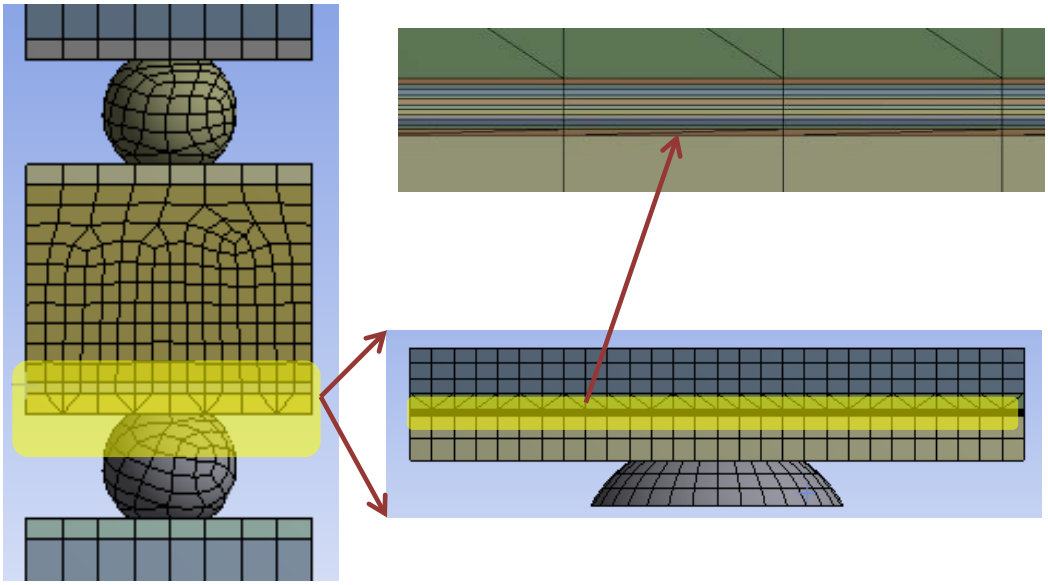


Figure 3-6 Package Cross-Section With 11 Layers

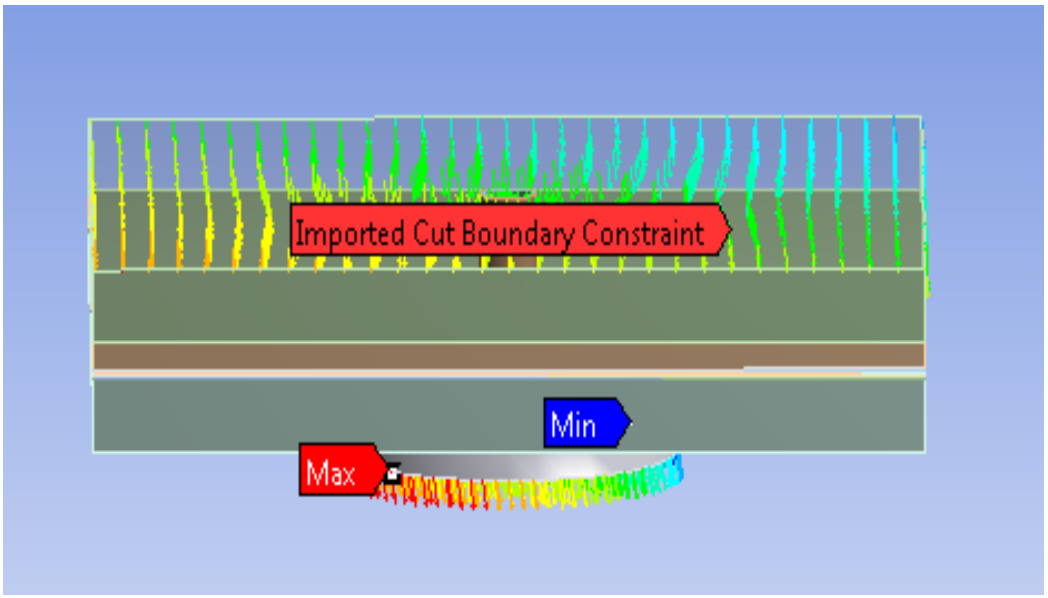


Figure 3-7 Sub-Model 2 Cut Face Boundary Condition (Corner Region)

Chapter 4

COMPACT MODELING TECHNIQUE

A typical mobile application HDI 3-D TSV package consists of thousands of TSVs and µ-bumps with fine pitches. Performing a thermo-mechanical simulation to estimate the warpage and the localized stresses in the TSV region and the µ-bumps is quite cumbersome (computationally expensive) and sometimes impossible. Also, if an isolated study of the TSV/µ-bump region is performed (just 1 unit cell) then the package warpage and the length effect on the damage cannot be estimated.

As demonstrated by Mirza *et al*. [7] And Chirag *et al.* [8], a compact modeling methodology was used and, the µ-bumps and the TSVs are replaced with an effective block with lumped material properties. The compact model resulted in significant reduction of the mesh size from 140449 elements to 5900 elements (most of the elements reduced were for the viscoplastic solder and the elastic-plastic Cu TSV), thereby leading to a huge computational time reduction. Figure 4-1 below is showing development of compact modeling. In compact model all the solder balls and TSV's except unit cell were replaced by block. The highlighted part in figure is showing how solder bumps and TSV's were replaced by block and unit cell at corner is kept as it is. Figure 4-2 is showing comparison between meshing of array model and compact model.

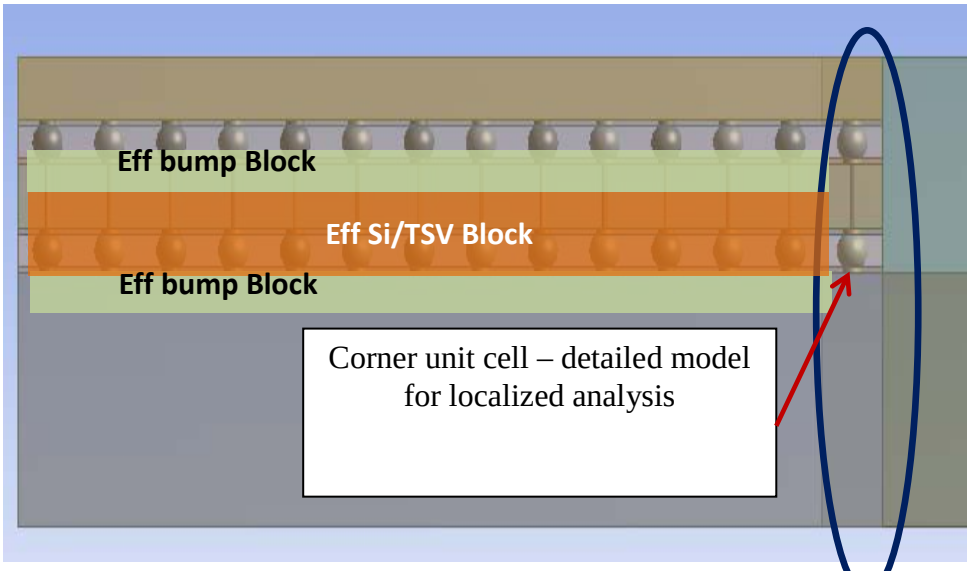


Figure 4-1 Compact Model Cross-Section (TSVs / µbumps Replaced With A Block)

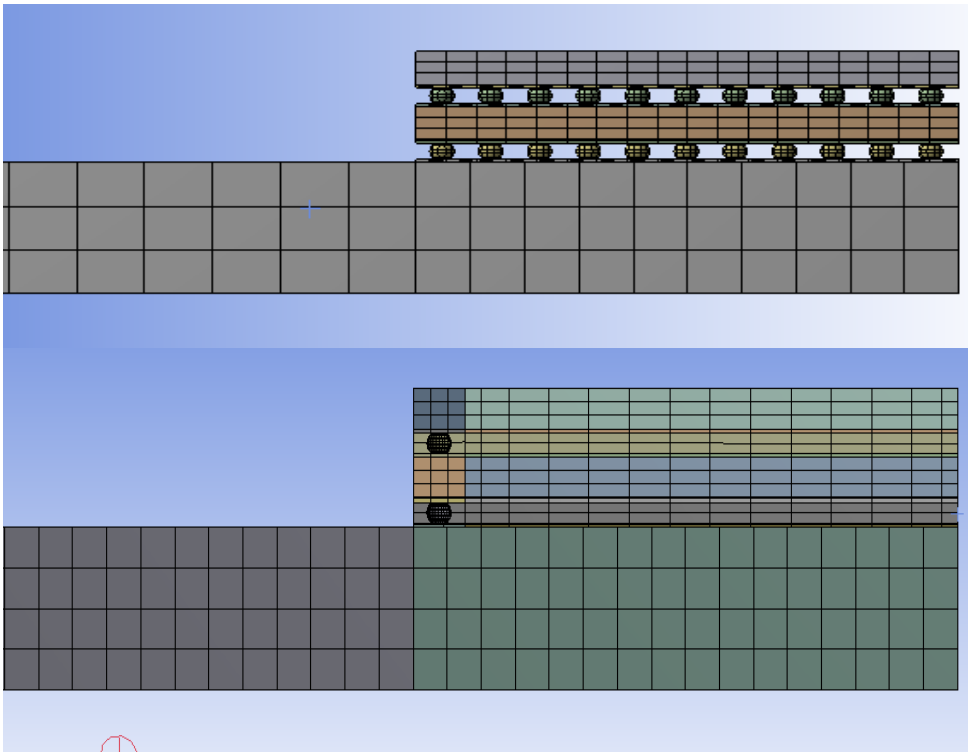


Figure 4-2 Array & Compact Model Meshing Comparison

Chapter 5

RESULTS AND DISCUSSION

5.1 Validation of Compact Modeling

The compact modeling methodology is successfully leveraged in this paper and different output parameters including global package warpage, stress-stain distribution in the µ-bumps (inter die strata) and stress-strain distribution in Cu-TSV region is studied. Using the sub modeling technique stress and strain distribution at the Si/TSV region and inter die µ-bumps during chip attachment to the substrate is exhibited. To closely study the stress-strain distribution at the BEoL region, a submodel-2 has been employed and the stress-strain distribution is studied in 150nm dielectric layer. The loading was the reflow condition for the 3D TSV package when it is being attached to the substrate, 200°C to Room (for Pb-free SAC 305 Alloy). *Validation of Compact Modeling with Full Array mode is shown in following Figures:*

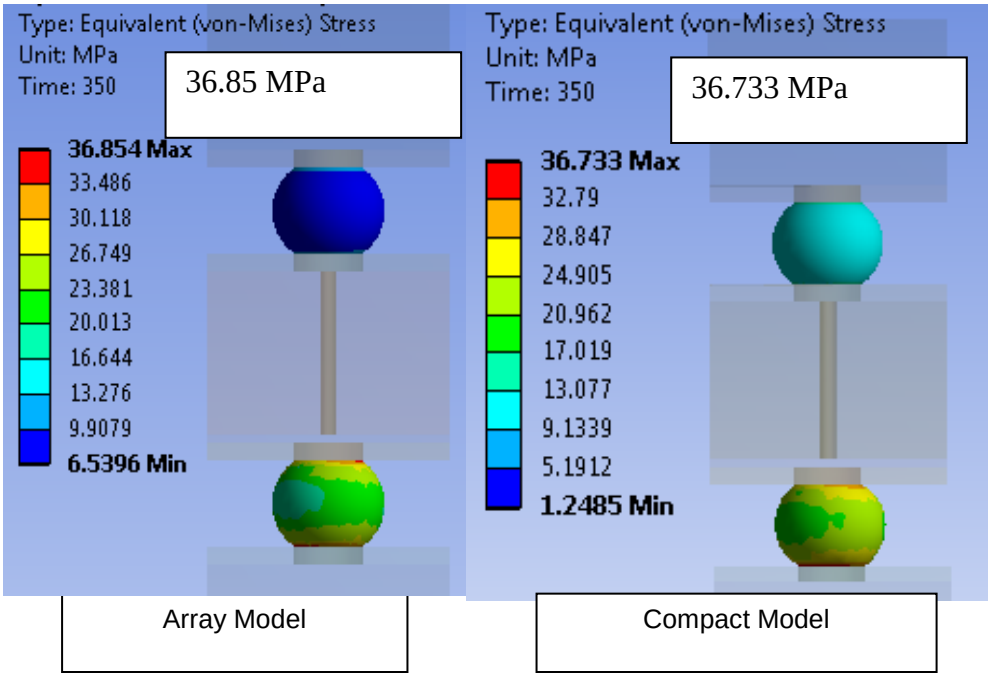
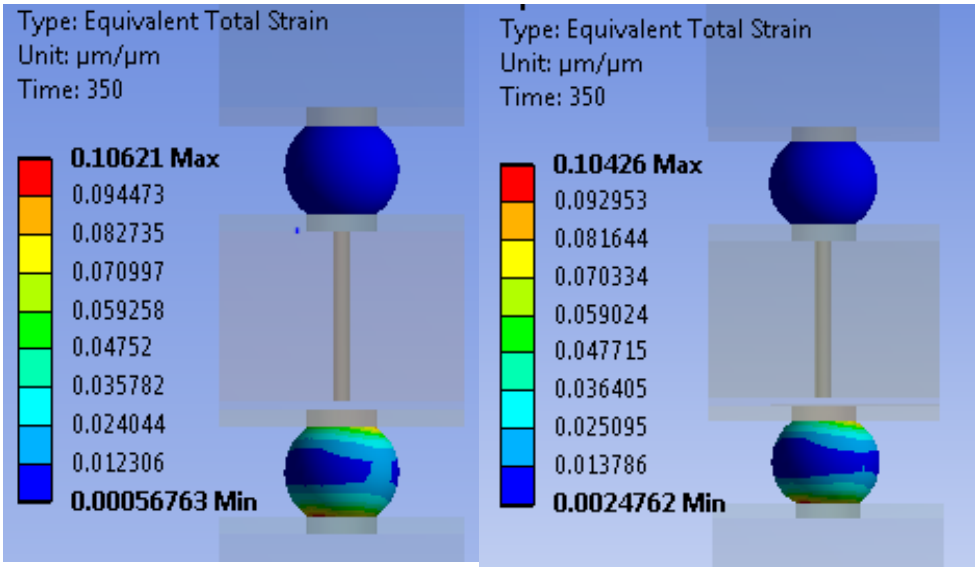


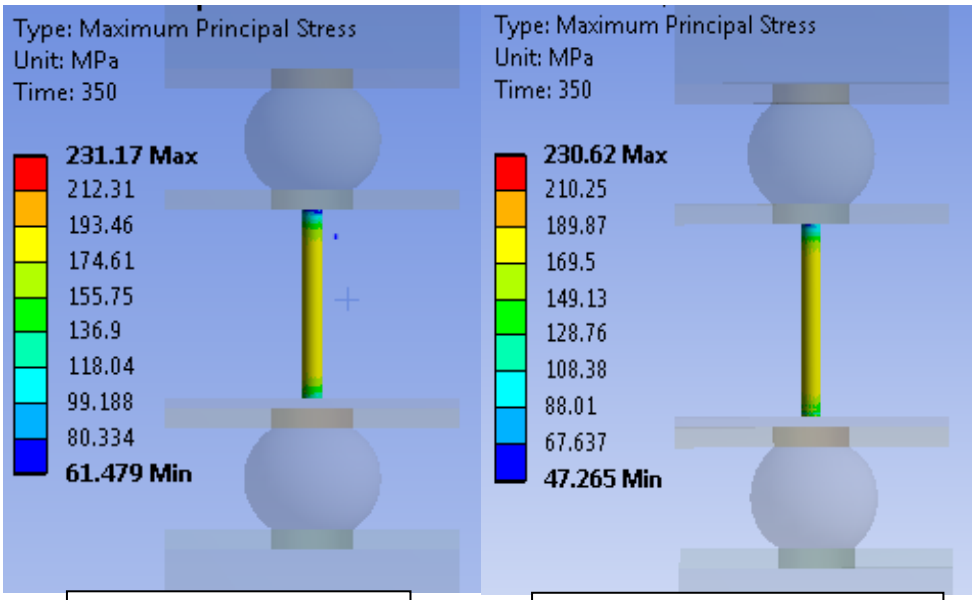
Figure 5-1 Equivalent Stress (Sub-Model-1)



Array Model

Compact Model

Figure 5-2 Equivalent Strain (Sub-Model-1)



Array Model

Compact Model

Figure 5-3 Principal Stress Sio2 Region (Sub-Model-1)

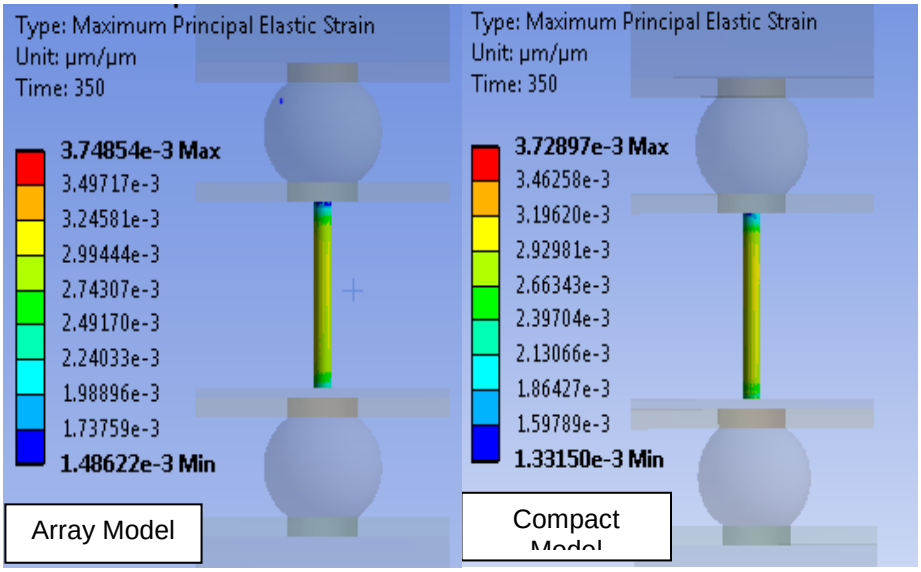


Figure 5-4 Principal Strain Sio2 Region

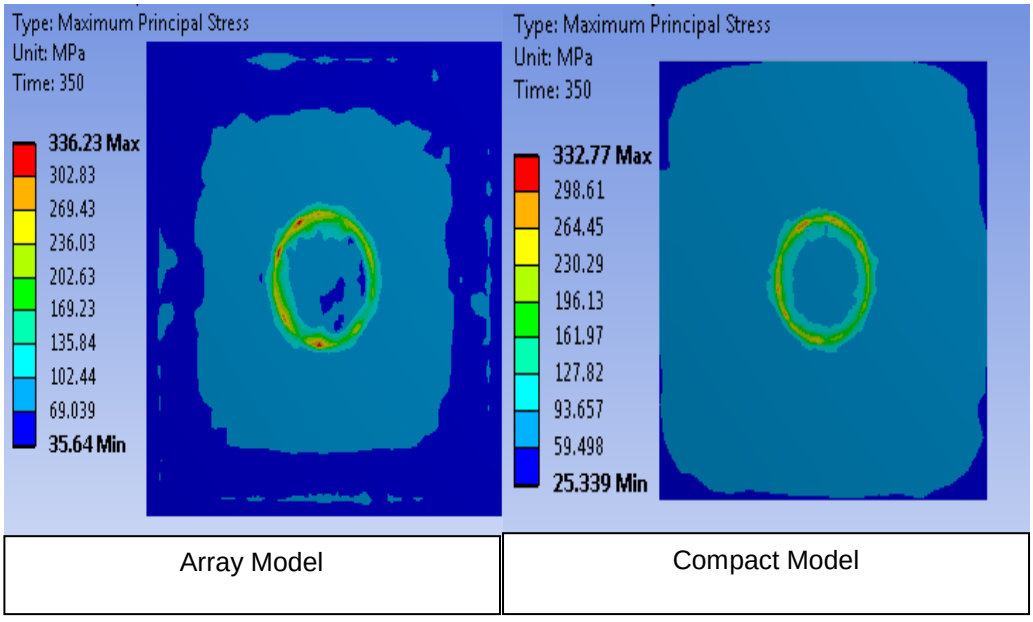


Figure 5-5 Principal Stress In Most Vulnerable Layer (Sub-Model2)

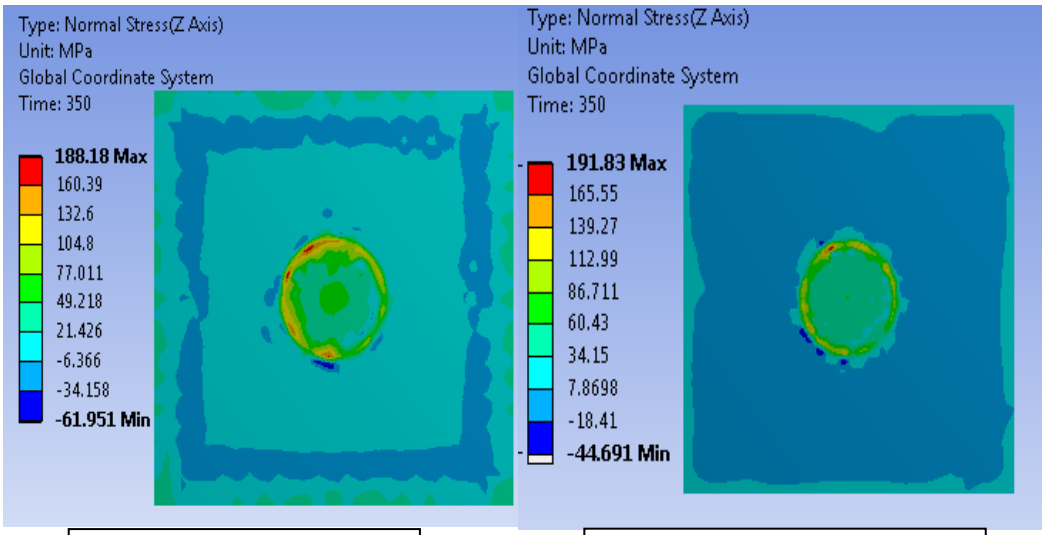


Figure 5-6 Normal Stress In Most Vulnerable Layer (Sub-Model2)

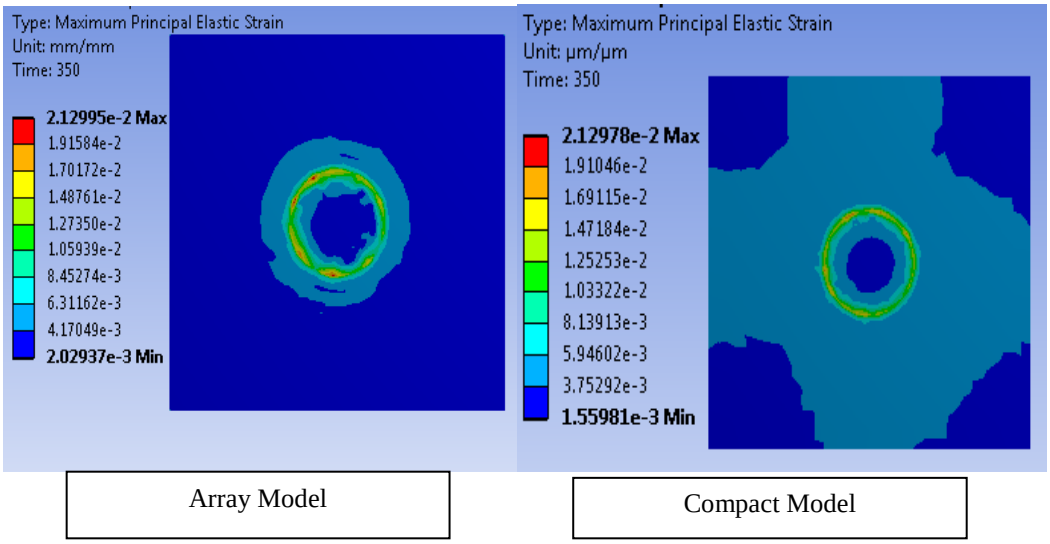


Figure 5-7 Principal Strain In Most Vulnerable Layer (Sub-Model2)

It is clearly demonstrated by Figure 5-1 through Figure 5-7 that the compact model prediction is in good agreement with the full array configuration. Interestingly, there is a significant variation between the global von-mises stress for the two configurations but the more accurate sub-model results are in excellent agreement. The magnitude and the distribution of the mechanical response is very similar between the 2 configurations with a maximum error of 4% in the principal strain. Table 3 is the summary of the various output correlation parameters between the array and the compact model configurations.

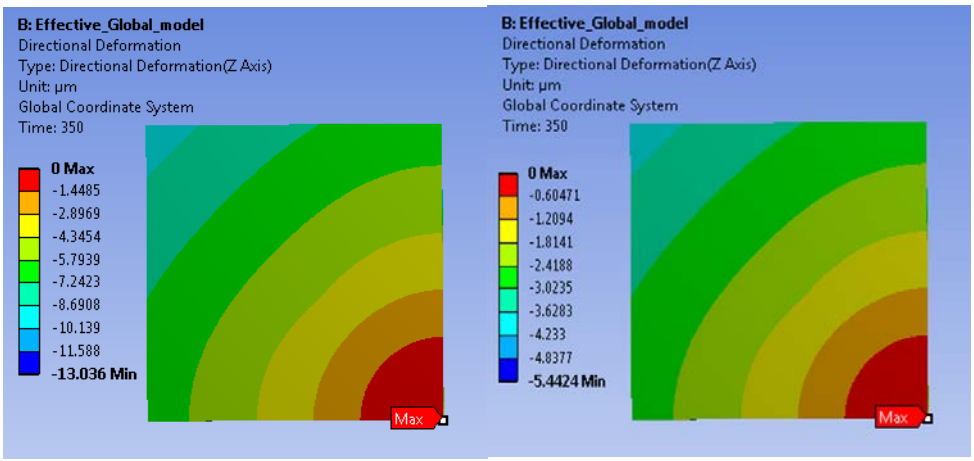
It is to be noted that the array configuration (quarter symmetry model) with only 121 TSVs and 242 µ-bumps took about 14 hours to solve on a 24GB RAM system with high-performance-computing (HPC) capability while the compact model for a similar footprint solves in few minutes (>50x reduction in the solution time). Now, we can see that if a similar analysis is to be done for a larger die 3-D TSV footprint with fine pitch TSVs/µ-bumps, it will be impractical or may not be even possible in some cases, thereby warranting a compact modeling approach.

Table 5-1 Correlation Parameters Summary

Damage Parameter	**Array Model**	**Compact Model**	**% Error**
Von Mises Stress in Solder (MPa)	36.85	36.733	0.3
Equivalent total strain in Solder(mm/mm)	0.106	0.104	0.02
Principal Stress TSV SiO_2 Region (MPa)	231.17	230.62	0.02
Principal Strain TSV SiO_2 Region (mm/mm)	3.75e-3	3.73e-3	0.005
Principal Stress in most vulnerable layer (MPa)	336.23	332.77	1
Normal Stress in most vulnerable layer (MPa)	188.18	191.83	1.93
Principal Strain in most vulnerable layer (mm/mm)	2.19e-2	2.129e-2	3.19

5.2 Study Of Effect Of Die To Substrate Ratio On Mechanical Integrity

As compact model has already been validated in previous section, in this study I have leveraged only compact model for analysis. To study the effect of die to substrate ratio, I ran two separate case by changing die size. Actual die size in this study was 3mm*3mm and substrate was 7.5mm*7.5mm. Then two models were developed with die size 4mm*4mm & 2mm*2mm and with same substrate size. The results obtained in this study were in agreement with literature. Increased die size showed more warpage and smaller die showed less warpage. Figure 5-8 below is sowing global model warpage comparison between both the models.



Die Size: 4*4mm Die Size: 2*2mm

Figure 5-8 Warpage

Figures below are showing result comparison for increased and reduced die size. Figures on left are 4mm*4mm die and on the right are 2mm*2mm die.

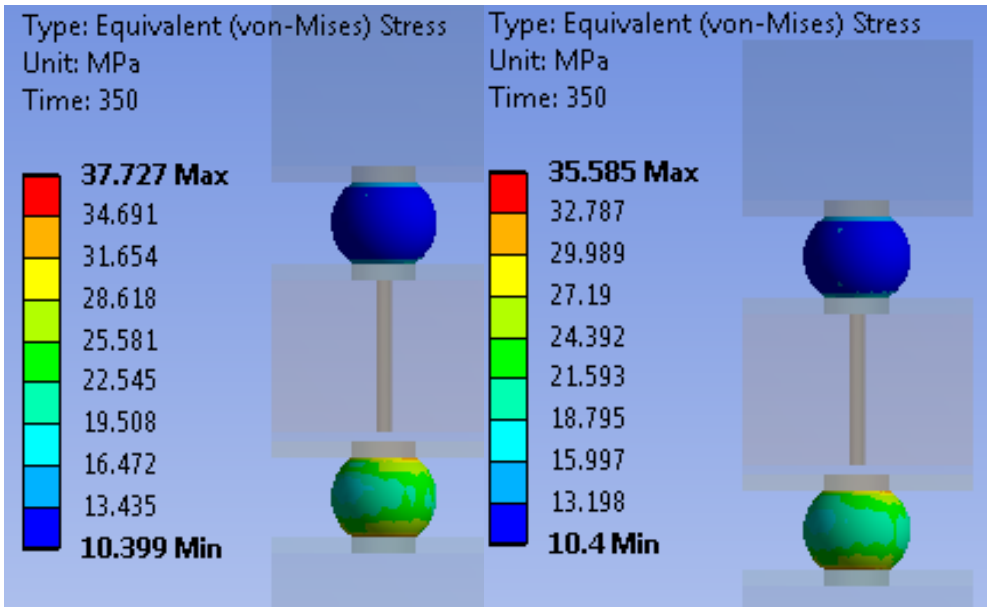


Figure 5-9 Equivalent von-Mises Stress

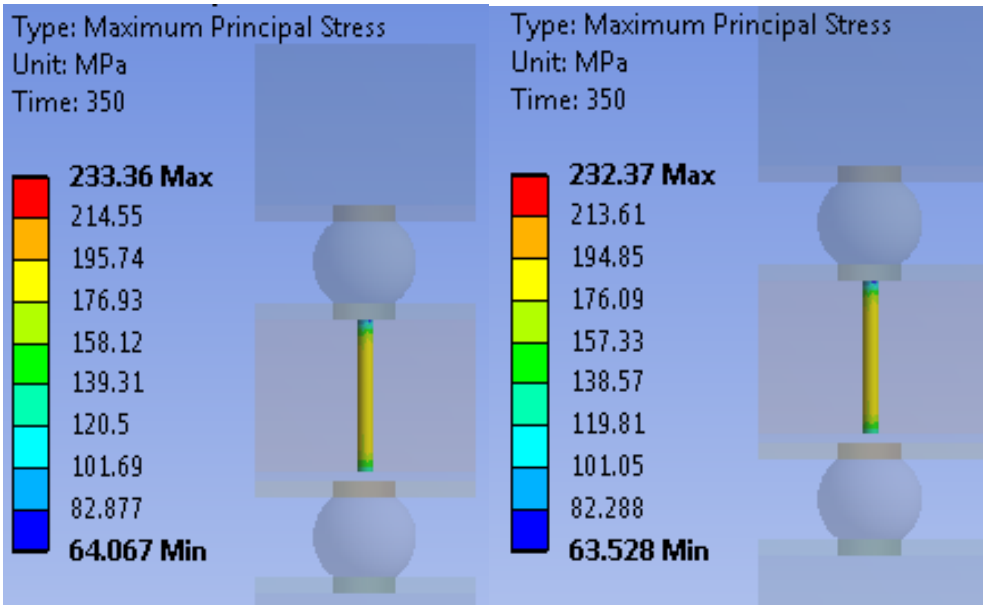


Figure 5-10 Maximum Principal Stress

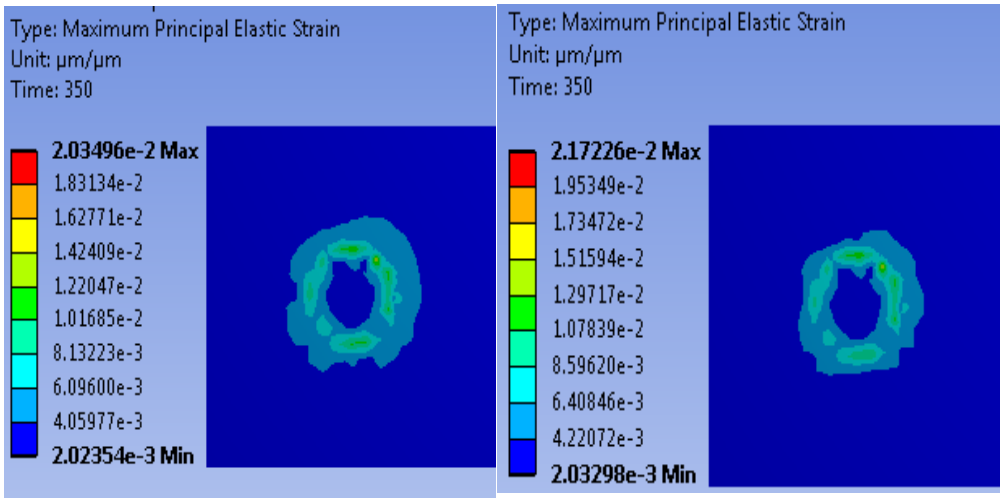


Figure 5-11 Maximum Principal Elastic Strain

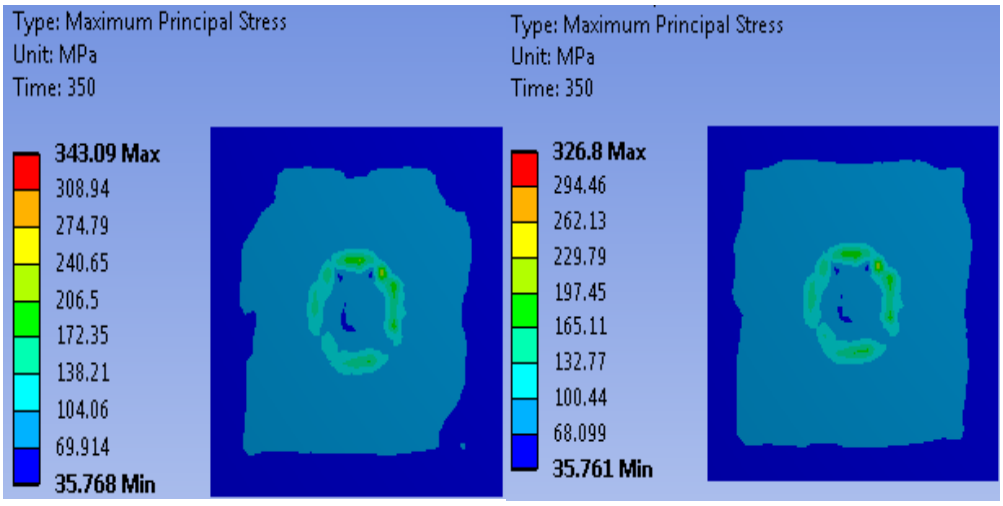


Figure 5-12 Maximum Principal Stress

Chapter 6

CONCLUSION

Full field 3D compact modeling methodology has been successfully demonstrated to assess the mechanical integrity of the BEoL Stack in a 3D TSV package. The feasibility of the compact modeling technique has been shown by validating the output damage parameters (Von Mises Stress/Strain in Solder, Maximum Principal Stress/Strain in TSV/SiO_2 Region, Principal Stress, Principle Strain and Normal Stress in most vulnerable low-k dielectric layer in the BEol stack) with the full array configuration. All the damage parameters in the compact model exhibit excellent agreement with the full array configuration with a maximum error of 3.2% in the principal strain. The compact model results in a 50X improvement in the solution time with negligible compromise in the prediction accuracy. As expected the location of the maxima in the BEoL via layer is along the µ-bump footprint in both the modeling approaches. Study of effect of die to substrate ratio is going in line with literature. Hence compact model is validated and can be used directly In future study.

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BIOGRAPHICAL STATEMENT

Pavan Rajmane received his Bachelor's degree in Mechanical Engineering from the University of Pune in the year 2011. He then decided to work for Precision Appliances, Pune, India as a Design Engineer for 1 year, from 2011 to 2012. He decided to pursue his Master's in Mechanical Engineering by enrolling in University of Texas at Arlington in Fall 13. There he joined the Electronics MEMS & Nanoelectronics Systems Packaging Center (EMNSPC) under Dr. Dereje Agonafer and developed a keen interest in reliability and failure analysis of electronic packages. His research interest includes reliability, fracture mechanics, thermo-mechanical simulation and material characterization. During his time, he was an integral part of the SRC funded project where he worked closely with the industry liaisons. Upon graduation, Pavan plans to pursue his career in the semiconductor industries.