3D INTERCONNECTS FOR DIE AND WAFER STACKS

by

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ABSTRACT

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3D integration results from the ever demanding trend towards smaller, lighter and lower cost packaged devices. With the present System-on-chip (SOC) technology reaching its limitation in terms of functionality and cost, effort are being concentrated on exploring the third dimension, i.e. 3D integration that provides a volumetric packaging solution for higher integration and performance. It can be achieved through die stacking and wafer stacking. A key technology to realize the potential of stacking is implementation of vertical electrical interconnects between die and wafer stacks.

This thesis discusses the approach to form vertical interconnects between wafer stacks through solder reflow and wafer level bonding. The processing recipe to achieve wafer bonding using photosensitive Benzocyclobutene (BCB) is developed. The fabrication process for formation of electrical interconnects through solder metal reflow

is elaborated and surface profiles of the reflowed solder metal are included. This thesis also discusses die level bonding for hermetic packaging of a MEMS device. Vertical electrical interconnections between dies are formed through thermo-compression bonding. A process is developed to achieve die bonding through a fluxless soldering technique. Experiments were conducted using two different solder compositions bonding results with each are discussed.

Furthermore, low frequency and high frequency analysis of interconnects is performed. This analysis is used as guidelines to select the correct dimension for interconnects specific to the application.

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CHAPTER 1

INTRODUCTION

1.1 Problem Statement

For the last few years, strong efforts are being made to miniaturize microelectronic systems. As a result, chip scale packages, flip chips and multi-chip modules are now commonly used in a great variety of products, e. g. mobile phones, hand-held computers and chip cards, etc. The current microelectronic applications require more complex devices with increased functionality. The performance trends of integrated circuits are moving towards faster circuits in the giga-hertz range [1]. The driving force behind the spectacular advancement of the integrated circuit technology has been the exponential scaling of the feature size, with migration to smaller devices. As integrated circuits enter the giga-hertz operating frequency range, various speed related challenges have become more evident [2]. The major impediment to fulfill the Moore's Law are length of the interconnect wires since ICs are using a greater fraction of clock cycles in charging these interconnect wires. Moreover, length of the interconnect wires introduce the effect of parasitics, which are mainly in the form of resistance, inductance and capacitance.

The electronic industry has used a combination of low-k dielectric to alleviate the wire capacitances and copper damascene processes to reduce the resistance. However, as minimum features size decrease below 50nm, Cu damascene and low-k

dielectric are expected to limit the performance of the integrated circuits [1]. Hence, a different approach is used to reduce the interconnect parasitics, which is 3D integration.

The large number of long interconnects needed in 2-D structures are replaced by short vertical interconnects, known as 3D interconnects. The 3D interconnect technology by-passes the large wire parasitics by shortening the interconnect length. It is a viable solution for increasing the electronic device functional density and reducing total packaging costs. 3D integration also has the potential to integrate heterogeneous wafers fabricated using different technologies such as DRIE microfluidics, surface micromachining MEMS, and semiconductor IC's.

In contrast to semiconductor IC packaging, MEMS packaging is challenging because most of the MEMS devices need to be housed in costly hermetic packages to exclude oxygen and moisture that can cause wear friction problems [3]. Hermetic packaging is particularly required in case long shelf life (20 – 30 years) is desired for the packaged devices. A common practice for packaging of MEMS devices is to bond a recessed cap die to another die hosting the device. However, conventional bonding techniques such as fusion or anodic bonding cannot be employed due to the high processing temperatures and high electric fields required [4]. Hence a low temperature process needs to be developed but at the same time it should provide hermetic packaging. Fluxless soldering is a viable solution to this problem.

1.2 Motivation

Wafer-level packaging (WLP) is a true technological revolution that will bring about a paradigm shift in the cost and reliability of microsystems. Major economic savings are possible if packaging and testing are done before the wafer is diced. WLP is being driven by the cost reduction that results from fabricating packages in a batch mode, rather than assembling individual discrete components. In creating the package, additional layers of material may be deposited over the active surface of the die, resulting savings in size and weight [5]. Moreover, as the wafer size goes up and device layout shrinks, wafer processing costs remain about the same, hence resulting in a decrease in the cost per die.

Technology based on wafer level manufacturing is 3D wafer stacking technology. 3D integration results from the ever demanding trend towards smaller and lower-profile, lighter and lower cost devices that require package miniaturization. With the present System-on-chip (SOC) technology, the silicon die is packed with most functions possible on a single planar die. As a result the SOC technology is becoming prohibitively expensive. As line geometries shrink to 40 nm and beyond, critical issues like higher costs and increased demands for thermal management have become more evident. Thus, there is a push towards leveraging the third dimension of silicon i.e. the Z-axis. 3D packaging technology provides a volumetric packaging solution for higher integration and performance. It results in size and weight reduction - vertical stacking reduces the number of chip-to-board interconnections and the area required for chips

and inter-chip traces, enables higher electrical performance through shorter interconnect architectures with stacking and reduces overall system level costs [6].

Wafer-level 3D integration allows heterogeneous integration of wafers fabricated using disparate processes and substrates. The finished wafers are stacked, bonded, and interconnected through vertical interconnections.

The key to realize 3D wafer stacking is 3D interconnect technology, which involves connecting in three dimensions at via or interconnect level. Dies can be connected in 3D through external wires along the periphery of the dies. However the same cannot be done with wafers. Currently, vertical vias between wafers are formed by: 1) bonding the wafers, 2) followed by wafer thinning, 3) deep reactive ion etching (DRIE) through the stack, and 4) deposition or plating of interconnect metal.

In this thesis, a second approach is used to form vertical interconnections between wafers or dies stacks. This approach involves formation of solder bumps before bonding the wafers, followed by remelting of the bumps during bonding to form interconnection between the wafers. This approach is commonly used in flip-chip bonding, but we used it in this research to fabricate the 3D interconnections between wafer stacks.

Microelectromechanical Systems (MEMS) consist of mechanical devices and machine components ranging in size from a few microns to a few hundred microns [7]. Unlike IC packages, MEMS packages needs to interface with the environment for sensing, interconnection and actuation, and hence they needs to be protected against harsh environment, such as temperature, moisture, magnetic field and electromagnetic

interference [3]. MEMS devices mostly have three dimensional structures and moving elements and require a cavity package to provide free space above the active surface of the device. Some MEMS devices require a hermetically sealed package to attain long shelf lives of 20 years or more. However, the high surface to volume ratio of the cavity makes it difficult to establish and attain the desired atmosphere inside the package. Hence the materials selected for the seals must be leak free, impermeable and not sources of out-gassing during assembly and the operating lifetime for the device [7].

Epoxy and polymers cannot be used for packaging since they are considered non-hermetic or near-hermetic seal materials. On the other hand, solders can be used as a seal ring material to provide a hermetic package for the device. A fluxless soldering process needs to be developed to package the dies since flux residues pose a risk to hermeticity.

Research is presently going on at the Automation & Robotic Research Institute, at UTA on wafer bonding and formation of 3D interconnects through wafer and die stacks and assembly and packaging of MEMS devices. The results presented in this thesis are a part of this on-going research effort.

1.3 Objective

The objective of this thesis is to accomplish wafer level bonding and form 3D electrical interconnects through wafer stacks; die level bonding and hermetic sealing for packaging of MEMS device and die level interconnects through thermo-compression bonding.

Wafer Stacking: The objective is to align and bond two wafers using adhesive polymer glue called photosensitive Benzocyclobutene (BCB), which has an excellent properties such as high mechanical strength, good planarization, low dielectric constant, low curing temperature and no reflow during bonding, etc. The processing parameters and conditions for photosensitive BCB need to be investigated to understand their impact on bonding. A new approach of solder reflow is to be investigated to form vertical interconnections between the bonded wafers. A fabrication process need to be established to combine the two processes of wafer bonding and solder reflow. The choice of solder material is to be made with the consideration that reflow temperature is bound by the curing and glass transition temperature of BCB. Factors affecting solder reflow, e.g. oxidation of solder, inert ambience and temperature profile need to be studied.

Die Level Bonding: Hermetic sealing of MEMS device is required for their longer shelf lives i.e. 20 – 30 years. Solder alloy of Au-Sn are investigated as sealing materials around the perimeter of the dies to provide hermetic packaging. Flux cannot be used to for soldering since its residues are difficult to remove, which in turn create voids in the bond. Hence the objective was to establish a fluxless soldering technique and to understand the bonding process parameters such as temperature, pressure, dwell time and surface cleaning and their effect on bond strength. Vertical electrical interconnects between the bonded dies are formed through thermo-compression bonding. The interconnect design guidelines in terms of diameter, length and pitch need

to be investigated, in order to understand their impact on electrical and thermal characteristics.

1.4 Contributions

The contributions to this thesis were:

1. BCB Processing: I worked to develop the processing recipe for photosensitive BCB (Cyclotene-4022-35). Process parameters such as wafer surface preparation, spin speed, bake time and temperature, exposure time, developing time and curing time and temperature were optimized to obtain a plain coating and uniform thickness over 4" Si and Pyrex glass wafers. The samples were prepared at the NanoFab Research and Teaching Facility, UTA. The patterned wafers were aligned and bonded at the Stanford Nanofabrication Facility by a colleague.

2. Fabrication of electrical interconnects for wafer stacks: I designed and fabricated 3D electrical interconnects for the bonded wafers. Metal was deposited using thermal evaporator. Further reflow characterization for the fabricated interconnects was performed. Reflow was done on a hotplate set up and also through laser. The interconnect fabrication was done at the NanoFab Research and Teaching Facility, UTA, whereas reflow experiments were performed at Texas Microfactory, at Automation & Robotics Research Institute. After evaluating the success of the BCB patterning and bonding and electrical interconnects formation, fabrication for the two processes was combined.

3. Die Level bonding: I worked to establish a fluxless soldering process for hermetic packaging of a MEMS device. Preliminary experiments were carried out on a hot plate set up, which was placed inside a glove box. The die bonding was later carried out using a Flip Chip bonder installed at the Texas Microfactory, Automation & Robotics Research Institute. Bonding parameters were identified with their impact on hermeticity and bond strength. Electrical interconnection between the bonded die were formed through thermo-compression bonding.

4. Design and Modeling of Interconnects: Impact of interconnect design (diameter and length) and choice of solder metal on the electrical characteristics of interconnect was studied. A low frequency analysis was conducted through finite element modeling of interconnect. The temperature profile across interconnect was plotted. The skin effect at high frequencies was also studied. Mask design of the dies for fabrication was done using L-Edit.

As a result of this research, a novel approach to 3D wafer stacking has been developed. Solder reflow has been established as a successful approach to form vertical interconnects between wafers bonded with photosensitive BCB. Also a fluxless bonding technique has been developed to hermetically package MEMS devices. Modeling of these 3D interconnects has provided us with the basic guidelines to select the correct interconnect dimensions specific to the application.

CHAPTER 2

BACKGROUND

2.1 Wafer-to-Wafer Bonding

Wafer-to-wafer bonding is a mature technology in microelectronics but is increasingly relevant for zero-level packaging of Micro-Electro-Mechanical System (MEMS) and microfluidics. Anodic and fusion bonding of silicon and glass wafers provide very strong, hermetic wafer bonds, but with very strict requirements for surface preparation and process conditions. Anodic bonding is mainly restricted to electrically conducting (sodium rich) glass with a CTE close to that of Silicon wafer. A high temperature is 350°C – 400°C is applied across the substrates and is high enough of make the sodium ions mobile. The presence of mobile sodium ions is not desirable for most microelectronic devices. Moreover, anodic bonding requires very low surface roughness (~20nm) and high electrostatic field (100~1kV), which can damage sensitive devices and bond unwanted wafer areas [8]. Fusion bonding is usually performed at high temperatures (~1000°C) and it requires very clean and flat surfaces [9]. Contrary to these two bonding methods, adhesive wafer bonding is being widely used for wafer-to-wafer bonding applications requiring low processing temperatures.

2.1.1 Adhesive Wafer Bonding

Direct wafer bonding methods i.e. anodic and fusion bonding, are high temperature and high voltage processes and it is difficult to bond wafers containing IC's with metal interconnect levels using these bonding techniques. Hence, adhesive wafer bonding (utilizing a low-k polymeric glue layer), which is a low temperature process, facilitates the wafer bonding for 3D integration. The adhesive layer should provide a seamless interface, be sufficiently thin to minimize via aspect-ratio, be sufficiently reactive to form a chemical bond and be thermally stable after bonding [11].

Various dielectric polymer glues, such as HTR3, PI2555, PI2610, S1818 and Benzocyclobutene (BCB) have been proposed for wafer bonding. However the properties of BCB – excellent mechanical strength, very low out gassing, less sensitivity to surface preparation, low dielectric constant, high optical transparency, high thermal stability, high solvent resistance, low cure temperature and no reflow during bonding (for partially cured BCB) makes it and excellent polymer for wafer bonding [11]. Also compared with other glues, BCB show a larger fraction of void-free bonded area, high bond strength as determined using the razor blade test, and good bonding integrity [12].

During adhesive wafer bonding, the intermediate polymer adhesive deforms to fit the surfaces to be bonded. BCB is a thermosetting polymer that undergoes cross-linking during curing to form a stable polymeric network. BCB flows for a short time during the cure process to achieve cross-linking but does not re-melt or reshape itself after curing [13]. Since around 2000, individual wafer bonding experiments have been performed by a few research groups around the world, including Frank Niklaus at the

Royal Institute of Technology in Sweden, Dan Popa and James Lu at Rensselaer Polytechnic Institute, Troy, NY, USA, and Khalil Najafi at the University of Michigan, USA. The experiments performed were with dry-etch BCB (Cyclotene 3000 series) supplied by Dow Chemicals. The 3000 series consists of a BCB polymer, approx 35% cross-linked, dissolved in the solvent mesitylene. In particular, soft baked BCB (35% cross-linked) and partially cured (43% cross-linked) were used to investigate BCB reflow during bonding. It had been found that soft-baked BCB reflows during bonding. In contrast, partially cured BCB maintains a high viscosity and does not reflow during the adhesive wafer bonding process [14].

Similar work has been done by Tae-Joo Hwang, Dan Popa and James Lu at the Rensselaer Polytechnic Institute, Troy, NY, USA with fully cured (95–100% cross-linked) dry-etched BCB (Cyclotene 3000 series). From the experiments, it has been established that hard cured BCB does not reflow during bonding. The hard cured BCB has a glass transition temperature (>350°C) which is higher than the bonding temperature of 250°C. This solid like property of hard cured BCB does not allow adhesive reflow during bonding. However, voids were formed between the bonded surfaces due to particle contamination.

For this current research, photo-sensitive BCB (Cyclotene 4000 series) is used for bonding wafers. Its photosensitive nature eliminates an additional step of patterning using photo resist. The photo and dry-etchable Cyclotene resins have similar physical and mechanical properties. However, photosensitive BCB has even higher viscosity (192 cSt @ 25°C) compared to the dry-etch BCB (14 cSt @ 25°C). Bonding

experiments were carried out with BCB cured at 95%, 85%, 75%, 60% and 55% to study its reflow during bonding and bond quality in terms of void formation. BCB curing is a function of time and temperature. Refer to Figure 3.2.

The processing was carried out using 4” Silicon and Pyrex glass wafers. The process flow is summarized below:

1. Clean wafers with Acetone and Isopropyl Alcohol and bake them at 160°C on a hotplate for 30 min.

2. Spin coat adhesion promoter AP3000 (Dow Chemicals)

3. Spin coat BCB 4022-35 (Dow Chemicals)

4. Soft bake at 65°C for 90 sec

5. Expose to UV light

6. Pre develop bake at 60°C for 5 min

7. Develop using DS3000 (Dow Chemicals) heated to 40°C for 1 min

8. Dip in DS3000 at room temperature for 30 sec

9. Blow dry the wafers

10. Hard cure BCB at 250°C for 1 hour

11. Plasma etch BCB for <30 sec

12. Manually pre-align the two wafers

13. Load the aligned wafers into the bonding chamber

14. Close and evacuate the chamber to 10 mbar -5

15. Heat the wafers to 250°C

16. Increase the pressure

17. Cool down to below 100

2.2 Formation of 3D Electrical Interconnects

Performance, multi-functionality and reliability of microelectronic systems are mainly limited by the wiring between the subsystems, causing a critical performance bottleneck for future IC generations. 3D interconnect technology has provided a base to overcome these bottlenecks [15]. It lowers the overall interconnection length, parasitic capacitance, system power consumption and system compactness.

One of the two approaches for formation of electrical interconnects between wafer stacks are through-via interconnects. Traditional approach to form through-wafer via formation is utilizing either laser drilling or wet etch processing using KOH solution. However, KOH etches preferentially along the <111> Si plane and results in sloped side walls which limits the aspect to ~0.7. Furthermore, KOH and similar etching agents are inherently incompatible with CMOS technology [16]. In contrast via with higher aspect ratios can be achieved through deep reactive ion etching (DRIE). With DRIE etch depths of 20μm – 300μm can be achieved with vertical side walls with higher etch rates as compared to wet etching.

Electrical interconnects can be created by etching through hole vias through the bonded wafers. In this approach, functional components are fabricated on separate wafers which are bonded following wafer alignment. This is followed by top wafer thinning and inter-wafer interconnection by drilling vias through the stacked wafers. Initially, the two processed wafers are aligned to each other. Wafer-to-wafer alignment

is a basic manufacturing issue for achieving a high inter-wafer interconnects density. The alignment accuracy of the wafer directly affects the smallest allowable pitch of the vertical vias. For good alignment wafer mechanical specifications such as flatness, bow and warpage in the starting wafers and after front-end and back-end IC processing are needed. Most of the wafer-level 3D technology platforms use IR or split-field optics to achieve wafer alignment [17].

Wafer bonding of a fully processed wafer requires intimate contact over the entire surface and compatibility with subsequent thinning and inter-chip interconnection processes. After bonding, the back of the top wafer is thinned to reduce the length of the vertical vias to be formed. The inter-wafer interconnections are then created using copper damascene patterning, which is high aspect ratio (HAR) etching, via filling and CMP process. Holes are created through the thinned wafers where vias need to be placed. These holes are then filled with metal. Lastly, the top of the wafer is passivated. The added complexity of the process posses' reliability and yield issues [18].

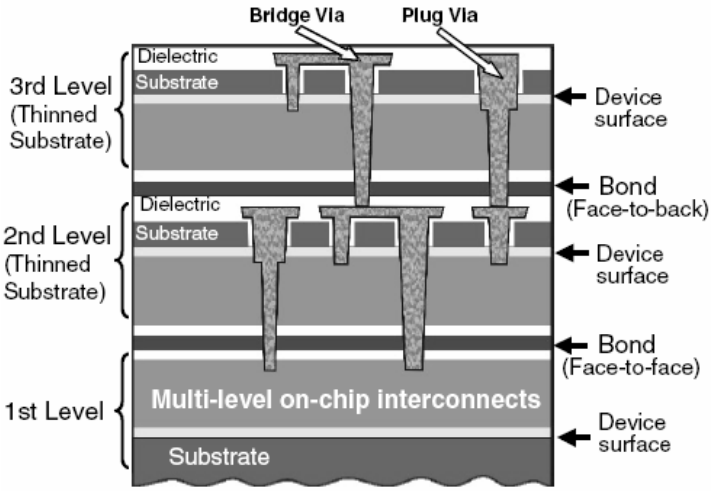


Figure 2.1 3D integration concept using wafer bonding and vertical inter-chip vias [19]

Another approach to vertical interconnections is InterChip Via/Soldering (ICV) technology. It involves formation of inter-chip vias on fully processed wafers by etching through passivation and ILD layers. Vias are filled with tungsten (W) and back etched to form metal plugs. Contact windows are opened for forming lateral interconnections. The wafer is then bonded to a handling wafer and thinned to open vias from the rear side. A dielectric layer of polyimide is deposited for electrical isolation. Cu is electroplated to cover the entire surface and electrical contacts are formed by isolation trenches in the copper layer. The known good dies are separated and stacked on a bottom wafer coated with a bi-layer of Cu/Sn and soldered at a temperature of 300°C. The handling wafers are finally removed and bond pads are opened [20].

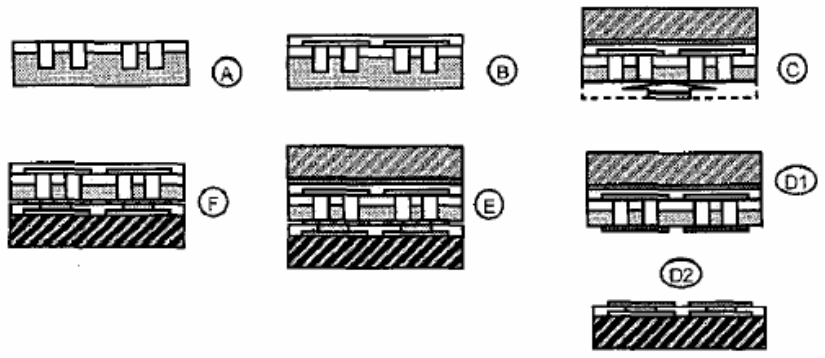


Figure 2.2 Process flow for InterChip via (ICV) technology [20]

2.2.1 Formation of Electrical Interconnects through Solder Reflow

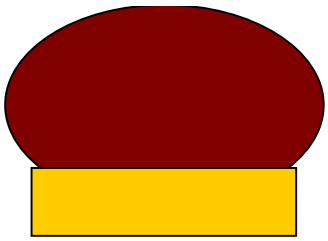
In our approach, electrical interconnections between wafers stacks are formed through solder reflow. Wafers are bonded using a 3μm (after curing) thick layer of photo sensitive BCB. The thickness of the solder bump after reflow should be less than

the thickness of the BCB layer used for bonding the wafers. In addition, the solder reflow temperature is bounded by the curing and glass transition temperatures of BCB.

Solder reflow is a process in which the metal is heated beyond its melting temperature. The surface tension of clean liquid solder is sufficient to overcome gravity and force the liquid into the lowest free energy configuration – a perfect sphere [21]. The surface of the solder needs to be free of oxides since they prevent reflow. The reflow temperature is usually 20°C – 30°C higher than the melting temperature. Figure 2.3 shows the schematic of solder metal before and after reflow. The solder metal is deposited over a base metal which acts as an interface between the wafer and the solder. It provides the following functions:

1. Defines the area for solder bump formation
2. Acts as an adhesion layer between the solder metal and the substrate
3. Acts as a solder diffusion barrier to prevent material migration

(a)



(b)

Figure 2.3 Schematic of solder (a) before reflow and (b) after reflow

Various lead free solder alloy compositions have been researched, with reflow temperatures in the above specified range for our application. A metallic alloy is a mixture of one metal with another. Table 2.1 summarizes the different solder compositions with their melting and reflow temperatures.

Table 2.1 Melting and reflow temperatures of various alloy compositions

Solder Alloy	% Composition	Melting Temp (°C)	Reflow Temp (°C)
Sn/Au	95/05	217	230
Au/Sn	80/20	280	320
In	100	157	200
Sn/Cu	92.3/0.7	227	245-257
Sn/Ag (E)	96.5/3.5	221	245-255
Sn/Ag/Cu	95.5/3.8/0.7	217	240-250
Sn/Ag/Bi	91.7/3.5/4.8	205-210	240-250
Sn/Ag/In	95/3.5/1.5	218	240-250
Sn/Ag	90/10	221	240-250

In our research, we have worked with two different solder compositions of Au and Sn – 95Sn/5Au and 80Au/20Sn. Figure 2.4 shows the binary Sn-Au equilibrium phase diagram [22].

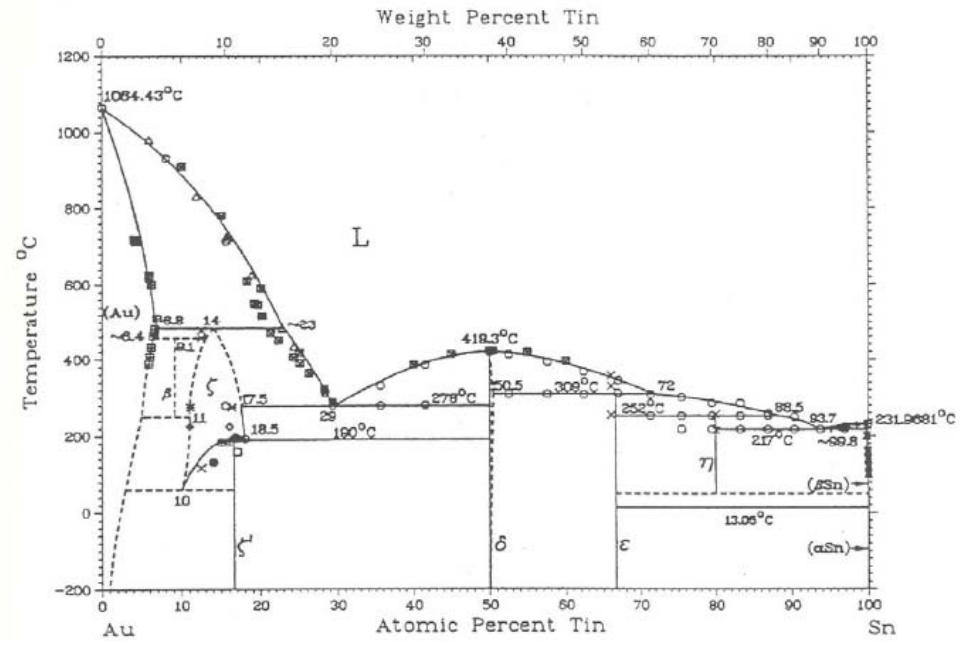


Figure 2.4 Au-Sn equilibrium phase diagram [22]

As exhibited in the phase diagram, the Au-Sn alloy has two eutectic compositions. A eutectic alloy composition is that in which the alloy has the same liquidus and solidus points.

1. 80% wt. Au and 20% wt. Sn: This is one of the most popularly used compositions in electronic and photonic packaging due to its excellent fatigue resistance and creep resistance [14]. This composition is classified as a hard solder with a eutectic melting temperature of 280°C

2. 90 % wt. Sn and 10% wt. Au: This composition is categorized as a soft solder and has a melting point of 217°C. Being a Sn rich composition, this solder composition is easily prone to oxidation and hence difficult to reflow. For our process, we have used 95% wt. Sn and 5% wt Au solder composition, which has a near eutectic temperature of 217°C.

Different solder deposition techniques and manufacturing processes are described below. The deposition techniques are:

1. Evaporation/Sputtering: Solder metal is evaporated by thermal evaporation or e-beam evaporation. The wafer is patterned with photo-resist prior to evaporation. A lift-off is performed to remove the metal from unwanted areas. Sputtering can also be used in place of evaporation. Vacuum processes are limited to depositing extremely thin layers of metal i.e. <5μm due to their slow deposition rates and long processing times. Also, the process is expensive in terms of expenditure for equipment and materials and throughput is limited.

2. Electroplating: It is a popular alternative to the evaporation process because of its lower equipment and processing costs. Thickness greater that 50μm can be deposited using this technique. Wafer is patterned with photo resist prior to plating and the thickness of metal deposited is determined by the height of the photo resist. Resist is stripped off after plating [23].

2.3 Overview to Die Bonding

One of the most pronounced developments in electronics today is the increase in telecommunications, RF and opto electronics, of which MEMS is the most interesting and challenging [24]. Research efforts in bonding technology for MEMS applications was mainly focused on bonding processes such as anodic bonding and silicon–silicon direct bonding. These processes impose limitations substrate preparation, particulation tolerances and processing temperatures. To overcome these limitations

various intermediate layer bonding processes have been developed. Low melting temperature glasses, polymers and metals such as gold have been used as intermediate layers. However, the use of solders as an intermediate layer is gaining importance, due to the emergence of flip chip technology, where the device chip is flipped and bonded to substrate using solder bumps. Solder compositions under consideration, typically consists of indium, tin, lead, bismuth and their alloys. However, the use of lead-based alloys is not desirable due to environmental concerns [25].

To produce flip-chip solder joints, the use of flux is necessary to remove oxides on the molten solder and base metal, and to shield the solder surface from further oxidation. In future flip chip devices, the gap between the chip and the substrate is getting small and it becomes difficult to completely remove flux residues. The residues trapped in the gap can degrade the performance of the device, possess reliability risks due to corrosion and have a negative effect on the upcoming optoelectronic technology [26].

Since most MEMS include moving structures, one of the requirements for their packaging includes providing a cavity for operation. Some MEMS functions include interaction with the surrounding environment and need to be protected against moisture in the ambience as it deteriorates MEMS device performance. Hence hermiticity of the package is required in some applications. It plays an important role with respect to the reliability and the long-term drift characteristics of the device. However, flux residues create voids in the soldered joint, which is a killer for hermetically packaged devices [27].

Hence a fluxless soldering technology is required for packaging MEMS devices, photonic devices, biomedical devices, and for hermetic packaging, where the use of fluxes is prohibited. It has been estimated that 700 million dollars a year could be saved on military microelectronics alone if a fluxless process were to be adopted which had the effectiveness of a highly activated flux [28].

Another important aspect in the design of a hermetic package is realization of electrical interconnects; connecting the MEMS device to its electronic circuitry placed outside the package. Hermetically sealed packages require that the active signal lines travel through the seal region to make electrical connection to the device. This can require additional processing, which increases the cost and complexity. Conventional single MEMS-chip packaging frequently limits the over all density and performance of MEMS systems [29].

These limitations can be overcome by providing vertical chip-to-chip to electrical interconnection in addition to active signal lines running through the perimeter seal. The interconnections through the package must conform to the hermetic sealing. Through hole vias are created to allow access to each of the active signal lines on the device wafer. These vias can then be connected to a metal line that runs to a bond pad at the periphery of the MEMS chip.

2.4 Conclusion

Wafer to wafer bonding using BCB has been discussed in this chapter. The bonding conditions have been summarized. The two different approaches to form

electrical interconnects between wafer stacks have also been elaborated. Lastly, this chapter discusses about die level packaging and the challenges associated with it.

CHAPTER 3

WAFER LEVEL BONDING AND FORMATION OF 3D ELECTRICAL INTERCONNECTS

Benzocyclobutene (Cyclotene 4022-35) is an adhesive polymer used to bond a Si wafer to another Si wafer or Pyrex glass wafer. This grade of BCB being photosensitive in nature can be patterned using standard lithographic technique. The 3000 series consists of a BCB polymer, approx 35% cross-linked, dissolved in the solvent mesitylene [14]. The polymer is supplied by Dow Chemicals. Two different compositions for Au-Sn solder were researched as interconnect material for wafer stacks. The metal is deposited though thermal evaporation. Processing recipes for BCB processing and metal deposition are explained in details in the following sections. Reflow results for the solder are also included.

3.1 BCB Processing

The fabrication process requires a number of established steps such as photolithography, lift-off, e-beam deposition, thermal evaporation, reflow.

Photo-sensitive BCB resin, Cyclotene 4022-35, is supplied as solutions of B-staged monomers in Mesitylene. The structure of the monomer is shown in figure 3.1. Cyclotene 4022-35 is designed for a film thickness range of 3.7 – 6.9µm. Spin speed of 4000 rpm is employed to achieve the range of thicknesses of 4.1µm after soft bake and 2.9µm after curing. Because of the high viscosity of 4022-35, higher ramp rates of 1000

rpm/sec are required using spin coating to obtain a uniform coating over the wafer. Low ramp rates (<800 rpm/sec) result in striations in the BCB film, which in turn causes voids during bonding.

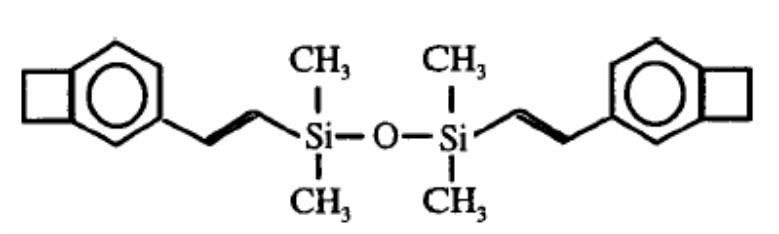


Figure 3.1 BCB monomer structure [30]

This grade of BCB can be exposed and patterned, thus eliminating an additional patterning step using photo resist. Adhesion promoter AP3000 is used, to improve the adhesion of BCB to a silicon or Pyrex glass surface. After spin coating BCB on the wafer surface and it is soft baked on a hotplate. It is a negative acting resin, and is sensitive to I-line, G-line and broad band radiation. Before developing, BCB coated wafers require a pre-develop bake. Without a pre-develop bake the development end point increases as the film sits at room temperature, and is thus dependent on the time delay between the process steps [31]. The pre-develop bake resets the develop end point to the same time, regardless of the time delay between the soft bake and develop.

Patterned BCB layer is developed using DS3000. It is recommended to heat the developer to 40°C to increase the development. At room temperature the development time may be an hour or more, whereas when heated the development time is the range of a few minutes. The wafer is then rinsed with DS3000 stored at room temperature for

stopping the develop process and rinsing the wafer. A water rinse for the wafer is not required [31].

3.1.1 Recipe for BCB Processing and Curing

Wafer Clean:

1. Wafers were rinsed with Acetone and Isopropyl Alcohol and baked at 160°C on a hotplate for 30 min. This is done to evaporate and solvent left on the wafer surface.

BCB Processing:

1. Spin AP3000 at 3000 rpm for 30 sec
2. Statically dispense the BCB on the wafer
3. Spin at 4000 rpm with a ramp rate of 1000 rpm/sec for 30 sec to achieve a thickness of 4.1µm.
4. Soft bake at 65°C for 90 sec
5. Expose for 24 sec
6. Bake at 60°C for 5 min
7. Develop using DS3000 heated to 40°C for 1 min.
8. Rinse in the room temperature DS3000 for 30 sec.
9. Post bake at 100°C for 1 min

Bonding experiments were carried out with BCB cured at 95%, 85%, 75%, 60%, 55% and 45% to study its reflow during bonding and bond quality in terms of void formation. Curing was carried out in a Blue M Oven purged with Nitrogen. BCB curing

is a function of time and temperature. Figure 3.2 below shows the oven curing curves for Cyclotene 4000 Resin [32]. Thickness of the Thickness of the BCB layer is reduced to 3µm after curing.

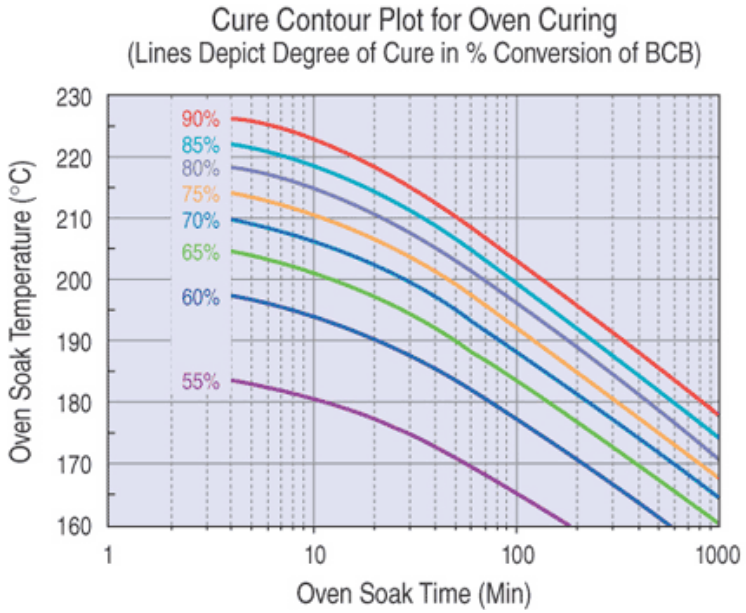


Figure 3.2 Oven curing of Cyclotene 4000 as a function of time and temperature [32]

BCB Curing: Recipe for hard curing i.e. 95% cured and partial curing (i.e. 75% cured) of BCB is given as follows:

Hard Cure (95%):

1. Ramp to 150°C in 15 min
2. Soak at 150°C for 15 min
3. Ramp to 250°C in 1 hour
4. Soak at 250°C for 1 hour
5. Cool down to 50°C

Partial Cure (70%)

1. Ramp to 150°C in 15 min
2. Soak at 150°C for 15 min
3. Ramp to 210°C in 1 hour
4. Soak at 210°C for 40 min
5. Cool down to 50°C

Figure 3.3 below shows some optical microscope pictures of alignment marks patterned using photo-sensitive BCB with the above mentioned recipe.

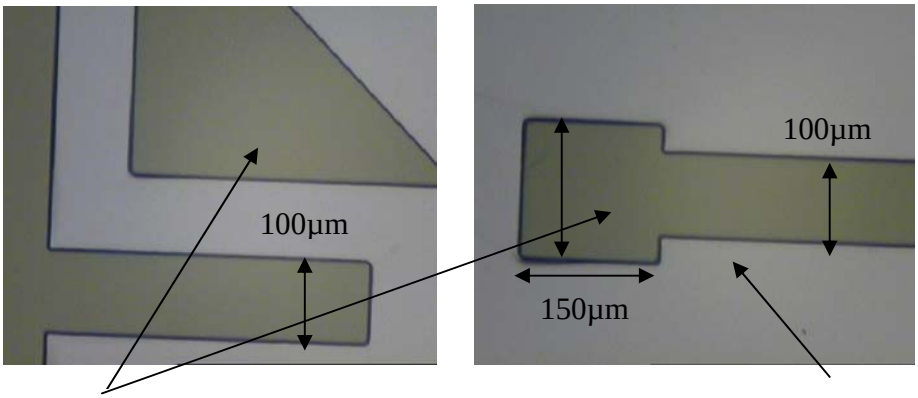


Figure 3.3 BCB patterning

3.2 Wafer Bonding Results

A Silicon and Pyrex glass wafer were bonded using photosensitive BCB with different curing percentage from 45% cured to up to fully cured BCB. Bonding experiments were also performed with uncured BCB which is 35% cross-linked. The curing was done in a nitrogen environment using the Blue-M oven. As stated above,

curing percentage for BCB is a function of dwell time and temperature (refer to Figure 3.2). For 55% curing of Cyclotene 4022-35, a dwell time of 10 minutes at 185 ºC was sufficient. Bonding was done at the Stanford Nanofabrication Facility by a colleague.

Wafers with patterned BCB layers are aligned and bonded using an EVG 501/620 bonder and aligner at 3340N pressure, 250 ºC, for 30 minutes. Good bonding results were observed without appreciable reflow. Figure 3.4 shows bonding results that are void-free, solvent-free and have no reflow in patterned channels using 55% or more cured BCB Si/Pyrex pairs. Through direct inspection through a high magnification optical microscope it was confirmed that the photolithographically defined interconnect wells have no size change after bonding.

All bonded wafers also passed the razor blade test [12]. A razor blade was inserted between the silicon and Pyrex wafer to break the bond. It was observed that either silicon or Pyrex wafer cracked and broke. BCB film residue remains only on one wafer indicating that the BCB to BCB bonding formed between the wafers is stronger than the bond between BCB to substrate. However, in the case of BCB cured less than 55% and uncured BCB, residual solvent remains trapped in between the wafers.

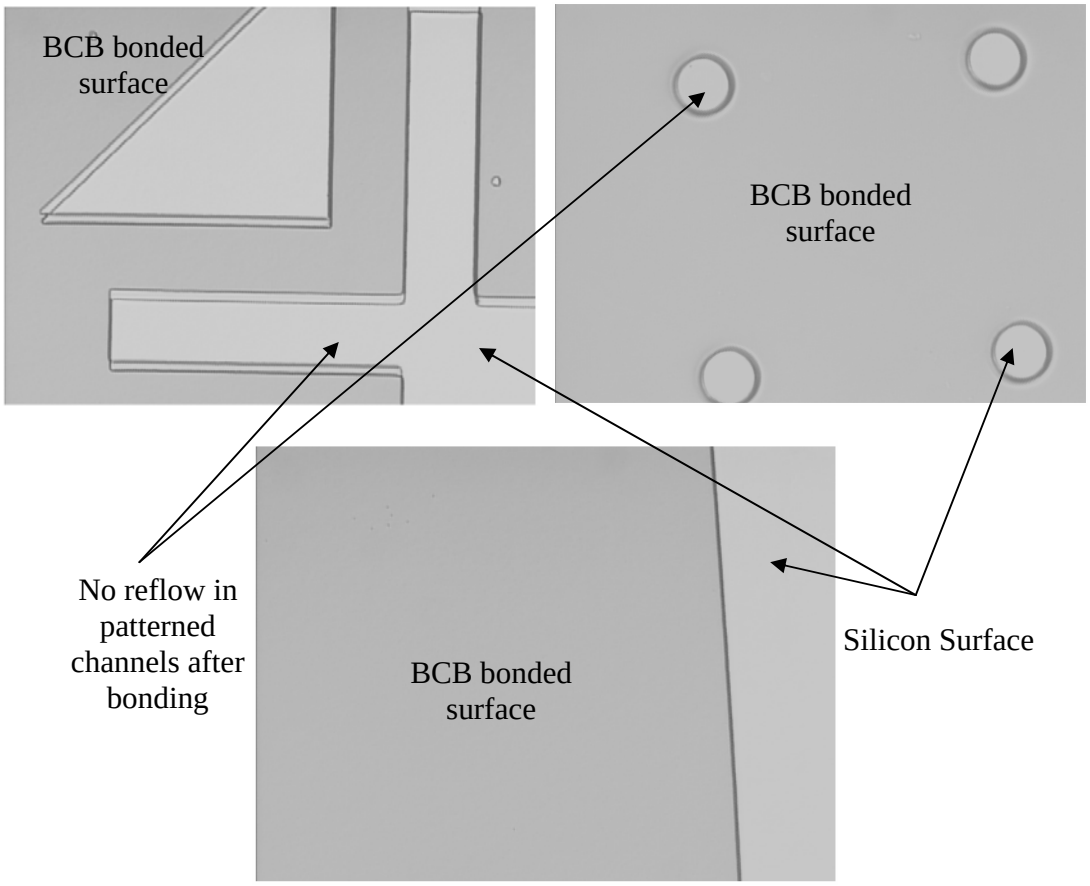


Figure 3.4 Bonded wafers with BCB at 55% cured

3.3 Design and Fabrication of 3D Electrical Interconnects

3.3.1 Photo Mask Design

The photo mask design for electrical interconnects was prepared for fabrication on a 4” Silicon or Pyrex glass wafer. The wafer was divided into four quadrants each of which had an array of 40 x 40 solder pads as electrical interconnects. The interconnect diameter sizes vary from 10µm - 80µm in steps of 10µm each. Each interconnect is enclosed by an outer circle of 130µm of BCB. In addition to solder pads, a square pattern of Cr/Au interconnect lines are formed between the 3D interconnects. The

interconnect lines run perpendicular to each other on the top and bottom wafers and are terminated on 40 metal pads on the bottom Silicon wafers, and 40 metal pads on the top Pyrex wafers. These pads are later exposed by dicing for electrical testing. Figure 3.5 shows the mask design schematic.

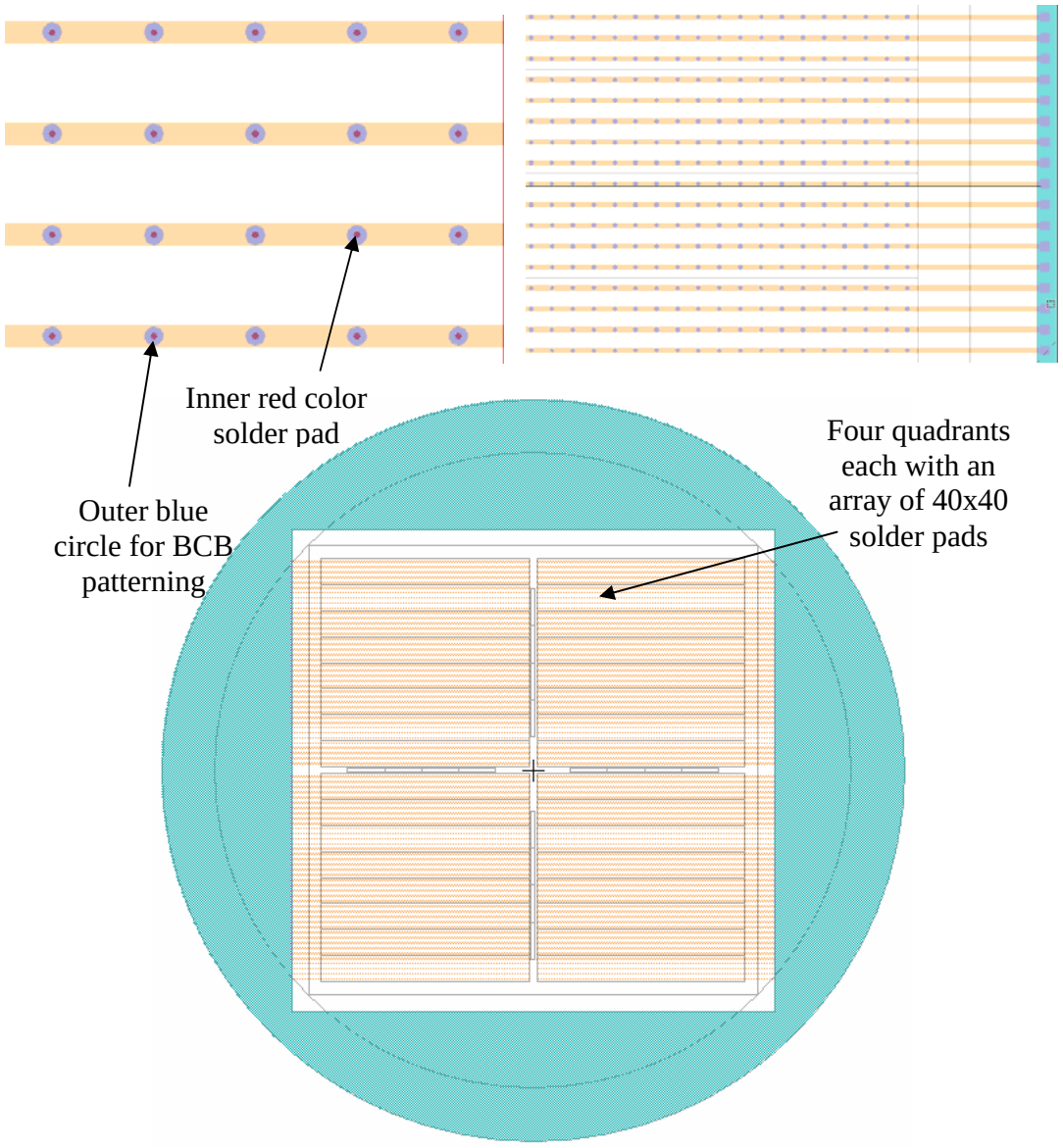


Figure 3.5 Mask design schematic

3.3.2 Fabrication Process

Solder composition of 95Sn/5Au is used to form electrical interconnections. Since the solder alloy is not commercially available, the desired composition is achieved by evaporating alternate layers of Sn and Au. The topmost layer is of gold, which acts as a cap layer and prevents the oxidation of the underlying Sn layers. The Au–Sn alloy is a rare material that exhibits interdiffusion to form an Au-Sn compound, even at room temperature. This is evident from the grayish color of the solder after deposition, even though the top layer is of gold. The sequentially deposited multiple layers get homogenized after reflow.

For the initial experiments, solder bump reflow and wafer bonding using BCB were tested as separate processes. The process flow for fabrication of electrical interconnection is shown below. RCA clean is performed to clean the wafers. The wafer is patterned with a 1.4µm thick layer of positive photo resist, Shipley S1813, for base metal deposition. It consists of sequentially deposited three layers of titanium, platinum and gold, each of which is 0.1µm thick. Base metal defines the area for solder reflow and also isolates the solder bump from the contact pad. After evaporation, lift-off is performed. The wafer is again patterned with a 2µm thick photo resist layer. The solder metal pattern is aligned on top of the already deposited base metal pad. This is followed by another thermal evaporation step for solder metal deposition.

Alternate layers Sn (0.6µm thick) and Au (0.02µm thick) are deposited to achieve a total thickness of 1.24µm. Gold is deposited as the top layer to prevent oxidation of the underlying layers of tin. Formation of oxides prevents the solder bump

from reflowing, since the oxide of tin melts at a very high temperature. After evaporation, lift-off is performed to remove the metal from unwanted areas. The process flow is described in Figure 3.6 below. The processing recipes for base and solder metal depositions are also described below.

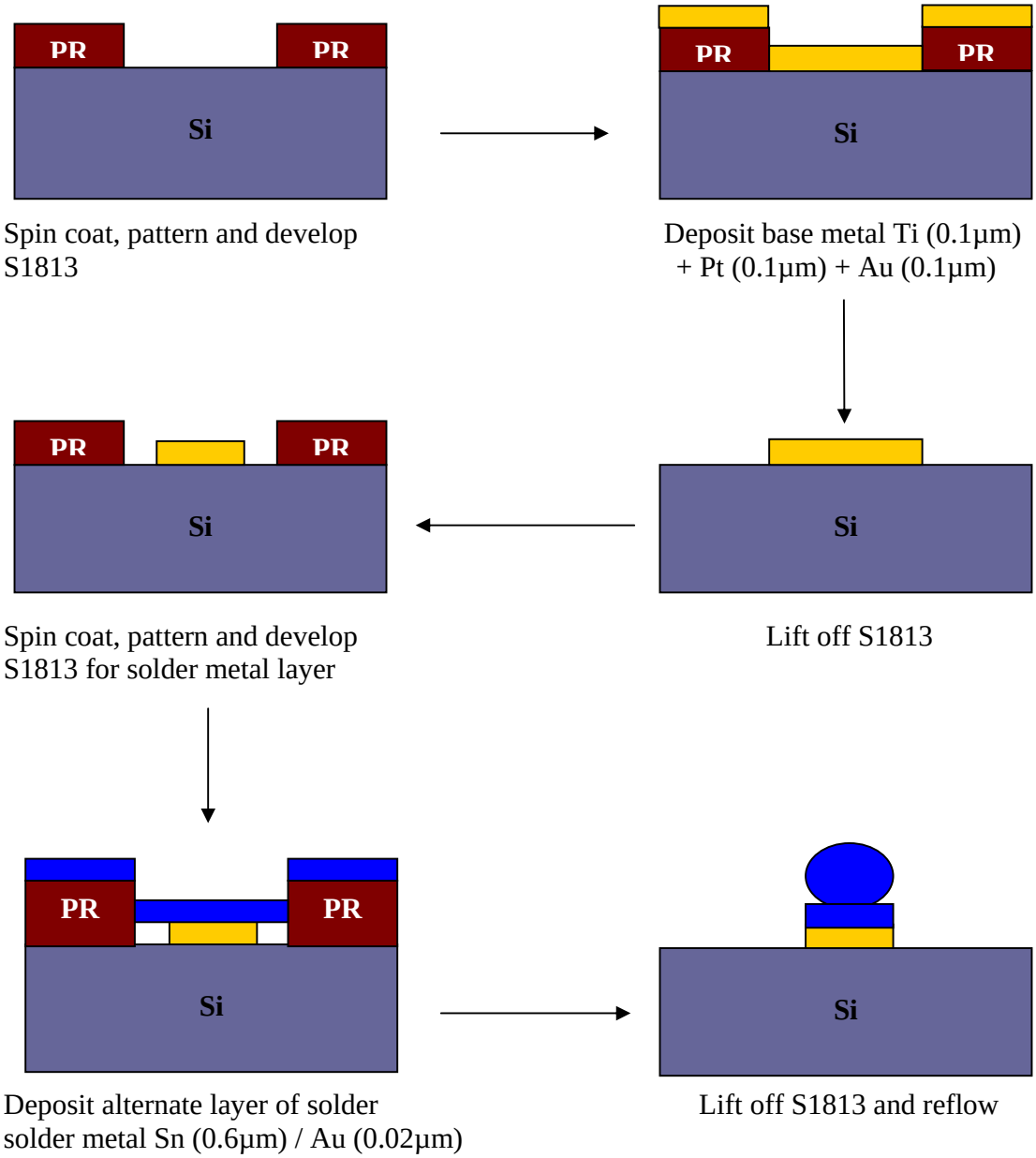


Figure 3.6 Process flow for electrical interconnection formation

Recipe for Base Metal Deposition:

1. RCA clean of the wafer
2. Spin coated HMDS @ 3000 rpm for 40 sec
3. Spin coated positive resist S1813 @ 2000 rpm for 30 sec (thickness 2µm)
4. Soft baked @ 90°C for 60 sec
5. Expose for 12.5 sec
6. Developed in MF319 for 35 sec
7. Hard baked @ 90°C for 90 sec
8. Deposited Ti (100nm) + Pt (100nm) + Au (100nm) through E-beam evaporation
9. Performed Lift off of S1813 in acetone

Recipe for Solder Metal Deposition:

10. Aligned and patterned S1813 for solder metal layer using the above mentioned processing recipe
11. Deposited two alternate layers of Sn (0.6µm) and Au (0.02µm) using E-beam evaporator
12. Performed Lift off of S1813 in acetone

After determining the success of solder reflow, the process was carried out simultaneous to BCB bonding. The process flow is depicted below in Figure 3.7. The processing recipes for metal deposition were same as described earlier in the chapter.

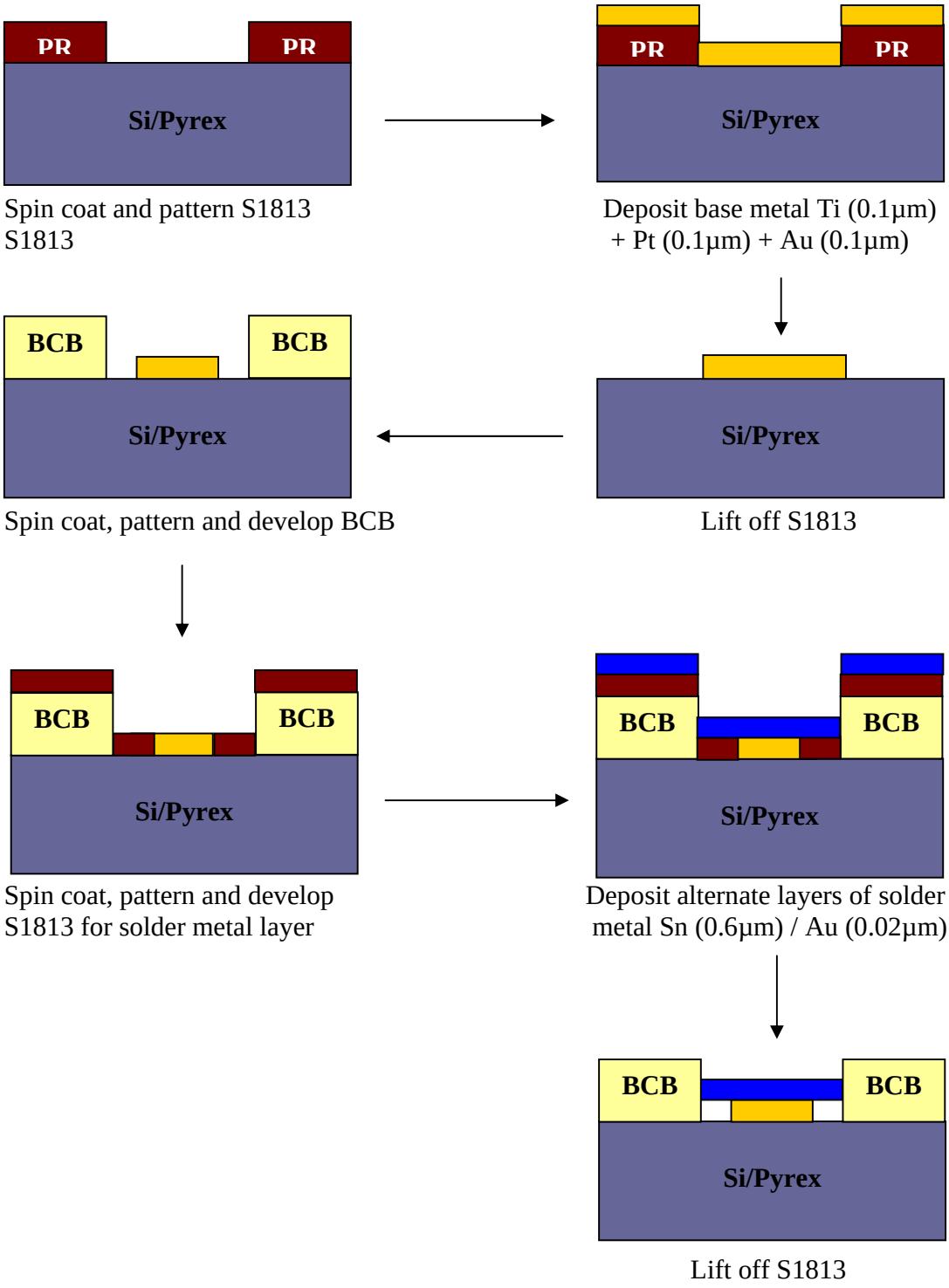


Figure 3.7 Process flow for BCB processing and electrical interconnection formation

Similarly, another wafer is patterned and two are bonded together using after solder metal deposition. The bonding temperature for BCB is 250°C. The solder metal is reflowed to form a bump and hence an electrical interconnection between the two bonded wafers. The schematic is shown in the figure 3.8:

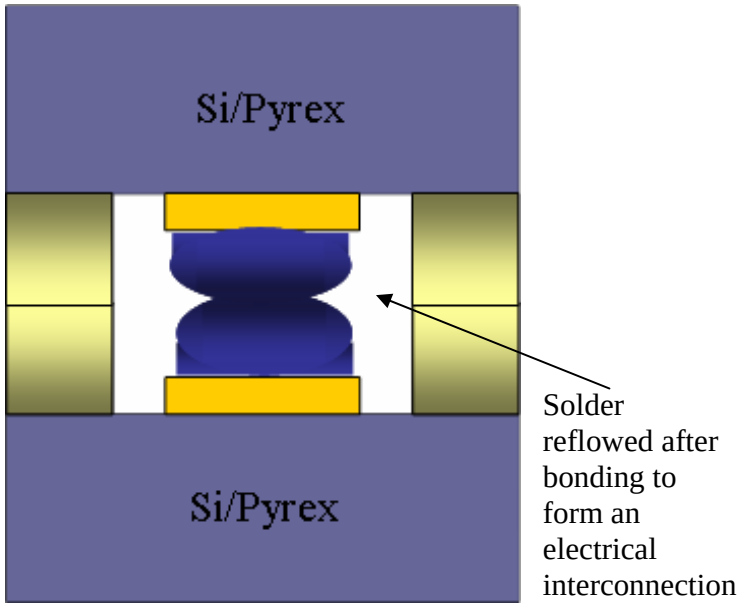


Figure 3.8 Schematic of the bonded wafers with the electric interconnect

3.4 Solder Reflow

The solder reflow profile for a Au-Sn alloy is shown in Figure 3.9 [33]. It is a bell shaped profile with equal heating and cooling rates of approx 1°C/sec. The reflow is temperature is around 30-40°C higher than the melting temperature of the alloy. And the total time above the melting temperature should not be more that 4-5 min. However, for this research the reflow experiments were performed either on a hotplate or in a

conventional oven that could not provide high heating and cooling rates of 1°C/sec. Also it was difficult to precisely control the temperature using a hotplate setup.

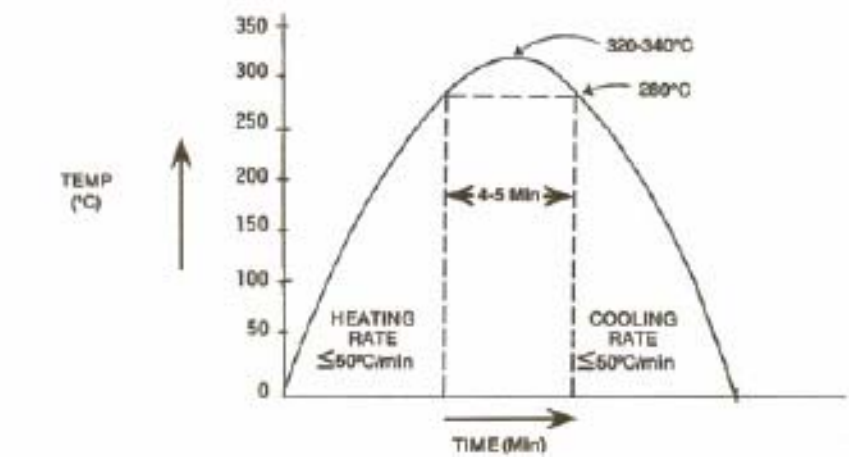


Figure 3.9 Standard reflow profile for a Au-Sn alloy [33]

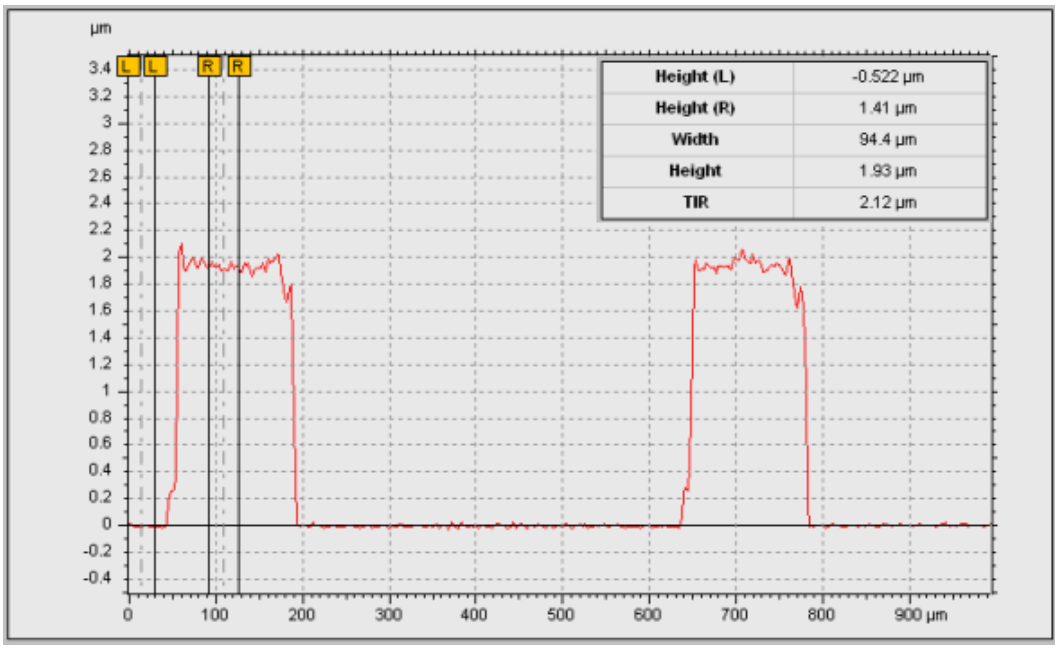
Solder reflow for wafer deposited with 95Sn/5Au solder composition was initially carried out on a hotplate. The wafer was diced into quarter inch pieces for reflow testing. Each quarter of the wafer has an array of 32 x 32 solder bumps. 10 such samples were reflowed on a hotplate in the natural ambience. The reflow conditions were:

1. Preheat the hotplate to 150°C
2. Place the wafer at the center of the hotplate
3. Let the temperature raise up to 250°C
4. Maintain the temperature for 1 min, following which the hotplate is turned off
5. Let the wafer cool down to about 150°C before removing it from the hotplate

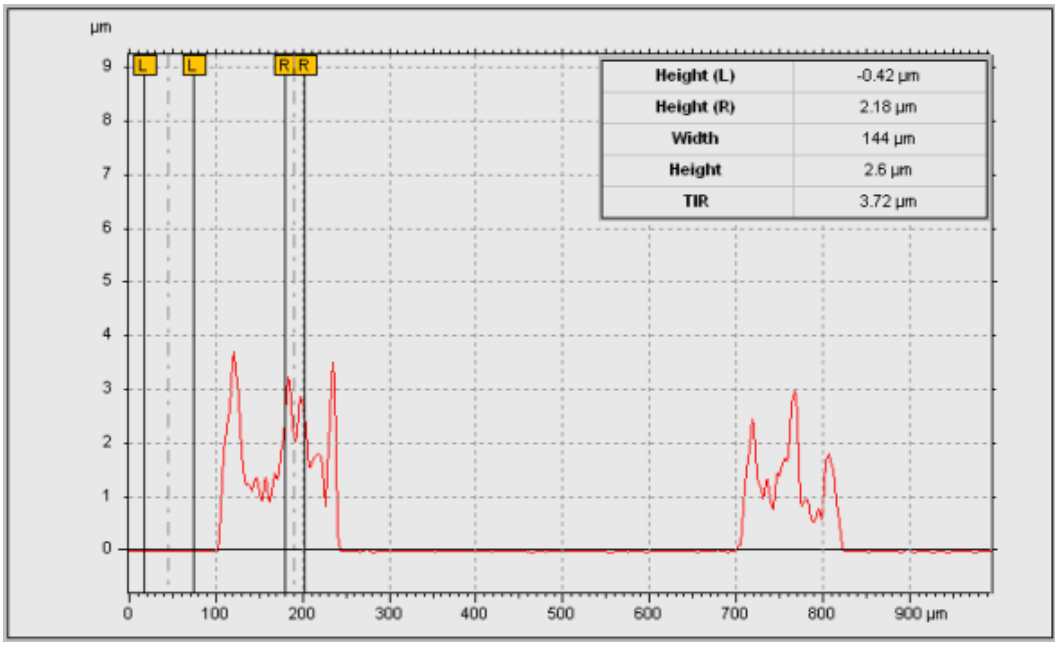
Observation: No reflow of the solder to form a bump shape was observed. However, melting of the solder metal was observed. Surface profiles were measured before and after reflow experiments, to measure solder height and diameter. Table 3.1 summarizes the solder height before and after reflow. The 2D surface profiles for the corresponding solder heights are also given below.

Table 3.1 Solder height before and after reflow

Before Reflow		After Reflow	
Width (µm)	Height (µm)	Width (µm)	Height (µm)
129	1.93	129	2.6
83.5	1.93	83.5	2.74
53.7	2.0	53.7	2.8

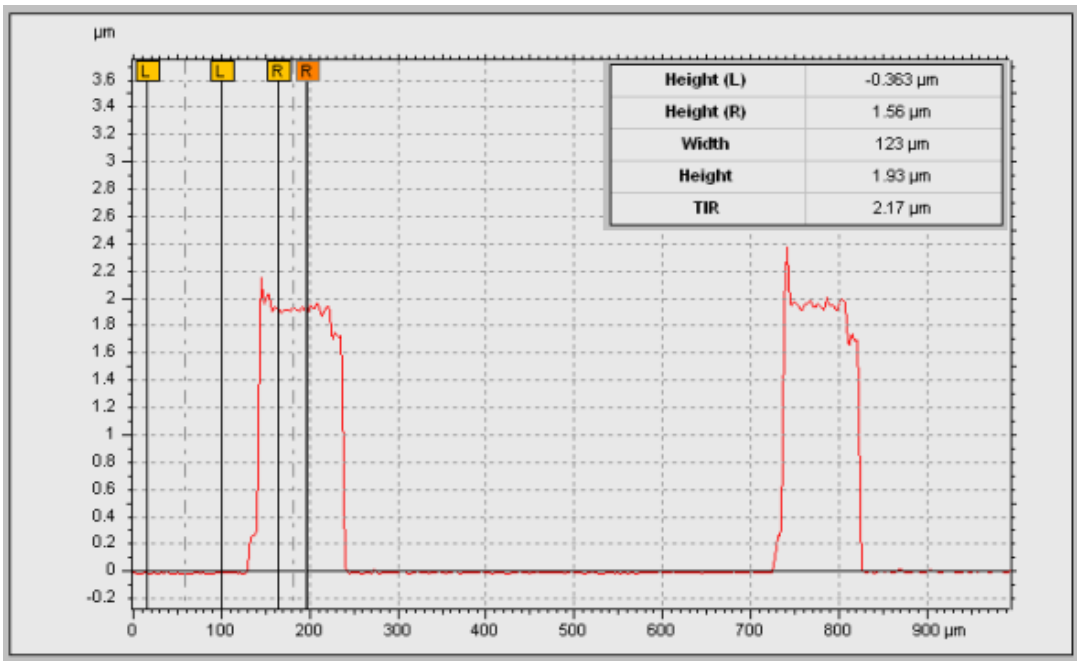


(a)

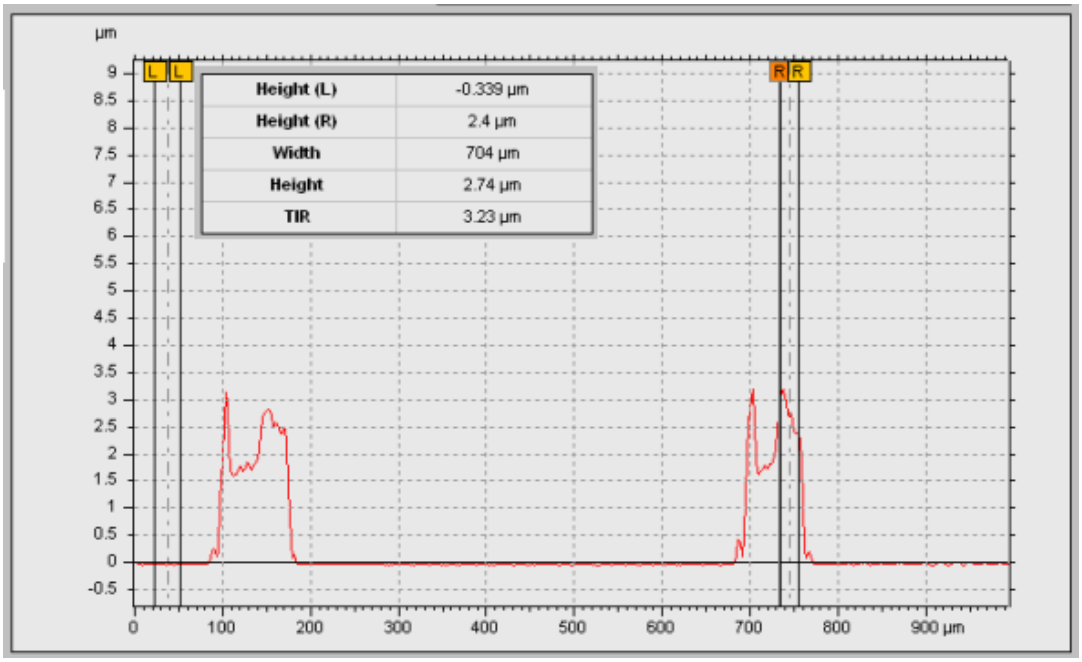


(b)

Solder height (a) before and (b) after reflow at base pad diameter of 129µm

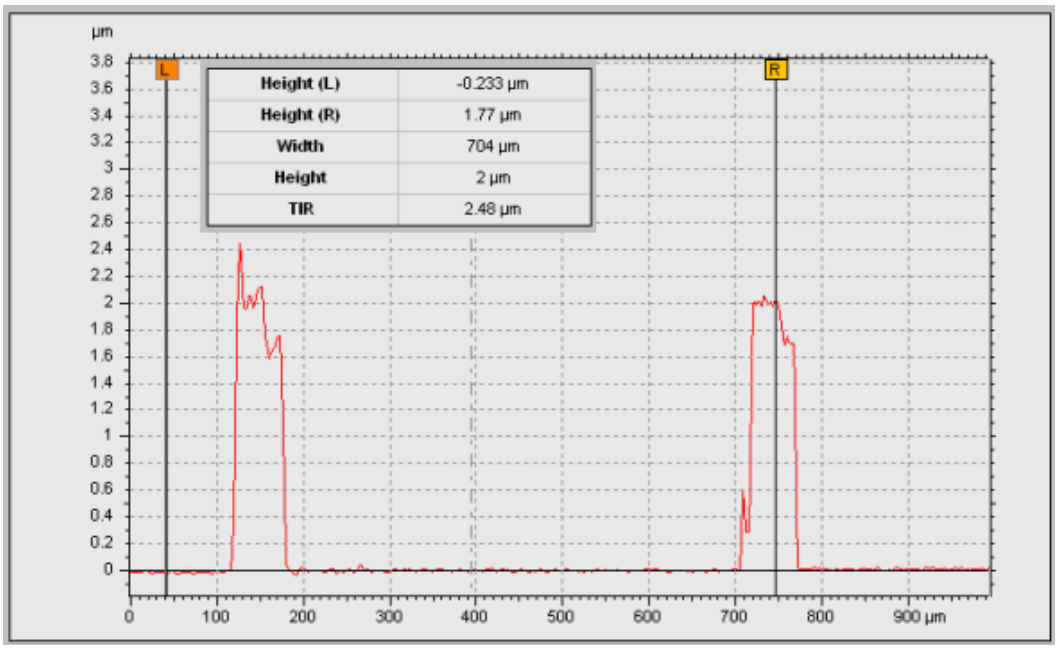


(a)

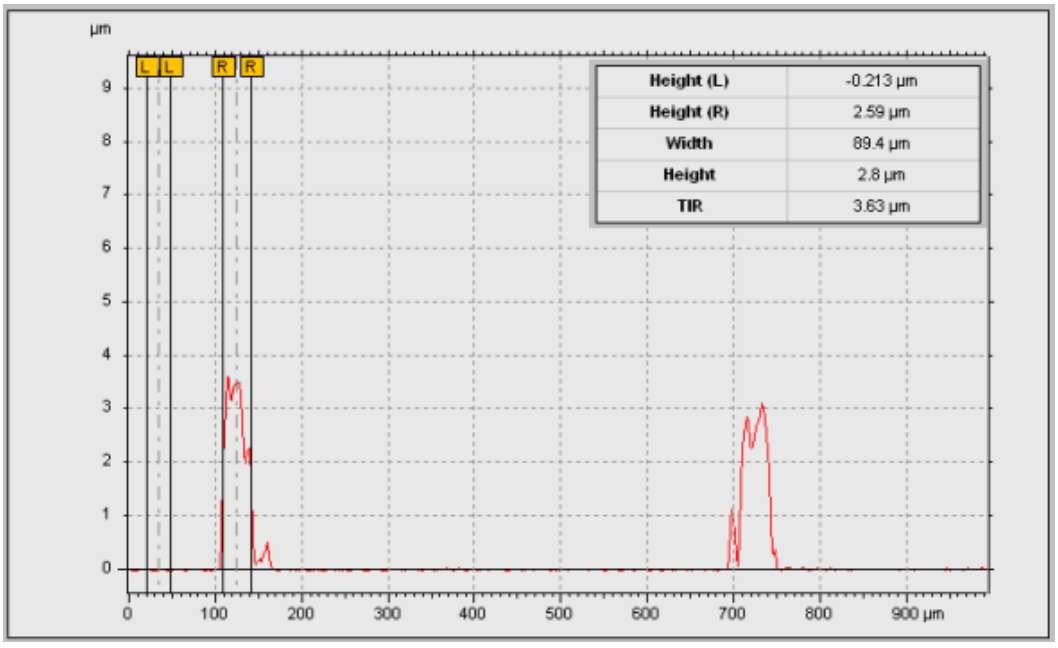


(b)

Solder height (a) before and (b) after reflow at base pad diameter of 83.5µm



(a)



(b)

Solder height (a) before and (b) after reflow at base pad diameter of 53.7µm

Conclusion: It was concluded that 95Sn/5Au solder composition is easily prone to oxidation due to the high concentration of Sn in it. The formation of oxide layer prevents the solder from forming a bump shape after reflow. Hence, for the next set of experiments an inert ambience was used during reflow. Also the wafers were cleaned using argon plasma to remove the oxide layer. Plasma cleaning was done for 30 min.

The reflow was carried out in an oven purged with nitrogen. The reflow profile used was:

1. Preheat the oven to 150°C in 5 min
2. Ramp up the temperature from 150°C to 200°C in 1 min
3. Ramp up the temperature from 200°C to 250°C in 1 min
4. Ramp down the temperature from 250°C to 200°C in 1 min
5. Ramp down the temperature from 200°C – 50°C in 30 min.

Equal heating and cooling rates are desired for solder reflow however, it was high cooling rates of approx 1°C/sec could not obtained by through the Blue M oven used for reflow.

Observation: Surface profiles were measured before and after reflow. Melting of the solder was observed however reflow of metal to form a bump shape could not be achieved.

Conclusion: Oxidation of the solder was suspected. To validate this assumption, a low residue flux was used for the next set of experiments to remove oxides from the solder and obtain reflow. The wafer was spin coated with a low residue CRX920 flux. Reflow was carried out in the oven and the reflow conditions used were:

1. Preheat the oven to 150°C in 5 min

2. Ramp up the temperature from 150°C to 200°C in 1 min. This is flux activation zone during which solvents are evaporated from it.

3. Ramp up the temperature from 200°C to 250°C in 1 min

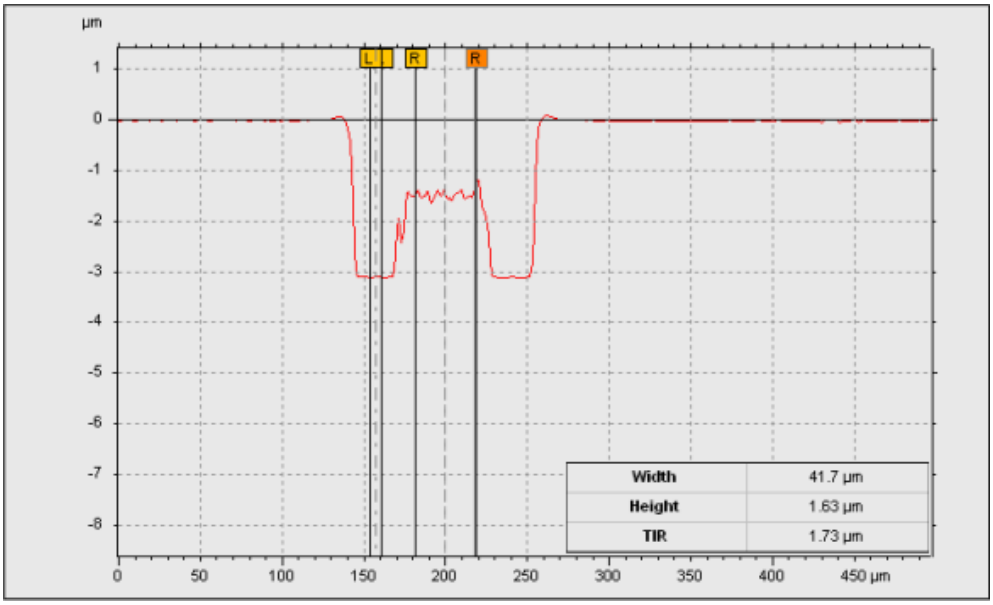
4. Ramp down the temperature from 250°C to 200°C in 1 min

5. Ramp down the temperature from 200°C – 50°C in 30 min.

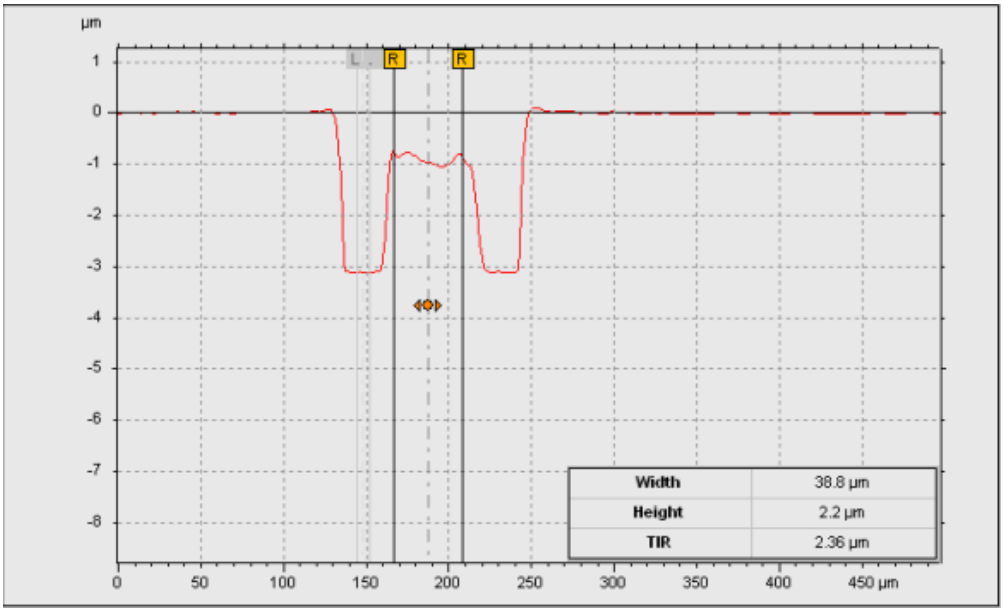
Observation: Reflow of solder was observed to form a bump shape. However, it was not uniform across the entire array of 32 x 32 solder pads. Surface profiles were measured before and after reflow and are shown in Figure 3.6. Table 3.2 summarizes the height before and after reflow.

Table 3.2 Solder height before and after reflow

Before Reflow		After Reflow	
Width (µm)	Height (µm)	Width (µm)	Height (µm)
71.6	1.63	62.654.7	2.2
60.6	1.63	54.7	2.33
49.7	1.63	41.7	2.45
38.8	1.64	35.8	2.8

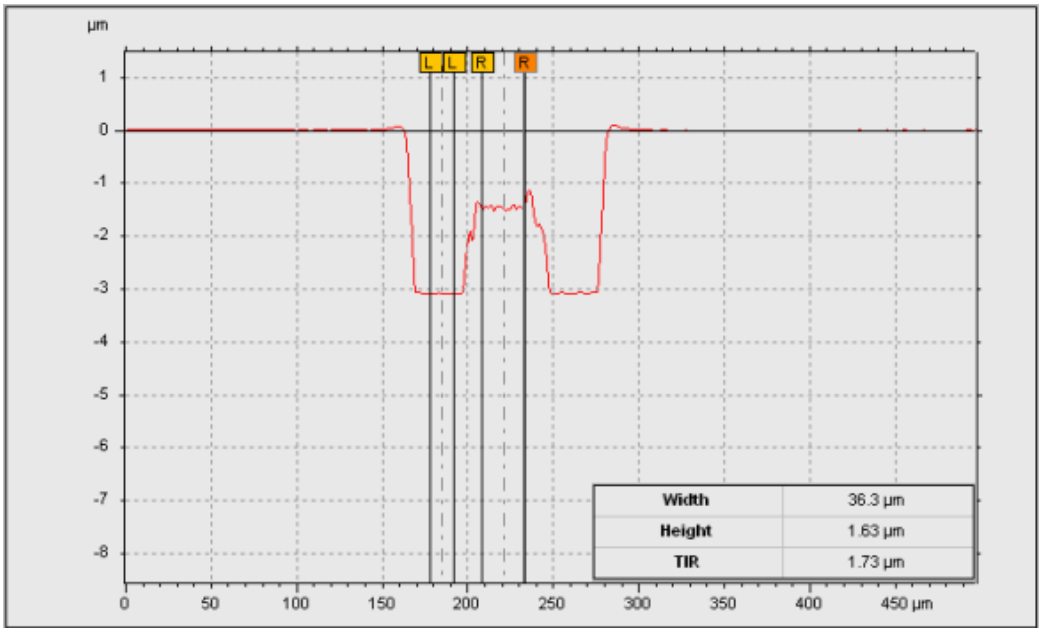


(a)

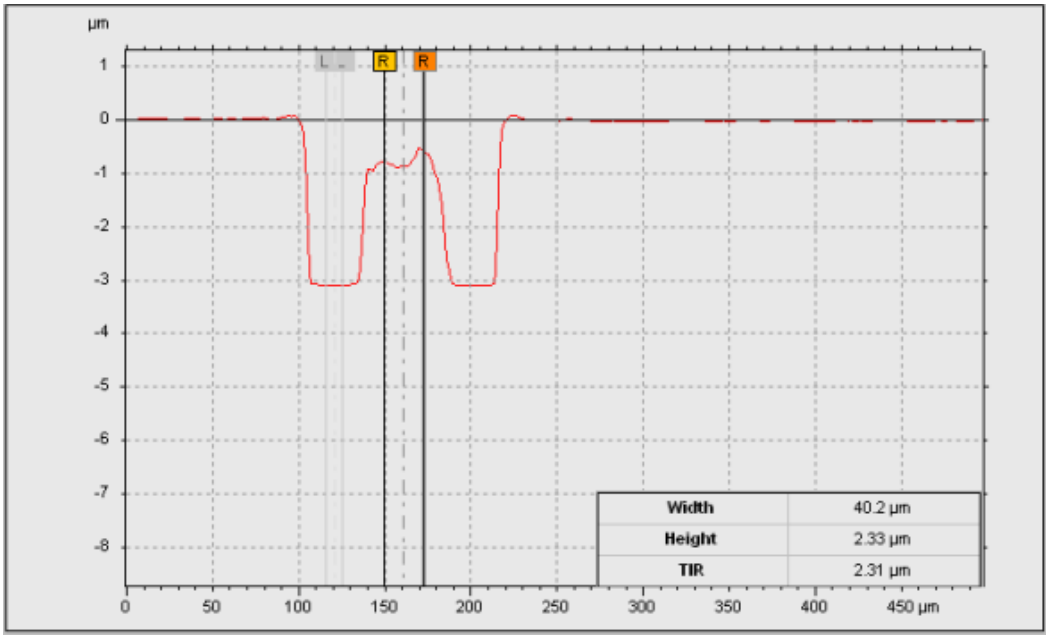


(b)

Solder height (a) before and (b) after reflow at base pad diameter of 71.6µm

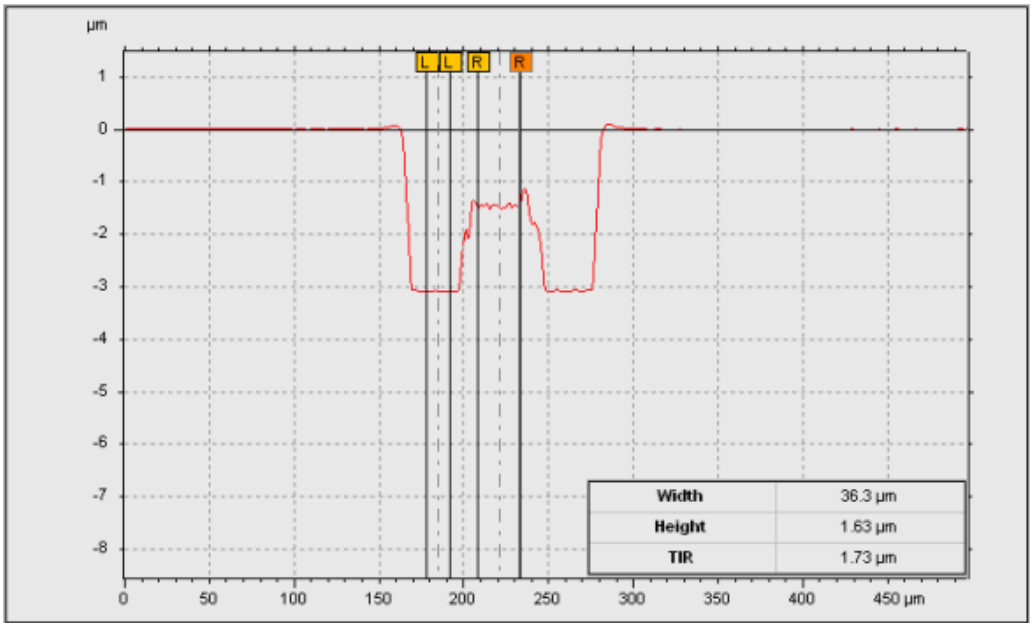


(a)

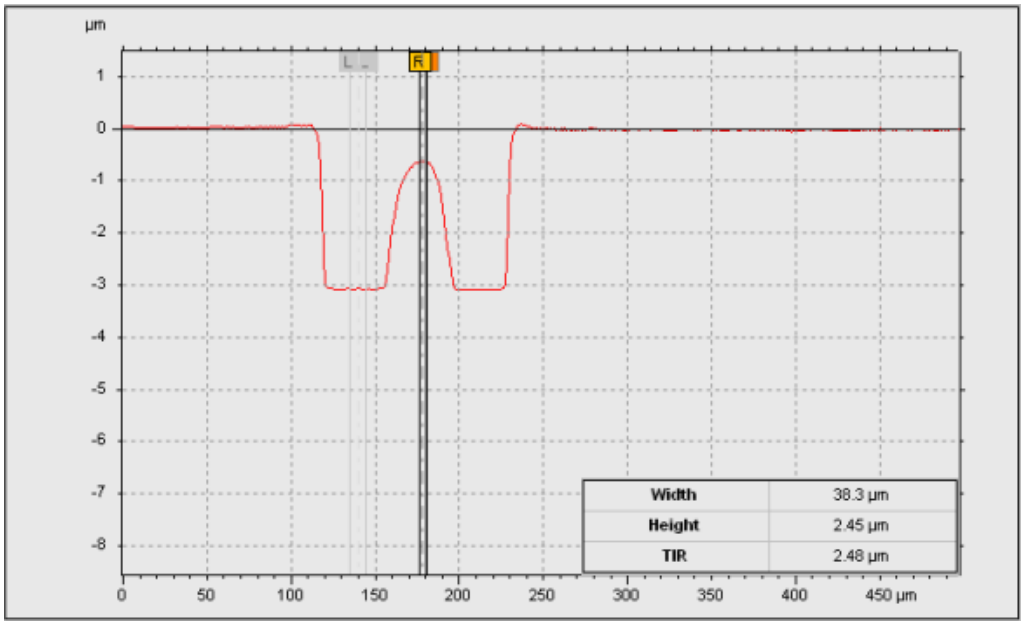


(b)

Solder height (a) before and (b) after reflow at base pad diameter of 60.6µm

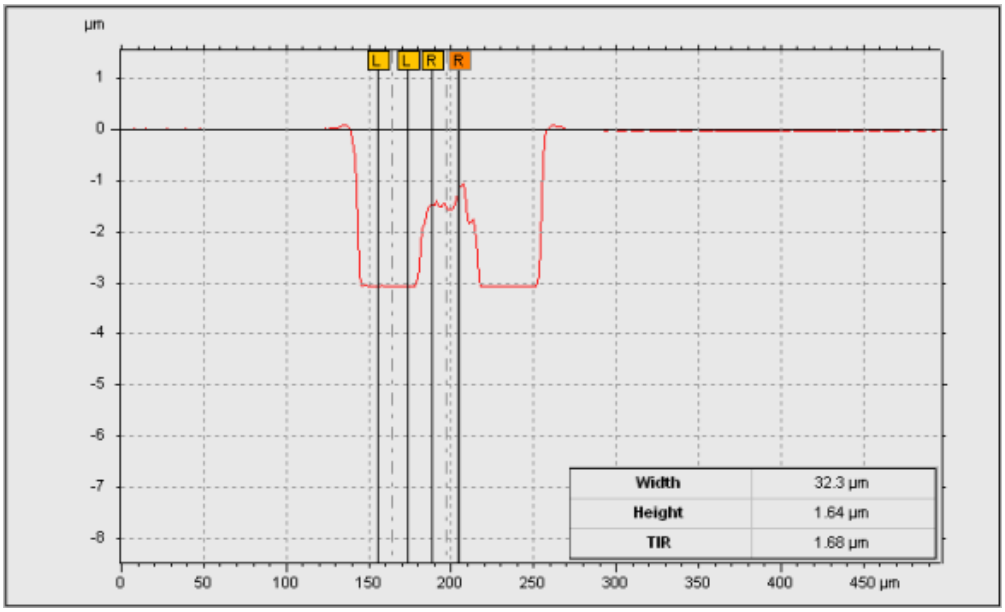


(a)

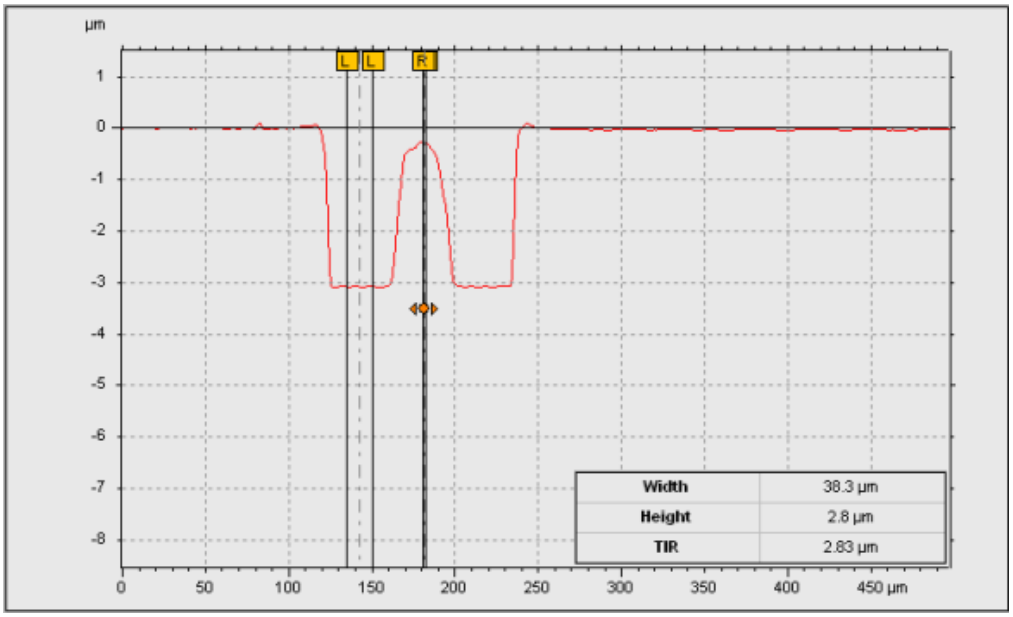


(b)

Solder height (a) before and (b) after reflow at base pad diameter of 49.7µm



(a)



(b)

Solder height (a) before and (b) after reflow at base pad diameter of 38.8µm

Conclusion: It was found that 95Sn/5Au being a Sn rich solder composition is difficult to reflow without the use of flux.

Since is a fluxless process is desired 80Au/20Sn solder composition is used to form electrical interconnects. Being a Au rich composition it is less prone to oxidation and hence easy to reflow. Electrical interconnections have been fabricated using this solder composition between wafers bonded with BCB. Figure 3.10 shows the picture of the 4" Si wafer bonded to another 4" Pyrex glass wafer.

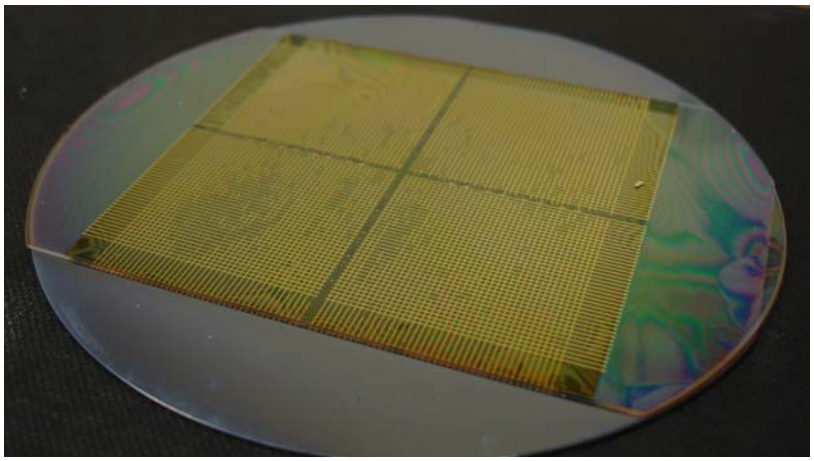


Figure 3.10 Wafer bonded with BCB and interconnected using 80Au/20Sn solder bumps

3.5 Conclusion

The processing recipe for photosensitive BCB was developed along with the recipes for metal deposition. Wafer bonding results show that BCB cured 55% and above shows no reflow during bonding. Also void-free, solvent-free bonds were formed between the Silicon and Pyrex wafers bonded with 55% or more cured BCB. Solder

reflow experiments were individually carried out on hotplate and in an oven purged with nitrogen. It was found that 95Sn/5Au being a Sn rich solder composition is difficult to reflow without the use of flux. Since is a fluxless process is desired, other solder compositions, for e.g. 80Au/20Sn, would be experimented as future work.

CHAPTER 4

DIE BONDING AND FORMATION OF ELECTRICAL INTERCONNECTS

This chapter discusses the design and fabrication of the hermetic package based on a fluxless soldering technique. Die bonding experiments performed using two solder compositions are discussed and the results of each are elaborated.

4.1 Design and Fabrication

The hermetic package consists of two Si dies with a perimeter sealing ring for hermeticity. The bottom silicon chip, also called the MEMS chip, carries the MEMS device. Whereas the top silicon chip, also called cap chip, has a 100µm deep DRIE trench accommodate for the motion of the MEMS device. A fluxless soldering technique was used to hermetic packaging. A 4.5µm thick layer of solder metal is deposited using sputtering on the cap chip dies. The MEMS chip contains base metal deposited through e-beam evaporation. The fabrication for MEMS chip and cap chip was carried out on two separate 4 inch Si wafers. The wafers were then diced into individual dies of 1cm x 1cm. Figure 4.1 shows the picture of the dies to be bonded.

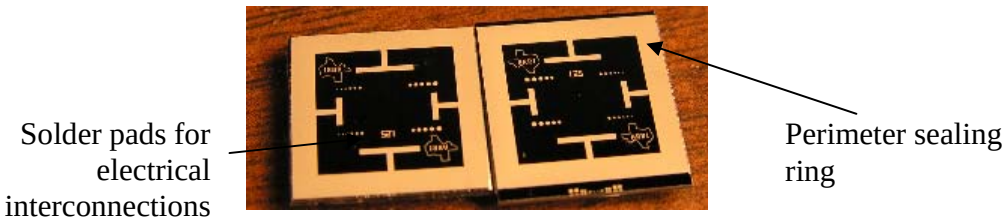


Figure 4.1 Die with perimeter sealing ring

4.1.1 Photo Mask Design

The hermetic package design was divided into two different sub modules given below. The photo masks were designed using L-Edit.

1. Die design for hermeticity testing
2. Die design for electrical interconnection testing

Die design for hermeticity testing: A sealing ring was designed around the perimeter of the die to provide hermeticity to the package. The width of the sealing ring is varied from 0.5mm – 2.0mm. Hermeticity of a package is determined through a helium leak test. A shear test is performed to test the bonding strength using the fluxless soldering technique. Square pads are deposited within the region of the perimeter ring to form vertical interconnects between the top and bottom dies. The side of the square pad is varied from 10µm – 90µm in length. Solder metal is deposited along perimeter on the cap chip only, which also has a DRIE trench. Overall dimension of the top and bottom die is 1cm x 1cm. The schematic of the die is shown in figure 4.2.

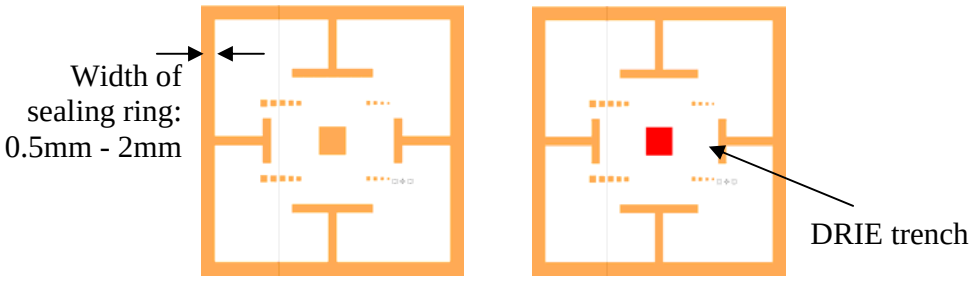
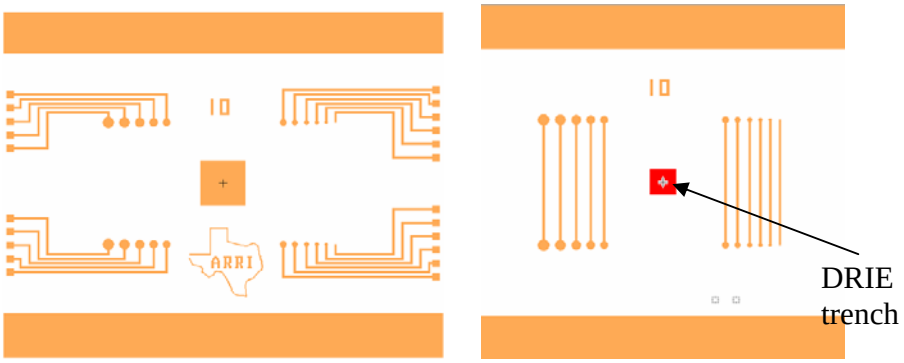


Figure 4.2 Hermetic sealing ring (a) Bottom Chip and (b) Cap Chip

Dies for electrical interconnection testing: Circular solder pads are deposited to form vertical interconnections between the top and bottom chip. Diameters

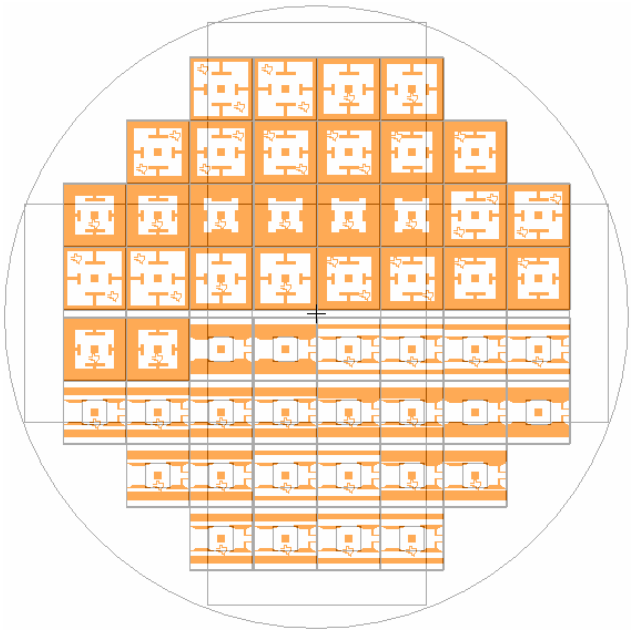
of the circular pads range from 10µm – 90µm. The bottom die connects the electrical interconnection pads to contact pads for electrical continuity testing and resistance measurement across interconnects. The dimension of the bottom die is 1cm x 1cm. Solder metal is deposited on cap chip only, the dimension of which is 0.8cm x 0.8cm. The top die also has a DRIE trench to house the MEMS device. The schematic of the bottom die and top die is shown in figure 4.3.



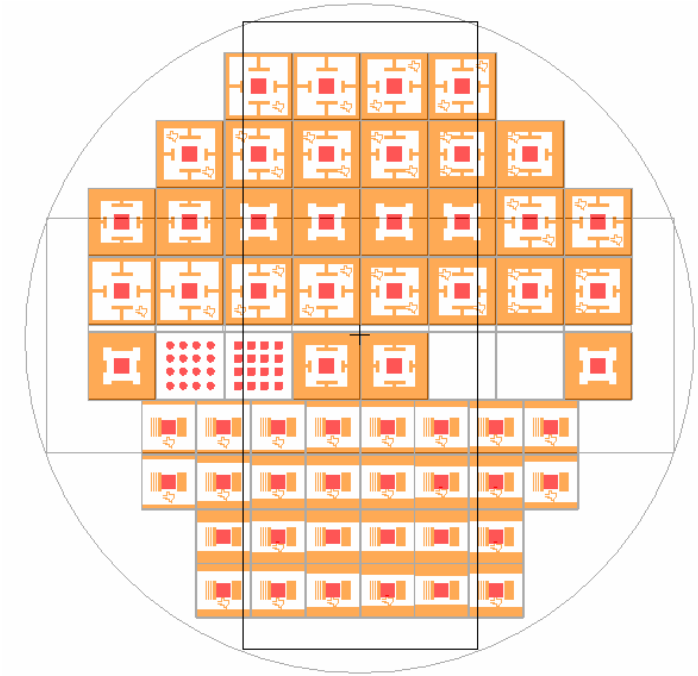
(a) (b)

Figure 4.3 Electrical interconnection testing (a) Bottom Chip and (b) Cap Chip

The fabrication of dies was carried out on two separate 4 inch Si wafers, where each wafer contained dies for both hermetic testing and electrical interconnection testing. A matrix of dicing lines (150µm wide) was drawn across the wafer for ease during dicing. The photo mask layout for a 4 inch wafer is shown below in figure 4.4.



(a)



(b)

Figure 4.4 Wafer containing (a) Bottom chip dies and (b) Cap chip dies

4.1.2 Fabrication Process

The two different solder compositions were used: 95% wt. Sn and 5% wt. Au and 80% wt. Au and 20% wt. Sn. Base metal consisted of three separate layers of Ti, Pt and Au. The total thickness of the solder metal deposited is 4.5µm whereas that of the base metal is 0.5µm. Vacuum deposition techniques were used to deposit the solder and base metal to avoid oxidation of 95Sn/5Au, which being a Sn-rich solder composition is extremely prone to oxidation. Formation of oxides prevents the solder from reflowing and hence forming a bond.

The wafers are cleaned using the RCA cleaning process before processing. It is then patterned with photo resist for base metal deposition. It consists of three sequentially deposited layers of Ti (0.1µm), Pt (0.2µm) and Au (0.2µm). A lift off is performed by soaking the wafer in Acetone to remove the metal from unwanted areas. Following this the wafer is patterned with photo resist for solder meal deposition. Alternate layers Sn and Au are sputtered to achieve a total solder thickness of 4.5µm. Gold is deposited as the top layer to prevent oxidation of the underlying layers of tin. After solder metal deposition, lift-off in acetone is performed to remove the metal from unwanted areas. Both Si and Pyrex glass wafer was used to deposit the solder metal.

Post fabrication, wafer is diced into individual dies of 1cm x 1cm and 0.8cm x 0.8cm. Wafer is covered photo resist to prevent it’s contamination during dicing from city water. After dicing the resist is removed by soaking dies in acetone.

4.2 Die Bonding

4.2.1 Die Bonding Using 95Sn/5Au Solder Alloy

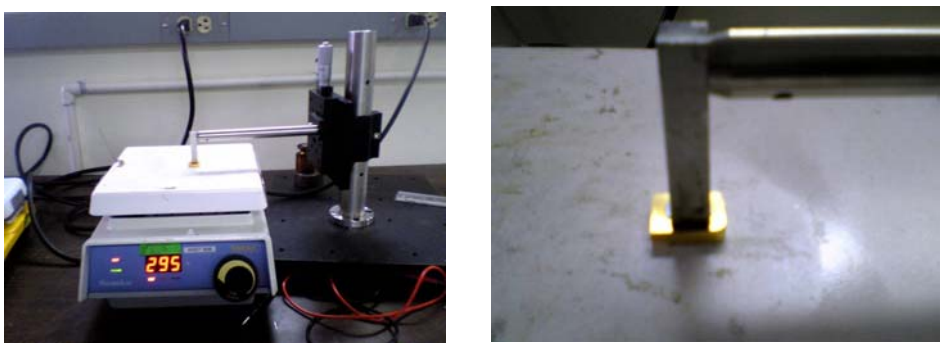
One of the commonly used solder's in electronic industry is the Sn-Au alloy, with main focus on 80Au/20Sn. However, the Sn rich solder composition of the Sn-Au alloy has been seldom used. In this research, experiments have been performed with 95Sn/5Au to explore its use as fluxless solder layer for die bonding. Secondly, it reduces cost by reducing the consumption of gold. However, being a Sn rich solder it oxidizes easily and it is much harder to achieve fluxless bonding using 95Sn/5Au. To prevent oxidation of Sn, the bonding is carried out in a nitrogen purged environment.

Preliminary die bonding experiments were performed on a hotplate with dies designed for hermeticity testing. Die bonding was carried out on a hotplate capable of attaining a maximum temperature of 500°C. The bonding temperature of the using 95Sn/5Au is in the temperature range of 220°C – 230°C. The weight is applied using a z-translation stage, the end effector of which is the size of a dies being bonded. Figure 4.5 shows the hotplate setup. This whole set up was placed inside a glove box, which is purged with nitrogen. An oxygen sensor is used to measure the percentage of oxygen inside the glove box. Oxygen level of 0.1% was desired and it takes around 3-4 hours to purge the glove box to the required level. Prior to bonding the dies were cleaned using Ar plasma to remove the oxides and other contaminants from the surface.

A bonding process using solder as an intermediate layer is sensitive to the following parameters:

1. Composition of solder

2. Surface cleaning
3. Bonding temperature
4. Ramp up and ramp down rates
5. Dwell time at peak temperature
6. Bonding Pressure
7. Ambience



(a) (b)

Figure 4.5 (a) Hotplate setup and (b) Pressure applied using z-translational stage

The initial experiments were carried out to check on the feasibility of using 95Sn/5Au composition as a soldering medium. The same experimental conditions were used more than once to check for repeatability. Also, at anytime only one of the bonding parameters was changed while the others were kept constant. The experimental conditions, results and observations are described below:

Experiment: Bond die pairs with solder ring width of 1.25mm, 1.5mm, 1.75mm. Solder metal was deposited as perimeter sealing ring on both the top and the bottom die.

Experiment Conditions:

- Cleaning: Plasma cleaned dies for 30 min to remove oxides

- Soldering gas environment *(Industrial Grade Nitrogen):* Inert environment was used to minimize oxidation of solder. Bonding was carried out in glove box.
- Oxygen level inside glove box: 0.1-0.2% as measured through an oxygen sensor.
- Dies were heated on a hotplate heated to 225°C.
- Dwell time at or above 225°C (since the hotplate temperature could not be maintained at a constant value) was 5min
- Pressure was applied through a z translation stage.

Result: No bond formed between the dies. The experiment was repeated twice to check if the result was the same.

Experiment: Bond die pairs with solder ring width of 1.0mm, 1.75mm. Low residue flux (920CXF) was used for bonding.

Experiment Conditions:

- Cleaning: Plasma cleaned dies for 30 min to remove oxides
- Experiment was carried out in air. Inert environment was not necessary since flux was already being used.
- Dies were heated on a hotplate heated to 225°C.
- Dwell time at or above 225°C (since the hotplate temperature could not be maintained at a constant value) was 5min.
- Bonding pressure applied using the end effecter of a translational z-stage

Result: A bond was formed between the dies. However, the dies came apart while trying to mount them.

Observation: No metallurgical bond was formed between the dies. This observation is based on visual inspection, as no imprint of solder on top die was found on the bottom die and vice versa. Flux was holding the dies together.

Conclusion: Based on the above experiments it was concluded that oxidation of the dies is one factor preventing them from bonding. Hence, it was decided to clean the dies in 10% HCl solution for 10 min.

Experiment: Bond die pairs with solder ring width of 0.75mm, 1.0mm. No flux was used.

Experiment Conditions:

- Dies were cleaned in 10% HCl solution for 10 min. This was followed by a rinse with IPA.
- Plasma cleaned dies for 30 min to remove oxides.
- Soldering gas environment *(Industrial Grade Nitrogen):* Bonding was carried out in a glove box.
- Oxygen level inside glove box: 0.1-0.2% as measured through an oxygen sensor.
- Dies were heated on a hotplate to a temperature of 225°C.
- Dwell time at or above 225°C (since the hotplate temperature could not be maintained at a constant value) was 5 min

- Bonding pressure applied using the end effecter of a translational z-stage

Result: No bond formed between the dies. The bonding temperature was raised to 240C for the next experiment.

Experiment: Bond die pairs with solder ring width of 1.25mm, 1.5mm. No flux was used.

Experiment Conditions:

- Dies were cleaned in 10% HCl solution for 10 min. This was followed by a rinse with IPA.
- Plasma cleaned dies for 30 min to remove oxides.
- Soldering gas environment *(Industrial Grade Nitrogen):* Bonding was carried out in a glove box.
- Oxygen level inside glove box: 0.1-0.2% as measured through an oxygen sensor.
- Dies were heated on a hotplate to a temperature of 240°C.
- Dwell time at or above 240°C (since the hotplate temperature could not be maintained at a constant value) was 5 min
- Bonding pressure applied using the end effecter of a translational z-stage

Result: The dies were held together. However, they disengaged after being dropped. This was due to mishandling of the dies using tweezers.

Observation: A metallurgical bond was not formed between the dies. However the top die left its solder trace over the bottom die. This implies that there has been

some solder reflow. Figure 4.6 below shows the solder imprint on the bottom die after the two dies were disengaged.

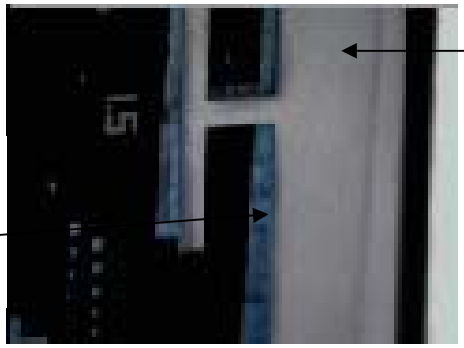


Figure 4.6 Solder trace left from the top die

Conclusion: It was concluded that the bonding process is quite sensitive to the peak bonding temperature. The next experiment was done to test if the solder reflows or not upon heating. Until the solder melts a bond cannot be formed between the two dies.

Experiment: To test solder reflow using laser.

Experiment Conditions:

- Used the die from previous experiment with a solder ring width of 1.5 mm.
- Laser beam was shone over one corner of the hermetic sealing
- Laser power was 17W
- Exposure time was 1 min.

Result: Solder reflow was observed.

Observation: The solder was seen to reflow upon heating with a laser beam. However, it did not spread outside the area defined by the hermetic ring after melting. This can be due to insufficient volume of the solder deposited.

Conclusion: The following two modifications are proposed for the process based on the results of the above experiments:

- Use a bonding temperature of 240°C
- Deposit the Sn/Au solder on the cap chip only. Use a layer of gold as bond pad instead of bonding two dies with solder.

For the next set of experiments, the Sn/Au deposited die was bonded to a gold coated surface. Some advantages of using a gold coated layer for bonding are:

- Gold has minimal surface oxide, hence it can allow use of fluxless soldering technique, which is a requirement for hermetic sealing
- Good wettability and solderability
- Good protection from environmental moisture

The preliminary experiments were carried out with the use of flux. Based on the results the bonding would be performed in a nitrogen environment using the glove box.

Experiment: Bond the Sn/Au solder deposited die to a silicon die with Cr and Au coating. Low residue flux (920CXF) was used.

Experiment Conditions:

- Dies were cleaned in 10% HCl solution for 10 min followed by a rinse with IPA.

- Plasma cleaned dies for 30 min to remove oxides.
- A 1 cm x 1cm silicon die with 0.02µm of Cr and 0.2µm of Au deposition was used.
- Experiment was carried out in air
- Dies were heated on a hotplate to a temperature of 240°C.
- Dwell time at or above 240°C was 5 min
- Bonding pressure applied using the end effecter of a translational z-stage

Result: The two dies were bonded together. Appreciable amount of force was applied using tweezers to de-bond the die from the substrate.

Observation: Solder traces were left on the gold coated after de-bonding. Figure 4.7 shows the solder traces left on the die after de-bonding.

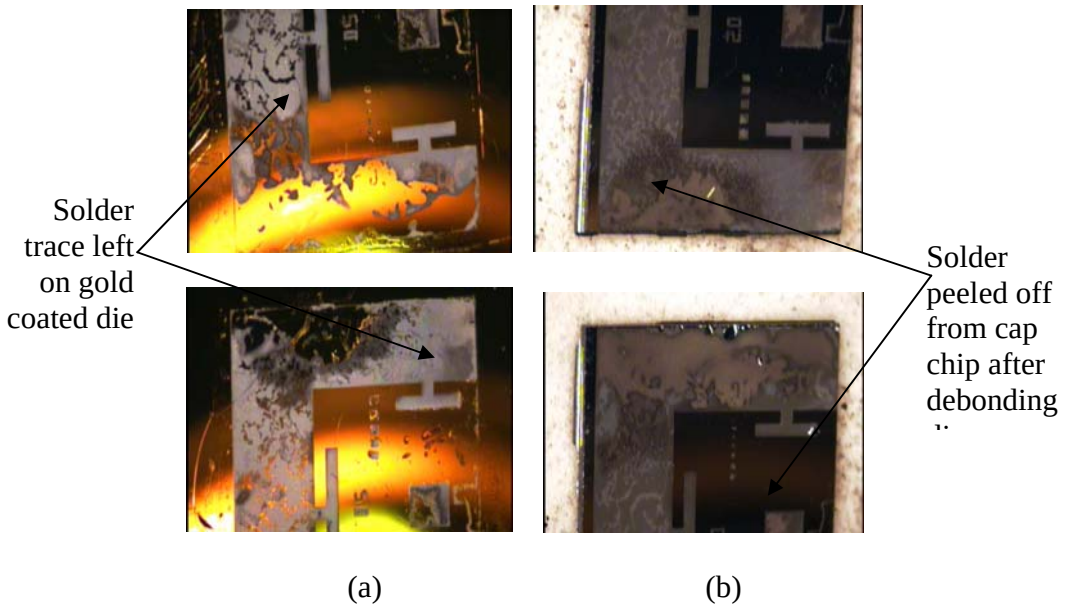


Figure 4.7 (a) Solder left on substrate die and (b) Solder coated die after de-bonding

Experiment: Bond die pairs with solder ring width of 1.5mm, 1.75mm. No flux was used.

Experiment Conditions:

- Dies were cleaned in 10% HCl solution for 10 min followed by a rinse with IPA.
- Plasma cleaned dies for 30 min to remove oxides.
- Soldering gas environment *(Ultra Pure Nitrogen):* Bonding was carried out in a glove box.
- Oxygen level inside glove box: 0.1-0.2% as measured through an oxygen sensor.
- Dies were heated on a hotplate to a temperature of 240°C.
- Dwell time at or above 240°C was 5 min
- Bonding pressure applied using the end effecter of a translational z-stage

Result: No bond formed. Although could see the imprint of solder left on the gold coated chip. The dwell time was increased to 10 minutes for the next experiment.

Experiment: Bond die pairs with solder ring width of 0.5mm, 0.75mm, 1.5mm. No flux was used.

Experiment Conditions:

- Dies were cleaned in 10% HCl solution for 10 min. This was followed by a rinse with IPA.
- Plasma cleaned dies for 30 min to remove oxides.

- Soldering gas environment *(Industrial Grade Nitrogen):* Bonding was carried out in a glove box.
- Oxygen level inside glove box: 0.1-0.2% as measured through an oxygen sensor.
- Dies were heated on a hotplate to a temperature of 240°C.
- Dwell time at or above 240°C was 10 min
- Bonding pressure applied using the end effecter of a translational z-stage

Result: Bond formed between die with a solder ring width of 1.5mm. Others were unsuccessful. The same conditions were repeated with more die pairs.

Experiment: Bond die pairs with solder ring width of 0.75mm, 1.0mm, 1.25mm, 2.0mm. No flux was used.

Experiment Conditions:

- Dies were cleaned in 10% HCl solution for 10 min. This was followed by a rinse with IPA.
- Plasma cleaned dies for 30 min to remove oxides.
- Soldering gas environment *(Industrial Grade Nitrogen):* Bonding was carried out in a glove box.
- Oxygen level inside glove box: 0.1-0.2% as measured through an oxygen sensor.
- Dies were heated on a hotplate to a temperature of 240°C.
- Dwell time at or above 240°C was 10 min

- Bonding pressure applied using the end effecter of a translational z-stage

Result: Able to attach one die with ring width of 1 mm. Others were unsuccessful

Based on the experiments performed above, the following observations were made about the process:

- Need to precisely control the temperature on both the top and bottom die surface, since the process is very sensitive to this bonding parameter. This could not be done using the hotplate where a heat is lost due to conduction and the top die surface is at a different temperature compared to bottom.
- The bonding pressure needs to be precisely controlled, which could not be done using the bonding setup described above. A load cell was required to measure the bonding force applied by the z-translation stage.
- The surface of the hotplate and that of the end effector should be perfectly flat, so that uniform pressure is applied at all points on the die surface, which is important for hermeticity. Non uniform pressure leads to voids in the bonded surface.
- Ramp up and ramp down rates of 1°C/sec are required (based on the reflow profile for Sn-Au solder). This could not be controlled using the hotplate set-up. Slow cooling rate results in more intermetallic formation. This lowers the reliability of the solder joint as intermetallics are inherently brittle in nature.
- Oxidation of the solder prevents it from melting and forming a bond which can otherwise be done with the use of flux.

The need for a sophisticated bonding setup was realized to attain a better control over the process parameters and to analyze the bonding results. A Flip Chip Bonder (shown if figure 4.8) was purchased for the above purpose. Another modification to the process was to use 80Au/20Sn solder composition. Being a Au rich solder it is less prone to oxidation and it's comparatively easy to achieve fluxless soldering using 80Au/20Sn.

Figure 4.8 Laurier M-9 Flip Chip Aligner Bonder

4.2.2 M-9 Flip Chip Aligner Bonder

System Overview: Laurier M-9 Flip Chip Aligner Bonder used PC based optics for repeatable alignment and bonding of a flipped die to a substrate. This is accomplished by using a single camera optical probe, shown in figure 4.9, with a prism

assembly that can provide superimposed images of the dies on the top and bottom chucks. The probe is capable of moving in x, y and z axes for focusing on die surfaces. A high resolution, color CCD camera within the probe utilizes a high power 10x magnifying borescope to view and align fiducial marks as small as several tens of microns [34].

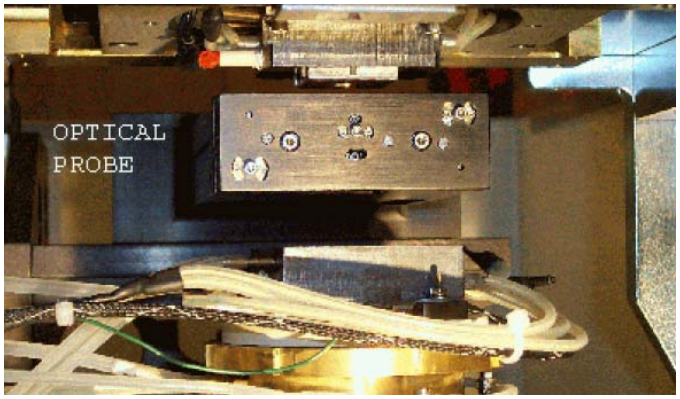
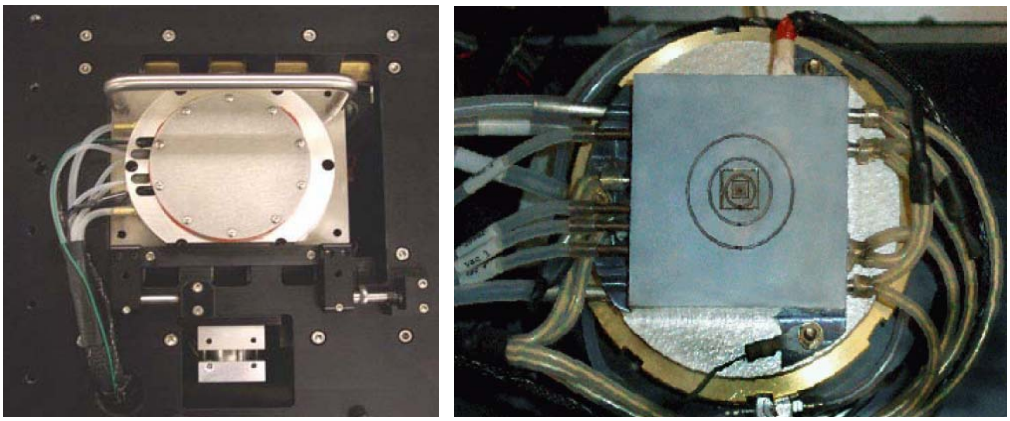


Figure 4.9 Optical probe inserted between the upper and lower chucks [34]

A pedestal tool is required to mount the die on the upper chuck. Both the dies and the pedestal are held during bonding through an externally supplied utility vacuum. Out of the two chucks, the upper chuck is fixed, whereas the bottom chuck is movable around the x, y, z and theta axes. This allows for precise alignment of the lower die to the upper [34]. Figure 4.10 shows a picture of the upper and lower chucks.



(a) (b)

Figure 4.10 (a) Upper Chuck and (b) Lower Chuck [34]

The chucks can reach a maximum temperature of 400°C and are capable of holding die 1 inch in diameter. The system also utilizes a planarization method called the pitch and roll (P & R) to allow the lower chuck to conform to the plane of the upper chuck. This ensures bonding accuracy and eliminates shearing forces from the dies during bonding. The bonder is available with both a vacuum held Floating P & R and a motorized P & R system to position the samples in parallel orientation. The Floating P & R uses a contact planarization technique to create a coplanar relationship between the chucks, while the Motorized Pitch and Roll is used in conjunction with a visible autocollimator [34].

The machine functions and operations are controlled through a Main User Interface, shown in figure 4.11. It contains all the controls for system operation in both button and menu form.

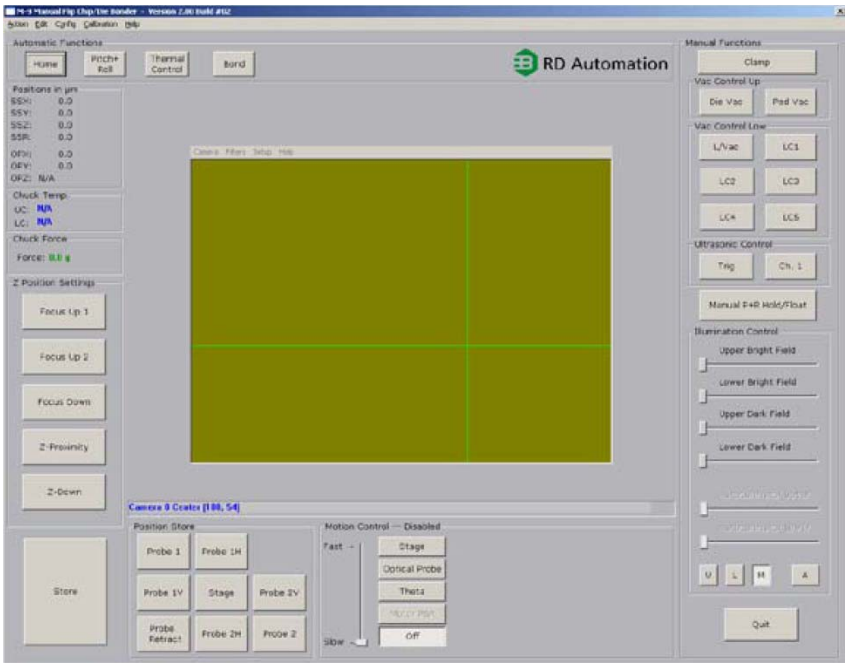


Figure 4.11 Main user interface [34]

4.2.3 Die Bonding Using 80Au/20Sn Solder Alloy

Soldering with 80Au/20Sn has been used in the microelectronics industry for hermetic sealing, die attach applications and to bond large metal components together. It offers several advantages when creating hermetic solder joints and packaging elements at wafer scale. For example, the ability to create a hermetic joint between metalized surfaces without use of flux, which eliminates post reflow cleaning. It also imparts superior thermal and electrical properties to the device packaging when compared to other solders and possesses a low intermetallic growth rate when used in conjunction with Ni, Ta, Ti, Pd or Pt base metallization [28].

The 80Au20Sn eutectic consists of AuSn and Au5Sn intermetallic phases. The eutectic alloy consists of 64.3% Au5Sn and 35.7% AuSn by mass. No free tin exists in the true eutectic but is found as the mixture of the two intermetallic compounds. From the phase diagram, this eutectic composition is defined by very steep liquidus lines on both sides of the eutectic melting point, indicating that enriching the composition by one percent of gold leads to an approximate 30°C increase in melting temperature. For this reason, the creation of AuSn solder forms requires accurate control of solder composition and bonding temperature [35].

Bonding process parameters have already been identified based on the previous soldering experiments using 95Sn/5Au. These are: bonding temperature, bonding pressure and dwell time at peak temperature. Die level bonding was conducted using the flip chip bonder to understand and analyze the process parameters and their effect on bond strength and hermeticity.

4.2.3.1 Bonding Procedure

Calibration of the machine for parallel alignment between the chucks needs to be done every time the machine is started. For floating pitch and roll calibration, the lower chuck is brought in contact with the upper chuck until the force sensor reads between 1000gm – 1500 gm. With the pressure applied the manual P + R button is turned on and off. This releases the vacuum holding the lower chuck allowing it to float on air and self align itself to the planarity of the top chuck. The value of force drops after releasing the button. The vacuum is turned on again to lock the chuck in that

position. The above step is repeated until no considerable drop in the force is observed. On the other hand, the motorized pitch and roll, utilizes a motorized tilt mechanism in the lower chuck together with a pair of autocollimators in the optical probe to parallel align the lower chuck to the upper chuck. A pair of dc motors tilts the lower chuck causing the intersection of the collimated beams of light, reflected off of both upper and lower bonding surfaces to achieve parallelism. After planarization vacuum is used to hold the lower chuck in position.

After calibration, the samples are loaded into the bonder. The MEMS chip die with the base metal deposition is placed on the lower chuck, where the cap chip die with solder metal deposition is mounted on the top chuck with the help of a pedestal tool. The alignment marks on the dies are aligned to each other while looking through the optical probe, which has the capability to simultaneously image the top and bottom chuck.

Post alignment, the bonding cycle is set where in the value of bonding force (calculated by dividing the bonding pressure value chosen by the total bonding area), bonding temperature and dwell time are entered in through the main user interface. The temperature is increased after the bonding force has been applied on the dies to avoid any contamination or oxidation of the molten solder. Upon the reaching the desired values, the pressure and temperature is held constant for a pre-specified time i.e. the dwell time. After the bonding cycle is complete the upper chuck releases the vacuum and the bonded die pair can be unloaded.

4.2.3.2 Experiments Performed

Die bonding experiments for perimeter sealing of a silicon die to another silicon or glass die for hermetically packaging of MEMS devices. The following metals were deposited on the dies:

1. Silicon die (bottom chip):

- Die size: 10mm x 10mm x 0.5mm
- Base Metal: 0.05µm of Ti + Pt 0.15µm of Pt + 0.1µm of Au

2. Silicon or Pyrex die (Cap chip):

- Die size: 10mm x 10mm x 0.5mm
- Base Metal: 0.05µm of Ti + Pt 0.15µm of Pt + 0.1µm of Au
- Solder metal: 2µm of Sn + 2.933µm of Au

The solder metal was deposited on the using two different approaches:

1. Sputtered as alternating layers of Sn and Au to reach a solder composition of 80Au/20Sn by weight percentage

2. Sputtered as 80Au/20Sn alloy

Process Parameters: The three parameters identified from the preliminary experiments using the hot plate set up were varied to analyze their affect on the output. The heating and cooling rates were kept constant at 1°C/sec, whereas the temperature, pressure and dwell time were varied one at a time while keeping the others constant. The dies were cleaned with Acetone and IPA. Four our case, the output is defined in terms of solder wetting, hermetic seal and bond shear strength. The solder wetting is inspected using a microscope. The hermeticity is measured in accordance with the MIL-

STD-883G METHOD 1014.12 test conditions C4 and C5 - optical gross/fine leak using the Norcom optical leak tester. The shear test will be conducted following the MIL-STD-883G METHOD 2019.7 test for die shear strength using the Instron microtester. The initial process window created used the following values:

- Bonding pressure (PSI) – 40 - 200
- Bonding temperature (°C) – 320, 340
- Dwell time (min) – 2 – 30 min
- Pitch and Roll – Motorized and Floating

Experiment:

Die pairs with 80Au/20Sn deposited as alternating layers were bonded using these process parameters. Solder was deposited as alternating layers. The die pairs were de-bonded by dropping them onto a steel surface from a height. The de-bonded dies were inspected under a microscope for solder wetting. Table 4.1 below summarizes the individual parameters for each die pair.

Table 4.1 Process parameters used for die bonding (set1 – set 10)

Set No.	Ring Width (mm)	Pressure (psi)	Force (kg)	Temp (°C)	Bond Formed	Solder Wetting
1	1.25	60	1.84	320	No	No
2	2.0	60	2.69	320	Yes	Little
3	1.0	80	2.02	340	Yes	Little
4	2.0	40	1.79	340	-	Little
5	1.5	80	2.86	340	No	Little
6	1.0	80	2.02	340	Yes	Yes
7	1.75	80	3.24	340	Yes	Yes
8	1.5	80	2.86	340	Yes	Yes
9	1.75	150	6.08	340	Yes	Yes
10	1.25	200	6.14	340	Yes	Yes

Observations: The bonding process for set1 – set5 was such that the chucks were heated to the target temperature before applying the bonding pressure. Little or no solder wetting from the solder on the cap chip was found on the gold metallization on the bottom chip. This is due to contamination/oxidation of the molten solder. Hence, the dies should be brought in close contact with each other before ramping up the temperature. For set6 – set10, the chucks were heated after applying the bonding pressure. Consequently, more solder wetting was observed for these die pairs when de-bonded. However, the wetting was not uniform over the whole bonded area. One

possible reason for that was imperfect parallel alignment between the dies. Set9 and set10 were bonded using the floating pitch and roll planarization system; where the lower chuck self aligns itself to the co-planarity of the upper chuck. Also higher pressures of 150psi and above showed more solder wetting. Uniformity in the solder wetting was observed for these die pairs when de-bonded. Figure 4.12 and 4.13 shows the microscopic pictures of the solder wetted area on the bottom chip.

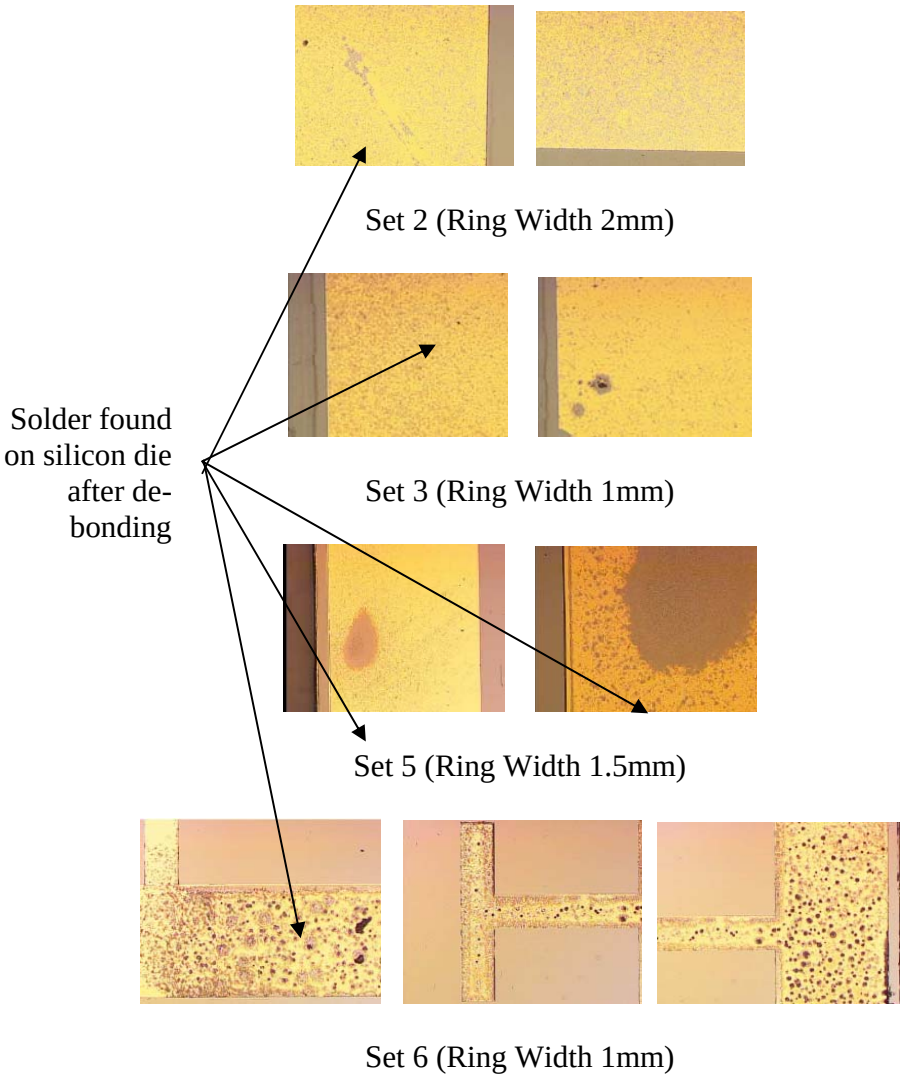


Figure 4.12 Solder wetted gold metallization on the bottom chip (set 2 – set 6)

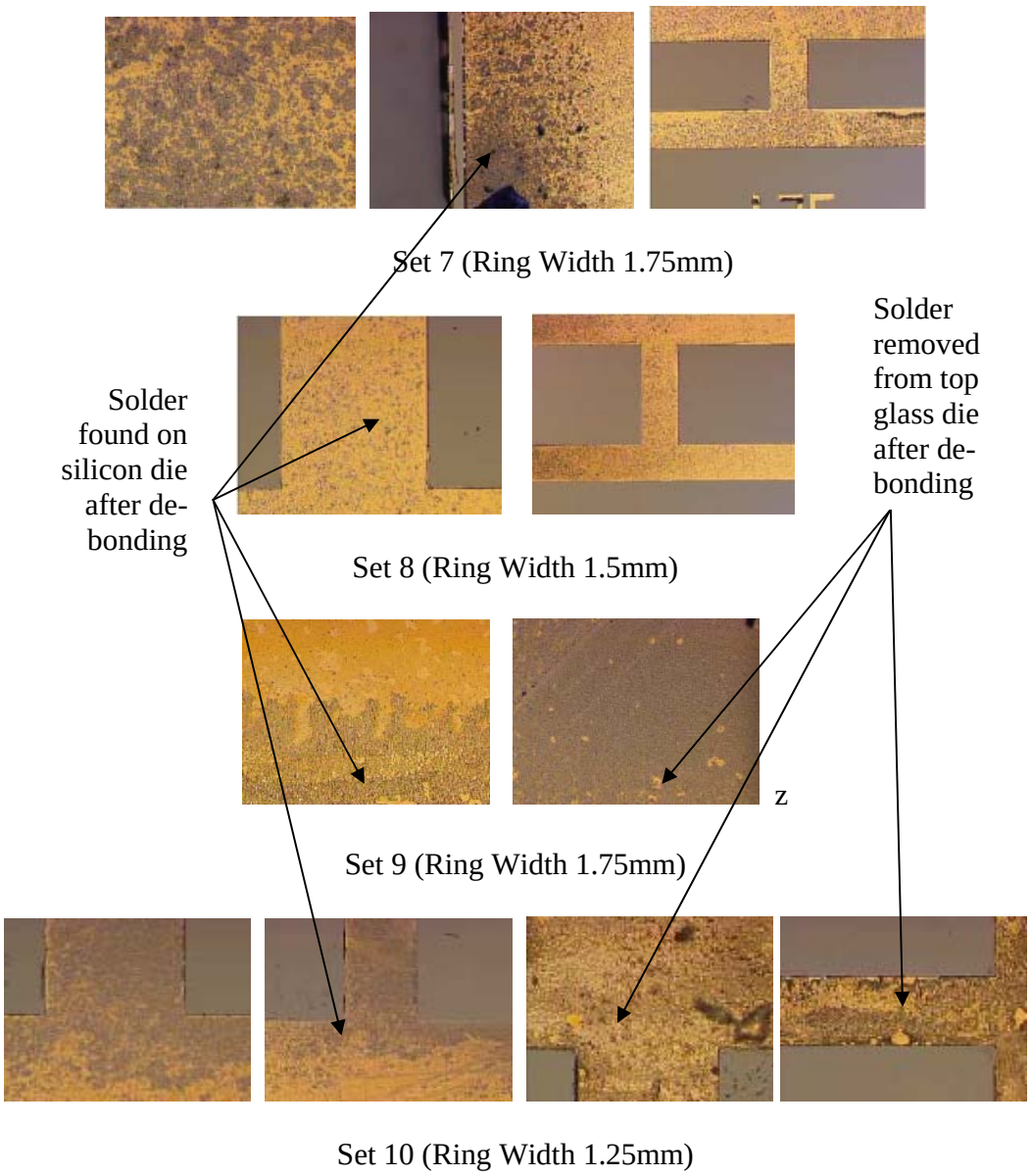


Figure 4.13 Solder wetted gold metallization on the bottom chip (set 7 – set 10)

Conclusion: It was observed that floating pitch and roll yields to a better parallel alignment between the two chucks and hence a more uniform bond around the perimeter sealing ring. Also application of bonding pressure prior to bonding

temperature prevents the oxidation and contamination of the molten solder. Result of which is more solder wetting of the base metallization.

For the next set of experiments, planarization of the chucks was achieved using floating pitch and roll. Bonding experiments were carried out with 80Au/20Sn deposited as both alternating layers and as alloy.

Experiment:

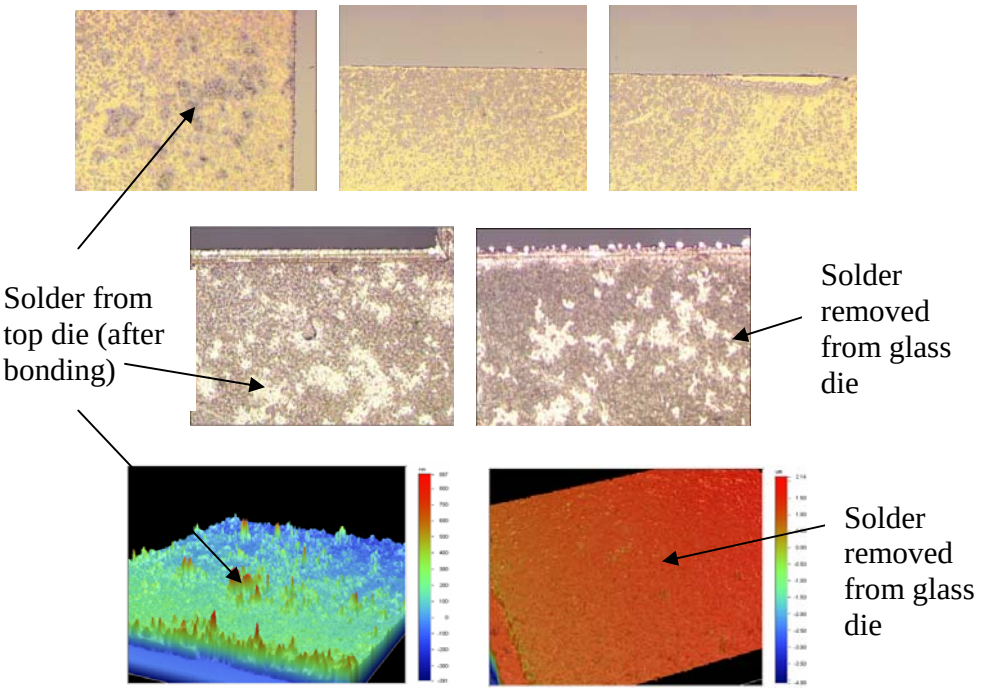
For set 11 – set 15, 80Au/20Sn solder was deposited as alternating layers along the perimeter seal ring on a with perimeter sealing ring on a glass die. For set 16 – set 20, 80Au/20Sn was deposited in alloy form. Higher values of pressure were used (above 100psi) while the bonding temperature and dwell time were kept constant at 340°C and 15 min respectively. To de-bond the sample, the die pair was dropped from a height on to a steel surface. Only set 11, set 12, set 14 and set 16 have been de-bonded.

Table 4.2 Process parameters used for die bonding (set11 – set 15)

Set No.	Ring Width (mm)	Pressure (psi)	Force (kg)	Temp (°C)	Bond Formed	Solder Wetting
11	1.25	100	3.07	340	Yes	Yes
12	1.25	150	4.61	340	Yes	Yes
13	0.75	200	3.90	340	Yes	-
14	0.75	250	4.87	340	Yes	Yes
15	0.5	300	4.00	340	Yes	-

Different points over the perimeter of the samples were inspected under the microscope before and after bonding. Traces of solder were found on the silicon die. 3D surface profiles were measured using the Veeco Wyko NT1100 3D profiler. Microscopic pictures and surface profiles of the dies are shown in Figure 4.14 and 4.15.

Observation (Set 11): Wetting of the base metal layer occurred were spotted. Solder traces were found over 50% of the total bonding area. However, no wetting was found on the top side of the perimeter sealing ring.



Set 11

Figure 4.14 Microscopic pictures and 3D profiles of top and bottom dies (set 11)

(Set 12): More amount of solder was found on the silicon surface as compared to set 11. This is due to the higher pressure 60% of solder wetting was found on the silicon die

(Set 14): The glass die could not be completely de-bonded from the surface of silicon. Solder layer was found on the silicon surface after de-bonding.

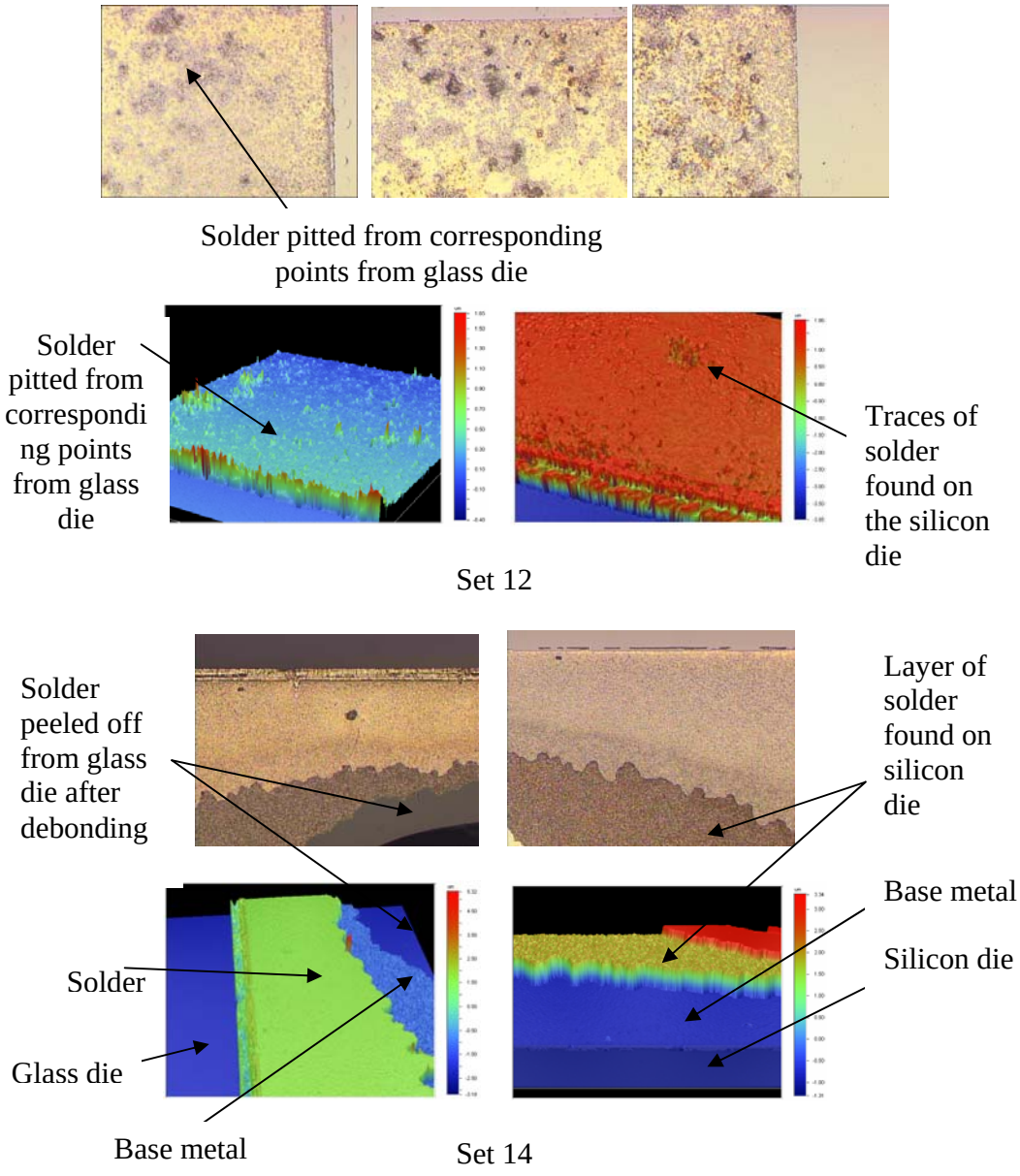


Figure 4.15 Microscopic pictures and 3D profiles of top and bottom dies (set 12 and 14)

Table 4.3 Process parameters used for die bonding (set16 – set 20)

Set No.	Ring Width (mm)	Pressure (psi)	Force (kg)	Temp (°C)	Dwell Time (min)	Bond Formed
16	1.25	100	3.07	340	15	Yes
17	1.25	150	4.61	340	15	Yes
18	0.75	200	3.90	340	15	Yes
19	0.75	250	4.87	340	15	Yes
20	0.5	300	4.00	340	15	Yes

Observation: De-bonding was tried only on set 16, by dropping it from a height onto a steel surface. The die pair broke into two pieces but could not be ripped apart. Bond strength was higher than set 11, 12 and 14.

Conclusion: More solder wetting was observed on dies bonded at pressures higher than 150psi. Bond strength for dies bonded with solder deposited as alloy was higher than the ones with solder deposited as alternating layers. Die shear test were performed on the remaining dies to better evaluate the bond strength.

Based on the above experiments a DOE matrix was created to evaluate which parameter, amongst temperature, pressure and dwell time, has the most significant affect on the bond strength. The following values were used for pressure, temperature and dwell time:

- Bonding pressure: varied from 50psi – 200psi
- Bonding temperature: 320°C, 340°C

- Dwell time: varied from 5 – 20 min

Table 4.4 Process parameters used for die bonding (set 21 – set 30)

Set No.	Ring Width (mm)	Pressure (psi)	Force (kg)	Temp (°C)	Dwell Time (min)	Force at failure(N)
21	2.0	50	2.24	320	10	130
22	2.0	75	3.37	320	5	100
23	2.0	75	3.37	340	10	150
24	1.75	100	4.05	320	10	80
25	1.75	150	6.08	320	10	410
26	1.5	150	5.37	340	20	210
27	1.5	200	7.16	340	5	250
28	1.25	200	6.14	320	20	240
29	1.25	250	7.68	340	20	220
30	1.0	300	7.59	320	10	190

The de-bonded die pairs were visually inspected under microscope. Pictures and 3D profiler readings from set 21, 22 and 25 are shown below in Figure 4.16. Surface profile after de-bonding for set 25 is shown in Figure 4.17.

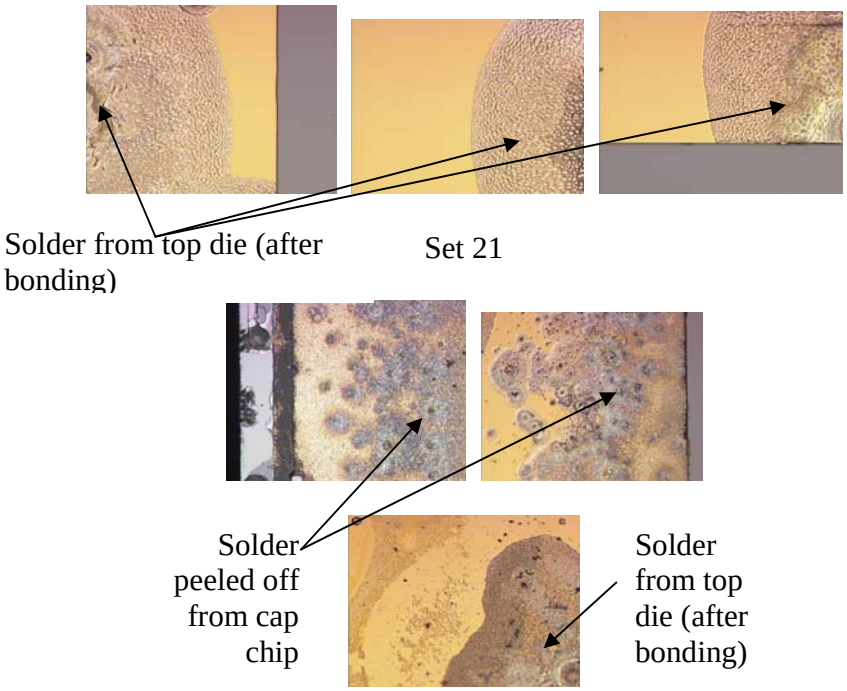
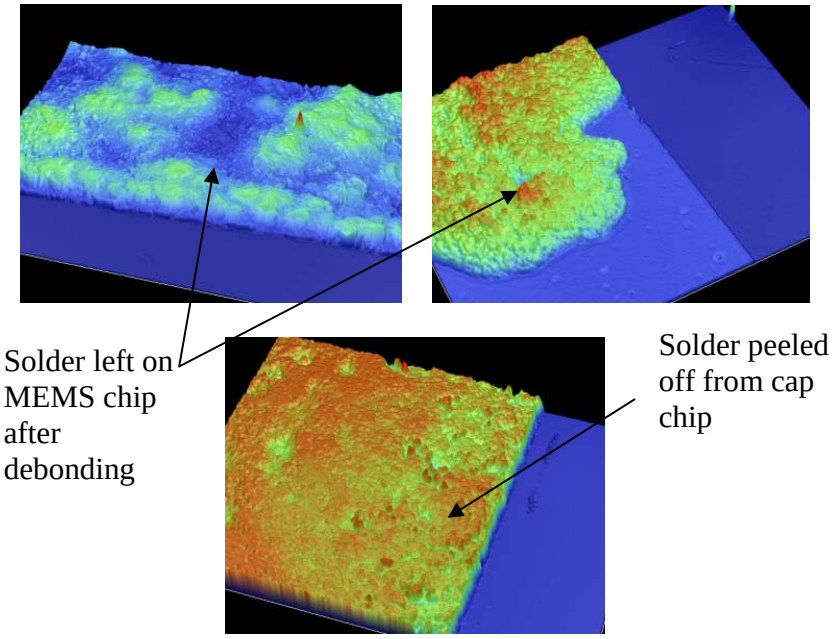


Figure 4.16 Microscopic pictures of top and bottom dies (set 21, 22 and 25)



Set 25

Figure 4.17 3D profiles of top and bottom dies (set 25)

Observation: A shear test was performed on the dies to evaluate bond strength. The shear test was performed using the Instron Microtester. For set 22, 23, 24, 27, the top die cracked from the corners leading to a slippage of the tool. Cracking of the die occurs if the force applied is less than the shear force that the die pair can withstand. This implies that the bonded die pair can withstand a shear force at least equal to or greater than the value at which failure occurred.

Around 75% of solder wetting was found for set 25 after debonding and 40% of solder wetting was found for set 37. Other sets were not fully disengaged to assess the total solder wetted area.

Conclusion: From the experiments if was found that the bonding temperature has the most significant impact on the bond strength followed by bonding pressure and

dwell time. Higher bond strength is achieved with solder deposited in the alloy form. It is difficult to achieve the precise ratio of 80:20 with deposition done as alternating layers. Enriching the composition of Au by 1% leads to a 30°C rise in melting temperature and hence the bonding temperature. This in turn would affect the bond strength since the process is highly sensitive to temperature.

4.3 Electrical Interconnection Continuity Testing

Continuity testing was performed on the bonded die pair to validate the formation of vertical interconnections between top and the bottom dies. The top Si/Pyrex die has dimensions of 0.8cm x 0.8cm where is the bottom Si die is 1cm x 1cm. Individual snapshots of the two dies is shown in Figure 4.3. The snapshot of the die pair after bonding is shown in Figure 4.18.

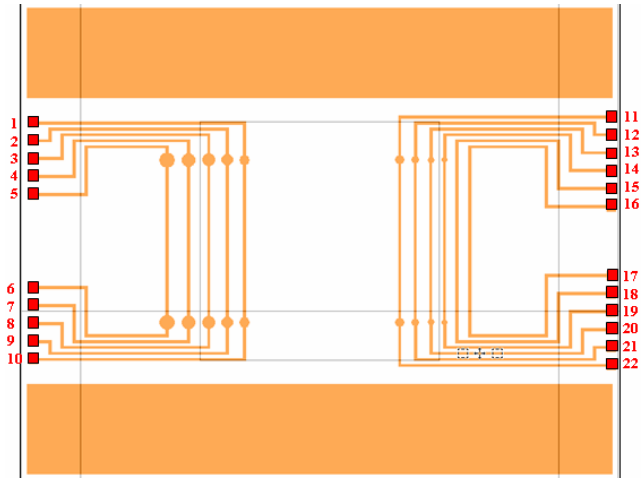


Figure 4.18 Bonded die pair for electrical continuity testing

The bottom die connects the electrical interconnection pads to contact pads for electrical continuity testing and resistance measurement across interconnects. Figure 4.19 shows a picture of the wire bonded die pair.

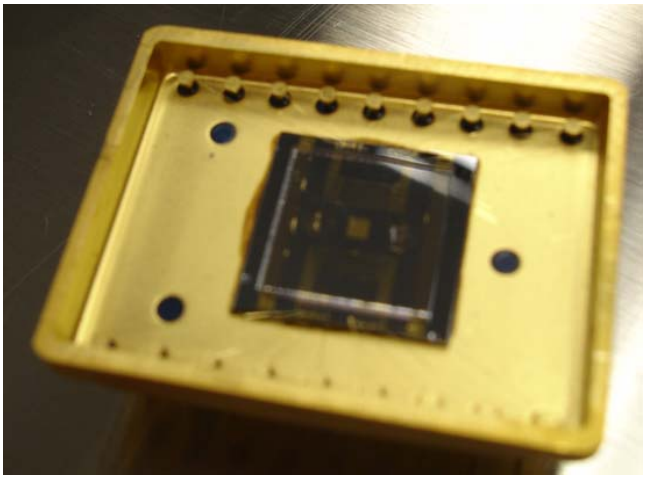


Figure 4.19 Wire bonded die pair

An optical probe station and a National Instrument's DAC interface were used to perform electrical testing. Continuity tests were performed using the digital multimeter interface of National Instrument's NI-6259 card. Electrical paths were found to be formed between silicon and Pyrex bonded wafer due to solder reflow. Resistance measurements for interconnects need to be performed to further characterize them. However, it is out of scope for this thesis.

4.4 Conclusion

The following conclusion can be drawn from the experiments carried out:

1. It is difficult to achieve fluxless soldering with 95Sn/5Au due to oxidation of tin.

2. A precise control of the bonding parameters, such as temperature, pressure, dwell time and ramp rates is required to achieve a bond.

3. Planarization system using floating pitch and roll provides better parallel alignment as compared to motorized pitch and roll.

4. Solder deposited as alloy of 80Au/20Sn yields better bond strength than that compared to solder deposited as alternating layers.

5. Bonding temperature has the highest affect on bond strength followed by bonding pressure and dwell time.

6. Continuity tests for interconnections were performed and electrical paths were formed between the top and bottom dies using thermo-compression bonding.

CHAPTER 5

MODELLING OF 3D INTERCONNECTS

5.1 Introduction

Modeling of 3D interconnects is done to dimension design interconnects in terms of their diameter and pitch. The vertical interconnects designed for die stacks would eventually be used to drive thermal MEMS devices. Hence, it is important examine the current carrying capacity of interconnects at different diameters. Also, interconnects have parasitic inductance, resistance and capacitance associated with them. Small length of interconnects is designed for faster propagation and low losses at higher frequencies (30 GHz), as parasitics increase the RC delays and reduce the speed of the operation. Secondly, fine interconnect pitch increases the crosstalk between two adjacent interconnects [36]. Hence interconnects need to be modeled resistance, capacitance and inductance to pick the optimum values of length, diameter and pitch. The following two analyses can be done:

1. Low frequency analysis: This includes a high current, low density and low frequency analysis. A high current is passed through interconnects to examine the increase in temperature across it due to joule heating.

2. High frequency analysis: This includes the following one analysis:

a) A high current, high density and high frequency analysis: This is done to understand the skin effect which comes into play at higher frequencies, resulting in an increase in the effective resistance of interconnects.

5.2 Low Frequency Analysis

The low frequency analysis utilizes a finite element approximation (FEA) to numerically predict the steady state temperature distribution across interconnect due to joule heating.

Joule Heating: It is defined as the increase in temperature of the conductor as a result of resistance to an electric current flowing through it.

As the interconnect diameter changes the resistance of the interconnect changes according to

$$R = \rho \frac{l}{A}$$

where, R is the resistance

ρ is the resistivity of the material

l is the length of interconnect

A is the area of interconnect

Decreasing the interconnect diameter decreases the area and hence results in an increase in its resistance value. This in turn raises the temperature across interconnect due to Joule heating. The purpose of this modeling is to know the minimum value of the

interconnect diameter at which the temperature across it is equal to higher than the re-melting temperature of the solder.

5.2.1 3D Model

The 3D model of interconnect sandwiched between a silicon and glass substrate is shown in Figure 5.1. The following dimensions were used:

1. Bottom silicon chip: 5mm x 5mm x 0.5mm
2. Metal deposition on silicon chip:

- Base Metal: The base metal was modeled as a single layer of Au 0.3µm thick, instead of three layers of Ti, Pt and Au with a total thickness of 0.3µm. The diameter of the base metal is varied from 1µm – 50µm.

3. Top pyrex glass chip: 5mm x 5mm x 0.5mm
4. Metal deposition on pyrex glass chip:

- Base metal: The base metal was again modeled as a single layer of Au 0.3µm thick, instead of three layers of Ti, Pt and Au with a total thickness of 0.3µm. The diameter of the base metal is varied from 1µm – 50µm.
- Solder metal: The thickness of the solder metal is 5µm and diameter is varied from 1µm – 50µm

Solid 98 element was used to obtain a mesh. The mesh size for the bottom Silicon and the top Pyrex glass substrate was 500µm. The mesh size for the solder was 1µm and that of the base metal layers were 0.25µm.

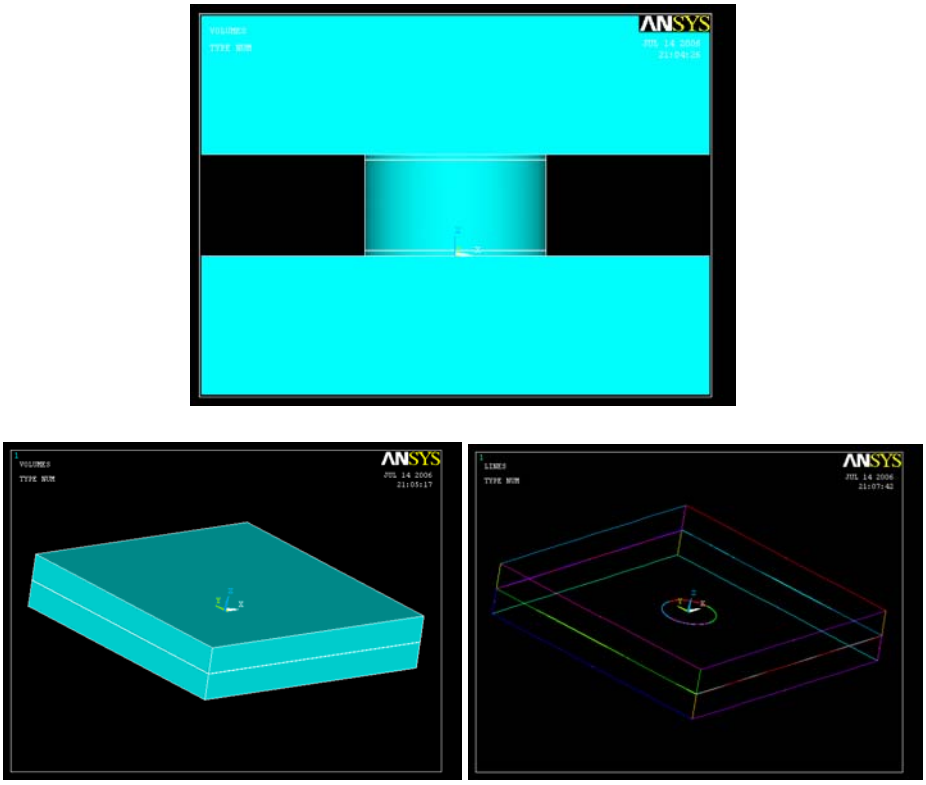


Figure 5.1 3D model

5.2.2 Boundary Conditions

The symmetrical boundary condition in a single block is applied as following:

1. Structural boundary conditions:

a) Silicon substrate is attached to the package frame and thus has fixed degree of freedom (DOF) in x, y, z coordinate, i.e. zero deflections.

b) The side wall deformation of brick element has only vertical elongation. This approximation is explained by two physical interpretations: first, the regular expansion of each block in x, y coordinate cause zero expansions at symmetrical

configuration. Second, the Pyrex glass end is not fixed and is free to move vertically in z-direction.

2. Thermal Boundary conditions:

a) The bottom surface of silicon substrate is attached directly to package surface whose temperature remains at the 21°C.

b) The upper surface of Pyrex glass is exposed to ambient. The natural heat convection coefficient and the thin film temperature are 50 W/m^2 and 21°C, respectively.

c) Heat generated from each brick element is assumed to be similar. Hence, the amount of heat transferred per unit normal area is zero (adiabatic) at the symmetrical configurations. i.e. the side walls of brick element have maximum temperature distribution.

3. Voltage boundary conditions:

a) Potential voltage is applied across top and the bottom base metal layers which sandwich solder ball.

The air gap layer which is sandwiched between glass and silicon substrates has small thickness of 5.6μm. Thus, a good representation of the air thermal behavior is by considering a conductive air layer instead convective layer with finite electrical resistivity of 3Gohm-m.

5.2.3 Material Properties

Table 5.1 gives the material properties used for the analysis. The electrical resistivity of the solder composition 80Au/20Sn and that of 95Sn/5Au is not known and was hence approximated to the resistivity of gold.

Table 5.1 Material Properties [37]

Material	Thermal Conductivity (W/m-K)	CTE (um/m-°C)	Modulus of Elasticity (GPa)	Poisson's Ratio	Electrical Resistivity (ohm-cm)
Si	124	3.61	112.4	0.28	0.01
Au	301	14.6	77.2	0.42	2.2e-6
Sn	63.2	30	41.4	0.33	1.15e-5
80Au/20Sn	57	16	-	-	-
Pyrex	1.1	3.25	62.75	0.2	8x1010
Air	0.0299	-	-	-	-

5.2.4 Temperature Profiles

Two solder compositions for interconnect were inspected – 95Sn/5Au and 80Au/20Sn. Their steady state temperature distribution was plotted. Interconnects would be used to power a thermal MEMS device with a typical current consumption of 100mA. Hence, a constant current of 100 mA was applied across interconnects to assess their maximum current carrying capability at different interconnect diameters.

a) 95Sn/5Au: The electrical resistivity for this solder is not known hence it was assumed to be as that of pure tin. The maximum temperature across interconnect at different diameters is given in the Table 5.2 below.

Table 5.2 Maximum temperatures across interconnects at different diameters for 95Sn/5Au

Interconnect Dia (µm)	Resistance (ohm)	Current (A)	Voltage (V)	Temperature (°C)
2	2.01E-01	0.1	2.01E-02	149.1
3	8.95E-02	0.1	8.95E-03	49.1
4	5.04E-02	0.1	5.04E-03	30.7
5	3.22E-02	0.1	3.22E-03	25.1
10	8.06E-03	0.1	8.06E-04	21.3
20	2.01E-03	0.1	2.01E-04	21.0

b) 80Au/20Sn: The electrical resistivity for this solder is not known hence it was assumed to be as that of pure gold. The maximum temperature across interconnect at different diameters is given in the Table 5.3 below.

Table 5.3 Maximum temperatures across interconnects at different diameters for 80Au/20Sn

Interconnect Dia (μm)	Resistance (ohm)	Current (A)	Voltage (V)	Temperature (°C)
1	1.54E-01	0.1	1.54E-02	76.2
2	3.85E-02	0.1	3.85E-03	25.7
3	1.71E-02	0.1	1.71E-03	22.02
4	9.63E-03	0.1	9.63E-04	21.3
5	6.17E-03	0.1	9.63E-04	21.3

5.3 High Frequency Analysis

The skin effect plays a significant role at high operating frequencies of interconnects.

Skin Effect: Skin effect is the tendency of AC at higher frequencies to distribute itself within a conductor such that the current density at the surface of the conductor is greater than that at its core. This limits the cross-sectional area of the conductor available for carrying the current, thus increasing the resistance of the conductor to the flow of current through it. The effective resistance is higher than that at DC or low AC frequencies [38]. This phenomena is depicted in the figure below:

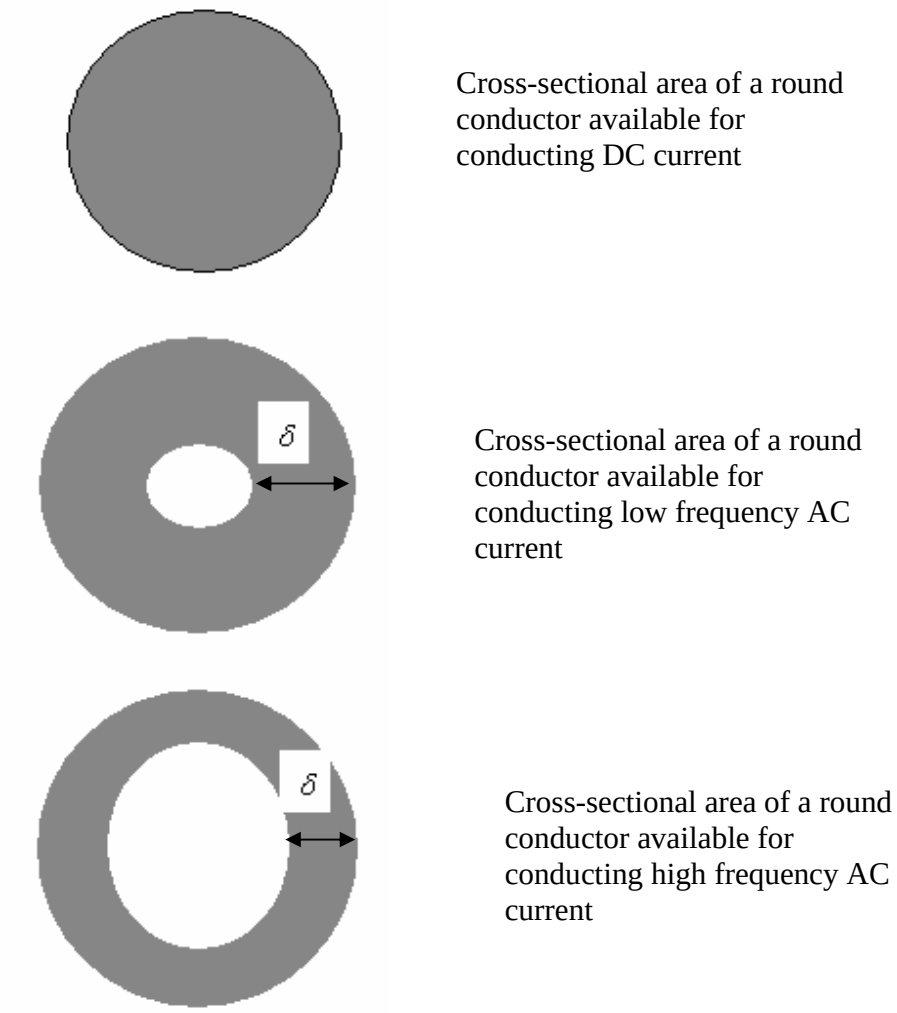


Figure 5.2 Skin depths for DC and AC [38]

Skin Depth: It is defined as the distance through which the amplitude of a traveling electromagnetic wave decreases by a factor of e-1 or 0.368. It's also called the depth of penetration of the conductor and is given as [39]:

$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}}$$

where δ is the skin depth

f is the frequency of operation

μ is the permeability of vacuum = 1.26x $^{10\text{-}12}$H/µm

σ is the electrical conductivity of the material

The value for skin depth is calculated at frequencies varying from 100MHz – 50GHz and is tabulated below. The electrical conductivity of 80Au/20Sn is approximated to that of pure Au and the electrical conductivity of 95Sn/5Au was approximated to that of pure tin. The values for skin depth are plotted vs. frequency for both the solder compositions. Electrical conductivity for Au is 45.2 x 10^6/m-ohm and that Sn is 8.6 x 10^6/m-ohm. Table 5.4 and 5.5 below gives the value for skin depth at different operating frequencies for 80Au/20Sn and 95Sn/5Au respectively.

Table 5.4 Calculated skin depth values for 80Au/20Sn

Frequency (GHz)	Permeability (H/μm)	Conductivity (S/μm)	Skin Depth (μm)	Attenuation (μm^{-1})
1.00E+09	1.26E-12	4.52E+01	2.36E+00	4.23E-01
3.00E+09	1.26E-12	4.52E+01	1.37E+00	7.32E-01
5.00E+09	1.26E-12	4.52E+01	1.06E+00	9.46E-01
1.00E+10	1.26E-12	4.52E+01	7.48E-01	1.34E+00
1.50E+10	1.26E-12	4.52E+01	6.11E-01	1.64E+00
2.00E+10	1.26E-12	4.52E+01	5.29E-01	1.8E+00
2.50E+10	1.26E-12	4.52E+01	4.73E-01	2.11E+00
3.00E+10	1.26E-12	4.52E+01	4.32E-01	2.32E+00
3.50E+10	1.26E-12	4.52E+01	4.00E-01	2.50E+00
4.00E+10	1.26E-12	4.52E+01	3.74E-01	2.67E+00
4.50E+10	1.26E-12	4.52E+01	3.53E-01	2.84E+00
5.00E+10	1.26E-12	4.52E+01	3.34E-01	2.99E+00

Table 5.5 Calculated skin depth values for 95Sn/5Au

Frequency (GHz)	Permeability (H/μm)	Conductivity (S/μm)	Skin Depth (μm)	Attenuation (μm^{-1})
1.00E+09	1.26E-12	8.6	5.42E+00	1.84E-01
3.00E+09	1.26E-12	8.6	3.13E+00	3.19E-01
5.00E+09	1.26E-12	8.6	2.42E+00	4.12E-01
1.00E+10	1.26E-12	8.6	1.71E+00	5.83E-01
1.50E+10	1.26E-12	8.6	1.40E+00	7.14E-01
2.00E+10	1.26E-12	8.6	1.21E+00	8.25E-01
2.50E+10	1.26E-12	8.6	1.08E+00	9.22E-01
3.00E+10	1.26E-12	8.6	9.90E-01	1.01E+00
3.50E+10	1.26E-12	8.6	9.16E-01	1.09E+00
4.00E+10	1.26E-12	8.6	8.57E-01	1.17E+00
4.50E+10	1.26E-12	8.6	8.08E-01	1.24E+00
5.00E+10	1.26E-12	8.6	7.67E-01	1.30E+00

Skin depth vs. frequency for 80Au/20Sn and 95Sn/5Au solder compositions is plotted in Figure 5.3 below.

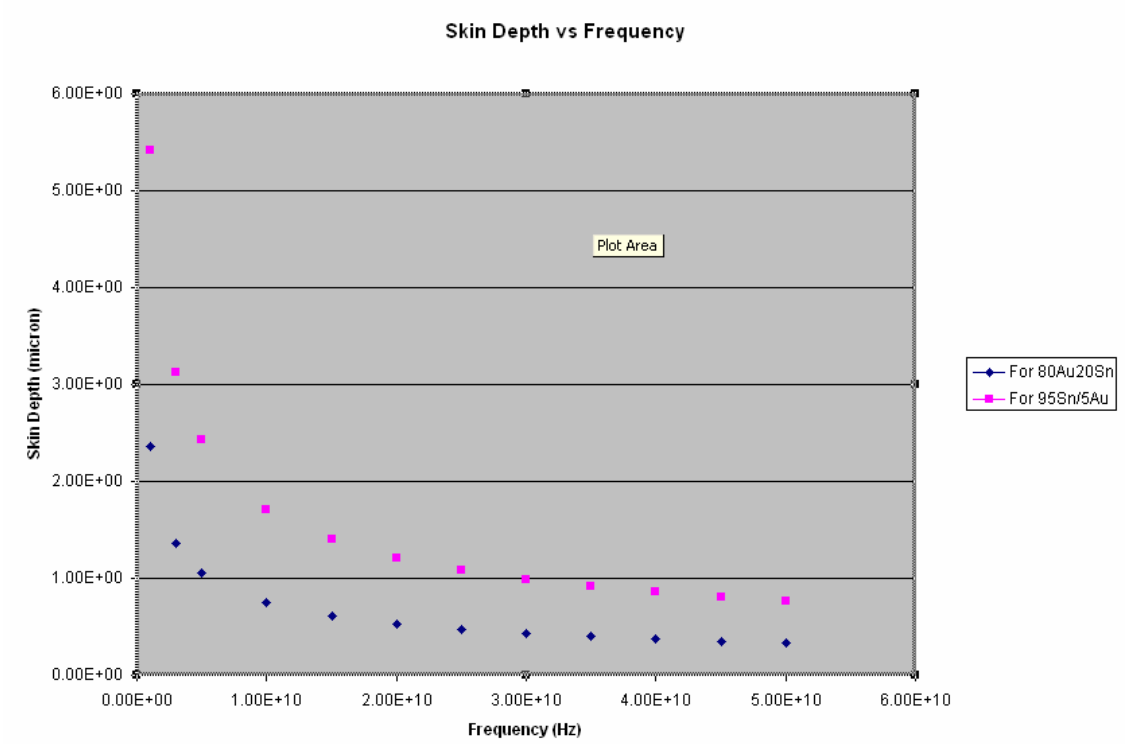


Figure 5.3 Plot of skin depth vs. frequency for 80Au/20Sn and 95Sn/5Au

It is seen from the graph that at higher frequencies the depth of penetration decreases i.e. the current is more concentrated at the outer surface of interconnect. The available area of interconnect for current flow decreases which in turn increases the effective resistance of interconnect. The change in the resistance is calculated as below:

Also, the resistance to current flow increases as the interconnect diameter decreases. This implies that the resistance of interconnect for smaller diameters is high at high frequency of operation. Thus the power loss across interconnect due to heat dissipation (i.e. joule heating) would be higher. The area of interconnect is calculated as below:

$$A = \pi[r^2 - (r - \delta)^2]$$

$$A = \pi(r^2 - r^2 - \delta^2 + 2r\delta)$$

$$A = \pi(2r\delta - \delta^2)$$

where, r is the radius of the interconnect

δ is the skin depth

Effective resistance of interconnect is calculated as:

$$R = \rho \frac{l}{\pi(2r\delta - \delta^2)}$$

Thus the power loss across interconnect is given as:

$$P = I^2 R$$

The graph in Figure 5.4 and 5.5 plots the power dissipation at different operating frequencies for varying values of interconnect diameters. Both 80Au/20Sn and 95Sn/5Au solder compositions are plotted.

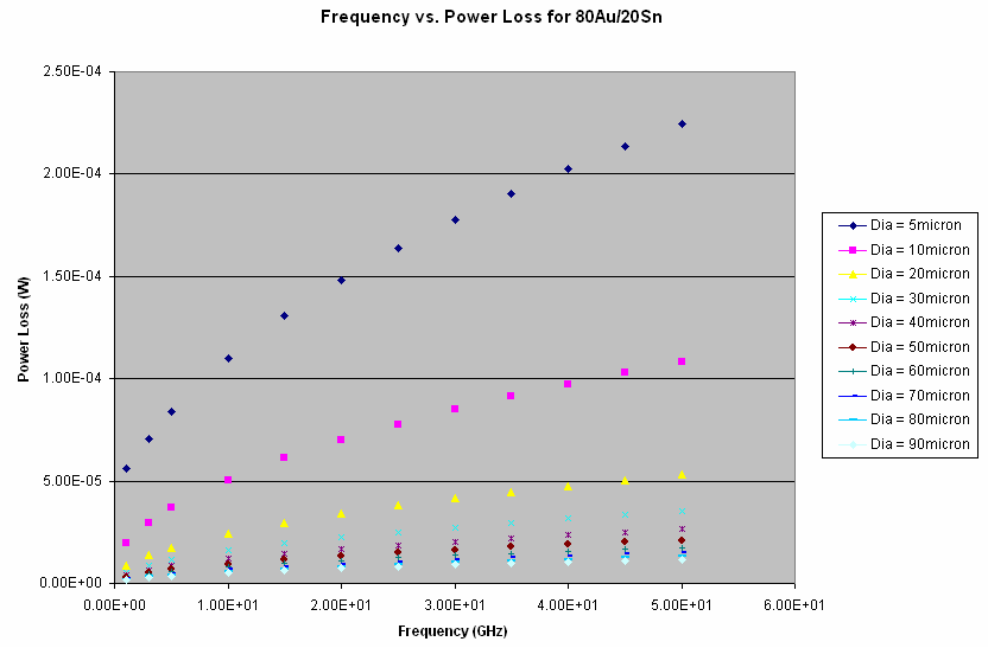


Figure 5.4 Power losses vs. frequency for different interconnect diameters for 80Au/20Sn

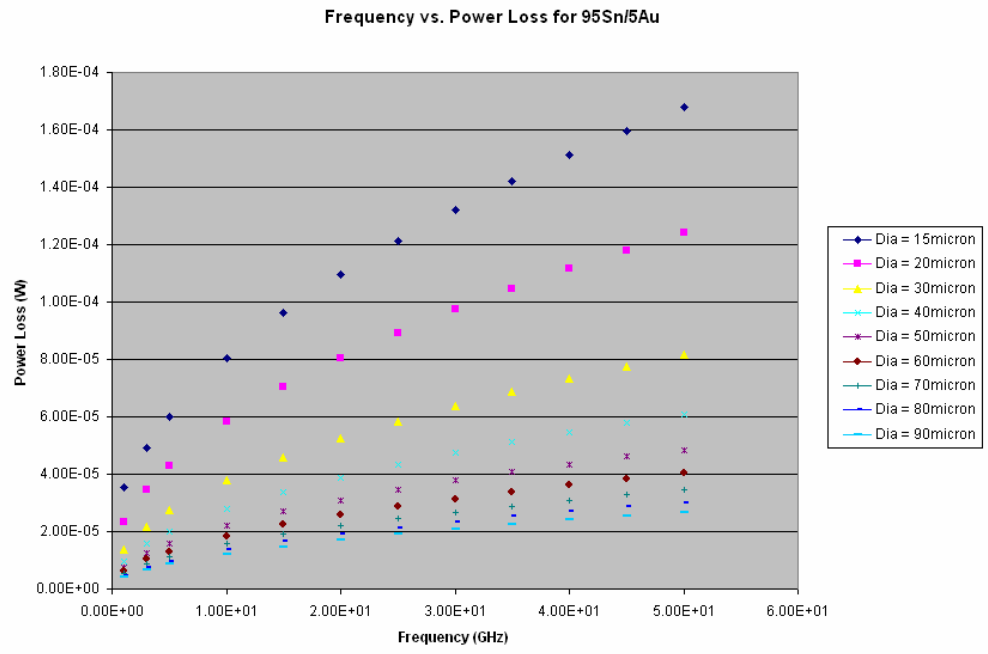


Figure 5.5 Power losses vs. frequency for different interconnect diameters for 95Sn/5Au

5.4 Conclusions

A low frequency analysis was done to plot the temperature distribution across interconnects at different diameters for a constant current value of 100mA. It was observed that even with the smallest diameter of 2µm for 95Sn/5Au and 1µm for 80Au/20Sn the temperature stays within the re-melting temperature limit of interconnect. However, the interconnect starts to heat up. Hence, for 95Sn/5Au composition minimum interconnect diameter of 10µm and for 80Au/20Sn composition, a minimum interconnect diameter of 5µm can be chosen. At these values of diameter, temperature across interconnect reaches a maximum of 21°C. For this analysis the electrical resistivity is approximated to that of pure Au and Sn, since the resistivity values for 80Au/20Sn and 95Sn/5Au solder compositions are not known.

From a high frequency analysis we observe that at an operating frequency of 1GHz, the penetration depth is 2.36µm for 80Au/20Sn and 5.42µm for 95Sn/5Au. Hence the minimum interconnect diameter to be designed for 80Au/20Sn should be equal to or greater than 5µm. For 95Sn/5Au it should be equal to or greater than 15µm. The simulation results for the low frequency analysis and the calculated skin depth and power loss values for the high frequency analysis depends on the material property assumptions made for the analysis and may differ if these assumptions are changed.

Small interconnect diameter (<10µm) help in achieving a high interconnect density; however the power losses due to heat dissipation increase at high operating frequencies. They also possess a low current carrying capacity due to Joule heating. It is also difficult to achieve precise alignment with small interconnect diameters.

CHAPTER 6

CONCLUSIONS AND FUTURE WORK

3D electrical interconnects between wafer stack were formed through solder bump reflow. A 4 inch Si wafer was bonded to another 4 inch Pyrex glass wafer using a adhesive polymer glue, Benzocyclobutene (BCB). It was found that BCB layer cured at 55% and above does not reflow during bonding. Two solder compositions were experimented as interconnect metal - 95Sn/5Au and 80Au/20Sn. The interconnect metal is deposited through evaporation. Solder reflow was performed and bump heights were measured using a 3D profiler. However, 95Sn/5Au being a Sn rich solder is extremely difficult to reflow because of oxidation of Sn. This is evident from the profiler results of 95Sn/5Au.

Also a fluxless soldering process was developed for hermetic packaging of MEMS device. Die bonding was carried out using the Laurier M9 Flip Chip bonder. Vertical interconnects between the bonded die pair was formed using thermo-compression bonding and interconnects were tested for electrical continuity. Interconnects would supply power to a thermal MEMS device with a typical current consumption of 100mA. Hence, a constant current of 100mA was supplied to interconnects for a low frequency analysis. The analysis showed that minimum interconnect diameter values of 5μm for 80Au/20Sn and 10μm for 95Sn/5Au can be

chosen without heating up of interconnects. However, from a high frequency analysis was done with operating frequencies between 1GHz – 50GHz. The analysis showed that at an operating frequency of 1GHz, the minimum interconnect diameter for 80Au/20Sn should be equal to or greater than 5µm. For 95Sn/5Au it should be equal to or greater than 15µm. These values of interconnect diameters are obtained from the simulation results and the calculated skin depth and power loss values which depend on modeling assumptions.

As a continuation to this work bond strength of the BCB bonded wafers need to be evaluated. Also resistance measurements of interconnects need to be performed to further characterize them. The bonded die pairs for die level bonding need to be tested for hermiticity and shear strength to further understand the impact of bonding parameters. Electrical characterization of the vertical interconnects formed through thermo-compression bonding need to be performed. A low current, high density and high frequency analysis for interconnects need to be performed to extract the capacitance values between two interconnects. These extracted capacitance value can be used as a guideline to select the correct interconnect pitch.

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