3-D FRACTURE STUDY OF THE BEoL *Cu/Low-k* STACK TO ASSESS AND MITIGATE THE CPI RISK DURING THE REFLOW PROCESS

by

ZAEEM BAIG

Presented to the Faculty of the Graduate School of

The University of Texas at Arlington in Partial Fulfillment

of the Requirements

for the Degree of

MASTER OF SCIENCE IN MECHANICAL ENGINEERING

THE UNIVERSITY OF TEXAS AT ARLINGTON

DECEMBER 2013

ACKNOWLEDGEMENTS

I am really grateful to my advisor, Prof. Dereje Agonafer for his continuous guidance and support. A special thanks goes out to Prof. Haji-Sheikh and Prof. Kent Lawrence for serving on my committee and providing numerous learning opportunities.

This work would not have been possible without the continuous guidance of Fahad Mirza and the readily available help from Hardik Parekh and A.R. Nazmus Sakib. I would like to thank my friends and colleagues who made these past couple of years a memorable one. A special shout out goes to Ms Sally Thompson and to Ms Debi Barton for assisting me in all everything from enrolling in classes to helping me travel to conferences.

I cannot express enough thanks to my parents and family who made all this possible and supported me throughout: my deepest gratitude.

November 8th, 2013

ABSTRACT

3-D FRACTURE STUDY OF THE BEOL CU/LOW-K STACK TO ASSESS AND MITIGATE THE CPI RISK DURING THE REFLOW PROCESS

Zaeem Baig, M.S.
The University of Texas at Arlington, 2013

Supervising Professor: Dereje Agonafer

As scaling of components continues, using SiO_2 as a dielectric in the Back-End-Of-Line (BEoL) is no longer a viable option and can be replaced with low-k and ultralow-k (ULK) dielectric materials for advanced integrated circuits (IC) packaging solutions. The low-k materials improve performance by reducing parasitic capacitance and crosstalk between adjacent metal lines. However, low-k dielectrics have lower modulus, lower fracture toughness, higher coefficient of thermal expansion (CTE), and poor adhesion as compared to SiO_2. Thus, low-k dielectric integration in the contemporary IC packages poses a significant reliability challenge. Delamination along the metal-dielectric interfaces and crack propagation in the dielectric layers has been widely observed during cooling from higher temperatures and thermal excursions. This provides the impetus for this work. In this study, 3D finite element (FE) analysis is performed to demonstrate the thermo-mechanical response of the BEoL region of a flip chip package with Pb-free solder interconnects. Crack propagation in the low-k layers is analyzed under the loading when the die is attached to the substrate (reflow). J-integral obtained from the FE analysis is

utilized to identify the dielectric layer most susceptible to crack propagation. Thickness of the metal layer, adjacent to the critical dielectric layer is increased and the new J-integral values are computed. This work suggests reinforcing the critical low-k layer by increasing the thickness of the adjacent metal layer can be an effective way to mitigate the dielectric crack issue.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

Figure Page

LIST OF TABLES

Table Page

NOMENCLATURE

IC	Integrated Circuits
PCB	Printed Circuit Board
SMT	Surface Mount Technology
CSP	Chip Scale Package
SMD	Surface Mount Devices
FEoL	Front End of Line
BEoL	Back End of Line
UBM	Under Bump Metallization
*f*BEoL	Far Back End of Line
RC	Resistive-Capacitive
CTE	Co-efficient of Thermal Expansion
CPI	Chip Package Interaction
FE	Finite Element
MLFE	Multi level Finite Element
BGA	Ball Grid Array
RDL	Redistribution Layer
FSG	Flourinated Silicate Glass
DOE	Design of Experiment
ULK	Ultra Low-K

CHAPTER 1

INTRODUCTION

1.1 Electronics Package

1.1.1 Electronics Package-Basics

Almost all the electric devices that we see and encounter in our modern day lives have a processor or some sort of Integrated circuit (IC) present inside. What we see is not the actual chip or the IC with all its circuitry visible and exposed, but the black plastic mold housing all the interconnects and electronic components. This whole assembly of the chip and housing is collectively called an electronic package.

Cluff, K.D., et. Al in the “Mechanical Engineering handbook” define electronic packaging as the “the art and science of connecting circuitry to reliably perform some desired function in some application environment. [1]” These packages include different electrical components like transistors, capacitors, resistors, diodes which in turn must be interconnected to perform a specific task. The connection of multiple devices to perform a function is called a circuit. As this level of integration increases, these multiple circuit connections are moving towards integrated circuit (IC) chips.

Not only do these ICs need to be structurally supported and interconnects environmentally protected during handling and processing, but the heat generated due to current passing through interconnects (Joule heating) must be allowed to dissipate to the surrounding efficiently.

This efficient heat removal is imperative because any temperature rise beyond certain range would adversely affect the device performance.

Thus, an electronic package must serve some essential functions:

- Signal Distribution
- Power Distribution
- Heat Dissipation
- Mechanical Support, chemical, electromagnetic and environmental protection

These functions of electronic package are illustrated in figure 1.1 below.

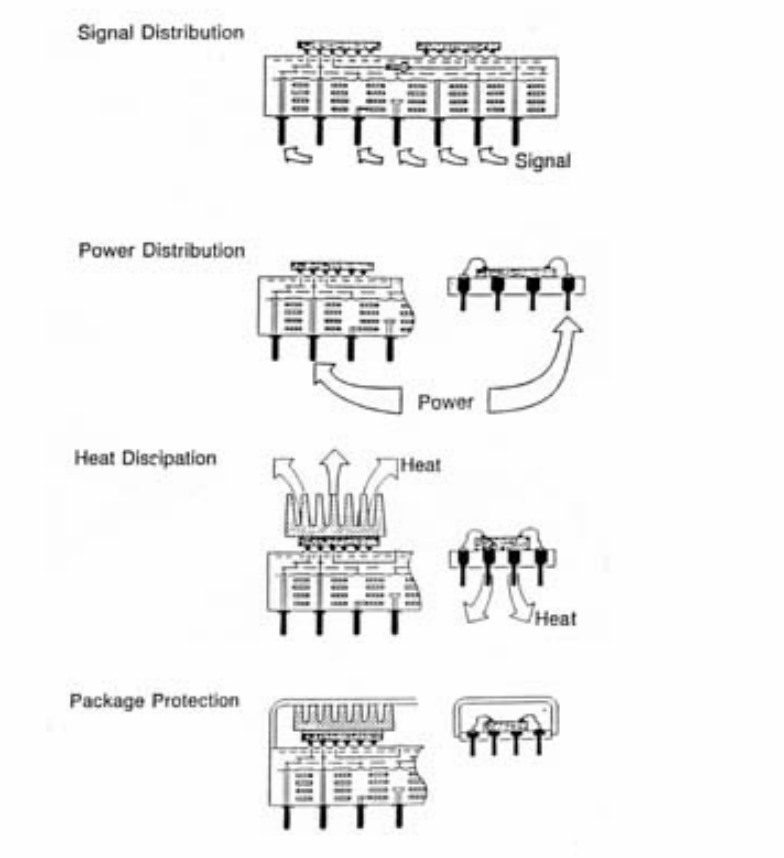


Figure 1.1 Four Main Functions of Electronic Packaging [2]

In addition to these requirements electronic package should function at pre-specified performance level of the product. [2]

1.1.2. Package Technology

Progress of packaging technology can be categorized into three stages as shown in figure 1.2

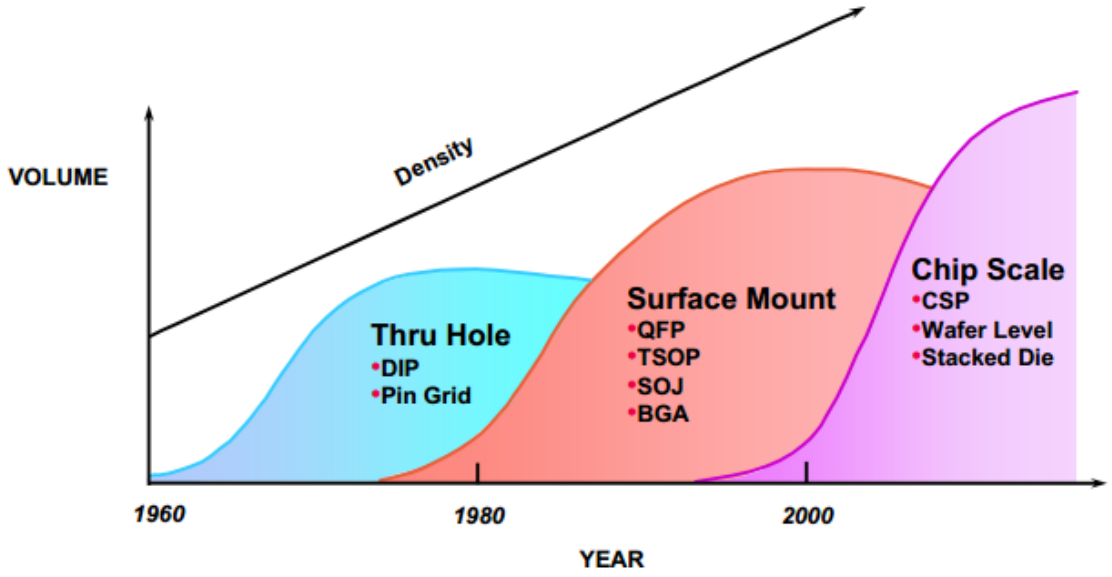


Figure 1.2 Electronics Packaging Technology [3]

Initially Semiconductor industry used Through hole technology to mount package on board in which pins of the component go through the previously drilled holes in PCB. In this kind of packaging signal has to pass through all PCB layers and due to low density one sided mounting was available. To fill the gap Surface Mount Technology (SMT) was invented which allowed pins of the device to directly mount on the surface of PCB. Provided much higher density and can be mounted at both sides of PCB [4]. A generic schematic diagram showing the difference between the surface mount technology (upper) and through hole mounting (lower) is shown in figure 1.3

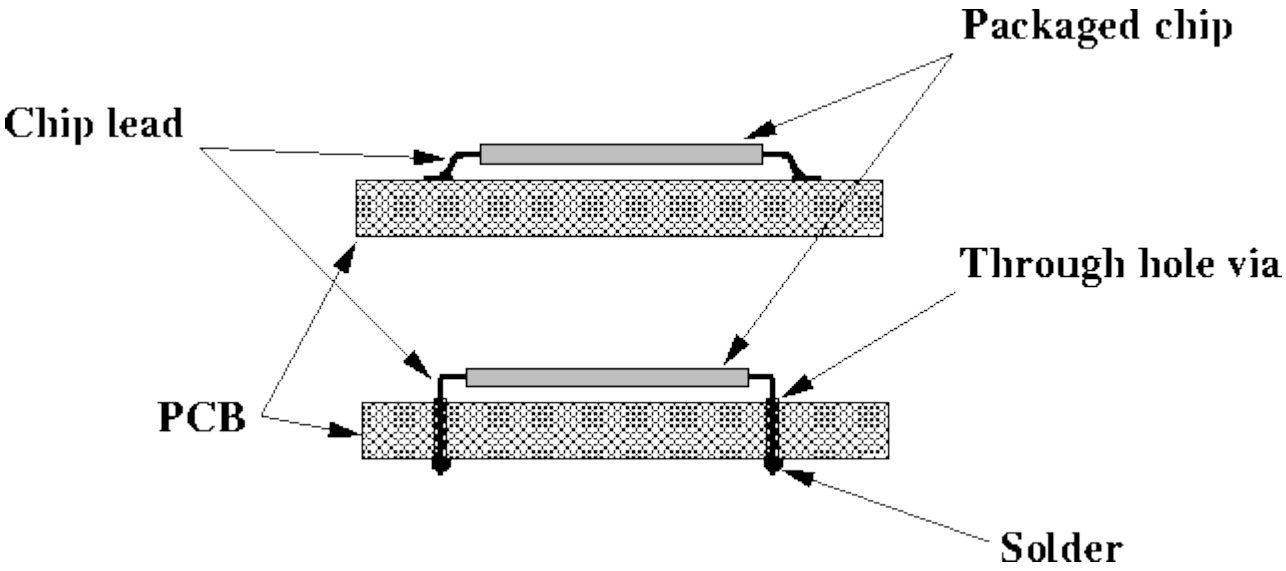


Figure 1.3 Through Hole vs Surface Mount Technology [5]

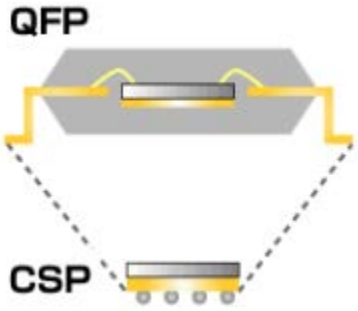


Figure 1.4 Chip Scale Packages [6]

Chip Scale Package, or CSP, based on IPC/JEDEC J-STD-012 definition, is a single-die, direct surface mountable package with an area of no more than 1.2 times the original die area. CSP is an evolution of SMT in which passive components such as resistors, capacitors must also be miniaturized to further improve the speed performance. These packages are hardly serviceable due to difficult fabrication process and there are issues related to long term reliability which need to be taken care of [3].

1.2 Flip Chip Package

1.2.1. Flip chip Package Introduction

Although, first introduced in 1964 by IBM in 1964 as Controlled Collapse Chip Connection (C4), it was not until recently that flip chip interconnect technology gained popularity. There are several reasons for flip chip technology's rise in popularity. The wire bond package usually limits the number of interconnects with the package and substrate. But in the case of the Flip chip package the entire surface of the die is used for the interconnect purpose so eventually the package size can be scaled down with increased features [7]. Also, in wire bond package interconnects are longer so signal delay is also an issue.

The typical flip-chip packaging technique is described in Figure 1.5

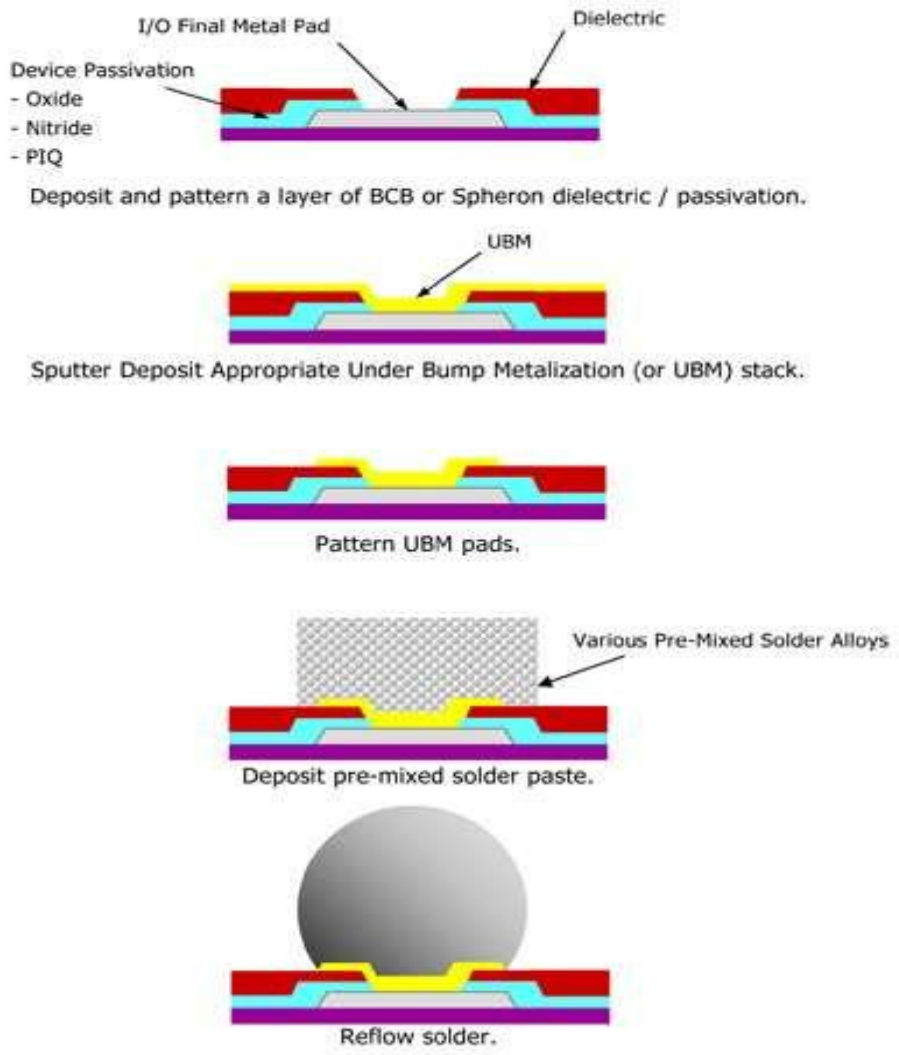


Figure 1.5 Flip Chip Processes [7]

In the first step, called the wafer bumping, passivation layer is coated on the top of the wafer and then the under bump metallization layers are electroplated on the patterned passivation layer. The UBM (under bump metallization) layers provide good solder wettability, good adhesion, and adequate electrical and mechanical connection between the device and solders. In the next stage, the unwanted UBM metal layers are etched away followed by the deposition of the solder alloy on the top of the pattered UBM

layers. The whole assembly is then heated to the reflow temperature and as cooling starts solder starts taking its usual round shape. The wafer is then sliced into individual dies for packaging. Finally an underfilling process is done in the gap between die and substrate to strengthen the solder joints and to protect the metal interconnects from the elements. [7]

1.3 Cu/low-k Interconnects

The exponential growth in device density has yielded high-performance microprocessors containing 2 billion transistors [8]. The continuing improvement in device performance requires scaling of all the features of an IC e.g. gate length, gate dielectric thickness, metal line width, etc. As the feature size reduces, resistive-capacitive delay (RC delay), cross talk, and power dissipation of the interconnect structure come into play and can limit the performance of the device. To overcome these issues and ideally to avoid them, certain changes in the process and geometry have to be made. In addition new materials have to be incorporated in the interconnect and packaging structures [8].

Traditionally aluminum (Al) and silicon dioxide (SiO_2) were used in the metal/ di-electric stack in the back-end-of-line (BEoL) of a package, but as the scaling of components continued the metal lines started getting closer and the dielectric thickness continued to decrease. This resulted in increased cross-talk between metal lines and signal delay. Unlike gate delay, which decreases linearly with reduction in feature size, interconnect delays increase with the square of reduction in feature size. So beyond a certain threshold node the

performance of the device is not governed by the feature size but by the interconnect distance and that threshold node is 0.18µm [9]. This can be visualized in figure 1.6 below.

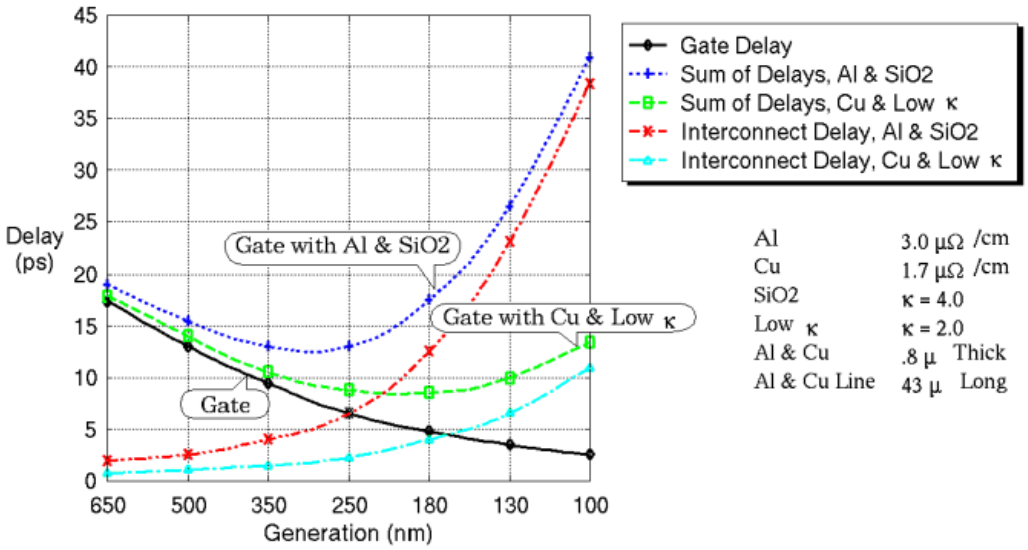


Figure 1.6 Delay vs. Technology Generation Node [4]

Adding more metal layers would have been the easy way forward to reduce the delay, but would have resulted in increased process and fabrication costs and at the same time generated more heat. Thus, affecting not only the performance but the reliability if the device. Instead, copper (Cu) was introduced as the replacement for aluminum in the metal/di-electric stack. Cu had a higher conductivity than aluminum (Al) as well as higher resistance to electro-migration, meaning that thinner metal lines could be used without any increased risk of bridging or break-up [9].

Cu alone could only provide a 30% improvement in performance, but when silicon dioxide (SiO_2) (k=3.9) was replaced by low-k (k<3) and ultra-low-k

(ULK) (k<2.5) as the dielectric in the metal/di-electric stack, a significant increase in the device performance was seen. A 266% improvement in performance could be achieved with ULK di-electric [9]. Figure 1.6 depicts the phenomenal improvement in performance that was achieved by migrating from Al/ SiO_2 to Cu/low-k interconnects.

To better visualize, as to where the BEoL region and more importantly the Cu/low-k stack is with respect to the all the other components in the package, a brief introduction of the IC fabrication process is required. IC fabrication consists of hundreds of individual processes inluding deposition, photolithography and etch, but broadly can be divided in two steps: Front-end-of-line (FEoL) and BEoL processing. FEoL is the first set of processes in device manufacturing where individual components such as capacitors, resistors and transistors are built on the silicon wafer [4].

Next is the stage where all the individual components need to be connected to each other and also to the rest of the package. This second stage is called the BEoL processing. During this stage metal layers are deposited to connect resistors, capacitors and transistors to one another. To connect these transistors to the rest of the device metal layers separated by dielectric layers are deposited and to connect different metal layers vias are used, as shown in figure 1.7.

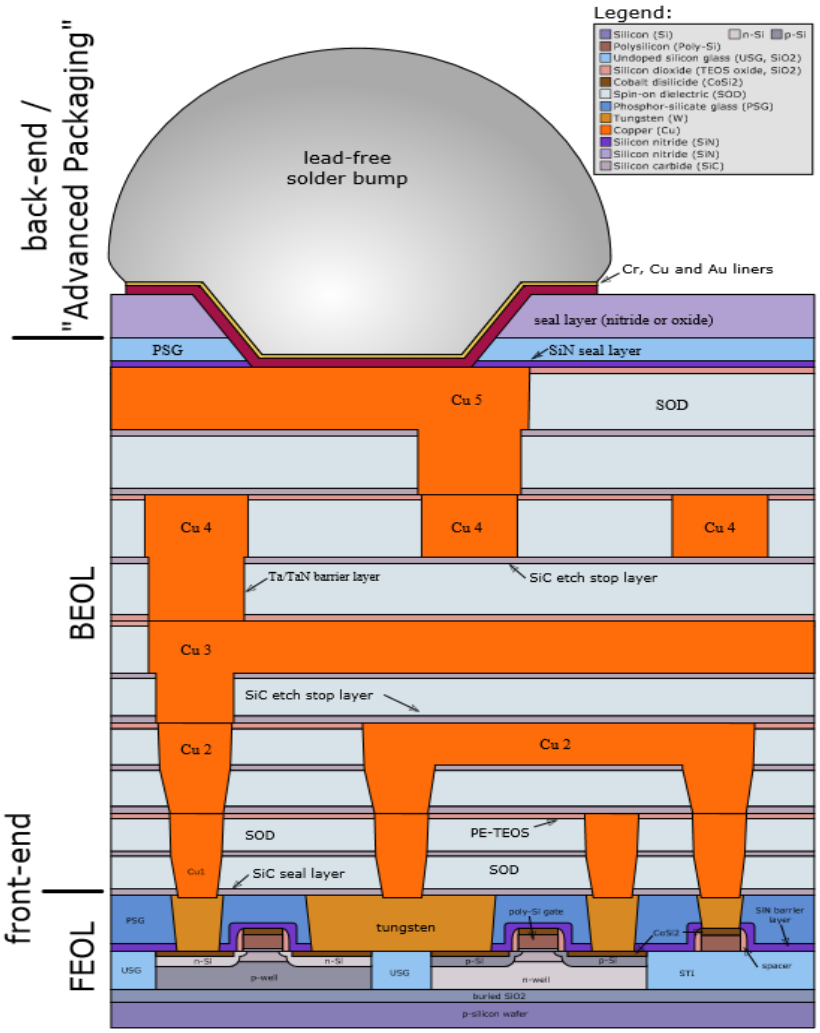


Figure 1.7 FEoL and BEoL [4]

1.3.1. Reliability issues with Cu/low-k Interconnects

As miniaturization continues, the semiconductor is driven to incorporate ULK di-electric material in the BEoL stack to reduce the delay and improve performance even more. However, doing so poses a risk from reliability standpoint. Low-k dielectric material is inherently porous and the porosity increases as we move towards ULK. This porosity in low-k and ULK dielectrics means that these materials have lower modulus, lower fracture toughness, higher coefficient of thermal expansion (CTE), and poor adhesion as compared

to SiO_2. Therefore, delamination along the metal-dielectric interfaces and crack propagation in the dielectric layers has been widely observed during cooling from higher temperatures and thermal excursions [10].

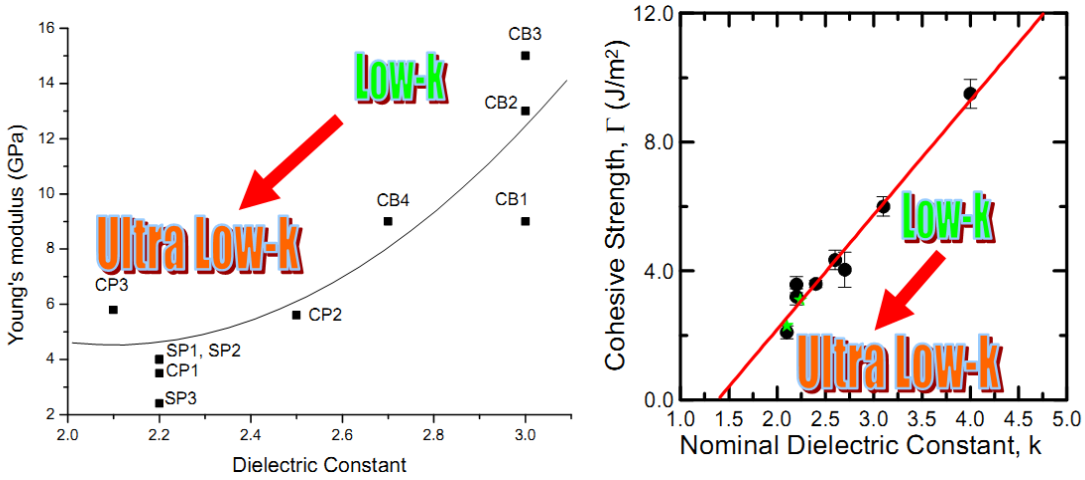


Figure 1.8 Effect of Increased Porosity [11]

Figure 1.8 illustrates the trend of deterioration in mechanical properties. As we move from low-k towards ULK the porosity increases and as a result Young's modulus and cohesive strength decrease. Due to brittleness and poor cohesive strength the di-electric material may fail during fabrication, even before the package has been incorporated in a consumer product. The ULK material may fail during the sawing process when the silicon wafer is diced into individual dies, or during the reflow when the chip is attached to the substrate. Failure in the di-electric material is predominantly either cracking of the low-k material or delamination along the metal di-electric interface. Due to its brittle nature crack can be introduced in the di-electric during dicing process which may propagate during the subsequent reflow process due to warpage and

thermo-mechanical stresses produced. Due to poor adhesion the metal and low-k layers might delaminate at higher temperatures [8].

This warping of the package and the peeling stress is primarily due to the CTE (Co-efficient of Thermal Expansion) mismatch between different materials present in the package. The important point to note is that the CTE mismatch between the Silicon and organic substrate dominates the warpage direction and magnitude. Typically during the chip attachment process the whole assembly is heated to temperatures around 200°C. During the cooling process, due to CTE mismatch between the chip and the substrate the whole assembly bends and this bending is called warpage. Due to this warpage bending stresses induces in low-k layers in BEoL, which may cause failure of brittle low-k material. Similarly the package has to go through the same process of heating and cooling during rest of the assembly/process when different components are being cured or attached [7].

1.4 Motivation of work

To tackle the aforementioned reliability issues, rising due to lower cohesive strength and adhesion of low-k materials, there is a need to understand the chip-package-interaction (CPI) risk under thermo-mechanical loading. The BEoL region most susceptible to failure needs to be identified and consequently techniques to mitigate the di-electric crack issue must be proposed. SnPb solders were predominant before the Pb-free solders were made mandatory for consumer electronics. Therefore, there is a need to establish a base line in order to gauge the effect of -replacing SnPb solders

with Pb-free solders on the BEoL, particularly on the fracture of low-k dielectric material. This would be helpful for defense and medical industry, which is still using SnPb solders but eventually has to move to Pb-free, to get at least a qualitative trend as to what impact will moving to Pb-free will have on the BEoL region of the package.

1.5 Objective and Scope

In this study a 3-D finite element technique is employed to examine the mechanical integrity of BEoL region during die attach process (reflow. Failures in microelectronics systems are mainly due to overstressing of components or due to wearout (gradual failure even at lower stress-fatigue). Since the system is under reflow condition, the failure can be attributed to overstressing of components, had we been doing thermal cycling then the failure would have been due to fatigue loading.

There are two ways to avoid failures;

- By reducing the stress (peeling stress)
- By reinforcing the critical area (failure prone area)

One way to do this is by changing in the geometry and/or material, but it will not be the most economical option. In this study a reinforcement technique is proposed that neither requires any material change nor any alterations in the overall package dimensions.

A 3-D Multi-Level Finite Element (MLFE) (sub modeling) technique has been leveraged to carry out whole analysis in ANSYS Workbench v14.5. Crack

propagation in the low-k layers is analyzed under the loading when the die is attached to the substrate (reflow). J-integral obtained from the FE analysis is utilized to identify the dielectric layer most susceptible to crack propagation (critical layer). Thickness of the metal layer, adjacent to the critical dielectric layer is increased in order to reinforce the critical layer and the new J-integral values are computed. The effect of this reinforcement on the overall stability of the metal/dielectric stack is also studied. In addition, BEoL damage between Pb-free and Sn-Pb solder alloy is also compared.

CHAPTER 2

LITERATURE REVIEW

Mercado et al. [12] studied the die attach process for both plastic ball grid array (PBGA) and ceramic ball grid array (CBGA). They used interface fracture mechanics-based approach to predict interfacial delamination and identified critical interfaces and locations for both packages. The impact of thin film residual stress was also incorporated in their analysis at both wafer level and package level. They reported that for both CBGA and PBGA die attach process the crack driving force for the low-k interfaces was significantly higher than what was seen for the wafer process. Due to higher process temperature CBGA die attach process was more critical and the crack driving force could exceed the interfacial strength for the low-k/passivation interface. At the end they suggested two solutions to avoid this failure; either improving the strength of low-k barrier interface or adding tiles and slots (crack stop structures) in low-k structures to reduce available area for crack growth.

Mercado et al [13] studied the effect of having either the low-k or SiO_2 as the last dielectric layer, using the fracture mechanics based finite element analysis. They also leverage multi-level finite element (MLFE) modelling approach in their 2-D analysis. They found out that the critical region was the last metal/passivation interface and using low-k material as the passivation layer for that interface would negatively impact the reliability. Furthermore, the

researchers investigated the effect of increasing number of layers in the metal/do-electric stack and concluded that the crack driving force in the top layers increased as the number of layers in the metal/dielectric stack increased. Since the last metal/passivation interface is most susceptible to delamination, replacing low-k with SiO_2 in the last layer seemed to mitigate the cracking and delamination issue.

Guotao Wang et al. [14] presented the experimental and modelling results from the investigation of the CPI and its impact on the BEoL integrity. They experimentally measured thermal deformation in a flip-chip package and compared it with the results from a 3-D multi-level finite element analysis coupled with the high resolution moiré interferometry. Crack driving forces at the Cu/low-k interfaces were computed and compared with corresponding interfaces in Cu/TEOS and Al/TEOS interconnect structures.

K. M. Chen [15] studied the ULK die crack failure during temperature cycling. He also performed a parametric finite element analysis to study the effect of underfill fillet height and fillet tip angle on the thermo-mechanical stress and validated the results experimentally. He concluded that low underfill height and smaller fillet tip angle can reduce the thermo-mechanical stress. Furthermore, he studied the effect of attaching a heat sink on the die to increase package stiffness and concluded that this mitigated the di-electric crack issue.

Fu et al [16] discussed CPI reliability issues, impact of crack stop design, mechanical properties of low-k /ultra low-k material, underfill material selection,

lead-free manufacturing and low-k/ultra low-k layers on CPI reliability. Furthermore, it has been emphasized that certain steps such as designing stronger crack stop, improving the adhesion and cohesive strength of low-k and ultra-low-k materials, selecting right underfill material , can significantly improve the reliability of the device.

Uchibori et al [17] studied the impact of CPI on Cu interconnects. They not only studied the effect of using different low-k materials but also the impact of moving from one technology node to the other. A 3D multi-level finite element modelling method was used. It was found that the thermo-mechanical integrity of Cu/low-k interconnects deteriorates by six times as the technology node changes from 90 nm to 65nm.

Che et al [18] carried out finite element simulation to compare the feasibility of using 3-D vs 2-D model. Testing was done for various metal/di-electric stacks having different structures. Moreover, they performed a parametric analysis for different solder bump materials, low-k stacks, UBM thickness, barrier layer material properties and shear heights. It was concluded that there was little change in the shear force across different low-k structures but more metal dielectric layers can reduce the stress along the critical low-k interface. It was reported that thinner UBM can reduce the interfacial stress induced by the solder bump deformation thus making the device more reliable.

Harman et al [19] mentioned various reliability problems associated with replacing wire bonds in the package with metal/dielectric stacks. Various issues like cracking, spalling and crazing of the low-k material and bond pad

indentation were discussed. Using low-k materials with high CTEs and low thermal conductivities can lead to higher stresses which may lead to more damage. They concluded that well designed low-k and under pad structures can overcome any bonding issues.

Jimmy et al [20] performed a 2D strain analysis to analyze the behavior of Cu/low-k stack in FCBGA package. They performed a parametric study replacing one FSG layer with polymer encapsulated dicing lane technology (PEDL), varying the height of Cu post, die thickness, and underfill selection. The goal was to minimize the peeling stress in the metal/di-electric layers and to minimize the inelastic energy in the solder bumps. Three different cases were simulated using 3-D finite element; (A) all rows with spherical solder joints, (B) 10 hourglass joints followed by 10 spherical joints and (C) 10 Spherical joints followed by 10 hourglass joints. It was found that case (C) gave the lowest inelastic strain energy dissipation and also the lowest stress in the Cu/low-k layers.

Yuan et al [21] developed a robust and rapid design procedure for a novel 3D stacking technique. They proposed the design procedure for a 3D-WLCSP structure with two chips stacked on top of each other, connected through wire bonds. Three parameters that affected the reliability of the test vehicle were put forward.

Kuo et al [22] developed a novel test methodology to accurately determine time temperature dependent mechanical properties of thin film materials. Specimen fabrication procedure, test program, modeling and

analysis are included in this test methodology. Also, this test can be extended to other polymer or metal thin films or solder material characterization. The investigation proved that mechanical behavior of underfill materials display strong temperature and strain rate dependent. In addition the cyclic creep strain rate was found to be higher than that of static creep strain rate which reveals the cyclic softening behavior. It was found that the interface of solder mask/FR4 is sensitive to temperature and moisture. The failure mode shifts from combined “adhesive and cohesive failure” to cohesive failure when test rate decreases.

Lai et al [23] verified the sub modelling technique applied in the reliability assessment of a FCBGA under accelerated thermal cycling. Far corner bump was taken as the sub model. Moreover, it was suggested that farther the boundary of the sub-model is from the enclosed bump, more accurate the predictions are for the fatigue indices. They built a detailed global model to verify sub modeling solutions and used that model as the benchmark to determine solution discrepancies cause by simplification of global model. It was concluded that if one can afford to conduct a comprehensive 3D analysis of the whole FCBGA, sub modeling may not be efficient because path dependent problems require numerical iterations and sub modelling would mean that more computation time is required.

Zhai et al [24] demonstrated experimentally that the CPI risk increases as we move towards low-k and ULK. They also reported that underfill material plays an important role in device reliability and risk of corner delamination can be mitigated by using an underfill material of lower modulus. Moreover, if the

underfill expands beyond a certain threshold, delamination of the metal/dielectric can occur.

Liu et al [25] leveraged MLFE modelling approach to investigate the parameters that drive the CPI failure. They determined that defect size in BEoL and the package geometry were dominant factors for delamination in the metal/di-electric layers. Finally they presented example of the “utility of modelling to optimize dicing to reduce defect size, and provide targets for crackstop toughness,” which had resulted in successfully qualifying the reliability guidelines for porous SiCOH to be used in45nm technology.

Wang et al [26] performed a finite element analysis and leveraged sub modelling. He modelled a bimetallic strip of two commonly used electronic packaging materials such as silicon and eutectic solder alloy. They then compared the results from the simplified global geometry with the results from detailed sub model geometry under fatigue loading. Results for sub modelling case were found to be more accurate.

Lofrano et al [27] studied that how different temperatures lead to stress induced voiding in low-k layers. 2D and 3D finite element models were used for three different configurations of BEoL interconnect structure. At first a 2D axisymmetric model was used but it was found that, stress gradient in asymmetrical plane was underestimated. 3D model was found to be more accurate

CHAPTER 3

FINITE ELEMENT MODELING

The following introduction to finite element method in this chapter is taken from Thiag Raman's Thesis with very slight changes [7]

3.1 Introduction to Finite Element Method (FEM)

"Among the various numerical methods, Finite element method is the most popular and widely used method. Other than this it is considered as the most sophisticated tool for solving engineering problems. In this method, the whole continuum is divided into a finite number of elements of geometrically simple shape. These elements are made of a number of nodes. The unknown are the displacements of these nodes. To describe the unknown displacements at each point a polynomial interpolation function is used. The entire force applied to the structure is replaced by an equivalent system of forces applied to the nodes. [33] The result of the entire displacement of the structure is obtained by assembling the governing equation

$$\{F\} = [K]\{u\} \quad \text{,where}$$

$\{F\}$ = Nodal Load Vector

$[K]$ = Global Stiffness Matrix

$\{u\}$ = Nodal Displacements

3.2 Applications of FEM in Engineering

- Aerospace/Mechanical/Civil/Automobile Engineering
- Structural Analysis(Static/Dynamic/Linear/Non-Linear)
- Thermal/Fluid flows
- Nuclear Engineering
- Electromagnetic
- Biomechanics
- Geomechanics
- Biomedical Engineering
- Hydraulics
- Smart Structures

3.3 Engineering Analysis Discipline

- Structural analysis (Motion of solid bodies, pressure on solid bodies etc.,)
- Thermal Analysis
- Magnetic Analysis
- Electric Analysis
- Fluid Analysis (Motion of gases/fluids)
- Coupled-Field Analysis (Combination of any of the above)

3.4 Structural Analysis

To compute the deformations, internal forces and stress of a particular object, the structural analysis is used. In order to perform a structural analysis we should first determine the structural loads, geometry, support conditions and material properties. This type of analysis can be used to capture the static response of the structure.

Example: Computation of deformations, internal forces, stresses and strains.

The following are the areas in which structural analysis play a major role,

- Static Analysis – Under static loading conditions, determining the displacements and stresses.
- Modal Analysis – For determining the mode shapes and natural frequencies of a structure.
- Harmonic Analysis – Under time varying loads, determining the harmonic response of the structure.
- Transient Dynamic Analysis – Under random time varying loads, determining the response of the structure.
- Spectrum Analysis – Due to a response spectrum or a random vibration input, calculating the stresses and strain of the structure.

- Buckling Analysis – For calculating the buckling loads and determining the buckling load shape.

- Advance Structural Analysis – This examines the dynamic response, stability and non-linear behaviour of the structure.

Linear Static Analysis

In most of the analysis when assumptions like small deformation, perfectly elastic material and loads are assumed to be static, the analysis can be treated as a specific linear problem.

3.5 Thermal Analysis

In a thermal analysis we will be able to calculate the temperature gradients, heat transfer and thermal flux of an object. Three modes like conduction, convection and radiation analysis can be performed on the desired model. The thermal analysis can be performed in two areas:

- Steady State Thermal Analysis – Under static loading conditions they are used to determine the temperature gradient and other thermal quantities.

- Transient Thermal Analysis – Under time varying loading conditions, they are used to determine the temperature gradient and other thermal quantities.

3.6 Steps in Finite Element Method

There are several steps in order to complete an analysis by finite element method. These methods are in coincidence with the matrix method. The theoretical approach is given to each and every step below,

3.6.1 Discretization

Initially to start with, the problem has to be divided into several elements, connect with nodes. This process is called discretization. Each and every element and their corresponding node should be numbered so that matrix of connectivity can be set up. The figure in the bottom shows the discretization process of a frame into beam elements and discretization of a plane stress problem to quadrilateral elements.

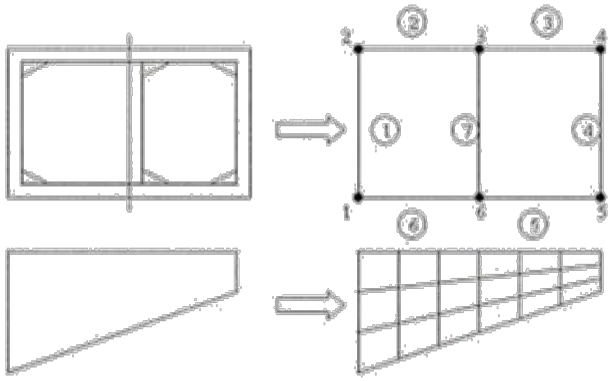


Figure 3.1 Discretization of Frame and Plane Stress Problems

The orders in which the nodes and elements are numbered are more important because it greatly affects the computation time. The reason is because we get a symmetrical, banded stiffness matrix, whose bandwidth is dependent on the difference in the node numbers for each element, and this bandwidth is in turn connected to the number of calculations that has to be done in the computer to solve the problem. Usually FEM programs perform an

internal numbering option to optimize this bandwidth to a minimum by renumbering these nodes if they are not optimal.

3.6.2 Element Analysis

To perform the element analysis there are two key components, one is expressing the displacements with in the elements and maintaining the equilibrium of the elements. Additionally the stress-strain relationship should be maintaining compatibility. The final result we obtain is the element stiffness relationship S=kv. These results could be obtained from the governing differential equation and boundary condition of the elements. For plane stress problems, the displacement within the elements are expressed as shape functions scaled by the node displacements. The displacement in an arbitrary point within the element is calculated by the nodal point displacement by assuming expression for shape functions. The section of the structure, which is made up of number of elements by which it is represented is kept by the stresses along the edges. Usually in finite element analysis it is easy to work with nodal point forces. The stress acting in the edge of the structure is replaced by the equivalent nodal point forces by making the element to be in an integrated equilibrium using work or energy considerations. This method of replacement is often called lump the edge forces to nodal forces. Thus the relationship between the nodal point displacements and forces are expressed as $S= kv + S^o$ where,

- S – Generalized nodal point forces
- K – Element stiffness matrix

- V – Nodal point displacements

- S^o – Nodal point forces for external loads

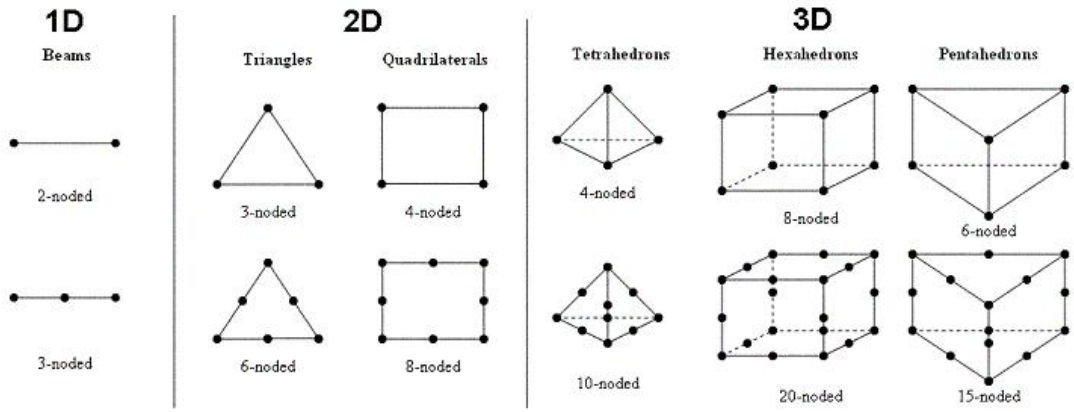


Figure 3.2 Different 1D, 2D and 3D Elements

3.6.3 System Analysis

A relationship between the load and nodal point displacements is established by demanding the equilibrium for all nodal points in the structure:

$$R = kr + R^o$$

By adding the contributions from the element stiffness matrices we can establish the global stiffness matrix. Similarly the load vector R is obtained from the known nodal forces.

3.6.4 Boundary Conditions

Boundary conditions are given to the structure by setting nodal displacements to known values of spring stiffness are added.

3.6.5 Finding Global Displacements

By solving the linear set of equations we can calculate the global displacements, $r = K^{-1}(R - R^0)$

3.6.6 Calculation of stresses

From Hooke's law, the stresses can be determined by the strains. Strains are in turn derived from the displacement functions within the element combined with Hooke's law. This can be expresses as,

$$\sigma (x, y, z) = D\, B(x, y, z)\, v$$

Where

$v = a\, r$

D - Hooke's law on matrix form

B - Derived from u(x, y, z)

Finally the post processors help users to sort the output and display it in the graphical form.

3.7 FEM Notation

Finite element method treats the continuous problem domain as a collection of individual finite elements. The problem parameters are defined at each node of the element. The commonly used definitions of the FEM notation are,

- Dimensionality: The elements can be defined differently depending on the problem context. Dimensionality indeed expresses whether the element has 1, 2 or 3 space dimensions.
- Nodal Points: Every element is described by its nodal points. Frequently the nodal points are chosen to be the corners of the element. However in case of nonlinear geometries nodal points are also defined on the edges.
- Geometry: This term is used to describe the domain on which finite element discretization needs to be applied. It can be smooth a regular (e.g. a rectangular plate), or complex (e.g. surface of a machine part). The geometry is defined by the placements of the nodal points.
- Degrees of Freedom: The degree of freedom is the number of ways in which the original problem domain can change its state. In the case of the continuous problem domain, the DOF is infinite, because problem characteristics can be defined in each point on the domain. In the discrete FEM domain, instead, the DOF is limited by the number elements, because problem characteristics can only be defined on the nodal points.
- Nodal Forces: A set of nodal forces (or any other actions depending on the problem) are defined on each nodal point. From the mathematical point of view this corresponds to the non-homogeneous right hand side of the governing DE.

3.8 Submodeling

In finite element analysis, the mesh developed in the element is too coarse to produce satisfactory results. Therefore a method called submodeling is introduced to generate finer meshes in the specific region of interest.

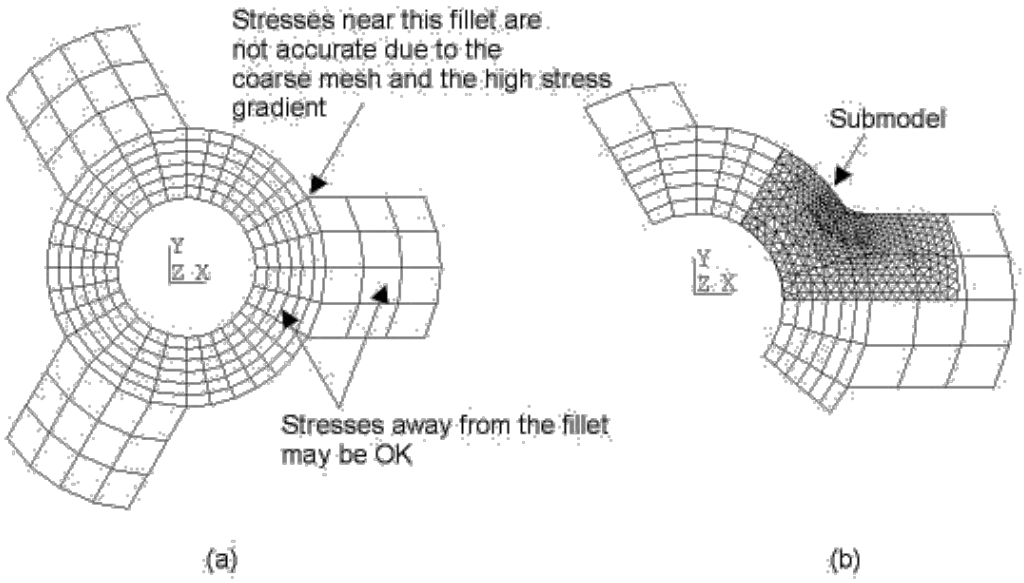


Figure 3.3 Sub Modeling of a Pulley Hub and Spokes: (a) Coarsely Meshed Model, and (b) Finely Meshed Sub Model

Sub modeling is commonly known as cut boundary displacement method or the specified boundary displacement method. The cut boundary is the boundary of the sub model which represents a cut through the coarse model. Displacements calculated on the cut boundary of the coarse model are specified as boundary conditions for the sub model.

Sub modeling is based on St. Venant's principle, which states that if an actual distribution of forces is replaced by a statically equivalent system, the

distribution of stress and strain is altered only near the regions of load application. The principle implies that stress concentration effects are localized around the concentration; therefore, if the boundaries of the sub model are far enough away from the stress concentration, reasonably accurate results can be calculated in the sub model.

The ANSYS program does not restrict sub modeling to structural (stress) analyses only. Sub modeling can be used effectively in other disciplines as well. For example, in a magnetic field analysis, you can use sub modeling to calculate more accurate magnetic forces in a region of interest.

Aside from the obvious benefit of giving you more accurate results in a region of your model, the sub modeling technique has other advantages:

- It reduces, or even eliminates, the need for complicated transition regions in solid finite element models.

- It enables you to experiment with different designs for the region of interest (different fillet radii, for example).

- It helps you in demonstrating the adequacy of mesh refinements.

Some restrictions for the use of sub modeling are:

- It is valid only for solid elements and shell elements.
- The principle behind sub modeling assumes that the cut boundaries are far enough away from the stress concentration region. You must verify that this assumption is adequately satisfied."

CHAPTER 4

FINITE ELEMENT MODELING AND METHODOLOGY

4.1 Modeling of Flip Chip Package

In this chapter Finite Element modeling and methodology which has been carried out to analyze the effect of chip package interaction on the overall reliability of the package, particularly on BEoL metal/di-electric stack, has been discussed in detail. The process being simulated in this study is the die-attach process (reflow). During the reflow process the silicon chip is attached to the substrate through solder bumps. This process requires melting and solidification of the solder and temperatures can reach as high as 230°C. As the assembly cools it starts to bend or warp due to CTE mismatch between the silicon chip and the organic substrate. This bending induces thermo-mechanical stresses in the whole structure. To capture this warpage and stress simulations are performed using commercially available code ANSYS WORKBENCH v14.5. Since the focus of this work is to capture the damage in the Cu/low-k stack of the BEoL, sub-modelling technique is leveraged to account for the huge scale difference between different components of the package. Metal/dielectric layers are in the order of nano-meters (nm) whereas; the rest of the components can have thicknesses in the order of several hundred microns (µm). In this study 3D finite element model was created for a flip chip package with 7 mm x 7 mm die size, 150 µm bump pitch, 16 mm x 16 mm substrate. Two levels of sub-models had to be used to capture the damage in BEoL region during the reflow process

[4]. The following assumptions have been made while performing this finite element analysis:

- All the parts in 3D package are assumed to be bonded to each other
- All components are considered linear elastic except for the solder bumps
- Anand's viscoplastic constitutive relation was used for the solder bumps (Sn-Pb and SAC)
- Volume Fraction lumping is considered to determine the mechanical properties of the metal/dielectric effective region in the global model and sub-model 1
- Isothermal temperature loading was imposed on the package (Reflow)
- All components are considered stress free at 200°C for Pb-free and 180°C for Sn-Pb bumps

4.2 Package components

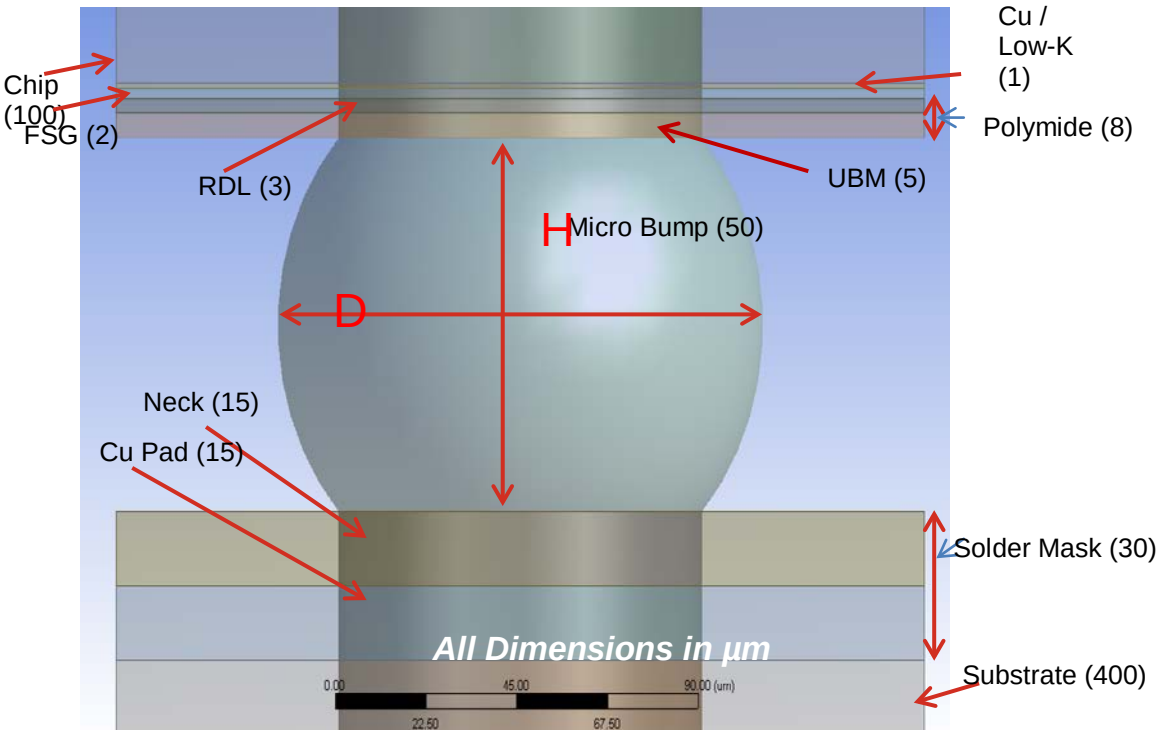


Figure 4.1 Package Components (Global)

A blown out view of the different components in a package is shown in figure 4.1. Functionality of a few of the layers in the BEoL is discussed below. Traditionally aluminum (Al) was used as the last metal layer for wire bond packages but in flip chip packages this Al layer can cause several problems. Aluminum readily oxidizes and forms a non-conductive aluminum oxide layer, due to this layer a good electrical connection is not possible. To overcome this issue a under bump metallization (UBM) layer was added. This layer adheres well with the al layer and at the same time provides good wettability for the solder during the reflow process. This UBM layer though easily deposited using the current deposition facilities available in Fabs, consists of different metal

layers. These include adhesion layer, diffusion barrier layer, solderable layer, and an oxidation barrier layer, which are being made of Titanium (Ti), Cooper (Cu) and Nickel (Ni) [28].

Redistributing IC bond pads before flip chip bumping is becoming increasingly common for lower cost, higher density, greater flexibility, and improved performance [29]. It were this redistribution layer that allowed industry to the peripheral wire bond pads to an area array for higher pitch solder bumps.

Fluorinated Silicate Glass (FSG) is the last dielectric layer but serves some very important functions. It overlays the bond pad to protect the doped silicon beneath form moisture and environmental effects. Thus, this layer is essential for improved reliability of the device [4].

4.3 Sub Modeling

At first the global model (the whole chip) was modelled to capture the global warpage and to identify the critical areas. To save computation time, without compromising the accuracy of the results, octant symmetry was taken as a representation of the whole package. Large deflection setting in ANSYS WORKBENCH was turned on because the deflection of the package may be more that 10% its thickness.

The thickness of the Cu/low-k layers on the BEoL region are in the order of ~100nm and the rest of the package dimensions are in the order of several hundred microns. This means that modelling the Cu/low-k layers in the global model is not feasible. To circumvent this hurdle the Cu/low-k stack is modelled

as a single block, whose properties have been determined using series lumping. Volume fraction method is used for calculating the effective properties of the *Cu/low-k* block and also for the metal and dielectric layers in the sub-model 2. The equations used are given below. [30]

Series Lumping (For Block in Global and Sub model 1)

$1/E = V_m/E_m + V_L/E_L$ - (i)

The mean of CTEs for metal and dielectric was taken as the effective CTE for the Cu/Low-k block

Parallel Lumping (For metal and dielectric layers in Sub Model 2)

$E=E_mV_m + E_LV_L$ - (ii)

$\alpha = (\alpha_mE_mV_m + \alpha_LE_LV_L)/ (E_mV_m + E_LV_L)$ - (iii)

where, ‘m’ refers to metal (Cu) and ‘L’ refers to low-k layer and ‘V’ is the volume fraction, ‘E’ refers to the Young’s Modulus, and ‘α’ refers to the CTE.

Far corner bump was found to be the critical bump following the analysis of the global model. To analyze this bump in greater detail and with higher accuracy, solder bump pitch was taken as a sub model and the displacements from the global model were transferred to the cut boundary faces, as can be seen in figure 4.5.

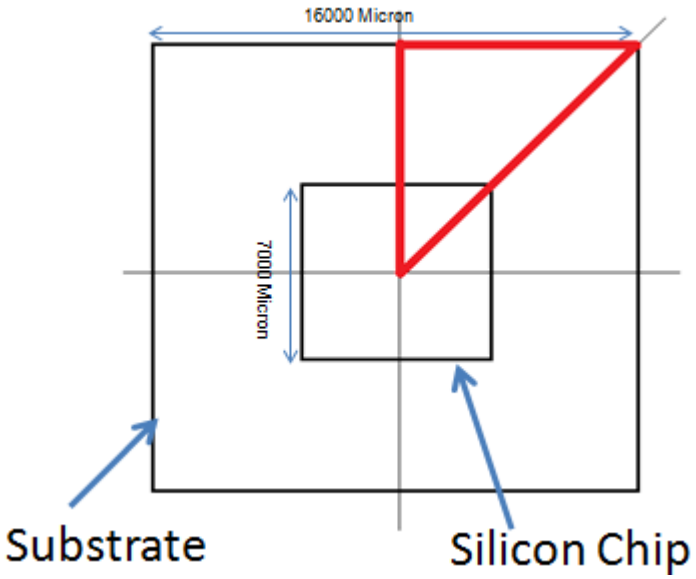


Figure 4.2 Octant Symmetry of Global Package.

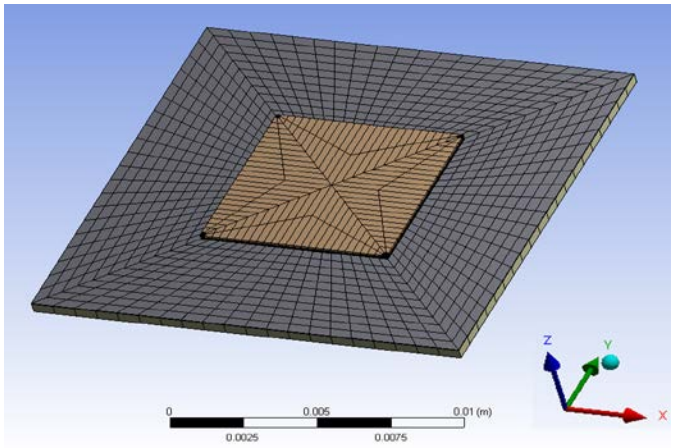


Figure 4.3 Global Model

The main focus of this work is the Cu/low-k stack, so from sub model 1 Cu/low-k stack was modelled as sub model 2 and as in the case of sub model 1, displacements from sub model 1 were transferred to cut boundary faces of

sub model 2 as shown in figure 4.6. The metal and di-electric layers in the BEoL are not pure Cu and low-k but have Cu vias and dielectric in various proportions. Since these vias have not been modelled effective properties have been determined for both metal and low-k layers using the parallel lumping method. See equations (ii) and (iii) above.

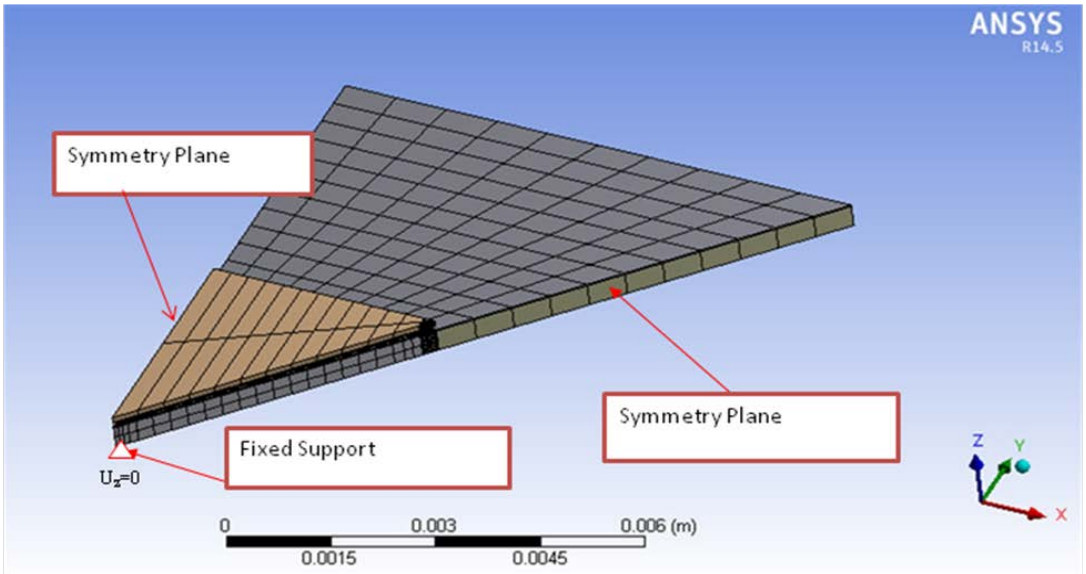


Figure 4.4 Octant Model with Boundary Conditions

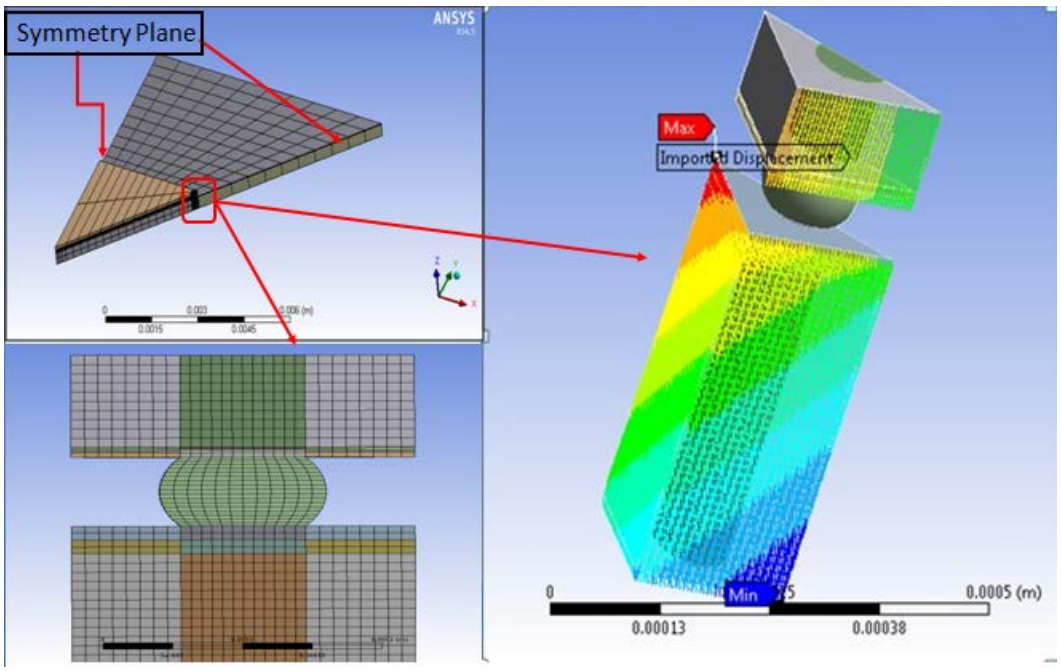


Figure 4.5 Sub model 1

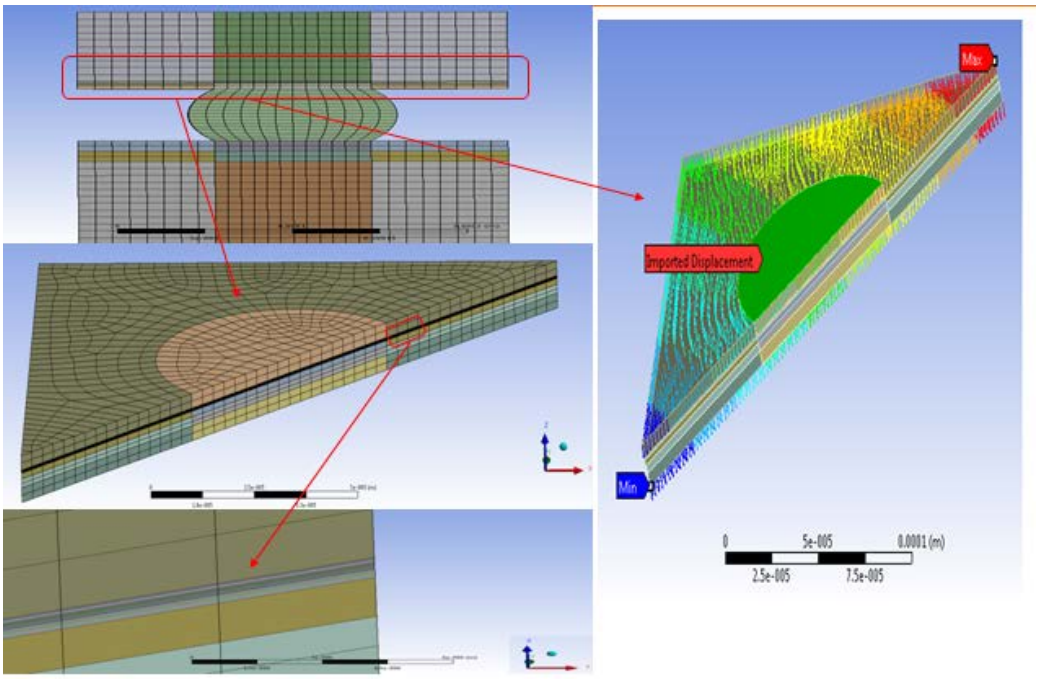


Figure 4.6 Sub Model 2 (Cu/low-k layers)

4.4 Meshing, Boundary Condition and Loading Condition

The global model was discretely meshed using different sizing options available in ANSYS Workbench v14.5. Foot print meshing was carried out to make sure that model has mesh continuity throughout the thickness of package in the far corner pitch as it is the critical region. Rest of the packages was meshed to achieve reasonable mesh continuity, because a high density mesh in rest of the package would significantly increase the computation time without affecting the end results. Mesh refinement was carried out in sub model 1 and sub model 2 to improve accuracy. Mesh sensitivity analysis was done to make sure that the results were independent if the mesh density [4].

Boundary conditions have been imposed as shown in figure 4.4. Two symmetry boundary conditions is applied to two symmetry boundary planes of the octant symmetry model. During the reflow process the assembly stays on a conveyer belt and there is no rigid body motion so to simulate this state of no motion the center of the package is constrained by restricting any motion in the z-direction (vertical). The model has been simulated to study the damage in BEoL/*f*BEoL regions during die attach reflow process of 200°C to room at 30°C per minute for Pb-free (SAC) alloy and from 180°C to room at 30°C per minute for Sn-Pb solder alloy [4].

4.5 Package Dimensions and Material Properties

Detailed geometry, package dimensions and material properties has been referred from the literature [10]. Detailed package dimensions are as shown in Table 4.1. Materials for all the parts of structure have been considered as linear elastic from literature [31, 32, 33] and shown in Table 4.2 except the solder bumps, which are taken as vicoplasic. Both the time and temperature dependent nonlinear properties are used for the solder to capture the creep and plastic behavior. Anand's constants for SAC 405 alloy [10] are shown in Table 4.3.

Table 4.1 Detailed Package Dimensions (mm)

Substrate	16 x 16 x 0.4
Solder Mask	16 x 16 x 0.03
Silicon	7 x 7 x 0.1
Polyimide	7 x 7 x 0.008
FSG	7 x 7 x 0.002
Cu/Low-k	7 x 7 x 0.001
Copper Pad Thickness	0.015
Neck (Height)	0.015
Micro Bump (diameter)	0.08
Micro Bump (height)	0.05
UBM (Thickness)	0.005
RDL (Thickness)	0.003
Micro Bump pitch	0.175

Table 4.2 Material Properties [31, 32, 33]

Material	**E (GPa)**	**Poisson's Ratio (υ)**	**CTE (/°C)**
Substrate	24.5	0.37	17e-6 (In Plane)
			52e-6 (Out of Plane)
Solder Mask	4	0.4	52e-6
Die	131	0.28	3e-6
Effective Cu/low-k block	21.3	0.34	21e-6
FSG	70	0.16	0.25e-6
Polymide	4	0.35	57e-6
Cu Pad	110	0.34	17e-6
UBM	120	0.32	14e-6
RDL	110	0.34	17e-6
Low-k Layer	13.2	0.3	25e-6
Cu Layer	56.2	0.3	18e-6

Table 4.3 Anand's Constants for SAC 405 Solder Alloy [10]

Variable	**Sn4Ag0.5Cu**
S_o (MPa)	20
Q/R (1/K)	10561
A (1/s)	325
A	10
M	0.32
h_o (MPa)	8.0E5
S^(MPa)	42.1
N	0.02
A	2.57

4.6 Design of Experiment

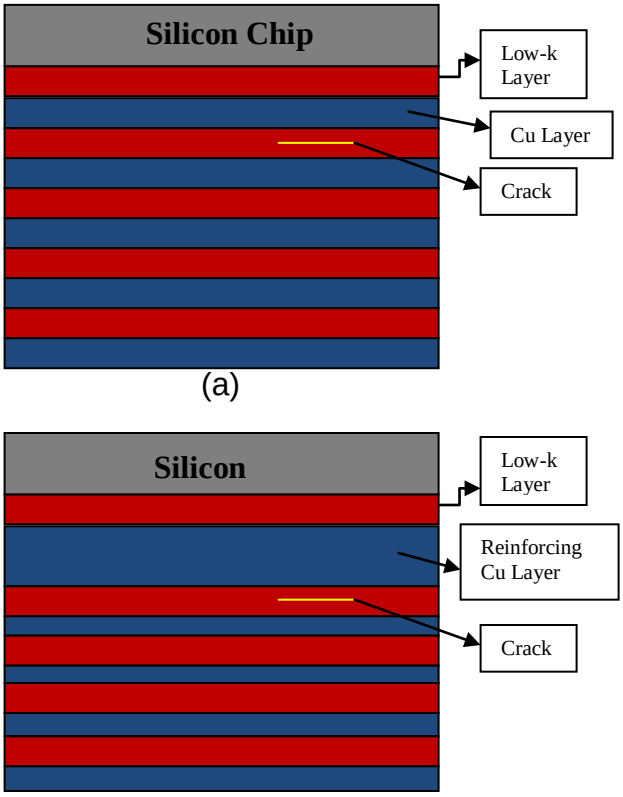


Figure 4.7 Cu/Low-k stack (a) Without Reinforcing Metal Layer; (b) with Reinforcing Metal Layer

A 3-D crack of length 2μm and depth 4μm is introduced in each of the five low k layers and the J-Integral value for the crack is computed and tabulated. The critical layer, i.e. for which the J-integral value is the largest, is identified. The Cu layer, adjacent to the critical dielectric layer, is doubled in thickness (from 100nm to 200nm), as shown in Figure 4.7. In order to keep the thickness of the metal/low-k stack constant, the thicknesses of the remaining metal layers were reduced from 100nm to 75nm. The thickness of the low-k

layers was unchanged. The cracks were again introduced into the low layers and the new J-integral values were computed in order to quantify the impact of reinforcement on the overall integrity of the Cu/low-k stack. I addition the J-integral for the critical layer is compared for the case when SAC is replaced with Sn-Pb solder to establish a baseline.

CHAPTER 5

RESULTS AND DISCUSSION

5.1 Background and Methodology

3-D Fracture analysis of the Back-End-Of-Line (BEoL) Cu/Low-k stack during the reflow process has been completed in ANSYS Workbench v14.5. The aim of this study was to identify the critical region in the Cu/low-k stack and to come up with a technique to mitigate the damage. Reflow process (die attach) process has been simulated and the thermo-mechanical response of the package. Since the focus of this analysis is the fracture damage in BEoL region, submodelling was leveraged to overcome the difference in dimensions of the Cu/low-k layers and rest of the package.

In sub model 2 the Cu/low-k stack was discretized into metal and dielectric layers and a crack was modelled in each of the low-k layers one at a time. The critical layer i.e. with the highest crack driving force was identified and the reinforced by thickening the adjacent metal layer. The effect of this reinforcement on the overall mechanical stability of the metal/dielectric stack was analyzed. Finally to establish a base line the J-integral in the critical layer was compared with the critical J-integral value for Sn-Pb solder. The results are discussed below.

5.2 Package Warpage

Figure 5.1 shows the warpage of the package. Although for simulation octant model was used, for clarity quarter model has been shown.

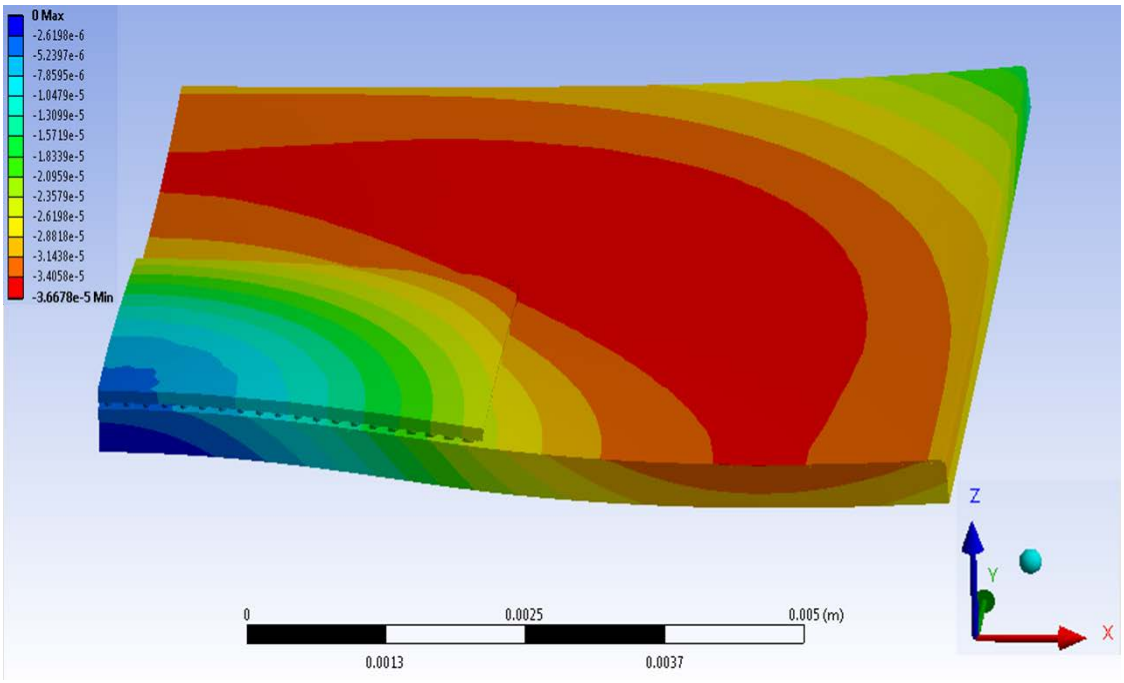


Figure 5.1 Warpage (Global)

As earlier the reason for bending is CTE mismatch between different materials used in the package. In the die shadow region bending is due to the CTE mismatch between silicon and the organic substrate, but as we beyond the shadow region, CTE mismatch between the substrate and the solder mask governs the bending. Thus, we see this wavy warpage profile.

5.3 Stress in *fBEoL and BEoL*

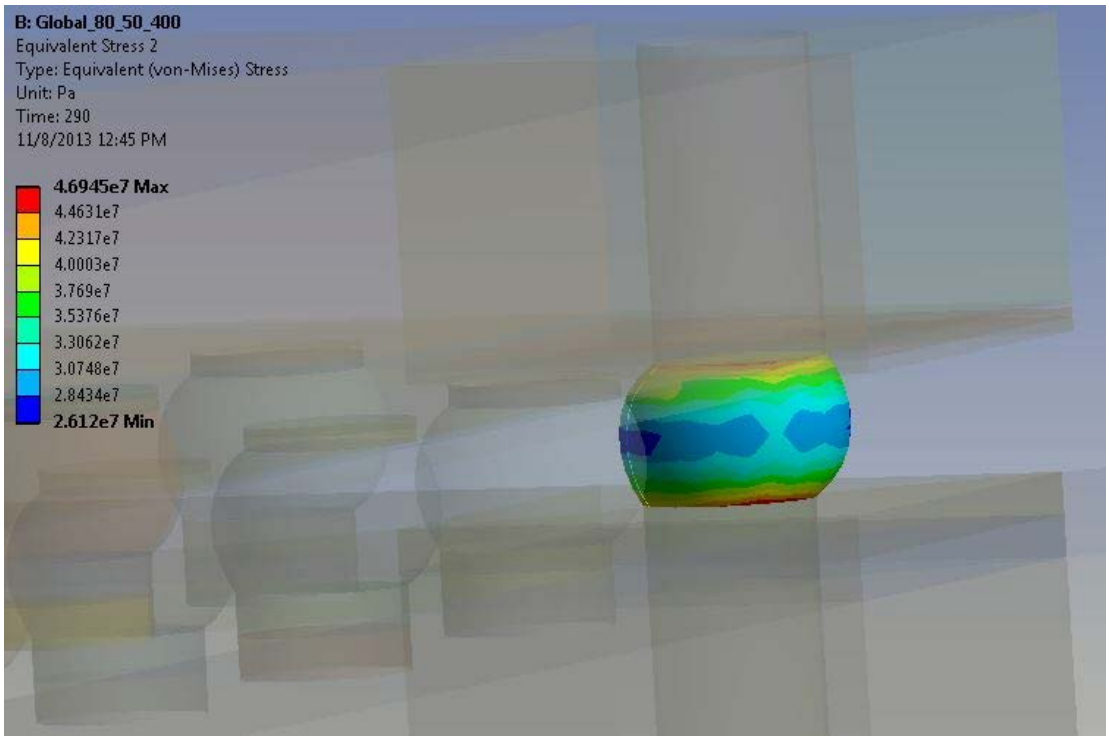


Figure 5.2 Stress in the Far Corner Bump

Figure 5.2 illustrates the stress profile and magnitude for the corner bump. This stress value was the highest so this was identified to be the critical bump and this pitch was taken as the sub model 1

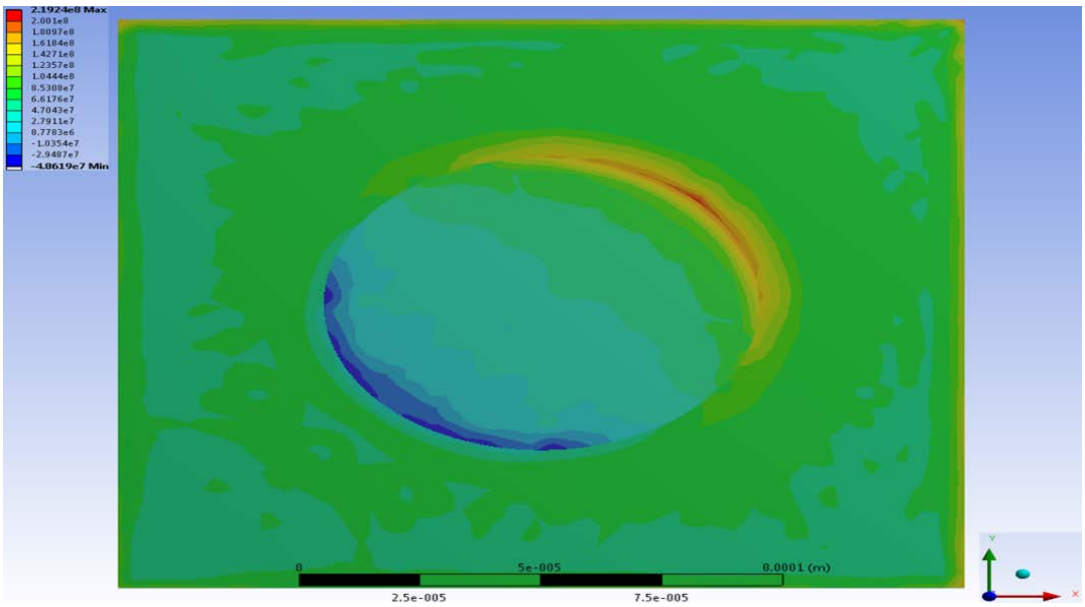


Figure 5.3 Peeling Stress in Cu/Low-k Stack

Figure 5.3 shows the principal stress (peeling stress) in the Cu/low-k stack (sub model 2). The maximum value of this stress is seen at the UBM footprint i.e. the region where the UBM meets the Cu/low-k stack.

5.4 Fracture analysis (Low-k Layers)-Before Reinforcement

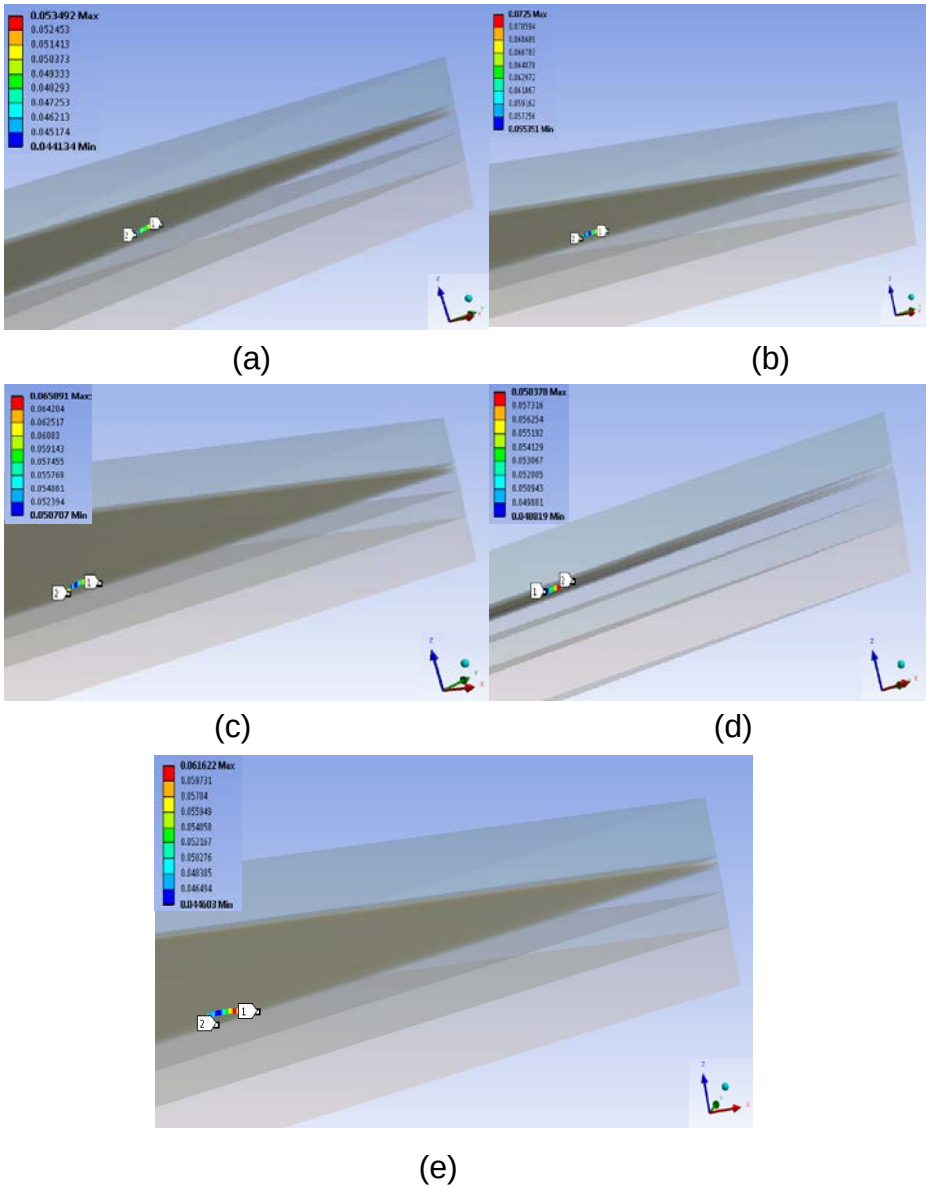


Figure 5.4. J-integral, (without reinforcement), for (a) Crack in the First/top Dielectric Layer- Crack 1; (b) Crack 2; (c) Crack 3; (d) Crack 4; (e) Crack 5

Figure 5.4 shows the J-integral value for all the cracks in each of the 5 layers when all the metal and dielectric layers are of the same thickness i.e. before reinforcement. Purpose of doing this was to identify the critical layer or the layer with the highest crack driving force. Since J-integral is a measure of the crack driving force so the layer with the highest J-integral value will be the critical layer. In this case 2nd layer from the chip side had the highest J-integral value, as shown in figure 5.5 below.

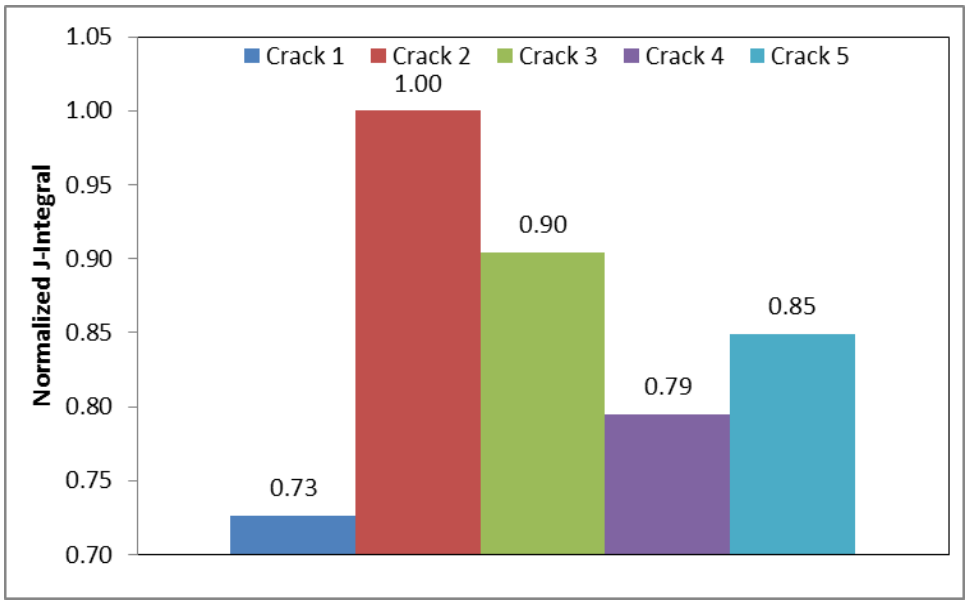
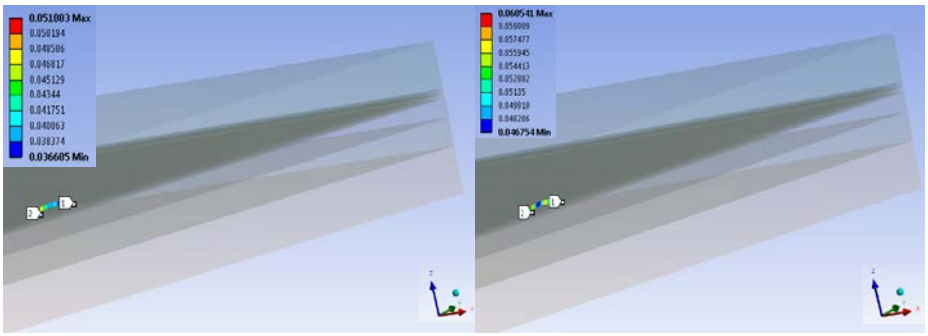


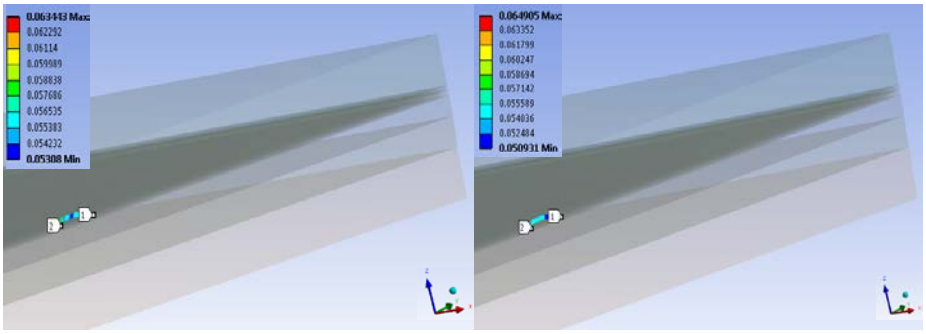
Figure 5.5 Normalized J-integral for all Five Low-k Layer Cracks

Figure 5.5 shows the normalized J-Integral value for all five cracks in low-k layers and the maximum value is observed for the second di-electric layer from the chip side.

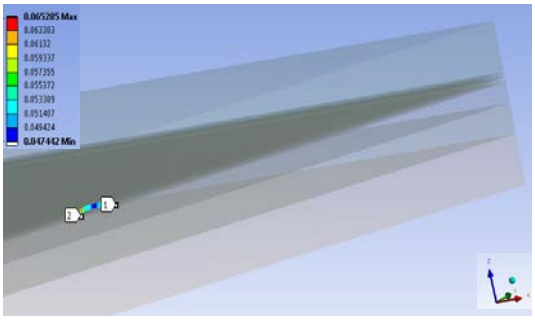
5.5 Fracture analysis (Low-k Layers)-After Reinforcement



(a) (b)



(c) (d)



(e)

Figure 5.6 J-integral, (with a reinforcing layer on top of the second low-k layer), for (a) Crack in the First/top Dielectric Layer- Crack 1; (b) Crack 2; (c) Crack 3; (d) Crack 4; (e) Crack 5

Figure 5.6 shows the J-integral value for all the cracks in each of the five low-k layers after the critical layer was reinforced by thickening the adjacent metal layer.

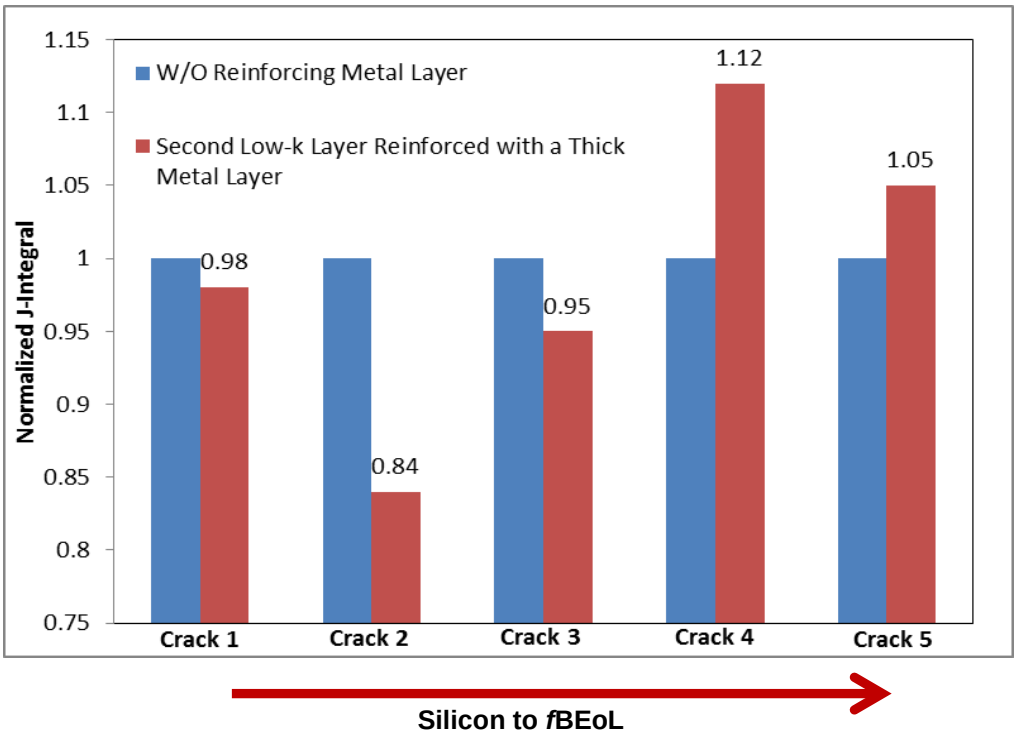


Figure 5.7 Effect of Reinforcing the Second Low-k Layer on J-integral

These new J-integral values were then compared with the corresponding values found when no reinforcing layer was present, as shown in figure 5.7. It is evident from figure above that there is a 2%, 16% and 5% decrease in the crack driving force (J-Integral) for the top three dielectric layers (from the silicon side). On the other hand, cracks in low-k layers 4 and 5 exhibit a 12% and 5% increase in the J-integral value, respectively. This increase is due to the fact that the thickness of the metal layer adjacent to every low-k layer, except the

second layer, has decreased. Thus, there is less reinforcement available and as we move away for the reinforcing metal layer, its reinforcing effect diminishes.

To gauge the feasibility of this reinforcement technique all the results were normalized against the maximum J-integral value, seen for the critical layer before reinforcement as shown in figure 5.8 below.

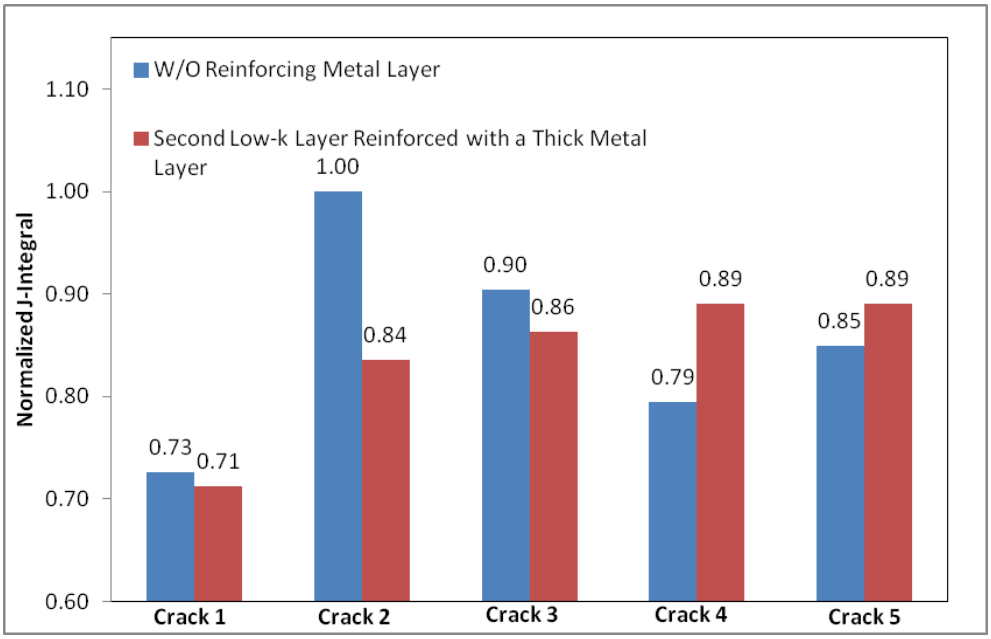


Figure 5.8 Normalized J-integral Comparisons

It is evident from figure 5.8 that although an increase in the crack driving force is observed for last two di-electric layers, the new higher J-integral values are still less than the critical value observed for the crack in the second dielectric layer with no reinforcement. Had this not been true then this technique would not have been feasible because instead of mitigating the di-electric

cracking issue we would have essentially just changed the critical failure location from one layer to another.

5.6 Comparison of Damage between *Pb-free* and *Sn-Pb* Solder Bumps

Up until them being banned in consumer electronics, Sn-Pb solder bumps were widely used in semiconductor industry. Even today medical and defense industry have not transitioned to lead free. So in order to establish a base line so as to get idea of the impact this transition, from Sn-Pb to lead free, had on the damage of BEoL region this study was done. This would also be helpful for the medical and military device industry because it would give them an idea of how transitioning to SAC (lead free) solder would affect their device reliability.

The same modelling methodology was followed for Sn-Pb solder as was for SAC 405 solder. The same reflow process was simulated only the reflow temperature was lowered from 200°C (for SAC 405) to 180°C, because the melting temperature for Sn-Pb 63/37 solder is slightly lower. In sub model 2 a crack in the second dielectric layer (critical layer) was modelled and the J-integral was computed. Similarly the layer was reinforced and the new J-integral value was computed. These results were then compared with the corresponding J-integral values for Pb-free solder. The results of these simulations are shown in figure 5.9 and 5.10 below.

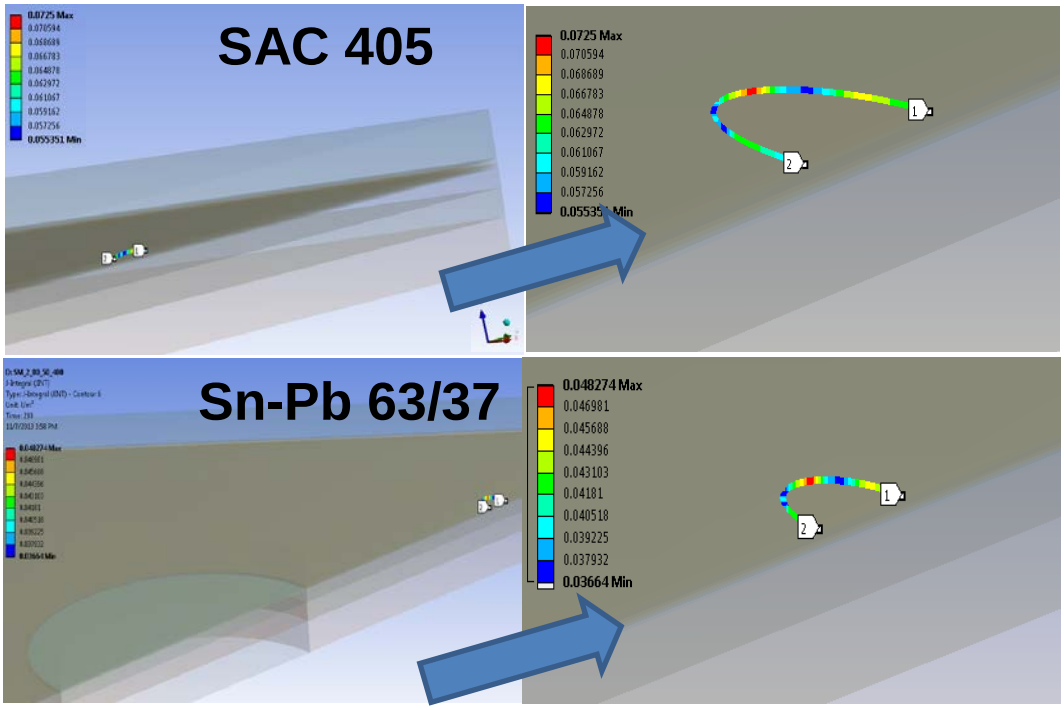


Figure 5.9 J-integral Comparison (Before reinforcement)

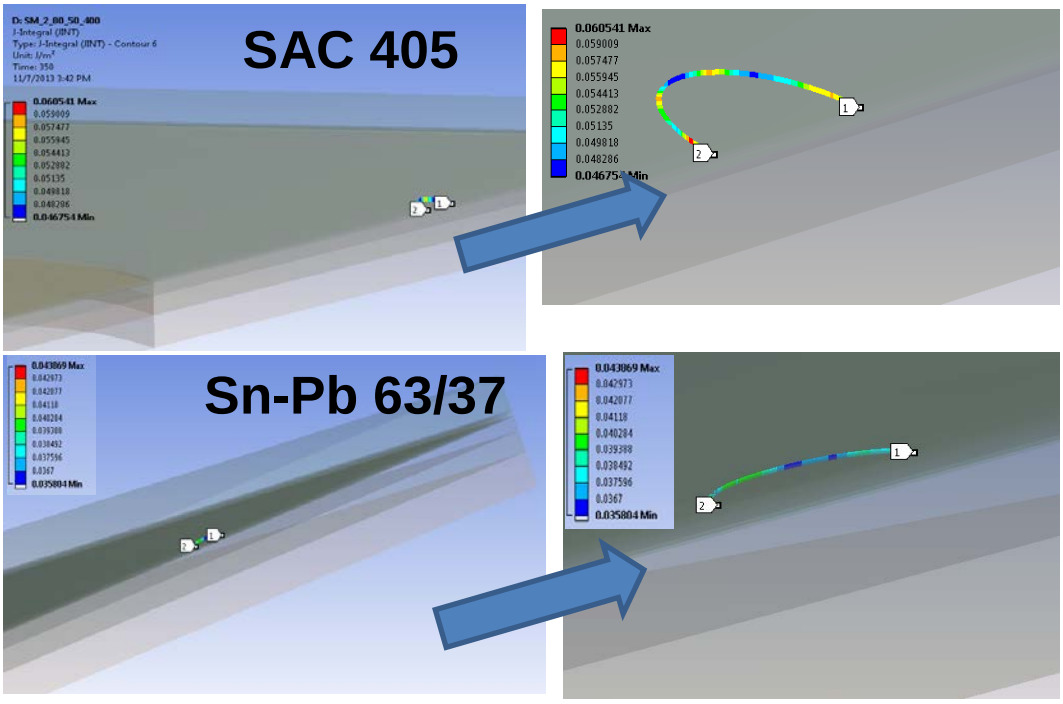


Figure 5.10 J-integral Comparison (After reinforcement)

The trend becomes more clear throgh figure 5.11 below.

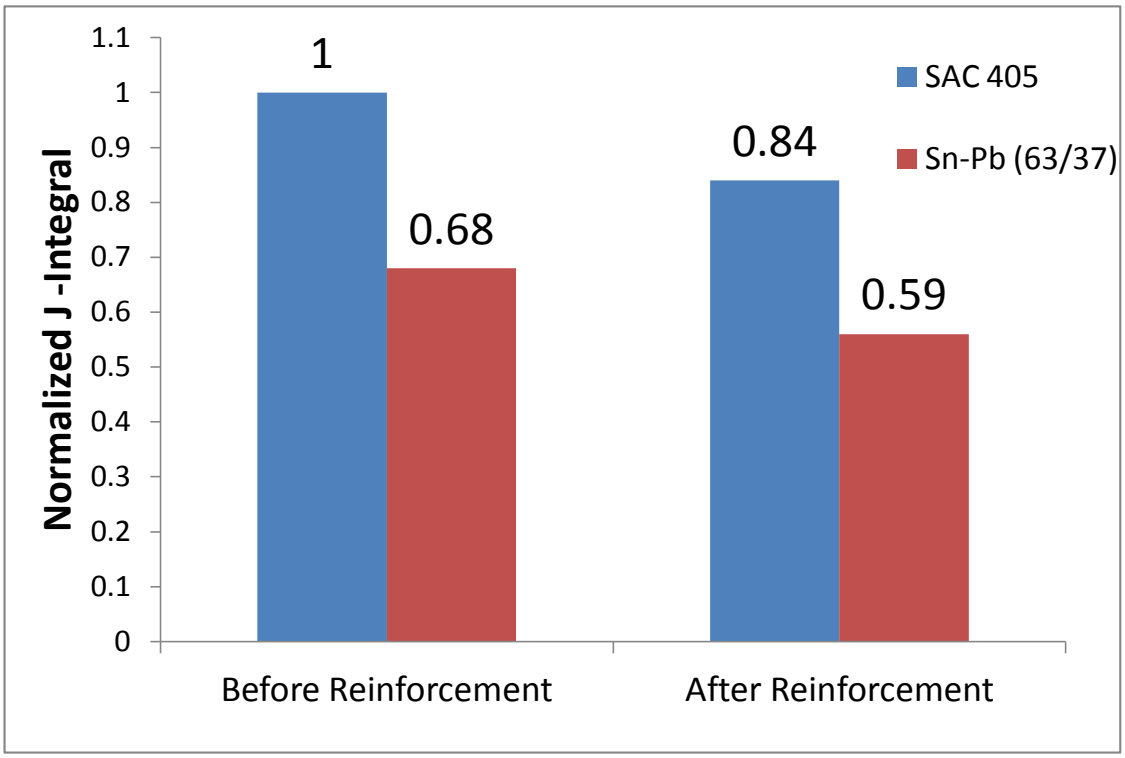


Figure 5.11 Comparison of SAC 405 with Sn-Pb 63/37 (Normalized J-integral)

Comparative study, figure 5.11, indicates that Sn-Pb solder shows about 30% less fracture damage than that of Pb-free. This can be accounted by the fact that reflow temperature for Sn-Pb solder is lower so lower stresses are generated due to CTE mismatch. Furthermore, Sn-Pb is more compliant than Pb-free and therefore, Sn-Pb solder transfers less stress to the BEoL region.

CHAPTER 6

CONCLUSION

6.1 Conclusion

A 3-D model for BEoL CPI risk mitigation has been formulated in ANSYS. Furthermore, the critical dielectric layer in the Cu/Low-k stack has been identified and a viable technique (reinforcement) to reduce the fracture damage has been demonstrated. Fracture damage in the Cu/Low-k stack has been reduced by this reiforcement of the critical dielectric layer without modifying the overall BEoL stack thickness or without changing the material. Therefore, reinforcing the critical layer is a cost effective method to overcome the dielectric crack issue.

Moreover,Comparative study indicates that Sn-Pb solder shows 30% less fracture damage than that of Pb-free. In addition, the baseline solder alloy (Sn-Pb 63/37) showed much higher mechanical stability than Pb-free, so BEoL fracture might not be an issue in Sn-Pb packages.

6.2 Future Work

As scaling of components continues, higher density interconnects and pitch < 130μm are needed and manufacturers are focusing on copper (Cu) pillars to achieve tighter pitches. [34]. Therefore, there is a need to investigate the effect of replacing solder bumps with Cu pillars on the fracture behavior of the BEoL dielectric.

This study has been carried out asssuming that low-k material behaves as linear elastic, which is not the case in actual situation. Therefore, non-linear properties can be extracted from molecular dynamics simulation and a feasibility study should be carried out by comparing the fracture damage between the cases when non-linearity is taken into account versus whenl linear properties for literature are used.

REFERENCES

1. Cluff, K.D., et. al. “Electronic Packaging Technologies” Mechanical Engineering Handbook Ed. Frank Kreith. Boca Raton: CRC Press LLC, 1999
2. Jonathan Luke Drake “THERMO-MECHANICAL RELIABILITY MODELS FOR LIFE PREDICTION OF BALL GRID ARRAYS ON CU-CORE PCBs IN EXTREME ENVIRONMENTS” Auburn University, 2007.
3. Lopez-Buedo, S., Boemo, E. “Electronics Packaging Technologies”.
4. H. Parekh, "MULTI-OBJECTIVE DESIGN OPTIMIZATION OF BEoL / fBEoL REGION DURING CHIP ATTACHMENT TO SUBSTRATE” University of Texas at Arlington, December 2013.
5. http://www.eleceng.adelaide.edu.au/personal/alsarawi/node10.html
6. Hocheol Kwak, Dr. Todd Hubing “ An overview of advanced electronic packaging technology” Technical Report: CVEL 007-001.
7. T. Raman, “ASSESSMENT OF THE MECHANICAL INTEGRITY OF CU/LOW-K DIELECTRIC IN A FLIP CHIP PACKAGE” University of Texas at Arlington, December 2012.
8. Zhang, X. “Chip package interaction (CPI) and its impact on reliability of flip-chip packages” The University of Texas, December 2009.
9. http://www.cemag.us/articles/2001/12/cu-integrated-low-k-dielectrics-future-now#.Uo6GiO1DuSp
10. Baig, Z., Mirza, F., Parekh, Hardik., Dereje, A. “3-D Fracture Analysis of the BEoL Region of a flip chip Package during Die Attach Process.” SMTA

International 2013

11. X.H. Liu, T.M. Shaw, G. Bonilla. “Mechanical Reliability Outlook of Ultra low-K Dielectrics” Advanced Metallization Conference, New York, 2010.
12. Lei L. Mercado., Shun-Meen Kuo.,Cindy Goldberg.,Darrel Frear., “Impact of flip-chip packaging on copper/low-k structures.” IEEE Transactions 2003
13. L.L Mercedo, S. Kuo, T. Lee, and S.K. Pozder, “Analysis of Flip chip packaging challenges on copper/Low-k interconnects”, IEEE Transactions on Device and Materials Reiliability, VOL. 3, NO.4, DEC 2003
14. Guotao Wang, Caroline Merrill, Jie Hua Zhao, Steven K. Groothius., Paul S Ho.,” Packaging effects on reliability of Cu/low-k interconnects ” IEEE Transactions 2003
15. K.M.Chen., “Ultra low-k die crack study for lead free solder bump flip-chip packaging.” J Marer Sci 2011
16. L. Fu, M. Su, F. Kuechenmeister, W. Huang, “Chip Package Interaction (CPI) Reliability of Cu/Low-k/Ultra-Low-k Interconnect” IEEE, 16th IPFA, China, 2009.
17. C.J. Uchibori, “Impact of Chip-Package Interaction on Reliability of Cu/Ultra Low-k Interconnects for 65nm Technology and Beyond” IEEE, 2006.
18. F.X. Che, X. Zhang, W.H Zhu, and T.C. Chai, “Reliability Evaluation for Copper/Low-k Structures Based on Experimental and Numerical Methods”, IEEE Transactions Sep 2008.
19. G.G. Harman, and C.E. Johnson, “Wire Bonding to Advanced Copper, Low-k Integrated Circuits, the Metal/Dielectrics Stacks, and Materials

Considerations”

20. O. Jimmy, “Structural Desgin and Optimization of 65nm Cu/low-k Flip chip package”, Thesis Defense, 2008.
21. C.Yuan, C.N. Han, M. Yew, C. Chou, and K. Chiang, “Design, Analysis, and Development of Novel Three-Dimesnional Stacking WLCSP”, IEEE Transactions of Advanced Packaging, Vol., 28, NO., 3, August 2005.
22. C. Kuo, M. Yip, and K. Chiang, “Time and Temperature-Dependent Mechanical Behavior of Underfill Materials in Electronic Packaging application”, Microelectronics Reliability 44 (2004) 627-638.
23. Y.S. Lai, T.H. Wang, “Verification of submodeling technique in thermo mechanical reliability assessment of flip-chip packaging assembly” Microelectronics Reliability, 2005.
24. C.J. Zhai, U. Ozkan, A. Dubey, Sidharth, R.C. Blish II, R.N.Master, “Investigation of Cu/Low-k Film Delamination in Flip Chip Packages” Electronics Components and Technology Conference, 2006.
25. X.H. Liu, T. M. Shaw., M. W. Lane., E.G. Liniger, B. W. Herbst, D. L. Questad, "Chip-Package-Interaction Modeling of Ultra Low-k/Copper Back End of Line" IITC, 2007
26. T.H. Wang, Y.S. Lai, “Submodeling Analysis for Path-Dependent Thermomechanical Problems” Journal of ELECTRONICS PACKAGING, 2005.
27. M. Lofrano, C.J. Wilson, K. Croes, B. Vandevelde, “Thermo-Mechanical Modeling of Stress- Induced-Voiding in BEOL Cu Interconnect Structures”

EuroSimE, 2009.

28. http://flipchips.com/tutorial/process/under-bump-metallization-ubm/

29. http://flipchips.com/tutorial/assembly/redistribution-layers/

30. Baig, Z., Parekh, Hardik., Mirza, F., Dereje, A. "A Finite Element Study to Evaluate the Feasibility of Solder Bump Depopulation Technique for BEoL-Cu/Low-K Damage Prediction" ESTC 2013

31. Ong Meng Guan, Jimmy “Structural Design and Optimization of 65nm Cu/Low-k Flip Chip Package” National University of Singapore, 2008.

32. Wang, G., Ho, P. “Packaging Effect on Reliability For Cu/Low-k Damascene Structures” University of Texas, Austin 2003.

33. Park, S., Izhar, A. “Shorter Field Life in Power Cycling of Organic Packages” Transaction of ASME, 2011.

34. www.i-micronews.com/upload/pdf/3DPackaging_May2013

BIOGRAPHICAL INFORMATION

Zaeem Baig completed his Bachelors of Science in Mechanical Engineering from University of Engineering and Technology, Lahore, Pakistan. He completed his Master of Science degree in Mechanical Engineering in December 2013. He was part of the Electronics, MEMS, Nano-electronics Systems Packaging (EMNSPC) research team from January 2013. His research primarily deals with the fracture analysis of BEoL interconnects. He has authored three conference papers related to electronic packaging.