RELIABILITY OF LEAD-FREE SOLDER UNDER CYCLIC BENDING

by

FAHAD ZAHEDI

Presented to the Faculty of the Graduate School of

The University of Texas at Arlington in Partial Fulfillment

of the Requirements

for the Degree of

MASTER OF SCIENCE IN MECHANICAL ENGINEERING

THE UNIVERSITY OF TEXAS AT ARLINGTON

May 2006

Copyright © by Fahad Zahedi 2006

All Rights Reserved

ACKNOWLEDGEMENTS

I would like to extend my heartfelt gratitude to the people who were part of this memorable portion of my life. First and foremost, my thesis advisor Professor Dereje Agonafer, who has been a constant source of inspiration to his students. His ability to motivate people and his vision of creating an institute to advance the study and research in the fields of electronic cooling and packaging at the University of Texas at Arlington has been the foundation on which all of this effort stands.

I would also like to thank Vishvam Puligandla who with his expertise and wit made all our sessions with him both informative and enjoyable. Most importantly I would like to thank Mohammed Hossain, who was a driving force in achieving the objectives of this project. His constant belligerence gave solutions to every problem and found a way out of every difficult situation. I am also very thankful to Murali Hanabe, Sridhar Canummala, Santosh Shetty and Steve Dunford of Nokia for all their input and the facilities they provided.

And finally none of this would have been possible without the prayers of my family to whom I remain eternally grateful

November 30, 2005

ABSTRACT

RELIABILITY OF LEAD-FREE SOLDER UNDER

CYCLIC BENDING

Publication No. _____

Fahad Zahedi, MS

The University of Texas at Arlington, 2006

Supervising Professor: Dereje Agonafer

To characterize particular compositions of lead free solder, four point cyclic bending test was conducted to study the affects of accelerated stress testing on the package to board interconnects. Nine CTBGA packages with 0.5 mm ball pitch and 12 x 12 mm package size were reflowed on 8 layered PWB's using solder balls with lead free composition alloys and different PWB copper pad finishes. The boards were subjected to test conditions based on proposed standards by JEDEC. Strain gages were mounted at different locations on the test boards as well as on bare boards in order to observe the difference caused in the board strain use this information for simulation

purposes. Failure analysis results have been presented as part of the work on the characterization of the various compositions of lead free alloys. This work reports and explains some of the observations found from the results of this test.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

CHAPTER 1

INTRODUCTION

1.1 Background and Motivation

Electronic devices have been a part of daily life for a considerable amount of time. From the workplace to the home and even in between, in all walks of life electronics have taken on roles that define the modern era. But this is not a new phenomenon at all, rather the logical development of trends started several years ago. One particular trend, that of miniaturization has achieved levels few had imagined. There is nothing new in the fact that electronic devices have been growing smaller and smaller, that is a trend that was foreseen and promoted by both manufacturers and marketers. What is certainly impressive is the scale at which this miniaturization has occurred and the continuing ability of designers and manufacturers to provide the same or more functionality on devices that shrink with every new version released. The major contributing factor here is the ability of manufacturers to take circuits designed in abstract space and cram them on top of silicon dies as small as say 40 mm^2. While these dies are growing smaller, the drive towards integration of different functioning blocks on to one single chip mean smaller feature sizes. This die and the package that surrounds it are the reason why electronic devices are now smaller and more portable than ever before.

In all of this development we cannot neglect the role of the PWB technology that has had to keep up with the shrinking device sizes. Printed wiring boards now come with High Density Interconnects (HDI). These are the conductor networks providing power and signal distribution in substrates.[Pecht et.al] Along with small packages this technology has taken the concept of small device size to a new level. Here lies a major portion of the work that goes into electronic device manufacturing. The circuit card assembly process takes packages from package manufacturers and assembles them on the PWB using solder material to form the connections between the packages and the boards. This is done by accurately placing the packages and other passive devices on the board and passing it through one or more cycles through reflow ovens. These re-flow ovens take the solder through a specific profile which allows them to melt and then re-solidify thus forming interconnects. These interconnects provide the electrical path between the actual chip and the outside world and any error in their functioning can lead to partial or complete failure of the device.

1.1.1 Impact of lead free solders

The reflow process described previously is not a simple operation. In fact it involves several parameters. As the reflow process is meant to melt the solder at a particular rate and then allow it to solidify by cooling it at a certain rate to obtain specific microstructure it is imperative that the solder material be well characterized. The importance of the material microstructure cannot be over emphasized. Improper reflow process can result in a material of different properties than those that are

expected. This can lead to flaws in the structure and affect the long term reliability of interconnects and by extension the whole device.

The reflow process and other manufacturing parameters are dependant on the material used as solder. The material of choice in this case was the Tin-Lead (Sn-Pb) eutectic alloy which had proved to be highly useful and convenient for the purpose of solder joint interconnects. However environmental research indicated that the presence of lead in the environment, even in small quantities could have severe effects. Lead is harmful in very small amounts (as are most heavy metals); once absorbed into the body lead combines with and inhibits the functioning of certain enzymes often with severe physiological or neurological consequences. Lead is an element hence it cannot be degraded or transformed into some other material, and it is extremely difficult to clean up after dispersal in the environment. The problem arises when old electronic devices are disposed using the usual solid waste management processes and ultimately end up in land fills. The acidity of the rain water washes the solder lead out from these crushed PCBs, which eventually ends up in the drinking water. Although electronic devices contain a very small amount of lead, the sheer number of devices being disposed off is a cause for concern since even 500 ppm of lead is considered to be hazardous. In order to prevent the spread of lead in the environment measures were taken to reduce the amount of lead being used in industries around the world. For example in January 2003 the parliament of the European Union passed a directive to restrict the use of lead and other heavy metals in electronic devices. The Directive on the Restriction of use of Hazardous Substances and the Waste Electrical and Electronic equipment directive outline the

policies of the EU and require that by 2006 all electronic devices in the EU markets must be lead free. Similarly in May 1998 the Japanese Government introduced legislation relating to recycling. Although lead was not specifically mentioned the implication was there. The industry has taken heed of "guidelines" from the Japanese EPA and the government suggesting reduced use of lead as part of the increased recycling, and many major companies have taken up the challenge and have announced measures and timescales to reduce and eliminate lead in the solder.

The impact of this legislation on the electronics industry has been massive. Many small and medium enterprises were not even aware of the requirements of the WEEE and RoHS and even major companies were forced to re-think their production processes. The reason for this as has been stated before was the immense dependence on the use of Sn-Pb solders and the knowledge data base that was associated with it. Replacing it with another material meant that this new material would have to be close to the original in terms of its mechanical and thermal properties so that there would be a minimum amount of restructuring required by manufacturers. As an alternative to Sn-Pb solder, researchers tried to use pure tin since it formed the major portion of the Sn-Pb alloy. But using tin had its own problems and did not prove to be the best alternative. Others tried to use tin zinc alloy but the study of this composition is still in progress and it is too early to make any comments on its usefulness. Much of the research was directed towards finding an appropriate composition of tin-silver-copper which was expected to give properties close to the original material. However, the actual composition of the Sn-Ag-Cu (SAC) alloy varies among manufacturers and to date

there are few compositions which are considered as benchmarks and no composition which can be considered to be standard.

1.1.2 Reliability testing of lead-free assemblies.

Apart from manufacturing concerns the other important area where lead free solders affect is yet unknown is in the reliability of lead free assemblies. Reliability testing is an integral part of the product development process and especially in the field of electronics reliability testing is a key factor in the success or failure of a new product. As we have mentioned before, the consumer expects electronic devices to get smaller and more portable without decreasing in functionality, and the manufacturers compete to fabricate smaller chips with smaller footprints to gain the advantage. While there seems to be no end to this trend it is a fact that factors that were previously non-issues are now important in the context of product life. For instance, low frequency vibrations that are common in cell phone buzzers are actually capable of affecting the solder joints within the phone over an extended period of time. Devices may be exposed to temperature extremes and portable devices will suffer handling damage and mechanical shocks.

The current reliability of products is such that they are more likely to be replaced by their owners well before the end of their useful life. For example the break even point of a common cell phone is approximately seven years, yet people change their cell phones for a newer model in just one or two years. This indicates a shift in the trend of consumer products, whereby the consumer is not looking for a long life from the product but rather short term reliability with a low cost. All this comes back to the

product design and development where the engineer is interested in the loads over a particular useful life and under a variety of conditions. Based on real life usage an electronic device can undergo one or more of several available tests such as

- Thermal cycling
- Power cycling
- Thermal shock
- Cyclic Bending
- Drop testing
- Vibration testing

Each of these tests is designed to simulate the same kind of stresses that the product would undergo in its useful life. For instance thermal cycling takes the test specimen through a series of temperature extremes in order to induce repeated thermal expansion and contraction in the specimen. This causes stresses which ultimately affect the solder joint interconnects causing failure. Similarly drop testing is meant to simulate the rapid vibrations caused by mechanical shock and drop. In real life situations the factors affecting the product work together and not alone, but it is necessary in these tests to isolate the effects of each one of these failure mechanisms. However, in recent times researchers have conducted combinations of these such as vibration testing coupled with thermal cycling, etc. In all cases, the results of these tests are specific to the particular material being tested and while the industry had a vast knowledge base for Sn-Pb solder there is still a lot of work required to determine the effect of lead free solder on the reliability of package to board interconnects. This task is further compounded by the variety of lead free compositions floating in the market since each one of them will have its own characteristics and effect on reliability.

1.2 Objectives and scope of the project

Introducing the problem thus far, we can now define the objectives and scope of this project. As we have mentioned one of the issues present with lead free solders is the variety of different compositions available including those that are provided by market vendors and those that are proprietary material compositions. In the scope of the larger project (of which this is one part) it is proposed to test at least four proprietary compositions for tensile, shear and creep testing. Since the cost of procuring test boards is prohibitively high, it is not possible for us to test all of the proposed compositions for reliability. Instead we choose to focus on one particular recommended composition which is of special interest to us. In order to characterize the material the scope of the larger project included three types of reliability tests namely thermal cycling, cyclic bending and drop testing. This report presents the details and results of the cyclic bend test. Since the actual material composition is proprietary to the sponsor it would be sufficient to state that it is a variant of SAC solder.

Another point of interest with regards to the reliability of the solder joints are the inter-metallics formed both within the solder and between the solder and the copper pads on the PWB. During the reflow process, when the solder metal melts the cooling rate is such that it re-solidifies to form particular microstructure. The melting solder combines with the copper on the PWB and this is necessary to form a strong joint.

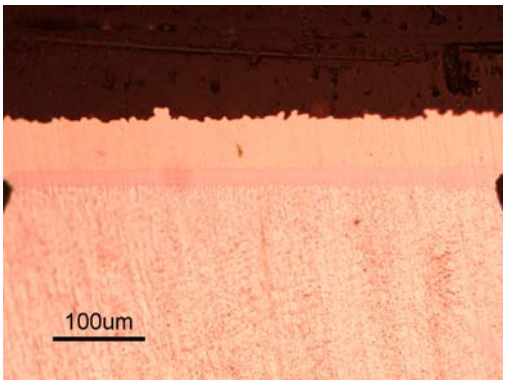

Figure 1.1 An example of the intermetallic layer formed between the copper pad and the solder material (package side)

However, the intermetallic layer is also the place where is the composition of the joint is not just that of the alloy. There may be two or three different kinds of intermetallics and this means that this layer is far from homogenous i.e. it is the place where we stresses can cause cracks to occur. The copper pads on the PWB are coated with a protective layer to ensure that they do not get corroded or spoilt in any other way. These protective coatings, also known as the Cu pad finishes also combine with the solder at the time of reflow and add to the mixture of intermetallics. One of the objectives of this study is to investigate the effect of different types of solder finish on the lead free intermetallics.

1.3 Literature Review

Research into the reliability of solder joint interconnects was underway by the late 90's and one of the primary references for this was done by S. Shetty, A Dasgupta et al who used a physics of failure approach to investigate the effects of quasi-static

bending loads on the reliability of chip scale package interconnects. This study used 0.5 mm ball pitch CSP's. While there were other studies which dealt with cyclic bending after this, each one of them used their own criteria for testing. This was pointed out in Darveaux's paper on the reliability of area array solder joints in bending. The table presented below illustrates this fact clearly.

Table 1.1 A survey of cyclic bend test specifications

Configuration	Support span mm	Control Method	Control limit range	Cyclic frequency	Ramp time (sec)	Dwell time (sec)	Sample size	Passing requirement	Ref
3-pt 63 units up double sided	250	deflection	1 to 25 mm	?	?	?	?	?	[2]
3-pt planar 1 unit up single sided	12 radius	load	30 N	1	0.5	0	?	300,000 cycles	[3]
3-pt planar 1 unit up single sided	22 radius	deflection	0.25 to 1.0 mm	1	0.5	0	?	?	[4]
3-pt 1 unit up single sided	100	deflection	2 or 3 mm	1	0.015	0.485	5	?	[5]
3-pt 2 unit up single sided	?	deflection	3 or 4%	0.14 to 0.25	?	2 to 3	5 to 12	?	[6]
3-pt 1 unit up single side	90	deflection	1 mm	0.5	1	0	?	10,000	[3]

Table 1.1- continued

3-pt 1 unit up single sided	90	deflection	2 mm	0.09	0.5	5	5	1,000	[3]
3-pt 1 unit up single sided	90	deflection	0.2 mm	1	0.5	0	5	10,000	[3]
3-pt 1 unit up single sided	100	deflection	2 or 3 mm	1	0.5	0	5	none	[3]
4-pt 15 units up single sided	150 inner 200 outer	deflection	5 mm	1	0.5	0	15	none	[3]

Darveaux's paper is of seminal importance and a major reference point for the current work. Data from Darveaux's work has also been used by A Syed in his paper on Predicting Solder Joint Reliability for Thermal, Power and Bend cycle within 25% Accuracy. Although the paper focuses on failure prediction models primarily for thermal cycling and extending to power and bend cycles it is useful for anyone attempting to develop failure models for lead free solder. Another paper by Mercado et al also presents the correlation between use conditions and reliability testing for the case of four-point bending, but work for this paper uses eutectic tin lead solder. All in all, the work done for lead free solder is confined to bulk material properties and since there are variations in the composition of the different lead free solders, it is hoped that the current work will be a useful contribution.

CHAPTER 2

TEST SETUP AND PROCEDURE

2.1 Test Specimen Details

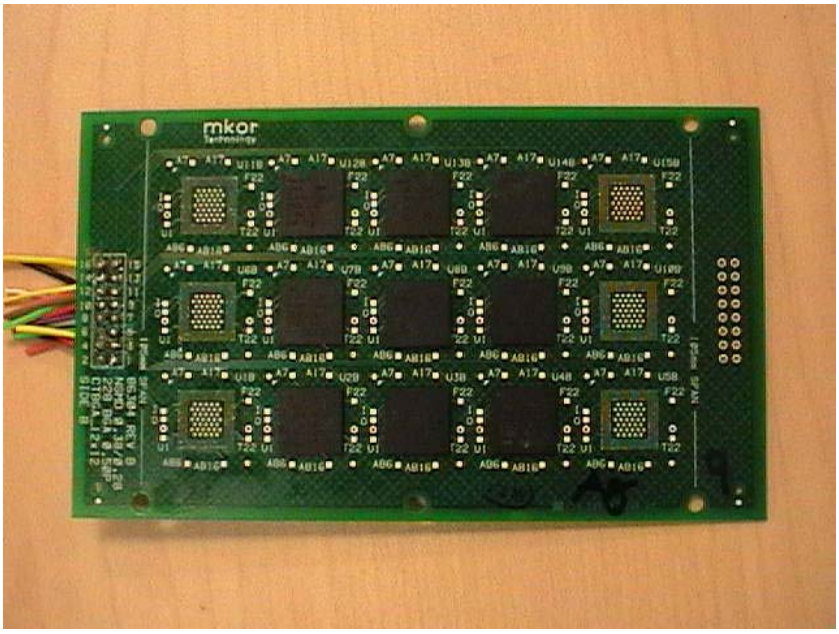

Figure 2.1 Example of test board as proposed by upcoming JEDEC standards

The test specimen for this study is an 8 layer PWB 132 mm x 77 mm populated on one side with 9 packages. The packages are 12x12 mm CTBGA with 8x8 mm dies size and 0.5 mm ball pitch. Each package has an arrangement of 22 x 22 ball array with 14 x 14 array depopulation in the center –i.e. a total of 288 balls per package. The packages are arranged in a 3x3 array with the middle column and middle row of

packages being centrally located. The package to board interconnects were made from a proprietary composition of SAC solder material. All boards used the same solder but there were three different types of surface finishes used on the copper pad of the PWB. The three surface finishes used were Immersion gold (Au), Immersion silver (Ag) and Organic Solderability Preservative (OSP). Overall surface finish of the boards was satisfactory although some boards were found to have bridges between the solder joints. All defective boards were removed and the final sample size for the boards was three boards with Au surface finish on pads, three boards with Ag pad finish and two boards for OSP type finish.

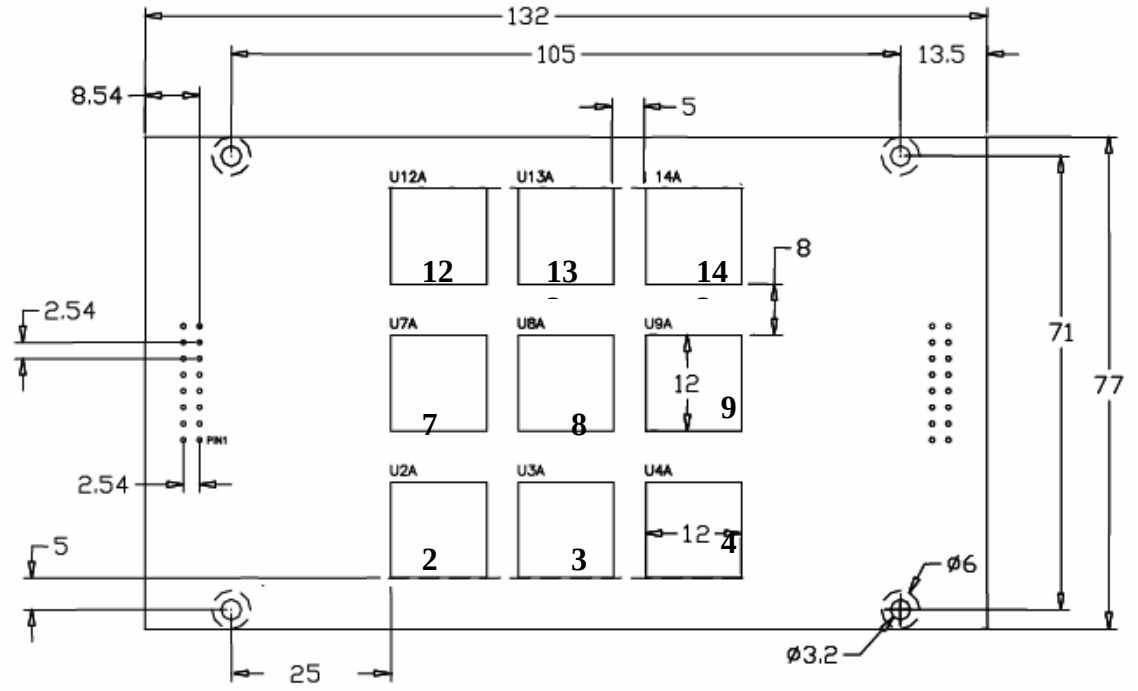

Figure 2.2 Board dimensions and specifications

2.2 Strain Gages

Strain gages were used in order to determine the actual strain (ε_{xx}) experienced at different locations on the board. Curvatures can be estimated as the product of the measured strains and half the thickness of the board at the point where the strain gage is located. EA-13-120LZ-120 type general purpose strain gages were placed at locations close to the corner balls of packages using M-Bond 200 adhesive. Previous work has shown that in the case of Pb-Sn solder and from general intuition it would be likely that the corner balls are subjected to more stress than the middle balls. Also the strain was monitored at different sections of the board in order to get a complete distribution of the strains. The data from the strain gages is also useful in order to validate simulations for failure life prediction. The figure below shows the arrangement for one side of the test board.

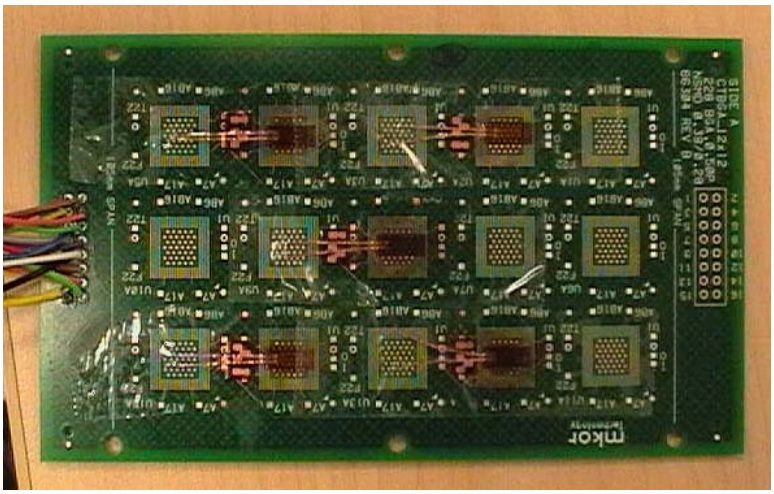

Figure 2.3 Example of strain gages applied to the lower side of the board

Strain gages were also mounted on an un-populated board in order to compare with the results of the test board. The gages mounted on the populated board followed two configurations. The first configuration allows for monitoring the strains close to the sites of expected failures. This was done on the side with the packages. The second configuration was on the side without packages. This configuration allows for monitoring the strains at the center of the packages although it is on the other side of the board. The strain gage arrangement for the bare board is the same as the second configuration.

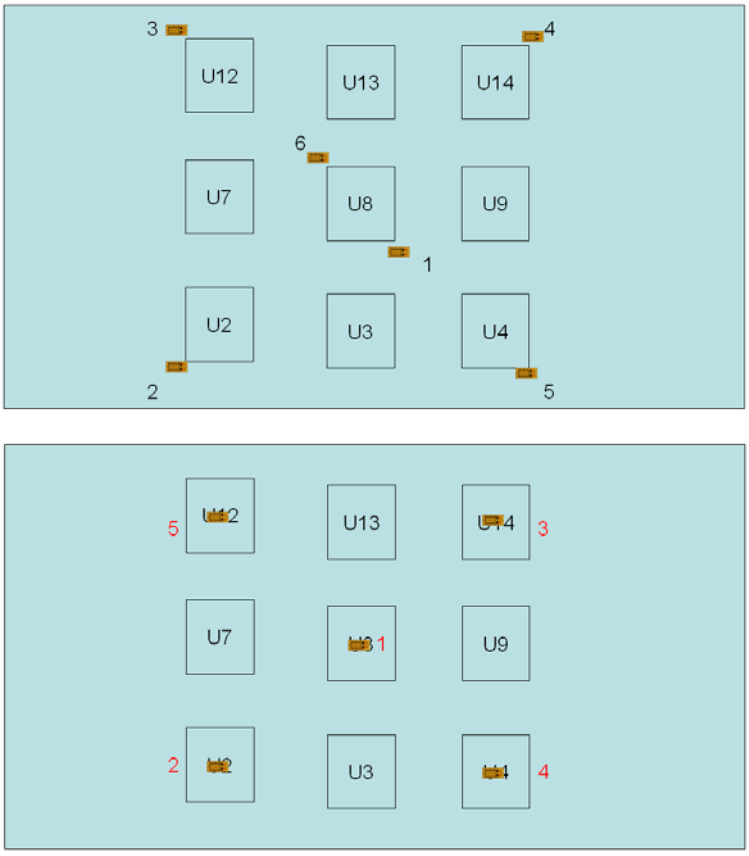

Figure 2.4 Strain gage arrangement: Configuration 1 (above) is for the populated side and configuration 2 (below) is for the empty side and for bare board

2.3 Test Procedure

The proposed standards prepared by JEDEC were used as the guidelines for the test procedure. The test was conducted on an Instron Universal Testing machine operating on a servo-hydraulic system with a load cell range of ±10 to ±25 kN. The test boards were connected to the data acquisition system and the failure monitoring equipment and placed such that the packages were facing towards the bottom i.e. the joints were subjected to expansion rather than compression. As pointed out in the work by Shetty, Dasgupta et al packages experiencing compressive stresses take longer to develop failures as compared to packages subjected to expansions.

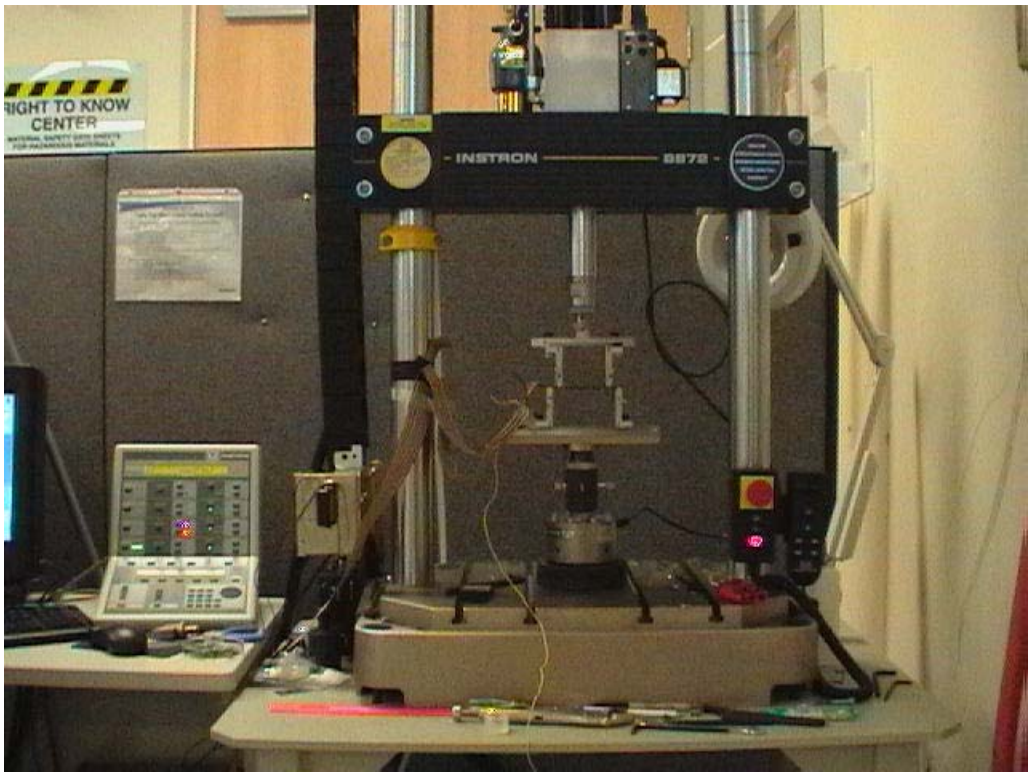

Figure 2.5 Test Apparatus

Two pairs of anvil supports were used to for the test. The lower pair of supports were spaced 200 mm apart with the board resting on them and the upper pair of supports were spaced 150 mm apart from each other and used to apply the load which is the usual four point bend test procedure. The relative merits of three point and four point bending are discussed in Appendix B.

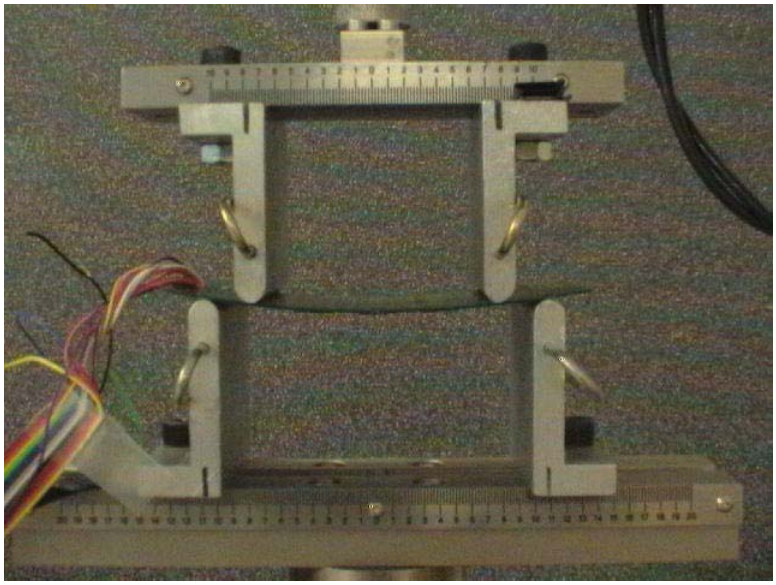

Figure 2.6 Detailed view of the four point bend fixture

Since the board was simply supported it was necessary to apply a pre-load in order to subject the test specimen to a cyclic load. Thus at the start of a cycle the board was in a slightly stressed condition and as the actuator moved down the deflection increased until it reached the maximum point. Also pre-loading ensured that the board did not jump when the actuator was coming upwards and the board was in a no-load condition.

The board was subjected to cyclic loading using a sinusoidal wave pattern with a frequency of 1 Hz and a vertical displacement of 2 mm.

2.4 Failure detection

The data acquisition system made by Analysis Tech™ was used to monitor failures. The solder joints of each package have an electrical continuity maintained by a daisy chain. This design is particularly made for testing inter-connect failures since it passes through each joint and if even one of the joints fail the continuity for that package will break. The ANATech event detector when connected to this daisy chain sends signals at regular intervals and records the feed back it receives. If the active signal does not return it implies that the joint has either failed due to an open or the resistance recorded is significantly high which indicates that there is a partially developed open somewhere in the chain. The test boards were checked for electrical continuity before the test and it was found that the normal resistance for a package was around 2 Ohms. The user can specify a value for resistance beyond which the event detector would register a failure even if the resistance was not infinite. For this test, the resistance threshold was set to 200 Ohms for the duration of 200 nanoseconds which would register as an event by the system. Each board was to be subjected to 100,000 cycles or tested until all packages failed. However, in actual event no board reached a 100,000 cycles and so the principle was not fully implemented.

CHAPTER 3

RESULTS AND ANALYSIS

This section covers the results obtained from the ANATech event detector and the readings obtained from the strain gage data acquisition system. The section concludes with the failure analysis of some of the packages and the results found therein.

3.1 Interconnect Failure Results

As mentioned before the ANATech event detector system was set to check for events. The event detector would send signals repeatedly through the board circuitry for 8 seconds and this counted as one cycle for the event detector. However the actual test cycles were operating at 1 Hz which meant that there was a numerical difference between the number of cycles of the actuator and the number of cycles of the event detector. In any case the actual number of cycles could be observed from the machine control system and this would be eight times the number of cycles registered by the event detector. The results below are plotted with reference to the location of the packages on the boards. The package on the lower left corner is assigned the number 2 instead of 1. This is because the numbering takes into account the 5 x 3 array of standard JEDEC boards, from which the left most and the right most rows are depopulated.

3.1.1 Results of Boards with Au type Finish

Table 3.1 shows the number of cycles to failure for the different boards. In the case of the three Au type boards the first failures recorded were at 9024, 11712 and 5832 cycles. In on case a package did not fail even after beyond 72000 cycles, but for the other two cases all the packages failed within 30,000 cycles.

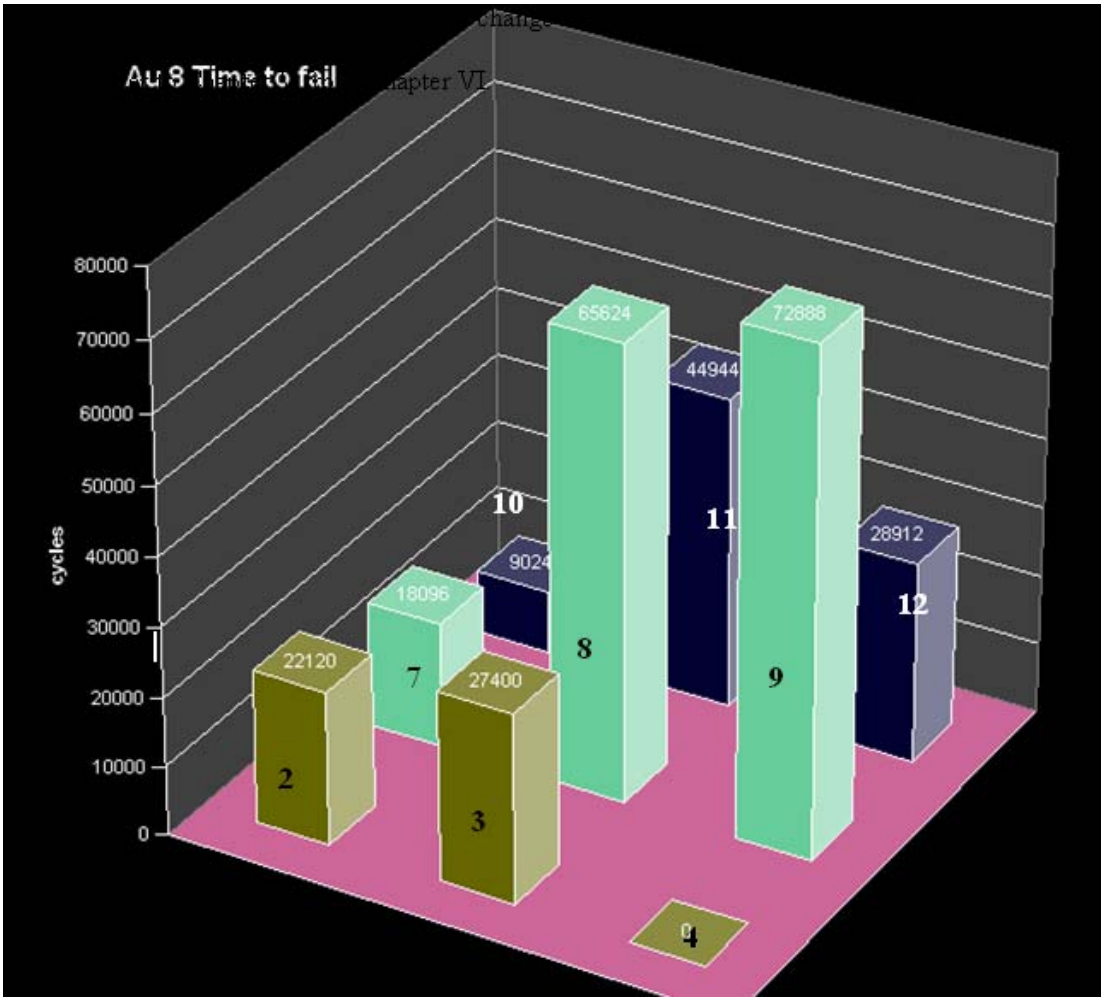

Figure 3.1 Number of cycles to fail and failure distribution of packages for Au 8

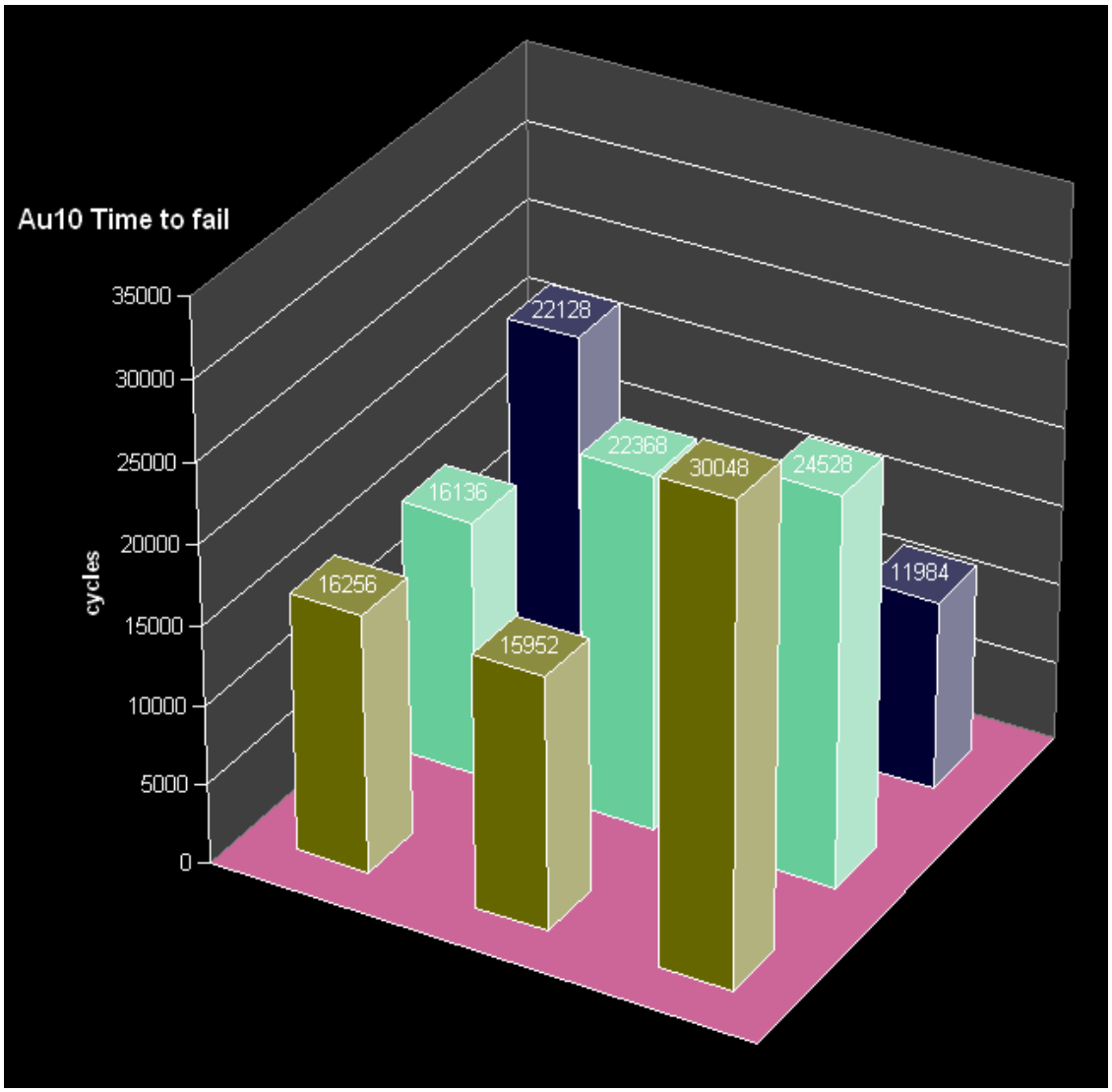

Figure 3.2 Number of cycles to fail and failure distribution of packages for Au 10

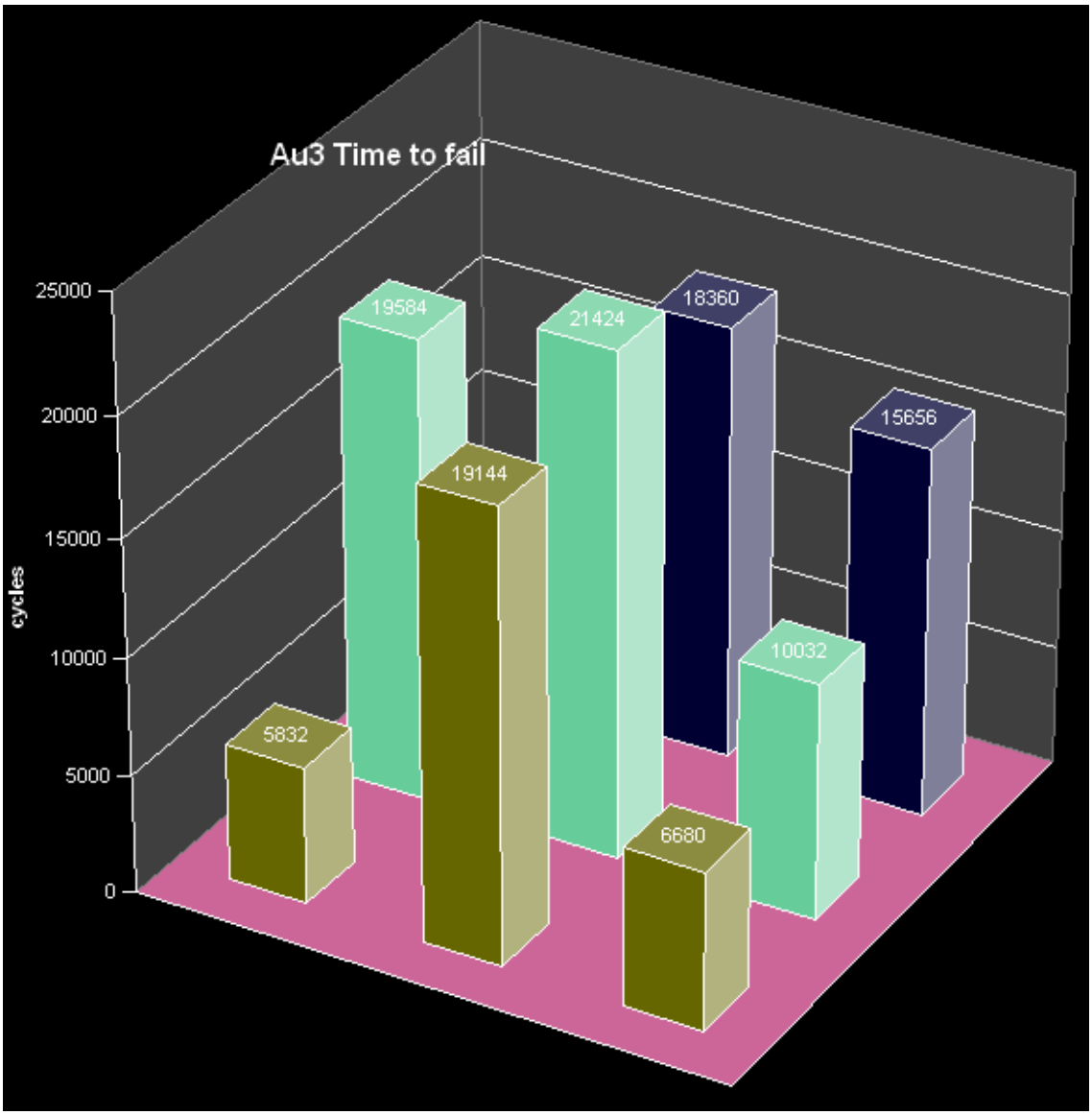

Figure 3.3 Number of cycles to fail and failure distribution of packages for Au 3

3.1.2 Results of Boards with Ag type Finish

In the case of the silver finish boards, the initial failures for all three boards were within 2000 cycles but more importantly in each case most of the packages failed within 6000 cycles. In the plot below the three packages marked with an ‘o’ indicate no failure, but this is because they were not taken all the way to failure in view of the poor performance of the other packages.

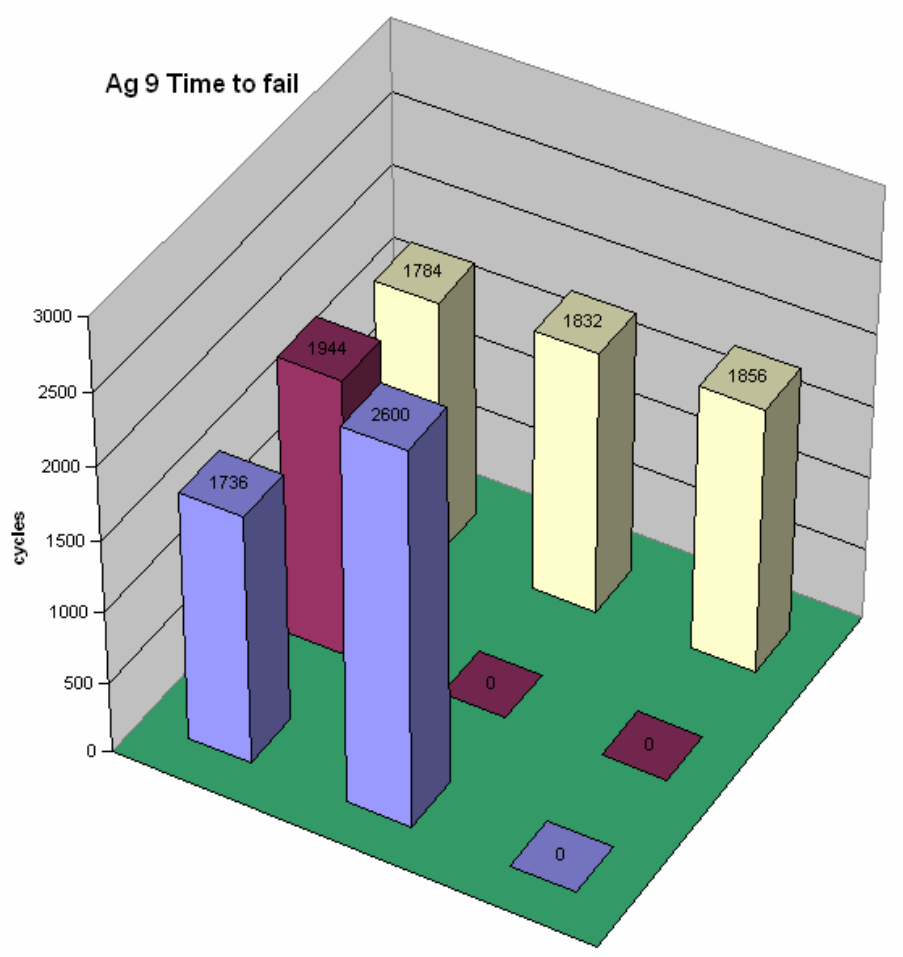

Figure 3.4 Number of cycles to fail and failure distribution of packages for Ag 9

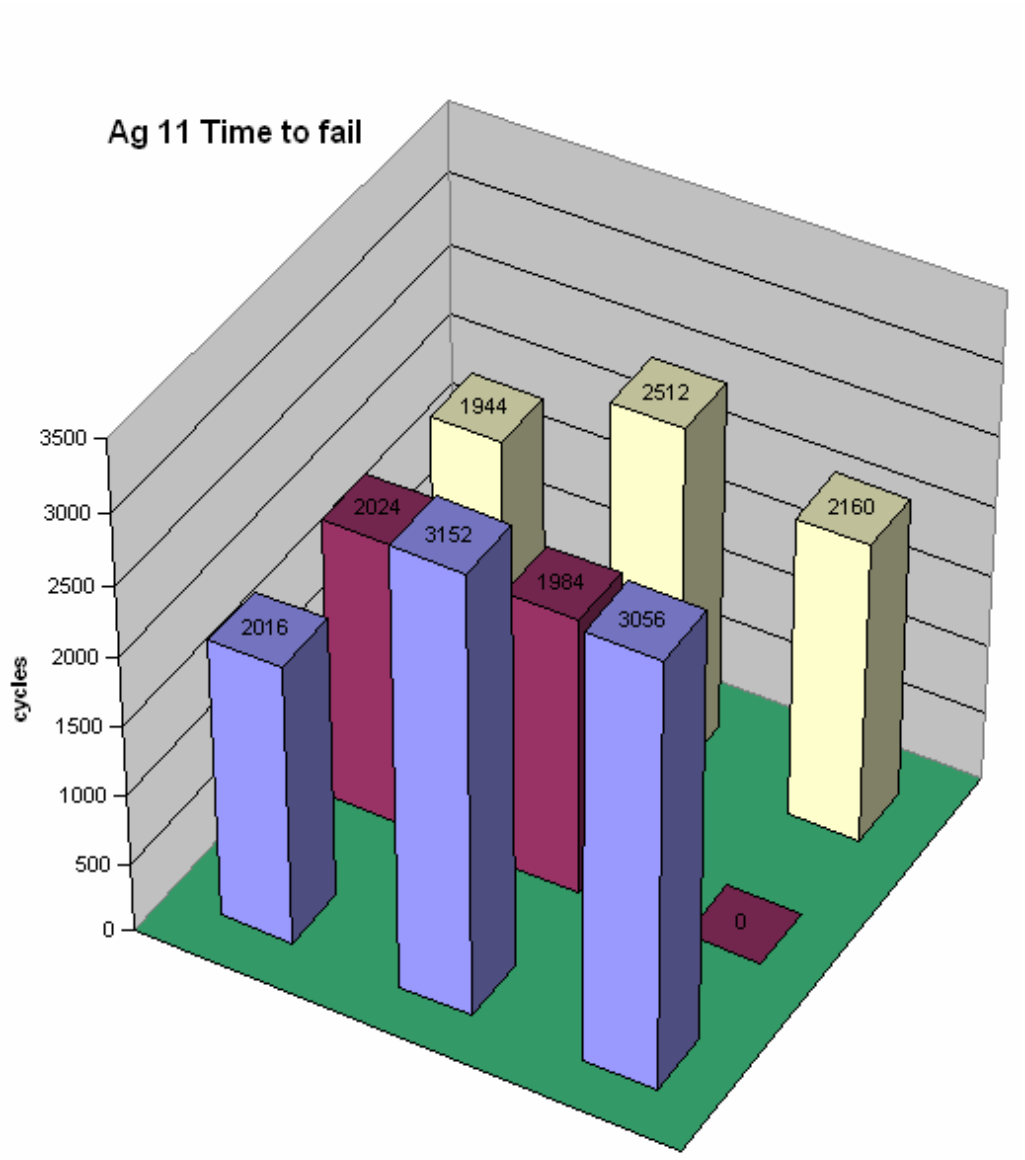

Figure 3.5 Number of cycles to fail and failure distribution of packages for Ag 11

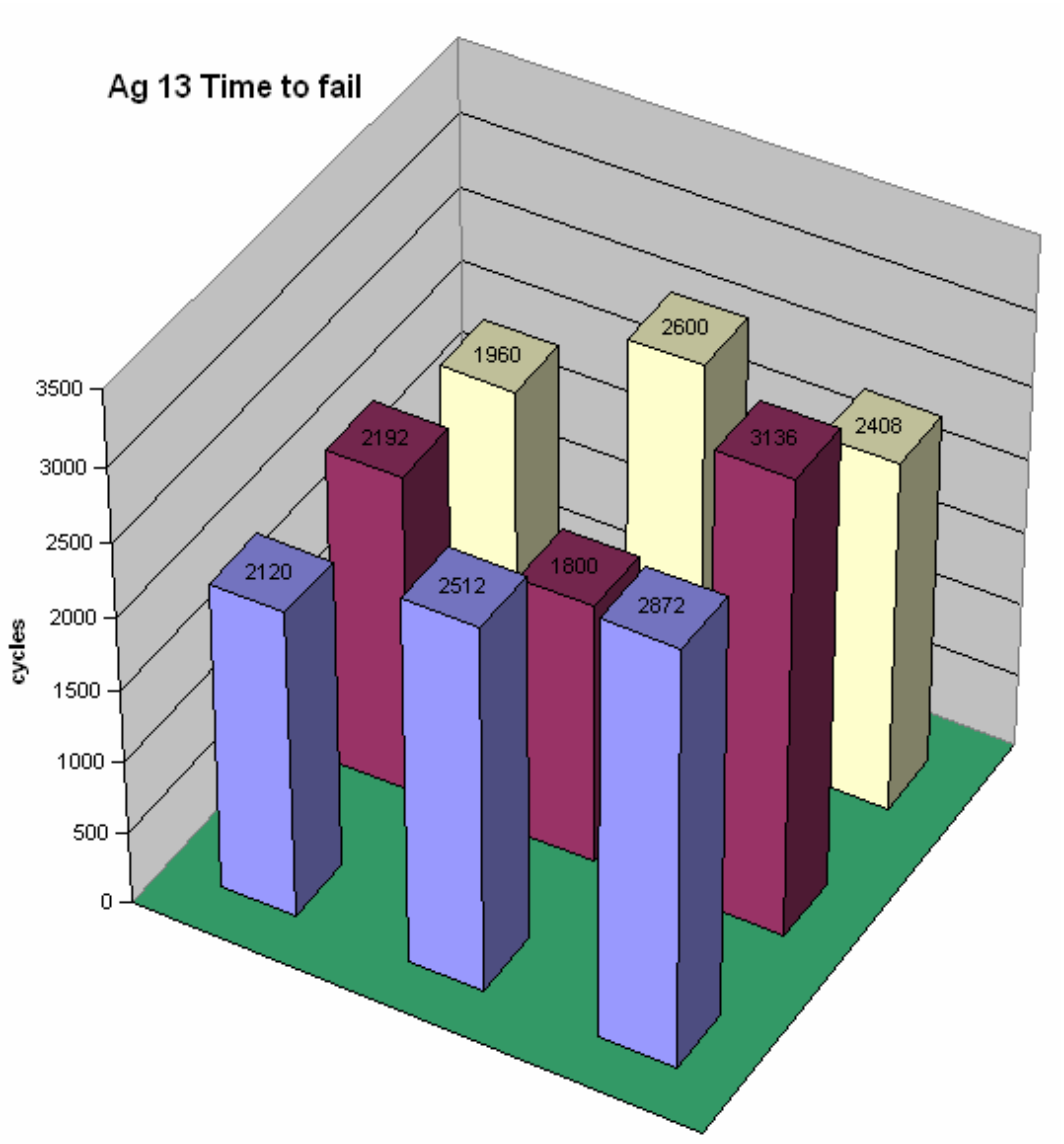

Figure 3.6 Number of cycles to fail and failure distribution of packages for Ag 13

3.1.3 Results of Boards with OSP type Finish

Again in the case of the OSP pad finish boards, the joints registered initial failure around 2000 cycles and almost all the packages had failed within 10,000 cycles.

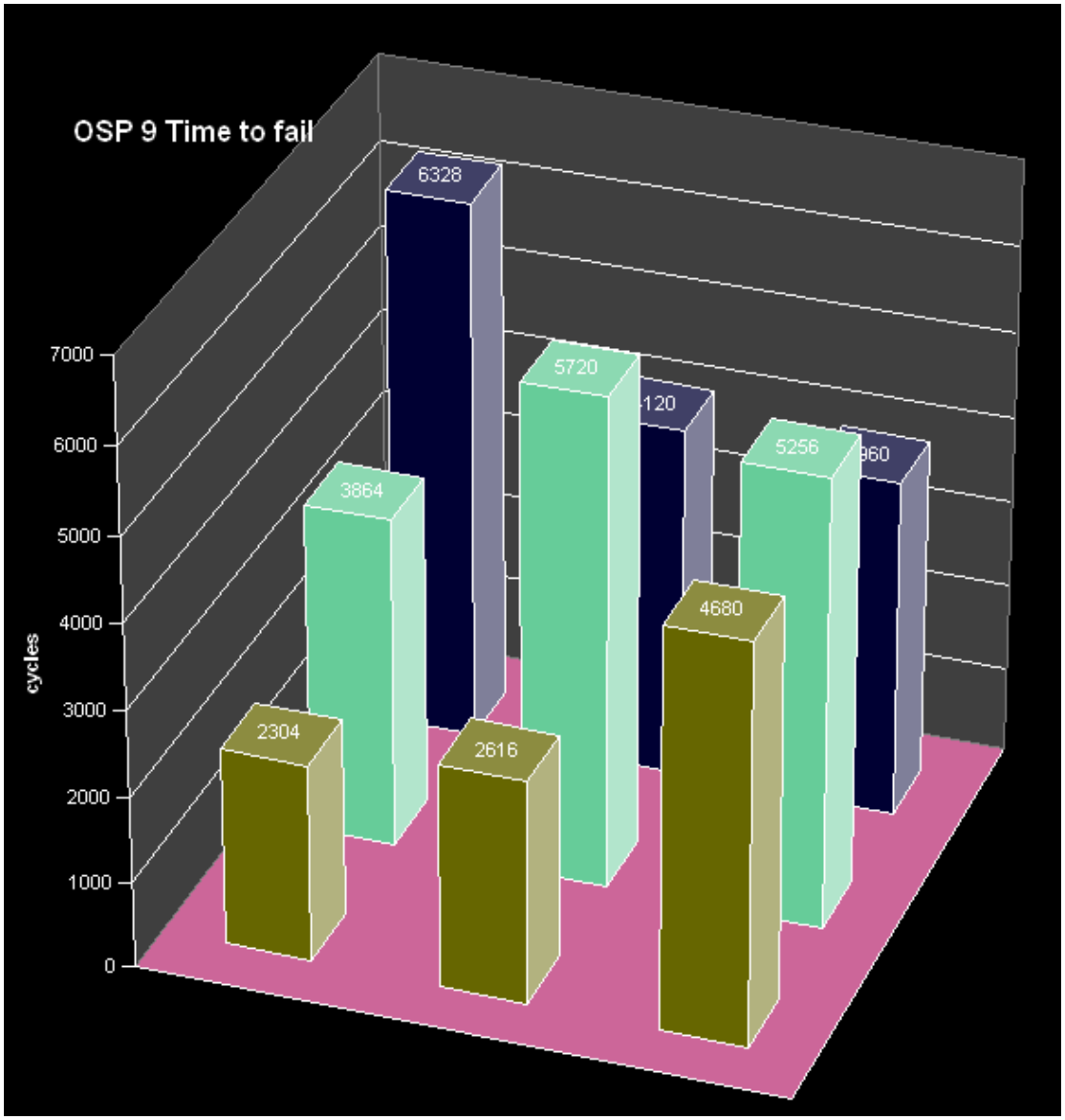

Figure 3.7 Number of cycles to fail and failure distribution of packages for OSP 9

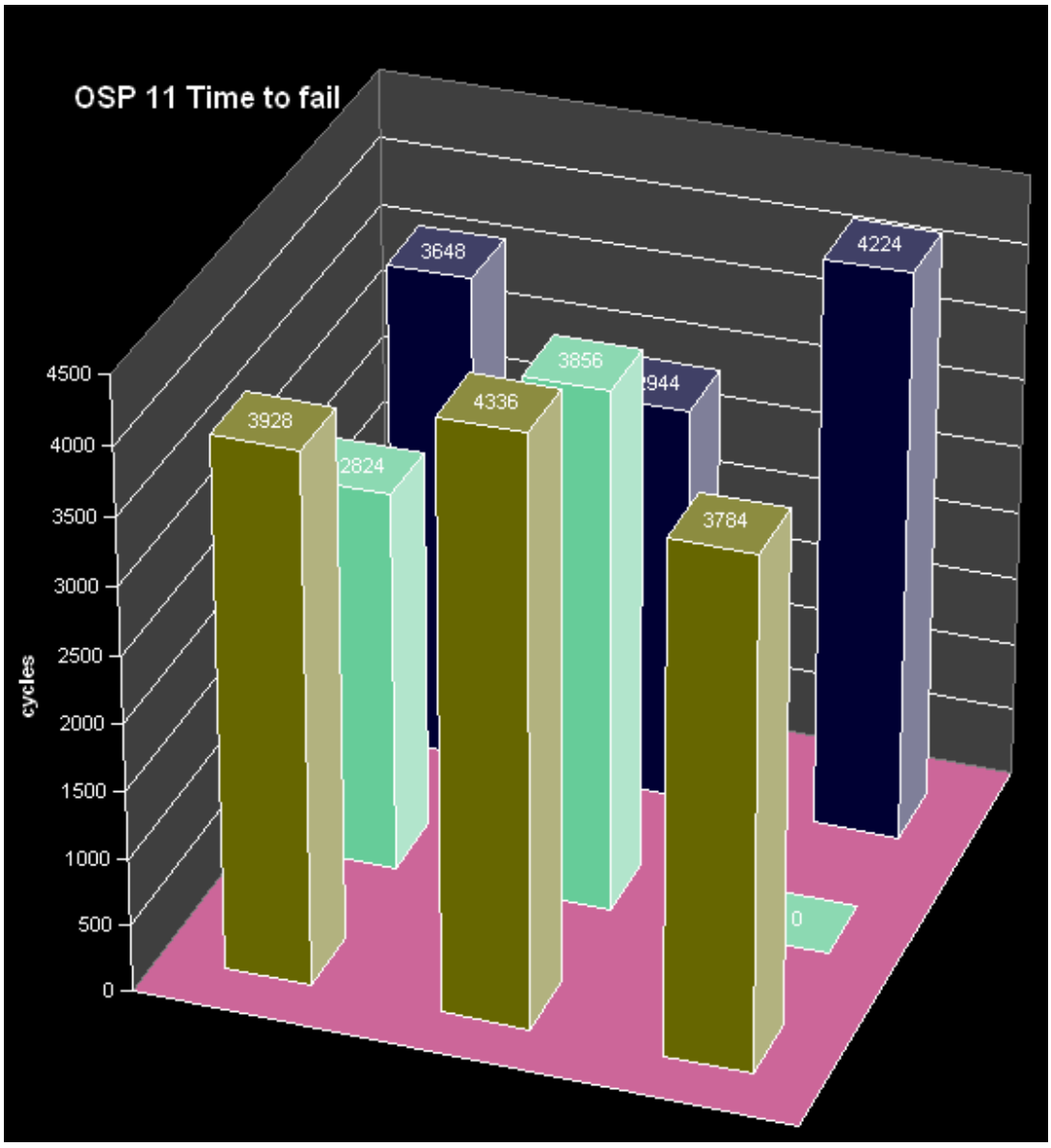

Figure 3.8 Number of cycles to fail and failure distribution of packages for OSP-11

Table 3.1 Combined results of cycles to fail for all packages

Package	Au8	Au10	Au3	Ag9	Ag11	Ag13	OSP9	OSP11
2	22120	16256	5832	1736	2016	2120	2304	3928
3	27400	15952	19144	2600	3152	2512	2616	4336
4	DID NOT FAIL AFTER 72000 CYCLES	30048	6680	NOT TAKEN TO FAILURE	3056	2872	4680	3784
7	18096	16136	19584	1944	2024	2192	3864	2824
8	65624	22368	21424	NOT TAKEN TO FAILURE	1984	1800	5720	3856

Table 3.1- continued

9	72888	24528	10032	NOT TAKEN TO FAILURE	NOT TAKEN TO FAILURE	3136	5256	NOT TAKEN TO FAILURE
12	9024	22128	7488	1784	1944	1960	6328	3648
13	44944	11712	18360	1832	2512	2600	4120	2944
14	28912	11984	15656	1856	2160	2408	3960	4224

3.2 Strain Gage Results

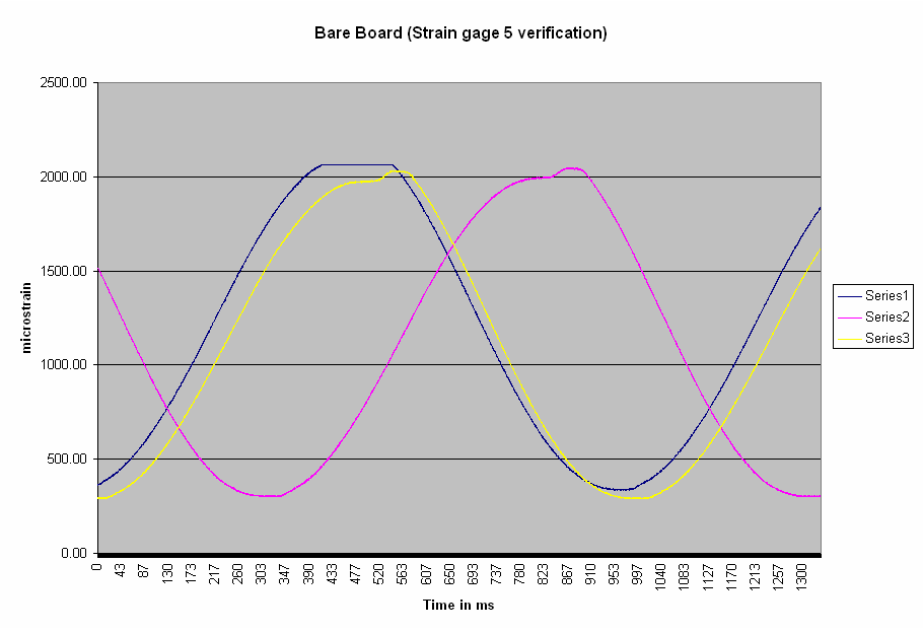

Figure 3.9 Plot of strain gage readings over several intervals

Multiple strain gage readings were taken and compared with each other in order to verify that each gage was giving similar readings over the period of the test. The above figure is an example comparing the different readings taken for a particular strain gage and matching them up, all strain gage readings were found to be similar although in one case a strain gage was consistently giving erroneous readings. The strain gage readings for the bare board as well as readings from both sides of the populated boards are plotted below. We can see that the strain on the bare board is less than that of the test board, since the test board has components which increase the overall stiffness.

Also we see that the back side of the board which experiences compression has lesser strain than the front of the board which is the populated side as well.

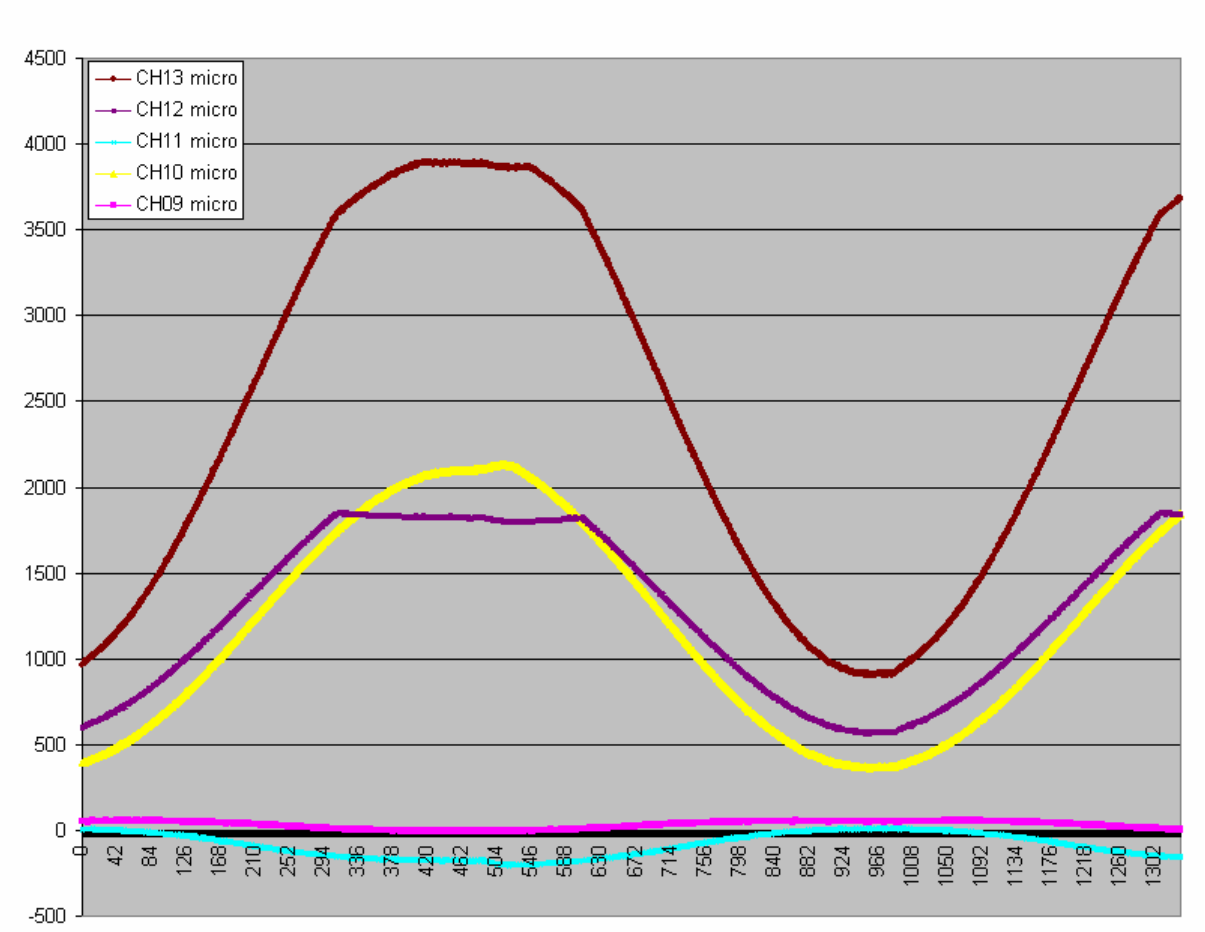

Figure 3.10 Strain gage distributions over an unpopulated board

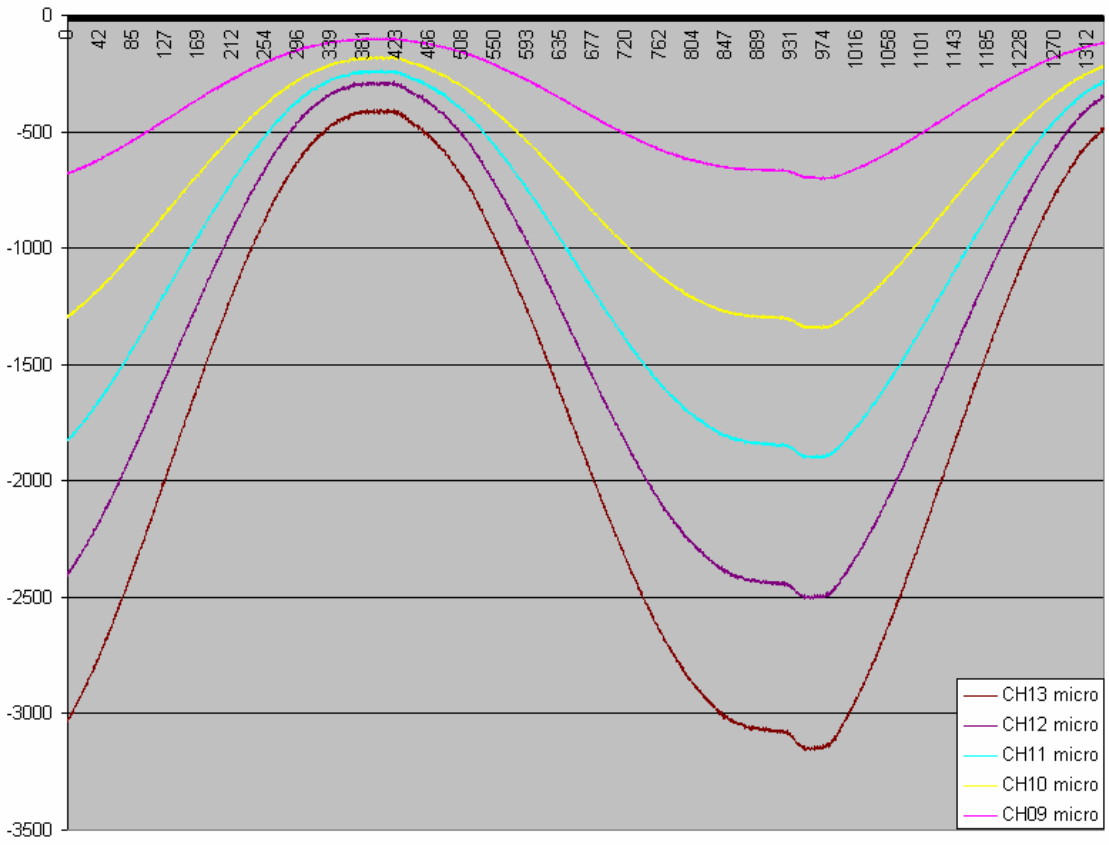

Figure 3.11 Strain gage distributions over the empty side of a populated board

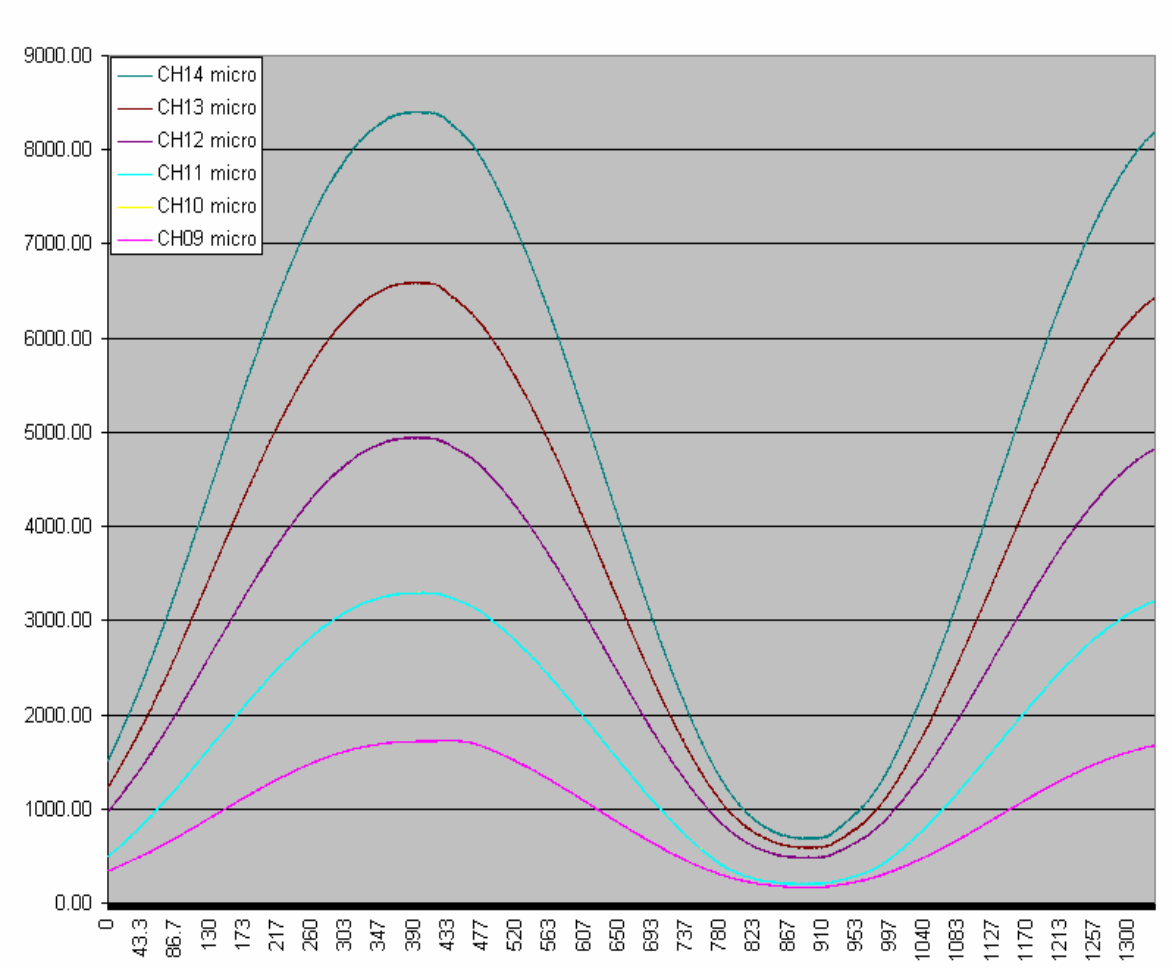

Figure 3.12 Strain gage distributions over the component side of a populated board

3.3 Failure Analysis

From the results of the bending test we can see that there is definitely a great difference between the performances of lead free solder as compared to the conventional Sn-Pb solder. Also we note that the different Cu pad finish on the PWB have supplied us with very different results. The next step is to locate the failure sites and try to find the mechanism behind the failure. The packages were singulated with a diamond saw after which they were mounted in epoxy resin mixture and polished to a fine level in order to observe possible failures. As the Weibull plot below shows, the Au pad surface finish was the longest lasting. During the failure analysis, cracks were found on the upper side (package side) of the joint. This was an expected result since the typical failure of solder joints occurs due to crack formation and propagation at the location of maximum stresses. Since the pad diameter on the package side is defined by the solder mask, it forms a point of stress concentration from where the crack initiates.

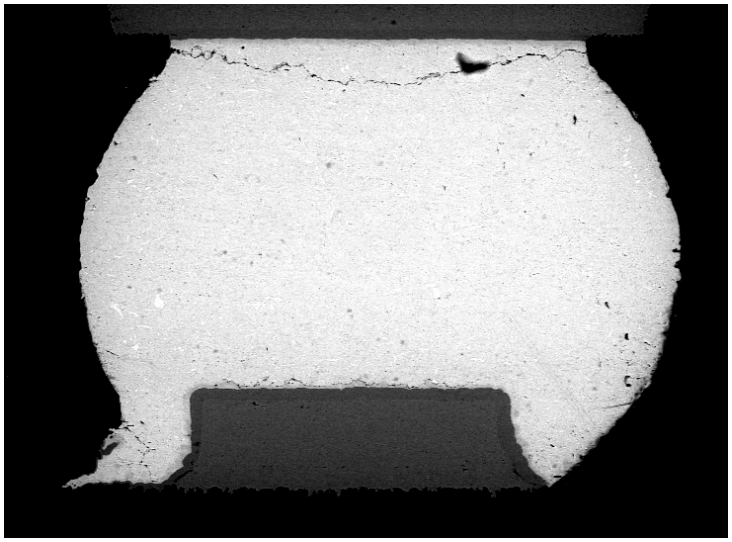

Figure 3.13 Cracks on the package side of the ball for Au pad finish board

This observation was made for joints on the Au type surface finish boards. The very early failures of OSP and Ag type boards were a cause for concern and it was expected that they would reveal several cracks in the balls. However, after polishing several packages for both OSP and Ag type, no ball failures could be found. There were some instances of voids for the Ag joints which may have been the cause for a weak joint and high electrical resistance but they were not the cause of failure. Another failure mode was found in the case of OSP joints which had failed because of trace failure rather than ball failure.

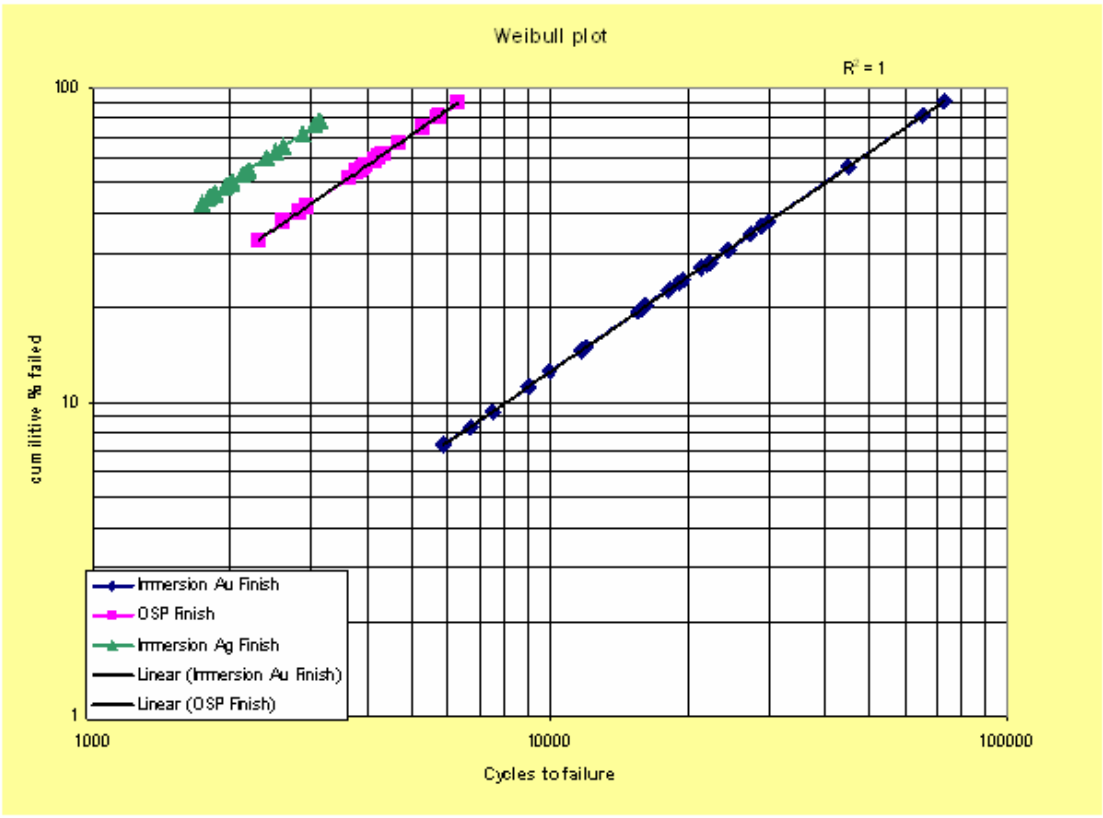

Figure 3.14 Weibull distribution of failures comparing the three types of boards

Figure 3.15 Voids observed during the analysis of Ag finish packages

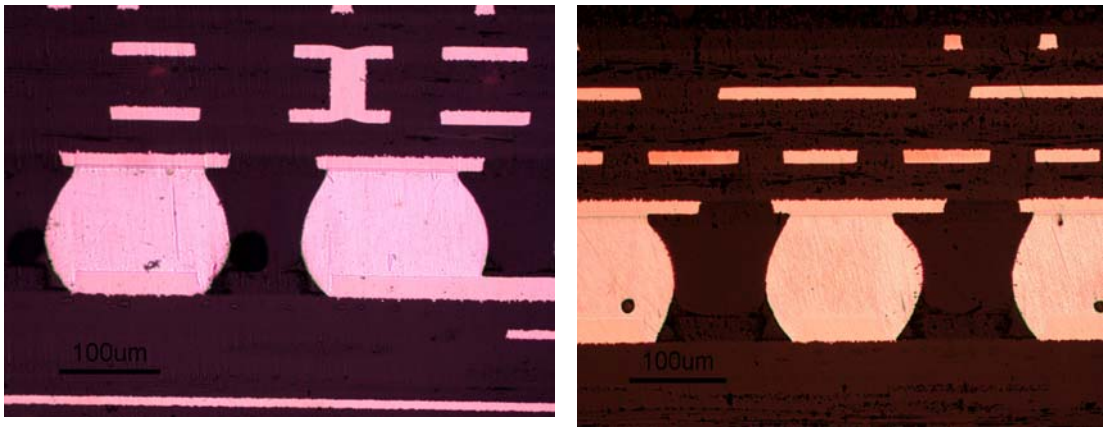

Figure 3.16 Examples of solder joints for Ag and OSP packages (no ball failures were observed on any of the joints for these two types)

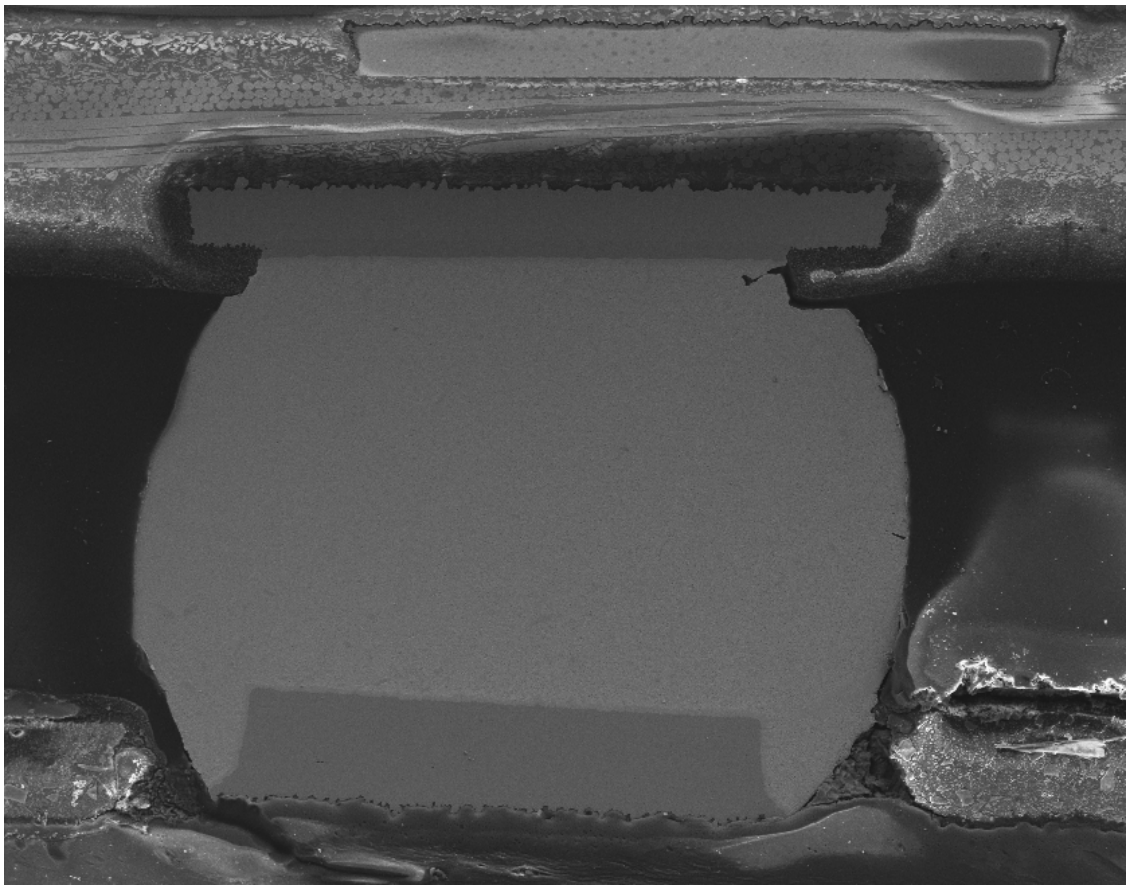

Figure 3.17 Peeling of Copper pad on an OSP board joint

The above image is important since it is one of the few that provide some clue as to why the OSP type boards failed earlier. Peeling of the copper pad would definitely register as an intermittent or permanent failure during the testing. In order to further verify the possibility of trace failures, dye and pry test was done on some of the OSP and Ag packages.

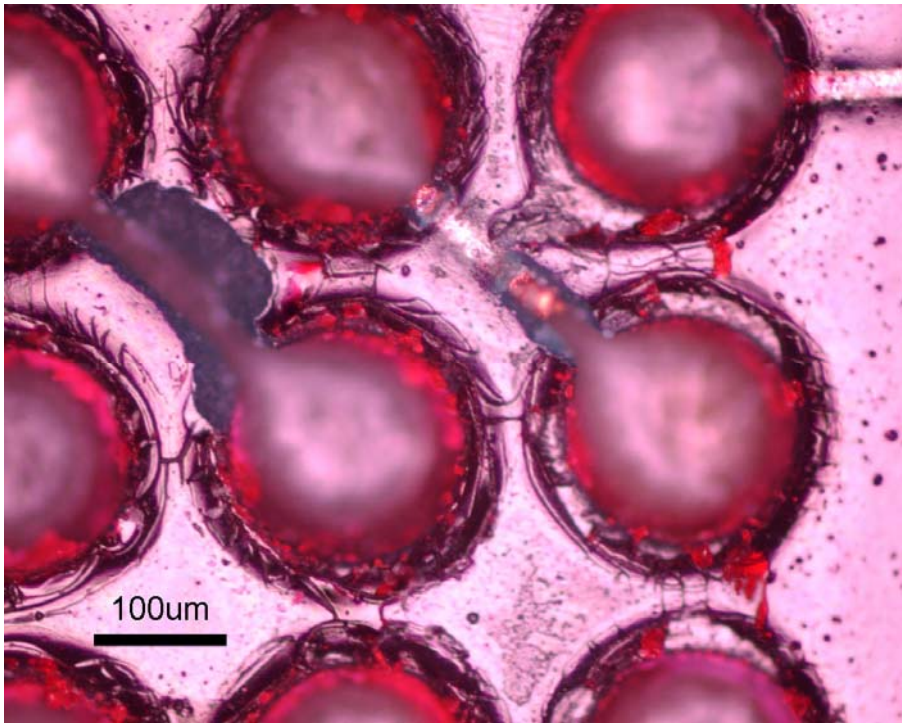

Figure 2.1 Sample Figure 3.18: Possible trace failure observed after Red Dye testing

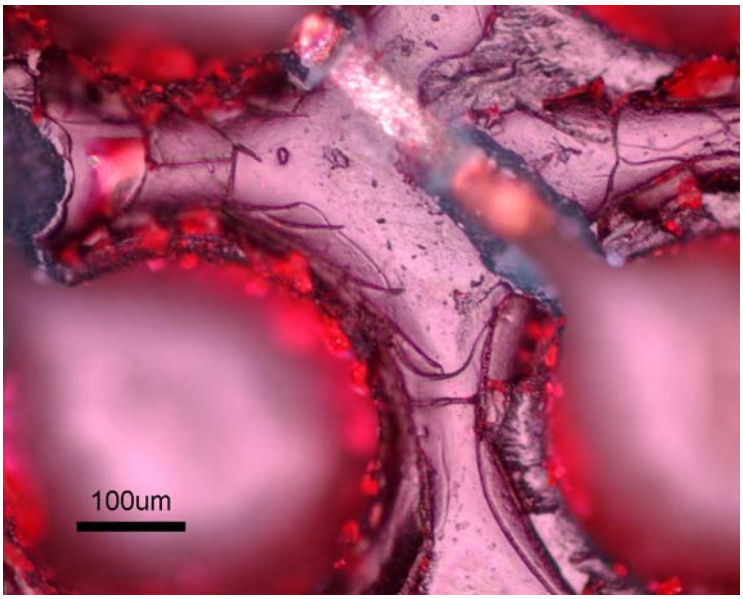

Figure 3.19: Close up view of trace failure on the board side of OSP package

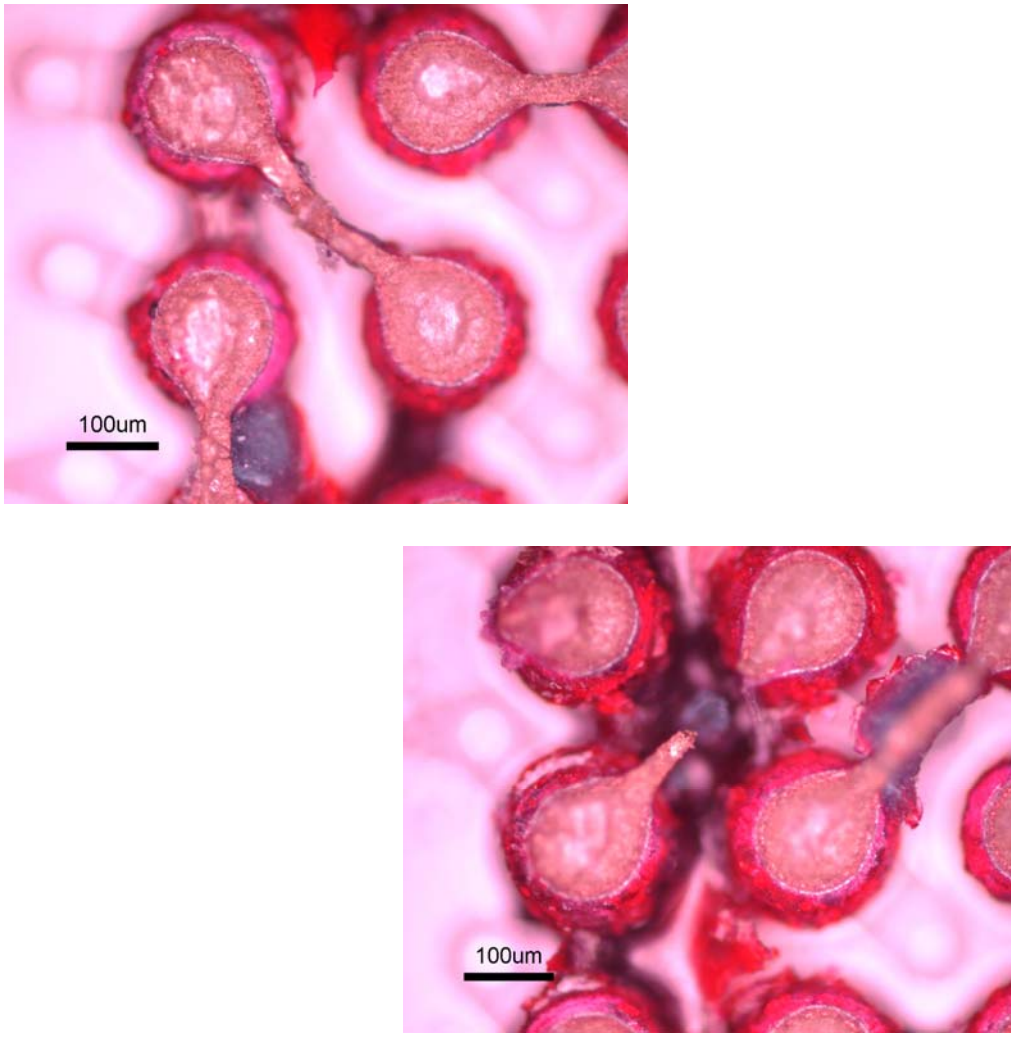

Figure 3.20: Failures observed on Ag finish packages. Image on the left shows a trace failure on the board and the right image is a counterpart on the package

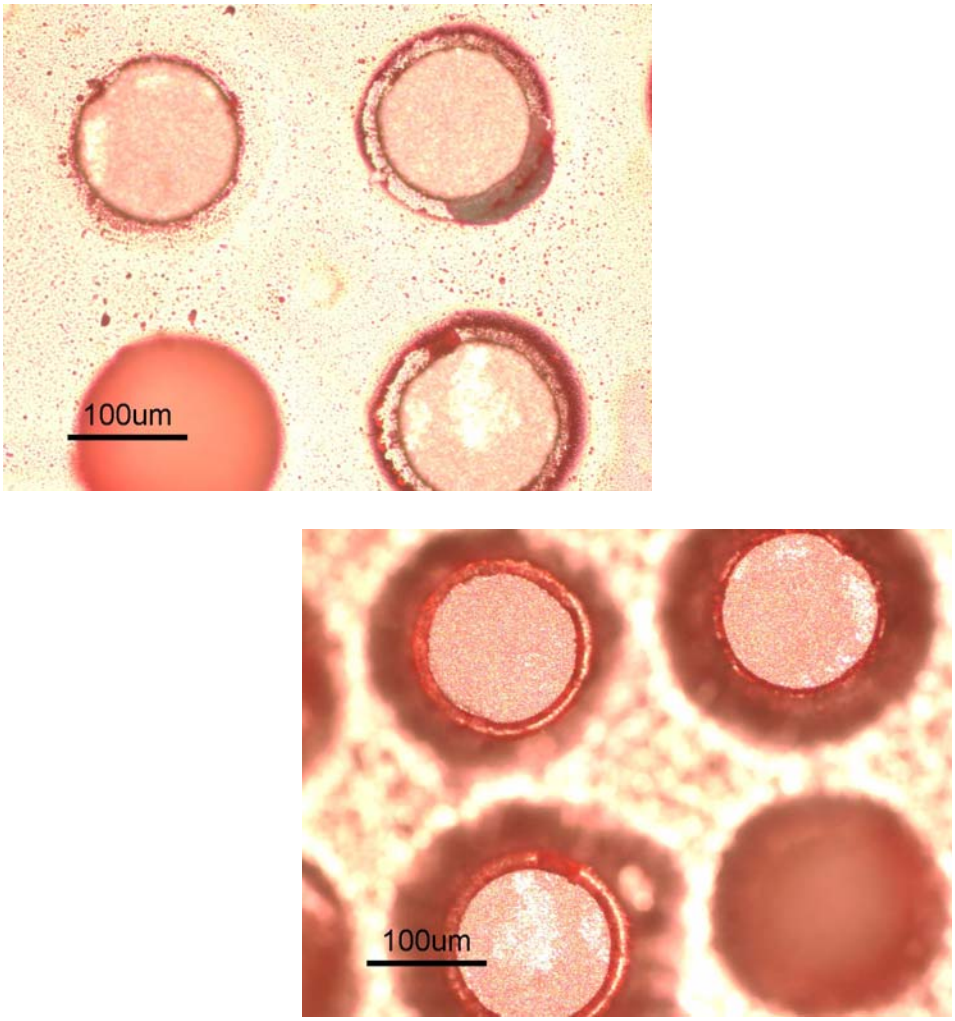

Figure 3.21: Possible ball failures observed on package (left) and board side (right) after Red Dye testing. Some penetration of the dye can be seen

CHAPTER 4

CONCLUSIONS

4.1 Conclusions from Failure Analysis

The results obtained from the cyclic bending test can be summarized as follows. The test was conducted in order to determine the failure modes and mechanisms for lead free solder so that it may be characterized and a failure model developed. The use of three different kinds of PWB pad surface finish was done to compare and find the best combination of solder material and intermetallics. From the results of the experiment it is clear that for the case of this particular composition of lead free solder and using the suggested reflow profile, the joints formed between pads covered with gold surface finish lasted much longer than joints with other surface finish materials.

An important point in the failure analysis is the condition of the boards used for testing. The appearance of trace failures at such an early stage calls in to question the quality of the boards used for testing. However, the boards were inspected thoroughly both before the reflow and after and it seems to much of a coincident that only the boards with OSP and Ag surface finishes failed very rapidly. It would be safe to conclude that the pad finish indeed has a significant impact on the reliability of the joint.

Since the difference between the failure times for the silver and OSP boards is much less than for the gold boards it seems as though neither pad finish is suitable for the case of lead free solder. However, the reliability of the solder joints is highly dependant on the intermetallic layer formed between the solder and the pad. This intermetallic formation is in turn dependant on the cooling rate and reflow profile it is subjected to. Although the solder balls used in all cases were the same, it is possible that by optimizing the reflow profile for the different surface finishes we can achieve better reliability than demonstrated in this study.

Another possible reason for the early failure of some boards could be the presence of voids in the solder joints. The evidence of trace failures presents another possibility. Since the cost of test boards is prohibitively high and some of the boards were already disregarded due to the presence of solder bridges or other defects, the total sample size for the experiment was just eight boards. These eight were further differentiated by the pad finish, meaning that for any given finish the number of boards tested were only two or three. More importantly it is appropriate to compare only those packages which have been subjected to the same strain i.e. the middle column of one board can be compared with the middle column of another similar board. For example a comparison can be made between six packages of the central row of the two OSP boards. The point being that the sample size is fairly small so that the different modes of failure need to be further studied in order to validate these results.

4.2 Further work and recommendations

In view of the previous discussion, it is required that the failure analysis of all the packages be continued until all possibilities are exhausted. Even then there may not be enough evidence to validate the previous claims. If possible it would be highly recommended that more testing be done using the same solder with due consideration given to the possibility of optimizing the reflow profiles. Also it would be desirable to proceed with one kind of surface finish and test it with a greater sample size.

Also, the present results can be used in the finite element simulations of the cyclic bending test, which will be used to develop a failure model for the case of lead free solder. In this context an important consideration is the size of the model used for the FE simulation. Since each package has 288 balls and there are 9 packages on each board, a full model of the problem would be too expensive in terms of computing. Even with the use of bi lateral symmetry the problem is still very large, since the balls need to be modeled as spheres in order to fully analyze the detail. At present a simplified model is being used which models the balls as cuboids rather than spheres. The mathematical modeling of components for structural problems is also an unexplored area and can be made in to an excellent project.

REFERENCES

[1] Effect of Cyclic Bending on Chip Scale Package Assemblies, Master's thesis, S. Shetty, V. Lehtinen, and A. Dasgupta, CALCE Electronic Products and Systems Consortium, University of Maryland, College Park

[2] S. Shetty, V. Lehtinen, A. Dasgupta, V. Halkola, and T. Reinikainen, "Effect of Bending on Chip Scale Package Interconnects," presented at 1999 ASME International Mechanical Engineering Congress at Nashville, Tennessee, Nov 14th - 19th.

[3] Reliability of Area Array Solder Joints In Bending;
Robert Darveaux and Ahmer Syed (SMTA 2000)

[4] L. Leicht and A. Skipor, "Mechanical Cycling Fatigue of PBGA Package Interconnects," Proc. International Symposium on Microelectronics, 1998, pp. 802-807.

[5] H. Juso, Y. Yamaji, T. Kimura, K. Fujita, and M. Kada, "Board Level Reliability of CSP," Proc. IEEE ECTC, 1998, pp. 525-531.

[6] U.D. Perera, "Evaluation of Reliability of mBGA Solder Joints Through Twisting and Bending," Microelectronics Reliability, 39, 1999, pp. 391-399.

[7] John H. Lau & S.W. Ricky Lee, Chip Scale Package- Design, Materials, Process, Reliability, and Applications, 1999

[8] Handbook of Lead-Free Solder Technology for Microelectronic Assemblies,Karl J Puttliz, Kathleen A Stalter

[9] Hossain, M., H., Agonafer, D., Puligandla V., Reinikainen, T.," The effect of intermetallic compound in solder joint fatigue life prediction using finite element modeling,", The Pacific Rim/ASME International Electronic Packaging Technical Conference and Exhibition, InterPACK' 03,July 6-11, 2003, Maui, Hawaii.

[10] Failure Modes and Mechanisms, Pratap Singh, Puligandla Viswanadham, Chapman & Hall publishing

[11] IPC/JEDEC-9702 Monotonic Bend Characterization of Board level interconnects

[12] Darveaux, R., Banerji, K., Mawer, A., and Dody, G., "Reliability of Plastic Ball Grid Array Assembly," Ball Grid Array Technology, J. Lau, ed., McGraw-Hill, Inc. New York, 1995, pp. 379-442.

[13] Fundamentals of Microsystems Packaging; Rao Tummala; McGraw Hill Publishing

[14] Quality Conformance and Qualification of Microelectronic Packages and Interconnects, Michael Pecht, Abhijit Dasgupta, John W. Evans , Wiley Interscience publication 1993

[15] DIRECTIVE 2002/95/EC OF THE EUROPEAN PARLIAMENT AND OF THE COUNCIL of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment Official Journal of the European Union

[16] Waste Electrical and Electronic Equipment (WEEE) Directive
Official Journal of the European Union

BIOGRAPHICAL INFORMATION

Fahad Iqbal Zahedi holds a Master's degree in Mechanical Engineering from the University of Texas at Arlington in 2005. He obtained his Bachelor's in Mechanical Engineering from N.E.D University of Engineering and Technology, Karachi, Pakistan which is one of the oldest and most reputed institutes of that country. His specialization is in electronic cooling and electronic packaging. His experience includes work in structural steel fabrication project for oil rigs as well as some work in HVAC applications.