

ROOM-TEMPERATURE SINGLE-ELECTRON DEVICES
BASED ON CMOS FABRICATION TECHNOLOGY

by

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ABSTRACT

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Single-electron devices, in which the transport and storage of individual electrons is precisely controlled, have many potential benefits in the field of electronics, optics, and sensors. Fabrication of these devices requires the arrangement of device components (Coulomb island, source, drain, and gate electrodes) with nanometer scale precision. Although several methods have successfully demonstrated single-electron behavior, large-scale fabrication of single-electron devices has not been possible.

This research aims to –

- Come up with a method which would allow the fabrication of single-electron devices on a large scale,
- Make the fabrication method compatible with current CMOS technology, and,
- Enable room-temperature operation of the single-electron devices.

A major achievement of this research has been the creation of a new single-electron device structure within the framework of current CMOS technology which has allowed for the fabrication of single-electron devices on a large scale and in parallel process. This was made possible by employing a vertical electrode configuration where the source and the drain electrodes were separated by a thin layer of dielectric medium (~10 nm). Next, Coulomb islands

were attached to the exposed sidewalls of the dielectric film using a combination of colloidal and surface chemistry. Individually addressable gate electrodes were then incorporated in devices, also in complete parallel processing.

Subsequent I-V measurements of these devices have yielded Coulomb blockade, Coulomb staircase, and Coulomb oscillations at room temperature and at low temperature. A systematic study of the single-electron charging/tunneling was carried out utilizing different sizes of Coulomb islands. The dependence of the nature of the Coulomb blockade and Coulomb staircase on nanoparticle size, temperature, and location of the Coulomb island were also investigated. Simulations based on the orthodox theory are in excellent agreement with the experimental results.

Another challenge toward the realization of nanoscale devices is to develop a technique which enables an accurate and reliable positioning of nanostructures onto the targeted locations. Combining wet chemistry and CMOS fabrication technology, a method was developed which enables precise positioning of nanoparticles in the gap between two electrodes. Such precise positioning of nanoparticles could be utilized to improve the yield of single-electron devices.

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CHAPTER 1
INTRODUCTION
1.1 Overview

In 1958 Jack Kilby working as an engineer in Texas instruments demonstrated the first working integrated circuit [1.1] for which he was awarded the Nobel Prize in Physics in 2000. Since then the growth of the modern semiconductor industry has been nothing short of phenomenal. Intel co-founder, Gordon E. Moore, published a famous article in *Electronics* magazine in 1965 in which he said that the number of transistors in a chip would double every year and predicted that this trend would continue into the next decade [1.2]. After Gordon Moore's initial prediction, the growth slope changed in the mid 1970s so that the number of transistor on a chip doubled every 18 months and for the next thirty years the device density on a chip has followed the famous "Moore's Law" [1.3,1.4]. The motivation for the miniaturization of devices include better device performance (faster operation, lower power consumption), smaller production costs per unit device (cheaper fabrication, less material input), and added functionalities.

Over the last few decades, the microelectronics industry has seen the continuous evolution of fabrication tools as well as materials and processes to keep up with the need to increase device density. Parallely, significant research is being carried out to come up with new concepts that may be used in conjunction with traditional CMOS devices. The use low dimensional objects such as carbon nanotubes [1.5-1.10], nanowires [1.11-1.13], individual molecules [1.14,1.15], quantum dots and metallic nanoparticles [1.16-1.18] are being investigated as possible candidates for applications in future electronic devices and sensors. However, as emerging technologies, these proposals must overcome many significant difficulties before they can realistically be implemented.

1.2 Single-electron devices

The International Technology Roadmap for semiconductors lists the various emerging technologies which might assist in the scaling of microelectronic devices under each category in the emerging technology sequence shown in Figure 1.1. In this, single-electron devices are of particular interest because of their predicted use in memory as well as logic applications. The advantages of single-electron devices over conventional silicon devices include their ultra-low power consumption, scalability down to the sub-nanometer range, and their ability to detect an extremely small amount of charge (theoretically down to a fraction of the charge of a single electron). These properties of single-electron devices could potentially benefit a variety of applications including commercial electronics, military, and space applications.

Despite the advantages of single-electron devices, their implementation is still in its infancy. A critical requirement for the fabrication of these devices is that the device components (Coulomb island, source, drain, and gate electrodes) be arranged with nanometer scale precision. This has so far been carried out using sophisticated nanoscale pattern definition techniques such as nano-oxidation using STM [1.16], e-beam lithography/shadow mask evaporation [1.17], electromigration [1.18], mechanically controlled break junctions [1.19, 1.20], etc. Although successful demonstration of single-electron behavior in devices has been reported using the aforementioned techniques, their fabrication has been limited to single device units or a combination of a few device units. Practical applications require that several single-electron devices be fabricated simultaneously and over a wafer-scale.

One of the objectives of this study is to fabricate single-electron devices, which operate at room temperature, on a large-scale, in parallel process, while using materials and processes within the framework of CMOS processing technology. Such multiple and individually addressable devices might enable the fabrication of chip-level integrated systems of single-electron devices. This method could also be applied to large-scale and parallel synthesis of other nanoscale devices and sensors using nanowires, carbon nanotubes, quantum dots etc.

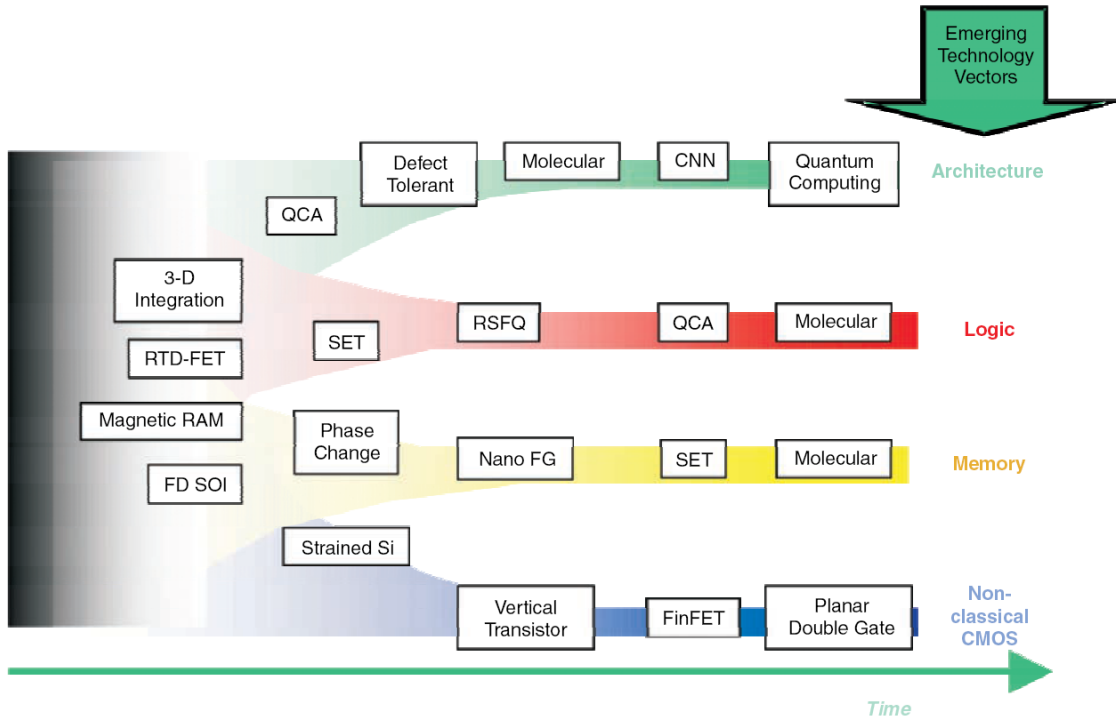


Figure 1.1 Emerging technology sequence of the Engineering, Research and Development section of the International Technology Roadmap for Semiconductors [1.21].

1.3 Organization of this thesis

The advantages of single-electron devices such as the ability to store and transport single electrons, very low operational power consumption, and the fact that they have a huge potential for a variety of practical applications was the major motivation to study single-electron transport in metallic nanoparticles. An important objective of this research was to create a new single-electron device structure within the framework of current CMOS processing technology which would enable the fabrication of single-electron devices on a large-scale and in complete parallel processing. Demonstration of room-temperature single-electron behavior using the proposed device structure was an equally important goal.

In Chapter 2, two single-electron device structures, the double junction single-electron device and the single-electron transistor, will be introduced. This chapter identifies the basic components of single-electrons devices, how these components are arranged in a double junction single-electron device and a single-electron transistor along with the equivalent circuit diagrams of the devices. To understand the electrical characteristics of single-electron devices, the equations governing the electron transport in these devices will be derived and how the results correspond to the observation of phenomena that are unique to single-electron devices will be explained. The tunneling or transport of single electrons in these devices will also be explained qualitatively using potential diagrams for both devices.

In Chapter 3, a brief history of single-electron devices and the noteworthy achievements that have been accomplished in the field will be presented. This will be followed by the description of the new single-electron device structure and the advantages that it has over the other methods that have been used to fabricate devices so far.

Chapter 4 will deal exclusively with the fabrication of the single-electron devices using only CMOS compatible processing techniques. The fabrication was done on a 4 inch silicon wafer. The devices were fabricated using a combination of optical lithography, e-beam evaporation, plasma enhanced chemical vapor deposition (PECVD), formation of self-

assembled monolayers (SAMs), RF magnetron sputtering, and reactive ion etching (RIE). Special precautions that are needed to mount the completed devices on chip carriers and details of wire bonding techniques will also be presented.

The measurement set-up for the electrical characterization of the single-electron devices at various temperatures will be presented in Chapter 5. This will be followed by the analysis of the electrical characterization data from many fabricated single-electron devices. Depending on device configurations, the different I-V characteristics and how they describe single-electron transport for each configuration will be described. These devices show single-electron behavior not only at low temperatures but at room-temperature as well, implying that practical applications for single-electron devices with the new single-electron device structure are feasible.

A new method with which charged nanostructures can be placed with nanometer scale precision on desired substrate locations will be presented in Chapter 6. Experimental methods involving this new technique will be applied to align Au nanoparticles of various sizes with a very high degree of precision. A model explaining such precise positioning will be discussed and detailed calculations regarding the nature of the aligning forces will be calculated using 20 nm diameter Au nanoparticles as a model system. How this method can be implemented in case of single-electron devices to improve device yield will also be included in this chapter.

In the concluding Chapter 7, the achievements of this study will be summarized and some experiments will be proposed that could be a continuation of this work in future.

CHAPTER 2
THEORY OF SINGLE-ELECTRON TUNNELING

2.1 Introduction

In the previous chapter, single-electron devices as promising candidates for applications in future electronic devices and sensors were presented. In this chapter, we will discuss how electron transport occurs in single-electron devices. The outline of this chapter is as follows:

- (a) We will start by describing a tunnel junction which is one of the most important components of single-electron devices.
- (b) The arrangement of the device components (Coulomb island, tunnel barriers, source and drain electrodes) in a double junction single-electron device and its equivalent circuit will be presented next. This will be followed by the derivation of an expression for the free energy of this single-electron device.
- (c) The expression for the free energy of a double junction single-electron device will be used to explain the Coulomb blockade and the Coulomb staircase which are decisive indications of single-electron transport in these devices. How the nature of the Coulomb blockade and Coulomb staircase is influenced by various device component parameters will also be analyzed. A qualitative understanding of the Coulomb blockade and Coulomb staircase will be explained with the aid of electrostatic potential diagrams for this device.
- (d) Next, a second single-electron device, the single-electron transistor will be introduced. The arrangement of device components for a single-electron transistor will be presented followed by the derivation of an expression for the free energy of this device. The existence of Coulomb diamonds and Coulomb oscillations which are current-

voltage characteristics unique to single-electron transistors will be explained using the expression for the free energy of this device. The appearance of Coulomb oscillations in the I-V characteristics of the device will also be explained with the aid of electrostatic potential energy diagrams.

- (e) In the concluding part of this chapter, the electron tunneling rate through a tunnel junction will be calculated using Fermi's Golden-Rule calculations and the change in the free energy of the single-electron device system as a single electron tunnels through a particular tunnel junction. Once the tunneling rate of electrons through all the tunnel junctions of a single-electron device is known, an expression for the total current in the device will be derived.

2.2 Tunnel junction

One of the essential elements of single-electron devices is a tunnel junction. A tunnel junction is a circuit element consisting of two conductors which are separated by a thin dielectric layer.

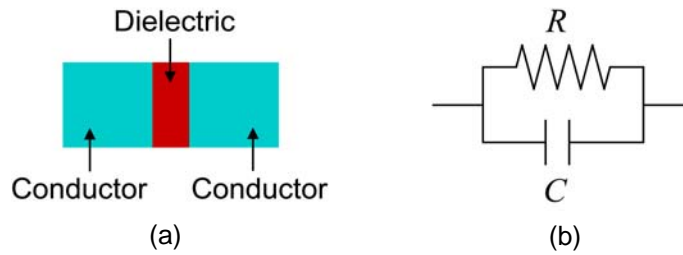


Figure 2.1 (a) Schematic of a tunnel junction (b) Equivalent circuit of a tunnel junction

A tunnel junction can be represented by a capacitor C and a resistor R connected in parallel. The capacitor in a tunnel junction differs from a classical capacitor in that it permits the tunneling of electrons across the dielectric barrier when energetically favorable. Although represented as a resistor, the tunneling resistance is fundamentally different from an Ohmic

resistor. In an ordinary resistor, charge flow due to the motion of electrons is continuous. But for a tunneling resistor, the motion of electrons through it is discrete, i.e., electrons move through it one at a time. Figure 2.1 shows the arrangement and the equivalent circuit of a tunnel junction.

2.3 Double junction single-electron device

A double junction single-electron device is formed when a Coulomb island is placed between two electrodes such that the island is separated from the electrodes by tunnel barriers as illustrated schematically in Figure 2.2 (a). Figure 2.2 (b) shows the equivalent circuit of a double junction single-electron device which can be represented as two tunneling junctions connected in series.

2.3.1 Free energy of a double junction single-electron device

The rate of electron tunneling across a tunnel junction Γ can be calculated from the orthodox theory of single-electron tunneling developed by Averin and Likharev [2.1, 2.3] using Fermi's Golden Rule [2.3] and is given by:

$$\Gamma = \frac{1}{e^2 R} \frac{-\Delta F}{1 - \exp(\Delta F / k_B T)} \quad (2.1)$$

where ΔF is the free energy change of the system when the electron tunnels across the junction, R is the tunneling resistance of the junction, e is the unit charge of an electron (1.602×10^{-19} Coulombs), k_B is the Boltzmann Constant (8.617×10^{-5} eV/K), and T is the absolute temperature. From equation (2.1), the change in the free energy of a single-electron device has to be known in order to calculate the electron tunneling rate across a barrier. Once the electron tunneling rate through a tunnel junction is known, the current through the device can be calculated. The equations for the current through a single-electron device will be derived later in this chapter. First, we will derive an expression for the free energy of a double junction single-electron device.

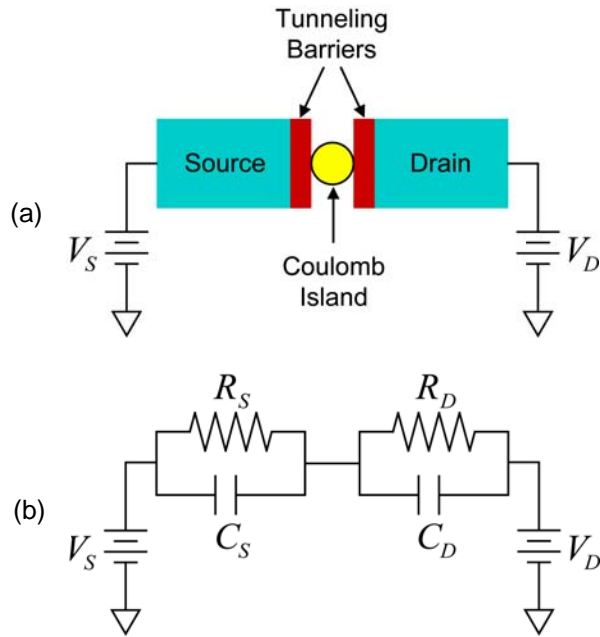


Figure 2.2 Schematic of a double junction single-electron device. (a) Schematic arrangement of single-electron device components (i.e., source electrode, drain electrode, and Coulomb island). The Coulomb island is separated from the electrodes by tunnel barriers. (b) The equivalent circuit of a double junction single-electron device which can be represented as two tunnel junctions connected in series. R_S , C_S , and R_D , C_D denote the resistances and capacitances of the tunnel junctions between the source electrode and the island, and between the drain electrode and the island, respectively.

The free energy of a single-electron device is obtained by calculating the total electrostatic energy stored in the individual tunnel junctions of the device (capacitive charging energy) and subtracting the work done to move electric charges in and out of the Coulomb island.

The model for electrostatic interaction in single-electron devices is based on the capacitive charging energy [2.1, 2.3] in which a tunnel junction is modeled as a parallel plate capacitor. An initially uncharged parallel plate capacitor can be charged by transferring a charge Q from one plate to the other leaving the former plate with a charge of $-Q$ and the latter plate with a charge of $+Q$. Once a charge transfer takes place, an electric field is set up between the plates which opposes any further charge transfer. In order to fully charge the capacitor, work has to be done against this field which becomes the energy stored in the capacitor.

Let us assume that the capacitor plates carry a charge of q and the potential difference between the plates is V . Now, the work done in transferring an infinitesimal amount of charge dq from the negatively charged plate to the positively charged plate can be written as:

$$dW = Vdq \quad (2.2)$$

In order to calculate the total work done $W(Q)$ in transferring a charge Q from one plate to the other we can divide this charge into small increments dq , calculate the incremental work done dW in transferring this incremental charge using equation (2.2), and then add up all of these works. The potential difference between the plates V is a function of the charge transferred.

$$\therefore V(q) = \frac{q}{C} \quad (2.3)$$

where C is the capacitance of the parallel plate capacitor.

Equations (2.2) and (2.3) can be combined and expressed as:

$$dW = \frac{q dq}{C} \quad (2.4)$$

Now, the total work done in transferring charge Q from one plate to another is obtained by integrating equation (2.4) from when there is no charge on the capacitor to when the capacitor is charged with Q .

$$\therefore W(Q) = \int_0^Q \frac{q dq}{C} = \frac{Q^2}{2C} \quad (2.5)$$

Since the work done W in charging the capacitor is the same as the energy stored in the capacitor E , the expression for the energy stored in a parallel plate capacitor is:

$$E = \frac{Q^2}{2C} \quad (2.6)$$

Figure 2.3 shows the equivalent circuit of a double junction single-electron device. Initially, the device is not connected to any external voltage sources and the number of extra electrons in the Coulomb island is defined as zero. Voltage sources V_S and V_D are now connected to the source electrode and the drain electrodes, respectively. If N_S number of electrons tunneled into the island through the tunnel barrier between the source and the island and N_D number of electrons tunneled out of the island through the tunnel barrier between the island and the drain, then the net number of excess electrons in the Coulomb island N is equal to $N_S - N_D$. The external voltage sources build up charges Q_D and Q_S in the tunnel junctions. These charges can be expressed as:

$$Q_D = C_D (V_D - \varphi_{IS}) \quad (2.7) \text{ (a)}$$

and

$$Q_S = C_S (\varphi_{IS} - V_S) \quad (2.7) \text{ (b)}$$

where φ_{IS} is the electrostatic potential of the Coulomb island. Therefore, the voltage drop across the tunnel junction between the drain and the island is $V_D - \varphi_{IS}$ and that between the island and the source is $\varphi_{IS} - V_S$.

In addition, there is usually a fractional electron charge known as the background charge Q_0 present in real structures. This non-integer offset charge on the Coulomb island arises due to the combination of the difference in the workfunctions of the metals forming the tunnel junctions [2.3, 2.13] and random charges that are trapped near the tunnel junctions. Tunneling allows an integer number of excess electrons to accumulate on the island so that the net charge Q on the island can be written as:

$$Q = -Ne + Q_0 = Q_S - Q_D \quad (2.8)$$

where $N = N_S - N_D$ is the net number of excess electrons on the island (which is an integer).

Substituting equation (2.7) in (2.8) and solving for φ_{IS} , we get

$$\begin{aligned} -Ne + Q_0 &= C_S(\varphi_{IS} - V_S) - C_D(V_D - \varphi_{IS}) \\ \Rightarrow -Ne + Q_0 &= C_S\varphi_{IS} - C_SV_S - C_DV_D + C_D\varphi_{IS} \\ \Rightarrow -Ne + Q_0 &= \varphi_{IS}(C_S + C_D) - C_SV_S - C_DV_D \\ \therefore \varphi_{IS} &= \frac{C_SV_S + C_DV_D - (Ne - Q_0)}{C_{TOT}} \end{aligned} \quad (2.9)$$

where $C_{TOT} \equiv C_S + C_D$.

The voltage drop across the tunnel junction between the island and the source $\varphi_{IS} - V_S$ can be simplified by substituting the value of φ_{IS} from equation (2.9) in $\varphi_{IS} - V_S$. Therefore,

$$\begin{aligned} \varphi_{IS} - V_S &= \frac{C_SV_S + C_DV_D - (Ne - Q_0)}{C_{TOT}} - V_S \\ &= \frac{C_SV_S + C_DV_D - (Ne - Q_0) - V_S(C_S + C_D)}{C_{TOT}} \\ &= \frac{C_SV_S + C_DV_D - (Ne - Q_0) - C_SV_S - C_DV_S}{C_{TOT}} \end{aligned}$$

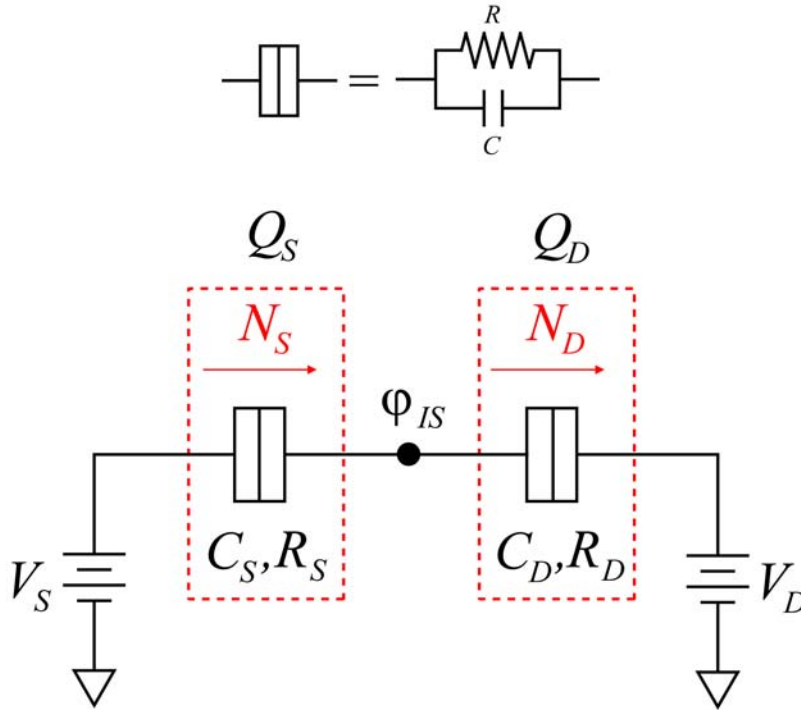


Figure 2.3 Equivalent circuit diagram of a double junction single-electron device. The two tunnel junctions are shown in the dashed red boxes. Q_S and Q_D are the capacitor charges, V_S and V_D are the voltage sources connected to the source electrode and drain electrode, respectively, and N_S and N_D are the integer number of electrons which have tunneled across the junction between the source and the island, and the island and the drain, respectively. ϕ_{IS} is the electrostatic potential of the Coulomb island.

$$\begin{aligned}
&= \frac{C_D(V_D - V_S) - (Ne - Q_0)}{C_{TOT}} \\
\therefore \varphi_{IS} - V_S &= \frac{C_D V_{DS} - (Ne - Q_0)}{C_{TOT}} \tag{2.10}
\end{aligned}$$

where $V_{DS} \equiv V_D - V_S$.

Similarly, the voltage drop across the tunnel junction between the drain and the island $V_D - \varphi_{IS}$ is simplified by substituting φ_{IS} from equation (2.9) in $V_D - \varphi_{IS}$. Therefore,

$$\begin{aligned}
V_D - \varphi_{IS} &= V_D - \frac{C_S V_S + C_D V_D - (Ne - Q_0)}{C_{TOT}} \\
&= \frac{V_D(C_S + C_D) - C_S V_S - C_D V_D + (Ne - Q_0)}{C_{TOT}} \\
&= \frac{C_S V_D + C_D V_D - C_S V_S - C_D V_D + (Ne - Q_0)}{C_{TOT}} \\
&= \frac{C_S(V_D - V_S) + (Ne - Q_0)}{C_{TOT}} \\
\therefore V_D - \varphi_{IS} &= \frac{C_S V_{DS} + (Ne - Q_0)}{C_{TOT}} \tag{2.11}
\end{aligned}$$

The total electrostatic energy stored in the system E_{TOT} is the sum of the electrostatic energy stored in the capacitors of the individual tunnel junctions. Therefore,

$$E_{TOT} = \frac{Q_D^2}{2C_D} + \frac{Q_S^2}{2C_S} \tag{2.12}$$

Substituting the values of Q_S and Q_D from equation (2.7) into equation (2.12), we get:

$$E_{TOT} = \frac{C_D^2 (V_D - \varphi_{IS})^2}{2C_D} + \frac{C_S^2 (\varphi_{IS} - V_S)^2}{2C_S}$$

$$\therefore E_{TOT} = \frac{1}{2} C_D (V_D - \varphi_{IS})^2 + \frac{1}{2} C_S (\varphi_{IS} - V_S)^2 \quad (2.13)$$

Substituting the values of $V_D - \varphi_{IS}$ and $\varphi_{IS} - V_S$ from equations (2.11) and (2.10), respectively in equation (2.13), the total electrostatic energy stored in the double junction single-electron device is given by:

$$\begin{aligned} E_{TOT} &= \frac{C_D}{2} \left[\frac{1}{C_{TOT}} \{C_S V_{DS} + (Ne - Q_0)\} \right]^2 + \frac{C_S}{2} \left[\frac{1}{C_{TOT}} \{C_D V_{DS} - (Ne - Q_0)\} \right]^2 \\ E_{TOT} &= \frac{C_D}{2(C_{TOT})^2} [(C_S V_{DS})^2 + (Ne - Q_0)^2 + 2(C_S V_{DS})(Ne - Q_0)] \\ &\quad + \frac{C_S}{2(C_{TOT})^2} [(C_D V_{DS})^2 + (Ne - Q_0)^2 - 2(C_D V_{DS})(Ne - Q_0)] \\ E_{TOT} &= \frac{1}{2(C_{TOT})^2} [C_D C_S^2 V_{DS}^2 + C_D (Ne - Q_0)^2 + C_D^2 C_S V_{DS}^2 + C_S (Ne - Q_0)^2] \\ E_{TOT} &= \frac{1}{2(C_{TOT})^2} [C_D C_S V_{DS}^2 (C_S + C_D) + (Ne - Q_0)^2 (C_S + C_D)] \\ \therefore E_{TOT} &= \frac{1}{2C_{TOT}} [C_S C_D V_{DS}^2 + (Ne - Q_0)^2] \quad (2.14) \end{aligned}$$

An electron can be added or subtracted from the Coulomb island in the following four ways:

- Electron tunnels into the island from the drain electrode.
- Electron tunnels into the island from the source electrode.
- Electron tunnels out of the island to the drain electrode.
- Electron tunnels out of the island to the source electrode.

If one extra electron is added to the Coulomb island changing its electron occupancy from N to $N + 1$, then the change in the electrostatic energy of the system is given by:

$$\Delta E_{TOT}^+ = \frac{1}{2C_{TOT}} [C_S C_D V_{DS}^2 + \{(N + 1)e - Q_0\}^2] - \frac{1}{2C_{TOT}} [C_S C_D V_{DS}^2 + \{Ne - Q_0\}^2]$$

$$\begin{aligned}
\Rightarrow \Delta E_{TOT}^+ &= \frac{1}{2C_{TOT}} \left[\{(N+1)e - Q_0\}^2 \right] - \frac{1}{2C_{TOT}} \left[\{Ne - Q_0\}^2 \right] \\
\Rightarrow \Delta E_{TOT}^+ &= \frac{1}{2C_{TOT}} \left[(Ne + e - Q_0 + Ne - Q_0)(Ne + e - Q_0 - Ne + Q_0) \right] \\
\therefore \Delta E_{TOT}^+ &= \frac{e}{C_{TOT}} \left[\frac{e}{2} + (Ne - Q_0) \right] \tag{2.15}
\end{aligned}$$

Similarly, if one electron is removed from the Coulomb island changing its electron occupancy from N to $N - 1$, then the change in the electrostatic energy of the system is given by:

$$\begin{aligned}
\Delta E_{TOT}^- &= \frac{1}{2C_{TOT}} \left[C_S C_D V_{DS}^2 + \{(N-1)e - Q_0\}^2 \right] - \frac{1}{2C_{TOT}} \left[C_S C_D V_{DS}^2 + \{Ne - Q_0\}^2 \right] \\
\Rightarrow \Delta E_{TOT}^- &= \frac{1}{2C_{TOT}} \left[\{(N-1)e - Q_0\}^2 \right] - \frac{1}{2C_{TOT}} \left[\{Ne - Q_0\}^2 \right] \\
\Rightarrow \Delta E_{TOT}^- &= \frac{1}{2C_{TOT}} \left[(Ne - e - Q_0 + Ne - Q_0)(Ne - e - Q_0 - Ne + Q_0) \right] \\
\therefore \Delta E_{TOT}^- &= \frac{e}{C_{TOT}} \left[\frac{e}{2} - (Ne - Q_0) \right] \tag{2.16}
\end{aligned}$$

Combining equation (2.15) and (2.16), we get the change in the electrostatic energy of the system when a single electron is added to or subtracted from the Coulomb island as:

$$\therefore \Delta E_{TOT}^\pm = \frac{e}{C_{TOT}} \left[\frac{e}{2} \pm (Ne - Q_0) \right] \tag{2.17}$$

where the \pm sign refers to the addition/subtraction of a single electron to/from the island.

In addition to the electrostatic energy stored in the capacitors, the work done by the voltage sources must also be taken into account to calculate the free energy of the system. Work is done by the voltage sources in transferring electrons into and out of the Coulomb island as well as supplying the necessary charges to the capacitor plates due to polarization.

The charges built up in the tunnel junctions by the voltage sources can be expressed by combining equations (2.7), (2.10), and (2.11) as:

$$Q_D = C_D(V_D - \varphi_{IS}) = \frac{C_D}{C_{TOT}}[C_S V_{DS} + (Ne - Q_0)] \quad (2.18) \text{ (a)}$$

$$Q_S = C_S(\varphi_{IS} - V_S) = \frac{C_S}{C_{TOT}}[C_S V_{DS} - (Ne - Q_0)] \quad (2.18) \text{ (b)}$$

If the electron occupancy in the Coulomb island changes from N to $N + 1$, the change in the charge stored in the tunnel barrier between the drain electrode and the island is given by:

$$\begin{aligned} \Delta Q_D^{N+1,N} &= Q_D^{N+1} - Q_D^N \\ &= \frac{C_D}{C_{TOT}}[C_S V_{DS} + \{(N+1)e - Q_0\}] - \frac{C_D}{C_{TOT}}[C_S V_{DS} + \{Ne - Q_0\}] \\ &= \frac{C_D}{C_{TOT}}[C_S V_{DS} + Ne + e - Q_0 - C_S V_{DS} - Ne + Q_0] \\ &\therefore \Delta Q_D^{N+1,N} = \frac{C_D}{C_{TOT}} e \end{aligned} \quad (2.19)$$

Similarly, the change in the charge stored in the tunnel junction between the island and the source electrode when the electron occupancy in the Coulomb island changes from N to $N + 1$ is given by:

$$\begin{aligned} \Delta Q_S^{N+1,N} &= Q_S^{N+1} - Q_S^N \\ &= \frac{C_S}{C_{TOT}}[C_D V_{DS} - \{(N+1)e - Q_0\}] - \frac{C_S}{C_{TOT}}[C_D V_{DS} - \{Ne - Q_0\}] \\ &= \frac{C_S}{C_{TOT}}[C_D V_{DS} - Ne - e + Q_0 - C_D V_{DS} + Ne - Q_0] \\ &\therefore \Delta Q_S^{N+1,N} = -\frac{C_S}{C_{TOT}} e \end{aligned} \quad (2.20)$$

If the electron occupancy in the Coulomb island changes from N to $N - 1$, the change in the charge stored in the tunnel barrier between the drain electrode and the island is given by:

$$\begin{aligned}
\Delta Q_D^{N-1,N} &= Q_D^{N-1} - Q_D^N \\
&= \frac{C_D}{C_{TOT}} [C_S V_{DS} + \{(N-1)e - Q_0\}] - \frac{C_D}{C_{TOT}} [C_S V_{DS} + \{Ne - Q_0\}] \\
&= \frac{C_D}{C_{TOT}} [C_S V_{DS} + Ne - e - Q_0 - C_S V_{DS} - Ne + Q_0] \\
&\therefore \Delta Q_D^{N-1,N} = -\frac{C_D}{C_{TOT}} e \tag{2.21}
\end{aligned}$$

Similarly, the change in the charge stored in the tunnel junction between the island and the source electrode when the electron occupancy in the Coulomb island changes from N to $N - 1$ is given by:

$$\begin{aligned}
\Delta Q_S^{N-1,N} &= Q_S^{N-1} - Q_S^N \\
&= \frac{C_S}{C_{TOT}} [C_D V_{DS} - \{(N-1)e - Q_0\}] - \frac{C_S}{C_{TOT}} [C_D V_{DS} - \{Ne - Q_0\}] \\
&= \frac{C_S}{C_{TOT}} [C_D V_{DS} - Ne + e + Q_0 - C_D V_{DS} + Ne - Q_0] \\
&\therefore \Delta Q_S^{N-1,N} = \frac{C_S}{C_{TOT}} e \tag{2.22}
\end{aligned}$$

The work done by the voltage sources if an electron is added to the Coulomb island from the drain electrode is:

$$\begin{aligned}
\Delta W_D^+ &= [\Delta Q_D^{N+1,N} \cdot V_D - eV_D] + \Delta Q_S^{N+1,N} \cdot (-V_S) \\
\Rightarrow \Delta W_D^+ &= \frac{C_D}{C_{TOT}} eV_D - eV_D + \frac{C_S}{C_{TOT}} eV_S
\end{aligned}$$

$$\begin{aligned}
\Rightarrow \Delta W_D^+ &= eV_D \left[\frac{C_D}{C_{TOT}} - 1 \right] + \frac{C_S}{C_{TOT}} eV_S \\
\Rightarrow \Delta W_D^+ &= eV_D \left[\frac{C_D - C_S - C_D}{C_{TOT}} \right] + \frac{C_S}{C_{TOT}} eV_S \\
\Rightarrow \Delta W_D^+ &= -\frac{C_S}{C_{TOT}} eV_D + \frac{C_S}{C_{TOT}} eV_S \\
\Rightarrow \Delta W_D^+ &= -\frac{C_S}{C_{TOT}} e(V_D - V_S) \\
\therefore \Delta W_D^+ &= -\frac{C_S}{C_{TOT}} eV_{DS} \tag{2.23}
\end{aligned}$$

The total work done by the voltage sources if an electron is subtracted from the Coulomb island to the drain electrode is:

$$\begin{aligned}
\Delta W_D^- &= [\Delta Q_D^{N-1,N} \cdot V_D + eV_D] + \Delta Q_S^{N-1,N} \cdot (-V_S) \\
\Rightarrow \Delta W_D^- &= -\frac{C_D}{C_{TOT}} eV_D + eV_D - \frac{C_S}{C_{TOT}} eV_S \\
\Rightarrow \Delta W_D^- &= -eV_D \left[\frac{C_D}{C_{TOT}} - 1 \right] - \frac{C_S}{C_{TOT}} eV_S \\
\Rightarrow \Delta W_D^- &= -eV_D \left[\frac{C_D - C_S - C_D}{C_{TOT}} \right] - \frac{C_S}{C_{TOT}} eV_S \\
\Rightarrow \Delta W_D^- &= \frac{C_S}{C_{TOT}} eV_D - \frac{C_S}{C_{TOT}} eV_S \\
\Rightarrow \Delta W_D^- &= \frac{C_S}{C_{TOT}} e(V_D - V_S) \\
\therefore \Delta W_D^- &= \frac{C_S}{C_{TOT}} eV_{DS} \tag{2.24}
\end{aligned}$$

The total work done by the voltage sources if an electron is added to the Coulomb island from the source electrode is:

$$\begin{aligned}
\Delta W_S^+ &= [\Delta Q_S^{N+1,N} \cdot (-V_S) - eV_S] + \Delta Q_D^{N+1,N} \cdot V_D \\
\Rightarrow \Delta W_S^+ &= \frac{C_S}{C_{TOT}} eV_S - eV_S + \frac{C_D}{C_{TOT}} eV_D \\
\Rightarrow \Delta W_S^+ &= eV_S \left[\frac{C_S}{C_{TOT}} - 1 \right] + \frac{C_D}{C_{TOT}} eV_D \\
\Rightarrow \Delta W_S^+ &= eV_S \left[\frac{C_S - C_S - C_D}{C_{TOT}} \right] + \frac{C_D}{C_{TOT}} eV_D \\
\Rightarrow \Delta W_S^+ &= -\frac{C_D}{C_{TOT}} eV_S + \frac{C_D}{C_{TOT}} eV_D \\
\Rightarrow \Delta W_S^+ &= \frac{C_D}{C_{TOT}} e(V_D - V_S) \\
\therefore \Delta W_S^+ &= \frac{C_D}{C_{TOT}} eV_{DS} \tag{2.25}
\end{aligned}$$

The total work done by the voltage sources if an electron is subtracted from the Coulomb island to the source electrode is:

$$\begin{aligned}
\Delta W_S^- &= [\Delta Q_S^{N-1,N} \cdot (-V_S) + eV_S] + \Delta Q_D^{N-1,N} \cdot V_D \\
\Rightarrow \Delta W_S^- &= -\frac{C_S}{C_{TOT}} eV_S + eV_S - \frac{C_D}{C_{TOT}} eV_D \\
\Rightarrow \Delta W_S^- &= -eV_S \left[\frac{C_S}{C_{TOT}} - 1 \right] - \frac{C_D}{C_{TOT}} eV_D \\
\Rightarrow \Delta W_S^- &= -eV_S \left[\frac{C_S - C_S - C_D}{C_{TOT}} \right] - \frac{C_D}{C_{TOT}} eV_D
\end{aligned}$$

$$\begin{aligned}\Rightarrow \Delta W_S^- &= \frac{C_D}{C_{TOT}} eV_S - \frac{C_D}{C_{TOT}} eV_D \\ \Rightarrow \Delta W_S^- &= -\frac{C_D}{C_{TOT}} e(V_D - V_S) \\ \therefore \Delta W_S^- &= -\frac{C_D}{C_{TOT}} eV_{DS}\end{aligned}\tag{2.26}$$

From equations (2.23), (2.24), (2.25), and (2.26), we can see that the work done by the voltage sources in adding or subtracting an electron to or from the Coulomb island is independent of the number of electrons originally residing in the island. Therefore, if N_S number of electrons tunnel into the island from the source electrode as shown in Figure 2.3, the total work done by the voltage sources will be:

$$N_S \cdot W_S^+ = N_S \frac{C_D}{C_{TOT}} eV_{DS}\tag{2.27}$$

and if N_D number of electrons tunnel out of the island to the drain electrode as shown in Figure 2.3, the total work done by the voltage sources will be:

$$N_D \cdot W_D^- = N_D \frac{C_S}{C_{TOT}} eV_{DS}\tag{2.28}$$

Combining equations (2.14), (2.27) and (2.28), we get the free energy of a double junction single-electron device system $F(N_S, N_D)$ corresponding to the schematic shown in Figure 2.3 as the difference between the electrostatic energy of the system and the work done by the voltage sources:

$$\begin{aligned}F(N_S, N_D) &= E_{TOT} - (N_S \cdot W_S^+) - (N_D \cdot W_D^-) \\ &= \frac{1}{2C_{TOT}} \left[C_S C_D V_{DS}^2 + (Ne - Q_0)^2 \right] - N_S \frac{C_D}{C_{TOT}} eV_{DS} - N_D \frac{C_S}{C_{TOT}} eV_{DS}\end{aligned}$$

$$\boxed{\therefore F(N_S, N_D) = \frac{1}{2C_{TOT}} \left[C_S C_D V_{DS}^2 + (Ne - Q_0)^2 \right] - \frac{eV_{DS}}{C_{TOT}} (C_D N_S + C_S N_D)} \quad (2.29)$$

2.3.1 Coulomb blockade in a double junction single-electron device

We may now look at the condition for Coulomb blockade based on the change in the free energy with the tunneling of an electron through either junction.

Consider the case when an electron tunnels into the Coulomb island from the source electrode changing the electron occupancy in the island from N to $N + 1$. The change in the electrostatic energy of the system due to this event is given by equation (2.15). The work done by the voltage sources to make this electron tunnel is given by equation (2.25). Combining these two equations, we get the change in the free energy of a double junction single-electron device when an electron is added to the island as:

$$\begin{aligned} \Delta F_S^+ &= \Delta E_{TOT}^+ - \Delta W_S^+ \\ \Rightarrow \Delta F_S^+ &= \frac{e}{C_{TOT}} \left[\frac{e}{2} + (Ne - Q_0) - C_D V_{DS} \right] \end{aligned} \quad (2.30)$$

Similarly, if the electron occupancy in the island changes from N to $N - 1$ as a result of an electron tunneling out of the island to the source electrode, the change in the free energy of the device is obtained by subtracting equation (2.26) from equation (2.16). This gives:

$$\begin{aligned} \Delta F_S^- &= \Delta E_{TOT}^- - \Delta W_S^- \\ \Rightarrow \Delta F_S^- &= \frac{e}{C_{TOT}} \left[\frac{e}{2} - (Ne - Q_0) + C_D V_{DS} \right] \end{aligned} \quad (2.31)$$

Combining equation (2.30) and equation (2.31), we get:

$$\boxed{\Delta F_S^\pm = \frac{e}{C_{TOT}} \left[\frac{e}{2} \pm (Ne - Q_0) \mp C_D V_{DS} \right]} \quad (2.32)$$

The electron occupancy in the island can also change from N to $N+1$ as a result of an electron tunneling into the island from the drain electrode. In this case, the change in the electrostatic energy of the system is given by equation (2.15) and the work done by the voltage sources by equation (2.23). Combining these, we get the free energy of the system when an electron is added to the island from the drain electrode as:

$$\begin{aligned}\Delta F_D^+ &= \Delta E_{TOT}^+ - \Delta W_D^+ \\ \Rightarrow \Delta F_D^+ &= \frac{e}{C_{TOT}} \left[\frac{e}{2} + (Ne - Q_0) + C_S V_{DS} \right]\end{aligned}\quad (2.33)$$

Similarly, if an electron tunnels out of the island to the drain electrode, the change in the free energy is given by equations (2.26) and (2.24) as:

$$\begin{aligned}\Delta F_D^- &= \Delta E_{TOT}^- - \Delta W_D^- \\ \Rightarrow \Delta F_D^- &= \frac{e}{C_{TOT}} \left[\frac{e}{2} - (Ne - Q_0) - C_S V_{DS} \right]\end{aligned}\quad (2.34)$$

Combining equations (2.33) and (2.34), we get:

$$\boxed{\Delta F_D^\pm = \frac{e}{C_{TOT}} \left[\frac{e}{2} \pm (Ne - Q_0) \pm C_S V_{DS} \right]}\quad (2.35)$$

It must be mentioned here that the number of excess electrons in the Coulomb island N in equations (2.32) and (2.35) is such that N is an integer which is nearest to Q_0/e i.e., $|Q_0| \leq e/2$.

For a double junction single-electron device where the island is initially free of excess electrons, i.e., $N = 0$, equation (2.32) reduces to:

$$\Delta F_S^\pm = \frac{e}{C_{TOT}} \left[\frac{e}{2} \pm (-Q_0) \mp C_D V_{DS} \right]$$

$$\Rightarrow \Delta F_S^\pm = \frac{e}{C_{TOT}} \left[\frac{e}{2} \mp (C_D V_{DS} + Q_0) \right] \quad (2.36)$$

and equation (2.35) reduces to:

$$\begin{aligned} \Delta F_D^\pm &= \frac{e}{C_{TOT}} \left[\frac{e}{2} \pm (-Q_0) \pm C_S V_{DS} \right] \\ \Rightarrow \Delta F_D^\pm &= \frac{e}{C_{TOT}} \left[\frac{e}{2} \pm (C_S V_{DS} - Q_0) \right] \end{aligned} \quad (2.37)$$

In a single-electron device, electron tunneling can only take place if the system free energy reduces as a result of the tunneling event. Therefore, from equations (2.36) and (2.37) the conditions for no tunneling to occur in a double junction single-electron device become:

$$\Delta F_S^\pm = \frac{e}{C_{TOT}} \left[\frac{e}{2} \mp (C_D V_{DS} + Q_0) \right] > 0 \quad (2.38) \text{ (a)}$$

and

$$\Delta F_D^\pm = \frac{e}{C_{TOT}} \left[\frac{e}{2} \pm (C_S V_{DS} - Q_0) \right] > 0 \quad (2.38) \text{ (b)}$$

If $\Delta F_S^+ = \frac{e}{C_{TOT}} \left[\frac{e}{2} - (C_D V_{DS} + Q_0) \right] > 0$, then,

$$V_{DS} < \frac{\frac{e}{2} - Q_0}{C_D} \quad (2.39) \text{ (a)}$$

If $\Delta F_S^- = \frac{e}{C_{TOT}} \left[\frac{e}{2} + (C_D V_{DS} + Q_0) \right] > 0$, then,

$$\frac{-\frac{e}{2} - Q_0}{C_D} < V_{DS} \quad (2.39) \text{ (b)}$$

If $\Delta F_D^+ = \frac{e}{C_{TOT}} \left[\frac{e}{2} + (C_S V_{DS} - Q_0) \right] > 0$, then,

$$\frac{-\frac{e}{2} + Q_0}{C_S} < V_{DS} \quad (2.39) \text{ (c)}$$

and if $\Delta F_D^- = \frac{e}{C_{TOT}} \left[\frac{e}{2} - (C_S V_{DS} - Q_0) \right] > 0$, then,

$$V_{DS} < \frac{\frac{e}{2} + Q_0}{C_S} \quad (2.39) \text{ (d)}$$

Equation (2.39) implies that four different inequalities have to be satisfied simultaneously to obtain the condition for Coulomb blockade in a double junction single-electron device. The four different cases are elaborated below:

Case (a): If $\frac{-\frac{e}{2} - Q_0}{C_D} < \frac{-\frac{e}{2} + Q_0}{C_S}$ and $\frac{\frac{e}{2} - Q_0}{C_D} < \frac{\frac{e}{2} + Q_0}{C_S}$, then the Coulomb blockade occurs

$$\text{between } \frac{-\frac{e}{2} + Q_0}{C_S} < V_{DS} < \frac{\frac{e}{2} - Q_0}{C_D}. \quad (2.40) \text{ (a)}$$

Case (b): If $\frac{-\frac{e}{2} - Q_0}{C_D} < \frac{-\frac{e}{2} + Q_0}{C_S}$ and $\frac{\frac{e}{2} - Q_0}{C_D} > \frac{\frac{e}{2} + Q_0}{C_S}$, then the Coulomb blockade occurs

$$\text{between } \frac{-\frac{e}{2} + Q_0}{C_S} < V_{DS} < \frac{\frac{e}{2} + Q_0}{C_S}. \quad (2.40) \text{ (b)}$$

Case (c): If $\frac{-\frac{e}{2} - Q_0}{C_D} > \frac{-\frac{e}{2} + Q_0}{C_S}$ and $\frac{\frac{e}{2} - Q_0}{C_D} < \frac{\frac{e}{2} + Q_0}{C_S}$, then the Coulomb blockade occurs

$$\text{between } \frac{-\frac{e}{2} - Q_0}{C_D} < V_{DS} < \frac{\frac{e}{2} - Q_0}{C_D}. \quad (2.40) \text{ (c)}$$

Case (d): If $\frac{-\frac{e}{2}-Q_0}{C_D} > \frac{-\frac{e}{2}+Q_0}{C_S}$ and $\frac{\frac{e}{2}-Q_0}{C_D} > \frac{\frac{e}{2}+Q_0}{C_S}$, then the Coulomb blockade occurs

$$\text{between } \frac{-\frac{e}{2}-Q_0}{C_D} < V_{DS} < \frac{\frac{e}{2}+Q_0}{C_S}. \quad (2.40) \text{ (d)}$$

For $0 < Q_0 < \frac{e}{2}$ or $-\frac{e}{2} < Q_0 < 0$, equations (2.39) (a) and (2.39) (d) are always positive and equations (2.39) (b) and (2.39) (c) are always negative.

From Case (a),

$$\frac{-\frac{e}{2}-Q_0}{C_D} < \frac{-\frac{e}{2}+Q_0}{C_S}$$

$$\Rightarrow \frac{-\frac{e}{2}-Q_0}{-\frac{e}{2}+Q_0} > \frac{C_D}{C_S} \quad (2.41) \text{ (a)}$$

and

$$\frac{\frac{e}{2}-Q_0}{C_D} < \frac{\frac{e}{2}+Q_0}{C_S}$$

$$\Rightarrow \frac{\frac{e}{2}-Q_0}{\frac{e}{2}+Q_0} < \frac{C_D}{C_S} \quad (2.41) \text{ (b)}$$

From Case (b),

$$\frac{-\frac{e}{2}-Q_0}{C_D} < \frac{-\frac{e}{2}+Q_0}{C_S}$$

$$\Rightarrow \frac{-\frac{e}{2}-Q_0}{-\frac{e}{2}+Q_0} > \frac{C_D}{C_S} \quad (2.41) \text{ (c)}$$

and

$$\frac{\frac{e}{2} - Q_0}{C_D} > \frac{\frac{e}{2} + Q_0}{C_S}$$
$$\Rightarrow \frac{\frac{e}{2} - Q_0}{\frac{e}{2} + Q_0} > \frac{C_D}{C_S} \quad (2.41) \text{ (d)}$$

From Case (c),

$$\frac{-\frac{e}{2} - Q_0}{C_D} > \frac{-\frac{e}{2} + Q_0}{C_S}$$
$$\Rightarrow \frac{-\frac{e}{2} - Q_0}{-\frac{e}{2} + Q_0} < \frac{C_D}{C_S} \quad (2.41) \text{ (e)}$$

and

$$\frac{\frac{e}{2} - Q_0}{C_D} < \frac{\frac{e}{2} + Q_0}{C_S}$$
$$\Rightarrow \frac{\frac{e}{2} - Q_0}{\frac{e}{2} + Q_0} < \frac{C_D}{C_S} \quad (2.41) \text{ (f)}$$

From Case (d),

$$\frac{-\frac{e}{2} - Q_0}{C_D} > \frac{-\frac{e}{2} + Q_0}{C_S}$$
$$\Rightarrow \frac{-\frac{e}{2} - Q_0}{-\frac{e}{2} + Q_0} < \frac{C_D}{C_S} \quad (2.41) \text{ (g)}$$

and

$$\frac{\frac{e}{2} - Q_0}{C_D} > \frac{\frac{e}{2} + Q_0}{C_S}$$

$$\Rightarrow \frac{\frac{e}{2} - Q_0}{\frac{e}{2} + Q_0} > \frac{C_D}{C_S} \quad (2.41) \text{ (h)}$$

The two inequalities in Case (a) can be represented by the area marked Case (a) in Figure 2.4. This area is obtained by simultaneously solving the inequalities given by equations (2.41) (a) and (2.41) (b). The width of the Coulomb blockade ΔV_{DS} is obtained from equation (2.40) (a) as:

$$\Delta V_{DS} = \frac{\frac{e}{2} - Q_0}{C_D} - \frac{-\frac{e}{2} + Q_0}{C_S}$$

$$\Rightarrow \Delta V_{DS} = \frac{C_S \left(\frac{e}{2} - Q_0 \right) - C_D \left(-\frac{e}{2} + Q_0 \right)}{C_S C_D}$$

$$\Rightarrow \Delta V_{DS} = \frac{C_S \frac{e}{2} - C_S Q_0 + C_D \frac{e}{2} - C_D Q_0}{C_S C_D}$$

$$\Rightarrow \Delta V_{DS} = \frac{(C_S + C_D) \left(\frac{e}{2} - Q_0 \right)}{C_S C_D}$$

$$\therefore \Delta V_{DS} = \frac{(C_\Sigma) \left(\frac{e}{2} - Q_0 \right)}{C_S C_D} \quad (2.42) \text{ (a)}$$

The two inequalities in Case (b) can be represented by the area marked Case (b) in Figure 2.4. This area is obtained by simultaneously solving equations (2.41) (c) and (2.41) (d).

The width of the Coulomb blockade ΔV_{DS} is obtained from equation (2.40) (b) as:

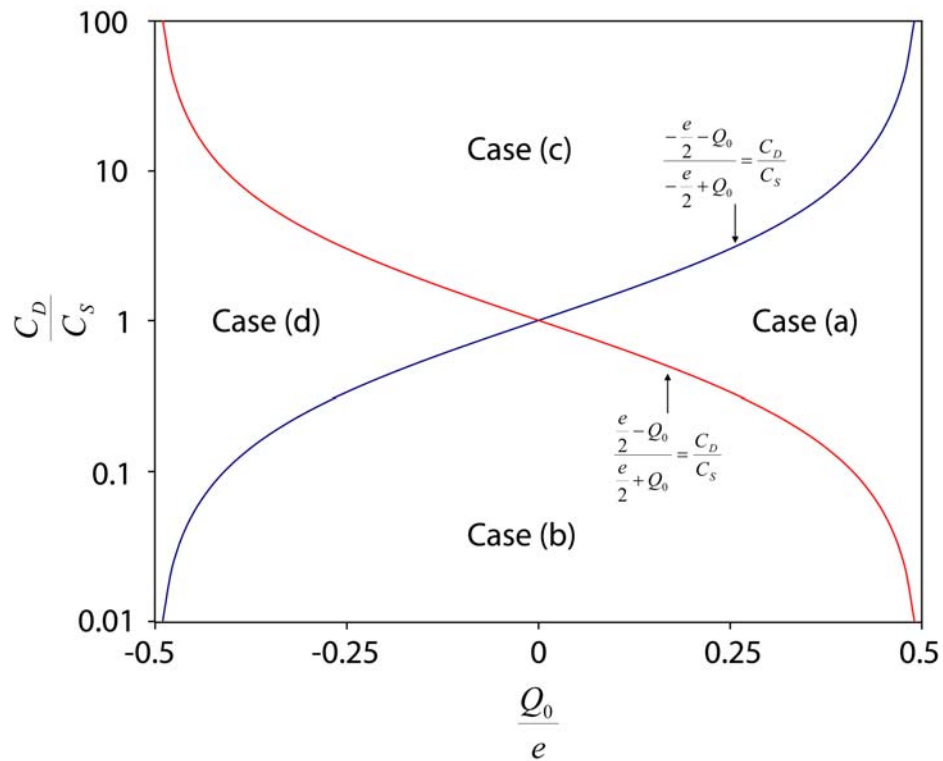


Figure 2.4 Numerically plotted $\frac{C_D}{C_S}$ vs $\frac{Q_0}{e}$ curves for Cases (a) – (d) described by equations (2.40) (a) – (d) in Section 2.3.1. These curves are obtained by solving the inequalities derived in equations (2.41) (a) – (h).

$$\begin{aligned}\Delta V_{DS} &= \frac{\frac{e}{2} + Q_0}{C_S} - \frac{-\frac{e}{2} + Q_0}{C_S} \\ \Rightarrow \Delta V_{DS} &= \frac{\frac{e}{2} + Q_0 + \frac{e}{2} - Q_0}{C_S} \\ \therefore \Delta V_{DS} &= \frac{e}{C_S}\end{aligned}\tag{2.42} (b)$$

The two inequalities in Case (c) can be represented by the area marked Case (c) in Figure 2.4. This area is obtained by simultaneously solving equations (2.41) (e) and (2.41) (f).

The width of the Coulomb blockade ΔV_{DS} is obtained from equation (2.40) (c) as:

$$\begin{aligned}\Delta V_{DS} &= \frac{\frac{e}{2} - Q_0}{C_D} - \frac{-\frac{e}{2} - Q_0}{C_D} \\ \Rightarrow \Delta V_{DS} &= \frac{\frac{e}{2} - Q_0 + \frac{e}{2} + Q_0}{C_D} \\ \therefore \Delta V_{DS} &= \frac{e}{C_D}\end{aligned}\tag{2.42} (c)$$

The two inequalities in Case (d) can be represented by the area marked Case (d) in Figure 2.4. This area is obtained by simultaneously solving the inequalities given by equations (2.41) (g) and (2.41) (h). The width of the Coulomb blockade ΔV_{DS} is obtained from equation (2.40) (d) as:

$$\Delta V_{DS} = \frac{\frac{e}{2} + Q_0}{C_S} - \frac{-\frac{e}{2} - Q_0}{C_D}$$

$$\Rightarrow \Delta V_{DS} = \frac{C_D \left(\frac{e}{2} + Q_0 \right) - C_S \left(-\frac{e}{2} - Q_0 \right)}{C_S C_D}$$

$$\Rightarrow \Delta V_{DS} = \frac{C_D \frac{e}{2} + C_D Q_0 + C_S \frac{e}{2} + C_S Q_0}{C_S C_D}$$

$$\Rightarrow \Delta V_{DS} = \frac{(C_S + C_D) \left(\frac{e}{2} + Q_0 \right)}{C_S C_D}$$

$$\therefore \Delta V_{DS} = \frac{(C_\Sigma) \left(\frac{e}{2} + Q_0 \right)}{C_S C_D} \quad (2.42) \text{ (d)}$$

From the results obtained from equations (2.42) (a) – (2.42) (d), the width of the Coulomb blockade ΔV_{DS} for Case (a) – Case (d) can be tabulated as follows:

Table 2.1 Width of the Coulomb blockade ΔV_{DS} for Cases (a) – (d).

Case	ΔV_{DS}
a	$\frac{(C_\Sigma) \left(\frac{e}{2} - Q_0 \right)}{C_S C_D}$
b	$\frac{e}{C_S}$
c	$\frac{e}{C_D}$
d	$\frac{(C_\Sigma) \left(\frac{e}{2} + Q_0 \right)}{C_S C_D}$

It can be seen from equations (2.42) (a) – (2.42) (d) that the Coulomb blockade in a double junction single-electron device depends on the parameters C_S , C_D , and Q_0 .

If $Q_0 = \frac{e}{2}$, then from equation (2.42) (a), the width of the Coulomb blockade is:

$$\Delta V_{DS} = \frac{(C_\Sigma) \left(\frac{e}{2} - \frac{e}{2} \right)}{C_S C_D}$$

$$\Rightarrow \Delta V_{DS} = 0$$

Therefore, no Coulomb blockade will be observed in devices where $Q_0 = \frac{e}{2}$.

If $Q_0 = -\frac{e}{2}$, then from equation (2.42) (d), the width of the Coulomb blockade is:

$$\Delta V_{DS} = \frac{(C_\Sigma) \left\{ \frac{e}{2} + \left(-\frac{e}{2} \right) \right\}}{C_S C_D}$$

$$\Rightarrow \Delta V_{DS} = 0$$

Therefore, no Coulomb blockade will be observed in devices where $Q_0 = -\frac{e}{2}$.

If $Q_0 = 0$, then from equation (2.42) (a),

$$\Delta V_{DS} = \frac{(C_\Sigma) \left(\frac{e}{2} \right)}{C_S C_D} \tag{2.43) (a)}$$

and from equation (2.42) (d),

$$\Delta V_{DS} = \frac{(C_\Sigma) \left(\frac{e}{2} \right)}{C_S C_D} \tag{2.43) (b)}$$

If $Q_0 = 0$ and $C_S = C_D = C$, then $C_\Sigma = C_S + C_D = 2C$. Therefore, the width of the Coulomb blockade from equations (2.43) (a) and (2.43) (b) becomes:

$$\Delta V_{DS} = \frac{(2C)\left(\frac{e}{2}\right)}{C^2}$$

$$\Rightarrow \Delta V_{DS} = \frac{e}{C} \quad (2.44)$$

If $Q_0 = 0$ and $C_S > C_D$, then from equation (2.42) (b),

$$\Delta V_{DS} = \frac{e}{C_S} \quad (2.45) \text{ (a)}$$

and for $Q_0 = 0$ and $C_D > C_S$, equation (2.42) (c) gives:

$$\Delta V_{DS} = \frac{e}{C_D} \quad (2.45) \text{ (b)}$$

Combining equations (2.45) (a) and (2.45) (b), we can say that for $Q_0 = 0$ and for different C_S and C_D :

$$\Delta V_{DS} = \frac{e}{\max(C_S, C_D)} \quad (2.46)$$

Figure 2.5 shows the simulated I-V characteristics of a double-junction single-electron device and the dependence of the Coulomb blockade for the various values of Q_0 . The simulation was done using $C_S = C_D = 3aF$ and $R_S = R_D = 8G\Omega$ at $T = 0K$. The three different values of Q_0 which were used for the simulation are $Q_0 = 0$ (Red), $Q_0 = \frac{e}{4}$ (Blue), and $Q_0 = \frac{e}{2}$ (Green).

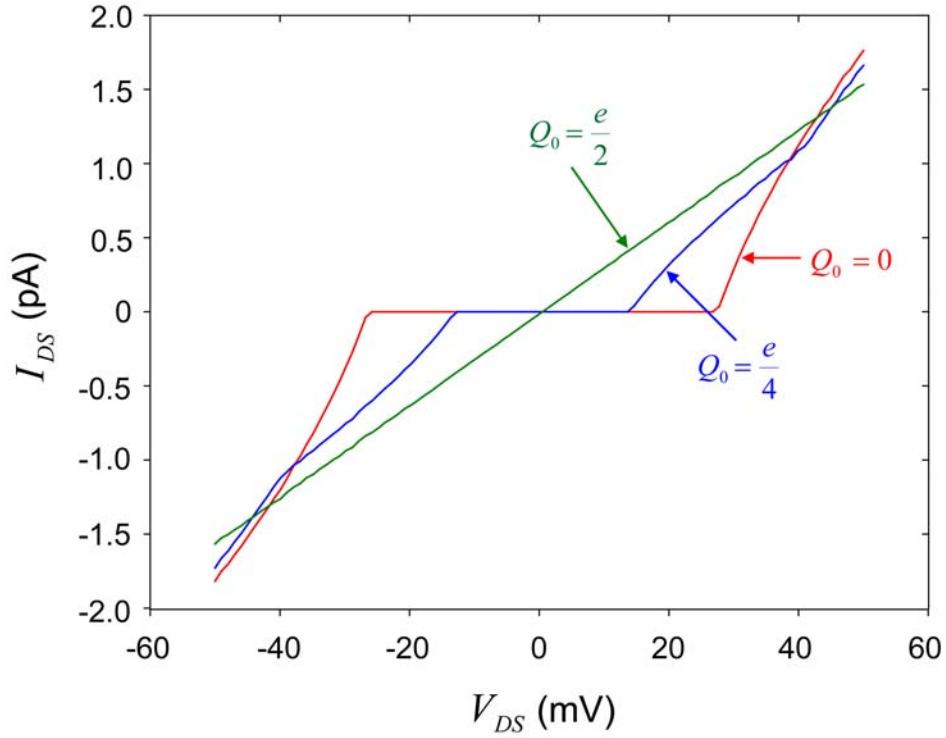


Figure 2.5 Simulated I-V characteristics of a double-junction single-electron device showing the effect of Q_0 on the width of the Coulomb blockade. Red: Simulated I-V characteristics of a double-junction single-electron device using $C_S = C_D = 3aF$, $R_S = R_D = 8G\Omega$, $Q_0 = 0$, and $T = 0K$. Blue: Simulated I-V characteristics of a double-junction single-electron device using $C_S = C_D = 3aF$, $R_S = R_D = 8G\Omega$, $Q_0 = \frac{e}{4}$, and $T = 0K$. Green: Simulated I-V characteristics of a double-junction single-electron device using $C_S = C_D = 3aF$, $R_S = R_D = 8G\Omega$, $Q_0 = \frac{e}{2}$, and $T = 0K$.

2.3.2 Coulomb staircase in a double junction single-electron device

If the double junction single-electron device is such that its tunnel junctions are asymmetric i.e., $R_S C_S \gg R_D C_D$ or $R_S C_S \ll R_D C_D$, then as V_{DS} is increased beyond the Coulomb blockade, the current rises in jumps giving a staircase like appearance as shown in Figures 2.7 and 2.8. This stepwise rise in the current of the single electron device with increasing source-drain bias is known as the *Coulomb staircase*. Each jump in the I-V characteristics corresponds to applied source-drain voltages where one more electron is added to or subtracted from the Coulomb island. Each plateau therefore corresponds to the stable regime with a fixed integer number of electrons in the island.

The Coulomb staircase in double junction single-electron devices can be qualitatively understood using the electrostatic potential diagrams of a device as shown in Figure 2.6. We assume a highly asymmetric device with $C_D > C_S$ and $R_D \gg R_S$ so that $R_D C_D \gg R_S C_S$. Initially, no voltage is applied across the device under which the Coulomb island is assumed to have N number of extra electrons in it as shown in Figure 2.6 (a).

The electrostatic potential of the island $\varphi_{IS}(N)$ having N number of excess electrons in it is given by equation (2.9) as:

$$\varphi_{IS}(N) = \frac{C_S V_S + C_D V_D - (Ne - Q_0)}{C_{TOT}}$$

If the electron occupancy in the island increases by one, then the resulting change in the electrostatic potential of the island $\Delta\varphi_{IS}^+$ is:

$$\begin{aligned} \Delta\varphi_{IS}^+ &= \varphi_{IS}(N+1) - \varphi_{IS}(N) \\ \Rightarrow \Delta\varphi_{IS}^+ &= \frac{C_S V_S + C_D V_D - \{(N+1)e - Q_0\}}{C_{TOT}} - \frac{C_S V_S + C_D V_D - \{Ne - Q_0\}}{C_{TOT}} \\ \therefore \Delta\varphi_{IS}^+ &= -\frac{e}{C_{TOT}} \end{aligned} \quad (2.47) \text{ (a)}$$

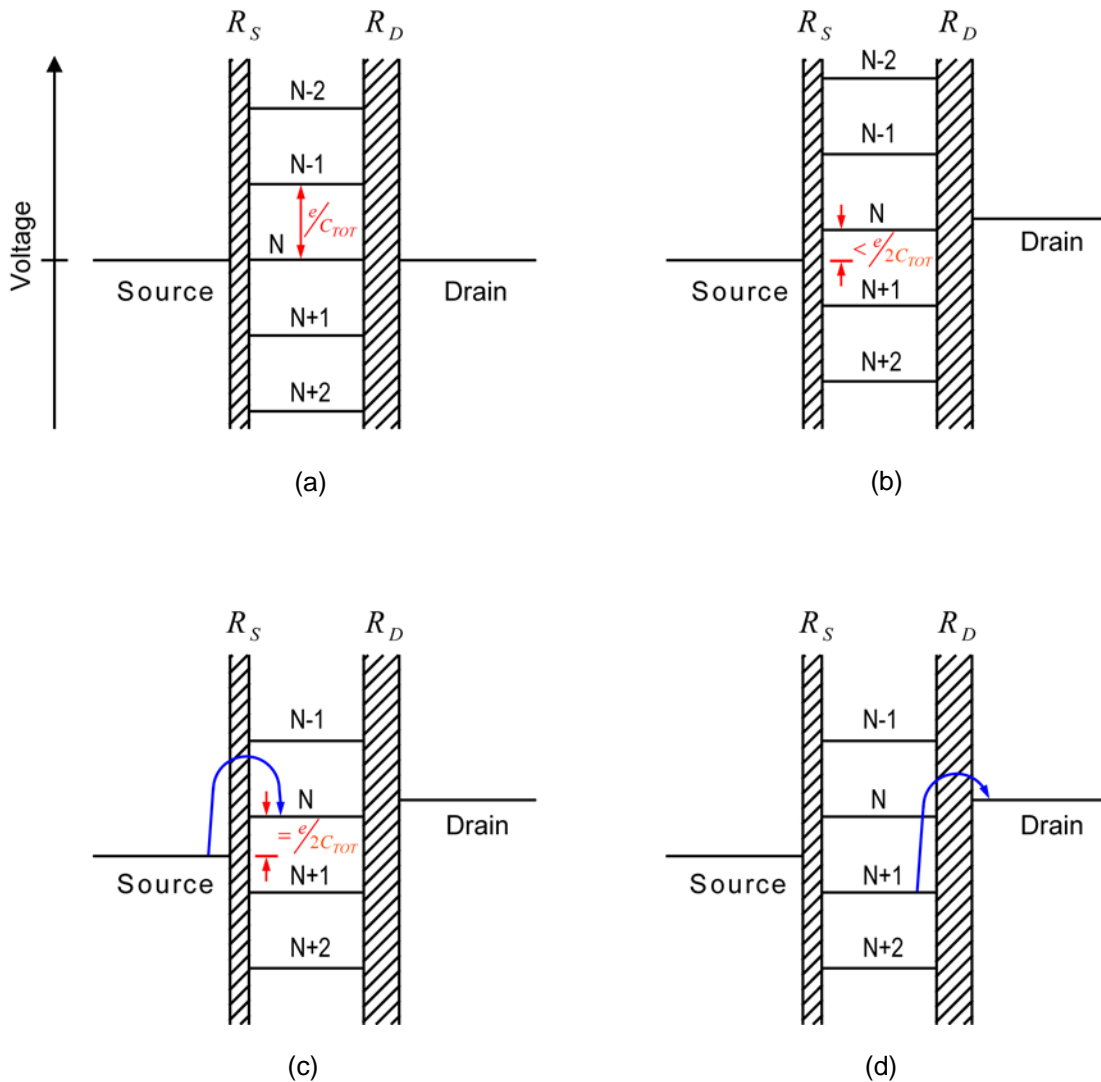


Figure 2.6 Schematic of the mechanism of current flow in an asymmetric ($C_D > C_S$ and $R_D \gg R_S$; $C_D R_D \gg C_S R_S$) double junction single-electron device. (a) When no source-drain bias is applied. (b) When a small source-drain bias is applied such that it is not enough to add an electron to the island. The device is under the Coulomb blockade regime. (c) Application of a suitable source-drain bias causes an electron to tunnel into the island from the source electrode. (d) The asymmetry causes the island to retain the extra electron till it can go back to the ground state when the electron tunnels out of the island into the drain electrode.

Similarly, if the electron occupancy in the island decreases by one, then the resulting change in the electrostatic potential of the island $\Delta\varphi_{IS}^-$ is:

$$\begin{aligned}\Delta\varphi_{IS}^- &= \varphi_{IS}(N-1) - \varphi_{IS}(N) \\ \Rightarrow \Delta\varphi_{IS}^- &= \frac{C_S V_S + C_D V_D - \{(N-1)e - Q_0\}}{C_{TOT}} - \frac{C_S V_S + C_D V_D - \{Ne - Q_0\}}{C_{TOT}} \\ \therefore \Delta\varphi_{IS}^- &= \frac{e}{C_{TOT}}\end{aligned}\tag{2.47} (b)$$

From equation (2.47), we can say that the addition or the subtraction of a single electron to or from the Coulomb island changes the electrostatic potential of the island by an amount $\frac{e}{C_{TOT}}$.

The voltage drop between the Coulomb island and the source electrode is given by equation (2.10) as:

$$\varphi_{IS} - V_S = \frac{C_D V_{DS}}{C_{TOT}} - \frac{(Ne - Q_0)}{C_{TOT}}$$

and the voltage drop between the drain electrode and the island is given by equation (2.11) as:

$$V_D - \varphi_{IS} = \frac{C_S V_{DS}}{C_{TOT}} + \frac{(Ne - Q_0)}{C_{TOT}}$$

Since for this device we have assumed that $C_D > C_S$, the term $\frac{C_D V_{DS}}{C_{TOT}}$ in $\varphi_{IS} - V_S$ of

equation (2.10) is larger than the term $\frac{C_S V_{DS}}{C_{TOT}}$ in $V_D - \varphi_{IS}$ of equation (2.11).

Assuming that the source electrode is grounded, when a positive source-drain voltage V_{DS} is applied, the potential of the island closely follows that of the drain electrode as shown in Figure 2.6 (b). Due to this, the voltage drop between the island and the source electrode is larger when compared to the voltage drop between the drain electrode and the island. As long

as the voltage drop between the island and the source electrode is less than $\frac{e}{2C_{TOT}}$, an electron cannot tunnel into the island from the source electrode. When the voltage drop between the island and the source electrode reaches $\frac{e}{2C_{TOT}}$, a single electron can tunnel into the island from the source electrode thereby increasing the electron occupancy in the island by one. The addition of the extra electron into the island causes the potential of the island to drop by an amount $\frac{e}{C_{TOT}}$. If a change in the voltage of ΔV_{DS} brought about the tunneling event from the source electrode to the island, then just before the tunneling of the electron from the source to the island occurred, the voltage drop between the island and the source from equation (2.10) is $\frac{C_D \Delta V_{DS}}{C_{TOT}}$. This voltage drop will be equal to the drop in the potential of the island due to the addition of the extra electron. Therefore:

$$\frac{C_D \Delta V_{DS}}{C_{TOT}} = \frac{e}{C_{TOT}}$$

$$\Rightarrow \Delta V_{DS} = \frac{e}{C_D} \quad (2.48)$$

As $R_D \gg R_S$ the time taken for this extra electron to tunnel out into the drain electrode from the Coulomb island is much larger compared to the time taken for an electron to tunnel into the island from the source electrode. Therefore, the island remains in the charged state for most of the time. As soon as an electron tunnels out of the island into the drain electrode (Figure 2.6 (d)), it is immediately replenished by another electron from the source electrode.

If the asymmetry of the double junction single-electron device is such that $C_D < C_S$ and $R_D \ll R_S$ so that $R_D C_D \ll R_S C_S$, then the term $\frac{C_S V_{DS}}{C_{TOT}}$ in $V_D - \phi_{IS}$ of equation (2.11)

will be larger than the term $\frac{C_D V_{DS}}{C_{TOT}}$ in $\phi_{IS} - V_S$ of equation (2.10). If the source electrode is

grounded and a positive source-drain bias V_{DS} is applied, the potential of the island will tend to remain closer to the source electrode. With increasing bias, the voltage drop between the drain and the island becomes larger compared to the voltage drop between the island and the source.

When the magnitude of this drop reaches $\frac{e}{2C_{TOT}}$, an electron from the island tunnels out into

the drain electrode. If a voltage change of ΔV_{DS} caused the electron to tunnel from the island to the drain, then the voltage drop between the drain and the island just before this tunneling

occurred from equation (2.11) is $\frac{C_S \Delta V_{DS}}{C_{TOT}}$. Equating this voltage drop to the shift up in the

potential of the island due to the removal of one electron, we get:

$$\begin{aligned} \frac{C_S \Delta V_{DS}}{C_{TOT}} &= \frac{e}{C_{TOT}} \\ \Rightarrow \Delta V_{DS} &= \frac{e}{C_S} \end{aligned} \quad (2.49)$$

Since we have assumed $R_S \gg R_D$ for this double junction single-electron device, the time taken for electrons to tunnel into the island from the source electrode is much larger than the time taken for them to tunnel out of the island into the drain. Therefore, island will continue to remain with a deficit of one electron till it is brought back to its original charge state when an electron tunnels into it from the source electrode.

From equations (2.48) and (2.49), the source-drain voltage range ΔV_{DS} over which the Coulomb island is most likely to have an integer number of electrons is:

$$\Delta V_{DS} = \frac{e}{C_D} \text{ if } C_D > C_S \quad (2.50) \text{ (a)}$$

or
$$\Delta V_{DS} = \frac{e}{C_S} \text{ if } C_S > C_D \quad (2.50) \text{ (b)}$$

Combining equations (2.50) (a) and (2.50) (b), the width of the plateau where the Coulomb island holds an integer number of electrons i.e., the width of the Coulomb staircase is:

$$\Delta V_{DS} = \frac{e}{\max(C_S, C_D)} \quad (2.51)$$

Figure 2.7 shows the simulated I-V characteristics of a double junction single electron device having asymmetric tunnel junctions. The simulation parameters are $C_S = 3aF$, $C_D = 30aF$, $R_S = 80M\Omega$, and $R_D = 8G\Omega$. Q_0 was taken to be zero and the simulation was done at $T = 0K$.

The Coulomb staircase can also be observed if the tunneling resistances R_S and R_D of the respective tunnel junctions are quite different. If $R_D \gg R_S$ with $C_S = C_D = C$, for example, then the rate of electron tunneling into the island through the barrier between the source and the island will be much faster than the electron tunneling rate from the island to the drain. This difference in the tunneling rate tends to maintain the number of electrons in the island at a fixed value. An electron tunneling into the island due to an increase in the source-drain bias will stay inside the island till it tunnels out into the drain, the time of residence in the island being determined by the tunneling rate between the Coulomb island and the drain electrode. As soon as this electron tunnels into the drain, it can be immediately replenished by another electron from the source. In such a case, the current in the device is controlled by the number of electrons tunneling out of the island into the drain electrode.

Starting from $N = 0$ (electrically neutral Coulomb island) and assuming that the background charge $Q_0 = 0$, the first plateau in the I-V characteristics from $V_{DS} = \frac{e}{2C}$ to $V_{DS} = \frac{3e}{2C}$ is the result of the sequence:

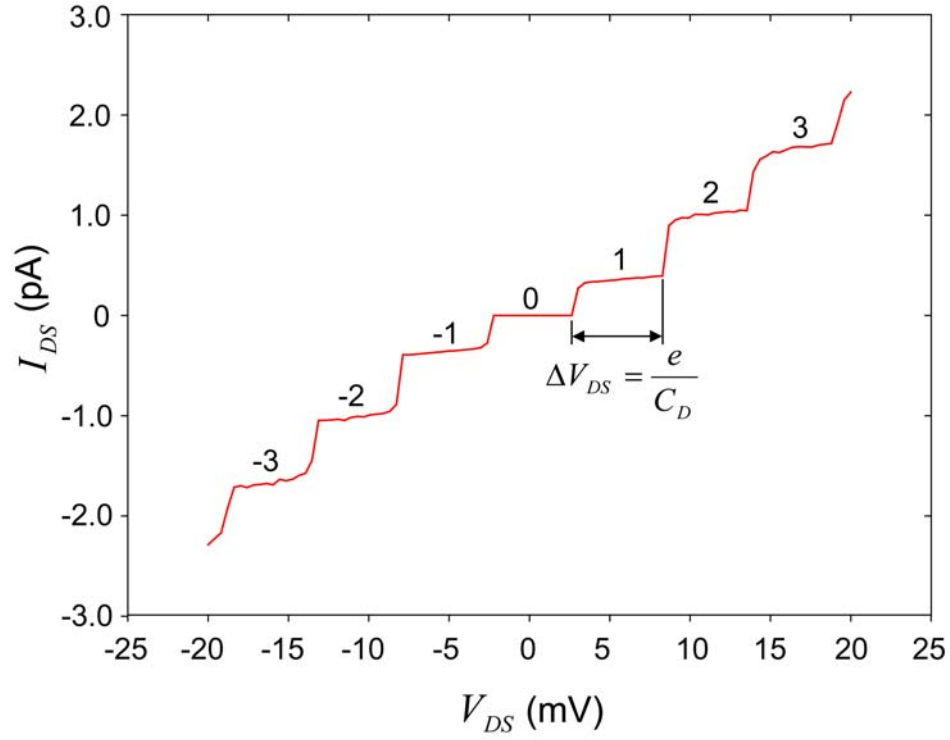


Figure 2.7 Simulated I-V characteristics of an asymmetric double junction single-electron device showing the existence of the Coulomb staircase. The simulation parameters are $C_S = 3aF$, $C_D = 30aF$, $R_S = 80M\Omega$, $R_D = 8G\Omega$ and $Q_0 = 0$. The simulation was done at $T = 0K$.

Since $C_D > C_S$, the width of the Coulomb staircase $\Delta V_{DS} = \frac{e}{C_D}$.

$$N = 0 \xrightarrow{\Gamma_S} N = 1 \xrightarrow{\Gamma_D} N = 0$$

where Γ_S^+ and Γ_D^- are the tunneling rates into the island from the source electrode and out of the island into the drain electrode, respectively. The $N = 0$ to $N = 1$ transition occurs much faster than $N = 1$ to $N = 0$ since $R_D \gg R_S$. The Coulomb island therefore remains in the $N = 1$ state for the majority of the time. The first plateau therefore corresponds to a net average number of extra electrons on the Coulomb island which is approximately equal to one. Figure 2.8 shows three simulated I-V characteristics of a double junction single-electron device in which $C_S = C_D = 3aF$ and $Q_0 = 0$ at $T = 0K$. $R_S = 80M\Omega$ for all three plots, $R_D = 240M\Omega$ (red line), $R_D = 400M\Omega$ (blue line), $R_D = 800M\Omega$ (green line).

The width of the Coulomb staircase can also be derived from the expressions for the change in the free energy of a double junction single-electron device when a single electron is added/subtracted to/from the Coulomb island. To obtain the width of the Coulomb staircase using the change in the free energy of the system, we consider the schematic of a Coulomb staircase as shown in Figure 2.9 (a). Beyond the Coulomb blockade, electrons are added to or subtracted from the Coulomb island one at a time so that the plateaus correspond to a fixed integer number of electrons in the island.

Since the necessary condition for the observation of a Coulomb staircase is asymmetric tunnel junction configuration, we will first consider an asymmetric tunnel junction which has $C_D > C_S$ and $R_D \gg R_S$ such that $C_D R_D \gg C_S R_S$ as shown in Figure 2.9 (b). The voltage drop between the Coulomb island and the source electrode is given by equation (2.10) as:

$$\varphi_{IS} - V_S = \frac{C_D V_{DS}}{C_{TOT}} - \frac{(Ne - Q_0)}{C_{TOT}}$$

and the voltage drop between the drain electrode and the island is given by equation (2.11) as:

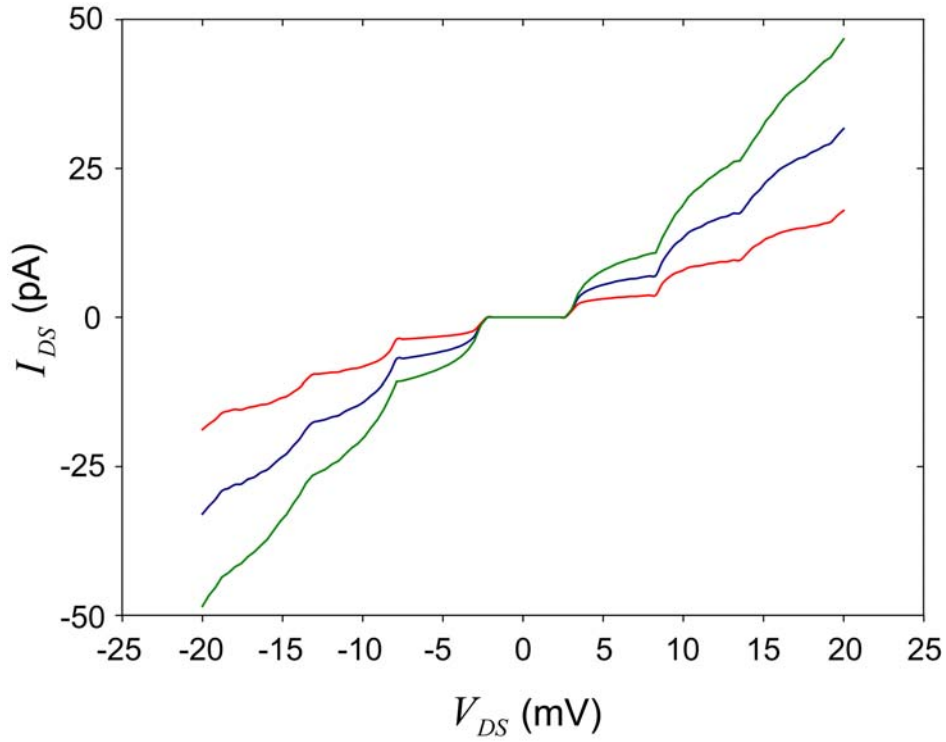


Figure 2.8 Simulated I-V characteristics of an asymmetric double junction single-electron device showing the presence of a Coulomb staircase. The asymmetry is formed by keeping $C_S = C_D = C$ and $R_D \gg R_S$ such that $R_D C_D \gg R_S C_S$. The simulation parameters are: Red: $C_S = C_D = 3aF$, $R_S = 80M\Omega$, $R_D = 240M\Omega$, $Q_0 = 0$, and $T = 0K$. Blue: $C_S = C_D = 3aF$, $R_S = 80M\Omega$, $R_D = 400M\Omega$, $Q_0 = 0$, and $T = 0K$. Green: $C_S = C_D = 3aF$, $R_S = 80M\Omega$, $R_D = 800M\Omega$, $Q_0 = 0$, and $T = 0K$.

$$V_D - \varphi_{IS} = \frac{C_S V_{DS}}{C_{TOT}} + \frac{(Ne - Q_0)}{C_{TOT}}$$

As $C_D > C_S$, the term $\frac{C_D V_{DS}}{C_{TOT}}$ in $\varphi_{IS} - V_S$ is much larger than the term $\frac{C_S V_{DS}}{C_{TOT}}$ in $V_D - \varphi_{IS}$.

Assuming that the source electrode is grounded, when a positive source-drain voltage V_{DS} is applied, the potential of the island closely follows that of the drain electrode as shown in Figure 2.9 (b). Due to this, the voltage drop between the island and the source electrode is much larger when compared to the voltage drop between the drain electrode and the island.

When the voltage drop between the island and the source electrode reaches $\frac{e}{2C_{TOT}}$, a single

electron can tunnel into the island from the source electrode thereby increasing the electron occupancy in the island by unity. In terms of the change in the free energy of the double junction single-electron device, this event can be represented as:

$$\Delta F_s^+(0 \rightarrow 1) < 0$$

From equation (2.30), $\Delta F_s^+ = \frac{e}{C_{TOT}} \left[\frac{e}{2} + (Ne - Q_0) - C_D V_{DS} \right]$. Substituting $N = 0$ in

equation (2.30) and solving the inequality $\Delta F_s^+(0 \rightarrow 1) < 0$ gives:

$$\frac{e}{C_{TOT}} \left[\frac{e}{2} + (0e - Q_0) - C_D V_{DS} \right] < 0$$

$$\Rightarrow \frac{e}{2} - Q_0 - C_D V_{DS} < 0$$

$$\Rightarrow \frac{e}{2} - Q_0 < C_D V_{DS}$$

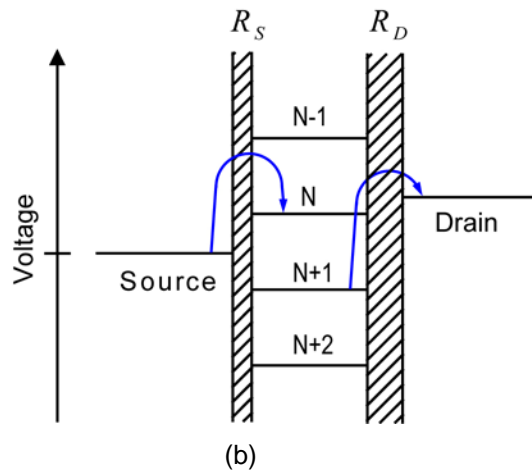
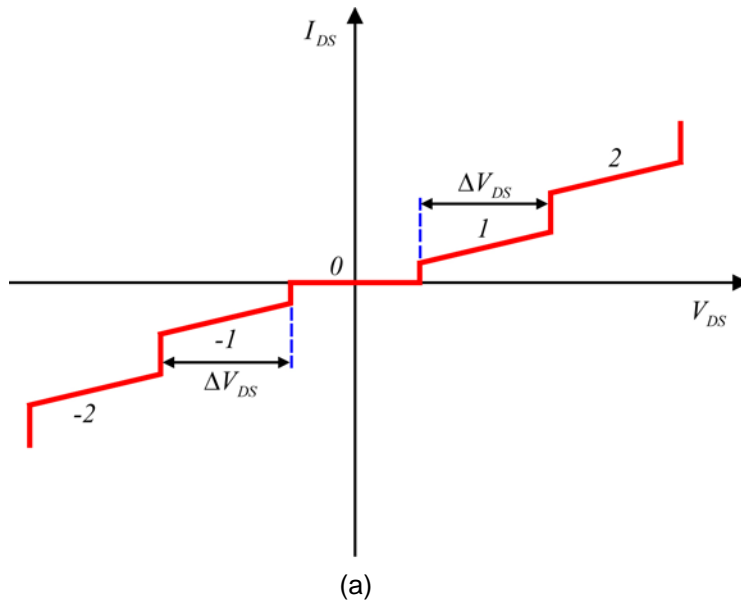


Figure 2.9 Schematic of Coulomb staircase in an asymmetric double junction single-electron device with $C_D > C_S$ and $R_D \gg R_S$ such that $C_D R_D \gg C_S R_S$. (a) Schematic of the $I_{DS} - V_{DS}$ characteristics showing electron occupancy in the Coulomb island as a function of the applied source-drain bias V_{DS} . (b) The voltage diagram of this device depicting the sequence of electron tunneling into and out of the island for a positive applied V_{DS} .

$$\therefore V_{DS} > \frac{\frac{e}{2} - Q_0}{C_D} \quad (2.52) \text{ (a)}$$

Since the resistances of the tunnel junctions are such that $R_D \gg R_S$, the rate of electrons tunneling into the island from the source electrode is must faster than the rate of electrons tunneling out of the island into the drain electrode. Therefore, the electron which had tunneled into the island from the source electrode will remain inside the island till it can tunnel out into the drain electrode. Once it tunnels out of the island, the electron occupancy inside the island goes back to its original charge state. The change in the free energy of the device due to this event is:

$$\Delta F_D^-(1 \rightarrow 0) < 0$$

From equation (2.34), $\Delta F_D^- = \frac{e}{C_{TOT}} \left[\frac{e}{2} - (Ne - Q_0) - C_S V_{DS} \right]$. Substituting $N = 1$ in equation

(2.34) and solving the inequality $\Delta F_D^-(1 \rightarrow 0) < 0$ gives:

$$\frac{e}{C_{TOT}} \left[\frac{e}{2} - (1e - Q_0) - C_S V_{DS} \right] < 0$$

$$\Rightarrow -\frac{e}{2} + Q_0 - C_S V_{DS} < 0$$

$$\Rightarrow -C_S V_{DS} < \frac{e}{2} - Q_0$$

$$\therefore V_{DS} > \frac{-\frac{e}{2} + Q_0}{C_S} \quad (2.52) \text{ (b)}$$

For the plateau region corresponding to one excess electron in the Coulomb island as shown in Figure 2.9 (a), the applied source-drain bias is not sufficient to add a second extra electron into the island. Therefore,

$$\Delta F_s^+(1 \rightarrow 2) > 0$$

$$\Rightarrow \frac{e}{C_{TOT}} \left[\frac{e}{2} + (1e - Q_0) - C_D V_{DS} \right] > 0$$

$$\Rightarrow \frac{3e}{2} - Q_0 - C_D V_{DS} > 0$$

$$\Rightarrow \frac{3e}{2} - Q_0 > C_D V_{DS}$$

$$\therefore V_{DS} < \frac{\frac{3e}{2} - Q_0}{C_D} \quad (2.52) \text{ (c)}$$

For $|Q_0| < \frac{e}{2}$, $\frac{e}{2} - Q_0$ from equation (2.52) (a) is always larger than $-\frac{e}{2} + Q_0$ from

equation (2.52) (b). Therefore, from equations (2.52) (a), (2.52) (b), and (2.52) (c), the source-drain voltage range for which the Coulomb island will be stable with a maximum of $N = 1$ electrons is:

$$\frac{\frac{e}{2} - Q_0}{C_D} < V_{DS} < \frac{\frac{3e}{2} - Q_0}{C_D} \quad (2.53)$$

For this asymmetric double junction single-electron device, if the source-drain voltage is further increased, a second excess electron can be added to the Coulomb island from the source electrode. In terms of the change in the free energy of the device this event is:

$$\Delta F_s^+(1 \rightarrow 2) < 0$$

$$\Rightarrow \frac{e}{C_{TOT}} \left[\frac{e}{2} + (1e - Q_0) - C_D V_{DS} \right] < 0$$

$$\Rightarrow \frac{3e}{2} - Q_0 - C_D V_{DS} < 0$$

$$\Rightarrow \frac{3e}{2} - Q_0 < C_D V_{DS}$$

$$\therefore V_{DS} > \frac{\frac{3e}{2} - Q_0}{C_D} \quad (2.54) \text{ (a)}$$

At this voltage, $\Delta F_S^+(0 \rightarrow 1)$ is also possible. Therefore:

$$V_{DS} > \frac{\frac{e}{2} - Q_0}{C_D} \quad (2.54) \text{ (b)}$$

Since a third extra electron cannot be added to the island at this particular source-drain bias,

$$\Delta F_S^+(2 \rightarrow 3) > 0$$

$$\Rightarrow \frac{e}{C_{TOT}} \left[\frac{e}{2} + (2e - Q_0) - C_D V_{DS} \right] > 0$$

$$\Rightarrow \frac{5e}{2} - Q_0 - C_D V_{DS} > 0$$

$$\Rightarrow \frac{5e}{2} - Q_0 > C_D V_{DS}$$

$$\therefore V_{DS} < \frac{\frac{5e}{2} - Q_0}{C_D} \quad (2.54) \text{ (c)}$$

At this voltage, an electron can tunnel out from the island into the drain electrode so that:

$$\Delta F_D^-(2 \rightarrow 1) < 0$$

$$\Rightarrow \frac{e}{C_{TOT}} \left[\frac{e}{2} - (2e - Q_0) - C_S V_{DS} \right] < 0$$

$$\Rightarrow -\frac{3e}{2} + Q_0 - C_S V_{DS} < 0$$

$$\Rightarrow -C_S V_{DS} < \frac{3e}{2} - Q_0$$

$$\therefore V_{DS} > \frac{-\frac{3e}{2} + Q_0}{C_S} \quad (2.54) \text{ (d)}$$

and $\Delta F_D^-(1 \rightarrow 0) < 0$

$$\Rightarrow V_{DS} > \frac{-\frac{e}{2} + Q_0}{C_S} \quad (2.54) \text{ (e)}$$

From the inequalities in equations (2.54) (a) – (2.54) (e), the voltage range for which the device can have a maximum of two excess electrons in the Coulomb island is:

$$\frac{\frac{3e}{2} - Q_0}{C_D} < V_{DS} < \frac{\frac{5e}{2} - Q_0}{C_D} \quad (2.55)$$

If a negative source-drain bias is applied to this device, then at a certain voltage, an electron will tunnel out of the island into the source electrode leaving the island with a deficit of one electron. Therefore,

$$\Delta F_S^-(0 \rightarrow -1) < 0$$

From equation (2.31), $\Delta F_S^- = \frac{e}{C_{TOT}} \left[\frac{e}{2} - (Ne - Q_0) + C_D V_{DS} \right]$. Substituting $N = 0$ in

equation (2.30) and solving the inequality $\Delta F_S^-(0 \rightarrow -1) < 0$ gives:

$$\frac{e}{C_{TOT}} \left[\frac{e}{2} - (0e - Q_0) + C_D V_{DS} \right] < 0$$

$$\Rightarrow \frac{e}{2} + Q_0 + C_D V_{DS} < 0$$

$$\Rightarrow C_D V_{DS} < -\frac{e}{2} - Q_0$$

$$\therefore V_{DS} < \frac{-\frac{e}{2} - Q_0}{C_D} \quad (2.56) \text{ (a)}$$

The island will continue to remain with a deficit of one electron till an electron tunnels into it through the drain electrode. The change in the system free energy due to this event is:

$$\Delta F_D^+(-1 \rightarrow 0) < 0$$

From equation (2.33), $\Delta F_D^+ = \frac{e}{C_{TOT}} \left[\frac{e}{2} + (Ne - Q_0) + C_S V_{DS} \right]$. Substituting $N = -1$ in

equation (2.34) and solving the inequality $\Delta F_D^+(-1 \rightarrow 0) < 0$ gives:

$$\frac{e}{C_{TOT}} \left[\frac{e}{2} + (-1e - Q_0) + C_S V_{DS} \right] < 0$$

$$\Rightarrow -\frac{e}{2} - Q_0 + C_S V_{DS} < 0$$

$$\Rightarrow C_S V_{DS} < \frac{e}{2} + Q_0$$

$$\therefore V_{DS} < \frac{\frac{e}{2} + Q_0}{C_S} \quad (2.56) \text{ (b)}$$

For the plateau region corresponding to $N = -1$ electron in the Coulomb island as shown in Figure 2.9 (a), the applied source-drain bias will not be sufficient to remove a second electron into the island. Therefore,

$$\Delta F_S^-(-1 \rightarrow -2) > 0$$

$$\Rightarrow \frac{e}{C_{TOT}} \left[\frac{e}{2} - (-1e - Q_0) + C_D V_{DS} \right] > 0$$

$$\Rightarrow \frac{3e}{2} + Q_0 + C_D V_{DS} > 0$$

$$\Rightarrow C_D V_{DS} > -\frac{3e}{2} - Q_0$$

$$\therefore V_{DS} > \frac{-\frac{3e}{2} - Q_0}{C_D} \quad (2.56) \text{ (c)}$$

From inequalities in equations (2.64) (a) – (2.64) (c), we can say that the voltage range for which the Coulomb island will have a minimum of $N = -1$ electron is:

$$\frac{-\frac{3e}{2} - Q_0}{C_D} < V_{DS} < \frac{-\frac{e}{2} - Q_0}{C_D} \quad (2.57)$$

If the applied source-drain bias is further reduced, a second electron can tunnel out from the Coulomb island into the source electrode. The change in the system free energy due to this event is:

$$\Delta F_S^-(-1 \rightarrow -2) < 0$$

$$\Rightarrow \frac{e}{C_{TOT}} \left[\frac{e}{2} - (-1e - Q_0) + C_D V_{DS} \right] < 0$$

$$\Rightarrow \frac{3e}{2} + Q_0 + C_D V_{DS} < 0$$

$$\Rightarrow C_D V_{DS} < -\frac{3e}{2} - Q_0$$

$$\therefore V_{DS} < \frac{-\frac{3e}{2} - Q_0}{C_D} \quad (2.58) \text{ (a)}$$

At this voltage, $\Delta F_S^-(0 \rightarrow -1)$ is also possible. Therefore:

$$V_{DS} < \frac{-\frac{e}{2} - Q_0}{C_D} \quad (2.58) \text{ (b)}$$

Since at this voltage, a third electron cannot be removed from the island into the source electrode,

$$\Delta F_s^-(-2 \rightarrow -3) > 0$$

$$\Rightarrow \frac{e}{C_{TOT}} \left[\frac{e}{2} - (-2e - Q_0) + C_D V_{DS} \right] > 0$$

$$\Rightarrow \frac{5e}{2} + Q_0 + C_D V_{DS} > 0$$

$$\Rightarrow C_D V_{DS} > -\frac{5e}{2} - Q_0$$

$$\therefore V_{DS} > \frac{-\frac{5e}{2} - Q_0}{C_D} \quad (2.58) \text{ (c)}$$

The other transitions that are possible at this voltage are: An electron tunneling into the Coulomb island from the drain electrode so that:

$$\Delta F_D^+(-2 \rightarrow -1) < 0$$

$$\frac{e}{C_{TOT}} \left[\frac{e}{2} + (-2e - Q_0) + C_S V_{DS} \right] < 0$$

$$\Rightarrow -\frac{3e}{2} - Q_0 + C_S V_{DS} < 0$$

$$\Rightarrow C_S V_{DS} < \frac{3e}{2} + Q_0$$

$$\therefore V_{DS} < \frac{\frac{3e}{2} + Q_0}{C_S} \quad (2.58) \text{ (d)}$$

and $\Delta F_D^+(-1 \rightarrow 0) < 0$

$$\Rightarrow V_{DS} < \frac{\frac{e}{2} + Q_0}{C_S} \quad (2.58) \text{ (e)}$$

From the inequalities in equations (2.58) (a) – (2.58) (e), the voltage range over which the Coulomb island can have a minimum of $N = -2$ electrons is:

$$\frac{-\frac{5e}{2} - Q_0}{C_D} < V_{DS} < \frac{-\frac{3e}{2} - Q_0}{C_D} \quad (2.59)$$

From equation (2.53), the voltage range over which the Coulomb island can have a

maximum of $N = 1$ electron is $\frac{\frac{e}{2} - Q_0}{C_D} < V_{DS} < \frac{\frac{3e}{2} - Q_0}{C_D}$. The width of the Coulomb staircase

ΔV_{DS} is therefore:

$$\begin{aligned} \Delta V_{DS} &= \frac{\frac{3e}{2} - Q_0}{C_D} - \frac{\frac{e}{2} - Q_0}{C_D} \\ \Rightarrow \Delta V_{DS} &= \frac{e}{C_D} \end{aligned} \quad (2.60)$$

From equation (2.55), the voltage range over which the Coulomb island can have a

maximum of $N = 2$ electrons is $\frac{\frac{3e}{2} - Q_0}{C_D} < V_{DS} < \frac{\frac{5e}{2} - Q_0}{C_D}$. The width of the Coulomb

staircase ΔV_{DS} is therefore:

$$\begin{aligned} \Delta V_{DS} &= \frac{\frac{5e}{2} - Q_0}{C_D} - \frac{\frac{3e}{2} - Q_0}{C_D} \\ \Rightarrow \Delta V_{DS} &= \frac{e}{C_D} \end{aligned} \quad (2.61)$$

From equation (2.57), the voltage range over which the Coulomb island can have a

minimum of $N = -1$ electron is $\frac{-\frac{3e}{2} - Q_0}{C_D} < V_{DS} < \frac{-\frac{e}{2} - Q_0}{C_D}$. The width of the Coulomb

staircase ΔV_{DS} is therefore:

$$\Delta V_{DS} = \frac{-\frac{e}{2} - Q_0}{C_D} - \frac{-\frac{3e}{2} - Q_0}{C_D}$$

$$\Rightarrow \Delta V_{DS} = \frac{e}{C_D} \quad (2.62)$$

From equation (2.59), the voltage range over which the Coulomb island can have a

minimum of $N = -2$ electrons is $\frac{-\frac{5e}{2} - Q_0}{C_D} < V_{DS} < \frac{-\frac{3e}{2} - Q_0}{C_D}$. The width of the Coulomb

staircase ΔV_{DS} is therefore:

$$\Delta V_{DS} = \frac{-\frac{3e}{2} - Q_0}{C_D} - \frac{-\frac{5e}{2} - Q_0}{C_D}$$

$$\Rightarrow \Delta V_{DS} = \frac{e}{C_D} \quad (2.63)$$

From the results of equations (2.60) – (2.63), we can see that for a double junction single-electron device which has asymmetric tunnel junctions with $C_D > C_S$ and $R_D \gg R_S$ such that $C_D R_D \gg C_S R_S$, the width of the Coulomb staircase ΔV_{DS} is always $\frac{e}{C_D}$.

Now let us consider another double junction single-electron device in which $C_S > C_D$ and $R_S \gg R_D$ so that $C_S R_S \gg C_D R_D$. The schematic of the Coulomb staircase obtained in such a device is shown in Figure 2.10 (a). Figure 2.10 (b) is the illustration of the voltage

diagram of the device. The voltage drop between the Coulomb island and the source electrode is given by equation (2.10) as:

$$\varphi_{IS} - V_S = \frac{C_D V_{DS}}{C_{TOT}} - \frac{(Ne - Q_0)}{C_{TOT}}$$

and the voltage drop between the drain electrode and the island is given by equation (2.11) as:

$$V_D - \varphi_{IS} = \frac{C_S V_{DS}}{C_{TOT}} + \frac{(Ne - Q_0)}{C_{TOT}}$$

As $C_S > C_D$ in this device, the term $\frac{C_S V_{DS}}{C_{TOT}}$ in $V_D - \varphi_{IS}$ of equation (2.11) is much

larger than the term $\frac{C_D V_{DS}}{C_{TOT}}$ in $\varphi_{IS} - V_S$ of equation (2.10). Assuming that the source electrode

is grounded, when a positive source-drain voltage V_{DS} is applied, the potential of the island tends to remain near the source electrode as shown in Figure 2.10 (b). Due to this, the voltage drop between the drain electrode and the island is much larger when compared to the voltage drop between the island and the source electrode. When the voltage drop between the drain electrode and the island reaches $\frac{e}{2C_{TOT}}$, a single electron will tunnel out of the Coulomb island

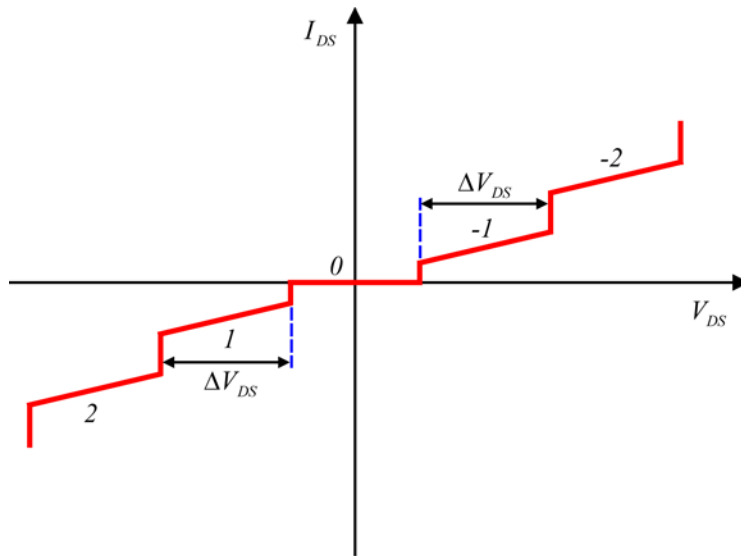
into the drain electrode thereby changing the electron occupancy in the island from 0 to -1. The change in the free energy of the double junction single-electron device due to this event is:

$$\Delta F_D^-(0 \rightarrow -1) < 0$$

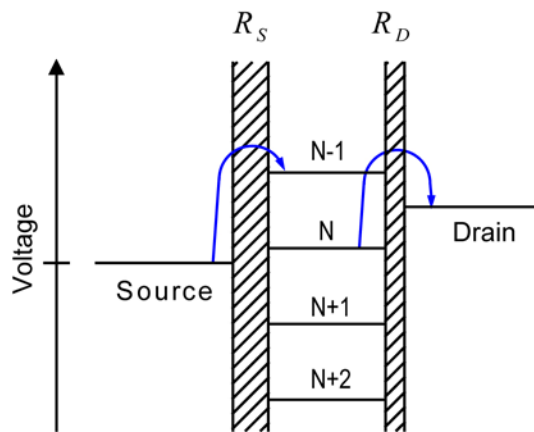
$$\Rightarrow \frac{e}{C_{TOT}} \left[\frac{e}{2} - (0e - Q_0) - C_S V_{DS} \right] < 0$$

$$\Rightarrow \frac{e}{2} + Q_0 - C_S V_{DS} < 0$$

$$\Rightarrow \frac{e}{2} + Q_0 < C_S V_{DS}$$



(a)



(b)

Figure 2.10 Schematic of Coulomb staircase in an asymmetric double junction single-electron device with $C_S > C_D$ and $R_S \gg R_D$ such that $C_S R_S \gg C_D R_D$. (a) Schematic of the $I_{DS} - V_{DS}$ characteristics showing electron occupancy in the Coulomb island as a function of the applied source-drain bias V_{DS} . (b) The voltage diagram of this device depicting the sequence of electron tunneling out of and into the island for a positive applied V_{DS} .

$$\therefore V_{DS} > \frac{\frac{e}{2} + Q_0}{C_S} \quad (2.64) \text{ (a)}$$

The Coulomb island will remain in the state with $N = -1$ electrons till an electron from the source electrode tunnels into it. Since $R_S \gg R_D$, the rate of electron tunneling out of the island to the drain electrode will be much faster than the rate of electrons tunneling into the island from the source electrode for positive source-drain biases. Therefore the island will remain in the state of $N = -1$ electron for the majority of the time. When an electron tunnels into the island from the source electrode bringing it back to its original charge state, the change in the free energy of the device is:

$$\Delta F_S^+(-1 \rightarrow 0) < 0$$

$$\Rightarrow \frac{e}{C_{TOT}} \left[\frac{e}{2} + (-1e - Q_0) - C_D V_{DS} \right] < 0$$

$$\Rightarrow -\frac{e}{2} - Q_0 - C_D V_{DS} < 0$$

$$\Rightarrow -\frac{e}{2} - Q_0 < C_D V_{DS}$$

$$\therefore V_{DS} > \frac{-\frac{e}{2} - Q_0}{C_D} \quad (2.64) \text{ (b)}$$

For the plateau region corresponding to $N = -1$ electron in the Coulomb island as shown in Figure 2.10 (a), the applied source-drain bias is not sufficient to subtract a second electron from the island. Therefore,

$$\Delta F_D^-(-1 \rightarrow -2) > 0$$

$$\Rightarrow \frac{e}{C_{TOT}} \left[\frac{e}{2} - (-1e - Q_0) - C_S V_{DS} \right] > 0$$

$$\Rightarrow \frac{3e}{2} + Q_0 - C_S V_{DS} > 0$$

$$\Rightarrow \frac{3e}{2} + Q_0 > C_S V_{DS}$$

$$\therefore V_{DS} < \frac{\frac{3e}{2} + Q_0}{C_S} \quad (2.64) \text{ (c)}$$

For $|Q_0| < \frac{e}{2}$, $\frac{e}{2} + Q_0$ from equation (2.64) (a) is always larger than $-\frac{e}{2} - Q_0$ from

equation (2.64) (b). Therefore, from equations (2.64) (a), (2.64) (b), and (2.64) (c), the source-drain voltage range for which the Coulomb island will be stable with a minimum of $N = -1$ electron is:

$$\frac{e}{2} + Q_0 < V_{DS} < \frac{\frac{3e}{2} + Q_0}{C_S} \quad (2.65)$$

Now if a more positive source-drain bias is applied, a second extra electron can tunnel out of the island into the drain electrode. Therefore:

$$\Delta F_D^-(-1 \rightarrow -2) < 0$$

$$\Rightarrow \frac{e}{C_{TOT}} \left[\frac{e}{2} - (-1e - Q_0) - C_S V_{DS} \right] < 0$$

$$\Rightarrow \frac{3e}{2} + Q_0 - C_S V_{DS} < 0$$

$$\Rightarrow \frac{3e}{2} + Q_0 < C_S V_{DS}$$

$$\therefore V_{DS} > \frac{\frac{3e}{2} + Q_0}{C_S} \quad (2.66) \text{ (a)}$$

At this voltage, $\Delta F_D^-(0 \rightarrow -1) < 0$ is also possible.

$$\Rightarrow V_{DS} > \frac{\frac{e}{2} + Q_0}{C_S} \quad (2.66) \text{ (b)}$$

Since a third electron cannot be subtracted from the island at this particular source-drain bias,

$$\Delta F_D^-(-2 \rightarrow -3) > 0$$

$$\Rightarrow \frac{e}{C_{TOT}} \left[\frac{e}{2} - (-2e - Q_0) - C_S V_{DS} \right] > 0$$

$$\Rightarrow \frac{5e}{2} + Q_0 - C_S V_{DS} > 0$$

$$\Rightarrow \frac{5e}{2} + Q_0 > C_S V_{DS}$$

$$\therefore V_{DS} < \frac{\frac{5e}{2} + Q_0}{C_S} \quad (2.66) \text{ (c)}$$

At this voltage, an electron can tunnel into the island from the source electrode so that:

$$\Delta F_S^+(-2 \rightarrow -1) < 0$$

$$\Rightarrow \frac{e}{C_{TOT}} \left[\frac{e}{2} + (-2e - Q_0) - C_D V_{DS} \right] < 0$$

$$\Rightarrow -\frac{3e}{2} - Q_0 - C_D V_{DS} < 0$$

$$\Rightarrow -\frac{3e}{2} - Q_0 < C_D V_{DS}$$

$$\therefore V_{DS} > \frac{-\frac{3e}{2} - Q_0}{C_D} \quad (2.66) \text{ (d)}$$

and $\Delta F_S^+(-1 \rightarrow 0) < 0$

$$\Rightarrow V_{DS} > \frac{-\frac{e}{2} - Q_0}{C_D} \quad (2.66) \text{ (e)}$$

Combining the inequalities in equations (2.66) (a) – (2.66) (e), the voltage range for which the device can have a minimum of $N = -2$ electrons in the Coulomb island is:

$$\frac{\frac{3e}{2} + Q_0}{C_S} < V_{DS} < \frac{\frac{5e}{2} + Q_0}{C_S} \quad (2.67)$$

If a negative source-drain voltage is now applied, then at a particular voltage, an electron will tunnel into the island from the drain electrode thereby increasing the electron occupancy in the island by one. Therefore,

$$\Delta F_D^+(0 \rightarrow 1) < 0$$

$$\Rightarrow \frac{e}{C_{TOT}} \left[\frac{e}{2} + (0e - Q_0) + C_S V_{DS} \right] < 0$$

$$\Rightarrow \frac{e}{2} - Q_0 + C_S V_{DS} < 0$$

$$\Rightarrow C_S V_{DS} < -\frac{e}{2} + Q_0$$

$$\therefore V_{DS} < \frac{-\frac{e}{2} + Q_0}{C_S} \quad (2.68) \text{ (a)}$$

Due to $R_S \gg R_D$, the island continues to hold the excess electron till it can tunnel out into the source electrode. The change in the system free energy due to this event is:

$$\Delta F_S^-(1 \rightarrow 0) < 0$$

$$\Rightarrow \frac{e}{C_{TOT}} \left[\frac{e}{2} - (1e - Q_0) + C_D V_{DS} \right] < 0$$

$$\Rightarrow -\frac{e}{2} + Q_0 + C_D V_{DS} < 0$$

$$\Rightarrow C_D V_{DS} < \frac{e}{2} - Q_0$$

$$\therefore V_{DS} < \frac{\frac{e}{2} - Q_0}{C_D} \quad (2.68) \text{ (b)}$$

For the plateau corresponding to $N = 1$ electron in the Coulomb island as shown in Figure 2.10 (a), the source-drain bias is not enough to add a second additional electron to the island. Therefore:

$$\Delta F_D^+(1 \rightarrow 2) > 0$$

$$\Rightarrow \frac{e}{C_{TOT}} \left[\frac{e}{2} + (1e - Q_0) + C_S V_{DS} \right] > 0$$

$$\Rightarrow \frac{3e}{2} - Q_0 + C_S V_{DS} > 0$$

$$\Rightarrow C_S V_{DS} > -\frac{3e}{2} + Q_0$$

$$\therefore V_{DS} > \frac{-\frac{3e}{2} + Q_0}{C_S} \quad (2.68) \text{ (c)}$$

Combining the inequalities in equations (2.68) (a) – (2.68) (c), we can say that the voltage span for which there can be a maximum of $N = 1$ electron in the island is:

$$\frac{-\frac{3e}{2} + Q_0}{C_S} < V_{DS} < \frac{-\frac{e}{2} + Q_0}{C_S} \quad (2.69)$$

If the applied source-drain bias is further reduced, a second excess electron can be added to the Coulomb island from the drain electrode. The change in the free energy of the system due to the addition of a second electron to the island is:

$$\Delta F_D^+(1 \rightarrow 2) < 0$$

$$\Rightarrow \frac{e}{C_{TOT}} \left[\frac{e}{2} + (1e - Q_0) + C_S V_{DS} \right] < 0$$

$$\Rightarrow \frac{3e}{2} - Q_0 + C_S V_{DS} < 0$$

$$\Rightarrow C_S V_{DS} < -\frac{3e}{2} + Q_0$$

$$\therefore V_{DS} < \frac{-\frac{3e}{2} + Q_0}{C_S} \quad (2.70) \text{ (a)}$$

At this voltage, $\Delta F_D^+(0 \rightarrow 1) < 0$ is also possible. Therefore:

$$V_{DS} < \frac{-\frac{e}{2} + Q_0}{C_S} \quad (2.70) \text{ (b)}$$

Since at this voltage, a third extra electron cannot be added to the island from the drain electrode,

$$\Delta F_D^+(2 \rightarrow 3) > 0$$

$$\Rightarrow \frac{e}{C_{TOT}} \left[\frac{e}{2} + (2e - Q_0) + C_S V_{DS} \right] > 0$$

$$\Rightarrow \frac{5e}{2} - Q_0 + C_S V_{DS} > 0$$

$$\Rightarrow C_S V_{DS} > -\frac{5e}{2} + Q_0$$

$$\therefore V_{DS} > \frac{-\frac{5e}{2} + Q_0}{C_S} \quad (2.70) \text{ (c)}$$

The other transitions that are possible at this voltage are: An electron tunneling out of the Coulomb island into the source electrode so that:

$$\Delta F_S^-(2 \rightarrow 1) < 0$$

$$\Rightarrow \frac{e}{C_{TOT}} \left[\frac{e}{2} - (2e - Q_0) + C_D V_{DS} \right] < 0$$

$$\Rightarrow -\frac{3e}{2} + Q_0 + C_D V_{DS} < 0$$

$$\Rightarrow C_D V_{DS} < \frac{3e}{2} - Q_0$$

$$\therefore V_{DS} < \frac{\frac{3e}{2} - Q_0}{C_D} \quad (2.70) \text{ (d)}$$

and $\Delta F_S^-(1 \rightarrow 0) < 0$

$$\Rightarrow V_{DS} < \frac{\frac{e}{2} - Q_0}{C_D} \quad (2.70) \text{ (e)}$$

Combining the inequalities in equations (2.70) (a) – (2.70) (e), the voltage range over which the Coulomb island can have a maximum of $N = 2$ excess electrons is:

$$\frac{-\frac{5e}{2} + Q_0}{C_S} < V_{DS} < \frac{-\frac{3e}{2} + Q_0}{C_S} \quad (2.71)$$

From equation (2.65), the voltage range for which the Coulomb island can have a

minimum of $N = -1$ electron is $\frac{\frac{e}{2} + Q_0}{C_S} < V_{DS} < \frac{\frac{3e}{2} + Q_0}{C_S}$. The width of the Coulomb

staircase ΔV_{DS} is therefore:

$$V_{DS} = \frac{\frac{3e}{2} + Q_0}{C_S} - \frac{\frac{e}{2} + Q_0}{C_S}$$

$$\Rightarrow V_{DS} = \frac{e}{C_S} \quad (2.72)$$

From equation (2.67), the voltage range for which the Coulomb island can have a

minimum of $N = -2$ electrons is $\frac{\frac{3e}{2} + Q_0}{C_S} < V_{DS} < \frac{\frac{5e}{2} + Q_0}{C_S}$. The width of the Coulomb

staircase ΔV_{DS} is therefore:

$$V_{DS} = \frac{\frac{5e}{2} + Q_0}{C_S} - \frac{\frac{3e}{2} + Q_0}{C_S}$$

$$\Rightarrow V_{DS} = \frac{e}{C_S} \quad (2.73)$$

From equation (2.69), the voltage range for which the Coulomb island can have a

maximum of $N = 1$ electron is $-\frac{\frac{3e}{2} + Q_0}{C_S} < V_{DS} < -\frac{\frac{e}{2} + Q_0}{C_S}$. The width of the Coulomb

staircase ΔV_{DS} is therefore:

$$V_{DS} = \frac{-\frac{e}{2} + Q_0}{C_S} - \frac{-\frac{3e}{2} + Q_0}{C_S}$$

$$\Rightarrow V_{DS} = \frac{e}{C_S} \quad (2.74)$$

From equation (2.71), the voltage range for which the Coulomb island can have a

maximum of $N = 2$ electrons is $\frac{-\frac{5e}{2} + Q_0}{C_S} < V_{DS} < \frac{-\frac{3e}{2} + Q_0}{C_S}$. The width of the Coulomb

staircase ΔV_{DS} is therefore:

$$V_{DS} = \frac{-\frac{3e}{2} + Q_0}{C_S} - \frac{-\frac{5e}{2} + Q_0}{C_S}$$

$$\Rightarrow V_{DS} = \frac{e}{C_S} \quad (2.75)$$

Combining the results of equations (2.80) – (2.83), we can see that for a double junction single-electron which has asymmetric tunnel junctions with $C_S > C_D$ and $R_S \gg R_D$ such that

$C_S R_S \gg C_D R_D$, the width of the Coulomb staircase ΔV_{DS} is always $\frac{e}{C_S}$.

The table below summarizes the results obtained for the width of the Coulomb staircase ΔV_{DS} for the different asymmetric double junction single-electron devices as obtained from equations (2.68) – (2.71) and (2.80) – (2.83).

Table 2.2 Width of the Coulomb staircase ΔV_{DS} for asymmetric tunnel junctions.

Tunnel barrier parameters	Width of Coulomb staircase ΔV_{DS}
$C_D > C_S$ and $R_D \gg R_S$ $(\Rightarrow C_D R_D \gg C_S R_S)$	$\frac{e}{C_D}$
$C_S > C_D$ and $R_S \gg R_D$ $(\Rightarrow C_S R_S \gg C_D R_D)$	$\frac{e}{C_S}$

In general, the width of the Coulomb staircase ΔV_{DS} for an asymmetric double junction single-electron device can be represented as:

$$V_{DS} = \frac{e}{\max(C_S, C_D)} \quad (2.76)$$

Figure 2.11 shows the simulated $I_{DS} - V_{DS}$ characteristics of an asymmetric double junction single-electron device in which $C_D > C_S$ and $R_D \gg R_S$ such that $C_D R_D \gg C_S R_S$.

These parameters for the tunnel junctions correspond to the Case (c) of Table 2.1. The width of

the Coulomb blockade for this device from Table 2.1 is equal to $\frac{e}{C_D}$. The width of the Coulomb

staircase from equations (2.51) and (2.76) is $\frac{e}{\max(C_S, C_D)}$. Since $C_D > C_S$, the Coulomb

staircase width is $\frac{e}{C_D}$.

The simulation parameters for this asymmetric double junction single-electron device are: $C_S = 3aF$, $C_D = 9aF$, $R_S = 80M\Omega$, $R_D = 4G\Omega$. Q_0 was taken to be zero and the

simulation was done at a temperature $T = 0K$. As can be seen from the plot, the Coulomb blockade appears around the zero bias region. Since $C_D > C_S$, the width of the Coulomb

blockade from Table 2.1 is $\frac{e}{C_D}$ which is equal to $17.8mV$. The widths of the Coulomb

staircases are also equal to $\frac{e}{C_D} = 17.8mV$. Since $C_D R_D \gg C_S R_S$, the device will exhibit

clear and crisp steps for the Coulomb staircase.

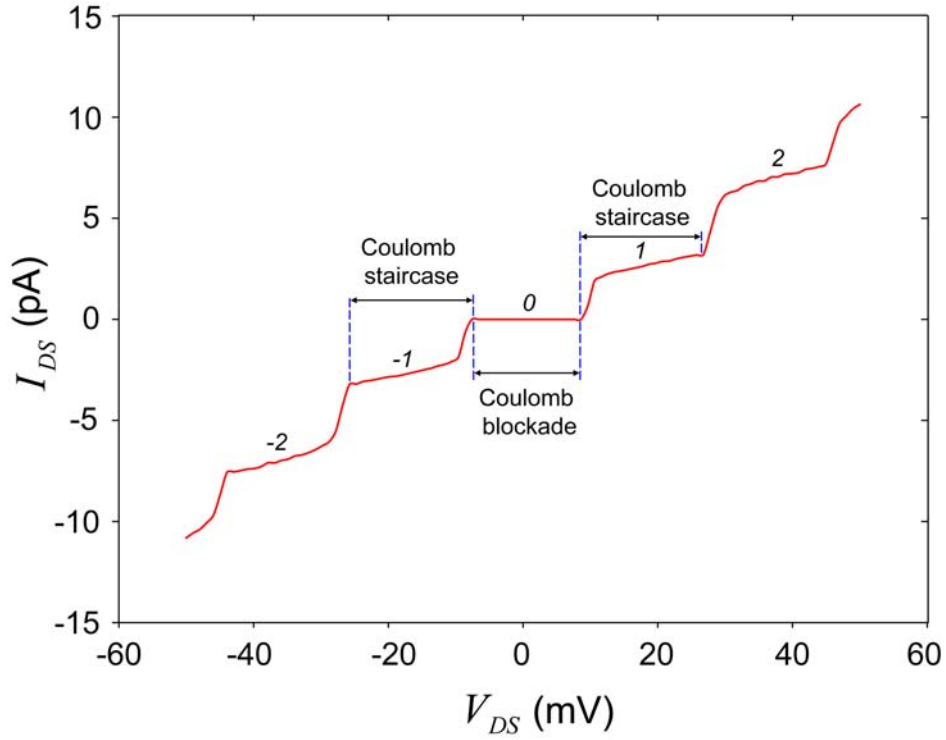


Figure 2.11 Simulated I-V characteristics of an asymmetric double junction single-electron device corresponding to Case (c) in Table 2.1 showing the existence of the Coulomb staircase. The simulation parameters are $C_S = 3aF$, $C_D = 9aF$, $R_S = 80M\Omega$, $R_D = 4G\Omega$ and $Q_0 = 0$. The simulation was done at $T = 0K$. The width of the Coulomb blockade is

$$\frac{e}{C_D} = 17.8mV. \text{ Also, the width of the Coulomb staircase is equal to } \frac{e}{C_D} = 17.8mV.$$

2.4 Charging energy of a double junction single-electron device

The electrostatic potential of the Coulomb island in a double junction single-electron device when it has N excess electrons in it is given by equation (2.9) as:

$$\varphi_{IS} = \frac{C_S V_S + C_D V_D - (Ne - Q_0)}{C_{TOT}}$$

By definition [2.8] the electrochemical potential of the Coulomb island with N excess electrons in it $\mu(N)$ is:

$$\mu(N) = E_N + e \cdot \varphi_{IS}(N) \quad (2.77)$$

where E_N = the highest occupied energy level of the Coulomb island when it contains N number of excess electrons in it.

Substituting the value of $\varphi_{IS}(N)$ in equation (2.77), we get the expression for the electrochemical potential of the Coulomb island with N excess electrons in it as:

$$\mu(N) = E_N + e \left[\frac{C_S V_S + C_D V_D - (Ne - Q_0)}{C_{TOT}} \right] \quad (2.78)$$

We define the charging energy E_C of a Coulomb island as the difference in the electrochemical potential of the island with $(N + 1)$ and N states. Therefore:

$$\begin{aligned} E_C &\equiv \mu(N + 1) - \mu(N) \\ \Rightarrow E_C &= E_{N+1} + e \left[\frac{C_S V_S + C_D V_D - \{(N + 1)e - Q_0\}}{C_{TOT}} \right] - E_N - e \left[\frac{C_S V_S + C_D V_D - \{Ne - Q_0\}}{C_{TOT}} \right] \end{aligned}$$

For metallic Coulomb islands of diameters larger than 1 nm, the separation of the energy states $E_{N+1} - E_N \approx 0$ [2.1]. Therefore, the charging energy can be expressed as:

$$E_C = e \left[\frac{C_S V_S + C_D V_D - \{(N + 1)e - Q_0\}}{C_{TOT}} \right] - e \left[\frac{C_S V_S + C_D V_D - \{Ne - Q_0\}}{C_{TOT}} \right]$$

$$\Rightarrow E_C = \frac{e}{C_{TOT}} [(N+1)e - Ne]$$

$$\therefore E_C = \frac{e^2}{C_{TOT}} \quad (2.79)$$

From equation (2.79), it can be seen that the charging energy E_C of the Coulomb island is independent of the number of N , the number of excess electrons originally occupying the island.

In order to observe the Coulomb blockade and Coulomb staircase in double junction single-electron devices, two important requirements must be satisfied [2.2].

- (1) The charging energy of the Coulomb island must be large enough compared to the thermal energy. From equation (2.79) we can see that the charging energy is inversely proportional to the capacitance of the island C_{TOT} . Therefore, to have a large charging energy, the capacitance of the island must be small. Capacitance of the island can be reduced by decreasing the size of the Coulomb island. In particular, the charging energy must be larger than the average thermal energy $k_B T$ of electrons.

$$E_C = \frac{e^2}{C_{TOT}} > k_B T \quad (2.80)$$

where k_B = Boltzmann Constant = 8.617×10^{-5} eV/K, and T = Absolute temperature.

- (2) The total number of electrons of the island must be well defined. In other words, this means that the amount of charge on the island must be quantized in units of e . This requirement mandates that the resistance of the tunneling barrier at each junction be sufficiently large. In quantum mechanical terms, this condition implies that the wavefunctions of the electrons in the island are well localized

within the boundaries of the Coulomb island. Correspondingly, the tunneling resistance R of the tunnel junctions must be large. The exact value of the resistance of a tunnel junction can be obtained by considering the energy uncertainty of an electron:

$$\Delta E \Delta t > h \quad (2.81)$$

where ΔE is the charging energy and Δt is the characteristic time for charge fluctuations, and h is Planck's constant.

The characteristic time for charging a capacitor C through a tunnel resistor R is given by:

$$\Delta t = R \cdot C \quad (2.82)$$

Substituting the values of ΔE and Δt from equations (2.79) and (2.82), respectively in equation (2.80), we get:

$$\begin{aligned} \frac{e^2}{C} \cdot R \cdot C &> h \\ \Rightarrow R &> \frac{h}{e^2} \\ \therefore R &> 25813\Omega \end{aligned} \quad (2.83)$$

Hence, in order to observe single-electron transport phenomena the resistances of the tunnel junctions must be greater than 25813Ω .

2.5 Electron transport in single-electron transistors

Figure 2.12 (a) shows the schematic and 2.12 (b) the equivalent circuit of a single-electron transistor. As can be seen from Figure 2.12, a single-electron transistor is formed when an additional electrode (the gate electrode) is incorporated to a double junction single-electron device structure. A separate voltage source V_G is coupled to the Coulomb island through an ideal (infinite tunneling resistance) capacitor C_G . This additional voltage modifies the charge balance on the island so that the net charge on the island Q now requires an additional charge Q_G induced by V_G which can be expressed as:

$$Q_G = C_G(V_G - \varphi_{IS}) \quad (2.84)$$

where φ_{IS} is the electrostatic potential of the Coulomb island.

The total charge on the Coulomb island now becomes:

$$Q = -Ne + Q_0 = Q_S - Q_D - Q_G \quad (2.85)$$

where Q_0 is a non-integer offset background charge on the Coulomb island which arises due to the difference in the workfunctions of the metals forming the tunnel junctions [2.3, 2.13] and random charges that are trapped near the tunnel junctions.

From equations (2.7) and (2.84), the charges induced on the Coulomb island are:

$$Q_D = C_D(V_D - \varphi_{IS})$$

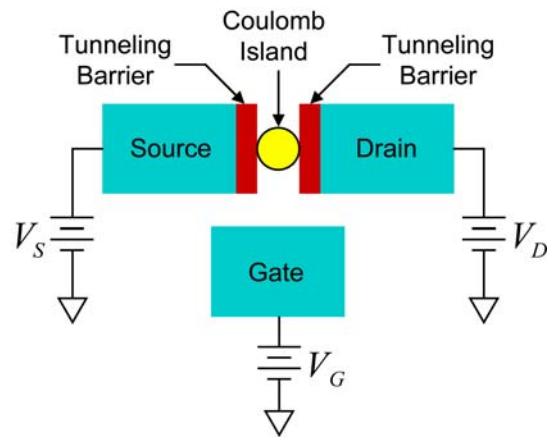
$$Q_S = C_S(\varphi_{IS} - V_S)$$

and

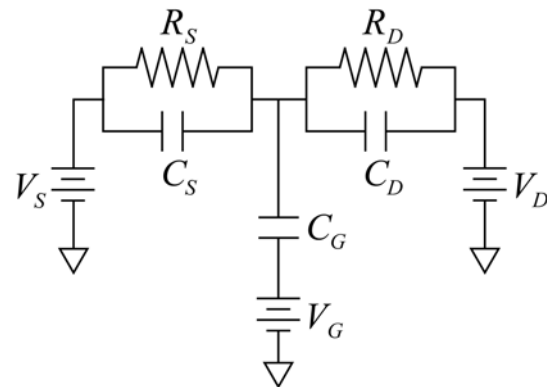
$$Q_G = C_G(V_G - \varphi_{IS}) \quad (2.86)$$

Substituting equation (2.86) in (2.85) and solving for φ_{IS} gives:

$$\begin{aligned} -Ne + Q_0 &= C_S\varphi_{IS} - C_S V_S - C_D V_D + C_D\varphi_{IS} - C_G V_G + C_G\varphi_{IS} \\ \Rightarrow -Ne + Q_0 &= \varphi_{IS}(C_S + C_D + C_G) - C_S V_S - C_D V_D - C_G V_G \end{aligned}$$



(a)



(b)

Figure 2.12 Schematic of a single-electron transistor. (a) Schematic arrangement of single-electron transistor components (i.e., source electrode, drain electrode, gate electrode, and Coulomb island). (b) The equivalent circuit of a single-electron transistor. R_S , C_S , and R_D , C_D denote the resistances and capacitances of the tunnel junctions between the source electrode and the Coulomb island, and between the Coulomb island and the drain electrode, respectively, while C_G denotes the capacitance of the gate which is coupled to the Coulomb island. The gate is connected to a separate voltage source V_G .

$$\therefore \varphi_{IS} = \frac{C_S V_S + C_D V_D + C_G V_G - (Ne - Q_0)}{C_\Sigma} \quad (2.87)$$

where $C_\Sigma \equiv C_S + C_D + C_G$.

If N_S number of electrons tunneled into the island through the tunnel barrier between the source and the island and N_D number of electrons tunneled out of the island through the tunnel barrier between the island and the drain, then the net number of excess electrons in the Coulomb island N is equal to $N_S - N_D$.

The total electrostatic energy stored in the single-electron transistor E_{TOT} is the sum of the electrostatic energy stored in the capacitors of the individual tunnel junctions and the electrostatic energy stored in the gate capacitor. Therefore,

$$E_{TOT} = \frac{Q_S^2}{2C_S} + \frac{Q_D^2}{2C_D} + \frac{Q_G^2}{2C_G} \quad (2.88)$$

Substituting the values of Q_S , Q_D , and Q_G from equations (2.86) in equation (2.88) gives:

$$\begin{aligned} E_{TOT} &= \frac{C_S}{2} (\varphi_{IS} - V_S)^2 + \frac{C_D}{2} (V_D - \varphi_{IS})^2 + \frac{C_G}{2} (V_G - \varphi_{IS})^2 \\ \Rightarrow E_{TOT} &= \frac{1}{2} [C_S \varphi_{IS}^2 + C_S V_S^2 - 2C_S \varphi_{IS} V_S + C_D V_D^2 + C_D \varphi_{IS}^2 - 2C_D V_D \varphi_{IS} + C_G V_G^2 + C_G \varphi_{IS}^2 - 2C_G V_G \varphi_{IS}] \\ \Rightarrow E_{TOT} &= \frac{1}{2} [\varphi_{IS}^2 (C_S + C_D + C_G) - 2\varphi_{IS} (C_S V_S + C_D V_D + C_G V_G) + C_S V_S^2 + C_D V_D^2 + C_G V_G^2] \\ \Rightarrow E_{TOT} &= \frac{1}{2} [\varphi_{IS}^2 C_\Sigma - 2\varphi_{IS} (C_S V_S + C_D V_D + C_G V_G) + C_S V_S^2 + C_D V_D^2 + C_G V_G^2] \quad (2.89) \end{aligned}$$

Substituting the value of φ_{IS} from equation (2.87) in equation (2.89) yields:

$$E_{TOT} = \frac{1}{2} \left[\left\{ \frac{A - (Ne - Q_0)}{C_\Sigma} \right\}^2 C_\Sigma - \frac{2\{A - (Ne - Q_0)\}}{C_\Sigma} A + C_S V_S^2 + C_D V_D^2 + C_G V_G^2 \right]$$

where $A = C_S V_S + C_D V_D + C_G V_G$, a constant.

$$\Rightarrow E_{TOT} = \frac{1}{2} \left[\frac{A^2}{C_\Sigma} + \frac{(Ne - Q_0)^2}{C_\Sigma} - \frac{2A(Ne - Q_0)}{C_\Sigma} - \frac{2A^2}{C_\Sigma} + \frac{2A(Ne - Q_0)}{C_\Sigma} + C_S V_S^2 + C_D V_D^2 + C_G V_G^2 \right]$$

$$\Rightarrow E_{TOT} = \frac{1}{2} \left[-\frac{A^2}{C_\Sigma} + \frac{(Ne - Q_0)^2}{C_\Sigma} + C_S V_S^2 + C_D V_D^2 + C_G V_G^2 \right]$$

$$\Rightarrow E_{TOT} = \frac{1}{2C_\Sigma} \left[-A^2 + (Ne - Q_0)^2 + (C_S V_S^2 + C_D V_D^2 + C_G V_G^2) \cdot C_\Sigma \right]$$

Re-substituting $A = C_S V_S + C_D V_D + C_G V_G$ and $C_\Sigma = C_S + C_D + C_G$ in the above equation,

$$\Rightarrow E_{TOT} = -\frac{1}{2C_\Sigma} \left[C_S^2 V_S^2 + C_D^2 V_D^2 + C_G^2 V_G^2 + 2C_S C_D V_S V_D + 2C_D C_G V_D V_G + 2C_S C_G V_S V_G \right]$$

$$+ \frac{1}{2C_\Sigma} (Ne - Q_0)^2 + \frac{1}{2C_\Sigma} \left[C_S^2 V_S^2 + C_S C_D V_D^2 + C_S C_G V_G^2 \right]$$

$$+ \frac{1}{2C_\Sigma} \left[C_S C_D V_S^2 + C_D^2 V_D^2 + C_D C_G V_G^2 \right]$$

$$+ \frac{1}{2C_\Sigma} \left[C_S C_G V_S^2 + C_D C_G V_D^2 + C_G^2 V_G^2 \right]$$

$$\Rightarrow E_{TOT} = \frac{1}{2C_\Sigma} \left[C_D C_G (V_D^2 + V_G^2 - 2V_D V_G) + C_S C_D (V_D^2 + V_S^2 - 2V_S V_D) \right]$$

$$+ \frac{1}{2C_\Sigma} \left[C_S C_G (V_G^2 + V_S^2 - 2V_S V_G) + (Ne - Q_0)^2 \right]$$

$$\Rightarrow E_{TOT} = \frac{1}{2C_\Sigma} \left[C_D C_G (V_D - V_G)^2 + C_S C_D (V_D - V_S)^2 + C_S C_G (V_G - V_S)^2 + (Ne - Q_0)^2 \right]$$

$$\therefore E_{TOT} = \frac{1}{2C_\Sigma} [Ne - Q_0]^2 + B \quad (2.90)$$

where B is a constant which is independent of N . The terms in the constant B are:

$$B = \frac{1}{2C_{\Sigma}} \left[C_D C_G (V_D - V_G)^2 + C_S C_D (V_D - V_S)^2 + C_S C_G (V_G - V_S)^2 \right] \quad (2.91)$$

If the electron occupancy in the island changes from N to $N + 1$, then the change in the electrostatic energy of the system is:

$$\begin{aligned} \Delta E_{TOT}^+ &= \frac{1}{2C_{\Sigma}} \left\{ (N+1)e - Q_0 \right\}^2 + B - \frac{1}{2C_{\Sigma}} \left\{ Ne - Q_0 \right\}^2 - B \\ \Rightarrow \Delta E_{TOT}^+ &= \frac{1}{2C_{\Sigma}} \left[(Ne + e - Q_0 + Ne - Q_0)(Ne + e - Q_0 - Ne + Q_0) \right] \\ \therefore \Delta E_{TOT}^+ &= \frac{e}{C_{\Sigma}} \left[\frac{e}{2} + (Ne - Q_0) \right] \end{aligned} \quad (2.92)$$

Similarly, if the electron occupancy in the island changes from N to $N - 1$, then the change in the electrostatic energy of the system is:

$$\begin{aligned} \Delta E_{TOT}^- &= \frac{1}{2C_{\Sigma}} \left\{ (N-1)e - Q_0 \right\}^2 + B - \frac{1}{2C_{\Sigma}} \left\{ Ne - Q_0 \right\}^2 - B \\ \Rightarrow \Delta E_{TOT}^- &= \frac{1}{2C_{\Sigma}} \left[(Ne - e - Q_0 + Ne - Q_0)(Ne - e - Q_0 - Ne + Q_0) \right] \\ \therefore \Delta E_{TOT}^- &= \frac{e}{C_{\Sigma}} \left[\frac{e}{2} - (Ne - Q_0) \right] \end{aligned} \quad (2.93)$$

The voltage drop across the tunnel junction between the island and the source $\varphi_{IS} - V_S$ can be simplified by substituting the value of φ_{IS} from equation (2.87) in $\varphi_{IS} - V_S$. Therefore,

$$\begin{aligned} \varphi_{IS} - V_S &= \frac{C_S V_S + C_D V_D + C_G V_G - (Ne - Q_0)}{C_{\Sigma}} - V_S \\ &= \frac{C_S V_S + C_D V_D + C_G V_G - (Ne - Q_0) - V_S (C_S + C_D + C_G)}{C_{\Sigma}} \end{aligned}$$

$$\begin{aligned}
&= \frac{C_S V_S + C_D V_D + C_G V_G - (Ne - Q_0) - C_S V_S - C_D V_S - C_G V_S}{C_\Sigma} \\
&= \frac{C_D (V_D - V_S) + C_G (V_G - V_S) - (Ne - Q_0)}{C_\Sigma} \\
\therefore \varphi_{IS} - V_S &= \frac{C_D V_{DS} + C_G (V_G - V_S) - (Ne - Q_0)}{C_\Sigma} \tag{2.94}
\end{aligned}$$

where $V_{DS} \equiv V_D - V_S$.

Similarly, the voltage drop across the tunnel junction between the island and the drain $V_D - \varphi_{IS}$ can be simplified by substituting the value of φ_{IS} from equation (2.87) in $V_D - \varphi_{IS}$.

This gives:

$$\begin{aligned}
V_D - \varphi_{IS} &= V_D - \frac{C_S V_S + C_D V_D + C_G V_G - (Ne - Q_0)}{C_\Sigma} \\
&= \frac{V_D (C_S + C_D + C_G) - C_S V_S - C_D V_D - C_G V_G + (Ne - Q_0)}{C_\Sigma} \\
&= \frac{C_S V_D + C_D V_D + C_G V_D - C_S V_S - C_D V_D - C_G V_G + (Ne - Q_0)}{C_\Sigma} \\
&= \frac{C_S (V_D - V_S) + C_G (V_D - V_G) + (Ne - Q_0)}{C_\Sigma} \\
\therefore V_D - \varphi_{IS} &= \frac{C_S V_{DS} + C_G (V_D - V_G) + (Ne - Q_0)}{C_\Sigma} \tag{2.95}
\end{aligned}$$

, and the voltage drop across the capacitor between the island and the gate electrode $V_G - \varphi_{IS}$ can be simplified by substituting the value of φ_{IS} from equation (2.87) in $V_G - \varphi_{IS}$. This gives:

$$V_G - \varphi_{IS} = V_G - \frac{C_S V_S + C_D V_D + C_G V_G - (Ne - Q_0)}{C_\Sigma}$$

$$\begin{aligned}
&= \frac{V_G(C_S + C_D + C_G) - C_S V_S - C_D V_D - C_G V_G + (Ne - Q_0)}{C_\Sigma} \\
&= \frac{C_S V_G + C_D V_G + C_G V_G - C_S V_S - C_D V_D - C_G V_G + (Ne - Q_0)}{C_\Sigma} \\
\therefore V_G - \varphi_{IS} &= \frac{C_S(V_G - V_S) + C_D(V_G - V_D) + (Ne - Q_0)}{C_\Sigma} \tag{2.96}
\end{aligned}$$

Now, the charges induced on the Coulomb island by the voltage sources can be expressed by substituting equations (2.94), (2.95) and (2.96) in (2.86). This gives:

$$Q_D = C_D(V_D - \varphi_{IS}) = \frac{C_D}{C_\Sigma} [C_S V_{DS} + C_G(V_D - V_G) + (Ne - Q_0)] \tag{2.97} (a)$$

$$Q_S = C_S(\varphi_{IS} - V_S) = \frac{C_S}{C_{TOT}} [C_D V_{DS} + C_G(V_G - V_S) - (Ne - Q_0)] \tag{2.97} (b)$$

$$\text{and } Q_G = C_G(V_G - \varphi_{IS}) = \frac{C_G}{C_{TOT}} [C_S(V_G - V_S) + C_D(V_G - V_D) + (Ne - Q_0)] \tag{2.97} (c)$$

If the electron occupancy in the island changes from N to $N + 1$, then the change in the charge stored in the tunnel barrier between the drain electrode and the island is given by:

$$\begin{aligned}
\Delta Q_D^{N+1,N} &= Q_D^{N+1} - Q_D^N \\
&= \frac{C_D}{C_\Sigma} [C_S V_{DS} + C_G(V_D - V_G) + \{(N + 1)e - Q_0\}] - \frac{C_D}{C_\Sigma} [C_S V_{DS} + C_G(V_D - V_G) + (Ne - Q_0)] \\
\therefore \Delta Q_D^{N+1,N} &= \frac{C_D}{C_\Sigma} e \tag{2.98}
\end{aligned}$$

Similarly, the change in the charge stored in the tunnel barrier between the island and the source electrode when the electron occupancy in the Coulomb island changes from N to $N + 1$ is given by:

$$\Delta Q_S^{N+1,N} = Q_S^{N+1} - Q_S^N$$

$$\begin{aligned}
&= \frac{C_S}{C_\Sigma} [C_D V_{DS} + C_G (V_G - V_S) - \{(N+1)e - Q_0\}] - \frac{C_S}{C_\Sigma} [C_D V_{DS} + C_G (V_G - V_S) - (Ne - Q_0)] \\
&\quad \therefore \Delta Q_S^{N+1,N} = -\frac{C_S}{C_\Sigma} e \tag{2.99}
\end{aligned}$$

, and the change in charge stored in the capacitor between the gate electrode and the island when the electron occupancy in the Coulomb island changes from N to $N+1$ is given by:

$$\begin{aligned}
\Delta Q_G^{N+1,N} &= Q_G^{N+1} - Q_G^N \\
&= \frac{C_G}{C_\Sigma} [C_S (V_G - V_S) + C_D (V_G - V_D) + \{(N+1)e - Q_0\}] - \frac{C_G}{C_\Sigma} [C_S (V_G - V_S) + C_D (V_G - V_D) + (Ne - Q_0)] \\
&\quad \therefore \Delta Q_G^{N+1,N} = \frac{C_G}{C_\Sigma} e \tag{2.100}
\end{aligned}$$

If the electron occupancy in the island changes from N to $N-1$, then the change in the charge stored in the tunnel barrier between the drain electrode and the island is given by:

$$\begin{aligned}
\Delta Q_D^{N-1,N} &= Q_D^{N-1} - Q_D^N \\
&= \frac{C_D}{C_\Sigma} [C_S V_{DS} + C_G (V_D - V_G) + \{(N-1)e - Q_0\}] - \frac{C_D}{C_\Sigma} [C_S V_{DS} + C_G (V_D - V_G) + (Ne - Q_0)] \\
&\quad \therefore \Delta Q_D^{N-1,N} = -\frac{C_D}{C_\Sigma} e \tag{2.101}
\end{aligned}$$

Similarly, the change in the charge stored in the tunnel barrier between the island and the source electrode when the electron occupancy in the Coulomb island changes from N to $N-1$ is given by:

$$\Delta Q_S^{N-1,N} = Q_S^{N-1} - Q_S^N$$

$$\begin{aligned}
&= \frac{C_S}{C_\Sigma} [C_D V_{DS} + C_G (V_G - V_S) - \{(N-1)e - Q_0\}] - \frac{C_S}{C_\Sigma} [C_D V_{DS} + C_G (V_G - V_S) - (Ne - Q_0)] \\
&\quad \therefore \Delta Q_S^{N-1,N} = \frac{C_S}{C_\Sigma} e \tag{2.102}
\end{aligned}$$

, and the change in charge stored in the capacitor between the gate electrode and the island when the electron occupancy in the Coulomb island changes from N to $N-1$ is given by:

$$\begin{aligned}
\Delta Q_G^{N-1,N} &= Q_G^{N-1} - Q_G^N \\
&= \frac{C_G}{C_\Sigma} [C_S (V_G - V_S) + C_D (V_G - V_D) + \{(N-1)e - Q_0\}] - \frac{C_G}{C_\Sigma} [C_S (V_G - V_S) + C_D (V_G - V_D) + (Ne - Q_0)] \\
&\quad \therefore \Delta Q_G^{N-1,N} = -\frac{C_G}{C_\Sigma} e \tag{2.103}
\end{aligned}$$

The total work done by the voltage sources if an electron is added to the Coulomb island from the drain electrode is:

$$\begin{aligned}
\Delta W_D^+ &= [\Delta Q_D^{N+1,N} \cdot (V_D) - e \cdot V_D] + \Delta Q_S^{N+1,N} \cdot (-V_S) + \Delta Q_G^{N+1,N} \cdot V_G \\
\Rightarrow \Delta W_D^+ &= \left[\frac{C_D}{C_\Sigma} e \cdot V_D - e \cdot V_D \right] + \left(-\frac{C_S}{C_\Sigma} e \right) \cdot (-V_S) + \frac{C_G}{C_\Sigma} e \cdot V_G \\
\Rightarrow \Delta W_D^+ &= eV_D \left[\frac{C_D}{C_\Sigma} - 1 \right] + \frac{C_S}{C_\Sigma} eV_S + \frac{C_G}{C_\Sigma} eV_G \\
\Rightarrow \Delta W_D^+ &= eV_D \left[\frac{C_D - C_S - C_D - C_G}{C_\Sigma} \right] + \frac{C_S}{C_\Sigma} eV_S + \frac{C_G}{C_\Sigma} eV_G \\
\Rightarrow \Delta W_D^+ &= -\frac{C_S}{C_\Sigma} eV_D - \frac{C_G}{C_\Sigma} eV_D + \frac{C_S}{C_\Sigma} eV_S + \frac{C_G}{C_\Sigma} eV_G \\
\Rightarrow \Delta W_D^+ &= -\left(\frac{C_S}{C_\Sigma} eV_D - \frac{C_S}{C_\Sigma} eV_S + \frac{C_G}{C_\Sigma} eV_D - \frac{C_G}{C_\Sigma} eV_G \right)
\end{aligned}$$

$$\therefore \Delta W_D^+ = - \left[\frac{C_S}{C_\Sigma} eV_{DS} + \frac{C_G}{C_\Sigma} e(V_D - V_G) \right] \quad (2.104)$$

The total work done by the voltage sources if an electron is subtracted from the Coulomb island to the drain electrode is:

$$\begin{aligned} \Delta W_D^- &= [\Delta Q_D^{N-1,N} \cdot (V_D) + e \cdot V_D] + \Delta Q_S^{N-1,N} \cdot (-V_S) + \Delta Q_G^{N-1,N} \cdot V_G \\ \Rightarrow \Delta W_D^- &= \left[-\frac{C_D}{C_\Sigma} e \cdot V_D + e \cdot V_D \right] + \left(\frac{C_S}{C_\Sigma} e \right) \cdot (-V_S) + \left(-\frac{C_G}{C_\Sigma} e \right) \cdot V_G \\ \Rightarrow \Delta W_D^- &= eV_D \left[-\frac{C_D}{C_\Sigma} + 1 \right] - \frac{C_S}{C_\Sigma} eV_S - \frac{C_G}{C_\Sigma} eV_G \\ \Rightarrow \Delta W_D^- &= eV_D \left[\frac{-C_D + C_S + C_D + C_G}{C_\Sigma} \right] - \frac{C_S}{C_\Sigma} eV_S - \frac{C_G}{C_\Sigma} eV_G \\ \Rightarrow \Delta W_D^- &= \frac{C_S}{C_\Sigma} eV_D + \frac{C_G}{C_\Sigma} eV_D - \frac{C_S}{C_\Sigma} eV_S - \frac{C_G}{C_\Sigma} eV_G \\ \Rightarrow \Delta W_D^- &= \frac{C_S}{C_\Sigma} eV_D - \frac{C_S}{C_\Sigma} eV_S + \frac{C_G}{C_\Sigma} eV_D - \frac{C_G}{C_\Sigma} eV_G \\ \therefore \Delta W_D^- &= \frac{C_S}{C_\Sigma} eV_{DS} + \frac{C_G}{C_\Sigma} e(V_D - V_G) \end{aligned} \quad (2.105)$$

The total work done by the voltage sources if an electron is added to the Coulomb island from the source electrode is:

$$\begin{aligned} \Delta W_S^+ &= [\Delta Q_S^{N+1,N} \cdot (-V_S) - e \cdot V_S] + \Delta Q_D^{N+1,N} \cdot V_D + \Delta Q_G^{N+1,N} \cdot V_G \\ \Rightarrow \Delta W_S^+ &= \left[-\frac{C_S}{C_\Sigma} e \cdot (-V_S) - e \cdot V_S \right] + \frac{C_D}{C_\Sigma} e \cdot V_D + \frac{C_G}{C_\Sigma} e \cdot V_G \\ \Rightarrow \Delta W_S^+ &= eV_S \left[\frac{C_S}{C_\Sigma} - 1 \right] + \frac{C_D}{C_\Sigma} eV_D + \frac{C_G}{C_\Sigma} eV_G \end{aligned}$$

$$\begin{aligned}
\Rightarrow \Delta W_s^+ &= eV_s \left[\frac{C_s - C_s - C_D - C_G}{C_\Sigma} \right] + \frac{C_D}{C_\Sigma} eV_D + \frac{C_G}{C_\Sigma} eV_G \\
\Rightarrow \Delta W_s^+ &= -\frac{C_D}{C_\Sigma} eV_s - \frac{C_G}{C_\Sigma} eV_s + \frac{C_D}{C_\Sigma} eV_D + \frac{C_G}{C_\Sigma} eV_G \\
\Rightarrow \Delta W_s^+ &= \frac{C_D}{C_\Sigma} eV_D - \frac{C_D}{C_\Sigma} eV_s + \frac{C_G}{C_\Sigma} eV_G - \frac{C_G}{C_\Sigma} eV_s \\
\therefore \Delta W_s^+ &= \frac{C_D}{C_\Sigma} eV_{DS} + \frac{C_G}{C_\Sigma} e(V_G - V_s) \tag{2.106}
\end{aligned}$$

The total work done by the voltage sources if an electron is subtracted from the Coulomb island to the source electrode is:

$$\begin{aligned}
\Delta W_s^- &= [\Delta Q_s^{N-1,N} \cdot (-V_s) + e \cdot V_s] + \Delta Q_D^{N-1,N} \cdot V_D + \Delta Q_G^{N-1,N} \cdot V_G \\
\Rightarrow \Delta W_s^- &= \left[\frac{C_s}{C_\Sigma} e \cdot (-V_s) + e \cdot V_s \right] + \left(-\frac{C_D}{C_\Sigma} e \right) \cdot (V_D) + \left(-\frac{C_G}{C_\Sigma} e \right) \cdot V_G \\
\Rightarrow \Delta W_s^- &= eV_s \left[-\frac{C_s}{C_\Sigma} + 1 \right] - \frac{C_D}{C_\Sigma} eV_D - \frac{C_G}{C_\Sigma} eV_G \\
\Rightarrow \Delta W_s^- &= eV_s \left[\frac{-C_s + C_s + C_D + C_G}{C_\Sigma} \right] - \frac{C_D}{C_\Sigma} eV_D - \frac{C_G}{C_\Sigma} eV_G \\
\Rightarrow \Delta W_s^- &= \frac{C_D}{C_\Sigma} eV_s + \frac{C_G}{C_\Sigma} eV_s - \frac{C_D}{C_\Sigma} eV_D - \frac{C_G}{C_\Sigma} eV_G \\
\Rightarrow \Delta W_s^- &= -\left(\frac{C_D}{C_\Sigma} eV_D - \frac{C_D}{C_\Sigma} eV_s + \frac{C_G}{C_\Sigma} eV_G - \frac{C_G}{C_\Sigma} eV_s \right) \\
\therefore \Delta W_s^- &= -\left[\frac{C_D}{C_\Sigma} eV_{DS} + \frac{C_G}{C_\Sigma} e(V_G - V_s) \right] \tag{2.107}
\end{aligned}$$

From equations (2.104), (2.105), (2.106), and (2.107), we can see that the work done by the voltage sources in adding or subtracting an electron to or from the Coulomb island is

independent of the number of electrons originally residing in the island. Therefore, if N_S number of electrons tunnel into the island from the source electrode in Figure 2.12, the total work done by the voltage sources will be:

$$N_S \cdot W_S^+ = N_S \left[\frac{C_D}{C_\Sigma} eV_{DS} + \frac{C_G}{C_\Sigma} e(V_G - V_S) \right] \quad (2.108) \text{ (a)}$$

and if N_D number of electrons tunnel out of the island to the drain electrode in Figure 2.12, the total work done by the voltage sources will be:

$$N_D \cdot W_D^- = N_D \left[\frac{C_S}{C_\Sigma} eV_{DS} + \frac{C_G}{C_\Sigma} e(V_D - V_G) \right] \quad (2.108) \text{ (b)}$$

Combining equations (2.90) and (2.108), we get the free energy of a single-electron transistor $F(N_S, N_D)$ in which N_S number of electrons has tunneled into the island from the source electrode and N_D number of electrons has tunneled out of the island into the drain electrode as the difference between the electrostatic energy of the system and the work done by the voltage sources:

$$\begin{aligned} F(N_S, N_D) &= E_{TOT} - (N_S \cdot W_S^+) - (N_D \cdot W_D^-) \\ \therefore F(N_S, N_D) &= \frac{1}{2C_\Sigma} [Ne - Q_0]^2 - N_S \left[\frac{C_D}{C_\Sigma} eV_{DS} + \frac{C_G}{C_\Sigma} e(V_G - V_S) \right] \\ &\quad - N_D \left[\frac{C_S}{C_\Sigma} eV_{DS} + \frac{C_G}{C_\Sigma} e(V_D - V_G) \right] + B \end{aligned} \quad (2.109) \text{ (a)}$$

where $N = N_S - N_D$ and B is a constant which is independent of N , N_S , and N_D given by equation (2.91).

Grouping the N dependent terms of the above equation gives:

$$F(N_S, N_D) = \frac{1}{2C_\Sigma} [Ne - Q_0]^2 - N_S \frac{C_D}{C_\Sigma} eV_{DS} - N_S \frac{C_G}{C_\Sigma} eV_G + N_S \frac{C_G}{C_\Sigma} eV_S$$

$$\begin{aligned}
& -N_D \frac{C_S}{C_\Sigma} eV_{DS} - N_D \frac{C_G}{C_\Sigma} eV_D + N_D \frac{C_G}{C_\Sigma} eV_G + B \\
\Rightarrow F(N_S, N_D) &= \frac{1}{2C_\Sigma} [Ne - Q_0]^2 - N_S \frac{C_G}{C_\Sigma} eV_G + N_D \frac{C_G}{C_\Sigma} eV_G \\
& - N_S \frac{e}{C_\Sigma} [C_D V_{DS} - C_G V_S] - N_D \frac{e}{C_\Sigma} [C_S V_{DS} + C_G V_D] + B \\
\Rightarrow F(N_S, N_D) &= \frac{1}{2C_\Sigma} [Ne - Q_0]^2 - (N_S - N_D) \frac{C_G}{C_\Sigma} eV_G \\
& - N_S \frac{e}{C_\Sigma} [C_D V_{DS} - C_G V_S] - N_D \frac{e}{C_\Sigma} [C_S V_{DS} + C_G V_D] + B \\
\Rightarrow F(N_S, N_D) &= \frac{1}{2C_\Sigma} [Ne - Q_0]^2 - Ne \frac{C_G}{C_\Sigma} V_G - N_S \frac{e}{C_\Sigma} [C_D V_{DS} - C_G V_S] - N_D \frac{e}{C_\Sigma} [C_S V_{DS} + C_G V_D] + B
\end{aligned}$$

(2.109) (b)

We substitute $M = N_S + N_D$ and $N = N_S - N_D$ in the above equation so that

$N_S = \frac{M + N}{2}$ and $N_D = \frac{M - N}{2}$. The free energy of the single-electron transistor can now

be expressed as functions of M and N as:

$$\begin{aligned}
F(M, N) &= \frac{1}{2C_\Sigma} \left[(Ne - Q_0)^2 - 2NeC_G V_G \right] \\
& - \frac{M + N}{2} \frac{e}{C_\Sigma} [C_D V_{DS} - C_G V_S] - \frac{M - N}{2} \frac{e}{C_\Sigma} [C_S V_{DS} + C_G V_D] + B \\
\Rightarrow F(M, N) &= \frac{1}{2C_\Sigma} \left[(Ne - Q_0)^2 - 2(Ne - Q_0)C_G V_G + C_G^2 V_G^2 - 2Q_0 C_G V_G - C_G^2 V_G^2 \right] \\
& - \frac{M + N}{2} \frac{e}{C_\Sigma} [C_D V_{DS} - C_G V_S] - \frac{M - N}{2} \frac{e}{C_\Sigma} [C_S V_{DS} + C_G V_D] + B
\end{aligned}$$

$$\begin{aligned}
&\Rightarrow F(M, N) = \frac{1}{2C_\Sigma} \left[(Ne - Q_0 - C_G V_G)^2 - 2Q_0 C_G V_G - C_G^2 V_G^2 \right] \\
&\quad - \frac{e}{C_\Sigma} \left[\frac{M}{2} C_D V_{DS} + \frac{N}{2} C_D V_{DS} - \frac{M}{2} C_G V_S - \frac{N}{2} C_G V_S + \frac{M}{2} C_S V_{DS} - \frac{N}{2} C_S V_{DS} + \frac{M}{2} C_G V_D - \frac{N}{2} C_G V_D \right] + B \\
&\Rightarrow F(M, N) = \frac{1}{2C_\Sigma} \left[(Ne - Q_0 - C_G V_G)^2 - 2Q_0 C_G V_G - C_G^2 V_G^2 \right] \\
&\quad - \frac{e}{C_\Sigma} \left[\frac{M}{2} (C_D + C_S) V_{DS} + \frac{M}{2} C_G (V_D - V_S) + \frac{N}{2} (C_D - C_S) V_{DS} - \frac{N}{2} C_G (V_D + V_S) \right] + B \\
&\Rightarrow F(M, N) = \frac{1}{2C_\Sigma} \left[(Ne - Q_0 - C_G V_G)^2 \right] - \frac{1}{C_\Sigma} Q_0 C_G V_G - \frac{1}{2C_\Sigma} C_G^2 V_G^2 \\
&\quad - \frac{e}{C_\Sigma} \left[\frac{M}{2} (C_D + C_S) V_{DS} + \frac{M}{2} C_G (V_{DS}) + \frac{N}{2} (C_D - C_S) V_{DS} - \frac{N}{2} C_G (V_D + V_S) \right] + B \\
&\Rightarrow F(M, N) = \frac{1}{2C_\Sigma} \left[(Ne - Q_0 - C_G V_G)^2 \right] - \frac{1}{C_\Sigma} Q_0 C_G V_G - \frac{1}{2C_\Sigma} C_G^2 V_G^2 \\
&\quad - \frac{e}{C_\Sigma} \left[\frac{M}{2} (C_D + C_S + C_G) V_{DS} + \frac{N}{2} (C_D - C_S) V_{DS} - \frac{N}{2} C_G (V_D + V_S) \right] + B \\
&\Rightarrow F(M, N) = \left[\frac{1}{2C_\Sigma} (Ne - Q_0 - C_G V_G)^2 \right] - \left[\frac{M}{2} e V_{DS} + \frac{N}{2C_\Sigma} (C_D - C_S) e V_{DS} - \frac{N}{2C_\Sigma} C_G e (V_D + V_S) \right] \\
&\quad + \left[B - \frac{1}{C_\Sigma} Q_0 C_G V_G - \frac{1}{2C_\Sigma} C_G^2 V_G^2 \right]
\end{aligned}$$

Re-substituting the value of B from equation (2.91), we get the free energy of the single-electron transistor in terms of M and N as:

$$F(M, N) = \left[\frac{1}{2C_{\Sigma}} (Ne - Q_0 - C_G V_G)^2 \right] - \left[\frac{M}{2} eV_{DS} + \frac{N}{2C_{\Sigma}} (C_D - C_S) eV_{DS} - \frac{N}{2C_{\Sigma}} C_G e(V_D + V_S) \right] + \left[\frac{1}{2C_{\Sigma}} \{ C_D C_G (V_D - V_G)^2 + C_S C_D (V_D - V_S)^2 + C_S C_G (V_G - V_S)^2 - 2Q_0 C_G V_G - (C_G V_G)^2 \} \right]$$

(2.109) (c)

If an electron tunnels into the Coulomb island from the source electrode, then M changes from $M \rightarrow M + 1$ and N changes from $N \rightarrow N + 1$. The free energy of the single-electron transistor due to the additional electron occupying the Coulomb island in terms of M and N as given by equation (2.109) (c) as:

$$F(M + 1, N + 1) = \left[\frac{1}{2C_{\Sigma}} \{ (N + 1)e - Q_0 - C_G V_G \}^2 \right] - \left[\frac{M + 1}{2} eV_{DS} + \frac{N + 1}{2C_{\Sigma}} (C_D - C_S) eV_{DS} - \frac{N + 1}{2C_{\Sigma}} C_G e(V_D + V_S) \right] + \left[\frac{1}{2C_{\Sigma}} \{ C_D C_G (V_D - V_G)^2 + C_S C_D (V_D - V_S)^2 + C_S C_G (V_G - V_S)^2 - 2Q_0 C_G V_G - (C_G V_G)^2 \} \right]$$

(2.110)

The change in the free energy of the single-electron transistor when an electron tunnels into the island from the source electrode ΔF_s^+ can be obtained by subtracting equation (2.109) (c) from (2.110). This gives:

$$\Delta F_s^+ = F(M + 1, N + 1) - F(M, N)$$

$$\Rightarrow \Delta F_s^+ = \frac{1}{2C_{\Sigma}} \left[(Ne + e - Q_0 - C_G V_G)^2 - (Ne - Q_0 - C_G V_G)^2 \right] - \left[\frac{M + 1}{2} eV_{DS} + \frac{N + 1}{2C_{\Sigma}} (C_D - C_S) eV_{DS} - \frac{N + 1}{2C_{\Sigma}} C_G e(V_D + V_S) \right] + \left[\frac{M}{2} eV_{DS} + \frac{N}{2C_{\Sigma}} (C_D - C_S) eV_{DS} - \frac{N}{2C_{\Sigma}} C_G e(V_D + V_S) \right]$$

[The third term in parenthesis on equations (2.109) (c) and (2.110) cancel each other out since they are independent of M and N].

$$\Rightarrow \Delta F_S^+ = \frac{1}{2C_\Sigma} [(Ne + e - Q_0 - C_G V_G + Ne - Q_0 - C_G V_G)(Ne + e - Q_0 - C_G V_G - Ne + Q_0 + C_G V_G)]$$

$$- \left[\frac{eV_{DS}}{2} + \frac{(C_D - C_S)eV_{DS}}{2C_\Sigma} - \frac{C_G e(V_D + V_S)}{2C_\Sigma} \right]$$

$$\Rightarrow \Delta F_S^+ = \frac{1}{2C_\Sigma} [(2Ne + e - 2Q_0 - 2C_G V_G)(e)] - \left[\frac{eC_\Sigma V_{DS} + (C_D - C_S)eV_{DS} - eC_G(V_D + V_S)}{2C_\Sigma} \right]$$

$$\Rightarrow \Delta F_S^+ = \frac{e}{C_\Sigma} \left[\frac{e}{2} + (Ne - Q_0) - C_G V_G \right]$$

$$- \left[\frac{e(C_S + C_D + C_G)V_{DS} + (C_D - C_S)eV_{DS} - eC_G(V_D + V_S)}{2C_\Sigma} \right]$$

$$\Rightarrow \Delta F_S^+ = \frac{e}{C_\Sigma} \left[\frac{e}{2} + (Ne - Q_0) - C_G V_G \right]$$

$$- \left[\frac{eC_S V_{DS} + eC_D V_{DS} + eC_G V_{DS} + eC_D V_{DS} - eC_G V_{DS} - eC_G V_D - eC_G V_S}{2C_\Sigma} \right]$$

$$\Rightarrow \Delta F_S^+ = \frac{e}{C_\Sigma} \left[\frac{e}{2} + (Ne - Q_0) - C_G V_G \right] - \left[\frac{2eC_D V_{DS} + eC_G(V_{DS} - V_D - V_S)}{2C_\Sigma} \right]$$

$$\Rightarrow \Delta F_S^+ = \frac{e}{C_\Sigma} \left[\frac{e}{2} + (Ne - Q_0) - C_G V_G \right] - \left[\frac{2eC_D V_{DS} + eC_G(V_D - V_S - V_D - V_S)}{2C_\Sigma} \right]$$

$$\Rightarrow \Delta F_S^+ = \frac{e}{C_\Sigma} \left[\frac{e}{2} + (Ne - Q_0) - C_G V_G \right] - \left[\frac{eC_D V_{DS} - eC_G V_S}{C_\Sigma} \right]$$

$$\Rightarrow \Delta F_S^+ = \frac{e}{C_\Sigma} \left[\frac{e}{2} + (Ne - Q_0) - C_G V_G - C_D V_{DS} + C_G V_S \right]$$

$$\therefore \Delta F_S^+ = \frac{e}{C_\Sigma} \left[\frac{e}{2} + (Ne - Q_0) - \{C_D V_{DS} + C_G (V_G - V_S)\} \right] \quad (2.111)$$

The change in the free energy of a single-electron transistor associated with the process of an electron tunneling into the Coulomb island from the source electrode ΔF_S^+ can also be obtained from equations (2.92) and (2.106) as:

$$\begin{aligned} \Delta F_S^+ &= \Delta E_{TOT}^+ - \Delta W_S^+ \\ \Rightarrow \Delta F_S^+ &= \frac{e}{C_\Sigma} \left[\frac{e}{2} + (Ne - Q_0) \right] - \left[\frac{C_D}{C_\Sigma} e V_{DS} + \frac{C_G}{C_\Sigma} e (V_G - V_S) \right] \\ \Rightarrow \Delta F_S^+ &= \frac{e}{C_\Sigma} \left[\frac{e}{2} + (Ne - Q_0) - \{C_D V_{DS} + C_G (V_G - V_S)\} \right] \end{aligned} \quad (2.112)$$

From equations (2.111) and (2.112), we see that the expressions for the change in the free energy of a single-electron transistor are the same and it only depends on the number of extra electrons occupying the Coulomb island N .

If an electron tunnels out of the Coulomb island through the junction between the island and the source electrode, the change in the free energy of the system is given by equations (2.93) and (2.107) as:

$$\begin{aligned} \Delta F_S^- &= \Delta E_{TOT}^- - \Delta W_S^- \\ \Rightarrow \Delta F_S^- &= \frac{e}{C_\Sigma} \left[\frac{e}{2} - (Ne - Q_0) \right] + \left[\frac{C_D}{C_\Sigma} e V_{DS} + \frac{C_G}{C_\Sigma} e (V_G - V_S) \right] \\ \Rightarrow \Delta F_S^- &= \frac{e}{C_\Sigma} \left[\frac{e}{2} - (Ne - Q_0) + \{C_D V_{DS} + C_G (V_G - V_S)\} \right] \end{aligned} \quad (2.113)$$

Combining equations (2.112) and (2.113), we get the change in the free energy of a single-electron transistor when a single electron tunnels into or out of the Coulomb island through the tunnel barrier between the island and the source electrode as:

$$\Delta F_S^\pm = \frac{e}{C_\Sigma} \left[\frac{e}{2} \pm (Ne - Q_0) \mp \{C_D V_{DS} + C_G (V_G - V_S)\} \right] \quad (2.114)$$

where \pm denotes the tunneling into and out of the island, respectively.

If an electron tunnels into the Coulomb island through the tunnel junction between the island and the drain electrode, then the change in the free energy of the single-electron transistor is given by equations (2.92) and (2.104) as:

$$\begin{aligned} \Delta F_D^+ &= \Delta E_{TOT}^+ - \Delta W_D^+ \\ \Rightarrow \Delta F_D^+ &= \frac{e}{C_\Sigma} \left[\frac{e}{2} + (Ne - Q_0) \right] + \left[\frac{C_S}{C_\Sigma} e V_{DS} + \frac{C_G}{C_\Sigma} e (V_D - V_G) \right] \\ \Rightarrow \Delta F_D^+ &= \frac{e}{C_\Sigma} \left[\frac{e}{2} + (Ne - Q_0) + \{C_S V_{DS} + C_G (V_D - V_G)\} \right] \end{aligned} \quad (2.115)$$

Similarly, if an electron tunnels out of the Coulomb island through the junction between the island and the drain electrode, the change in the free energy of the system is given by equations (2.93) and (2.105) as:

$$\begin{aligned} \Delta F_D^- &= \Delta E_{TOT}^- - \Delta W_D^- \\ \Rightarrow \Delta F_D^- &= \frac{e}{C_\Sigma} \left[\frac{e}{2} - (Ne - Q_0) \right] - \left[\frac{C_S}{C_\Sigma} e V_{DS} + \frac{C_G}{C_\Sigma} e (V_D - V_G) \right] \\ \Rightarrow \Delta F_D^- &= \frac{e}{C_\Sigma} \left[\frac{e}{2} - (Ne - Q_0) - \{C_S V_{DS} + C_G (V_D - V_G)\} \right] \end{aligned} \quad (2.116)$$

Combining equations (2.115) and (2.116), we get the change in the free energy of a single-electron transistor when a single electron tunnels into or out of the Coulomb island through the tunnel barrier between the drain electrode and the island as:

$$\Delta F_D^\pm = \frac{e}{C_\Sigma} \left[\frac{e}{2} \pm (Ne - Q_0) \pm \{C_S V_{DS} + C_G (V_D - V_G)\} \right] \quad (2.117)$$

where \pm denotes the tunneling into and out of the island, respectively.

2.5.1 Stability diagram of a single-electron transistor

Similar to double junction single-electron devices, electron transport in single-electron transistors can only take place if the free energy of the system reduces as a result of the tunneling event. From equations (2.114) and (2.117), conditions for tunneling can be written as:

$$\Delta F_S^\pm = \frac{e}{C_\Sigma} \left[\frac{e}{2} \pm (Ne - Q_0) \mp \{C_D V_{DS} + C_G (V_G - V_S)\} \right] < 0 \quad (2.118) \text{ (a)}$$

and

$$\Delta F_D^\pm = \frac{e}{C_\Sigma} \left[\frac{e}{2} \pm (Ne - Q_0) \pm \{C_S V_{DS} + C_G (V_D - V_G)\} \right] < 0 \quad (2.118) \text{ (b)}$$

From equation (2.118) (a), the change in the free energy of the single-electron transistor if an electron tunnels into the island from the source electrode is:

$$\Delta F_S^+ = \frac{e}{C_\Sigma} \left[\frac{e}{2} + (Ne - Q_0) - \{C_D V_{DS} + C_G (V_G - V_S)\} \right]$$

At absolute zero temperature, tunneling is prohibited as long as the change in the free energy of the single-electron transistor is greater than zero. Therefore, the tunneling of an electron from the source electrode into the island is blocked when:

$$\begin{aligned} \Delta F_S^+ &= \frac{e}{C_\Sigma} \left[\frac{e}{2} + (Ne - Q_0) - \{C_D V_{DS} + C_G (V_G - V_S)\} \right] > 0 \\ \Rightarrow \frac{e}{2} + Ne - Q_0 - C_D V_{DS} - C_G V_G + C_G V_S &> 0 \\ \Rightarrow \left(N + \frac{1}{2} \right) e - Q_0 &> C_D V_{DS} + C_G V_G - C_G V_S \end{aligned} \quad (2.119) \text{ (a)}$$

Similarly, at absolute zero temperature, an electron tunneling out of the Coulomb island into the source electrode is prohibited when:

$$\begin{aligned} \Delta F_S^- &= \frac{e}{C_\Sigma} \left[\frac{e}{2} - (Ne - Q_0) + \{C_D V_{DS} + C_G (V_G - V_S)\} \right] > 0 \\ \Rightarrow \frac{e}{2} - Ne + Q_0 + C_D V_{DS} + C_G V_G - C_G V_S &> 0 \end{aligned}$$

$$\Rightarrow C_D V_{DS} + C_G V_G - C_G V_S > \left(N - \frac{1}{2}\right)e - Q_0 \quad (2.119) \text{ (b)}$$

Combining equations (2.119) (a) and (2.119) (b), we get the conditions for which an electron cannot tunnel into/out of the Coulomb island from/to the source electrode as:

$$\left(N - \frac{1}{2}\right)e - Q_0 < C_D V_{DS} + C_G V_G - C_G V_S < \left(N + \frac{1}{2}\right)e - Q_0 \quad (2.120)$$

Similarly, at absolute zero temperature, tunneling of an electron from the drain electrode into the Coulomb island is prohibited when:

$$\begin{aligned} \Delta F_D^+ &= \frac{e}{C_\Sigma} \left[\frac{e}{2} + (Ne - Q_0) + \{C_S V_{DS} + C_G (V_D - V_G)\} \right] > 0 \\ \Rightarrow \frac{e}{2} + Ne - Q_0 + C_S V_{DS} + C_G V_D - C_G V_G &> 0 \\ \Rightarrow \left(N + \frac{1}{2}\right)e - Q_0 &> -C_S V_{DS} - C_G V_D + C_G V_G \end{aligned} \quad (2.121) \text{ (a)}$$

and at absolute zero temperature, the tunneling of an electron from the Coulomb island out into the drain electrode is prohibited when:

$$\begin{aligned} \Delta F_D^- &= \frac{e}{C_\Sigma} \left[\frac{e}{2} - (Ne - Q_0) - \{C_S V_{DS} + C_G (V_D - V_G)\} \right] > 0 \\ \Rightarrow \frac{e}{2} - Ne + Q_0 - C_S V_{DS} - C_G V_D + C_G V_G &> 0 \\ \Rightarrow -C_S V_{DS} - C_G V_D + C_G V_G &> \left(N - \frac{1}{2}\right)e - Q_0 \end{aligned} \quad (2.121) \text{ (b)}$$

Combining equations (2.121) (a) and (2.121) (b), we get the conditions for which an electron cannot tunnel into/out of the Coulomb island from/to the drain electrode as:

$$\left(N - \frac{1}{2}\right)e - Q_0 < -C_S V_{DS} - C_G V_D + C_G V_G < \left(N + \frac{1}{2}\right)e - Q_0 \quad (2.122)$$

Inequalities (2.119) (a), (2.119) (b), (2.121) (a), and (2.121) (b) are used to generate the *stability diagram* in the $V_{DS} - V_G$ plane of a single-electron transistor for different values of N as shown in Figure 2.13. Here we will discuss the formation of the central trapezoid corresponding to the regime where the Coulomb island is stable with $N = 0$ electrons. The other trapezoids can be obtained by substituting various integer values of N in the inequalities listed above. The precise shape and the position of the stable regions depend on the capacitances, background charges, and the form of biasing. Here we will assume asymmetric biasing (i.e., $V_D = V_{DS}$ and $V_S = 0$). This is because we apply an asymmetric bias in all of the measurements described in the following chapters.

From equation (2.118), tunneling of an electron is prohibited as long as $\Delta F_S^\pm, \Delta F_D^\pm > 0$ and tunneling occurs when $\Delta F_S^\pm, \Delta F_D^\pm < 0$. To find the edge of the trapezoid in the stability diagram we will replace the inequality sign with the equal to sign which corresponds to the boundary between tunneling and no tunneling regions.

From equation (2.119) (a), the boundary where the onset of tunneling occurs is:

$$\left(N + \frac{1}{2}\right)e - Q_0 = C_D V_{DS} + C_G V_G - C_G V_S$$

Substituting $N = 0$ in the above equation, we get:

$$\frac{e}{2} - Q_0 = C_D V_{DS} + C_G V_G - C_G V_S$$

Since V_S is grounded (i.e., $V_S = 0$), the above equation reduces to:

$$\frac{e}{2} - Q_0 = C_D V_{DS} + C_G V_G \quad (2.123)$$

To find out the intercepts equation (2.123) makes with the V_G axis and the V_{DS} axis, we substitute $V_{DS} = 0$ and $V_G = 0$, respectively in the above equation. Therefore the intercept equation (2.123) makes with the V_G axis is:

$$V_G = \frac{\frac{e}{2} - Q_0}{C_G}$$

and the intercept the equation (2.80) makes with the V_{DS} axis is:

$$V_{DS} = \frac{\frac{e}{2} - Q_0}{C_D}$$

Therefore, inequality (2.119) (a) corresponds to the edge of the central trapezoid marked by 1 in the stability diagram.

From equation (2.119) (b), the boundary where the onset of tunneling occurs is:

$$\left(N - \frac{1}{2}\right)e - Q_0 = C_D V_{DS} + C_G V_G - C_G V_S$$

Substituting $N = 0$ and $V_S = 0$ in the above equation, the intercepts made by the above

equation with the V_G axis and V_{DS} axis are $V_G = -\frac{\frac{e}{2} + Q_0}{C_G}$ and $V_{DS} = -\frac{\frac{e}{2} + Q_0}{C_D}$,

respectively. Therefore, inequality (2.119) (b) corresponds to the edge of the central trapezoid marked by 2 in the stability diagram.

From equation (2.121) (a), the boundary where the onset of tunneling occurs is:

$$\left(N + \frac{1}{2}\right)e - Q_0 = -C_S V_{DS} - C_G V_D + C_G V_G$$

Substituting $N = 0$ and $V_D = V_{DS}$ in the above equation, the intercepts made by the above

equation with the V_G axis and V_{DS} axis are $V_G = \frac{\frac{e}{2} - Q_0}{C_G}$ and $V_{DS} = -\frac{\frac{e}{2} - Q_0}{C_S + C_G}$,

respectively. Therefore, inequality (2.121) (a) corresponds to the edge of the central trapezoid marked by 3 in the stability diagram.

From equation (2.121) (b), the boundary where the onset of tunneling occurs is:

$$\left(N - \frac{1}{2}\right)e - Q_0 = -C_S V_{DS} - C_G V_D + C_G V_G$$

Substituting $N = 0$ and $V_D = V_{DS}$ in the above equation, the intercepts made by the above

equation with the V_G axis and V_{DS} axis are $V_G = -\frac{\frac{e}{2} + Q_0}{C_G}$ and $V_{DS} = \frac{\frac{e}{2} + Q_0}{C_S + C_G}$,

respectively. Therefore, inequality (2.121) (b) corresponds to the edge of the central trapezoid marked by 4 in the stability diagram.

To obtain the point of intersection of edge 1 and edge 4 of the central trapezoid, equations (2.119) (a) and (2.121) (b) are solved simultaneously. The inequality sign in both the equations are replaced with the equal to sign to find out the actual point of intersection. Thus:

$$Ne + \frac{e}{2} - Q_0 = C_D V_{DS} + C_G V_G - C_G V_S$$

and
$$Ne - \frac{e}{2} - Q_0 = -C_S V_{DS} - C_G V_D + C_G V_G$$

By subtracting one equation from the other, we get:

$$e = C_D V_{DS} + C_S V_{DS} + C_G V_G + C_G V_D + C_G V_S - C_G V_G$$

$$\Rightarrow e = C_D V_{DS} + C_S V_{DS} + C_G (V_D - V_S)$$

$$\Rightarrow e = C_D V_{DS} + C_S V_{DS} + C_G V_{DS} = C_\Sigma V_{DS}$$

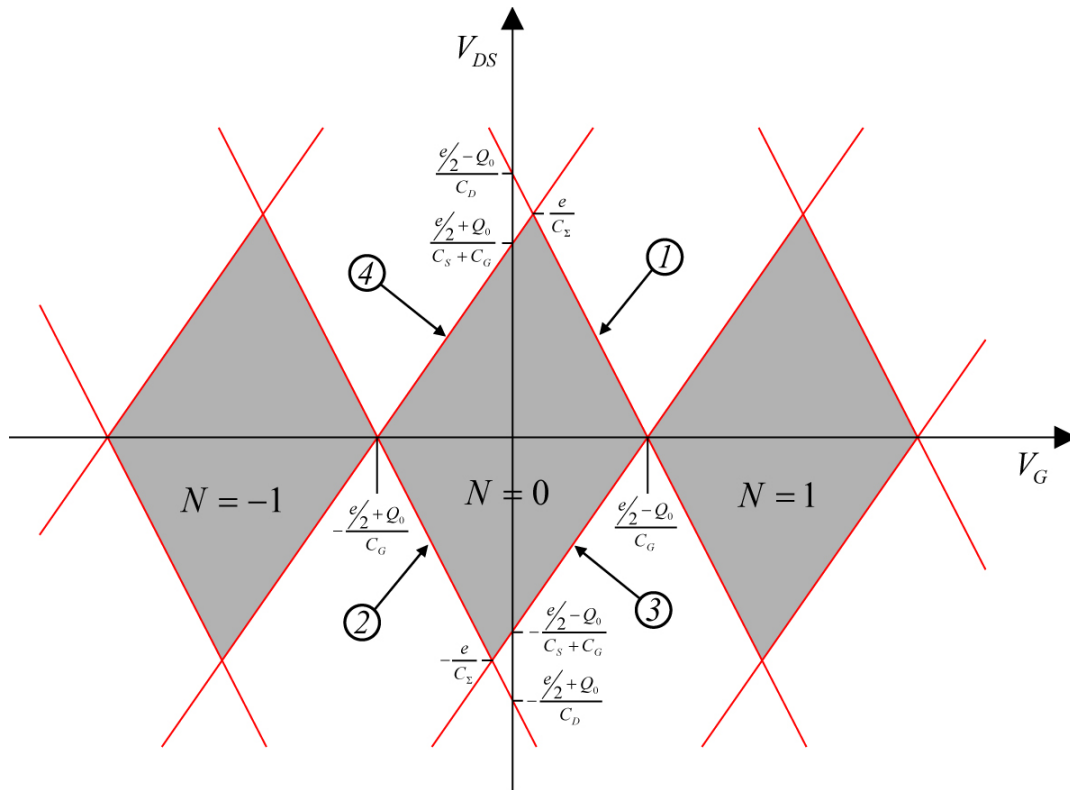


Figure 2.13 Schematic of a stability diagram of a single-electron transistor. The shaded areas of the trapezoids correspond to the regions where no tunneling through either junction may occur, thus putting the device in the Coulomb blockade regime. The red lines forming the boundaries of the trapezoids represent the onset of tunneling in the device.

$$\therefore V_{DS} = \frac{e}{C_{\Sigma}} \quad (2.124)$$

Therefore, point of intersection of edges 1 and 4 of the central rhombus occur at $V_{DS} = \frac{e}{C_{\Sigma}}$.

Similarly, the intersection between edges 2 and 3 of the central trapezoid is obtained by solving equations (2.119) (b) and (2.121) (a) simultaneously. This gives:

$$Ne - \frac{e}{2} - Q_0 = C_D V_{DS} + C_G V_G - C_G V_S$$

and
$$Ne + \frac{e}{2} - Q_0 = -C_S V_{DS} - C_G V_D + C_G V_G$$

By subtracting one equation from the other, we get:

$$-e = C_D V_{DS} + C_S V_{DS} + C_G V_G + C_G V_D - C_G V_S - C_G V_G$$

$$\Rightarrow -e = C_D V_{DS} + C_S V_{DS} + C_G (V_D - V_S)$$

$$\Rightarrow -e = C_D V_{DS} + C_S V_{DS} + C_G V_{DS} = C_{\Sigma} V_{DS}$$

$$\therefore V_{DS} = -\frac{e}{C_{\Sigma}} \quad (2.125)$$

Therefore, point of intersection of edges 2 and 3 of the central rhombus occur at $V_{DS} = -\frac{e}{C_{\Sigma}}$.

The red lines in the stability diagram (Figure 2.13) represent the boundaries for the onset of tunneling given by equation (2.118) for different values of N . The trapezoidal shaded areas correspond to the regions where no solution satisfies equation (2.118), and hence Coulomb blockades exist in these regions. Each of these regions therefore correspond to a different integer number of electrons in the island which is stable. The variation of the gate voltage V_G allows us to tune between the stable regimes, essentially allowing us to add or subtract one electron at a time to the Coulomb island.

When a small source-drain bias and no gate bias are applied to a single-electron transistor, it behaves as a double junction single-electron device. Under these conditions, the device is under the Coulomb blockade regime as described previously. Now if the gate bias is swept keeping the source-drain bias at a constant value, a measurement of the device current versus the gate bias will exhibit peaks in the current. These peaks are known as the *Coulomb oscillations* as they are a signature of electron transport in single-electron transistors. In the following sections, it will be shown how the gate voltage can be modulated to add/subtract single electrons to/from the Coulomb island giving rise to Coulomb oscillations.

2.5.2 Charging energy of a single-electron transistor

The electrostatic potential of the Coulomb island in a single-electron transistor when it has N excess electrons in it is given by equation (2.87) as:

$$\varphi_{IS}(N) = \frac{C_S V_S + C_D V_D + C_G V_G - (Ne - Q_0)}{C_\Sigma}$$

By definition [2.8] the electrochemical potential of the Coulomb island with N excess electrons in it $\mu(N)$ is:

$$\mu(N) = E_N + e \cdot \varphi_{IS}(N) \quad (2.126)$$

where E_N = the highest occupied energy level of the Coulomb island when it contains N number of excess electrons in it.

Substituting the value of $\varphi_{IS}(N)$ in equation (2.126), we get the expression for the electrochemical potential of the Coulomb island with N excess electrons in it as:

$$\mu(N) = E_N + e \left[\frac{C_S V_S + C_D V_D + C_G V_G - (Ne - Q_0)}{C_\Sigma} \right] \quad (2.127)$$

The charging energy E_C of a Coulomb island in a single-electron transistor is defined as the difference in the electrochemical potential of the island with $(N + 1)$ and N states.

Therefore:

$$E_C \equiv \mu(N + 1) - \mu(N)$$

$$\Rightarrow E_C = E_{N+1} + e \left[\frac{C_S V_S + C_D V_D + C_G V_G - \{(N + 1)e - Q_0\}}{C_\Sigma} \right]$$

$$- E_N + e \left[\frac{C_S V_S + C_D V_D + C_G V_G - \{Ne - Q_0\}}{C_\Sigma} \right]$$

For metallic Coulomb islands of diameters larger than 1 nm, the separation of the energy states $E_{N+1} - E_N \approx 0$ [2.1]. Therefore, the charging energy can be expressed as:

$$\Rightarrow E_C = e \left[\frac{C_S V_S + C_D V_D + C_G V_G - \{(N + 1)e - Q_0\}}{C_\Sigma} \right] - e \left[\frac{C_S V_S + C_D V_D + C_G V_G - \{Ne - Q_0\}}{C_\Sigma} \right]$$

$$\Rightarrow E_C = \frac{e}{C_\Sigma} [(N + 1)e - Ne]$$

$$\therefore E_C = \frac{e^2}{C_{TOT}} \tag{2.128}$$

From equation (2.128), it can be seen that the charging energy E_C of the Coulomb island in a single-electron transistor is independent of the number of N , the number of excess electrons originally occupying the island.

2.5.3 Coulomb oscillations in a single-electron transistor

The existence of conductance peaks or Coulomb oscillations in a single-electron transistor can be explained with the aid of the electrostatic potential diagram of the system as shown in Figure 2.14. Initially, no source-drain bias is applied across the device and under this condition, the Coulomb island is assumed to have N excess electrons in it.

The electrostatic potential of the island is given by equation (2.87) as:

$$\varphi_{IS}(N) = \frac{C_S V_S + C_D V_D + C_G V_G - (Ne - Q_0)}{C_\Sigma}$$

If the electron occupancy in the island increases by unity, then the resulting change in the electrostatic potential of the island $\Delta\varphi_{IS}^+$ is:

$$\begin{aligned} \Delta\varphi_{IS}^+ &= \varphi_{IS}(N+1) - \varphi_{IS}(N) \\ \Rightarrow \Delta\varphi_{IS}^+ &= \frac{C_S V_S + C_D V_D + C_G V_G - \{(N+1)e - Q_0\}}{C_\Sigma} - \frac{C_S V_S + C_D V_D + C_G V_G - \{Ne - Q_0\}}{C_\Sigma} \\ \therefore \Delta\varphi_{IS}^+ &= -\frac{e}{C_\Sigma} \end{aligned} \quad (2.129) \text{ (a)}$$

Similarly, if the electron occupancy in the island decreases by one, then the resulting change in the electrostatic potential of the island $\Delta\varphi_{IS}^-$ is:

$$\begin{aligned} \Delta\varphi_{IS}^- &= \varphi_{IS}(N-1) - \varphi_{IS}(N) \\ \Rightarrow \Delta\varphi_{IS}^- &= \frac{C_S V_S + C_D V_D + C_G V_G - \{(N-1)e - Q_0\}}{C_\Sigma} - \frac{C_S V_S + C_D V_D + C_G V_G - \{Ne - Q_0\}}{C_\Sigma} \\ \therefore \Delta\varphi_{IS}^- &= \frac{e}{C_\Sigma} \end{aligned} \quad (2.129) \text{ (b)}$$

From equation (2.129), we can say that the addition or the subtraction of a single electron to or

from the Coulomb island changes the potential of the island by an amount $\frac{e}{C_\Sigma}$.

Assuming that the source electrode is now grounded, when a positive source-drain voltage V_{DS} and no gate voltage V_G is applied to the device, the potential of the island will rise with the rise in V_{DS} . Now the potential of the island lies in between the source and the drain electrodes as shown in Figure 2.14 (a). As long as V_{DS} is small enough so that the voltage drop between the island and the drain or the voltage drop between the drain and the island is less

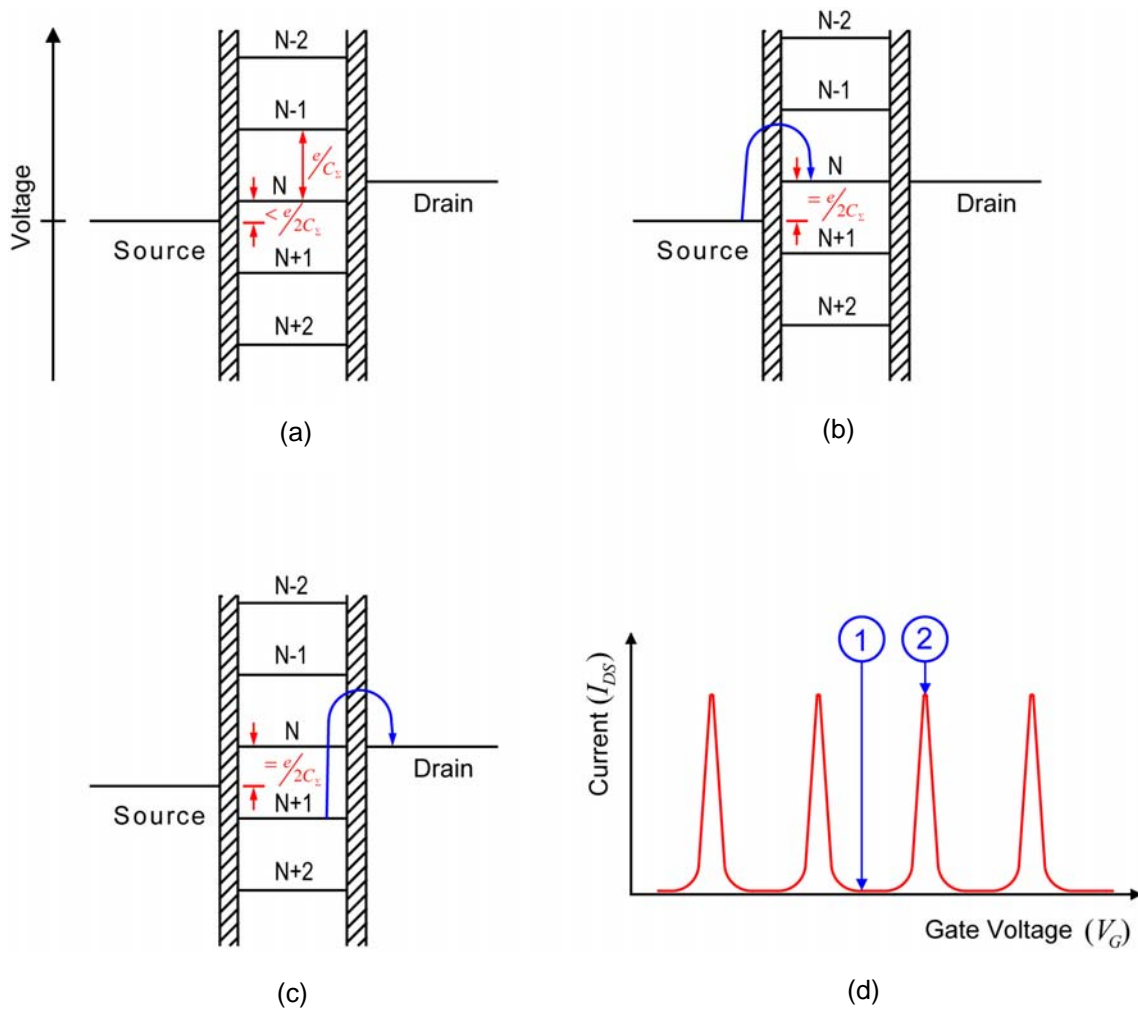


Figure 2.14 Electrostatic potential diagrams of a single-electron transistor. (a) Single-electron transistor under Coulomb blockade regime under the application of a small source-drain bias and zero gate bias. (b) The application of a suitable positive gate voltage V_G increases the potential of the Coulomb island causing a single electron to tunnel into the island from the source electrode. (c) The extra electron tunnels out of the Coulomb island into the drain electrode and brings the island back to its original charge state. (d) Conductance versus gate voltage characteristics of a single-electron transistor. Arrow 1 denotes regions of Coulomb blockade and arrow 2 the Coulomb oscillation peak where the electron occupancy in the island changes by one.

than $\frac{e}{2C_{\Sigma}}$, the tunneling of a single electron into the island from the source electrode or the tunneling of an electron from the island into the drain electrode, respectively is prohibited. Under these circumstances, the single-electron transistor is under Coulomb blockade.

Under this Coulomb blockade condition, now let a positive gate voltage V_G be applied to the single-electron transistor. This gate voltage increases the potential of the island according to equation (2.87). If the voltage drop between the island and the source electrode is still less than $\frac{e}{2C_{\Sigma}}$, the device continues to remain under Coulomb blockade. In the I_{DS} versus V_G characteristics of the device, the Coulomb blockade appears as regions of suppressed electrical conductance as shown by the arrow marker 1 in Figure 2.14 (d).

If the gate voltage is further increased keeping V_{DS} at the same level as before, a stage comes when the voltage drop between the island and the source equals $\frac{e}{2C_{\Sigma}}$ and a single electron can therefore tunnel into the island from the source electrode thereby changing the electron occupancy in the island from N to $N + 1$. Charges flow in from the external power supply to compensate for the additional electron in the island which is manifested as a sudden rise in the $I_{DS} - V_G$ of the device (Coulomb conductance peak) as shown by arrow marker 2 in Figure 2.14 (d). The extra electron tunnels out of the island into the drain electrode bringing the island back to having N excess electrons as shown in Figure 2.14 (c).

With the further increase in the applied gate voltage, the Coulomb island becomes stable with $N + 1$ electrons and the device goes into Coulomb blockade again. The current in the $I_{DS} - V_G$ characteristics of the device again reaches the minima.

If a negative gate voltage is applied to the single-electron transistor when the device is under Coulomb blockade, the potential of the island starts to decrease. When the voltage drop

between the island and the drain electrode reaches $\frac{e}{2C_{\Sigma}}$, an electron can tunnel out from the island and into the drain electrode. Therefore the electron occupancy in the island changes from N to $N - 1$. This event too causes the appearance of a Coulomb oscillation peak in the $I_{DS} - V_G$ characteristics of the device.

Therefore, as the gate voltage is modulated, the conductance of the device oscillates between zero (Coulomb blockade) and non-zero (no Coulomb blockade). In the case of the Coulomb blockade, there is a fixed integer number of electrons in the island and the conductance of the device is at its minima. At the Coulomb conductance peak, the number of electrons in the island changes by one and the electrostatic potential by $\frac{e}{C_{\Sigma}}$.

Figure 2.15 provides a simple graphical interpretation of the analysis presented above [2.8]. Figure 2.15 (a) shows the electron occupancy in the Coulomb island as a function of the gate voltage V_G for a small and constant source-drain bias V_{DS} such that in the absence of the applied gate voltage, the device would be under the Coulomb blockade regime. Figure 2.15 (b) is the plot of the change in the electrochemical potential of the island as a function of applied gate bias. This is obtained by solving equation (2.127). As can be seen from the plot, the application of a positive gate bias starts to lower the electrochemical potential of the island till a single electron can then tunnel into it. The addition of the extra electron to the island causes its electrochemical potential to increase by an amount equal to its charging energy $\frac{e^2}{C_{\Sigma}}$. This results in the observation of a Coulomb conductance peak in the current versus gate voltage of the device as shown in Figure 2.15 (c). Upon further increasing the applied gate bias, the Coulomb island becomes stable with $N + 1$ electrons. The conductance drops to the minima till

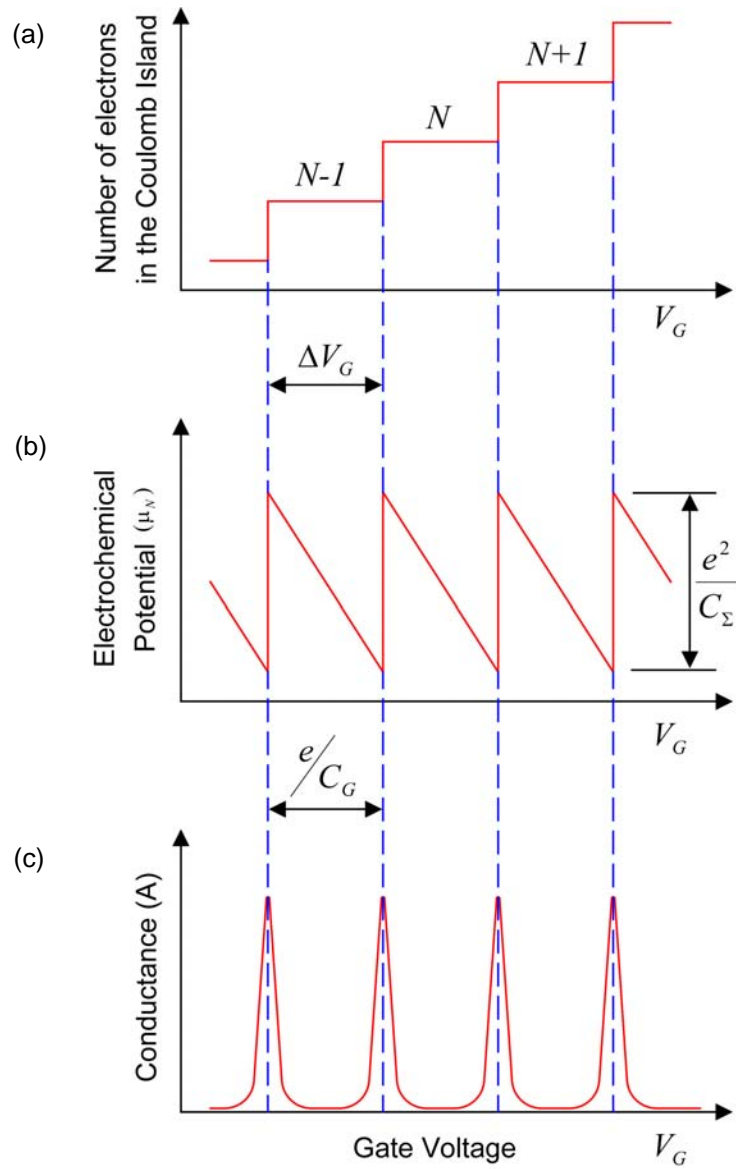


Figure 2.15 (a) Electron occupation in the Coulomb island as a function of the applied gate voltage (V_G). The actual charge state of the Coulomb island is quantized and increases in a step-wise manner with V_G . (b) Electrochemical potential (μ_N) of the island as a function of V_G . (c) Conductance of the single electron transistor as a function of V_G . The peaks (non-zero current) in the plot are Coulomb oscillations which are observed only when the electron occupancy in the island changes by one electron.

such a gate voltage is reached when the $N + 2^{\text{th}}$ electron can tunnel into the island resulting in the appearance of the next Coulomb oscillation peak.

2.5.4 Interval between Coulomb oscillation peaks in a single-electron transistor

The spacing between two adjacent Coulomb oscillation peaks of a single-electron transistor can be obtained by calculating the difference in the electrostatic potential of the Coulomb island before and after the addition of a single electron.

From equation (2.129) (a), the change in the electrostatic potential of the Coulomb island when an electron is added to it $\Delta\phi_{IS}^+$ is $-\frac{e}{C_{\Sigma}}$ and from equation (2.129) (b), the change in the electrostatic potential when an electron is subtracted $\Delta\phi_{IS}^-$ is $\frac{e}{C_{\Sigma}}$.

Since the source-drain bias voltage is kept at a constant value and the gate voltage is modulated to observe the Coulomb oscillations, let a change of ΔV_G cause the electron occupancy in the island to change by one. Therefore from equation (2.87):

$$\begin{aligned} \frac{C_G \Delta V_G}{C_{\Sigma}} &= \frac{e}{C_{\Sigma}} \\ \Rightarrow \Delta V_G &= \frac{e}{C_G} \end{aligned} \quad (2.130)$$

Therefore the interval between two adjacent Coulomb oscillation peaks ΔV_G in a single-electron transistor where the source-drain bias is kept at a constant value is $\frac{e}{C_G}$.

2.6 Orthodox theory of single-electron tunneling

The orthodox theory of single-electron tunneling was first developed by Kulik and Shekhter [2.10] for a particular case study, and was later extended for general systems by Averin and Likharev [2.1, 2.3]. The charging energy of the Coulomb island E_C is the largest energy in a single-electron device system. There is also room for comparison between the thermal energy of electrons $k_B T$ and the quantum level spacing of single-particle states ΔE_N . Therefore, the Coulomb blockade phenomenon can have two different regimes:

- (1) **Classical Limit** – In this, $E_C > k_B T > \Delta E_N$. If the electron temperature is larger than the single electron level spacing, the electron density of states in the Coulomb island is effectively continuous. This situation is known as the *classical* Coulomb blockade.
- (2) **Quantum Limit** – In this, $E_C \geq \Delta E_N > k_B T$. The single-particle energy levels retain their individual character if charging energy E_C and the single electron level spacing ΔE_N are comparable. Under this circumstance, the Coulomb island is treated as a quantum mechanical object with discrete single-particle density of states.

For my experiments involving the study of single-electron behavior and the fabrication of single-electron devices, I used Au nanoparticles as the Coulomb islands. For metal nanoparticles with diameters more than 1 nm, $E_C \gg \Delta E_N$ [2.1]. So, I will only concentrate on describing and utilizing the classical Coulomb blockade in this thesis.

2.6.1 Electron tunneling rate through tunnel junctions

To calculate the electron tunneling rate through a tunnel junction, we consider a system comprising of j tunnel junctions that are coupled together and characterized by the number of electrons that have passed through the junction $\{j\}$.

$$\{j\} = \{j_1, j_2, \dots, j_j, \dots, j_N\} \quad (2.131)$$

The electron tunneling rate for the j^{th} junction is represented by $\Gamma_j^\pm(N)$, where \pm refers to the electrons tunneling into/out of the Coulomb island ($N \rightarrow N \pm 1$). $\Gamma_j^\pm(N)$ is obtained from the basic golden-rule calculation [2.3] and is expressed as:

$$\Gamma_j^\pm(N) = \frac{1}{R_j e^2} \left[\frac{-\Delta F_j^\pm}{1 - \exp\left(\frac{\Delta F_j^\pm}{k_B T}\right)} \right] \quad (2.132)$$

where ΔF is the change in the free energy of the system when an electron tunnels across a tunnel barrier, R_j is the tunneling resistance of the j^{th} junction, e is the unit charge of an electron (1.602×10^{-19} Coulombs) ($e > 0$), k_B is the Boltzmann Constant (8.617×10^{-5} eV/K), and T is the absolute temperature.

To calculate the I-V characteristics of a double junction single-electron device or a single-electron transistor, we have to take into consideration four tunneling events: (a) tunneling of electron into the island through the tunnel barrier between the island and the drain $\Gamma_D^+(N)$, (b) tunneling of an electron out of the island through the tunnel barrier between the island and the drain $\Gamma_D^-(N)$, (c) tunneling of an electron into the island through the tunnel barrier between the island and the source $\Gamma_S^+(N)$, and (d) tunneling of an electron out of the island through the tunnel barrier between the island and the source $\Gamma_S^-(N)$.

The change in the free energy for a double junction single-electron device when a single electron tunnels into or out of the Coulomb island was derived in equations (2.32) and (2.35) as:

$$\Delta F_S^\pm = \frac{e}{C_{TOT}} \left[\frac{e}{2} \pm (Ne - Q_0) \mp C_D V_{DS} \right]$$

and

$$\Delta F_D^\pm = \frac{e}{C_{TOT}} \left[\frac{e}{2} \pm (Ne - Q_0) \pm C_S V_{DS} \right]$$

The change in the free energy for a single electron transistor when a single electron tunnels into or out of the Coulomb island was derived in equations (2.114) and (2.117) as:

$$\Delta F_S^\pm = \frac{e}{C_\Sigma} \left[\frac{e}{2} \pm (Ne - Q_0) \mp \{C_D V_{DS} + C_G (V_G - V_S)\} \right]$$

and

$$\Delta F_D^\pm = \frac{e}{C_\Sigma} \left[\frac{e}{2} \pm (Ne - Q_0) \pm \{C_S V_{DS} + C_G (V_D - V_G)\} \right]$$

Substituting the values of ΔF_S^+ , ΔF_S^- , ΔF_D^+ , and ΔF_D^- from the above equations into equation (2.132), $\Gamma_S^+(N)$, $\Gamma_S^-(N)$, $\Gamma_D^+(N)$, and $\Gamma_D^-(N)$ can be obtained, respectively. The current in the double junction single-electron device or the single-electron transistor $I(V)$ can be calculated by:

$$I(V) = e \sum_{N=-\infty}^{\infty} \sigma(N) [\Gamma_D^+(N) - \Gamma_D^-(N)]$$

or

$$I(V) = e \sum_{N=-\infty}^{\infty} \sigma(N) [\Gamma_S^-(N) - \Gamma_S^+(N)] \quad (2.133)$$

where $\sigma(N)$ is the ensemble distribution of the number of electrons in the Coulomb island [2.6]. The distribution $\sigma(N)$ is obtained by noting that the net probability for making a transition between any two adjacent states in the steady state is zero [2.6], i.e.,

$$\sigma(N) [\Gamma_S^+(N) + \Gamma_D^+(N)] = \sigma(N+1) [\Gamma_S^-(N+1) + \Gamma_D^-(N+1)] \quad (2.134)$$

Since Γ_S^+ , Γ_S^- , Γ_D^+ , and Γ_D^- are known, the distribution $\sigma(N)$ can be solved using the normalization condition $\sum_{N=-\infty}^{\infty} \sigma(N) = 1$ [2.6]. The current in single-electron devices can therefore be obtained by numerically solving equation (2.133).

CHAPTER 3

NEW SINGLE-ELECTRON DEVICE STRUCTURE

3.1 Introduction

In this Chapter, we will look back briefly into the history of single-electron devices and the recent advancements that have been made in the field of single electronics. This will be followed by the introduction of a new single-electron device structure which aims to overcome the shortcomings of the existing methods of fabricating single-electron devices.

3.2 History of single-electron devices

Historically, Coulomb blockade effects were first predicted and observed in small metallic tunnel junctions. The dominant single-electron effect for small metal tunnel junctions is the charging energy due to the transfer of individual electrons. The effects of single-electron charging in the conductance properties of very thin metallic films was observed in the early 1950s by Gorter [3.1] and Darmais [3.2]. Neugebauer and Webb [3.3] developed a theory of *activated tunneling* in which the activation energy was the electrostatic energy required to tunnel electrons into and out of the metal islands.

A number of experiments have been conducted to study the transport properties of metal clusters or islands embedded in an insulator and then connecting it to conducting electrodes. A schematic for such a structure for Au nanoparticles embedded in Al_2O_3 matrix is shown in Figure 3.1. Each metal cluster represents a Coulomb island like the one shown schematically in Figure 2.2 (a). Electrons may tunnel through the insulating medium from the electrodes to the islands and vice-versa. Giaever and Zeller [3.4] investigated the differential resistance of oxidized Sn islands sandwiched between two Al electrodes forming Coulomb islands down to 2.5 nm diameter. The size of the islands obtained in their experiments depended on the evaporating conditions of metallic Sn. They measured signs of Coulomb

blockade in these samples, that is, a region of high resistance for small applied biases followed by strong decrease in the resistance beyond a certain voltage.

Shortly after, Lambe and Jaklevic [3.5] performed capacitance-voltage measurements on structures similar to that of Giaever and Zeller. Their structures were defined with thick oxides between the islands and the substrate so that tunneling of electrons occurred only through the top contact. They observed oscillatory behavior in the differential capacitance measurements of the samples and interpreted it in terms of the addition of charges one by one to the islands as the bias voltages increased in multiples of $\frac{e}{C}$, where C is the substrate to the island capacitance.

At the same time, a detailed theoretical study of single-electron effects during tunneling was introduced by Kulik and Shekhter [3.6] based on the tunneling Hamiltonian method in order to derive a kinetic equation for charge transport. This kinetic equation approach was later improved by Averin and Likharev [3.7] to derive the *Orthodox Theory* of single-charge tunneling. The *Coulomb staircase* was first observed by Kuzmin and Likharev [3.8] and Barner and Ruggiero [3.9] in metallic island structures of similar structure as in Figure 3.1 except that the thickness of the insulation on one side of the Coulomb islands was much larger compared to the other side.

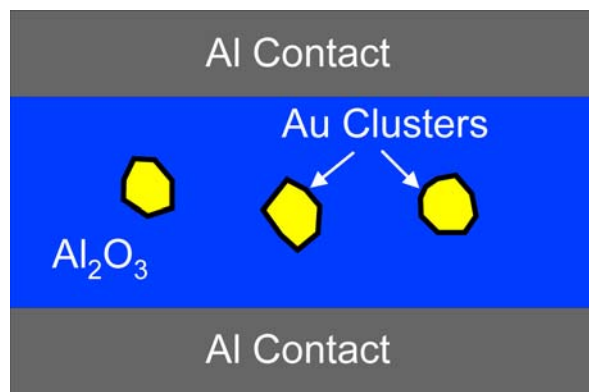


Figure 3.1 A cross section of embedded metal clusters such as Au in a dielectric medium. The ends of the dielectric film are connected to conducting electrodes for applying a bias from an external source.

3.2.1 Recent advancements in the field of single electronics

The creation of a nanometer scale gap between two conducting electrodes and then placing the Coulomb island in between the two electrodes such that it is separated from each of the electrodes by tunnel junctions of required thickness is the key towards the successful fabrication of single-electron devices. Up until 1980, the manipulation of individual nanoparticles and the creation of a nanoscale gap between two conducting electrodes was a formidable task. The discovery of the scanning tunneling microscope (STM) in 1981 proved to be an invaluable tool to study the single-electron transport phenomena in metallic and semiconducting nanoparticles. It has been used in several variations to demonstrate single-electron behavior. Hanna and Tinkham [3.10] reported a measurement of Coulomb staircase in a two-junction system using a STM. They carried out their measurements at a temperature of 4.2 K and simulated their data with the orthodox theory of single-electron tunneling. Kubaik and co-workers [3.11] used an approach similar to Hanna and Tinkham to demonstrate single-electron transport at room temperature in gold nanoparticles. A schematic of their experimental set-up is shown in Figure 3.2 (a). The double junction is formed between a conducting Au {111} substrate, an organic self-assembled monolayer, individual crystalline Au clusters, vacuum, and a conducting Pt/Ir STM tip. The size of the Au clusters were ~ 1-2 nm in diameter. An ultrahigh vacuum STM was used to measure the current-voltage characteristics. When the tip was positioned over a cluster, current-voltage data showed a Coulomb staircase behavior. The experimental data was in good agreement with the semiclassical predictions for correlated single-electron tunneling.

Fabrication of single-electron transistor has also been reported by Matsumoto and co-workers [3.12] by the nanooxidation process for a TiO_x/Ti system. Using the STM tip as a cathode, they were able to oxidize the surface of titanium metal into lines of TiO_x of width of a few tens of nanometers. Using this process, they were able to define a source electrode, a drain electrode and a Coulomb island which were electrically isolated from each other by oxidized Ti

lines as shown in Figure 3.2 (b). Upon suitably biasing the device, distinct Coulomb staircases were observed in the current-voltage characteristics. The underlying n-type silicon substrate was used as the back-gate to make the observed Coulomb staircase even more pronounced.

With the advent of nanofabrication techniques such as e-beam lithography, it became a tool of choice to fabricate devices, observe, and study single-electron behavior in nanoparticles. Klein and co-workers [3.13] successfully combined e-beam lithography and shadow mask evaporation to create a nanoscale gap between two conducting Au leads. Using linker molecules as tunneling barriers, CdSe nanocrystals were immobilized in the gap between the two leads to fabricate a single-electron device as shown in Figure 3.2 (c). I-V measurements carried out at 4.2 K yielded clear Coulomb blockade in the devices. A degenerately doped Si wafer was used as a back gate, applying a suitable bias to which could lift the Coulomb blockade and make the device act as a single-electron transistor. A Coulomb oscillation conductance peak was also observed when the gate bias was modulated keeping the source drain bias at a constant value.

Ralph and co-workers [3.14] have reported the fabrication of single-electron transistors using electromigration to create the source-drain electrode gap. A nanoparticle was then introduced in the gap between the electrodes and the entire structure rested on top on an oxidized aluminum film which also acted as the gate electrode as shown in Figure 3.2 (d). The finished devices were cooled to 4.2 K and the current-voltage curves were measured as a function of the gate voltage. Clear Coulomb staircases as well as Coulomb diamonds were observed for the devices representing single-electron transistor behavior.

In addition to the above mentioned methods, other techniques that have been used for the fabrication of single-electron devices include mechanically controllable break junctions [3.15, 3.16], use of an atomic force microscope (AFM) [3.17], electrodeposition [3.18, 3.19] and the use of silicon-insulator-silicon nanopillars [3.20].

3.3 New single-electron device structure

Although all of the above mentioned techniques and various others have been able to successfully demonstrate single-electron behavior in metallic as well as semiconducting nanoparticles, large-scale fabrication of single-electron devices using the abovementioned methods have not been possible mainly because of low throughputs, inability to accurately control the source-drain electrode gap for every device and/or because the processes are too slow for practical applications. Large-scale fabrication of single-electron devices is necessary to have multiple and individually addressable devices. If several such single-electron devices are integrated at the chip-level, these could be used in the microelectronics industry, military, space as well as other commercial applications.

One of the major aims of this research was to introduce a new single-electron device structure which would address the shortcomings of the existing methods by addressing three important issues:

- (1) Fabrication of single-electron devices on a large-scale and in parallel processing:** Practical applications require that devices be fabricated on a large-scale and in parallel processing. In other words, this means that several single-electron devices must be fabricated in a single batch instead of fabricating them as single units.
- (2) Fabrication using CMOS compatible processes:** CMOS fabrication technology has been developed and standardized over a period of about 40 years. It has also been a proven method for wafer-scale fabrication of devices. Taking advantage of CMOS compatible processes ensures that the fabrication of single-electron devices carried out using existing equipment and recipes.
- (3) Room-temperature operation of single-electron devices:** Another requirement for practical application of single-electron devices is that they be operable at room temperature. For this, the size of the Coulomb island should

be ≤ 10 nm. Since the Coulomb island itself is in the nanometer scale, it requires that all other associated components of a single-electron device (source, drain, and gate electrodes and the tunneling barriers) be arranged in their respective positions around the Coulomb island with nanometer scale precision.

Figures 3.3 (a) and 3.3 (b) show the schematic of the new single-electron device structure which aims to realize the issues discussed above. The three key aspects of the new design are:

- (1) The gap between the source and the drain electrodes is defined by the thickness (h in Figure 3.3 (a)) of the intervening dielectric film. With deposition techniques such as plasma enhanced chemical vapor deposition (PECVD), the thickness of the film can be controlled with sub-nanometer scale precision over a large area. Hence, the source-drain electrode gap can be accurately controlled over the entire wafer on which the deposition is being done.
- (2) The drain, dielectric layer, and the source are vertically self-aligned in the architecture. This means that the gap between the source and the drain electrodes created by the sandwiched layer of dielectric film is the same all along the periphery of the source-drain electrodes.
- (3) The Coulomb islands are positioned on the exposed side-wall of the dielectric film so that an island which is well positioned in between the source and the drain electrodes (like the one shown in Figure 3.3 (b) with the white arrow) will take part in electron transport. The lateral dimensions (L_x and L_y), therefore, are not of significance to the operation of the single-electron device. This liberty of arbitrarily choosing the lateral dimensions of the device allows us to use photolithography and associated CMOS based pattern definition processes, enabling large-scale fabrication.

When a Coulomb island is suitably positioned in between the source and the drain electrodes like the one shown in Figure 3.3 (c), a double barrier tunnel junction is formed between the electrodes and the island. What forms in the dashed box shown in Figure 3.1 (c) is a double junction single-electron tunneling device and it can be represented by an equivalent electrical circuit as shown. A gate electrode can also be incorporated in a double junction single-electron tunneling device as represented schematically in Figure 3.3 (d). In this, the gate electrode is electrically isolated from the source and drain electrodes as well as the Coulomb island by means of a dielectric. Such a three electrode system with a Coulomb island is forms a single-electron transistor. An equivalent circuit of a single-electron transistor is shown to the top left corner of Figure 3.3 (d).

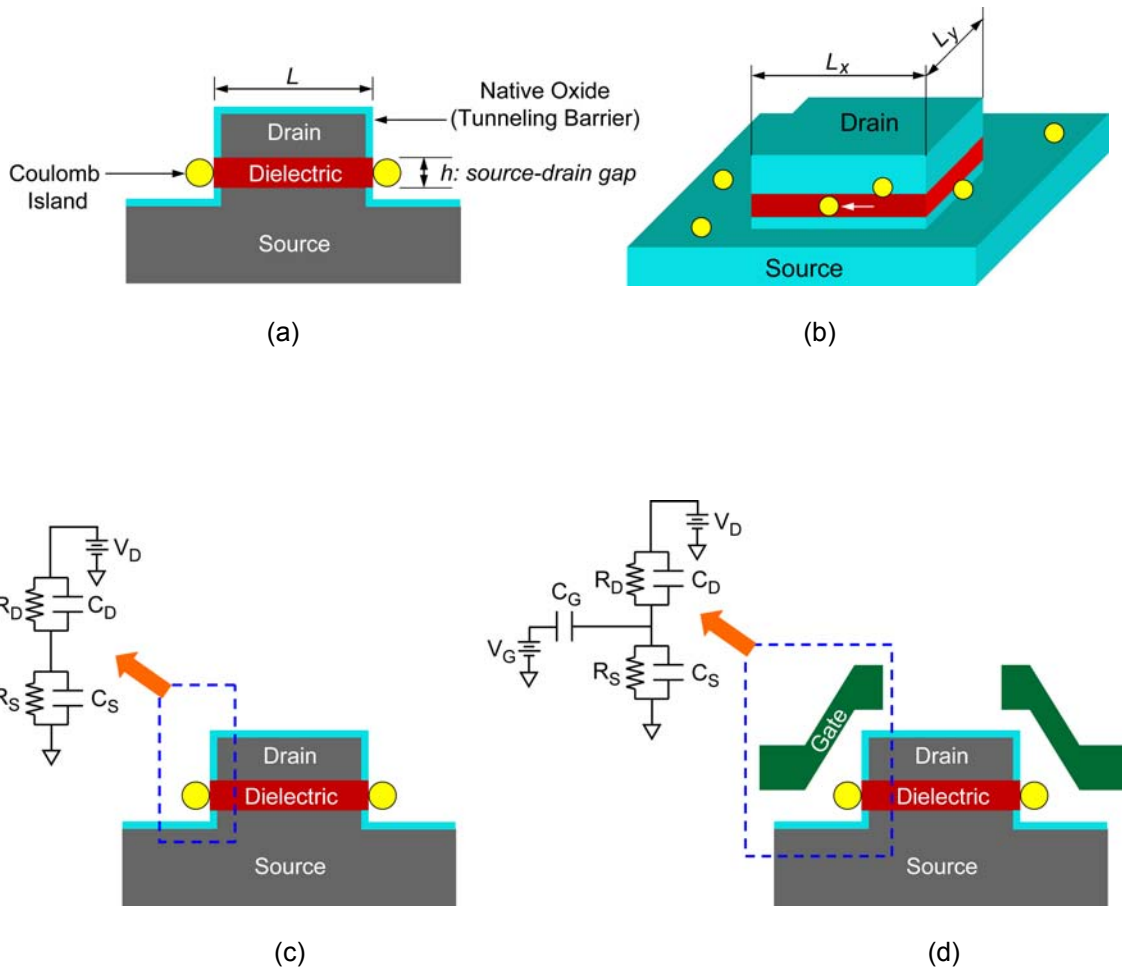


Figure 3.3 Schematic of the new single-electron device structure (a) Vertical arrangement of the source and the drain electrodes. The thickness of the intervening dielectric film (h) defines the source-drain electrode gap. (b) Isometric view of the single-electron device structure. The source and the drain electrodes are self-aligned so that the gap between the source and the drain is uniform along the periphery of the device. The lateral dimensions (L_x and L_y) can be of any dimension since the electron transport takes place only through an island positioned on the side-wall of the exposed dielectric layer (c) Schematic of a double junction single-electron tunneling device and its equivalent circuit (d) Schematic of a single-electron transistor and its equivalent circuit.

CHAPTER 4

FABRICATION OF SINGLE-ELECTRON DEVICES

4.1 Introduction

The detailed process of fabrication of single-electron devices will be described in this chapter starting from a 4 inch silicon wafer to finished devices ready for electrical characterization at room temperature and at cryogenic temperatures. Silicon wafers are used as substrates for making the devices which are fabricated using a combination of optical lithography, e-beam evaporation, plasma enhanced chemical vapor deposition (PECVD), self-assembled monolayers, RF magnetron sputtering, and reactive ion etching (RIE). The equipments used to fabricate these devices are described in detail in the University of Texas at Arlington's Nanofabrication Facility home page [4.1].

4.2 Thermal oxidation

A layer of silicon dioxide $\sim 1.5 \mu\text{m}$ thick is used to isolate the single-electron devices from the silicon wafer. Four inch silicon {100} wafers are first cleaned in an ultrasonic bath of acetone to dissolve out any organic impurities from the wafer surface typically for 5 minutes. The wafers are then blown dry in a stream of nitrogen gas. Oxidation is performed in a Minibrute oxidation furnace maintained at 1000°C . Initially the tube is purged with flowing nitrogen gas at 3 liters/minute. The silicon wafers are then slowly loaded in the furnace so as to avoid thermal shock. Wet oxidation of the wafers is then initiated by passing oxygen gas at 3 liters/minute through a bubbler containing DI water (resistivity $> 18.2 \text{ M}\Omega\cdot\text{cm}$) maintained at 90°C . Desired thickness of oxide is reached after 3 hours of oxidation following which the oxygen gas supply is cut off and nitrogen gas reintroduced to anneal the wafer and purge the furnace before unloading the wafers. The wafers are unloaded once the temperature of the furnace drops below 200°C . The oxide thickness formed is measured using Gaertner Ellipsometer.

4.3 Deposition of the source electrodes

Optical lithography is used to pattern the source electrodes on the substrates using photomask 1. Each oxidized wafer is cleaved diametrically into 4 quadrants prior to optical lithography. The samples are first rinsed in acetone followed by ashing in an UV-O₃ substrate cleaner (Novascan Inc.) for 30 minutes. This cleaning step is necessary to remove any organic contaminants that might have accumulated during the handling of the wafer pieces. Negative photoresist NR9-1000PY (Futurrex Inc.) is spun onto the substrates at 3000 rpm for 30 seconds. Pre exposure bake is carried out on the samples on a hot plate maintained at 150°C for 1 minute. Optical lithography is performed on an OAI (Model 806) contact mask aligner which uses a primary wavelength of 365 nm from a mercury short-arc lamp. The exposure time for the samples under UV light is 23 seconds. Immediately after exposure, the samples are baked on a hot plate at 100°C for 1 minute. The samples are then developed in resist developer RD-6 (Futurrex Inc.) typically for 12 seconds followed by rinsing in copious amounts of DI water (resistivity > 18.2 MΩ.cm). Wafers are then blown dry under a stream of nitrogen gas and loaded in an e-beam evaporator (CHA Industries). Chrome, which is used as the source electrode metal, is evaporated onto the substrates once the vacuum level inside the e-beam evaporator reaches $\sim 1 \times 10^{-7}$ Torr. 2000 Å of chrome is deposited at a rate of 3-4 Å/sec with an acceleration voltage of 10 KV for the electron beam. The samples are then unloaded and metal lift-off is done by ultrasonic agitation in an acetone bath typically for 15 minutes. Once the lift-off is complete, the wafers are blown dry under a stream of nitrogen and treated in the UV-O₃ cleaner for 30 minutes to remove any residual photoresist that might have been left behind after the lift-off process. Figure 4.1 (a) to 4.1 (e) schematically illustrates processes involving the patterning of the source electrodes. Figure 4.1 (f) is a 3-dimensional schematic showing the profile of the source electrode. An optical microscope image of the top view of the source electrode is shown in Figure 4.1 (g). Only one device unit is shown for clarity.

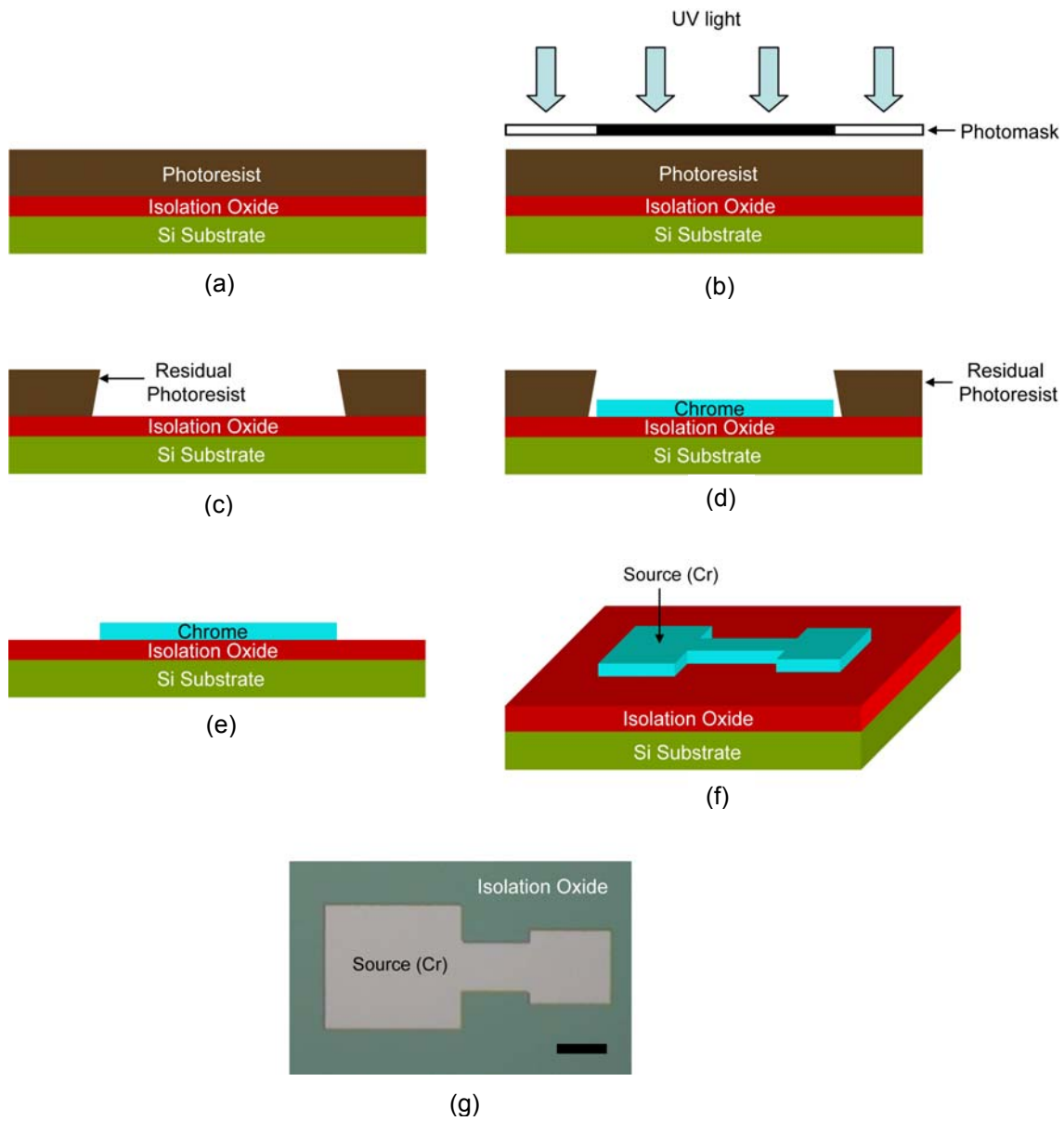


Figure 4.1 Deposition of the source electrodes. (a) Negative photoresist is spun onto the substrate and baked. (b) The wafers are exposed to UV light through photomask followed by a post-exposure bake. (c) Unexposed resist is removed by the developer. (d) Chrome is evaporated onto the samples. (e) Lift-off is done in acetone. (f) 3-dimensional schematic showing the profile of the source electrode. (g) Top view of a source electrode taken with an optical microscope. Scale bar = 100 μm .

4.4 Deposition of the silicon dioxide dielectric film

Silicon dioxide (SiO_2) deposited by plasma enhanced chemical vapor deposition (PECVD) is the dielectric layer which will create the nanometer scale gap between the source and the drain electrodes. Before deposition of SiO_2 , chamber preconditioning is required to ensure that the quality of the deposited film is within specifications. All components inside the PECVD reactor chamber are cleaned with isopropyl alcohol to physically remove particles that might have accumulated due to usage. The reactor chamber is then pumped down so that the vacuum level inside remains steady at ≤ 1 mTorr. The wafers which already have the source electrodes defined are then loaded and the deposition of PECVD SiO_2 is carried out using the following conditions:

- (1) Silane (SiH_4) flow rate – 7 sccm.
- (2) Nitrous Oxide (N_2O) flow rate – 179 sccm
- (3) Nitrogen (N_2) flow rate – 250 sccm
- (4) Reactor pressure – 1000 mTorr
- (5) Reactor temperature – 350°C
- (6) Power – 500 Watts

It must be mentioned that Argon is used as the carrier gas for SiH_4 and the percentage of SiH_4 in the SiH_4/Ar gas mixture is 15%. A film thickness of 110 Å is obtained with this recipe when the deposition is carried out for 19 seconds.

4.5 Deposition of the drain electrodes

Optical lithography is used to define the drain electrodes using a second photomask. After the deposition of the SiO_2 dielectric film, negative photoresist (NR9-1000PY) is spun onto the wafers at 3000 rpm for 30 seconds. Wafers are then baked at 150°C for 1 minute. Drain electrode patterns are aligned with the source electrodes and optical lithography is performed using the OAI mask aligner where the samples are exposed to UV light for 23 seconds. Post exposure bake is done at 100°C for 1 minute. Unexposed areas are developed using resist

developer RD-6 for 12 seconds. This is followed by rinsing the wafers thoroughly in DI water and drying under a stream of nitrogen gas. The samples are again loaded in the e-beam evaporator and 2000 Å of chrome is evaporated onto the structure as described in section 4.3. Lift-off is done by ultrasonic agitation in a bath of acetone for 15 minutes. Figure 4.2 (a) shows the schematic arrangement of the drain on top of the source electrode. The drain and the source electrodes are now separated by the SiO₂ layer which was deposited using PECVD as described in section 4.4.

4.5.1 Etching of the PECVD SiO₂ film

After lift-off, the wafers are treated in the UV-O₃ cleaner to remove residual photoresist. To obtain the exposed side-wall of the SiO₂ film between the electrodes, the PECVD SiO₂ is etched in a reactive ion plasma etcher (Trion Inc.) using the drain electrode as the hard mask. CF₄ is used as the etching gas. In the etcher chamber, two electrodes are used during the etching process. The top electrode creates the plasma required to carry out the etching process and the bottom electrode gives directionality to the plasma so that a vertical profile of the etched wall can be obtained. Following were the conditions used to etch the film:

- (1) CF₄ flow rate – 50 sccm
- (2) Process pressure – 20 mTorr
- (3) Top electrode power – 3000 W
- (4) Bottom electrode power – 50 W
- (5) Process time – 180 seconds

The SiO₂ film is intentionally overetched so as to remove all of the exposed PECVD SiO₂ and a small portion from the top of the source electrode of 10-20 nm in depth. Figure 4.2 (b) shows the schematic and Figure 4.2 (c) the SEM image of the single-electron device structure obtained after this etch process. The exposed side-wall of the PECVD SiO₂ (indicated by the yellow arrow) can be clearly seen from the SEM image. This film creates a uniform and nanometer scale insulating gap between the source and the drain electrodes.

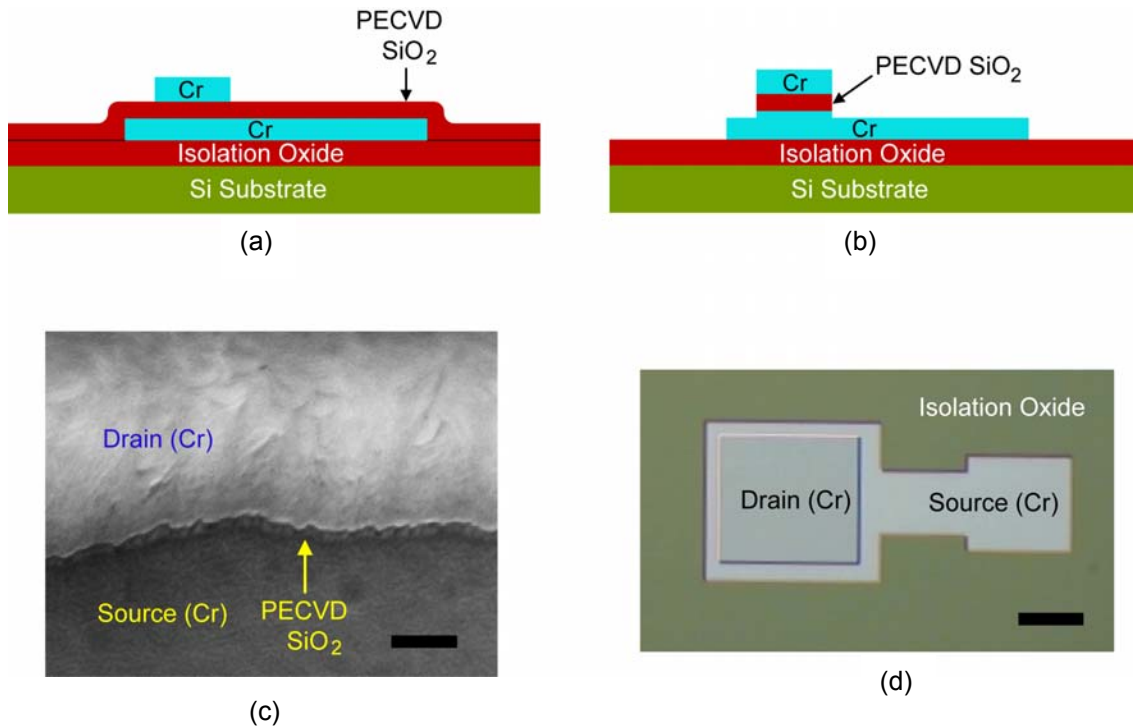
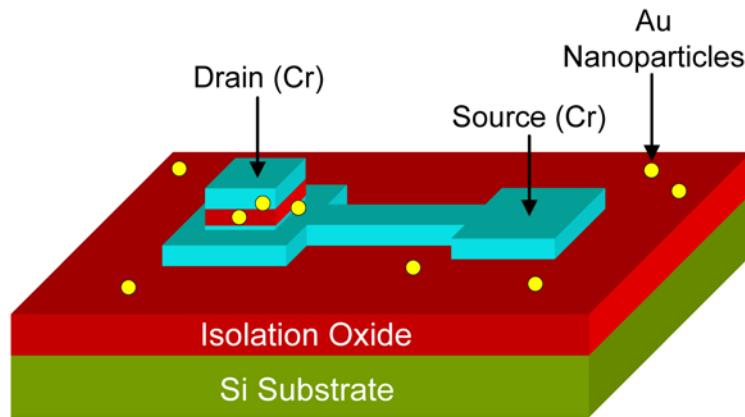


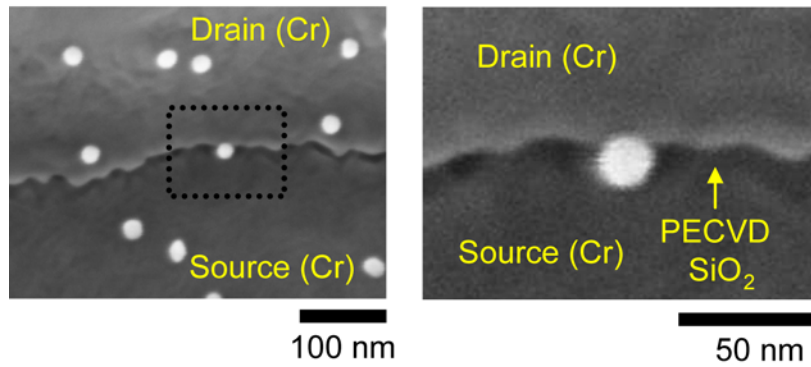
Figure 4.2 Deposition of the drain electrodes. (a) Schematic arrangement of the drain on top of the source electrode. The source and the drain electrodes are separated by the dielectric film of SiO₂ deposited by PECVD process. (b) The intervening layer of SiO₂ film between the electrodes is etched away using the drain electrode as the hard mask. The SiO₂ film that remains underneath the drain electrodes defines the gap between the source and the drain electrodes in the single-electron device structure. (c) SEM image of the device side-wall after the SiO₂ film has been etched. The yellow arrow indicates the remaining portion of the SiO₂ film which creates a uniform and nanometer scale gap between the source and the drain electrodes. Scalebar = 100 nm. (d) Optical microscope image (top view) of the single-electron device structure showing the arrangement of the drain electrode on top of the source electrode. Scalebar = 100 μ m.

4.6 Attachment of Au nanoparticles

For the single-electron devices, Au nanoparticles of diameters ~ 10 nm and ~ 20 nm are used as Coulomb islands. The positioning of the Au nanoparticles on the exposed side-wall of the PECVD SiO_2 so that they sit in the gap between the source and the drain electrodes is done using self-assembled monolayers (SAMs). After the SiO_2 film has been etched, the wafers are cleaned in the UV- O_3 cleaner for 30 minutes. A 1 mM solution of (3-aminopropyl)triethoxysilane (APTES; $(\text{C}_2\text{H}_5\text{O})_3\text{-Si-(CH}_2)_3\text{-NH}_2$) is prepared in chloroform. The wafers are then immersed in the solution for 30 minutes at room temperature followed by rinsing in chloroform and 2-propanol and drying under a stream on nitrogen gas. This forms a self-assembled monolayer (SAM) of APTES on the surfaces of chromium native oxide and the exposed side-wall of the PECVD SiO_2 . In an aqueous solution, the APTES SAMs provide a net positive charge on the surfaces over which they form [4.2, 4.3]. The Au nanoparticles are passivated by citrate ions and are negatively charged in the colloid. The APTES functionalized substrates are immersed in colloidal solutions of Au for 8-24 hours and 4-5 hours for ~ 10 nm and ~ 20 nm Au nanoparticles, respectively. The opposite charge polarities of the APTES SAMs and the Au nanoparticles attract resulting in their attachment of nanoparticles to the device surfaces. The wafers are treated in the UV- O_3 cleaner for 30 minutes to burn off the APTES monolayer, which (or their disintegrated components) could potentially act as charge-trapping sources. Figure 4.3 (a) shows the schematic of one single-electron device after the attachment of Au nanoparticles. Since the APTES monolayers forms on the exposed surface of chrome native oxide as well as the side-wall of PECVD SiO_2 , the attachment of the Au nanoparticles on the devices are random. So there is a probability that a nanoparticle will be positioned on the exposed side-wall of the PECVD oxide such that it is in correct tunneling range from both the source and the drain electrodes and participate in single-electron transport. Figure 4.3 (b) is a SEM image which shows one such Au nanoparticle in the dotted box. The magnified view of this Au nanoparticle sitting on the exposed side-wall of the PECVD SiO_2 is shown in Figure 4.3 (c).



(a)



(b)

(c)

Figure 4.3 Attachment of Coulomb islands on the single-electron device. (a) Schematic of a single-electron device after the attachment of Coulomb islands (Au nanoparticles). The attachment of the Au nanoparticles on the device is random. (b) SEM image of a single-electron device side-wall after the attachment of 20 nm Au nanoparticles (bright dots). The exposed side-wall of the PECVD oxide is the dark line separating the source and the drain electrodes. The dotted box shows a ~ 20 nm Au nanoparticle which is good candidate for single-electron transport. (c) A magnified view of the dotted box in (b). The sample stage is tilted at an angle of 30° from the vertical during imaging. So the thickness of the PECVD SiO_2 appears two times ($1/\sin 30^\circ$) smaller than actual.

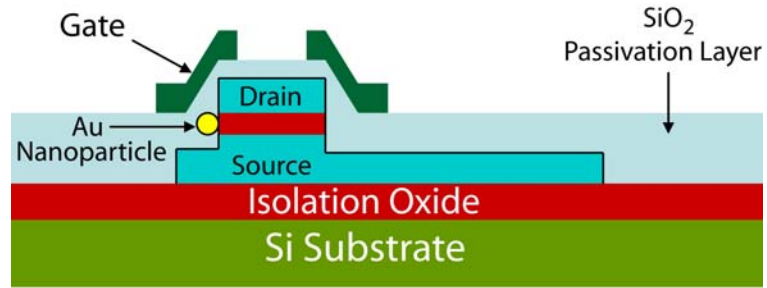
4.7 Deposition of the gate electrodes

Immediately after the attachment of the Au nanoparticles and removing the monolayer of APTES in a UV-O₃ atmosphere, the samples are passivated with a layer of SiO₂ of ~ 250 nm thickness. This passivation is done either using sputtered SiO₂ or thermally evaporated SiO₂.

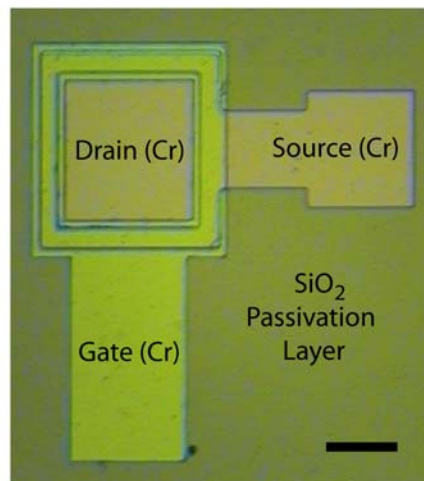
For passivation using sputtered SiO₂, the wafers are loaded in a sputtering chamber which is pumped down till the base pressure reaches ~ 1×10^{-6} Torr. Argon gas is flowed into the chamber at 37.5 sccm. A RF power of 80 Watts and a process pressure of 10 mTorr are used for the sputtering process. A thickness of ~ 250 nm is obtained after 90 minutes of sputtering.

For passivation of the devices using e-beam evaporation, 99.99% pure SiO₂ pieces (Kurt. J. Lesker) are put in a graphite crucible and loaded in the e-beam evaporator (CHA Inc.) The chamber is evacuated till the pressure reaches ~ 1×10^{-7} Torr. 250 nm of SiO₂ is evaporated at a rate of 3-4 Å/sec with an acceleration voltage of 10 KV for the electron beam.

Optical lithography is used to define the gate electrodes. After passivation of the devices, negative resist (NR9-1000PY) is spun onto the wafers at 3000 rpm for 30 seconds. This is followed by baking the wafers on a hot plate at 150°C for 1 minute. A third photomask is used to define the gate electrodes. The gate electrode patterns are aligned to the underlying source and drain electrodes so that they form a continuous band around the drain electrodes as illustrated schematically in Figure 4.4 (a). Exposure to UV light is done in the mask aligner (OAI) for 23 seconds followed by a post exposure bake at 100°C for 1 minute. Unexposed photoresist is removed by developing in resist developer RD-6 for 12 seconds followed by rinsing the wafers thoroughly in DI water and drying under nitrogen gas. The wafers are again loaded in the e-beam evaporator and ~ 3500 Å of chrome is evaporated using the same parameters as described in section 4.3. Lift-off is done by ultrasonic agitation in an acetone bath for 15 minutes. Figure 4.4 (b) is an optical microscope image showing the top view of the single-electron device after the gate electrodes have been defined.



(a)



(b)

Figure 4.4 Deposition of the gate electrodes for a single-electron transistor (a) Schematic illustration of the position of the gate electrode with respect to the source electrode, the drain electrode and the Coulomb island (Au nanoparticle) in a single-electron transistor. Schematic not to scale. (b) Top view of device structure after the definition of the gate electrode. Scale bar = 100 μm .

4.8 Deposition of bond pads for the single-electron devices

After the deposition of the gate electrodes, any residual photoresist that might have been left behind after lift-off is removed by UV-O₃ treatment for 30 minutes. The wafers are then passivated with another layer of e-beam evaporated SiO₂ of thickness ~ 750 nm using the parameters as described in section 4.7.

4.8.1 Formation of vias

A combination of photolithography and reactive ion etching is used to create vias in the single-electron device structure. After the devices have been passivated with e-beam evaporated SiO₂ for the second time, negative photoresist (NR9-1000PY) is spun onto the wafers at 2000 rpm for 30 seconds. Pre exposure bake is done on a hot plate maintained at 150°C for 1 minute. A fourth photomask defines the patterns of the vias which were aligned to underlying source, drain and gate electrodes. The samples were exposed to UV light for 26 seconds followed by a post exposure bake at 100°C for 1 minute. Unexposed resist was removed by immersing the samples in resist developer (RD-6) for 12 seconds followed by rinsing in DI water and drying under a stream of nitrogen. This photolithography step creates small wells devoid of photoresist each of which is directly above a source, drain or gate electrode.

Wafers are then loaded in the reactive ion etching chamber (Trion Inc.) and the exposed part of the passivated SiO₂ layer is etched using the following conditions:

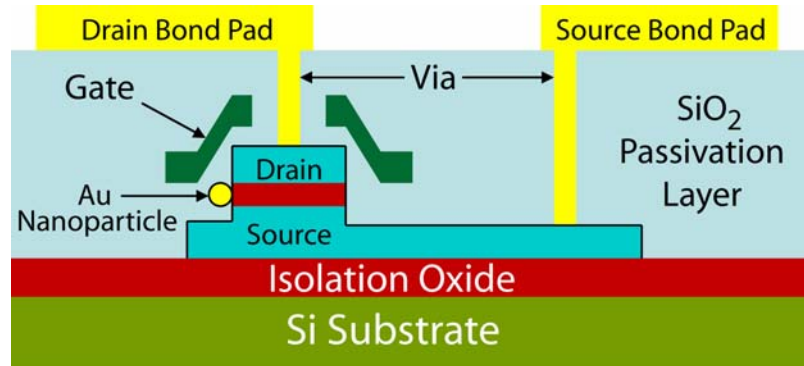
- (1) CF₄ flow rate – 50 sccm
- (2) Process pressure – 20 mTorr
- (3) Top electrode power – 3000 W
- (4) Bottom electrode power – 50 W
- (5) Process time – 240 seconds

The photoresist is also consumed during the plasma etching of SiO₂ using CF₄ chemistry. So, this photolithography step used to define the via patterns and the etching of the SiO₂

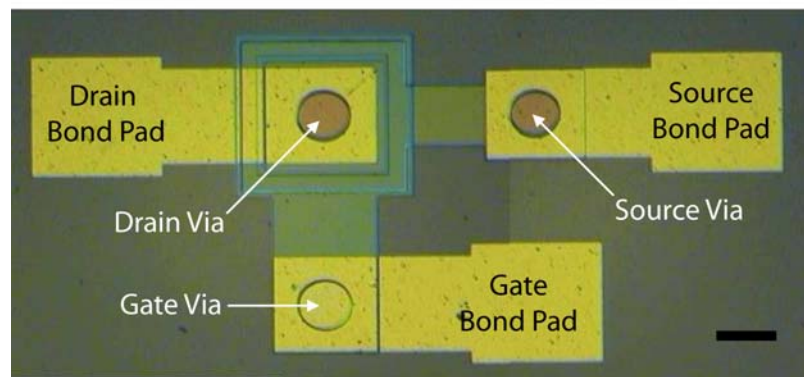
passivation layer have to be repeated till the vias reach the underlying chrome electrodes which also act as the etch stop layer.

4.8.2 Deposition of the bond pads

Photolithography and a fifth photomask is used to pattern the bond pads of the single-electron devices. After the vias have been etched, a layer of negative photoresist (NR9-1000PY) is spun onto the wafers at 2000 rpm for 30 seconds followed by baking on a hot plate at 150°C for 1 minute. Wafers are then aligned in the OAI mask aligner and the samples are exposed to UV light through the fifth photomask for 23 seconds. A post exposure bake at 100°C is carried out followed by developing in resist developer (RD-6) for 12 seconds. DI water is used to thoroughly rinse the wafers which are then dried under a stream of nitrogen. The wafers are then loaded in the e-beam evaporator (CHA Inc.) and the chamber is evacuated till the pressure reaches 1×10^{-7} Torr. 400 Å of chrome and 4500 Å of gold are evaporated at the rate of 3-4 Å/sec. Lift-off of is done by first immersing the wafers in acetone for 1 hour followed by ultrasonic agitation in an acetone bath for 15 minutes. Figure 4.5 (b) shows the optical microscope image of a completed single-electron transistor. The three bond pads of the single-electron transistor are the yellow areas of the device. The chrome and gold which was evaporated after the bond pads were patterned fill up the vias to make electrical contact with the source, drain and gate electrodes which are buried underneath the passivation layer of SiO₂.



(a)



(b)

Figure 4.5 Etching of vias and deposition of bond pads of a single-electron transistor. (a) Schematic illustration of vias and bond pads in a single-electron transistor. (b) Optical microscope image showing the top view of a completed single-electron transistor. Scale bar = 100 μm .

4.9 Mounting individual dies on a chip carrier

For electrical characterization of the single-electron devices at cryogenic temperatures, it is a requirement that they be mounted on suitable chip carriers. After the bond pads have been defined, the wafer is diced into individual dies of dimensions 0.8 cm × 0.8 cm. This is done by marking out the periphery of an individual die using a diamond scribe. Care should be taken to avoid touching any of the features on the die during the scribing process. The die is then carefully cleaved from the parent wafer along the scribed lines using Teflon tweezers so that none of the device features are touched with the tweezers. The individual dies are treated in UV-O₃ atmosphere for 30 minutes to ensure clean surfaces. This step is especially necessary at this stage so that the device bond pads are free of any organic contaminants which will ensure good wire bonding of the device in the next step.

Ceramic chip carriers (CCF06404; Kyocera) were used for mounting the dies containing the single-electron devices. These chip carriers were chosen for the application because of the high thermal conductivity and good electrical insulation properties of the ceramic. Conducting silver paste (SPI supplies brand) was used to adhere the individual dies on the chip carrier. A drop of silver paste was put in the chip carrier cavity immediately followed by picking up the die with a Teflon tweezers by the edges and carefully placing it in the middle of the chip carrier cavity so that the die is not in contact with the edges of the cavity. The chip carrier with the die mounted in it is allowed to dry for 3-4 hours under ambient conditions. Figure 4.6 shows a photograph of an individual die that has been mounted on a chip carrier. The die contains an array of 60 single-electron transistors. The devices are now ready to be wire bonded for electrical measurements.

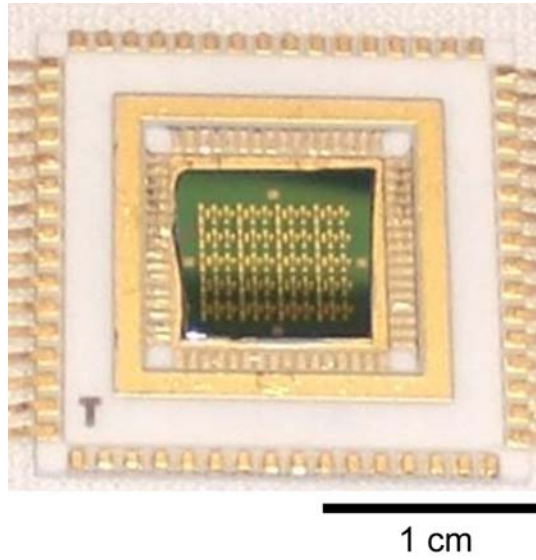


Figure 4.6 An individual die containing an array of 60 single-electron transistors that has been mounted on a chip carrier.

4.10 Device wire bonding

After the die has been securely adhered onto the chip carrier, the bond pads of the device have to be bonded to pre-designated legs of the chip carrier. If not done properly, the wire bonding process can potentially short circuit the single-electron devices through electrostatic discharge ultimately leading to their failure. Certain precautions need to be followed in order to successfully wire bond the devices as are explained below.

Figure 4.7 (a) shows a view of the Wedge Bonder (West Bond Model 7476E) used to bond the single-electron devices. After turning the system on, the electrically conducting parts of the wire bonder with which the chip carrier will be in physical contact during the bonding process (i.e., the chuck and the stylus) has to be connected to an electrical ground to remove any static charge that might have built up. This is done in the following manner: the operator first wears an anti-static wrist strap (Radioshack Corp.) (not pictured) and connects the free end of the strap to an earth ground. Another length of multi-strand copper wire as shown in the image is taken with one end connected to the same earth ground as the wrist strap. The free end of the copper wire is now touched one by one to the chuck and the stylus to remove any static electricity from the wire bonder.

After this is completed, the chip carrier containing the array of devices is mounted on the chuck with the wrist strap still securely fastened to the operator's hand. Figure 4.7 (b) shows the image of the wire bonder with a chip carrier mounted on the chuck. The copper wire which is connected to the earth ground is now touched individually to all the legs of the chip carrier to remove any static charge built up in the carrier itself. Extreme precaution should be exercised so that the grounding wire does not touch the die or any of the devices on it.

With the static charge eliminated from the wire bonder and the chip carrier, it is now safe to wire bond the device bond pads to the legs of the chip carrier.

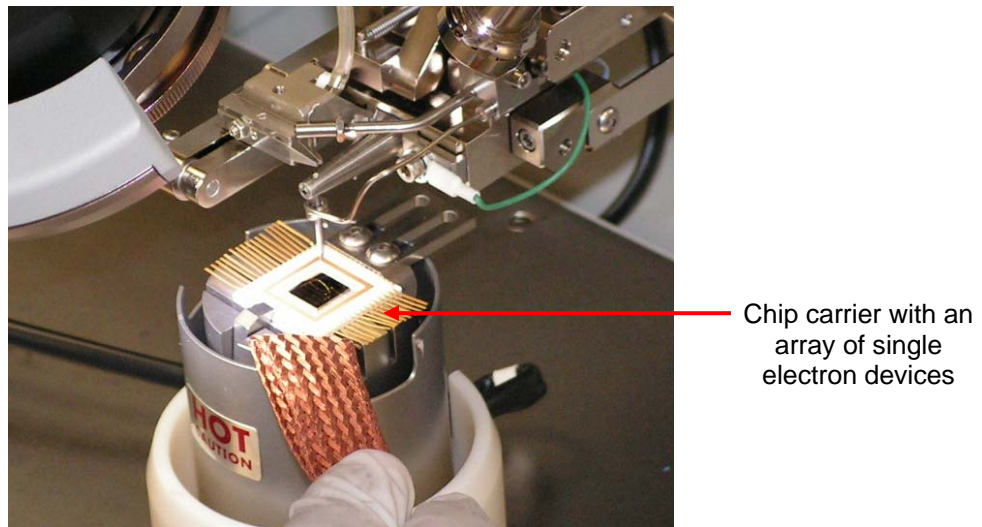
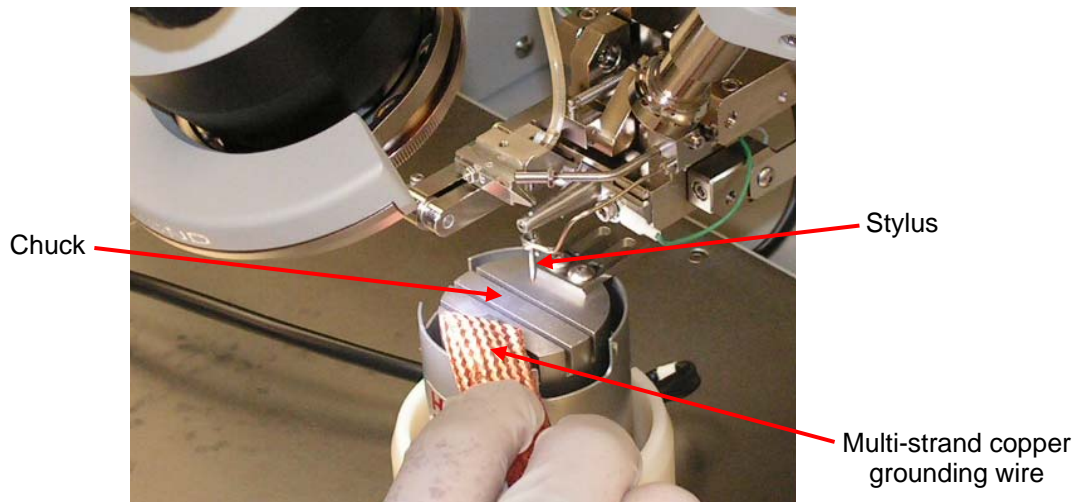


Figure 4.7 Removal of static charge before wire bonding. (a) Static charge built up is removed from the wire-bonder body by connecting its electrically conducting surfaces to an earth ground. (b) Static charge is removed from the chip carrier (with a die mounted on it) by touching the legs of the carrier to an earth ground.

Figure 4.8 shows the schematic layout of the chip carrier. For clarity, only one completed single-electron transistor is shown in the chip carrier cavity. Initially, the carrier has 64 legs in total (16 on each side of the square periphery). For the sake of mounting convenience, the legs from the top and the bottom edge of the carrier are cut off. A spool of gold wire (99.99%) of diameter 25 μm is used to connect the bond pads of the single-electron transistors to the legs of the chip carrier.

A successful bond is a combination of two bonding steps; the first one on the bond pad of the device and the second one on the leg of the chip carrier. Also, the stage holding the chip carrier should be moved only in directions parallel to the direction of the wire feed to avoid wire entanglement. Following these procedures, the source bond pad is connected to legs R1 and R5, the drain bond pad to legs L1 and L5, and the gate bond pads to legs L11 and L15, respectively of the chip carrier as shown in the schematic. This convention of bonding particular bond pads to pre-designated legs should always be maintained to match the sequence in which the electrical connections have been soldered inside the cryostat (details of which are given in Chapter 5).

The following conditions were used for the wire bonding process:

- (1) Ultrasonic power for bond 1 = 400 mW
- (2) Ultrasonic power for bond 2 = 450 mW
- (3) Bond time for bond 1 = 40 ms
- (4) Bond time for bond 2 = 40 ms
- (5) Loop height = 150 μm
- (6) Wire pull = 50 μm
- (7) Wire tail = 36 μm
- (8) Temperature used during bonding = 75 $^{\circ}\text{C}$.

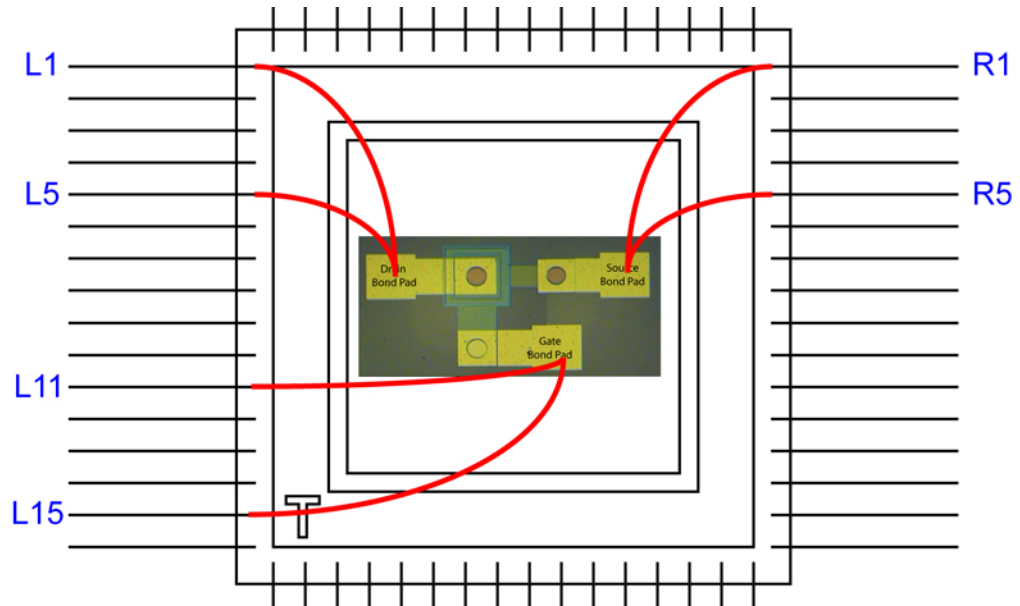


Figure 4.8 Schematic layout of a chip carrier with a single-electron transistor wire bonded to predesignated legs of the chip carrier. Only one completed single-electron transistor is shown in the carrier cavity for clarity. The source bond pads are bonded to legs R1 and R5, the drain bond pads to L1 and L5 and the gate bond pads to L11 and L15, respectively.

CHAPTER 5
ELECTRICAL CHARACTERIZATION OF SINGLE-ELECTRON DEVICES

5.1 Introduction

This chapter will focus exclusively on the electrical characterization of the single-electron devices at temperatures ranging from 10 K to 315 K. The room temperature electrical characterization of the single-electron devices was done using an Agilent 4155 C semiconductor parameter analyzer and the variable temperature measurements were done using an Agilent 4157 B semiconductor parameter analyzer. For measuring the electrical characteristics of our single-electron devices, Kelvin (4-wire) connections [5.1] were used to eliminate the residual resistance effects of the test leads and contacts. Figure 5.1 shows the schematic of the Kelvin connection used for the single-electron devices. In this configuration, the current is forced through the device under test (DUT) through the Force leads while the voltage across the DUT is measured through a second set of leads known as the Sense leads. Although some small current may flow through the sense leads, it is usually negligible and can be ignored for all practical purposes. To cancel the effects of the residual resistance, the test leads are connected as close to the DUT as possible.

For the electrical measurements, a sweep measurement mode [5.1] was used as shown in Figure 5.2. In this, the voltage was the stimulant and the current in the device was the measurand. The following parameters were used for the sweep mode:

- (1) Hold Time = 30 seconds
- (2) Delay Time = 10 seconds
- (3) Step Delay Time = 10 seconds
- (4) Integration Time = High for Agilent 4155 C; 1000 for Agilent 4157 B.

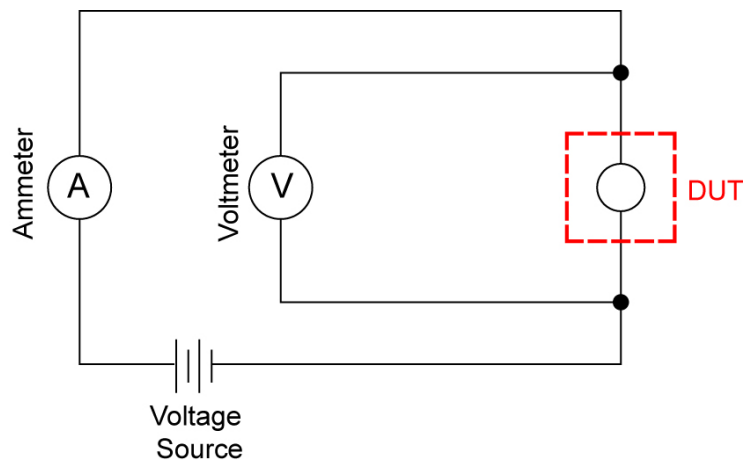


Figure 5.1 Schematic of Kelvin (4-wire) resistance measurement used for the electrical characterization of single-electron devices.

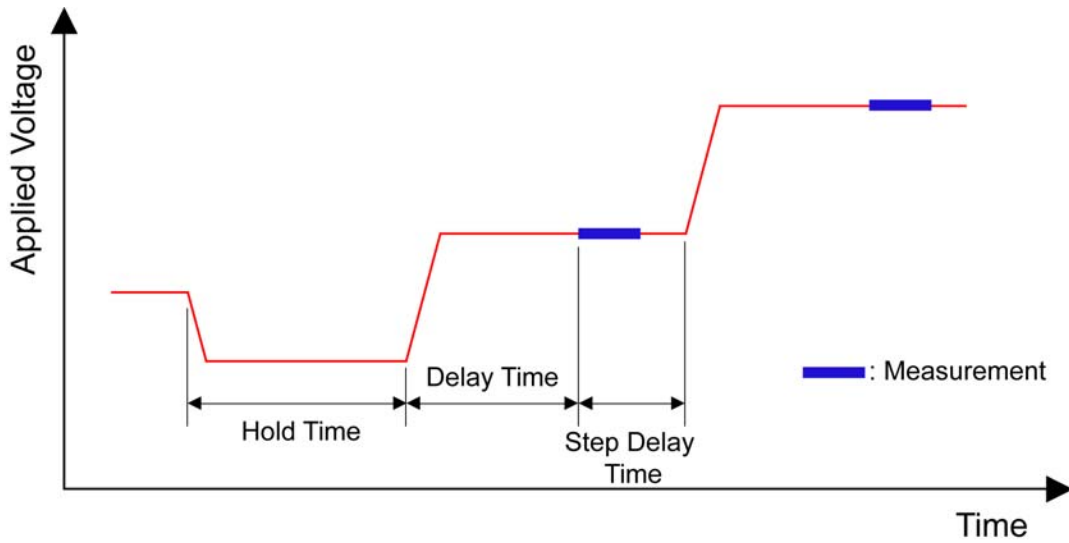


Figure 5.2 Schematic of the sweep measurement mode used for the electrical characterization of single-electron devices.

5.1.1 Room temperature measurement set-up

Figure 5.3 shows the schematic diagram of the measurement setup for the room-temperature electrical characterization of single-electron devices using Agilent 4155 C semiconductor parameter analyzer. For the room-temperature measurements, it is not required to wire bond the devices. The bond pads of the device are connected to the parameter analyzer using probe tips as shown in the figure. The probe tips are connected to the SMUs of the parameter analyzer using central conductor of low noise triaxial cables. The outer shield of these triaxial cables are connected to the chassis of the acoustic box. For best results, the parameter analyzer is switched on allowed to warm up for 30 minutes. The chuck and the acoustic box are connected to the same earth ground as the parameter analyzer. Before placing the wafer containing the single-electron devices on the chuck, it is freed from any static by touching one end of a multistrand copper wire on it and the end to an earth ground.

The computer controlled data acquisition system allows the measurement of the source-drain current as a function of the applied source-drain bias voltage and the gate voltage. The source-drain bias and the gate voltage are controlled by the computer using a GPIB protocol. Before the measurements are carried out on the actual devices, it is important to measure the noise in the set-up which is done in the following manner: In the absence of a device, the source-drain bias is held constant at 400 mV and the current monitored. In the best case scenario, the noise level for the set-up is <1 pA.

The wafer is then placed on the chuck and the source probe tip, drain probe tip, and the gate probe tip is touched to the source, drain, and gate bond pads, respectively in that order. Electrical measurement of the device is carried out using the sweep measurement mode described previously. After the measurement of a device is over, the gate, drain, and source probe tips are lifted up from the bond pads in that order. The chuck is moved so that the next device to be characterized moves into position. The probe tips are lowered down on their respective bond pads and the measurement is repeated.

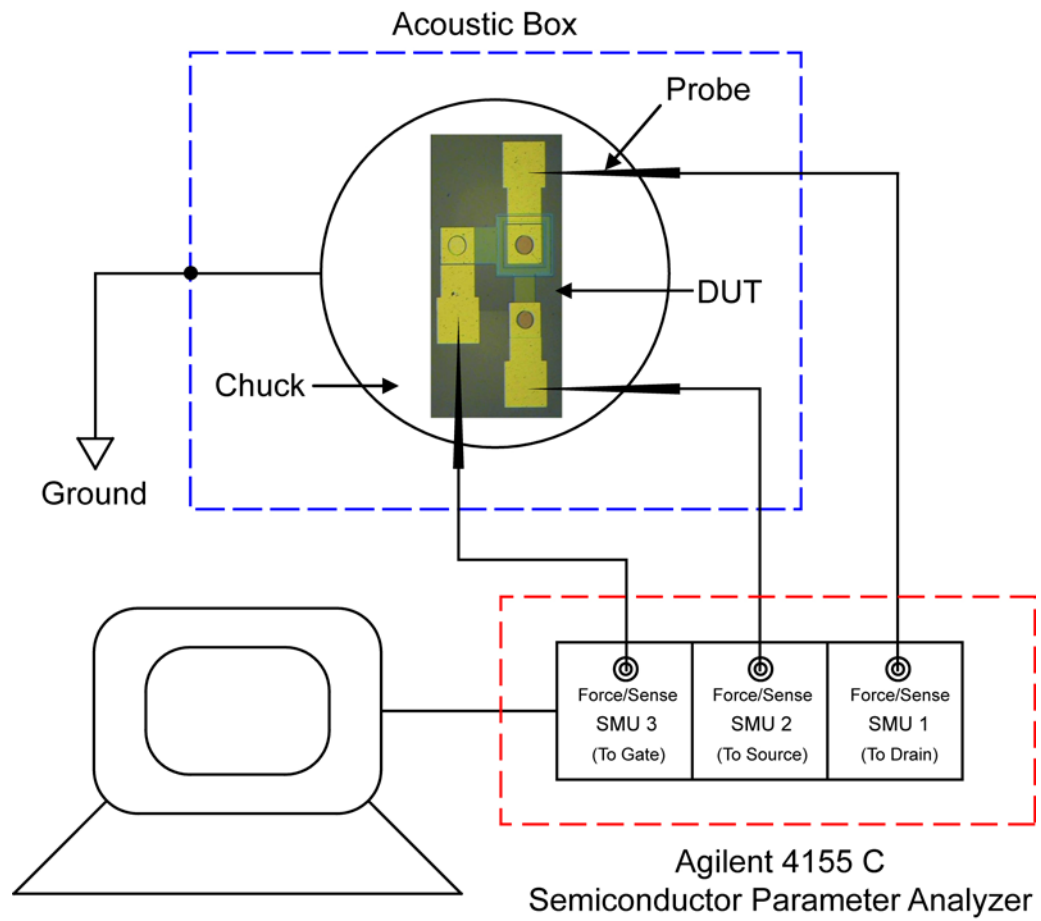


Figure 5.3 Schematic diagram of the room-temperature measurement set-up of single-electron devices.

5.1.2 Low temperature measurement set-up

Figure 5.4 shows the schematic front view of the cryostat used to cool the single-electron devices for electrical characterization at low temperatures. The cryostat stage is machined out of a block of oxygen free high conductivity copper. The machined stage is then gold plated so as to prevent the exposed copper surfaces from being oxidized under ambient conditions.

A multi-pin chip carrier socket is securely attached to the cryostat stage using low-temperature epoxy as shown in Figure 5.4. This multi-pin socket accommodates the single-electron devices which have been mounted on a chip carrier and wire bonded to the designated legs as was described previously in section 4.10. The legs of the multi-pin chip carrier socket are connected to one of the 10-pin electrical feedthroughs of the cryostat using cryogenic wire. The schematic of the connection from the chip carrier socket to the 10-pin electrical feedthrough is shown in Figure 5.5. The 10-pin electrical feedthrough has connections labeled A, B, C, D, E, F, G, H, and J for soldering convenience. Looking from the front-on position at the multi-pin chip carrier socket so that its legs are facing away from the observer, the legs are numbered from L1 to L16 and from R1 to R16 as shown in Figure 5.5. The following connections are now made between the legs of the chip carrier socket and the 10-pin electrical feedthrough of the cryostat using the cryogenic wire.

- (a) Leg L1 of the chip carrier socket is connected to connection A of the feedthrough.
- (b) Leg L5 of the chip carrier socket is connected to connection B of the feedthrough.
- (c) Leg L11 of the chip carrier socket is connected to connection F of the feedthrough.
- (d) Leg L15 of the chip carrier socket is connected to connection G of the feedthrough.
- (e) Leg R1 of the chip carrier socket is connected to connection D of the feedthrough.
- (f) Leg R5 of the chip carrier socket is connected to connection C of the feedthrough.

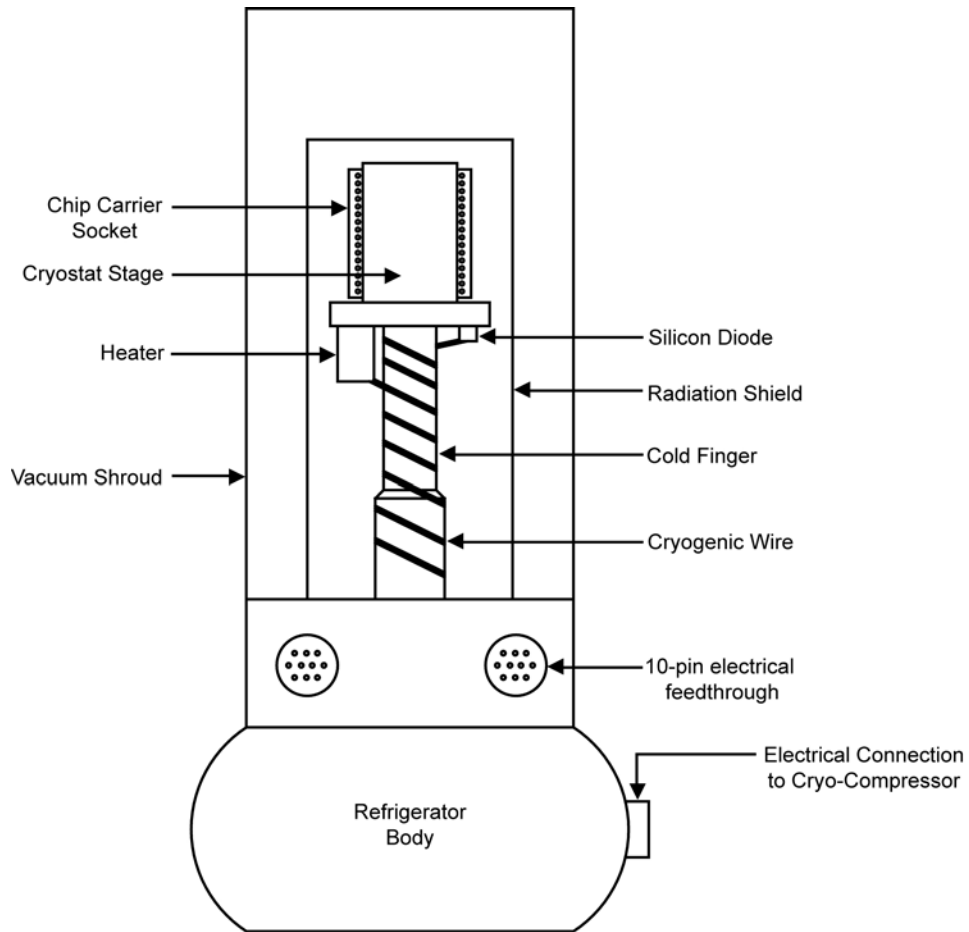


Figure 5.4 Schematic front view of the cryostat used for the electrical characterization of single-electron devices at low temperatures.

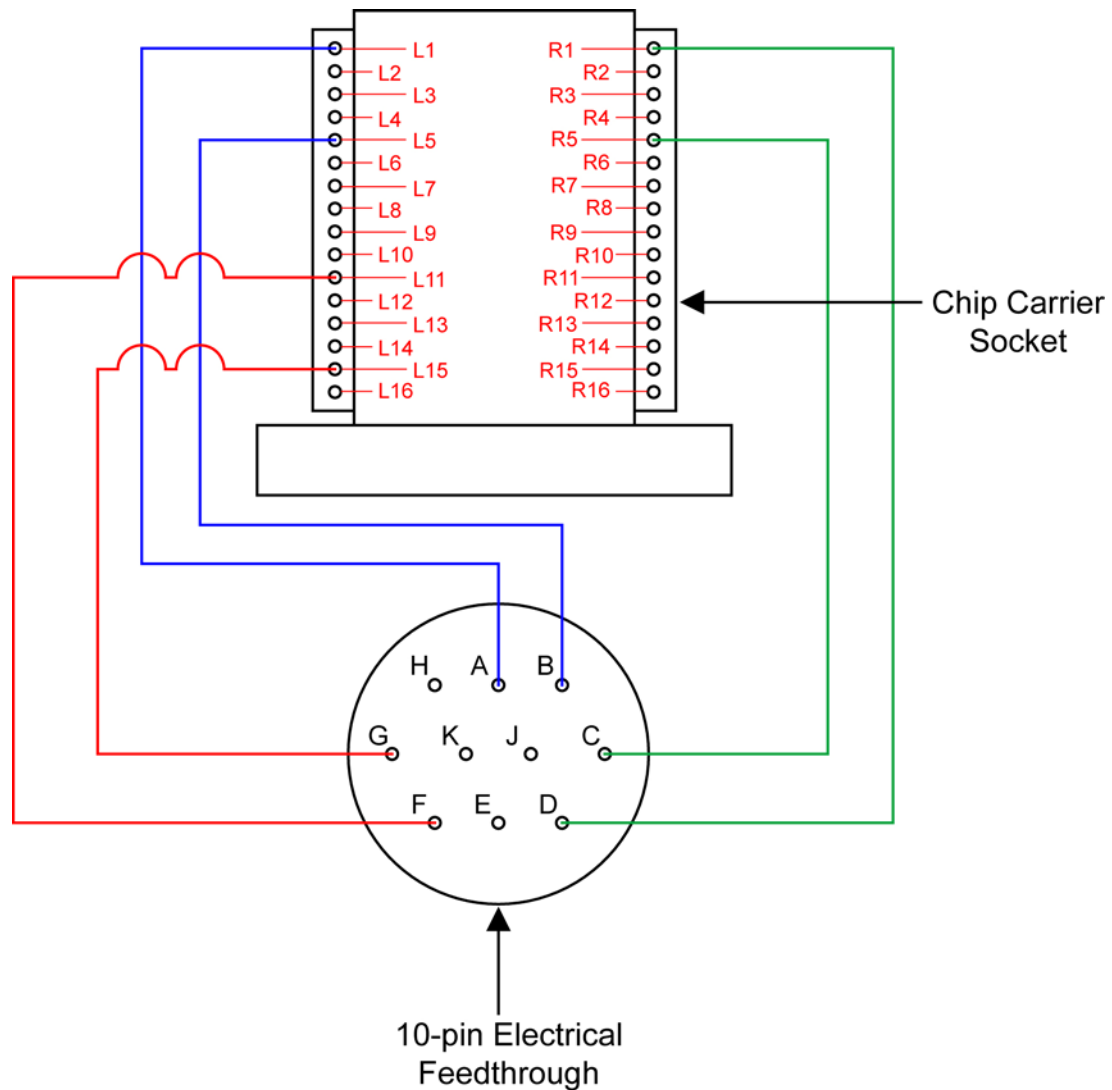


Figure 5.5 Schematic of the connections between the legs of the multi-pin chip carrier socket of the cryostat and a 10-pin electrical feedthrough attached to the cryostat body.

The cryogenic wire can be a significant source of electrical noise if it not properly heat sunk. The goal of heat sinking is to cool the wire to a temperature as close to the DUT as possible. This can be accomplished by wrapping a significant length of the wire around the cold finger. By doing this, the wire will be in thermal contact with the cooled surface thereby reducing the noise during measurement. In our cryostat, the wires are adhered to the cold finger of the cryostat by winding it around the cold finger first and then holding them in contact using cryogenic tape.

The connections between the 10-pin electrical feedthrough attached to the cryostat body and the SMUs of the Agilent 4157 B semiconductor parameter analyzer is made using male triaxial connectors (CS-631; Keithley Instruments Inc.), low-noise triaxial cables (SC-22; Keithley Instruments Inc.), and a 10-slot adapter for the electrical feedthrough (AEI 851-06EC12-10S50; Souriau Connection Technology). The 10-slot adapter also has connections labeled A, B, C, D, E, F, G, H, and J which correspond to the same connections as on the 10-pin electrical feedthrough on the cryostat body. Figure 5.6 shows the wiring diagram between the 4157 B parameter analyzer and the 10-slot adapter. The following connections are made between the parameter analyzer and the 10-slot adapter.

- (a) The first triaxial connector is connected to Sense lead of the HRSMU of 4157 B. The central conductor of the free end of the triaxial cable is soldered to the connection A of the 10-slot adapter.
- (b) The second triaxial connector is connected to the Force lead of the HRSMU of 4157 B. The central conductor of the free end of the triaxial cable is soldered to the connection B of the 10-slot adapter.
- (c) The third triaxial connector is connected to the Force lead of the MPSMU of 4157 B. The central conductor of the free end of the triaxial cable is soldered to the connection G of the 10-slot adapter.

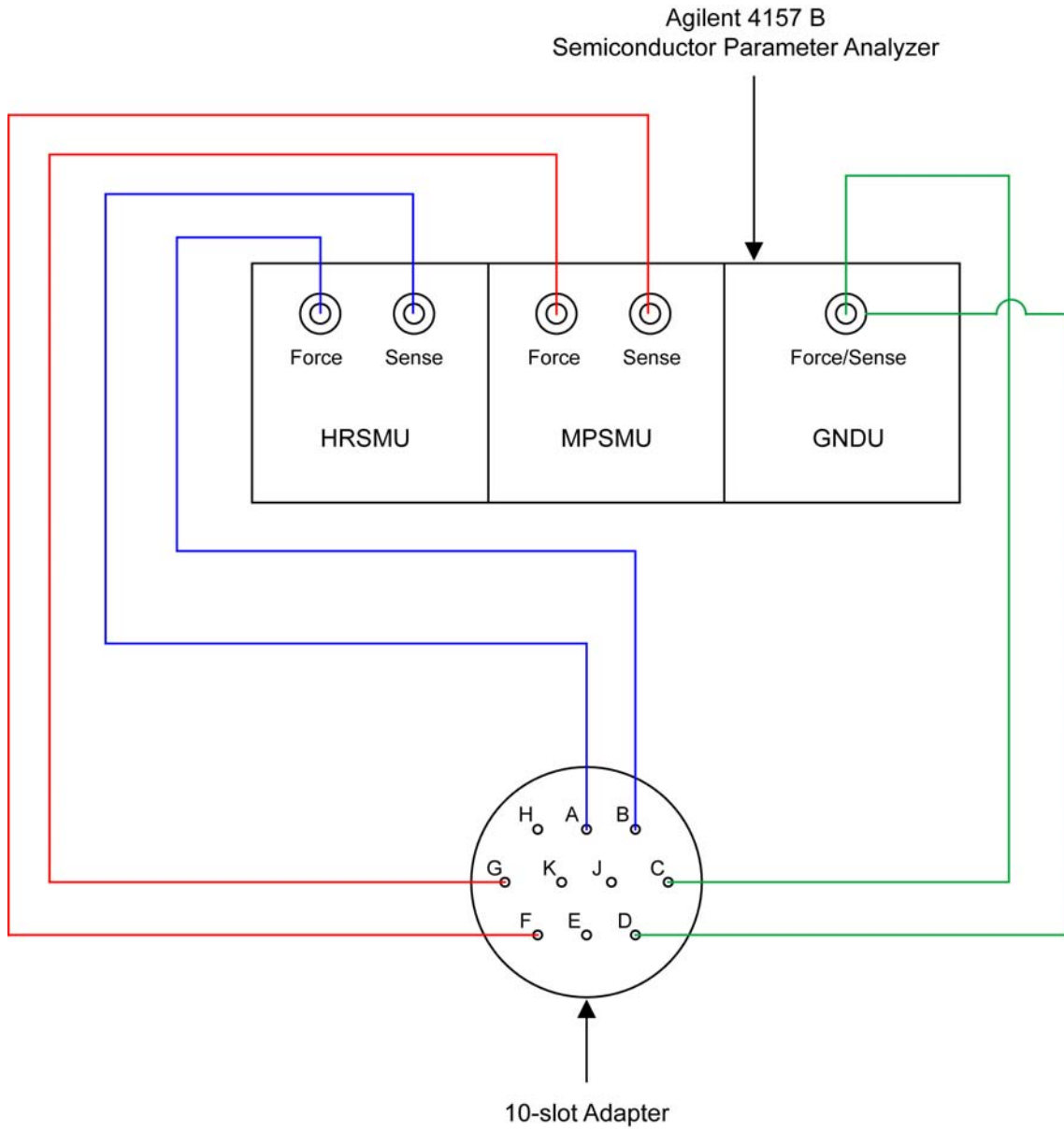


Figure 5.6 Wiring diagram between the 4157 B semiconductor parameter analyzer and the 10-slot adapter.

- (d) The fourth triaxial connector is connected to the Sense lead of the MPSMU of 4157 B. The central conductor of the free end of the triaxial cable is soldered to the connection F of the 10-slot adapter.
- (e) The fifth triaxial connector is connected to the Force/Sense lead of the GNDU of 4157 B. The central conductor of the free end of the triaxial cable is soldered to the connection C of the 10-slot adapter and the middle conductor of the free end of the triaxial cable is soldered to the connection D of the 10-slot adapter.

During soldering of the free end of the triaxial cables to the 10-slot adapter, extreme care should be exercised so that all three conductors of a triaxial cable come as close to the 10-slot adapter as possible but only the conductors described in (a) – (e) above are soldered to the 10-slot adapter. In our configuration, the outer shield and the middle guard of the triaxial cables come to ~ 5 mm of the soldering connections for the 10-slot adapter. This ensures good noise shielding during the electrical measurement of the single-electron devices. If the shield and the guard lines are separated, for example, by ~ 10 mm from the soldering connections of the 10-slot adapter, the peak-to-peak noise level during the measurement reaches values of ~ 1nA. For the measurement of our devices, a peak-to-peak noise level of < 1pA is desirable.

Underneath the cryostat stage, a heater is attached so that the electrical characterization of the single-electron devices can be done at various temperatures. There is also a silicon diode sensor attached to the cryostat stage which is used to monitor the temperature at which the electrical characterization of the device is being carried out. The heater and the sensor are connected to a Lake Shore Model 331 Temperature Controller. Connections are first made between the heater and the silicon diode to the other 10-pin electrical feedthrough of the cryostat body and then between the electrical feedthrough and the temperature controller. Figure 5.7 shows the wiring diagram from the heater and the silicon diode sensor to the 10-pin electrical feedthrough.

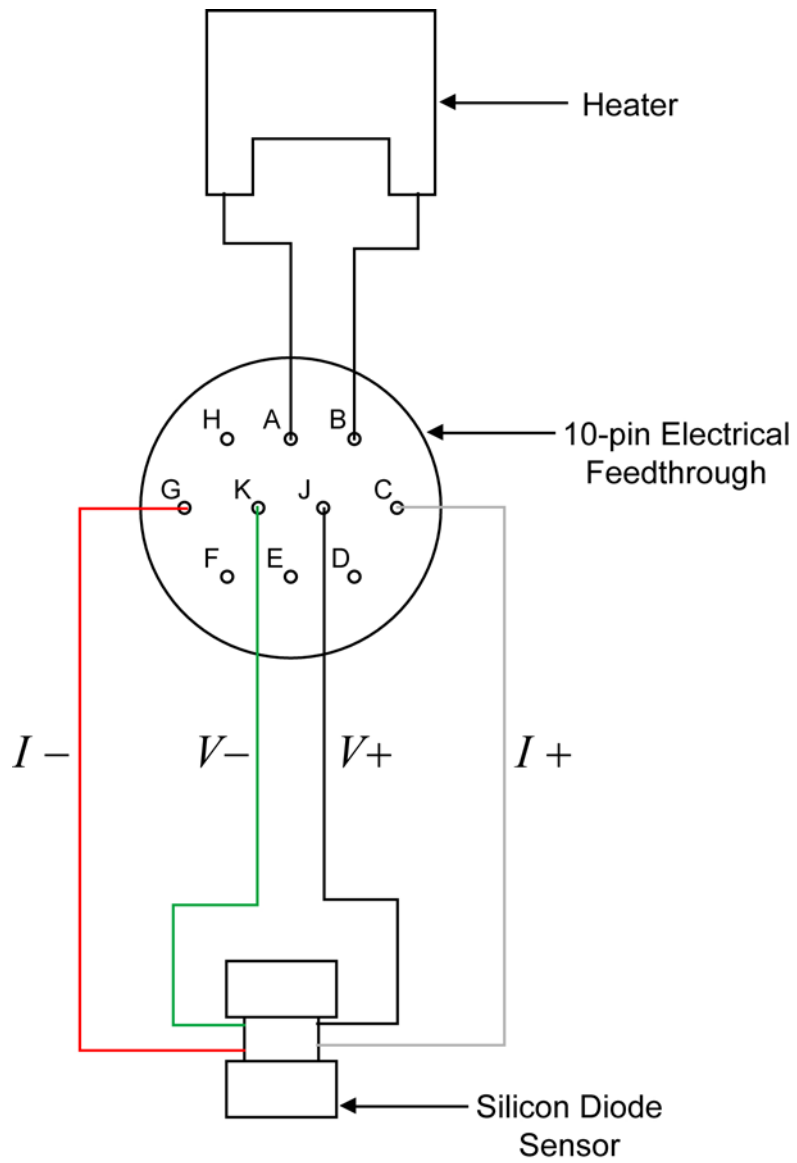


Figure 5.7 Wiring diagram from the heater and the silicon diode sensor to the 10-pin electrical feedthrough on the cryostat body.

The silicon diode sensor is a 4 – lead sensor. Each lead is color coded and should go to a predesignated pin on the temperature controller. The connections between the silicon diode and the 10-pin electrical feedthrough are made as follows:

- (a) The Red lead from the silicon diode corresponding to $I -$ is soldered to connection G of the 10-pin electrical feedthrough.
- (b) The Green lead from the silicon diode corresponding to $V -$ is soldered to the connection K of the 10-pin electrical feedthrough.
- (c) The Black lead from the silicon diode corresponding to $V +$ is soldered to the connection J of the 10-pin electrical feedthrough.
- (d) The Clear lead from the silicon diode corresponding to $I +$ is soldered to the connection C of the 10-pin electrical feedthrough.

The heater has two leads coming out of it. One of the leads is soldered to connection A and the other one to connection B of the 10-pin electrical feedthrough.

The sensor leads of the silicon diode can also be a significant source error if they are not properly heat sinked. Therefore, the leads of the silicon diode are also wrapped around the cold finger as described previously in this section in order to minimize the error.

Figure 5.8 is the schematic of the back panel of the temperature controller. It has two Sensor Input Connector and Pinouts as shown. Each input connector has 6 slots as shown alongside which the letters $I +$, $V +$, $V -$, and $I -$ are marked as shown in Figure 5.8. Any one of the Sensor Input Connectors could be connected to the silicon diode sensor. A 10-slot adapter (AEI 851-06EC12-10S50; Souriau Connection Technology) and a 6-pin DIN 45322 socket are used to connect the temperature controller to the heater and the silicon diode sensor via the electrical feedthrough. Figure 5.8 shows the wiring diagram between the temperature controller and the 10-slot adapter. The 6-pin DIN 45322 socket mates with the Sensor Input Connector and the following connections are soldered to the 10-slot adapter:

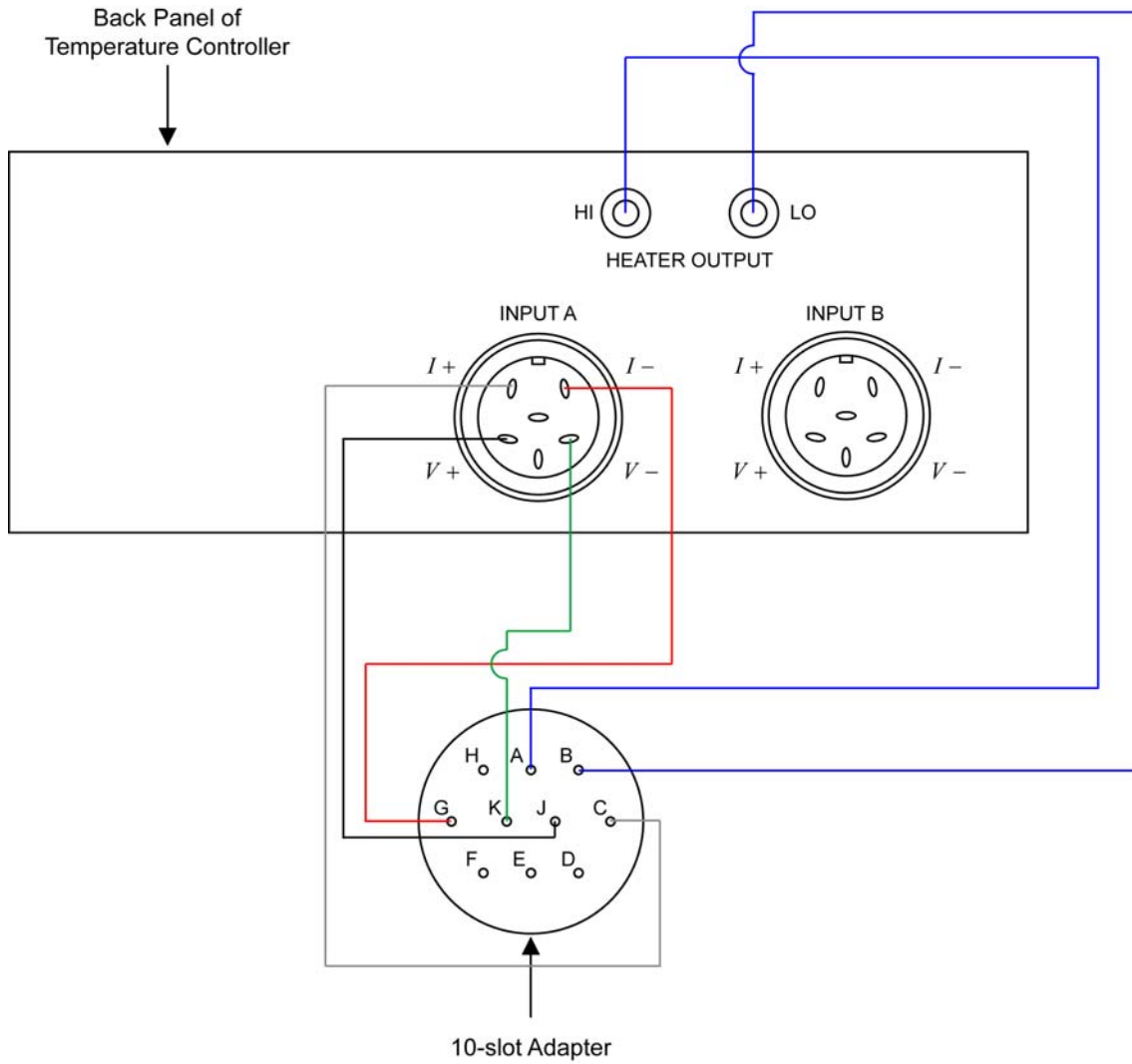


Figure 5.8 Wiring diagram between the temperature controller and the 10-slot adapter.

- (a) $I +$ from the Sensor Input Connector is soldered to connector C of the 10-slot adapter.
- (b) $V +$ from the Sensor Input Connector is soldered to connector J of the 10-slot adapter.
- (c) $I -$ from the Sensor Input Connector is soldered to connector G of the 10-slot adapter.
- (d) $V -$ from the Sensor Input Connector is soldered to connector K of the 10-slot adapter.

Using a separate set of wires, the heater output HIGH is soldered to connector A of the 10-slot adapter and the heater output LO is soldered to connector B of the 10-slot adapter.

Figure 5.9 is the overall schematic of all the components used in the low temperature electrical characterization of single-electron devices. The entire cryostat is placed on top of an electrically isolated vibration isolation table housed in an acoustic box. The vibration isolation table eliminates noise due to floor and support structure vibration. The triaxial cables connect the parameter analyzer to the single-electron device via one of the 10-pin electrical feedthroughs. Since the guard and the shield lines of the triaxial cable come only to ~ 5 mm of the cryostat, the device has a floating ground during the measurement. The heater and the silicon diode sensor inside the cryostat are connected to the temperature controller via the other 10-pin feedthrough.

The noise in the set-up is checked in a manner similar to the one described for the room-temperature measurement. Ground loops are a prominent source of noise in the low temperature measurement set-up and are caused by the presence of two grounds in the circuit. The best way to check for them is by looking over the circuit and ensuring that the outer shield of the triaxial cables connecting the device to the parameter analyzer is separate from the cryo compressor's ground connection and support structure. Typically the noise level for the low temperature measurement set-up is ~ 0.5 pA.

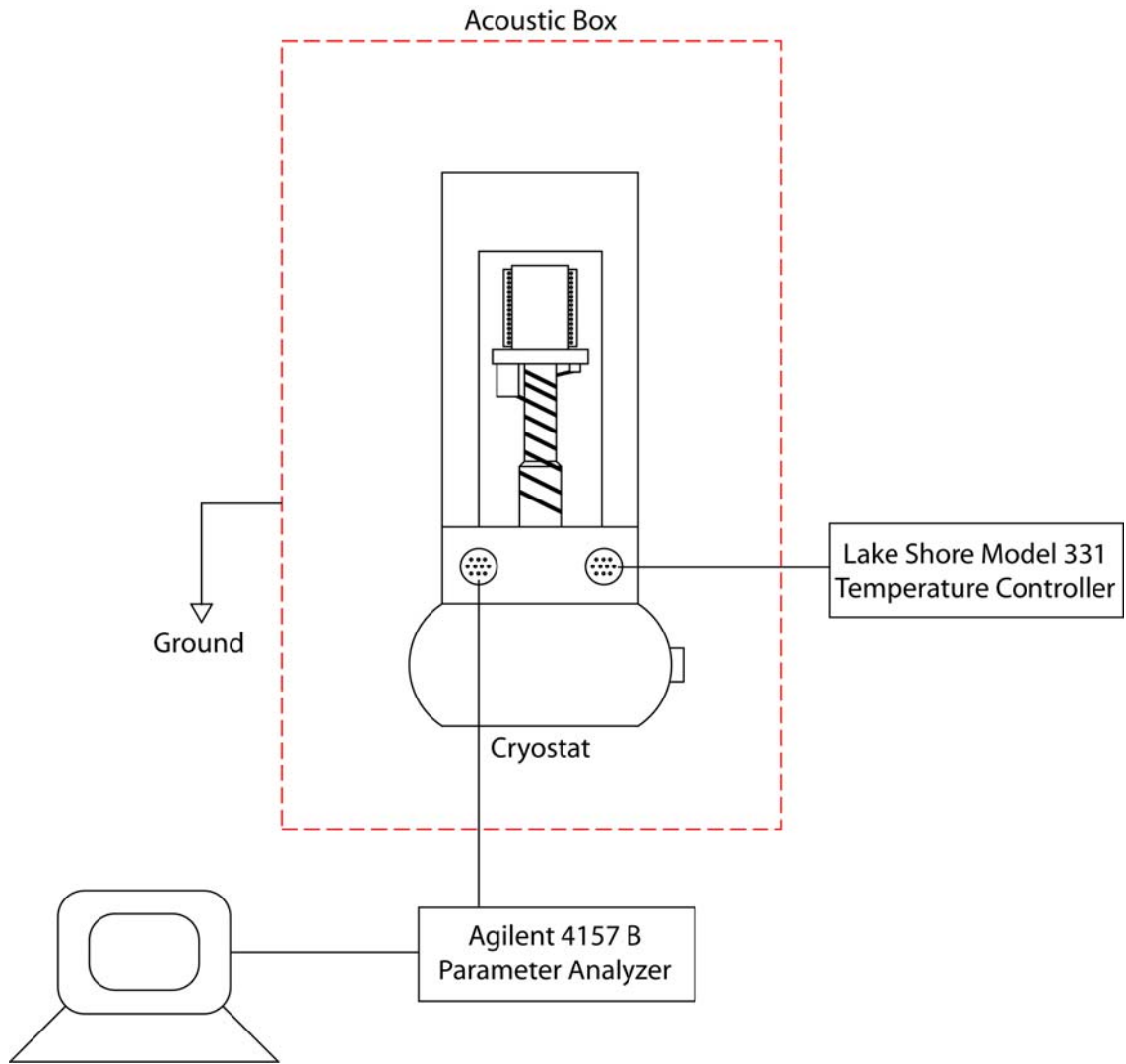


Figure 5.9 Schematic diagram of the overall set-up for the electrical characterization of single-electron device at low temperatures.

Electrostatic discharge (ESD) is the major cause of device failure during the low temperature measurement and it happens during mounting the sample onto the cryostat. To avoid device failure due to ESD, the following procedure should be followed: The user should first wear an anti-static wrist strap and connect its free end to an earth ground. The parameter analyzer is turned on and allowed to warm up for 30 minutes. At this point, none of the wires between the parameter analyzer and the cryostat/device or between the temperature controller and the cryostat are connected. A multistrand copper wire is taken and one of its free ends is connected to the same earth ground as the wrist strap. With the other end, all the legs of the chip carrier socket on the cryostat are touched to remove static electricity as shown in Figure 5.10 (a).

The chip carrier is now inserted into the socket as shown in Figure 5.10 (b). The legs of the socket are again touched with the grounded multistrand copper wire to remove static electricity. The radiation shield of the cryostat is then moved into place slowly taking care so that it does not touch the legs of the chip carrier during its descent. This is shown in Figure 5.10 (c). This is followed by placing the vacuum shroud into position (Figure 5.10 (d)). The chamber is then pumped down to ~ 50 mTorr using a mechanical pump. Once the pressure falls, the electrical lines from the compressor are connected to cryostat but the connections from the parameter analyzer and the temperature controller to the cryostat are not. The cooling water supply to the compressor is turned on and the water flow rate should be checked so that it is not below 1 gallon/minute. The compressor is then turned on. A temperature of ~ 10 K is reached in ~ 3 hours.

The compressor is then turned off and the electrical lines from it to the cryostat are disconnected. The triaxial cables from the parameter analyzer to the cryostat/device are connected next. The measurement can now be started using the sweep measurement mode as described previously.

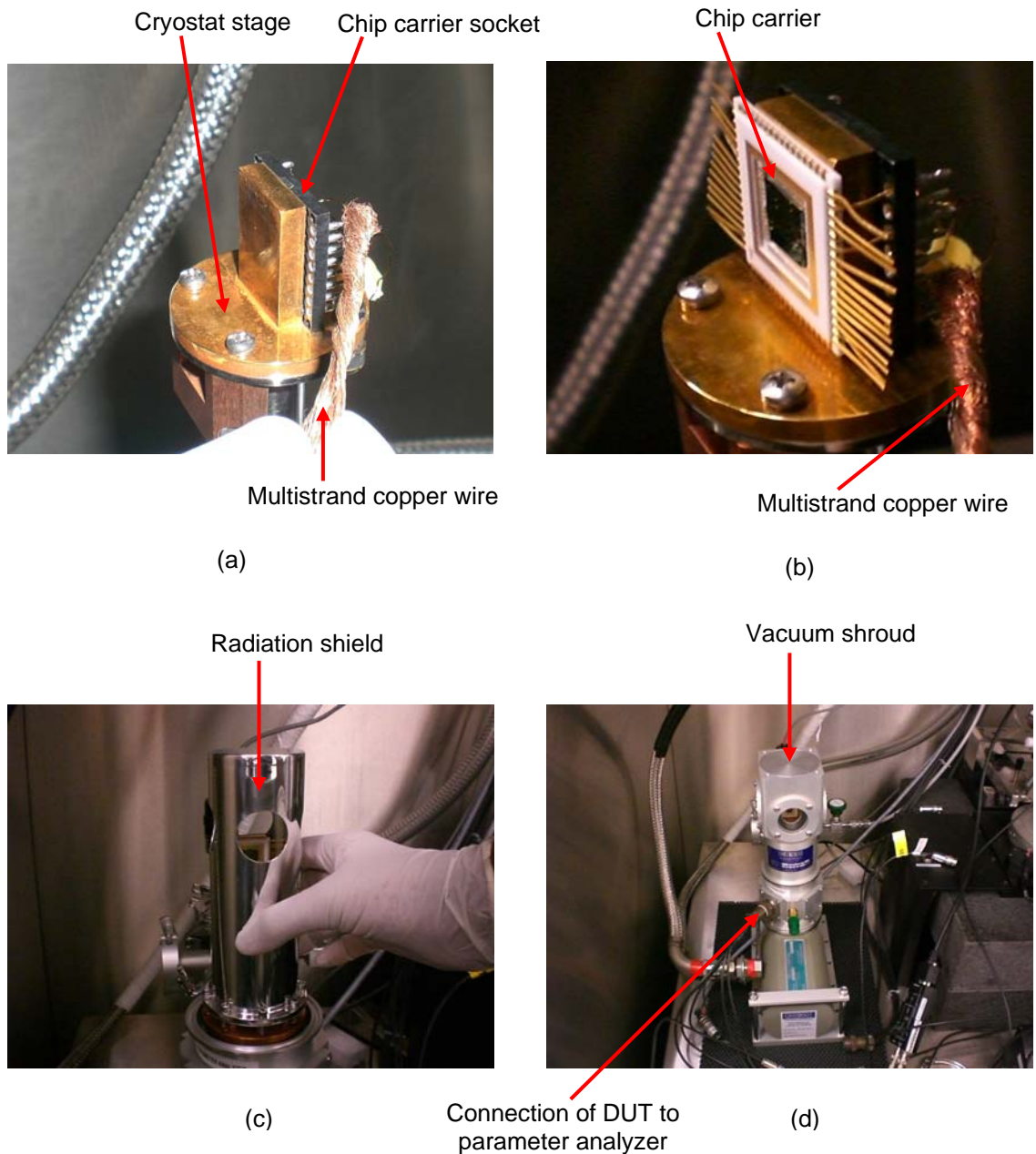


Figure 5.10 Mounting of the chip carrier on the cryostat stage. (a) Removal of static from the chip carrier socket which is attached to the cryostat stage. (b) Mounting of the chip carrier into the multi-pin chip carrier socket. (c) Lowering of the radiation shield into position. (d) Placing the vacuum shroud in position.

5.2 Coulomb staircase in a double junction single-electron device using 10 nm Au nanoparticles

A double junction single-electron device with 10 nm diameter Au nanoparticles as Coulomb islands was characterized at room-temperature using the Agilent 1455 C semiconductor parameter analyzer. The voltage was swept from -200 mV to 200 mV in increments of 4 mV using the sweep measurement mode and the device current recorded. Figure 5.11 shows the current-voltage characteristics of the device.

As can be seen from the I-V characteristics in Figure 5.11, the device exhibited clear Coulomb blockade and Coulomb staircase at room temperature which are decisive indications of single-electron transport in the device [5.2-5.4]. Each abrupt change in the device current at a given voltage is marked with arrows numbered 1 to 8 in the figure. Between the arrows 4 and 5 is the region of suppressed electrical conductance at low applied biases. This corresponds to the Coulomb blockade region of the double junction single-electron device.

In addition to the Coulomb blockade, the Coulomb staircase was also observed for this single-electron device. The observation of Coulomb staircase in the I-V characteristics of this device implies that the two tunnel junctions are highly asymmetric, that is, the rate of tunneling of an electron into the island is very different when compared to the rate of tunneling on an electron out of it.

To get a better picture of the periodicity of the changes in the current of the device, the voltage at which a sharp change in the current occurred was tabulated in Table 5.1. From Table 5.1, it can be seen that the average step width (the average distance between the adjacent arrow positions) is very periodic with a periodicity ΔV_{DS} of 46 ± 3 mV which suggests that only a single 10 nm Au nanoparticle takes part in the single-electron transport in the device [5.5, 5.6]. The average voltage interval ΔV_{DS} for this device is ~ 46 meV and is about two times greater than the room temperature thermal energy of 25 meV permitting the observation of single-electron phenomena at room temperature.

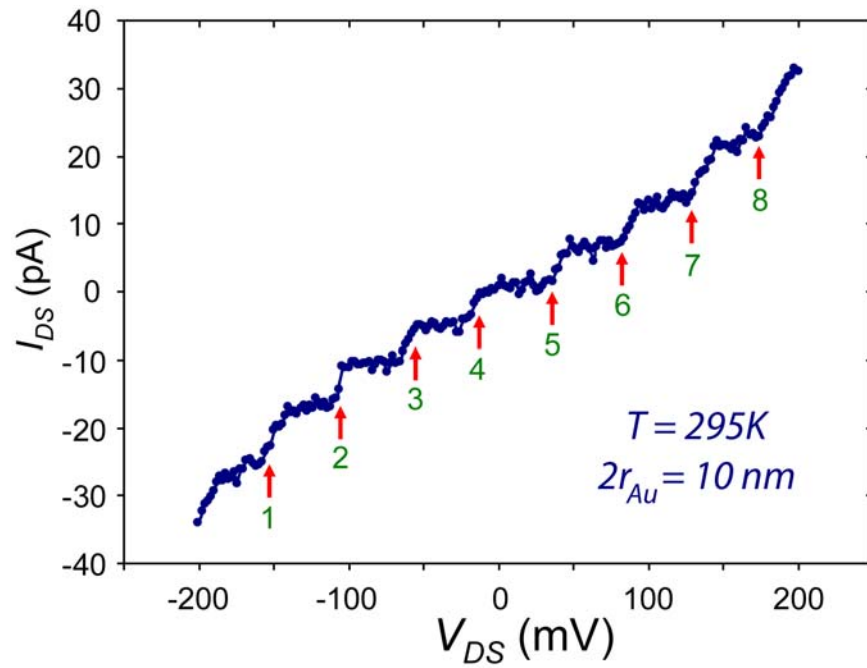


Figure 5.11 Plot of the I-V characteristics of a double junction single-electron device using 10 nm diameter Au nanoparticles as the Coulomb islands. The current-voltage characteristics of the device show a clear Coulomb blockade and Coulomb staircase at room-temperature. Each arrow in the plot indicates source-drain voltage at which there is a sharp change in the current of the device.

Table 5.1 Voltage data points corresponding to arrow positions from Figure 5.11

Arrow Index (A_i)	Voltage corresponding to A_i (V_i) mV	Abs ($V_i - V_{i-1}$) mV
1	-150	—
2	-104	46
3	-54	50
4	-12	42
5	36	48
6	82	46
7	130	48
8	174	44

Also, the step periodicity ΔV_{DS} of the Coulomb staircase is inversely proportional to the larger of the capacitances C_S and C_D of the tunnel junctions and is given by:

$$\Delta V_{DS} = \frac{e}{\max(C_S, C_D)} \quad (5.1)$$

This gives $\max(C_S, C_D)$ as 3.5 ± 0.2 aF which is a reasonable value considering that the self-capacitance C_{self} for a 10 nm Au nanoparticle ($r = 5$ nm) embedded in silicon oxide ($\epsilon_r = 4$) is 2.2 aF.

The self capacitance, C_{self} , of a spherical particle is given by:

$$C_{self} = 4\pi\epsilon_0\epsilon_r r \quad (5.2)$$

where ϵ_0 , ϵ_r and r are vacuum permittivity, dielectric constant of the surrounding medium, and particle radius, respectively. Figure 5.12 shows the high degree of periodicity of the Coulomb staircase from the data obtained from Table 5.1.

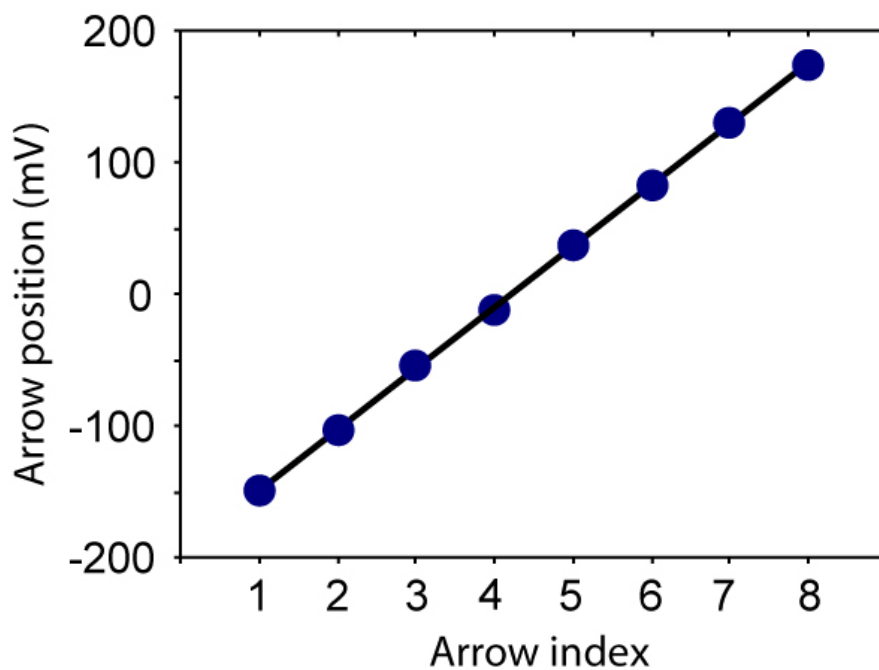


Figure 5.12 Plot of the voltage data points corresponding to the arrow positions at which a sharp change in current is observed for the single-electron device with 10 nm diameter Au nanoparticles as Coulomb islands. The values for the voltages are obtained from the I-V plot of the device shown in Figure 5.11 and tabulated in Table 5.1. The average step width ΔV_{DS} (the average distance between adjacent arrow positions) is 46 ± 3 mV. This highly periodic step size confirms that the single-electron tunneling is taking place only through a single nanoparticle that is positioned in the right tunneling range from the source and the drain electrodes.

5.3 Coulomb staircase in a double junction single-electron device using 20 nm Au nanoparticles

The fact that the observed single-electron phenomena for the single-electron device using 10 nm Au nanoparticles originated from the nanoparticles and not from any contamination that might have been introduced during the fabrication process was verified in the following way. Another batch of single-electron devices was fabricated to be used in conjunction with 20 nm diameter Au nanoparticles as the Coulomb islands. For this, a thicker layer of PECVD oxide (21 nm) was deposited to create a wider insulating gap between the source and drain electrodes. The completed devices were characterized using the Agilent 4157 B semiconductor parameter analyzer at a temperature of 10 K.

Figure 5.13 shows the current-voltage characteristics of a single-electron device with 20 nm Au nanoparticles as the Coulomb islands. For this device, the voltage was swept from -100 mV to 100 mV in increments of 2 mV. Similar to the single-electron device described previously in section 5.3, this device too exhibited clear Coulomb blockade and Coulomb staircase which verified that single-electron transport was taking place through the 20 nm diameter Au nanoparticle in this device as well. Each voltage data point in Figure 5.13 where a sharp change in the current was observed and marked with arrows numbered 1 to 5. The table below lists the voltage data points corresponding to the arrow markers where the abrupt change in the current for the device occurs.

Table 5.2 Voltage data points corresponding to arrow positions from Figure 5.13

Arrow Index (A_i)	Voltage corresponding to A_i (V_i) mV	Abs ($V_i - V_{i-1}$) mV
1	-30	—
2	-10	20
3	8	18
4	30	22
5	50	20

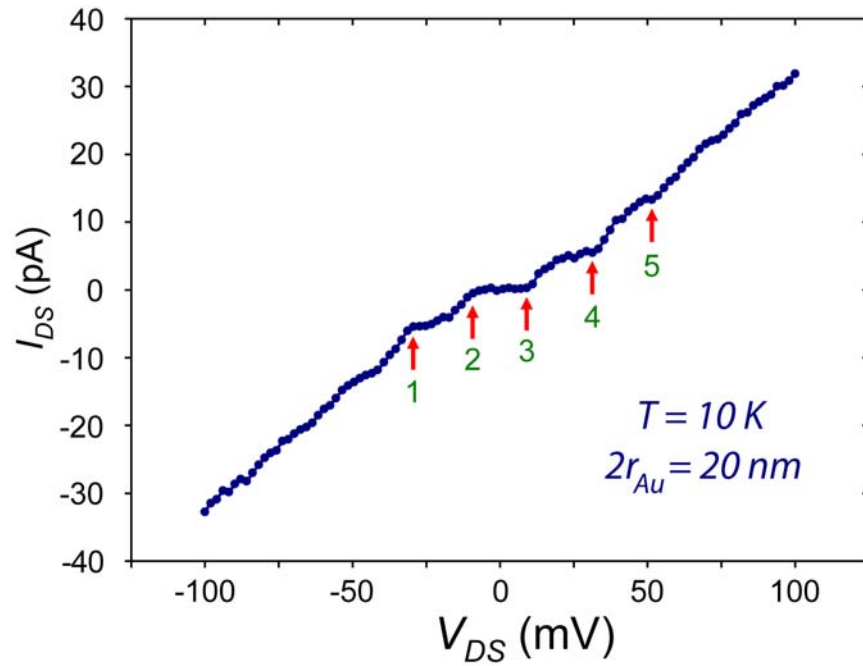


Figure 5.13 Plot of the I-V characteristics of a double junction single-electron device using 20 nm diameter Au nanoparticles as the Coulomb islands. The current-voltage characteristics of the device show a clear Coulomb blockade and Coulomb staircase at a temperature of 10 K. Each arrow marker in the plot indicates the source-drain voltage at which there is a sharp change in the current of the device.

For this device, over a voltage range of 200 mV, the steps of the Coulomb staircase were very periodic with a periodicity of 20 ± 2 mV as measured from the distance between neighboring arrows markers from Figure 5.13 which are listed in Table 5.2. Figure 5.14 shows the high degree of periodicity for the steps of the Coulomb staircase in this single-electron device.

It is known that the width of the Coulomb blockade and Coulomb staircase depends on the size of the Coulomb island. This is exactly what was observed when the I-Vs from the single-electron devices with 10 nm and 20 nm Au nanoparticles were compared. For the device with 20 nm Au nanoparticles, the average step width of the Coulomb staircase was found to be 20 ± 2 mV which is about half of the width of the single-electron device processed with 10 nm Au nanoparticles as the Coulomb islands, 46 ± 3 mV. From equation (5.1), $\max(C_S, C_D)$ for the device processed with 20 nm Au nanoparticle is 8.0 ± 0.7 aF. This value is about twice that of the device with 10 nm Au nanoparticles, 3.5 ± 0.2 aF. These values are in close proximity considering that the proportionality of the self-capacitance with particles of different diameters are given by equation (5.2). This dependence of the width of the step periodicity of the Coulomb staircase with differing sizes of Coulomb islands proves the single-electron behavior of the devices originated from a single Au nanoparticle positioned between the source and the drain electrodes.

Simulation of the I-V data for the single-electron device with 20 nm Au nanoparticles was also done. The equations governing the current in a single-electron device as a function of the applied voltage between the electrodes were described previously in Chapter 2. Figure 5.15 shows the simulated I-V for this device (red line) in comparison with the measured I-V data (blue dots). The simulation parameters were $C_D = 7.30$ aF, $C_S = 0.88$ aF, $R_D = 2.05$ G Ω , and $R_S = 0.40$ G Ω . A background charge of $Q_0 = 0.05e$ had to be incorporated in the simulation parameters. As can be seen from Figure 5.15, the simulated data and the experimental data are in excellent agreement.

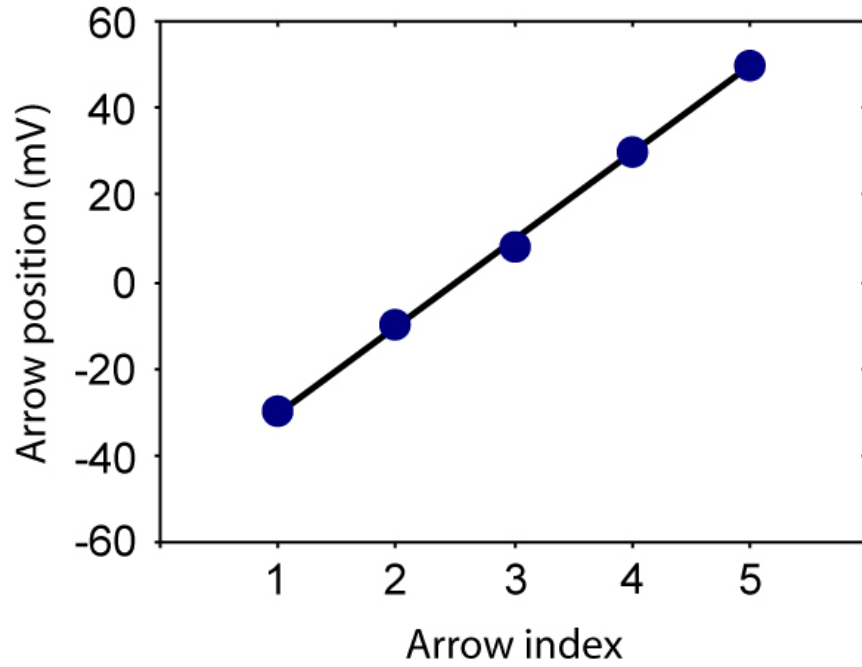


Figure 5.14 Plot of the voltage data points corresponding to the arrow positions at which a sharp change in current is observed for the single-electron device with 20 nm diameter Au nanoparticles as Coulomb islands. The values for the voltages are obtained from the I-V plot of the device shown in Figure 5.13 and tabulated in Table 5.2. The average step width ΔV_{DS} (the average distance between adjacent arrow positions) is 20 ± 2 mV. This highly periodic step size confirms that the single-electron tunneling is taking place only through a single nanoparticle that is positioned in the right tunneling range from the source and the drain electrodes.

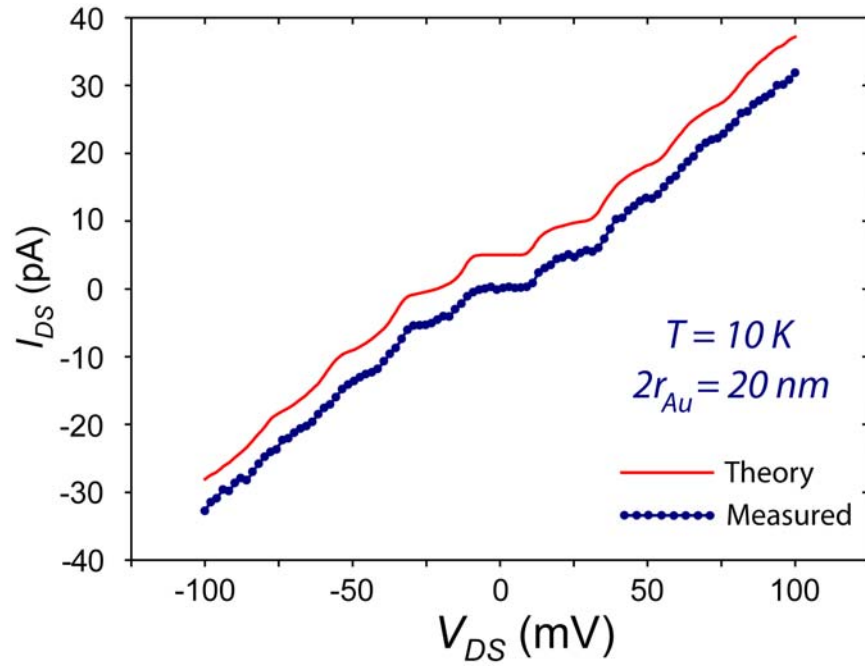


Figure 5.15 Comparison between the measured I-V characteristics (blue dots) and simulated I-V characteristics based on the orthodox theory (red line) of the double junction single-electron device using 20 nm diameter Au nanoparticles as Coulomb islands. The simulation parameters were $C_D = 7.30$ aF, $C_S = 0.88$ aF, $R_D = 2.05$ G Ω , and $R_S = 0.40$ G Ω , and background charge of $Q_0 = 0.05e$. The simulated I-V data is offset vertically by 5 pA for clarity.

5.4 Coulomb blockade in a double junction single-electron device using 10 nm Au nanoparticles

If the Coulomb island is positioned between the source and the drain electrodes such that the tunneling junctions are asymmetrical (i.e., $C_S R_S \gg C_D R_D$ or $C_D R_D \gg C_S R_S$), then Coulomb staircase will be observed in the single-electron devices in addition to Coulomb blockade [5.2, 5.4, 5.7]. Since our nanoparticles are positioned randomly in between the electrodes, the formation of an asymmetric tunneling junction is favored. However, symmetric junctions can be formed ($R_D C_D \approx R_S C_S$) if the nanoparticle is positioned in between the two electrodes such that it is at the same tunneling distance from both the electrodes. In this case only a clear Coulomb blockade will be present without a Coulomb staircase. Symmetrical tunneling junctions imply that the number of electrons jumping into the Coulomb island per unit time is identical or almost identical to the number of electrons jumping out of the Coulomb island per unit time. This is manifested in the current-voltage characteristics of the device where a linear increase in the device current with increasing applied source-drain voltage will be observed beyond the region of Coulomb blockade.

Figure 5.16 is the measured I-V characteristics of one such device measured at various temperatures starting from 10 K to 315 K. As can be seen from the plot, the Coulomb blockade is most pronounced at the lowest temperature and smears out gradually with increasing temperature. This happens because as the device temperature is raised, some electrons are thermally activated so that they have enough energy to tunnel through the barrier.

I-V for this device was also simulated based on the orthodox theory. Figure 5.17 shows the simulated I-V for this device (red line) in comparison with the measured I-V data obtained at a temperature of 10 K (blue dots). The simulation parameters were $C_D = 3.5$ aF, $C_S = 3.4$ aF, $R_D = 1.8$ G Ω , and $R_S = 2.1$ G Ω . A background charge of $Q_0 = 0.07e$ had to be incorporated in the simulation parameters. It can be seen from Figure 5.17 that the simulated and measured current-voltage characteristics for the device are an almost identical match.

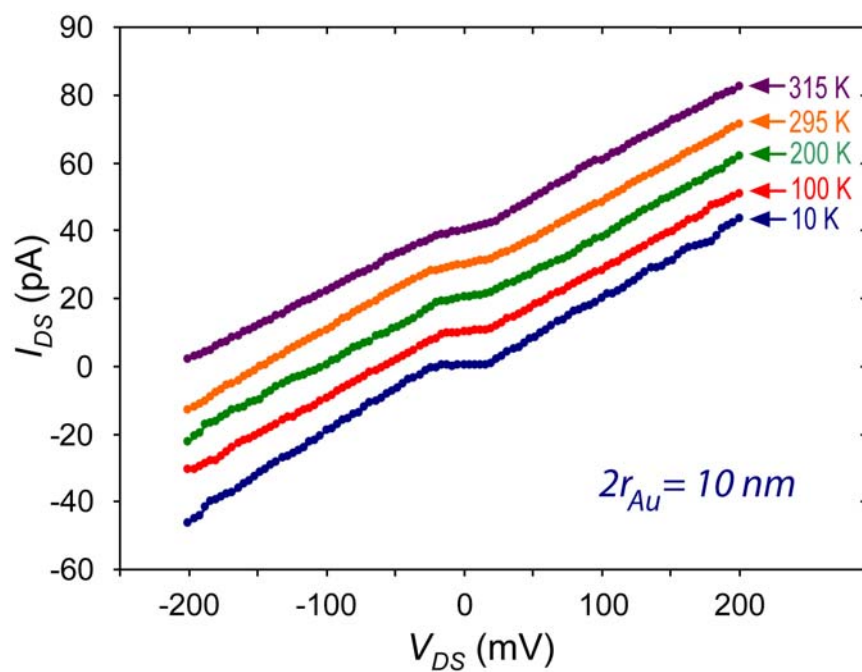


Figure 5.16 Plot of I-V characteristics of a double junction single-electron device using 10 nm diameter Au nanoparticles as Coulomb islands that has symmetrical tunneling junctions, measured at five different temperatures. Since the tunnel junctions are symmetrical, only a clear Coulomb blockade without the evidence of Coulomb staircase is observed. With increasing temperature, the blockade region gradually smears out due to thermally activated tunneling of electrons. Some remnant blockade can still be observed at 315 K.

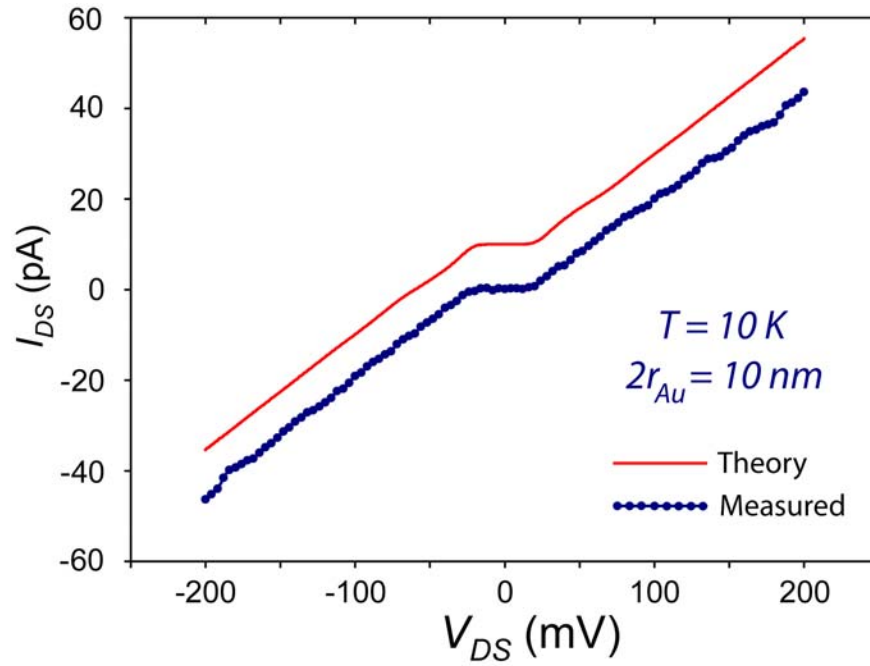


Figure 5.17 Comparison between the measured I-V characteristics (blue dots) and simulated I-V characteristics based on the orthodox theory (red line) of the double junction single-electron device using 10 nm diameter Au nanoparticles as Coulomb islands. The simulation parameters were $C_D = 3.5$ aF, $C_S = 3.4$ aF, $R_D = 1.8$ G Ω , and $R_S = 2.1$ G Ω , and background charge of $Q_0 = 0.07e$. The simulated I-V data is offset vertically by 10 pA for clarity.

5.5 Coulomb blockade/staircase statistics for double junction single-electron devices with 10 nm Au nanoparticles

To get a statistical overview of the exhibition of Coulomb blockade/staircase for single-electron devices, the Coulomb blockade/staircase data from eight different devices were considered. Each of these eight devices used 10 nm diameter Au nanoparticles as Coulomb islands. Since the step width of a single-electron device solely depends on the charging energy of the island, which in turn depends upon the size of the island, the average widths of the Coulomb blockade/ staircase from these devices were compared.

Figure 5.18 shows the average width ΔV_{DS} of the Coulomb blockade/staircase for all eight single-electron devices. Overall, the devices had an average Coulomb blockade/staircase width of 42.2 ± 12.7 mV. As can be seen from the plot, all except device 2 had an average Coulomb blockade/staircase step width of ~ 50 mV. Since the deviation in the size of the Au nanoparticles during synthesis is about 10% [5.8], such variations in the Coulomb blockade/staircase widths can be expected. The variations in the widths of the Coulomb blockade/staircase can also be attributed the presence of background charge (Q_0) in the device during measurements. These background charges usually get trapped during the device fabrication stage and are very difficult to eliminate. Since all of the devices, except for device number 2, show similar widths of Coulomb blockade/staircase, it can safely be concluded that the observed single-electron phenomena in the tested devices originate from the 10 nm Au nanoparticles and not from any impurities or contamination that might have been introduced during the fabrication steps.

The reason as to why device 2 exhibits a much smaller Coulomb blockade/staircase width can be attributed to the fact that it is probably two nanoparticles that are joined together which in combination act as one nanoparticle whose size is much larger than 10 nm. Since the width of the Coulomb blockade/staircase step is inversely related to the size of the Coulomb island, it could explain the anomaly in characteristics of device 2.

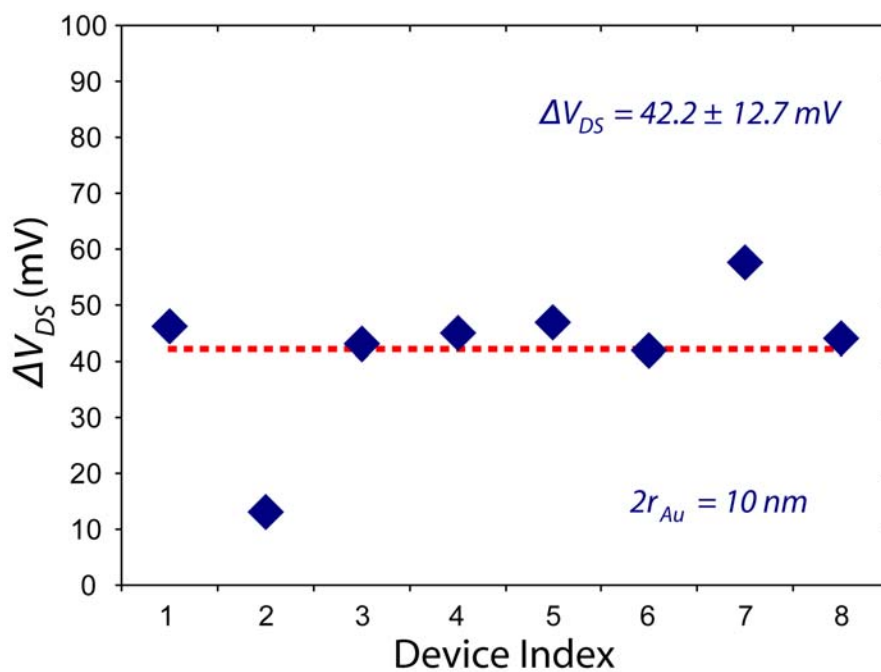


Figure 5.18 The step widths ΔV_{DS} of Coulomb blockade/staircase for eight different double junction single-electron devices. Each of the eight devices had 10 nm diameter Au nanoparticles as Coulomb islands. Overall, the eight devices had an average ΔV_{DS} of $42.2 \pm 12.7 \text{ mV}$. With the exception of device 2, all other devices had $\Delta V_{DS} \sim 50 \text{ mV}$.

5.6 Single-electron transistors using 10 nm Au nanoparticles

After successful demonstration of single-electron tunneling through metal nanoparticles with our proposed single-electron device structure, single-electron transistors were fabricated using all the steps outlined in Chapter 4. After wire bonding a device to the respective legs of the chip carrier the chip was mounted on the cryostat and the device cooled to a temperature of 10 K.

Once the device was cooled down to this temperature, current-voltage characteristics were measured using the Agilent 4157 B semiconductor parameter analyzer. With the source-drain bias kept constant at 10 mV, the gate bias was swept from -350 mV to 350 mV with increments of 7 mV.

Figure 5.19 shows the plot of the source-drain current I_{DS} as a function of the applied gate voltage V_G . From the curve it can be seen that the device exhibits clear Coulomb oscillation peaks which are very periodically spaced. These periodically spaced Coulomb oscillations peaks are a definitive indication of single-electron transistor characteristics. The spacing between successive peaks ΔV_G was measured to be ≈ 205 mV.

As was seen from the Coulomb blockade and Coulomb staircase data for double junction single-electron devices using 10 nm Au nanoparticles as Coulomb islands, the width of the Coulomb blockade is ~ 50 mV. The application of a source-drain bias of 10 mV initially and no gate bias means that the single-electron transistor will be under Coulomb blockade regime. Now, with the application of a positive gate bias, a stage is reached when a single electron can tunnel into the Coulomb island from the source electrode which is manifested as a spike in the source-drain current I_{DS} of the device known as a conductance peak. As the gate voltage is further increased, the island becomes stable with the extra electron and the device goes in to the Coulomb blockade regime again which is manifested as the valley between two successive Coulomb oscillation peaks.

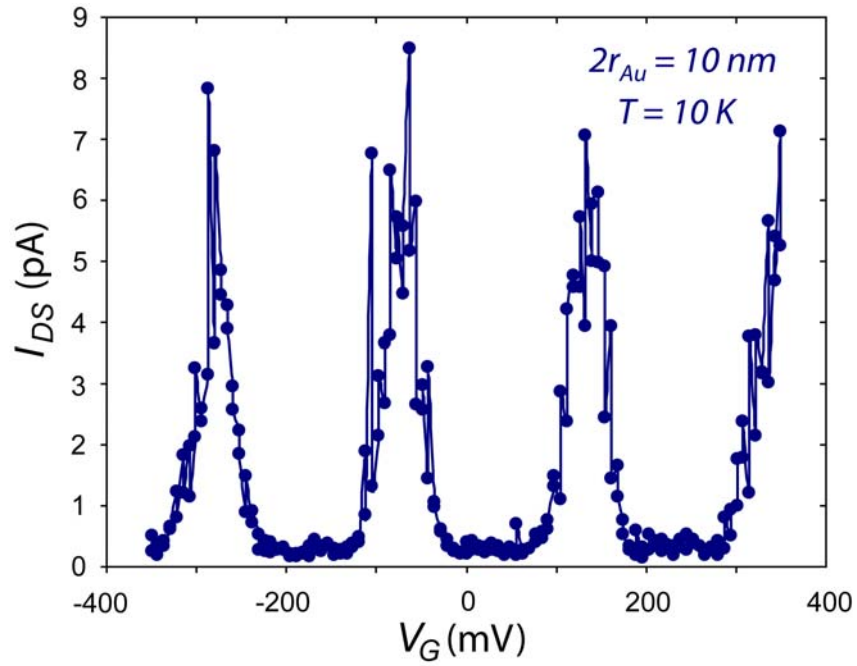


Figure 5.19 Demonstration of Coulomb oscillations in a single-electron transistor using 10 nm diameter Au nanoparticles as Coulomb islands at a temperature of 10 K. The source-drain bias was kept constant at 10 mV and the gate bias was swept from -350 mV to 350 mV. The average gap between two successive Coulomb oscillation peaks ΔV_G was ≈ 205 mV.

The current-voltage characteristics for this device were also measured at room temperature. As previously, the gate voltage was swept from -350 mV to 350 mV in steps of 7 mV keeping the source-drain bias fixed at 10 mV. Figure 5.20 shows the plot of the source-drain current of the device as a function of the applied gate bias. As can be seen from the plot, the Coulomb oscillation peaks were distinctly visible even at room-temperature. The average gap between two successive Coulomb oscillation peaks ΔV_G for the room temperature measurement was also ≈ 205 mV. It must be noted that the peaks have broadened and the baseline current has increased considerably as compared to the measurement done at 10 K. This is because at room temperature, electrons can be thermally excited to take part in tunneling which results in an earlier onset and a delayed end to the Coulomb oscillation peak. The higher value of the baseline current can also be attributed to thermally activated electron tunneling which results in the Coulomb blockade region being smeared out (instead of being absolutely flat) as described previously for the case of a double junction single-electron device in section 5.4.

For this single-electron transistor, the effect of a constant gate voltage on the source-drain current as a function of the source-drain voltage was also examined. With the device cooled to 10 K and in the absence of an applied gate bias, the source-drain voltage of the device was swept from -100 mV to 100 mV in increments of 2 mV. Next, the gate bias was fixed at 250 mV and the same source-drain voltage sweep for the device was carried out. Figure 5.21 shows the effect of the gate biasing on the source-drain current/voltage characteristics of the single-electron transistor. The blue dots are the measured I-V at $V_G = 0$ V and the red diamonds are the measured I-V at $V_G = 250$ mV, respectively. In both the cases, the device exhibits a clear Coulomb blockade and Coulomb staircases, but most importantly, a shift in the position of the Coulomb blockade due to gate biasing is clearly visible. Hence, at a certain value

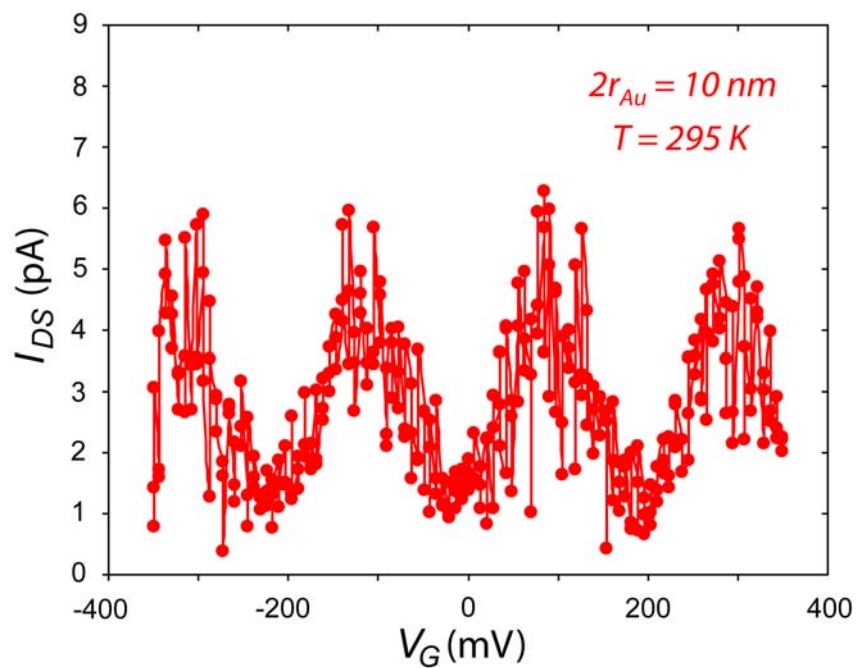


Figure 5.20 Demonstration of Coulomb oscillations in a single-electron transistor using 10 nm diameter Au nanoparticles as Coulomb islands at a temperature of 295 K. The source-drain bias was kept constant at 10 mV and the gate bias was swept from -350 mV to 350 mV. The average gap between two successive Coulomb oscillation peaks ΔV_G was ≈ 205 mV.

of source-drain bias, the device can either be conducting or show suppressed conductance for a specific gate voltage which is analogous to the operation of a transistor.

Simulations based on the orthodox theory were also done for the single-electron transistor. From the spacing between the Coulomb oscillation peaks, the gate capacitance C_G of the device was calculated to be $= \frac{e}{\Delta V_G} \sim 0.78$ aF. Figures 5.22 and 5.23 are the comparisons between the experimentally observed I-Vs and simulated I-Vs without and with the application of gate bias, respectively. As can be seen, the experimental results are in excellent agreement with the theory. The simulation parameters for Figure 5.22 ($V_G = 0$ V) were $C_D = 3.4$ aF, $C_S = 0.24$ aF, $C_G = 0.78$ aF, $R_D = 0.79$ G Ω , $R_S = 0.19$ G Ω , and $Q_0 = 0.05e$. The simulation parameters for Figure 5.23 ($V_G = 250$ mV) were $C_D = 3.4$ aF, $C_S = 0.24$ aF, $C_G = 0.78$ aF, $R_D = 0.79$ G Ω , $R_S = 0.19$ G Ω , and $Q_0 = 0.05e$.

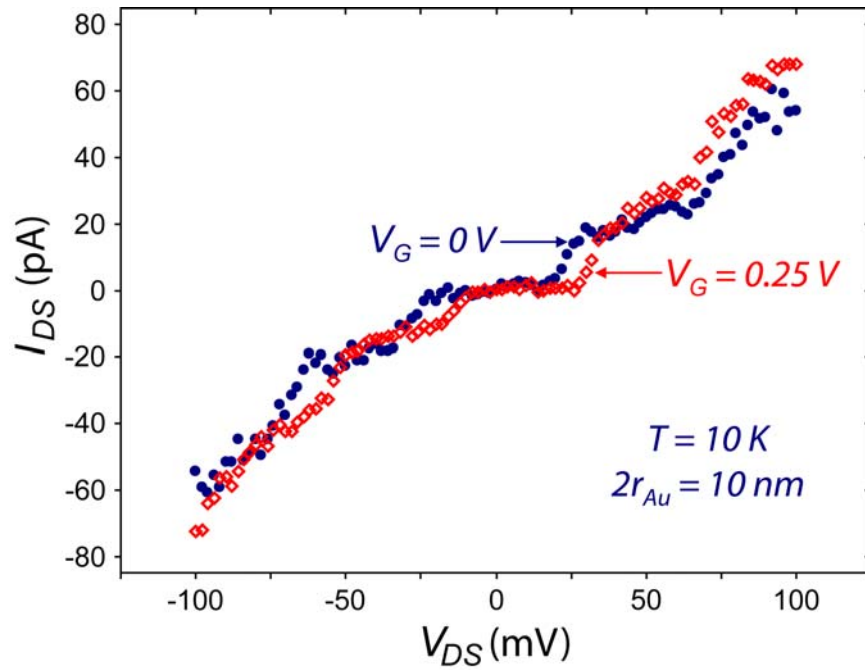


Figure 5.21 Coulomb blockade and Coulomb staircase characteristics of a single-electron transistor when the applied gate bias, $V_G = 0$ V (blue dots) and when $V_G = 250$ mV (red diamonds). The Coulomb island size for this device was 10 nm and the electrical characterization was done at 10 K. A shift in the Coulomb blockade/staircase of the device is clearly observed demonstrating the effect of gate biasing on single-electron transistors.

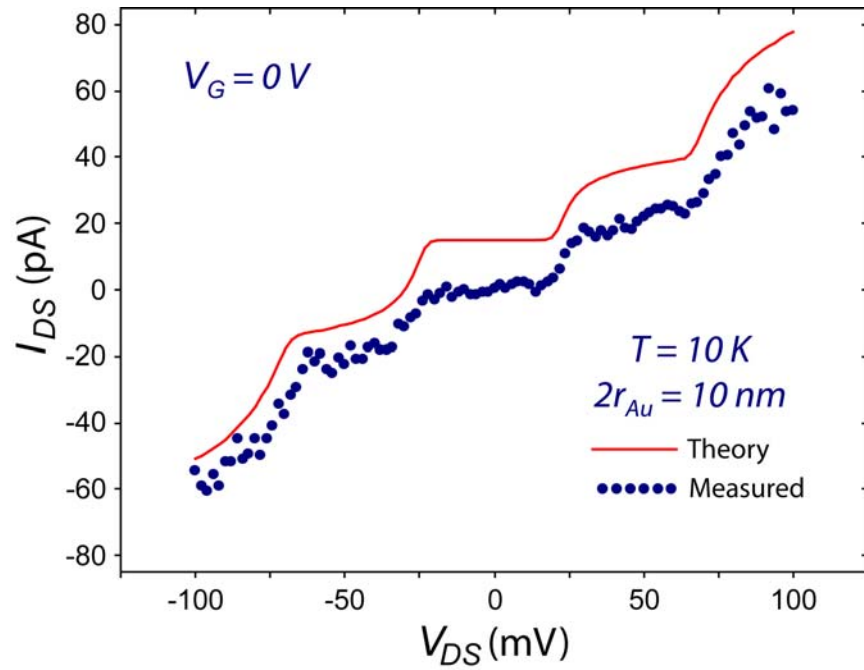


Figure 5.22 Comparison between the measured I-V with $V_G = 0\text{ V}$ in Figure 5.21 (blue dots) with the simulated I-V using the orthodox theory (red line). The simulation parameters are $C_D = 3.4\text{ aF}$, $C_S = 0.24\text{ aF}$, $C_G = 0.78\text{ aF}$, $R_D = 0.79\text{ G}\Omega$, $R_S = 0.19\text{ G}\Omega$, and $Q_0 = 0.05e$. The simulated curve is shifted by 15 pA vertically for clarity.

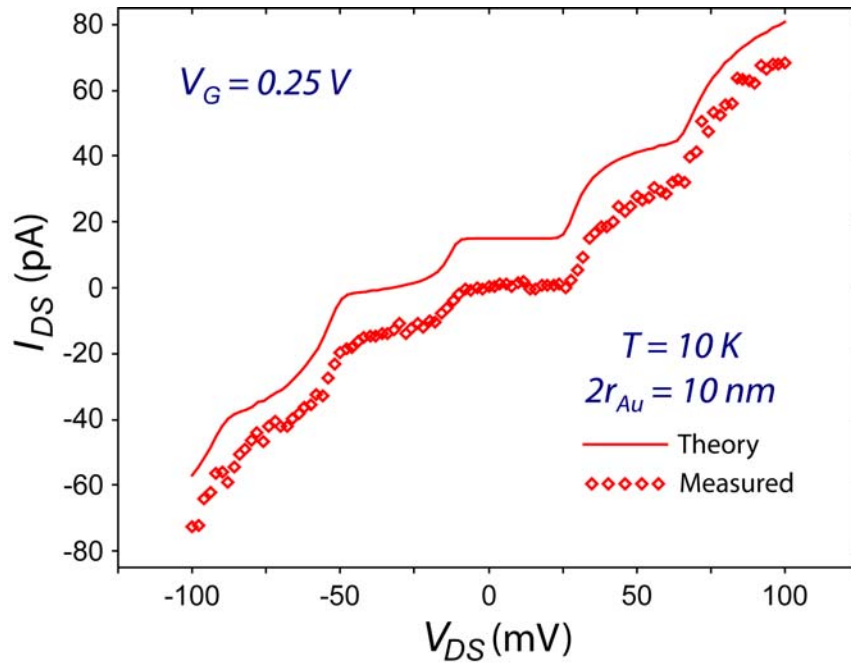


Figure 5.23 Comparison between the measured I-V with $V_G = 250$ mV in Figure 5.21 (red diamonds) with the simulated I-V using the orthodox theory (red line). The simulation parameters are $C_D = 3.4$ aF, $C_S = 0.24$ aF, $C_G = 0.78$ aF, $R_D = 0.79$ G Ω , $R_S = 0.19$ G Ω , and $Q_0 = 0.05e$. The simulated curve is shifted by 15 pA vertically for clarity.

5.7 Statistics of Coulomb oscillations in single-electron transistors

To get a statistical overview of the Coulomb oscillations in single-electron transistors, ten different devices each using 10 nm diameter Au nanoparticles as Coulomb islands were electrically characterized at room temperature using the Agilent 4155 C semiconductor parameter analyzer. The source-drain biases V_{DS} for these devices were kept at a constant value of 10 mV and the gate voltage V_G was swept from -350 mV to 350 mV. The source-drain current I_{DS} was recorded against V_G . The distance between the Coulomb oscillation peaks for each of the single-electron transistors was averaged and the results were plotted as shown in Figure 5.24. The measured interval between the Coulomb oscillation peaks for the ten devices had an average value ΔV_G of 183 mV (red line) with a standard deviation of ± 17 mV. The $\sim 10\%$ standard deviation in the average values of ΔV_G most probably arises from the difference in the size of the Au nanoparticles during their synthesis [5.8]. If the particle size is larger, then the average ΔV_G will decrease due to the decrease in the charging energy of the island and ΔV_G will increase with the decrease in the size of the Coulomb island.

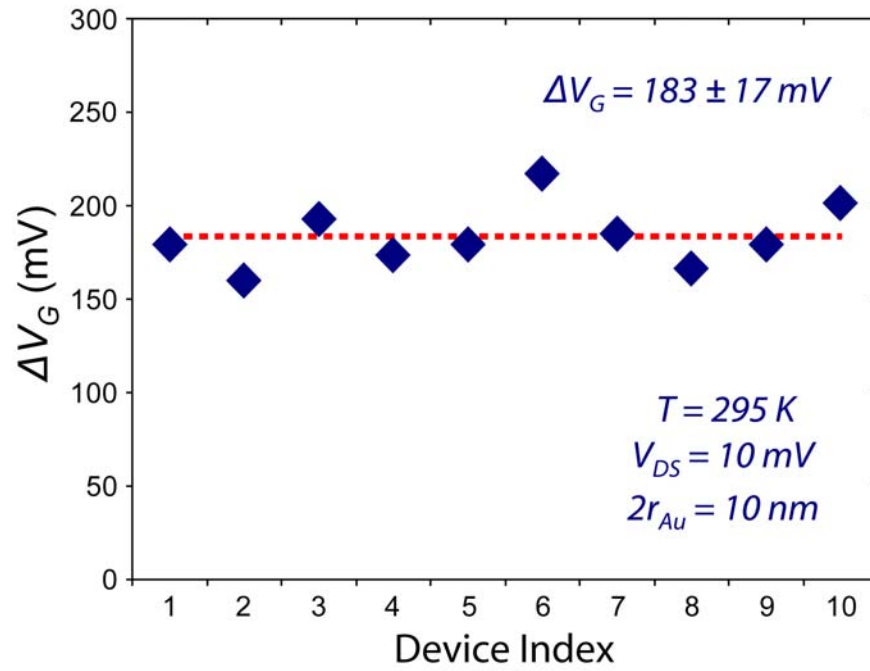


Figure 5.24 Average interval of Coulomb oscillation peaks ΔV_G for 10 different single-electron transistors measured at room temperature. All the 10 devices used 10 nm diameter Au nanoparticles as Coulomb islands. The red broken line is the average ΔV_G of 183 mV.

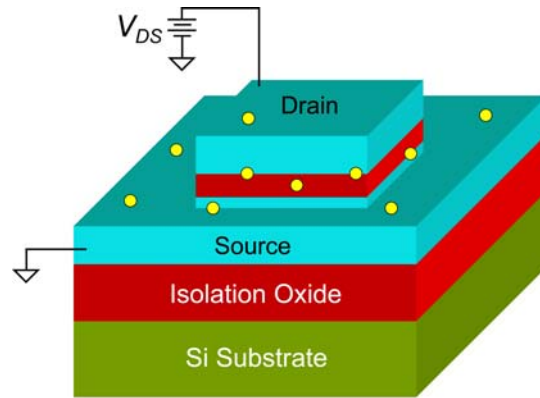
CHAPTER 6

ELECTROSTATIC FUNNELING FOR PRECISE NANOPARTICLE PLACEMENT

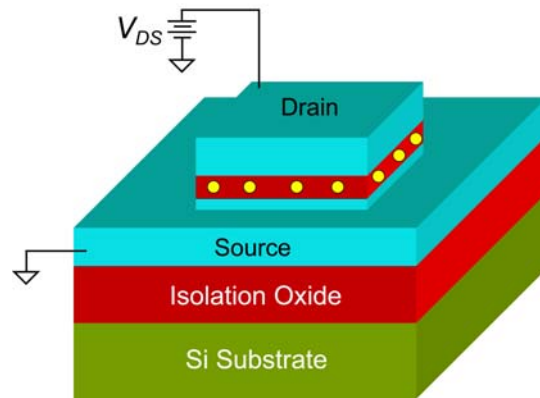
6.1 Introduction

In the preceding chapters the fabrication and the electrical characterization of single-electron devices were presented. A step in the fabrication of the devices involved the formation of self-assembled monolayers (SAMs) of APTES on the surfaces of the exposed side-wall of the PECVD oxide and the native oxide of chrome. The formation of this SAMs layer was necessary to provide an attractive force on the negatively charged Au nanoparticles in the colloidal solution with which they could be positioned in the gap between the source and the drain electrodes. While the use of only one kind of SAMs layer considerably simplifies the process of device fabrication, the attachment of the nanoparticles on the device is completely random. The formation of APTES SAMs on both SiO₂ and native oxide of chrome leads to the attraction of the nanoparticles from both surfaces as shown schematically in Figure 6.1 (a). This random attachment of nanoparticles on the device surface leads to most of the fabricated devices being open circuited. Statistically, more than 70% of the single-electron devices fabricated by using just one kind of SAMs had no nanoparticle positioned in the right tunneling range from the source and the drain electrodes resulting in no observation of Coulomb blockade, staircase, or oscillations in these devices. This non-ideal placement of the nanoparticles meant that the yield of the single-electron devices was close to 1%.

For practical applications of single-electron devices, a much higher device yield has to be attained. One method of achieving a larger yield could be to selectively attach the nanoparticles only on the exposed side-wall of the PECVD oxide and rather than randomly. This could be realized if the nanoparticles experienced a force of attraction from the exposed side-wall of the PECVD oxide only and repulsive forces from the rest of the areas. In other words, if



(a)



(b)

Figure 6.1 Schematic illustration of random and selective attachment of nanoparticles on a single-electron device. (a) The random attachment of nanoparticles on the exposed side-wall of the PECVD oxide of a single-electron device. The random attachment leads to low device yield. (b) Controlled positioning of nanoparticles on a single-electron device. This could be a method of achieving higher yields for single-electron devices with the new device structure.

the single-electron device structure could be functionalized with two different kinds of SAMs layers such that the SAMs on the exposed side-wall of the PECVD oxide provided only attractive force on the nanoparticles and the SAMs on the rest of the device area provided only forces of repulsion to the nanoparticles, then a selective placement of nanoparticles could be obtained as shown schematically in Figure 6.1 (b). With such controlled positioning of the nanoparticles, it could be ensured that most devices had more number of nanoparticles positioned between the electrodes in the current tunneling range thereby improving the yield.

In the characterization of single-electron transistors, it was seen that if each device unit had exactly one single nanoparticle, then the plot of the source-drain current I_{DS} as a function of the applied gate voltage V_G will show characteristic Coulomb oscillation peaks which are evenly spaced (please refer to Figures 5.19 and 5.20). If the number of nanoparticles in the device that contribute to single-electron transport is now two, then there will be two different sets of Coulomb oscillation peaks, each coming from a different particle. With several Coulomb islands attached to the device side-wall such that all of them are in the correct tunneling range between the electrodes, the I-V characteristics of the single-electron transistor would therefore comprise of as many sets of Coulomb oscillation peaks as the number of particles. If however, the Coulomb oscillations arising from each island are relatively in phase, then they would be superimposed on each other and an I_{DS} vs V_G characteristics as shown schematically in Figure 6.2 could be expected. In the figure, the Coulomb oscillation peaks arising from one nanoparticle is depicted in one kind of color. If the oscillation peaks from all the other particles are relatively closely spaced, then they could add up to give a broadened Coulomb oscillation peak (black line). The existence of several single-electron devices on a single piece of wafer could therefore open up the possibility of connecting them together to create integrated circuits.

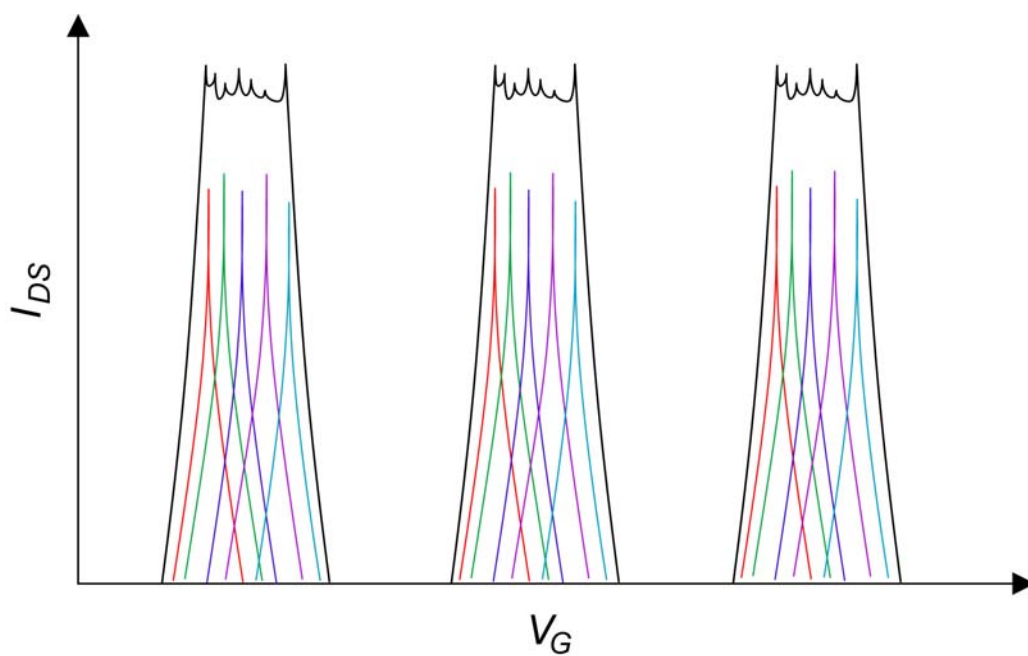


Figure 6.2 Schematic of the I_{DS} vs V_G characteristics of a single-electron transistor that has several nanoparticles exhibiting Coulomb oscillations simultaneously. If the oscillations arising from each nanoparticle are relatively in phase, then the I_{DS} vs V_G characteristic would be the superimposition of the oscillations from the individual nanoparticles.

6.2 Concept of Electrostatic Funneling

In the recent past, several approaches have been investigated to place nanoscale building blocks such as nanoparticles, nanowires, carbon nanotubes, DNA, proteins, etc. on specified substrate locations. These include the use of microfluids [6.1, 6.2], electric fields [6.3, 6.4], magnetic field [6.5], surface functionalization [6.6-6.10], capillary forces [6.11-6.13], biological templates [6.14-6.19], and scanning probe microscopy [6.20]. Although these methods and many others have had significant success in demonstrating precise positioning of nanostructures, large-scale placement using these methods has yet to be demonstrated.

In the earlier chapters, the fabrication of single-electron devices with the new device structure was shown to be a large-scale process. To improve device yield, the process of assembling nanoparticles on targeted substrate locations must meet three very important requirements:

- **Large-scale assembly:** The new scheme of assembling nanostructures must be scalable so that it can be applied to processes preferably over a wafer-scale. This will enable the fabrication of millions of devices which require precise positioning of nanocomponents to be done simultaneously (parallel processing).
- **Nanoscale precision in placement:** The placement precision of the nanostructures with this scheme must be such that it is at least comparable to the physical dimensions of the nanostructure being assembled.
- **CMOS compatibility:** Most electronic/optical devices and chemical/biological sensors made using nanostructures are fabricated over a CMOS based chip. The compatibility of the new scheme with CMOS based processes might ensure a practical method of fabricating integrated systems of nanoscale devices and sensors.

Figure 6.3 schematically demonstrates the concept of “Electrostatic Funneling”. In this, a substrate having alternating lines of two different materials are functionalized such that one material has a positive charge and the other material has a negative charge in an aqueous solution. When such a substrate is immersed in an aqueous solution containing negatively charged nanoparticles, the substrate and the nanoparticles interact in the liquid medium via double layer interaction [6.21]. The interaction energy between a negatively charged particle and the alternating lines of positively and negatively charged regions of the substrate will have a maxima and minima as illustrated in Figure 6.3 (a). When a nanoparticle is being attracted by the positively charged region of the substrate, it will start to move in the direction of the attractive forces. At the same time, it experiences a repulsive force from the negatively charged regions of the substrate. This concurrent attractive and repulsive force on the nanoparticle produces a gradient in the interaction energy in a direction parallel to the substrate (X direction in Figure 6.3). As a result of this the nanoparticle will experience a lateral force in addition to the vertical force of attraction which will push it towards the center of the positively charged region. Once a nanoparticle occupies a position on the substrate, it will repel other nanoparticles (since they are charged with the same polarity) such that the approach of other nanoparticles to the same substrate site is prohibited.

The forces of attraction and repulsion on a nanoparticle will also be a function of its separation from the substrate surface. This means that a nanoparticle nearer to the substrate surface will experience greater forces than a nanoparticle that is far away from it. Hence a virtual funnel is created near the substrate surface which only allows directed movement of the nanoparticles.

Another important aspect of electrostatic funneling is that it is possible to functionalize an entire wafer at the same time allowing large-scale placement of nanoparticles in parallel processing.

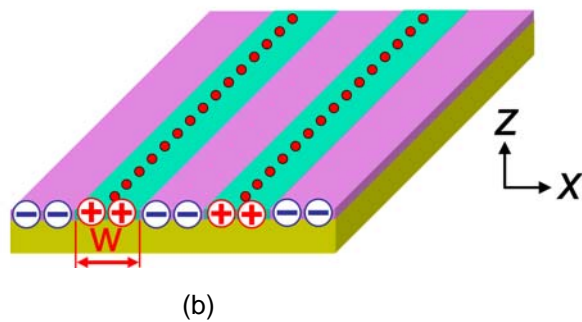
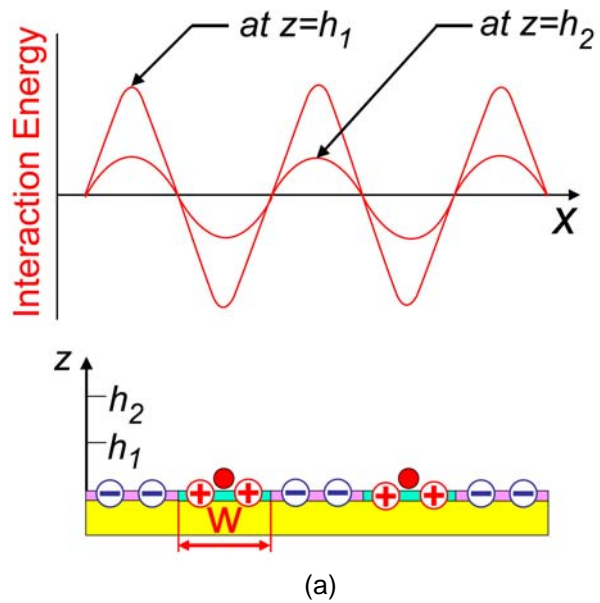


Figure 6.3 Schematic of the electrostatic funneling scheme for precise nanoparticle positioning. (a) A schematic of the electrostatic interaction energy in an aqueous solution for a negatively charged nanoparticle near a substrate functionalized with positively and negatively charged molecules. (b) The nanoparticles (red dots) are guided towards the centers of the positively charged regions of the substrate where the interaction energy is minimum.

6.3 Experimental procedures for electrostatic funneling

Figure 6.4 outlines the experimental procedures followed to demonstrate electrostatic funneling. A wafer comprising of alternating lines of copper and silicon oxide was used as the starting substrate. The copper and silicon oxide lines were defined using damascene technology [6.22] on a 200 mm silicon wafer. The widths of the copper and silicon oxide lines were 120 nm and 80 nm, and the height of the copper lines were ~ 5 nm lower than the silicon oxide lines as measured with an AFM. The wafer was cut into small pieces of size about 2 cm × 2 cm and rinsed in acetone followed by cleaning in a UV-O₃ chamber for 30 minutes to remove residual organic impurities. Immediately following this step, the wafer was immersed in a 1% citric acid solution in DI water for 15 minutes to remove any copper oxide from the surfaces of the copper lines. The wafer was then rinsed thoroughly in DI water and dried under a stream of compressed nitrogen. The copper regions of the wafer were then selectively electroless plated with gold of thickness ~ 15 nm (the reason for plating the copper surfaces only with gold will become obvious later). This was done by immersing the wafers into an electroless plating solution (Alfa Aesar; major components of the plating solution are KAu(CN)₂, NH₄OH, and water) maintained at 65 °C for 45 seconds followed by rinsing in pure ethanol (200 proof) and then with copious amounts of DI water. The plating resulted in the Au-coated copper lines now being ~ 10 nm higher than the silicon oxide lines as measured with AFM.

Positive and negative charges were imparted to the silicon oxide and gold regions, respectively, using self-assembled monolayers (SAMs) [6.23-6.24]. To obtain a positive charge exclusively on the surfaces of the silicon oxide regions, the wafer was immersed into a 1 mM solution of (3-aminopropyl)triethoxysilane (APTES, (C₂H₅O)₃-Si-(CH₂)₃-NH₂, 99%; Sigma-Aldrich) in chloroform for 30 minutes at room temperature followed by rinsing with 2-propanol and drying under a stream of nitrogen gas. This was followed by providing a negative charge only to the gold coated copper areas by immersing the wafer in a 5 mM solution of 16-mercaptohexadecanoic acid (MHA, HS-(CH₂)₁₅-COOH, 99%; ProChimia, Poland), in ethanol for

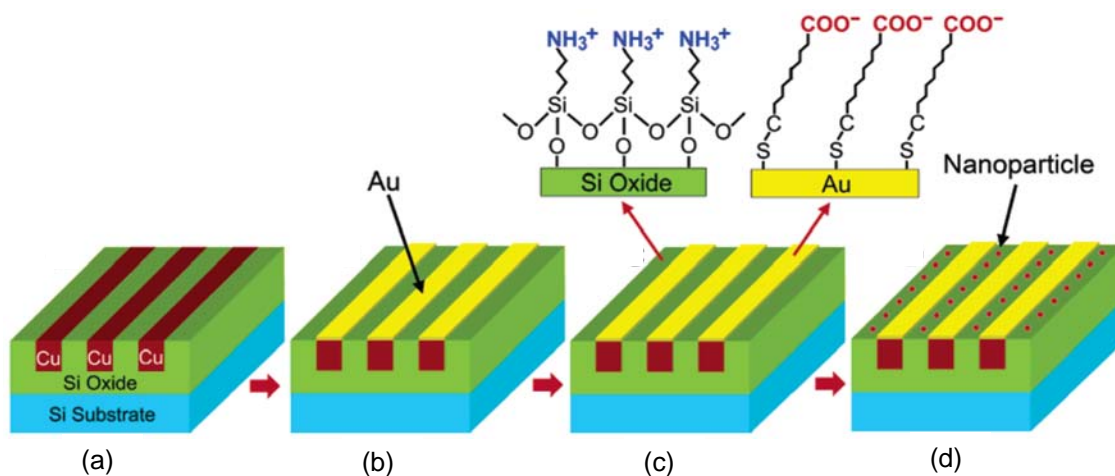


Figure 6.4 Experimental procedures followed to demonstrate electrostatic funneling. (a) Starting structure in which copper lines (brown) are embedded in silicon oxide dielectric (green) fabricated on a 200 mm wafer. (b) Electroless plating of the exposed copper lines with gold (c) Selective formation of self-assembled monolayers (SAMs) of APTES ($-\text{NH}_2$; $-\text{NH}_3^+$) on silicon oxide regions and MHA ($-\text{COOH}$; $-\text{COO}^-$) on gold regions, respectively. These SAMs provide the silicon oxide surfaces with a positive charge and the gold surfaces with a negative charge, respectively, in an aqueous medium. (d) Immersion of the wafer into a colloidal solution containing negatively charged Au nanoparticles.

3 hours at room temperature, followed by rinsing in a 1% solution of HCl in ethanol and drying under compressed nitrogen gas.

The wafer was then immersed into a colloidal solution of negatively charged gold nanoparticles of mean diameter ~ 20 nm (3.5×10^{11} particles/ml; Ted Pella Inc.) for 30 minutes at 4 °C. After removing the wafer from the gold colloid, the sample was rinsed with methanol and dried under nitrogen gas. The samples were then imaged under a field emission scanning electron microscope (FE-SEM).

6.4 Effectiveness of electrostatic funneling

Figure 6.5 is the representative FE-SEM image of the wafer after the attachment of Au nanoparticles from the previous step. As can be seen from the image, the electrostatic funneling method is a very effective in positioning several nanoparticles simultaneously along the centers of the silicon oxide lines.

To get a statistical idea as to how good this alignment was, the deviation of each nanoparticle from the centers of the silicon oxide line was measured. From all the 217 particles that are present in the image the standard deviation was found to be 6.2 nm which is about 3 times smaller than the size of the nanoparticle itself.

From the figure, it can also be seen that the nanoparticles are very regularly spaced with a mean separation of ~ 50 nm from the center of one particle to another. This is because the nanoparticles share the same charge polarity and are almost of the same physical dimensions (<10% variation) [6.25]. These facts combined create a similar effective repelling force between pairs of nanoparticles. It will be shown later in this chapter that the particle to particle separation matches very well with the theoretical calculations.

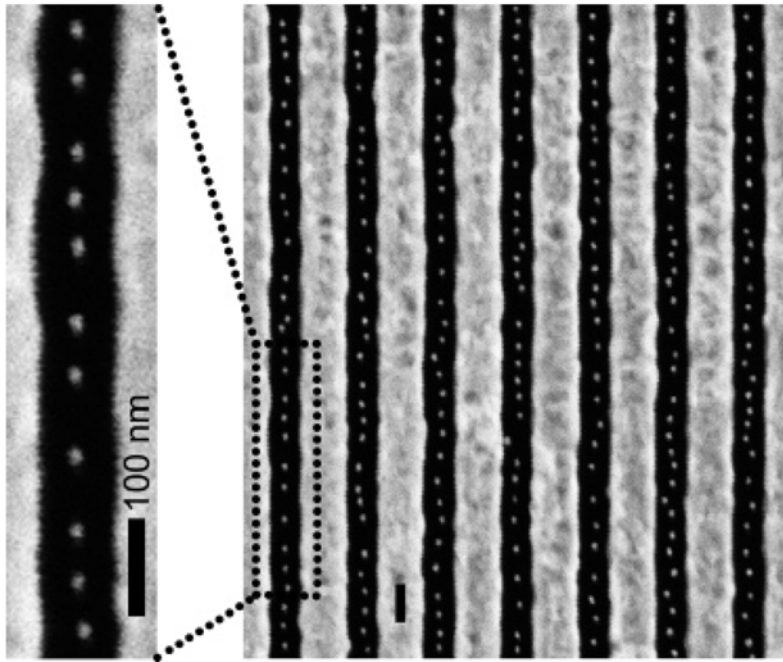


Figure 6.5 FE-SEM image showing the effectiveness of the electrostatic funneling method for precise positioning of nanoparticles. The 20 nm Au nanoparticles (bright dots) are placed along the centers of the silicon oxide lines (dark bands). The bright bands running parallel to and alternating the silicon oxide lines are gold lines. Scale bars = 100 nm.

The effectiveness of the electrostatic funneling scheme is not only applicable to the alternating lines of gold and silicon oxide as shown in Figure 6.5 but can be applied to a variety of geometries as long as the proper electrostatic funnel is created. Figure 6.6 shows the FE-SEM image in which the substrate pattern has been changed from a line to a dot of diameter ~ 100 nm. This pattern was formed using electron beam lithography on a silicon substrate, metal evaporation, and lift-off processes. After cleaning the samples, SAMs of APTES and MHA were formed on the silicon oxide and the gold surfaces, respectively, and the samples were immersed in a colloidal solution of 20 nm Au nanoparticles for 24 hours. Immediately afterwards, samples were rinsed in methanol and dried under nitrogen gas as before. From the FE-SEM image of the sample, it can be seen that almost all the circular patterns are occupied by exactly one nanoparticle. Once a nanoparticle occupies a site, it prohibits the approach of other nanoparticles due to the same polarity of their surface charges.

This method of precisely positioning nanoparticles can also be applied to a 3-dimensional step structures similar to the new single-electron device structure shown schematically in Figure 3.3. Figure 6.7 shows three such step structures comprising of a layer of silicon oxide (black band) which is sandwiched between two gold layers (bright areas). These structures were fabricated using a combination of optical lithography, metal evaporation, dielectric sputtering, and lift-off process. The thickness of the metal and dielectric layers is different in the three structures shown in the figure to create proper electrostatic funnels for different sizes of Au nanoparticles to be aligned. After cleaning the wafers, SAMs of APTES and MHA were formed on the silicon oxide and the gold surfaces, respectively. The samples were then immersed into Au colloids of diameters ~ 200 , ~ 80 , ~ 50 nm (all negatively charged in their colloidal solution; Ted Pella Inc) for 30, 20, and 10 minutes respectively. After sample rinsing and drying described previously, they were imaged under the SEM. The effectiveness of the guidance structure is clearly seen in this case too which results in the different sizes of Au nanoparticles all being aligned along the centers of the positively charged silicon oxide regions.

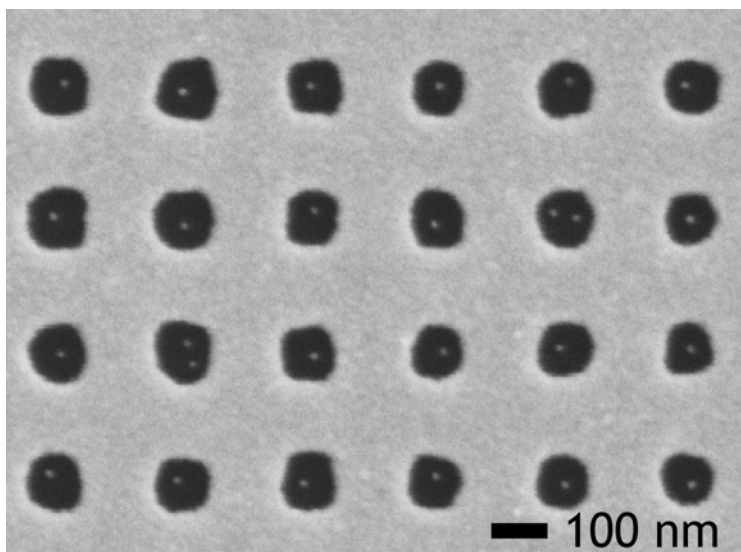


Figure 6.6 FE-SEM of a sample demonstrating the effectiveness of electrostatic funneling for single particle placement. The bright dots are ~20 nm Au nanoparticles and the dark circular patterns are silicon oxide surfaces functionalized with SAMs of APTES. The bright area is Au surface functionalized with SAMs of MHA. For most of the circular features, only one nanoparticle occupies a site.

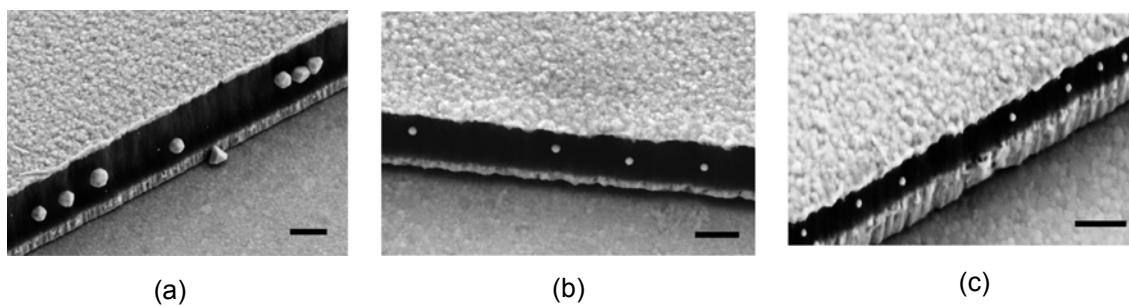


Figure 6.7 FE-SEM of samples in which the electrostatic funneling scheme was used to precisely align nanoparticles on a 3-dimensional step structure similar to the new single-electron device structure. (a) Alignment of ~ 200 nm Au nanoparticles. (b) Alignment of ~ 80 nm Au nanoparticles. (c) Alignment of ~ 50 nm Au nanoparticles. Scale bars = 400 nm.

6.5 Interaction between charged surfaces and nanoparticles in an aqueous medium

To get a more quantitative picture of the interaction between the nanoparticle and substrate, the interaction energies were calculated based on the DLVO theory [6.21, 6.26]. The interaction energies between an Au nanoparticle and an infinite surface functionalized with either APTES or MHA was first calculated. The total interaction energy, $V_j(z)$, is the sum of the double layer interaction energy, $\Phi_j(z)$ and the van der Waals interaction energy, $W_j(z)$, where j represents the surface type (functionalized with MHA or APTES) and z is the separation between the nanoparticle surface and the functionalized substrate.

$$V_{MHA}(z) = \Phi_{MHA}(z) + W_{MHA}(z)$$

and

$$V_{APTES}(z) = \Phi_{APTES}(z) + W_{APTES}(z) \quad (6.1)$$

6.5.1 The electric double layer

To understand the electric double layer interaction between charged surfaces in a liquid medium, the nature of events that take place when a charged surface is immersed in an aqueous medium must be understood. If a charged surface is immersed in a solution containing ions as show in Figure 6.8, then near the surface there is an accumulation of counterions (ions of the opposite charge to the surface charge) and a depletions of co-ions (ions of the same charge to the surface charge). The charge on the surface is balanced by the counterions which accumulate near the surface forming a region known as the *Stern* layer or *Helmholtz* layer [6.21]. Beyond this *Stern* or *Helmholtz* layer, the rest of the ions form an atmosphere around the charged surface known as the diffuse *electric double layer*. Since the double layer forms to neutralize the charged surface, it causes a rearrangement of ions near the charged surface which extends into the bulk liquid. The rearrangement of ions causes an electrokinetic potential difference to develop between the charged surface and any point in the mass of the electrolyte in which it is immersed. This voltage difference that is set up is known as the electrostatic

surface potential (ψ). The magnitude of the electrostatic surface potential is related to the surface charge density (σ) of the charged surface and the thickness of the double layer. As one moves away from the charged surface, the potential drops linearly in the Stern layer and then exponentially through the double layer. In order to calculate the strengths of the forces between charged surfaces, it is therefore essential to know the surface potentials of the charged surfaces in a given electrolyte. The surface potential is known to depend on the level of ions present in the electrolyte and can be calculated by solving the non-linear Poisson-Boltzmann equation [6.21]:

$$\nabla^2\psi(\vec{r}) = -\frac{e}{\epsilon_r\epsilon_0} \sum_i z_i\rho_{0i} \exp(-z_i e\psi(\vec{r})/kT) \quad (6.2)$$

where e is the unit charge of an electron, ϵ_r is the dielectric constant of water, ϵ_0 is the permittivity of free space, z_i is the valency of ion species i , ρ_{0i} is the ion concentration of ion species i in the bulk, k is the Boltzmann constant, and T is the absolute temperature.

There is no exact analytical solution to the non-linear Poisson-Boltzmann equation except for a planar geometry. However, numerical solutions [6.27] and approximate analytical expressions [6.28-6.31] to the non-linear Poisson-Boltzmann equation are available. Using these numerical solutions and approximations the interaction energies between charged surfaces and nanoparticles and between pairs of nanoparticles have been calculated.

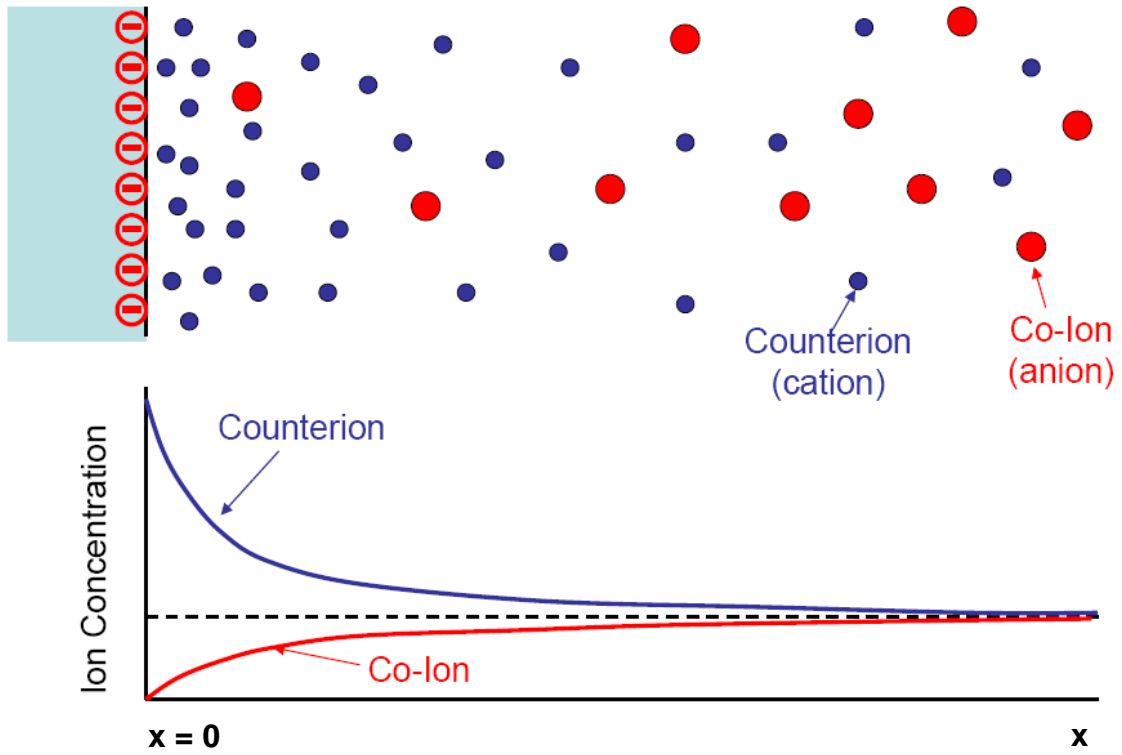


Figure 6.8 Schematic of the rearrangement of ions in an electrolyte when a charged surface is immersed into it. Near the charged surface there is an accumulation of counterions and a depletion of co-ions. The ion concentrations decrease exponentially as one moves from the surface in to the bulk solution.

6.5.2 Calculation of double layer interaction energies

The double layer interaction energies between a nanoparticle and a MHA functionalized substrate, $\Phi_{MHA}(z)$, and that between a nanoparticle and an APTES functionalized substrate, $\Phi_{APTES}(z)$, can be calculated using the linear superposition approximation [6.29, 6.32, 6.33] (LSA) and is given by:

$$\Phi_{MHA}(z) = 4\pi\varepsilon\varepsilon_0 a \left(\frac{kT}{e}\right)^2 Y_{Au} Y_{MHA} \exp(-\kappa z)$$

and

$$\Phi_{APTES}(z) = 4\pi\varepsilon\varepsilon_0 a \left(\frac{kT}{e}\right)^2 Y_{Au} Y_{APTES} \exp(-\kappa z) \quad (6.3)$$

where ε is the dielectric constant of water, ε_0 is the permittivity of free space, a is the radius of a Au nanoparticle, k is the Boltzmann constant, T is the absolute temperature, e is the electronic charge, and Y_{Au} , Y_{MHA} , and Y_{APTES} are the effective reduced surface potentials [6.27-6.29] of an isolated Au nanoparticle, an isolated MHA functionalized substrate and an isolated APTES functionalized substrate, respectively. κ is the inverse Debye length defined by [6.21, 6.34]

$$\kappa = \left[\left(\frac{1000e^2 N_A}{\varepsilon\varepsilon_0 kT} \right) \sum_i z_i^2 M_i \right]^{1/2} \quad (6.4)$$

where N_A is the Avogadro's number, z_i is the valency of the ion species i and M_i is the molar concentration of ion species i . The aqueous 20 nm gold colloid solution contains Na^+ , citrate ions ($\text{C}_6\text{O}_7\text{H}_7^-$, $\text{C}_6\text{O}_7\text{H}_6^{2-}$, $\text{C}_6\text{O}_7\text{H}_5^{3-}$), Cl^- , H_3O^+ , and OH^- ions. Their concentrations at a pH of 6.6 are $[\text{Na}^+] = 7.8 \times 10^{-6}$ M, $[\text{C}_6\text{O}_7\text{H}_7^-] = 1.5 \times 10^{-8}$ M, $[\text{C}_6\text{O}_7\text{H}_6^{2-}] = 1.0 \times 10^{-6}$ M, $[\text{C}_6\text{O}_7\text{H}_5^{3-}] = 1.6 \times 10^{-6}$ M, $[\text{Cl}^-] = 1.2 \times 10^{-6}$ M, $[\text{H}_3\text{O}^+] = 2.5 \times 10^{-7}$ M, and $[\text{OH}^-] = 4.0 \times 10^{-8}$ M. Substituting these values in equation 6.4 gives the Debye length, κ^{-1} , for the gold colloid as 81.5 nm.

6.5.3 Calculation of effective reduced surface potentials

The effective reduced surface potentials Y_{Au} , Y_{MHA} , and Y_{APTES} are related to the asymptotic expression of the electrostatic potentials $\psi_{Au}(r)$, $\psi_{MHA}(r)$, and $\psi_{APTES}(r)$ for an isolated Au nanoparticle, and isolated MHA functionalized substrate and an isolated APTES functionalized substrate, respectively, by: [6.27-6.29, 6.32]

$$\begin{aligned}\psi_{Au}(r) &= \frac{kT}{e} a Y_{Au} \frac{e^{-\kappa(r-a)}}{r} \\ \psi_{MHA}(z) &= \frac{kT}{e} Y_{MHA} e^{-\kappa z} \\ \psi_{APTES}(z) &= \frac{kT}{e} Y_{APTES} e^{-\kappa z}\end{aligned}\quad (6.5)$$

For a given electrolyte condition, the effective reduced surface potentials Y_{Au} , Y_{MHA} , and Y_{APTES} are functions of the actual surface potentials $\psi_{s,Au}$, $\psi_{s,MHA}$, and $\psi_{s,APTES}$ of a Au nanoparticle, MHA, and APTES functionalized surfaces, respectively. The surface potentials $\psi_{s,Au}$, $\psi_{s,MHA}$, and $\psi_{s,APTES}$ are functions of the surface charge densities σ_{Au} , σ_{MHA} , and σ_{APTES} of a Au nanoparticle, MHA and APTES functionalized substrates, respectively [6.21, 6.27, 6.30]. For the calculation of Y_{Au} , Y_{MHA} , and Y_{APTES} , the approximate analytical expression by Ohshima [6.28, 6.30] were used.

6.5.4 Calculation of effective reduced surface potentials for planar geometry

For planar surfaces functionalized with either MHA or APTES, Y_{MHA} , and Y_{APTES} are related to their surface potentials $\psi_{s,MHA}$, and $\psi_{s,APTES}$ by [6.28].

$$Y_{MHA} = \frac{\psi_{s,MHA}}{kT} \exp \left[\int_0^{\frac{\psi_{s,MHA}}{kT}} \left\{ \frac{1}{f(y)} - \frac{1}{y} \right\} dy \right]$$

and

$$Y_{APTES} = \frac{\psi_{s,APTES}}{kT} \exp \left[\int_0^{\frac{\psi_{s,APTES}}{kT}} \left\{ \frac{1}{f(y)} - \frac{1}{y} \right\} dy \right] \quad (6.6)$$

with

$$f(y) = (1 - e^{-y}) \times \left[\frac{2 \sum_{i=1}^N M_i (e^{-z_i y} - 1)}{(1 - e^{-y})^2 \sum_{i=1}^N z_i^2 M_i} \right] \quad (6.7)$$

where z_i is the valency of the ion species i , and M_i is the molar concentration of ion species i .

For planar surfaces, the relationship between the surface potential ψ_s ($\psi_{s,MHA}$ or $\psi_{s,APTES}$) and the surface charge density σ (σ_{MHA} or σ_{APTES}) is given by the Grahame equation [6.21]

$$\sigma^2 = 1000 N_A (2 \varepsilon \varepsilon_0 kT) \sum_i \left\{ M_i (e^{-z_i e \psi_s / kT} - 1) \right\} \quad (6.8)$$

where N_A is the Avogadro's number, ε is the dielectric constant of water, and ε_0 is the permittivity of free space. Once σ_{MHA} and σ_{APTES} are known, Y_{MHA} and Y_{APTES} can be calculated using equations (6.6), (6.7), and (6.8).

The value of the surface charge density for a carboxyl terminated surface, σ_{MHA} , was obtained from the detailed AFM measurements by Kane and Mulvaney, where the surface potential data at various pH values and ionic strengths were reported [6.35]. For each of their experimental conditions, the surface charge density was calculated using the Grahame equation (6.8). The results of the obtained surface charge densities are summarized in Table 6.1.

Table 6.1 The surface charge densities of carboxyl terminated surfaces in an aqueous solution of varying ionic strengths.

Electrolyte condition ^a	Surface Potential ^a (at pH ~ 6.5)	Surface Charge Density ^b
0.03 mM NaNO ₃	-87 (mV)	- 0.0017 (C/m ²)
0.1 mM NaNO ₃	-57 (mV)	- 0.0016 (C/m ²)
1 mM NaNO ₃	-23 (mV)	- 0.0015 (C/m ²)

^a Data from Kane and Mulvaney [6.35]

^b Calculated values using the Grahame equation (6.8)

It should be noted from Table 6.1 that for the same pH, the surface charge density remains the same irrespective of the ionic strengths. This is because the deprotonation of H⁺ from the carboxyl group is governed by the pH value and not by the concentration of other ions unless they are strongly bound to the carboxyl group. A surface charge density of - 0.0017 (C/m²) was used for the MHA functionalized substrate in the calculation of the interaction energies.

For the surface charge density of APTES functionalized surface, σ_{APTES} , a reported value of 0.0042 (C/m²) was used. This value was obtained with laser Doppler electrophoresis [6.36].

With the known values of σ_{MHA} and σ_{APTES} , the surface potentials $\psi_{s,MHA}$ and $\psi_{s,APTES}$, and the effective reduced surface potentials Y_{MHA} and Y_{APTES} were calculated using equations (6.6), (6.7), and (6.8). Table 6.2 summarizes the calculated results.

Table 6.2 Surface potentials $\psi_{s,i}$ and the effective reduced surface potentials Y_i calculated from equations (6.6), (6.7) and (6.8) and known charge densities σ_i under the ionic strength used for the experiments.

Surface Functionalization	Surface charge density σ_i	Surface potential $\psi_{s,i}$	Effective reduced surface potential Y_i
MHA	- 0.0017 (C/m ²)	-120 (mV)	- 5.62
APTES	0.0042 (C/m ²)	69 (mV)	1.07

6.5.5 Calculation of effective reduced surface potentials for spherical geometry

For a spherical Au nanoparticle, the effective reduced surface potential, Y_{Au} , is given by [6.28]

$$Y_{Au} = \frac{\psi_{s,Au}}{kT} \exp \left[\int_0^{\frac{\psi_{s,Au}}{kT}} \left\{ \frac{1}{F(y)} - \frac{1}{y} \right\} dy \right] \quad (6.9)$$

where

$$F(y) = \frac{\kappa a}{\kappa a + 1} f(y) \times \left[1 + \frac{2(2\kappa a + 1)}{(\kappa a)^2} \frac{1}{f^2(y)} \int_0^y f(u) du \right] \quad (6.10)$$

and

$$f(y) = (1 - e^{-y}) \times \frac{\left[2 \sum_{i=1}^N M_i (e^{-z_i y} - 1) \right]}{(1 - e^{-y})^2 \sum_{i=1}^N z_i^2 M_i} \quad (6.11)$$

The relationship between the surface potential, $\psi_{s,Au}$, and the surface charge density, σ_{Au} , is obtained through [6.30]

$$\sigma_{Au} = \frac{\varepsilon\varepsilon_0\kappa kT}{e} f\left(\frac{\psi_{s,Au}}{kT}\right) \left[1 + \frac{2}{\kappa a f^2\left(\frac{\psi_{s,Au}}{kT}\right)} \int_0^{\frac{\psi_{s,Au}}{kT}} f(y) dy \right] \quad (6.12)$$

From equations (6.9) to (6.12) the effective reduced surface potential, Y_{Au} , can be calculated once the surface charge density, σ_{Au} , is known.

The surface charge density, σ_{Au} , was obtained from the AFM experiment by Biggs *et al.*, who deduced the surface potentials from measurements of forces between a Au surface and a Au coated cantilever in aqueous trisodium citrate solutions at different concentrations. From the surface potentials obtained for given trisodium citrate concentration, the surface charge densities were calculated using the Grahame equation (6.8). The results are summarized in Table 6.3. It should be noted that the surface charge densities remain almost the same even though trisodium citrate concentrations varied about two orders of magnitude. This can be easily understood, as in the case of carboxyl terminated surface discussed earlier, because the citrates strongly adsorb on the Au surfaces [6.37, 6.38] and their deprotonation remains the same for a given pH. The surface charge density value of -0.0028 (C/m²) for used in the calculation of Y_{Au} since its corresponding trisodium citrate concentration is close to that of the Au colloid used in the experiments.

From equations (6.9) to (6.12) and with -0.0028 (C/m²) for σ_{Au} , the effective reduced surface potential for a Au nanoparticle of 10 nm radius, Y_{Au} , was obtained as -1.59 .

Table 6.4 summarizes the effective reduced surface potentials Y_{MHA} , Y_{APTES} , and Y_{Au} .

Table 6.3 The surface charge densities of Au surfaces in aqueous trisodium citrate solutions of varying concentrations.

Trisodium citrate concentration ^a	Surface Potential ^a (at pH 6.3)	Surface Charge Density ^b
6×10^{-6} M	- 125 (mV)	- 0.0028 (C/m ²)
1×10^{-4} M	- 84 (mV)	- 0.0050 (C/m ²)
3×10^{-4} M	- 53 (mV)	- 0.0045 (C/m ²)

^a Data from Biggs *et al.* [6.38]

^b Calculated values using the Grahame equation (6.8)

Table 6.4 Summary of all the effective reduced surface potentials calculated for the ionic strength used in the experiments.

Y_{MHA}	Y_{APTES}	Y_{Au}
- 5.62	1.07	- 1.59

The van der Waals interaction energies $W_{MHA}(z)$ and $W_{APTES}(z)$ are given by [6.21]

$$W_{MHA}(z) = -\frac{A_{MHA}a}{6z}$$

and

$$W_{APTES}(z) = -\frac{A_{APTES}a}{6z} \quad (6.13)$$

where A_{MHA} and A_{APTES} are the Hamaker constants for the system of Au/MHA/water/Au and SiO₂/APTES/water/Au, [6.39, 6.40] the reported values of which are 2.5×10^{-19} and 5.7×10^{-19} J, respectively [6.41, 6.42].

6.5.6 Calculation of total interaction energies

From equations (6.1), (6.3), (6.4), and (6.13), the total interaction energies $V_{MHA}(z)$ and $V_{APTES}(z)$ are obtained and plotted as shown in Figure 6.9 and 6.10, respectively. The calculation results shown in these plots reveal the nature of the guiding forces seen in the experiments. The total interaction energies $V_{MHA}(z)$ and $V_{APTES}(z)$ are dominated by the electrostatic double layer interactions as long as the nanoparticle surface separation is more than 10 nm. For MHA functionalized substrates, the interaction with a Au nanoparticle is repulsive (positive interaction energies) and for APTES functionalized substrates, the interactions are attractive (negative interaction energies), as expected from the surface charge states of Au nanoparticles, MHA, and APTES.

Most importantly, the plots indicate that the interactions are of long range: for the interaction between a Au nanoparticle with MHA functionalized substrates, the interaction energy, $V_{MHA}(z)$, reaches the room temperature thermal energy of ~ 25 meV at ~ 370 nm away from the substrate surface. For the interaction between a Au nanoparticle and an APTES functionalized surface, $V_{APTES}(z)$, reached room temperature thermal energy of ~ 25 meV at ~ 270 nm from the substrate surface.

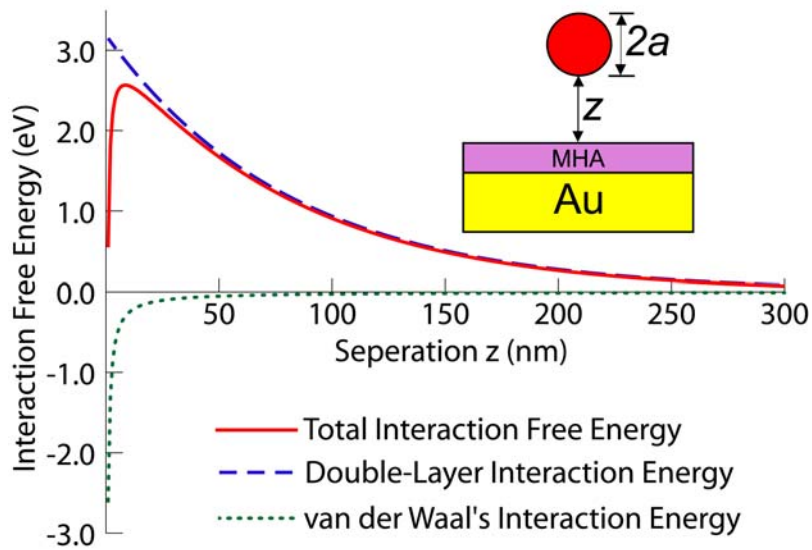


Figure 6.9 The total interaction energy $V_{MHA}(z)$ between a 20 nm Au nanoparticle ($a = 10$ nm) and a MHA functionalized substrate (red line) as the sum of the double layer interaction energy $\Phi_{MHA}(z)$ (blue dashed line), and the van der Waals interaction energy $W_{MHA}(z)$ (green dotted line).

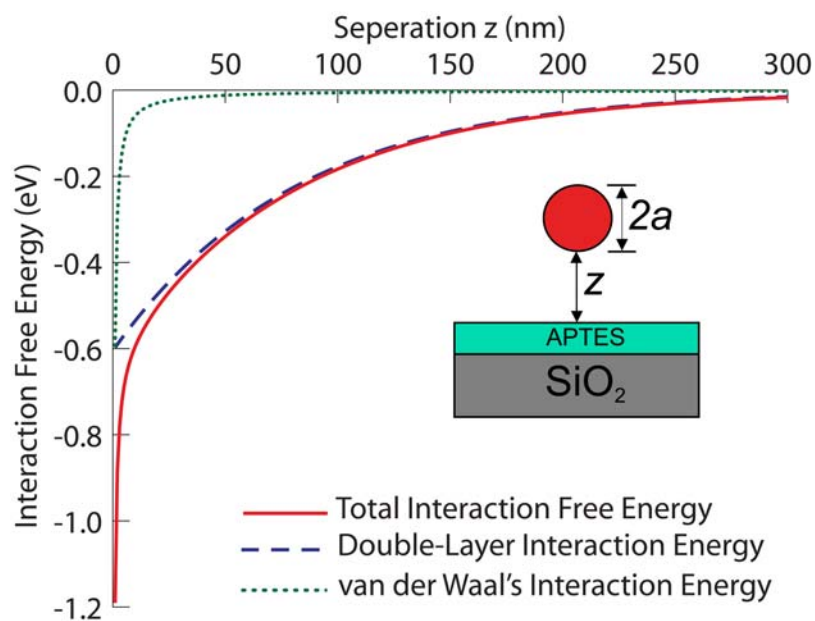


Figure 6.10 The total interaction energy $V_{APTES}(z)$ between a 20 nm Au nanoparticle ($a = 10$ nm) and an APTES functionalized substrate (red line) as the sum of the double layer interaction energy $\Phi_{APTES}(z)$ (blue dashed line), and the van der Waals interaction energy $W_{APTES}(z)$ (green dotted line).

6.6 Interaction between two identical nanoparticles in an aqueous medium

The electrical double layer interaction energy between two identical Au nanoparticles, $\Phi_{Au}(z)$, can be calculated by [6.28, 6.33]

$$\Phi_{Au}(z) = 4\pi\epsilon\epsilon_0 \left(\frac{kT}{e}\right)^2 \left(\frac{a^2}{2a+z}\right) Y_{Au}^2 \exp(-\kappa z) \quad (6.14)$$

where a is the nanoparticle radius ($a = 10$ nm for my experiments) and z is the separation between the particle surfaces. $Y_{Au} = -1.59$ (Table 6.4) and $\kappa = \frac{1}{81.5} \text{ nm}^{-1}$, was used in equation (6.14) to give the double layer interaction energy between a pair of 20 nm Au nanoparticles.

The van der Waals interaction energy between a pair of nanoparticles, $W_{Au}(z)$, is given by [6.21]

$$W_{Au}(z) = -\frac{A_{Au}a}{12z} \quad (6.15)$$

where A_{Au} is the Hamaker constant for Au-water-Au system, which is equal to 2.5×10^{-19} J [6.41]. Inserting these values into equation (6.15), the van der Waals forces of attraction between two similar Au nanoparticles in the colloid can be obtained.

The total free energy of interaction, $V_{Au}(z)$, is the sum of the double layer interaction energy and the van der Waals interaction energy. Figure 6.11 shows the free energy of interaction between a pair of 20 nm diameter Au nanoparticles as a function of the distance between their surfaces. From the plot, it can be seen that $V_{Au}(z)$ reaches the room temperature thermal energy of 25 meV at $z \sim 70$ nm. This value agrees very well with the observed interparticle separations of ~ 50 nm in Figure 6.5.

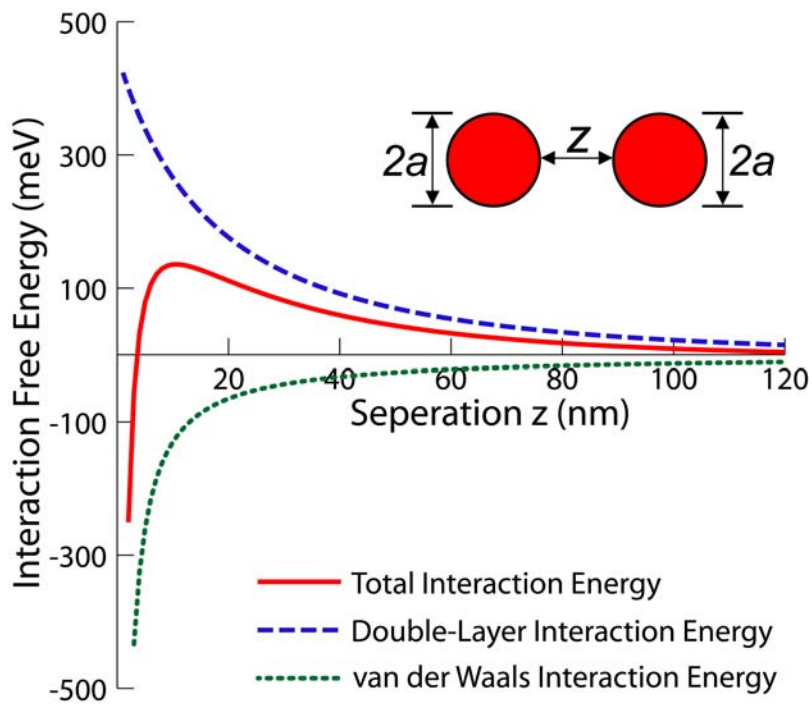


Figure 6.11 The total interaction energy $V_{Au}(z)$ between a pair of 20 nm Au nanoparticles ($a = 10$ nm) as the sum of the double layer interaction energy $\Phi_{Au}(z)$ (blue dashed line), and the van der Waals interaction energy $W_{Au}(z)$ (green dotted line).

6.7 Application of electrostatic funneling in the fabrication of single-electron devices

The electrostatic funneling method has been successful in aligning Au nanoparticles on the side-walls of a 3-dimensional step structure as shown in Figure 6.7. This step structure consisted of a layer of silicon oxide which was sandwiched between two gold electrodes similar to the new single-electron device structure. For single-electron transport to take place the dielectric between the source electrode and the island and between the island and the drain must be thin (~ 1 nm) so that electron tunneling can occur in the device. It can be seen from Figure 6.7 that the insulating gap between the Au nanoparticle and the top and bottom metal layers are much larger than what is desirable for single-electron tunneling. The reason as to why this happens is because the repelling forces on the nanoparticles exerted by the surfaces functionalized with MHA (Au surfaces) are very large thus pushing the nanoparticles to greater distances away from the surfaces.

To apply the electrostatic funneling scheme for single-electron devices, the thickness of the silicon oxide layer must be comparable to the size of the Au nanoparticle (ideally, the thickness of the silicon oxide layer must be $\sim 1-2$ nm more than the size of the Au nanoparticle) so that tunneling barriers of the desired thickness can form on either side of the island. Also, the nature of the guiding forces on the nanoparticles to be aligned must be such that it does not experience a very large repelling force but large enough so that they position themselves on the exposed silicon oxide side-wall between the two electrodes.

Figure 6.12 is the schematic of how the electrostatic funneling scheme can be applied in the fabrication of single-electron devices. In the structure, the silicon oxide areas were functionalized with APTES SAMs (described earlier) but the negatively charged SAMs on the gold surface was replaced with nonpolar SAMs using *n*-octadecanethiol (ODT; $\text{HS}-(\text{CH}_2)_{17}-\text{CH}_3$; 98%; Sigma-Aldrich). The APTES SAMs was formed on the silicon oxide surfaces first followed by the formation of the ODT SAMs. The ODT SAMs were formed by immersing the sample in a 5 mM solution of ODT in hexadecane for 42 hours at 40 °C, followed by rinsing the sample with

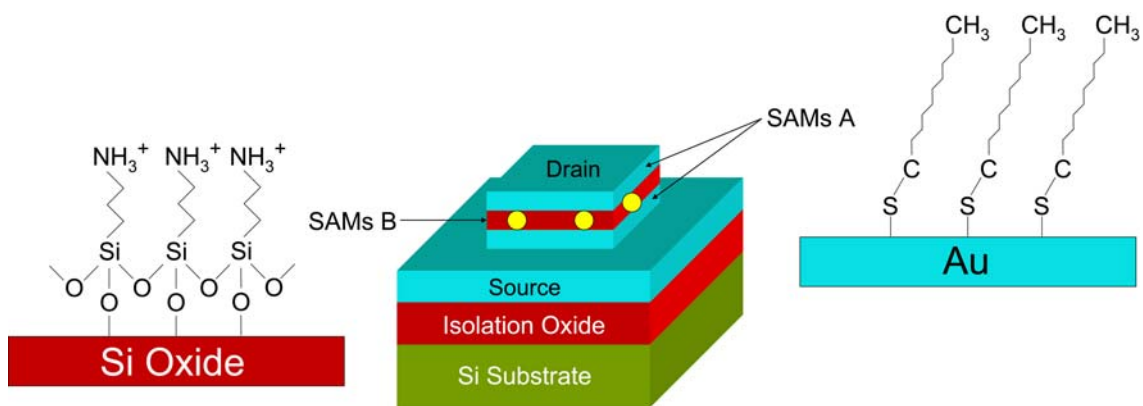


Figure 6.12 Schematic for the selective placement of nanoparticles exclusively on the side walls of silicon oxide. The oxide side walls and the source/drain electrodes are functionalized with SAMs having different polarities.

warm acetone (40 °C) and drying under a jet of compressed nitrogen gas.

Figure 6.13 shows an FE-SEM image of a single-electron device structure in which ~ 80 nm Au nanoparticles were placed precisely in between two Au electrodes. The electrostatic funnel was created using a combination of APTES and ODT SAMs as described above. It can be seen from the image that not only are the nanoparticles perfectly positioned in between the two electrodes but there is a complete absence of the nanoparticles on the source and the drain electrodes. Also, it is evident that the ODT SAMs provides the ~ 80 nm Au nanoparticles with a much smaller repelling force as compared to the MHA SAMs (Figure 6.7 (b)) because the nanoparticles occupy positions that are not far away from the metal/dielectric interface. If the thickness of the silicon oxide layer is reduced down to ~10 nm and ~10 nm diameter Au nanoparticles are used as the Coulomb islands, single-electron devices may be able to be fabricated with a much higher yield as compared to the present study.

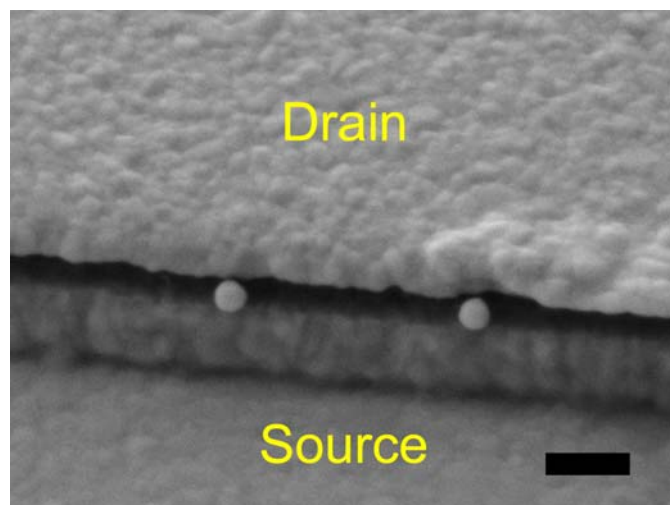


Figure 6.13 FE-SEM image showing the selective placement of ~ 80 nm Au nanoparticles exclusively on the side wall of silicon oxide (dark lines). The oxide side walls are functionalized with SAMs of 3-aminopropyltriethoxysilane (APTES; $(\text{C}_2\text{H}_5\text{O})_3\text{-Si-(CH}_2)_3\text{-NH}_2$) while the surfaces of the source and drain electrodes are functionalized with SAMs of *n*-octadecanethiol (ODT; $\text{HS-(CH}_2)_{17}\text{-CH}_3$). Scale bar = 200 nm

CHAPTER 7

CONCLUSION

Single-electron devices have many advantages over conventional electronic devices, including the fact that they consume very little power, can operate in the sub-nanometre regime (which means that many devices can be packed into an extremely small space), and have the ability to detect an extremely small amount of charge (even down to a fraction of the charge of a single electron). These advantages of single-electron devices could benefit a variety of applications including space, military, and commercial electronics.

However, fabricating these devices on a large scale has not been possible mainly due to low throughputs, inability to accurately control the source-drain electrode gap for every device and/or because the processes are too slow for practical applications. Large-scale fabrication of single-electron devices is necessary to have multiple and individually addressable devices.

In Chapter 3, a new single electron device structure was proposed. The key merit of the new structure is to provide a way to fabricate single-electron devices on a large-scale, in parallel processing, and using existing CMOS fabrication technology. This was accomplished by employing a vertical electrode configuration in which the source and the drain electrodes were vertically stacked on top of each other and were separated by a thin layer of dielectric film as detailed in Chapter 4. Using this configuration, the gap between the electrodes was able to be controlled down to a sub-nanometer scale precision over an entire wafer thereby allowing the concurrent fabrication of many device units in parallel processing. Coulomb islands were positioned in the gap between the source and the drain electrodes using a combination of self-assembled monolayers and colloidal chemistry. Individually addressable gate electrodes were then incorporated in these devices also in complete parallel processing.

In Chapter 5, the I-V measurements of these devices were carried out at room temperature as well as at low temperatures. The devices have yielded clear Coulomb blockade, Coulomb staircase, and Coulomb oscillations which are decisive indications of single-electron transport phenomena in these devices. The nature of the I-V characteristics suggests that the single-electron transport takes place only through one nanoparticle. A detailed and systematic study of device characteristics depending upon the size of the Coulomb island, location of the Coulomb island on the device structure, and effect of temperature were also carried out. The I-V characteristics of these devices were also simulated based on the orthodox theory of single-electron tunneling. It was found that the results of the simulations were in excellent agreement with the experimental data.

To improve the device yield of the single-electron devices, a new method named electrostatic funneling was proposed in Chapter 6. In this method, charged nanoparticles were guided by an electrostatic guiding structure and placed onto targeted substrate locations. The guiding structures were formed by self-assembled monolayers (SAMs) on silicon wafers which had alternating lines of silicon oxide and gold. With this method, a placement precision of ~ 6.2 nm was demonstrated using 20 nm Au nanoparticles. Detailed calculations were also performed based on the DLVO theory to determine the nature of the guiding forces. These calculations were able to quantitatively explain the observed results very well.

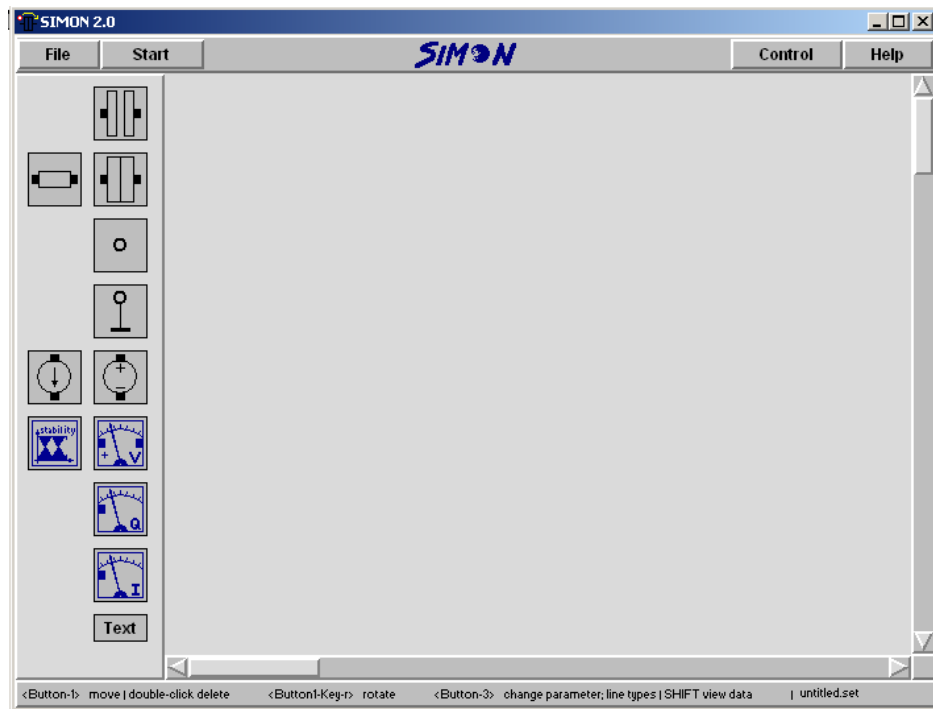
This study demonstrated the chip level fabrication of single-electron devices that are operable at room temperature. The biggest advantage of this method is that it does not employ any sophisticated methods for the nanoscale pattern definition and has no limitations for large-scale processing. The simplicity of this approach combined with the fact that it is compatible with existing CMOS technology means that the fabrication of chip-level integrated systems of single-electron devices may now be possible using current CMOS fabrication technology.

APPENDIX A

SIMULATION OF SINGLE-ELECTRON DEVICES USING SIMON

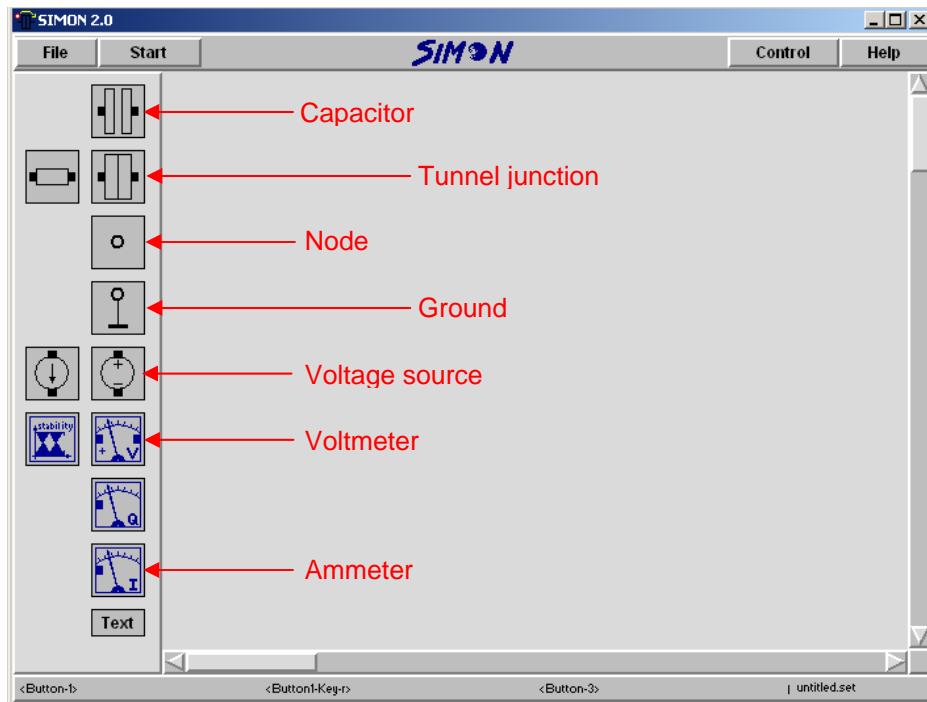
SIMON (Simulation of Nano Structures) is a multipurpose simulator for single-electron devices and circuits developed by Dr. Christoph Wasshuber. The simulation of the single-electron devices reported in this thesis was carried out using SIMON. This software calculates the current in the single-electron devices as a function of the applied voltages. This Appendix is the detailed description of how to use SIMON to simulate single-electron devices.

Install the SIMON software onto a Windows based PC by double clicking the SIMON v 2.0 application onto C:\Program Files\SIMON2.0. Once the installation is complete, run the application from the Windows Start Menu > All Programs > SIMON. The interactive screen looks like the one shown in Screenshot A.1. Additionally create a temporary folder on the C:\ drive. This folder will be used to store the temporary files used by this program.



Screenshot A.1.

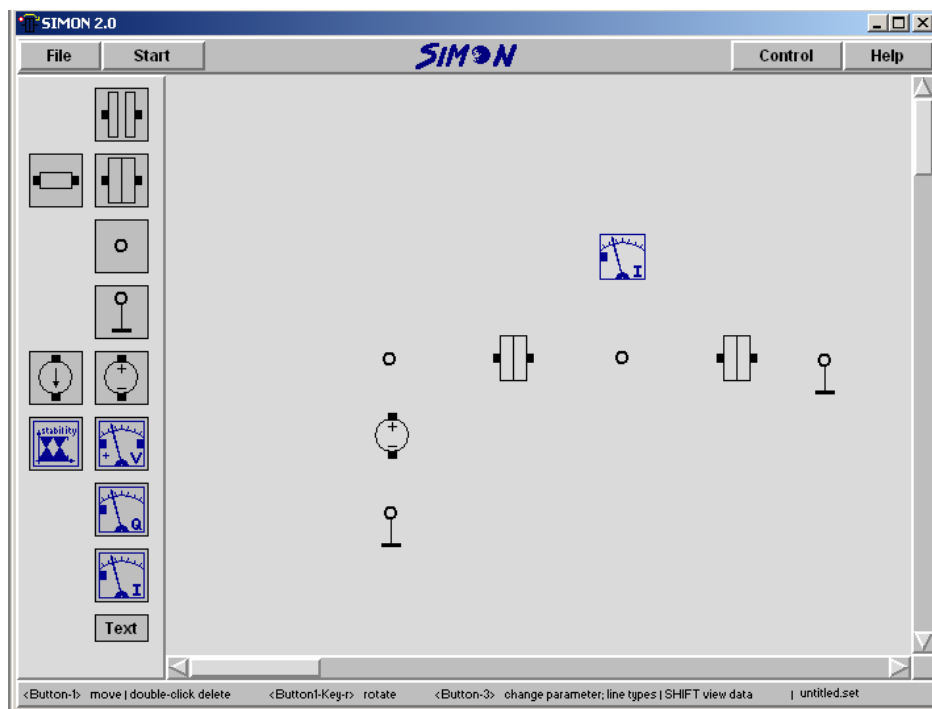
The basic building blocks required to create single-electron devices are labeled in Screenshot A.2.



Screenshot A.2.

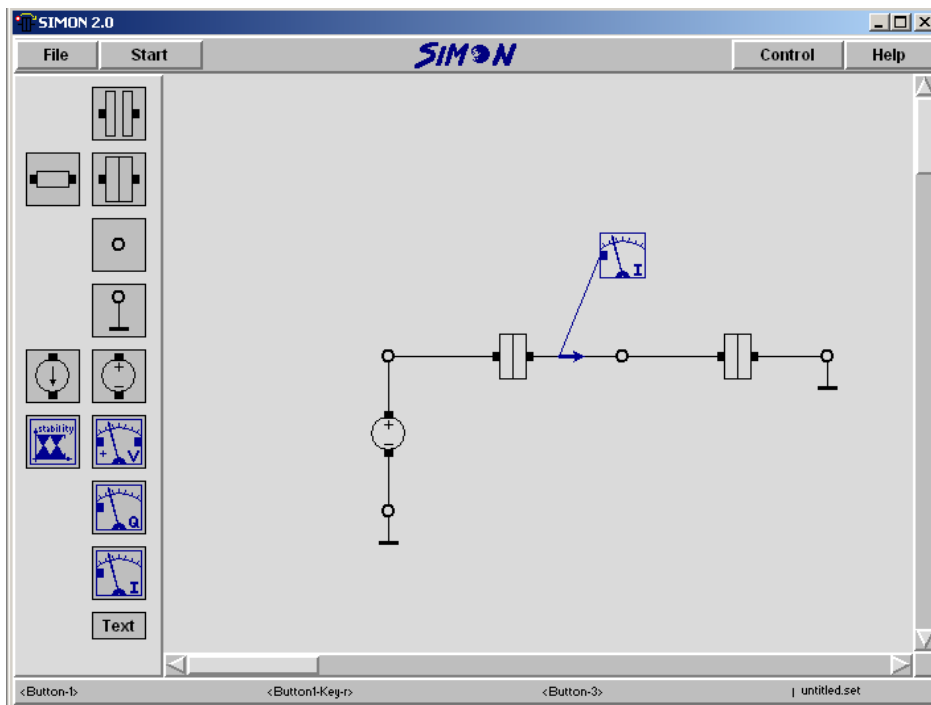
To create a double junction single-electron device

Move the mouse cursor over the voltage source icon. Left click on the voltage source icon and drag it onto the working area of the SIMON screen. Use the same procedure to include two ground icons, two nodes, two tunnel junctions, and an ammeter onto the working area as shown in Screenshot A.3.



Screenshot A.3.

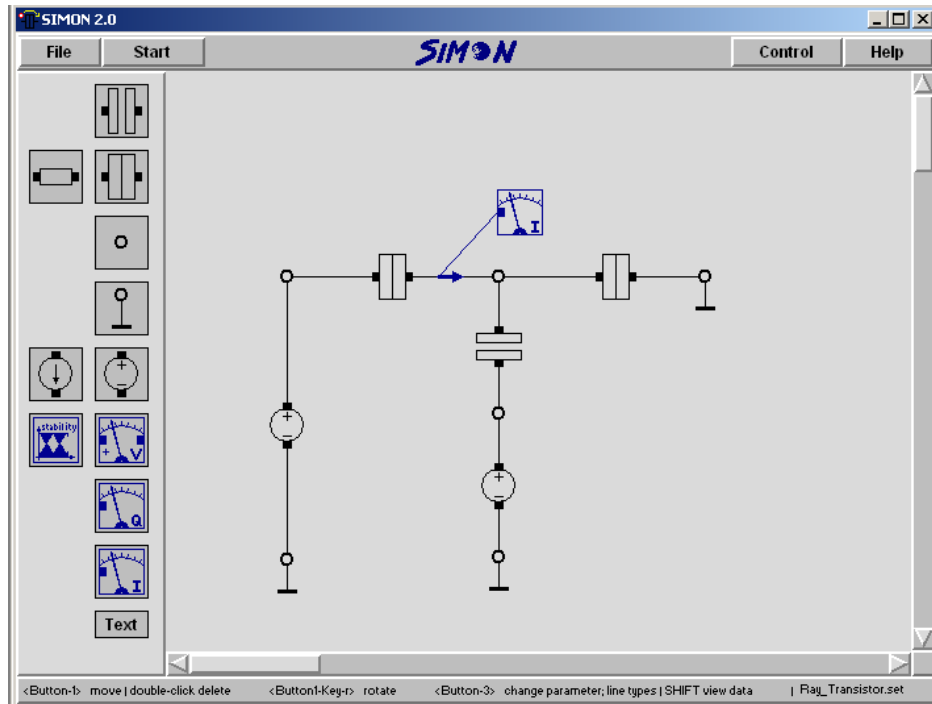
Connect the components i.e., voltage sources, tunnel junctions, or ammeter to the nodes or the grounds by moving the mouse over the black square regions of the components and clicking and holding the left mouse button at the same time. Now move the mouse so as to drag a connection from the component to the node or ground as shown in Screenshot A.4. Save the device using File > Save As > "Device Name".



Screenshot A.4.

To create a single-electron transistor

To create a single-electron transistor, drag another voltage source, a ground, a node and a capacitor into the working area. Make the connections as shown in Screenshot A.5. Save the device using File > Save As > “Device Name”.

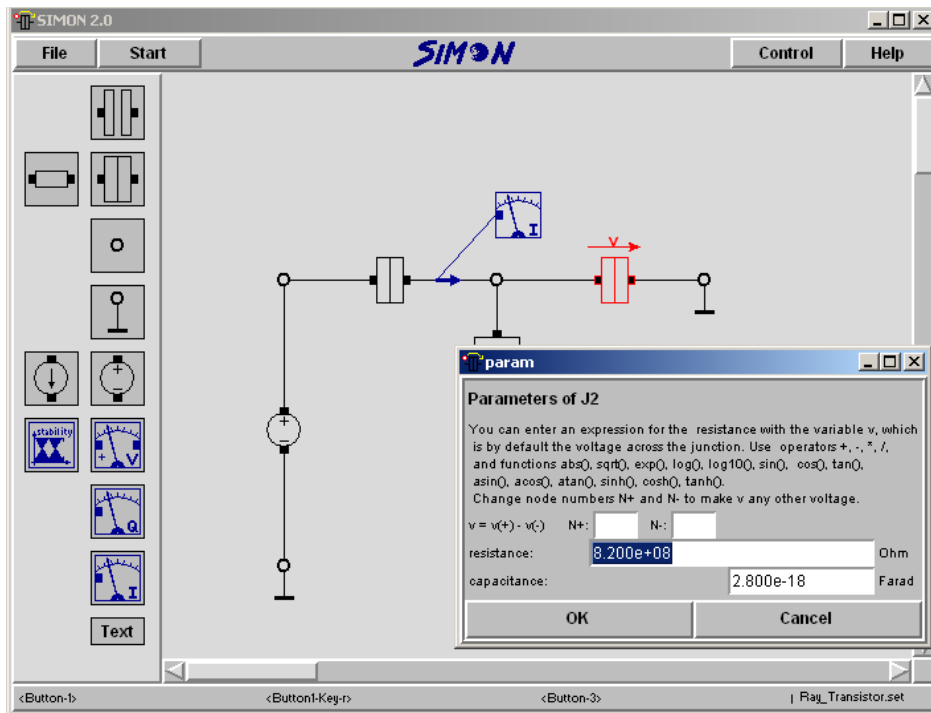


Screenshot A.5.

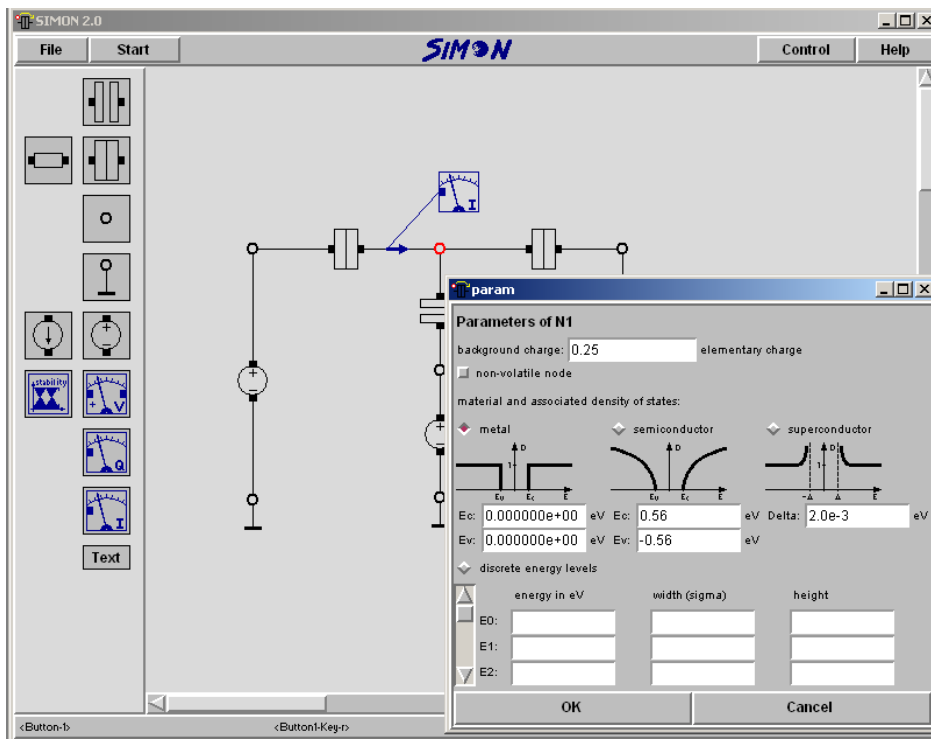
To set the parameters of a tunnel junction (C and R), move the mouse over a tunnel junction and right click on it. Enter the parameters in the boxes provided (see Screenshot A.6.)

To set the parameters for the Coulomb island, move the mouse over the Coulomb island (center node) and right click. Set the parameters as required (see Screenshot A.7). For

example, to give a background charge of $\frac{e}{4}$ to the Coulomb island, enter 0.25 in the background charge area. You can also chose what type of Coulomb island to use in the simulation i.e., metal, semiconductor, or superconductor.

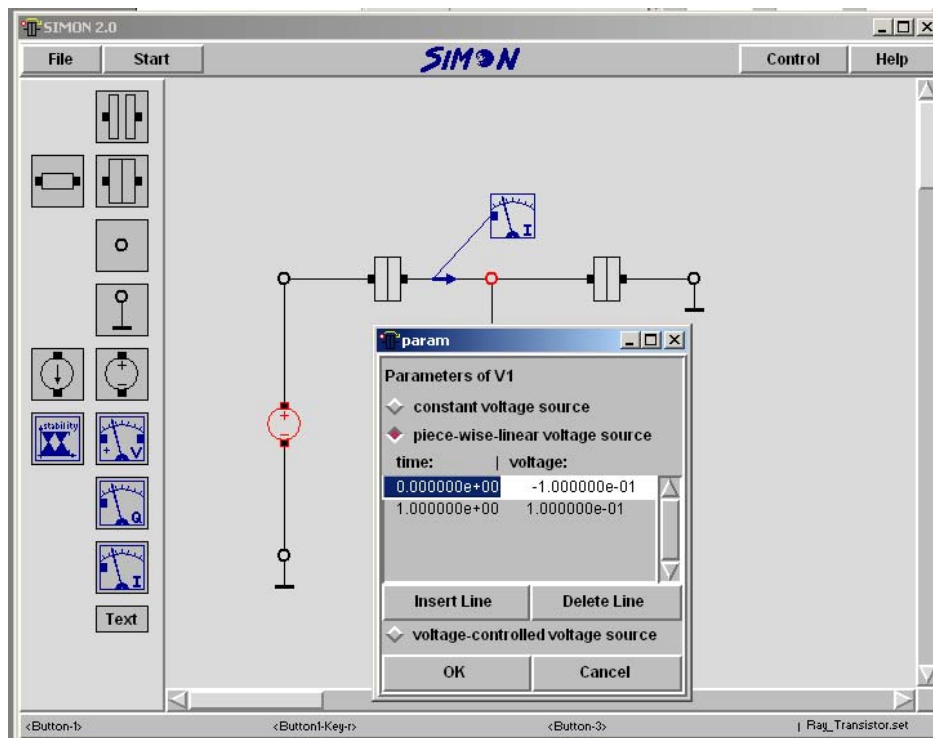


Screenshot A.6.



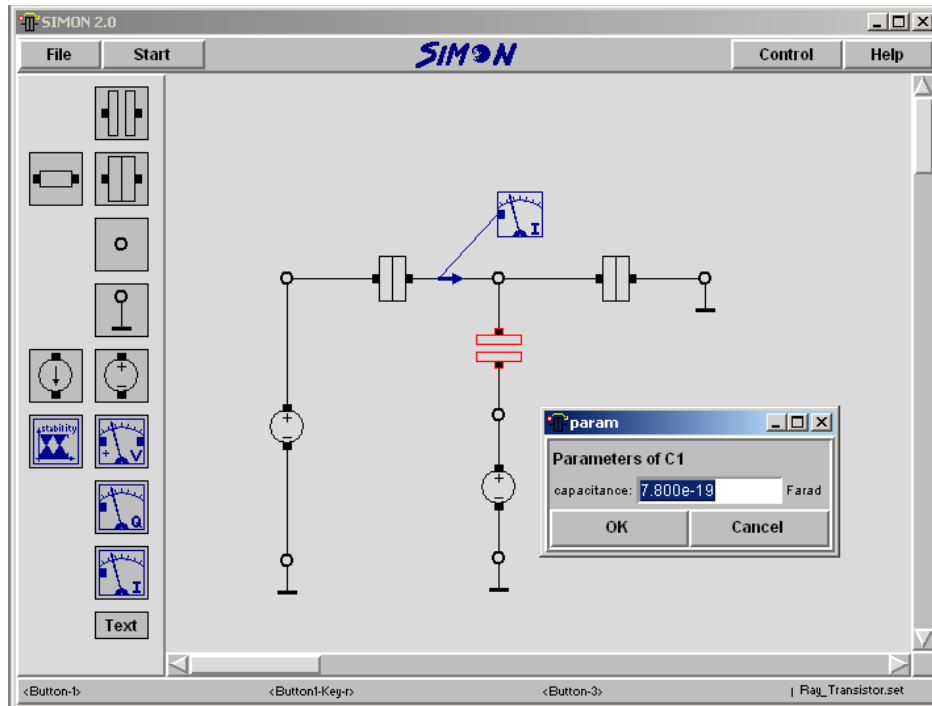
Screenshot A.7.

To set the voltage range, for the voltage sources, right click on the voltage source and chose either the constant voltage source or piece-wise-linear voltage source. If you chose piece-wise-linear voltage source, make sure that the start time is 0 and the end time is 1 on the left hand columns. On the right hand columns, enter the start voltage and the stop voltage that you want for the simulation. This is shown in Screenshot A.8.



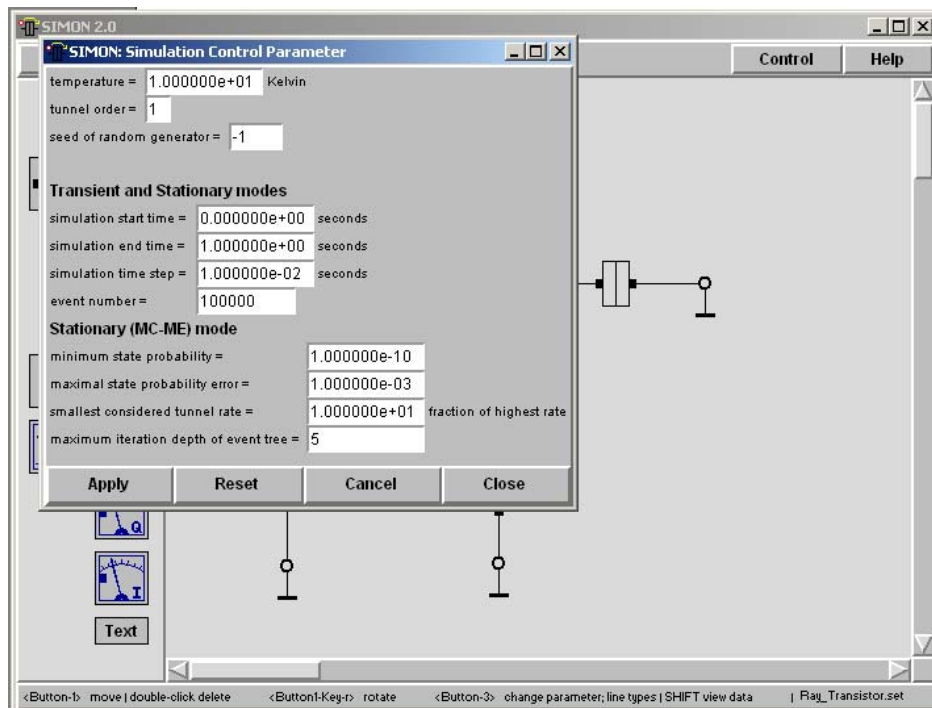
Screenshot A.8.

To set the capacitance value of the capacitor, right click on the capacitor and enter the desired capacitance value as shown in Screenshot A.9.



Screenshot A.9.

Once all the parameters of the various components of the single-electron device are set, go to the control tab on the top right corner of the screen. Click the control tab and select parameters. A screen resembling Screenshot A.10. will appear.



Screenshot A.10.

In this,

- (a) Set the desired temperature in K
- (b) Tunnel order = 1
- (c) Seed of random generator = -1
- (d) Simulation start time = 0 second
- (e) Simulation end time = 1 second
- (f) Simulation step time = 1.0×10^{-2} will give 100 data point for the simulation. A step time of 1.0×10^{-1} will give 10 data points and a step time of 1.0×10^{-3} will give 1000 data

points. Select the appropriate step time so as to obtain the desired number of data points

(g) Event number = 100000. The more the event number, the more number of averages the simulator performs and hence the simulation output has lesser noise. Less number of points will give more noisy simulation data. In order to obtain smooth curves, typically an event number between 75000 and 100000 is used.

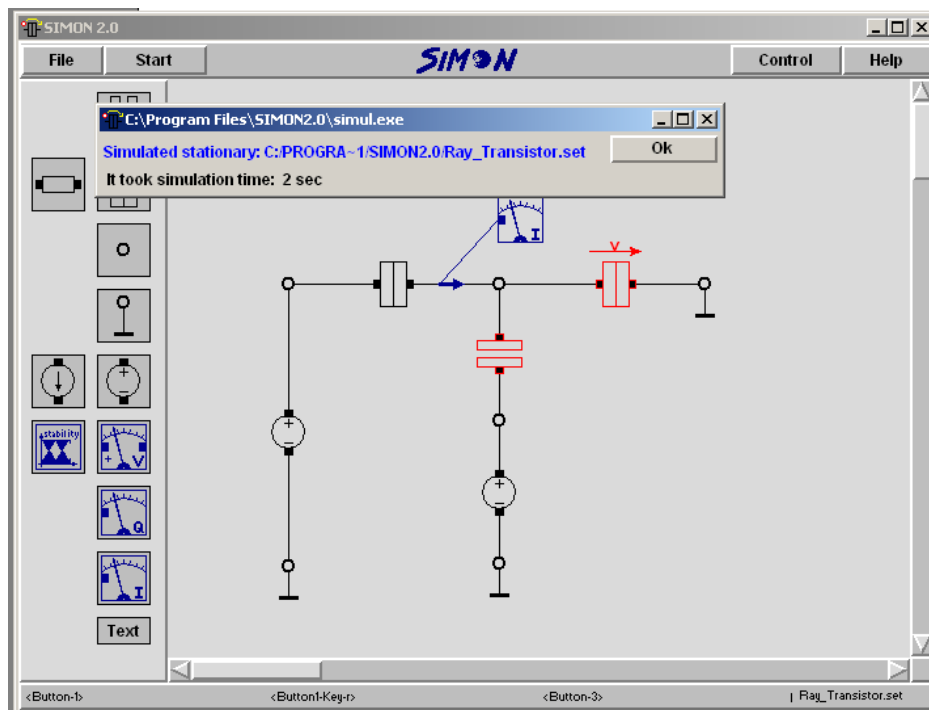
(h) Minimum state probability = 1.0×10^{-10}

(i) Maximal state probability error = 1.0×10^{-3}

(j) Smallest considered tunnel rate = 1.0×10^1

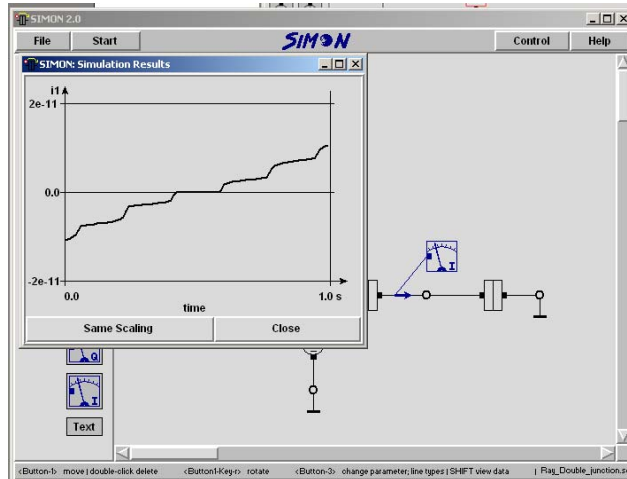
(k) Maximum iteration depth of event tree = 5.

Once the parameters are set, go to the start tab on the top left corner of the screen. Click the Start tab and select the Stationary Simulation from the drop down menu. The simulator starts the simulation for the particular device (refer Screenshot A.11.)

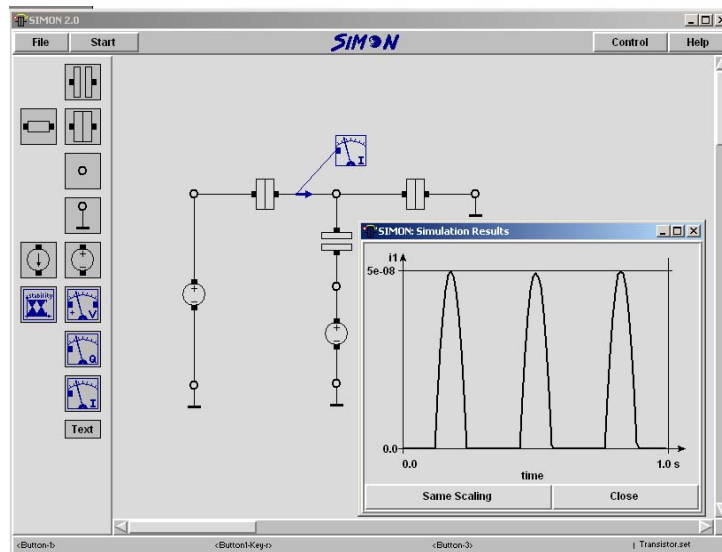


Screenshot A.11.

Once the simulation is complete, press OK. To observe the I-V characteristics of the device, right click on the Ammeter of the single-electron device while holding down the Shift button on the keyboard at the same time. Screenshot A.12. shows the I-V characteristics of a double junction single-electron device showing the Coulomb staircase and Screenshot A.13. shows the Coulomb oscillations in a single-electron transistor.



Screenshot A.12.



Screenshot A.13.

To import the simulated results to an Excel spreadsheet go to the Folder C:\Program Files\SIMON2.0. Look for a file name with "Device Name".i1. Copy this particular file and paste it in a separate location (usually in the temporary folder that was created in the C: drive). Save this file in "Device Name".txt format. Now open Microsoft Excel. Go to Data > Import External Data > Import Data. Select the location where the "Device Name".txt is saved and open it. Under the original data type, select the Delimited tab and click Next. Under the delimiters tab, select Tab and Space. Click Next and in the following screen, click Finish. To end, click OK. The results of the simulation will be imported to a excel sheet.

The first column in the spreadsheet is the Voltage and the second is the Device Current. Note that the start voltage appears as 0 second and the end voltage as 1 second. This has to be replaced with Volts to plot the I-V characteristics of the single-electron device. Replace the start voltage (initially 0 second) with the start voltage entered as shown in Screenshot A.8. For example, if the simulation start voltage was entered as -0.05 Volts, replace the 0 in the first column by -0.05. Similarly replace all the numbers in column 1 so that the voltage intervals are equally spaced and the last number in column 1 is the simulation end voltage, for example 0.05 Volts.

Once this is complete, use the Microsoft Excel Chart Wizard to plot the I-V data.

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