CHARACTERIZATION OF THERMAL CHALLENGES IN ELECTRONICS: LEAKAGE CURRENT, CO-ARCHITECTURAL DESIGN AND RACK LEVEL COOLING

by

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This thesis is dedicated to my parents, brother and friends

for their continuous support and encouragement

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ABSTRACT

CHARACTERIZATION OF THERMAL CHALLENGES IN ELECTRONICS:
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AND RACK LEVEL COOLING

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Since the advent of transistors and integrated circuits the complexity and functionality of the electronic products has gone up. In line with this, the scaling of the products is catching up at all levels of packaging. Current electronics era is driven by a mantra - “Miniaturization”. Recently the number of transistors on high end microprocessor has exceeded a billon mark. The design at board level becomes sophisticated to meet the growing demands. All of these lead to thermal and reliability challenges. A good thermal design is one which makes sure that the chip is operating at its rated frequency or speed while maintaining the junction temperature within permissible limits. Due to miniaturization the device dimensions shrink leading to various problems at device level like leakage current, hotspots, etc., these problems at device level add up and in turn creates thermal issues at system level. Owing to time to market requirements, CFD analysis allows to complete thermal optimization long before the product test can be made available bringing about financial benefits and timely engineering support during product development. Thus thermal management at various level of electronics design becomes

inevitable. In broad view thermal issues in electronics field is no longer an independent issue, it's ought to be multidisciplinary one. In this study device level issues like effect of gate oxide thickness on leakage current and co-architectural design of microprocessors is discussed. It is followed by system level thermal analysis of a telecommunication cabinet.

Part-1 of the thesis addresses a device level issue, "Static Power Consumption – Silicon on Insulator Metal Oxide Semiconductor Field Effect Transistor". The static power consumption due to leakage current plays a significant part in semiconductor devices, as the device dimensions continue to shrink. Low power dissipation is one of the critical factors needed to achieve high performance in a chip. New methods are continuously being implemented for reduction of leakage current in deep sub micron ultra thin SOI MOSFET using device simulator tools. In this paper, an 18nm gate length ultra thin SOI MOSFET is simulated for different silicon body thicknesses and the leakage current is determined by using the device simulator, MEDICITM. It is demonstrated that MEDICI™ device simulations is a good tool that can effectively be used for ultra thin SOI MOSFET devices to study the effect of design parameters on the leakage current.

Ultra thin SOI MOSFET with 18nm gate length of different Silicon body thickness is simulated and the leakage current as determined by using MEDICI™ shows that the leakage current decreases by 10-15% as the silicon body thickness reduces by 2 nm.

Part-2 of the thesis again focuses on a device level issue, "Multi-Objective optimization entailing computer architecture and thermal design for non-uniformly powered microprocessors". Microprocessors continue to grow in capabilities, complexity and performance. Microprocessors typically integrate functional components such as logic and level two (L2) cache memory in their architecture. This functional integration of logic and memory results in improved performance of the microprocessor. However, the integration also introduces a layer of complexity in the thermal design and management of microprocessors. As a direct result of functional integration,

the power map on a microprocessor is typically highly non-uniform and the assumption of a uniform heat flux across the chip surface has been shown to be invalid post Pentium II architecture. The active side of the die is divided into several functional blocks with distinct power assigned to each functional block. A lot of work has been done addressing this issue with a need of thermally aware computer architecture with a concurrent design approach based on thermal and device clock performance. Previous work has been done to minimize the thermal resistance of the package by optimizing the distribution of the non-uniform powered functional blocks with different power matrices. The study also provided design guidelines to minimize thermal resistance for any number of functional blocks for a given non-uniformly powered microprocessor. This analysis, however, had no constraints placed on the redistribution of functional blocks regarding the total wiring length of a particular configuration of functional blocks to satisfy electrical timing and computational performance requirements.

In this study, numerical model is developed that utilizes muti-objective optimization consists of redistribution of functional blocks to both improve device performance and thermal performance. Previously developed design guideline for thermal optimization is used as a base line case. This baseline case will be embedded into computer architecture (floor Plan) to developed numerical model satisfying both electrical and thermal performance. Constraints for the electrical optimization will include the total wiring length of a particular configuration of functional blocks. Once positioning of the functional blocks is done, thermal and electrical optimization of these non-uniformly powered functional blocks will be carried out simultaneously. This process will be repeated until you get both improved device performance and thermal performance for the non-uniformly powered microprocessor. Finally recommendation will be provided for an architecture design considering both the electrical constraint (total wiring length) and minimum thermal resistance there by improving the performance.

Part- 3 of the thesis deals with system level issue, “Rack Level Cooling”. Computational Fluid Dynamics (CFD) is an integral part in the development of new products. A telecommunication

cabinet has many components; therefore before the cabinet is manufactured it is necessary to know the thermal stability of the cabinet. It is extremely ineffective both in time and cost to build prototypes and test them (build and break approach). A CFD tool comes in handy for these kinds of problems where in lots of configurations can be modeled and tested in short periods of time. Based on the CFD results, a prototype cabinet is built and tested experimentally. Thus CFD tool allows for significant savings in both development and production. The development savings are realized by not having to physically build and test multiple configurations and the production savings are realized from cost reduction in the design.

This paper deals with design and thermal analysis of a Commscope telecommunication cabinet, RBA48. This cabinet is completely sealed and is cooled by Heat Exchangers (HX) and TEC modules. This kind of cooling technology is first tried in this family of cabinets by Commscope, hence the different design configurations needs to be tested for thermal stability. The analysis of RBA48 concentrates on

1. The optimum door opening for the TEC modules
2. Selection of HX fans – Outer loop fans
3. Position of Bay Fans in the Bay Fan Tray.

The CFD code Flotherm by Mentor Graphics is used for the analysis

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NOMENCLATURE

V	Voltage (V)
I	Current (I)
V_{dd}	Drain Voltage (V)
V_{gs}	Threshold Voltage (V)
I_d	Drain Current (I)
T	Temperature (^{0}C)
K	Thermal Conductivity (W/mK)
h	Convective Heat Transfer Coefficient (W/m^{2}K)

CHAPTER 1

INTRODUCTION

1.1 Introduction to Electronic Packaging

Electronic packaging refers to the enclosure for integrated circuit (IC) chips, passive devices, the fabrication of circuit cards and the production of a final product or system. Packaging is important for signal and power transmission, heat dissipation, electromagnetic interference (EMI) shielding and protection from environmental factors such as moisture, contamination, hostile chemicals and radiation.

The effectiveness, with which an electronic system performs its electrical functions, as well as the reliability and cost of the system, are strongly determined not only by the electrical design, but also by various aspects of packaging. It is packaging and assembly strategy that decides the weight, size, durability, performance and cost of the product. Increasing the electronic packaging technology determines the productivity and competitiveness of the electronics industry [1].

1.2 Packaging Hierarchy

In developing a thermal design for electronic products it is necessary to know about the various levels of packaging. Basically it is divided into three levels

1. Device or First level package : Chips into single chip modules (SCM) or Multichip modules (MCM)
2. Package or Second Level : Components (SCMs, MCMs, Connectors, etc.,) on a printed circuit board (PCB)

3. System of Third Level: PCB assemblies, cables, power supplies, cooling systems and peripherals into a frame or a box.

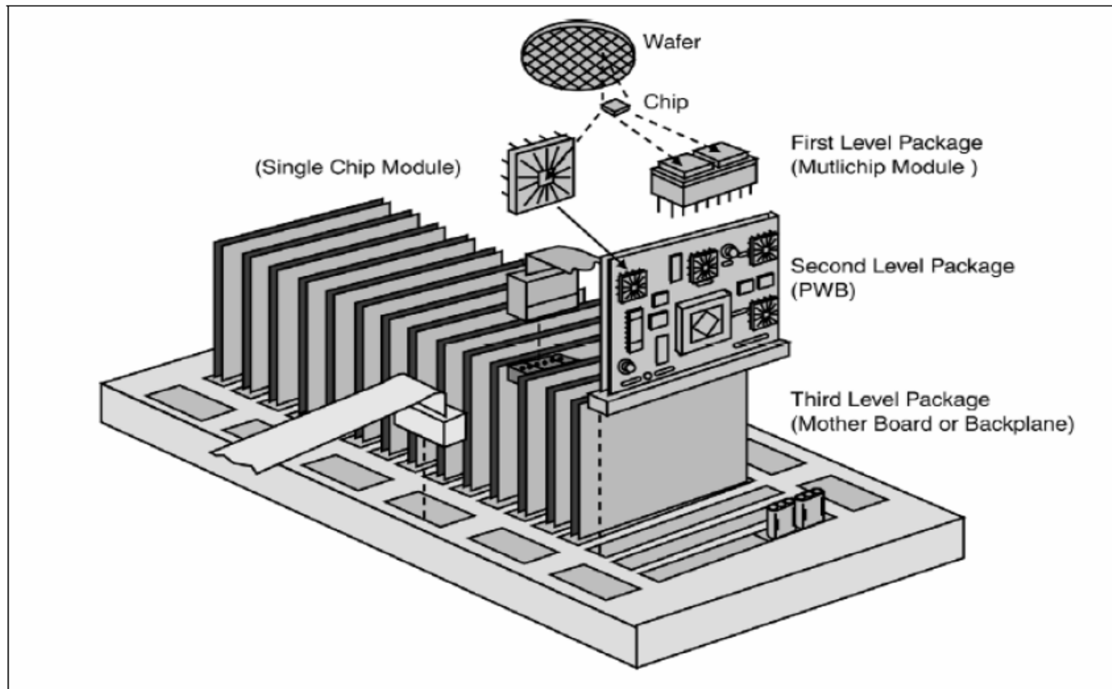


Figure 1.1 Packaging Hierarchy [2]

The packaging hierarchy starts from device level with the chip package, which houses and protects the chip. Then comes the PWB which houses lots of chip and it enables communication between them. The back plane or motherboard which interconnects the PWB comes next in the hierarchy order. So with these discrete structural levels in packaging, it is very important to focus on the level of the level of the package which is worked on. Moreover, based on the level of the package to be addressed, there are varied thermo-mechanical solution techniques that could be implemented for the optimal and reliable working of the electronic product [3]. Figure 1.1 shows the packaging hierarchy with the different structural levels.

1.3 Power Trends

In 1965 Gordon Moore published an article stating that the number of transistors on integrated circuit would keep doubling every 18-24 months, figure 1.2. This law had kept the electronics industry moving for half a decade and this law will hold good for another two technology nodes.

Ever since transistor and integrated circuit was invented the performance of electronic products kept on increasing and this trend will continue. On the other hand footprint of the products keeps on reducing demanding for better thermal design. The IRTS road map for industry shows that the maximum power dissipated by a chip is going to be 300W by 2015, figure 1.3. Figure 1.4, shows the heat load per equipment footprint increases for wide range of electronic products. Owing to increasing power trend, efficient thermal management without affecting the reliability and performance of the electronic products is going to be a challenge for the packaging industry.

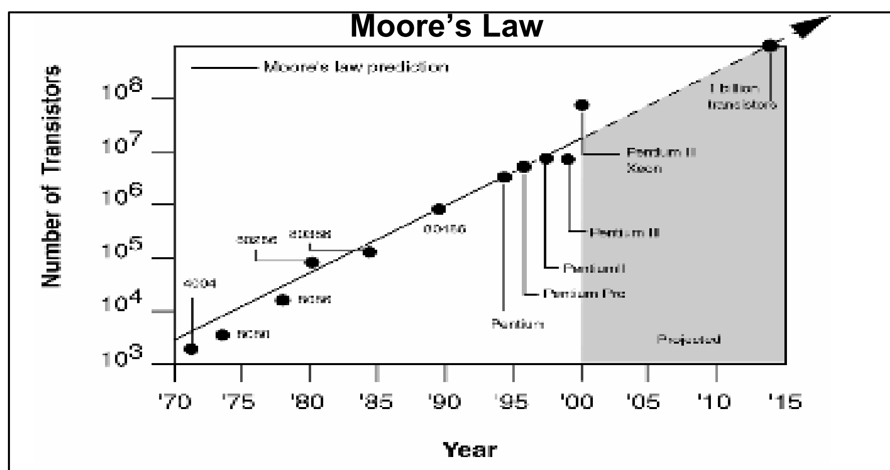


Figure 1.2 Moore's Law [2]

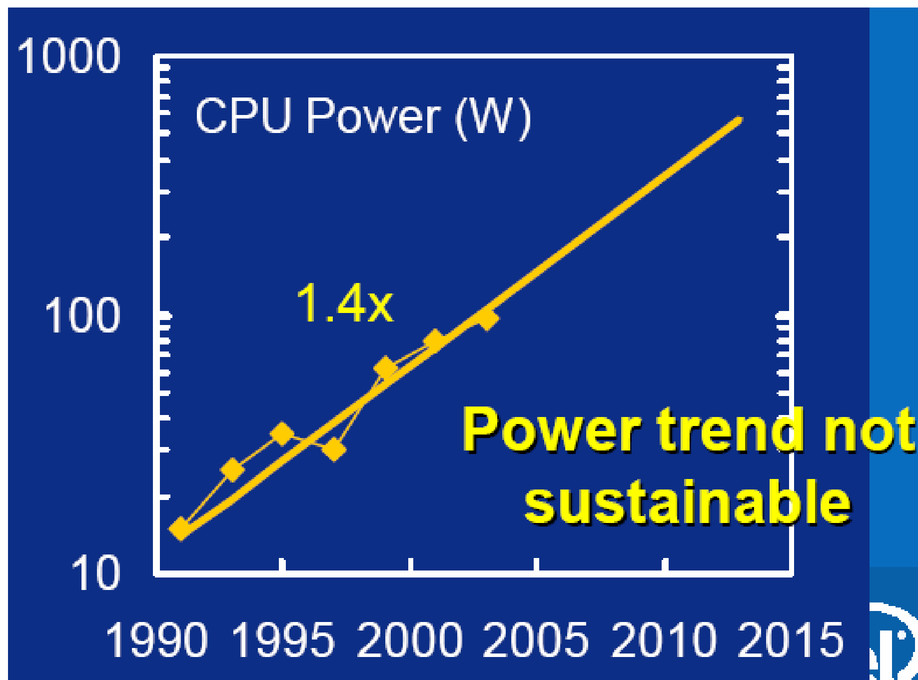


Figure 1.3 Power trend projection [4]

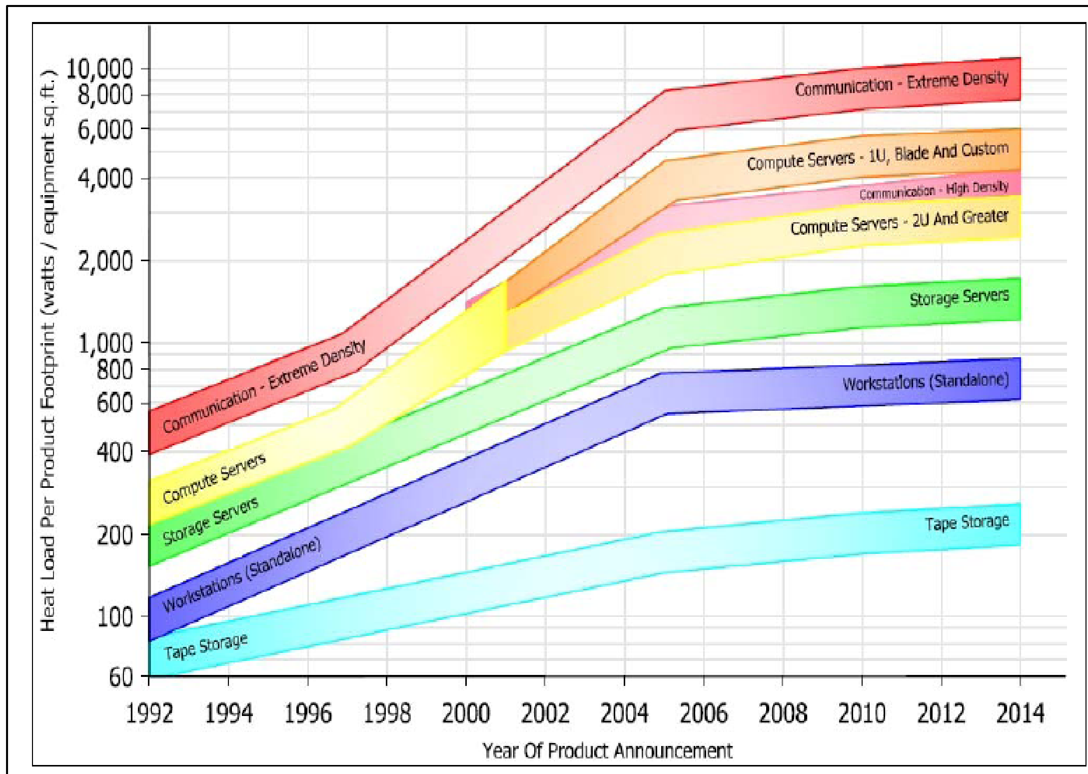


Figure 1.4 Heat density trend chart [5]

1.4 Thermal Management

The resistance to flow of electrical current through the leads, poly-silicon layers and transistors comprising a semiconductor device, results in significant internal heat generation within an operating electronic component. In the absence of some heat removal mechanisms the temperature of the components would rise and finally fail. So thermal management becomes a vital part in electronic packaging.

Despite the wide variety in size, power dissipation and sensitivity to temperature, the thermal management of all microelectronic components is motivated by similar concerns and common hierarchy of design constraints. The prevention of catastrophic failure – an immediate and total loss of electronic function and package integrity – is the primary and foremost aim of electronic thermal control [packaging book tumala] Thermal management in packaging may employ different modes of heat transfer at different levels [2].

1.4.1 Device Level Cooling

The chip package which houses and protects the chip forms the bottom of the packaging hierarchy or first level or device level. Thermal management at this level is primarily concerned with conducting heat form the chip to the package surface and then into the printed wiring board. At this packaging level, reduction of the thermal resistance between the silicon die and the outer surface of the package is the most effective way to lower the chip temperature. The thermal resistance can be brought down by number of ways. Improved thermal performance can be obtained by using die-attach adhesives with high thermal conductivity fill materials, thermal greases, phase change materials which soften at the operating temperature to better conform to the surface of the chip and metal plate heat spreaders. The cooling can be enhanced by attaching the package to heat sink, heat pipes etc., and cooling it by either by natural convection or forced convection [2].

1.4.2 Package Level Cooling

In this level, heat is removed both by conduction in PWB and by convection to the ambient air. Use of printed wiring board with thick, high conductivity power and ground planes or embedded heat pipes, provides improved thermal spreading at this level of packing. Heat sinks are often attached to the back of printed wiring board. There are many systems where convective cooling is not possible; instead, heat must be conducted to the edge of the PWB. Attachment of heat sink or a heat exchanger at this edge then serves to remove the accumulated heat [2].

1.4.3 System Level Cooling

At system level it involves the use active thermal control measures, such as air handling systems, refrigeration systems or heat pipes heat exchangers and pumps. Based on the application it is possible t cool the rack or module by relying on natural circulation of heated air [2].

PART 1

STATIC POWER CONSUMPTION – SILICON ON INSULATOR METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR

CHAPTER 2

INTRODUCTION

2.1 Background

IC technology is continuing to scale in size with an exponential increase in speed and density with time. Speed and area were the main design constrains in the early years. With the miniaturization, millions of transistors can fit into a single IC. But the high level of integration leads to rise in temperature due to power dissipation. A design with low power dissipation is desirable for reliability, portability, performance, cost and longer life. Due to the above factors, low power design has become one of the critical design parameters for VLSI (Very Large Scale Integration) systems.

The average power dissipation in digital CMOS circuits can be described by

$$P_{avg} = P_{dynamic} + P_{short\text{-}circuit} + P_{leakage} \qquad (1)$$

$P_{dynamic}$ is the dynamic power dissipation due to switching of transistors, $P_{short\text{-}circuit}$ is the short-circuit current power dissipation, when there is a direct current path from power supply down to ground, $P_{leakage}$ is the power dissipation due to leakage currents [6].

At present leakage current almost contributes to 50% of the average power [7]. This directly raises the temperature dissipated by the processors leading to electro migration and eventually leading to the failure of the chips. So leakage current has direct influence on the reliability of the chips.

2.2 Physical Layout

MOSFETs are metal-oxide semiconductor Field Effect Transistors, where the gate electrode has an oxidized surface. The oxidized layer insulates the gate electrode from the

channel. This oxidized layer acts as a dielectric reducing the current between the gate and channel, providing the MOSFET with large input impedance. A typical layout of a MOSFET is shown in Figure 2.1.

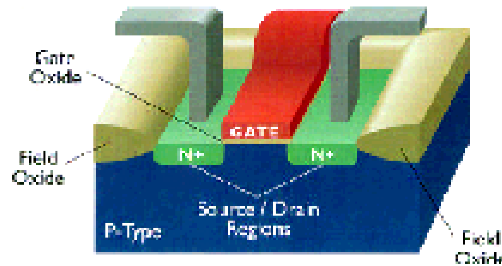


Figure 2.1 Typical layout of MOSFET

The Channel in a MOSFET can be either n-type or p-type semiconductor. The materials used for building a MOSFET are a science in itself. The usual semiconductor material of choice is silicon. Materials with better electrical properties than silicon such as GaAs are not used in MOSFETs since they do not form good gate oxides.

The material used for the gate electrode is poly-silicon placed over the channel, but separated from the channel by an oxidized metal layer. The material used for source and drain depends on the type of MOSFET desired. In a N-MOSFET both the source and drain contacts are made of n-type silicon on p-type substrate.

2.3 Reduction Of Leakage Current–Ultra Thin-Body Silicon-On-Insulator Mosfet

There are a number of methods to reduce leakage current. There are around five notable techniques followed to reduce leakage current. Among these reduction of silicon body thickness is considered for this study.

1. Use of gate dielectric materials such as crystalline praseodymium oxide or, silicon nitride with high permittivity (k). But this approach increases the physical thickness of the gate dielectric barrier.
2. Design of double gate SOI MOSFET
3. Turning off stacks of transistor which reduces effective width and thereby the leakage current
4. Use of Strained SOI- very thin layer of single-crystal silicon with built-in strain (stress) leading to accelerated electrons[8]
5. Reduction of silicon body thickness (Tsi) on SOI MOSFET

In this paper, the analysis of the simulation of reduction of leakage current by reducing the silicon body thickness in SOI MOSFET is presented.

2.4 Silicon On Insulator Mosfet Device

Silicon on Insulator (SOI) is a semiconductor fabrication technique developed by IBM that uses a pure silicon oxide layer on top of a pure silicon crystal [9]. SOI technology is being widely used for integrated circuits and microchips. SOI offers the ability to fabricate higher clocked CPUs, while lowering the power requirement of the high performance components [10]. Use of SOI based chip increases processing speed by about 15% and reduces power consumption by about 20% as compared to earlier CMOS based chips.

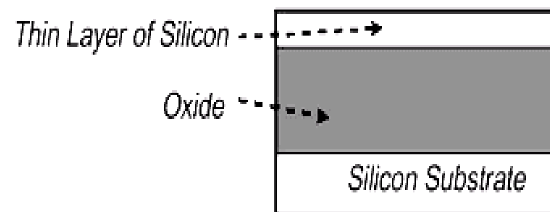


Figure 2.2 Typical SOI structure [11]

Figure 2.2 is a schematic representation of a typical SOI structure. It has a layered structure consisting of a thin layer of silicon (50 nm to 100 micrometer thickness) separated from the silicon substrate by an insulating layer of silicon oxide of about 80 nm thickness.

2.4.1 Function of SOI

Prior to SOI technology, the transistors were based on the metal oxide semiconductor (MOS) design. A MOS transistor can be considered as a capacitive circuit due to the capacitance between the impurity layer and silicon substrate. The MOS circuit must completely charge to full capacitance to activate its switching capability. The process of discharging and recharging the transistor requires long periods of time. The main objective of SOI design is to eliminate the capacitance, as a low capacitance circuit will allow faster transistor operation. Figure 2.3 is a schematic representation of a MOS circuit (left) as compared to an SOI circuit (right).

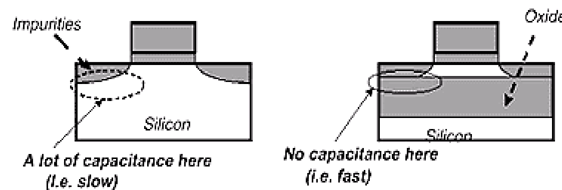


Figure 2.3 Comparison between Bulk MOSFET and SOI MOSFET [10]

In MOS design, a filament of metallic oxide is placed on a doped silicon surface. When a current is passed through the metallic conducting layer, the corresponding metal oxide path will allow current to pass through the impurity layers. Thus the MOS circuit can become either a conductor or an insulator with a simple change in the current. By combining both CMOS and MOS in CPU design, higher speeds can be achieved as it can operate with alternating voltage states simultaneously.

In spite of such a combined approach, it was realized that current CMOS fabrication techniques will not be able to scale efficiently below 0.1 micron size. Thus CMOS is not a viable technology for upcoming generations of processors [12].

The new development of SOI circuit differs from the generic CMOS by having its silicon junction above an electrical insulator. The SOI circuit's capacitance will be negligible since the silicon oxide provides an efficient insulation barrier. The insulator reduces the capacitance, implying that the transistor has less to charge up before completing a switch resulting in reduced switching time. SOI chips also reduce the soft error state, wherein the data corruption is caused by cosmic rays and natural radioactive background signals.

SOI chips are fabricated by two main techniques: SIMOX (Separation by Implantation of Oxygen into Silicon) which obtains a buried oxide layer through high field oxide implantation and waver bonding techniques that flip two wavers with oxidized surfaces on top of each other.

2.5 Ultra-Thin Body SOI Mosfet

The need for high speed circuits has resulted in the application of Silicon on Insulator MOSFET. But the conventional fully depleted SOI MOSFET has serious short channel effects compared to partially depleted SOI MOSFETs. Choosing ultra thin body structure can eliminate the current leakage path between the source and drain [13]. Ultra-thin body (UTB) SOI MOSFET devices have channel lengths of 10nm or lower as shown in Figure 2.4. In this device, gate current can be suppressed due to vertical electric field, which is the electric field near the bottom of the inversion layer

.

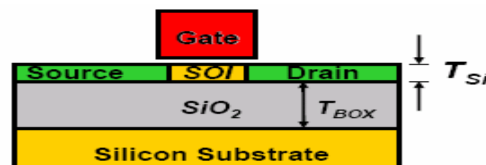


Figure 2.4 UTB SOI MOSFET

In Figure 2.5 the reduction in the slope of the potential in silicon channel, especially at the points away from the silicon/dielectric interface causes a reduction in the electric field. The

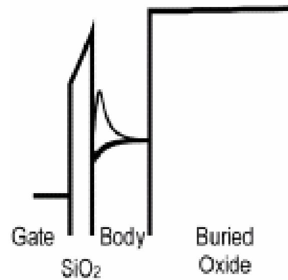


Figure 2.5 UTB SOI MOSFET Energy Band Diagrams [15]

reduction in electric field in turn reduces the depth of the potential well and expands the inversion charge distribution and lowers the state energies. Thus, the overall tunneling probability and the frequency of mobility of electrons towards silicon-dielectric interface are reduced. [14]

2.6 Simulation Of Ultra Thin Body SOI Mosfet

Simulations were carried out in 2-D device simulator MEDICI™ for both NMOS and PMOS. MEDICI™ is a simulation program that can be used to simulate behavior of MOS, bipolar transistors and other semiconductor devices [16]. It models the two-dimensional distributions of potential and carrier concentrations in a device. The program can be used to predict the electrical characteristics for bias conditions.

2.6.1 Basic Semiconductor Equations

The equations primarily used to describe semiconductor device behavior are of the following types [17]

The electrical behavior of semiconductor devices is governed by the Poisson's equation.

$$\varepsilon \nabla^2 \psi = -q\left(p - n + N_D^{+} - N_A^{-}\right) - \rho_s \qquad (2)$$

Ψ=electrostatic potential

ρ_s= surface charge density

n=electrons; p=holes

Poisson's equation gives the fundamental relationship between voltage and electric field distribution in a semiconductor.

Continuity equations for the electrons and holes also provide information about electrical behavior of a semiconductor device. The equation is based on the principle that current density in a semiconductor vary with time only due to generation-recombination processes, that is change in carrier density over time is equal to incoming flux of carrier and generation minus outgoing flux and recombination.

For electrons

$$\frac{\partial n}{\partial t} = \frac{1}{q}\vec{\nabla}\cdot\vec{J}_n - U_n = F_n(\psi, n, p) \qquad (3)$$

For holes

$$\frac{\partial p}{\partial t} = \frac{1}{q}\vec{\nabla}\cdot\vec{J}_p - U_p = F_p(\psi, n, p) \qquad (4)$$

2.6.2 Boltzmann Transport Theory

Electron and hole current densities can be written as a function of the carrier concentrations and the quasi Fermi potentials for the electrons and holes. Quasi Fermi potential is the difference between the Fermi potential after doping impurities and the intrinsic Fermi level, which is a measure of the least tightly held electrons within a solid.

For electrons

$$\vec{J}_n = -q\mu_n n \vec{\nabla} \cdot \varphi_n \qquad (5)$$

For holes

$$\vec{J}_p = -q\mu_p p \vec{\nabla} \cdot \varphi_p \qquad (6)$$

The current densities can also be written as a function of their drift and diffusion components as follows:

For electrons

$$\vec{J}_n = q\mu_n E_n n + qD_n \overset{\rho}{\nabla} \cdot n \qquad (7)$$

For holes

$$\vec{J}_p = q\mu_p E_p + qD_p \overset{\rho}{\nabla} \cdot p \qquad (8)$$

The simulation software couples the partial differential equations (1), (2) and (3) and solves them self-consistently. The current density term in those equations is found from the set of equations (5) and (6) or (7) and (8) as the doping concentrations are specified by the user and hence other terms on the right hand side of the equations are known.

CHAPTER 3

ANALYSIS AND RESULTS

3.1 Simulation

The structure of the NMOS device was constructed using the following input parameters.

- Length of gate (Lg) = 18nm
- Height of gate oxide = 1.5nm
- Buried oxide = 100nm
- Height of elevated source/drain= 100nm
- Uniform body doping concentration =3x1015cm^{-3}
- Source/drain doping concentration =1x1020cm^{-3}
- Gate doping concentration = 7x1019cm^{-3} (figure 3.1)

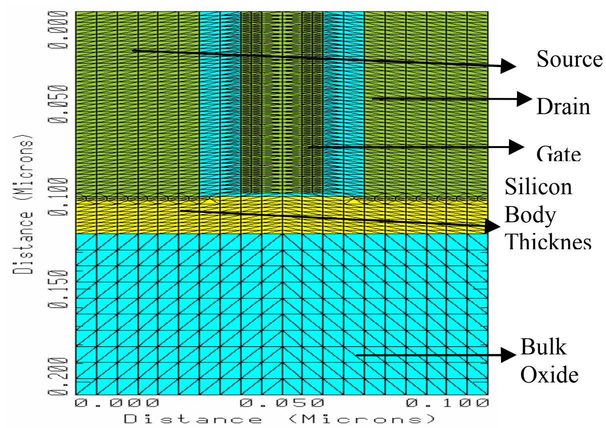


Figure 3.1 Structure of NMOS in Medici

A rectangular mesh solution was performed similar to figure 3.2. For planar devices like MOSFET, a rectangular grid is a good choice. The initial grid in MEDICI™ is created by specifying the structure in the most basic dimensions by using different input statements in the X and the Y-axes for multiple regions. Since the main grid is composed of several triangles, it is

unavoidable to create a grid without some of the triangles being obtuse in nature. Obtuse elements have two undesirable effects on a simulation:

1. Roughness is more apparent in the grid and 2-D plots such as contour plots become difficult to interpret.
2. Higher the number of obtuse elements, greater is the possibility of the solution to converge.

The equations described above were discretized in a simulation grid. The resulting set of algebraic equations were coupled and solved by nonlinear iteration method. Once it is set to run, the program generates a map of matrix. The incomplete LU conjugate gradient squared (ILUCGS) method was used to solve the matrix which results from device simulation. This is an iterative method and has a good convergence property.

The silicon body thickness was varied and its effect on leakage current was varied. The following Tsi (Silicon Body Thickness) were considered: 20nm, 11nm, 7nm and 5nm.

3.2 Results

The results from the Medici simulation for leakage current for NMOS circuit is in figure 3.3. Figure 3.3 shows the variation of the leakage current with drain voltage for varying thickness of silicon body (Tsi). The gate voltage was kept as zero for this simulation.

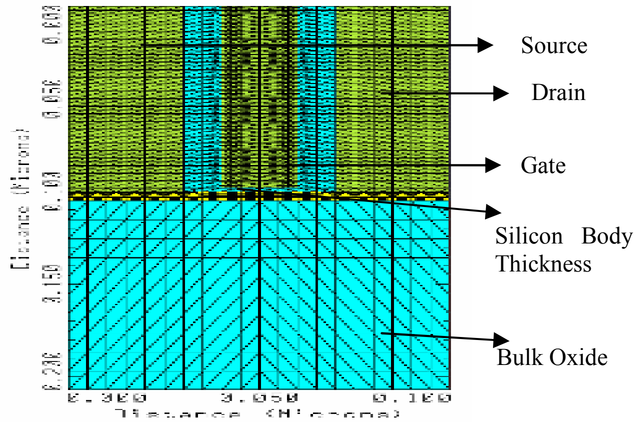


Figure 3.2 NMOS structure after meshing

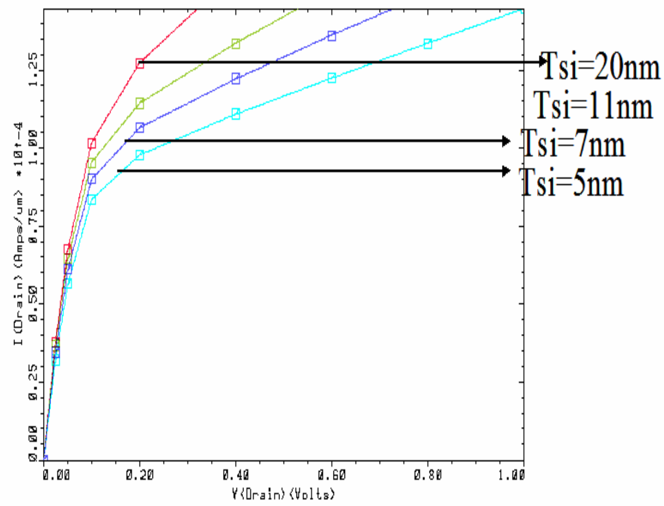


Figure 3.3 Variation of leakage current with drain voltage in NMOS

Table 3.1 shows the leakage current for silicon body thickness 7nm and 5nm for different drain voltages. It can be seen that the leakage current decreases as the body thickness decreases. The variation in percentage reduction in leakage current as a function of drain voltage is shown in the form of a bar graph in figure 3.4.

Table 3.1 Percentage reduction in leakage current as a function of drain voltage

Drain	Current (7nm) (10^{-4} A)	Current (7nm) (10^{-4} A)	% Reduction in Leakage Current
0.2	1.08	0.95	12
0.4	1.25	1.11	11.2
0.6	1.37	1.23	10.21
0.8	1.48	1.34	9.4

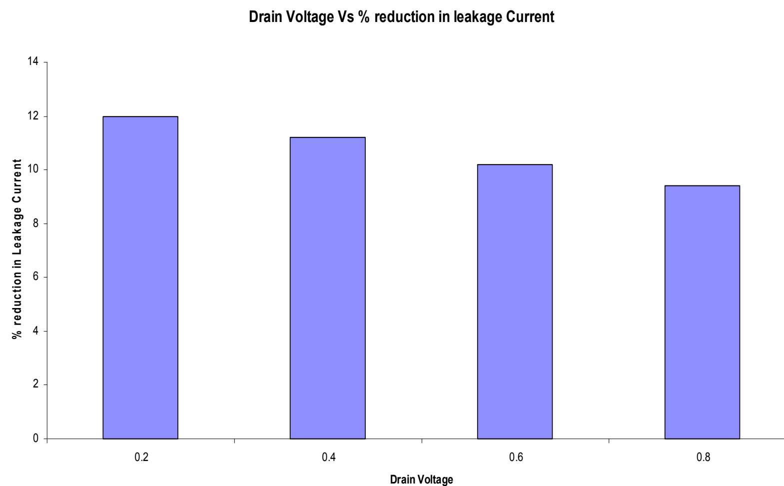


Figure 3.4 Variation in percentage reduction in leakage current as a function of drain voltage

The reduction in leakage current with the reduction in silicon layer thickness is an expected result. As the silicon body thickness is reduced, the electric field far way from the silicon/dielectric interface is reduced. The reduction in electric field leads to broadening of the inversion charge distribution leading to a decrease in the leakage current. Thus, by reducing the thickness of silicon body from 7nm to 5 nm, the leakage current can be reduced by about 10 to 12% as shown in figure 3.4. However, if the body thickness is reduced below 5 nm, the leakage

current increases, as the carrier lifetime is reduced owing to the charges being near the gate oxide interface.

Figure 3.5 shows the results of the variation of the leakage current with drain voltage for different silicon body thickness in PMOS. The variation in leakage current is similar to the NMOS case.

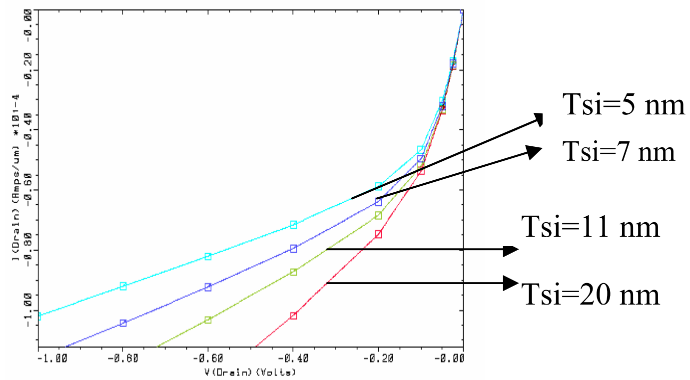


Figure 3.5 Variation of the leakage current with drain voltage in PMOS

CHAPTER 4

FUTURE WORK

An ultra thin SOI MOSFET was simulated using MEDICI^{TM}, device simulation software for understanding the reduction of leakage current for a particular gate length. It was determined that the leakage current decreases by 10-15% as the silicon body thickness reduces by 2 nm.

One of the currently successful methods to reduce the leakage current is to use strained silicon substrate. In the strained SOI technique, a very thin layer of single-crystal silicon with built-in strain is used. The controlled strain opens the lattice structure, leading to higher acceleration of electrons, thereby reducing the leakage current. It is worthwhile to analyze the strained SOI devices, using a combination of MEDICI and ANSYS simulation tools.

Silicon nitride and other dielectric materials are being developed as substrates for improving the performance of SOI MOSFET for high temperature and high speed operations. It will be useful to evaluate the effect of the different substrate materials on the leakage current. Further we can use strained silicon or high K dielectric material as gate material and study the effect of leakage current.

PART 2

MULTI-OBJECTIVE OPTIMIZATION ENTAILING COMPUTER ARCHITECTURE AND THERMAL DESIGN FOR NON-UNIFORMLY POWERED MICROPROCESSORS

CHAPTER 5

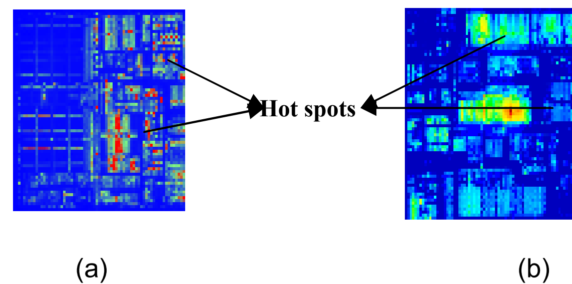
INTRODUCTION

In recent years, power density in microprocessors has doubled every three years [18, 19], and this rate is expected to increase within one to two generations as feature sizes and frequencies scale faster than operating voltages [20]. As the total power increases, the power density of the silicon chip is increasing as well. In order to keep transistors within their allowed operating temperature range, the generated heat has to be dissipated from its source in a cost-effective manner. These constraints limit the processor's peak power consumption. Peak power consumption limits apply both to desktops and mobile computers. Increased power dissipation results in higher operating temperature, more expensive cooling mechanisms and reduced reliability.

The integration level and the clock speed of high-performance microprocessors have increased so rapidly that the average power density of the advanced microprocessor chips is now more than 10 W/cm^2. Many chips are now running at peak power of >30 W even at V_{dd} =3.3V. Furthermore, the average power density is expected to increase in scaling.

Power-aware design alone has failed to solve thermal management problem, requiring temperature-aware design at all system levels, including the processor architecture. Many low power techniques do not reduce power density in hot spots with having little impact on operating temperature. Temperature-aware design will make use of power-management techniques. In sub-100nm technologies, temperature plays an important role in performance and reliability. Localized heating occurs much faster than chip-wide heating; since power dissipation is spatially non-uniform across the chip as shown in figure 5.1, this leads to "hot spots" and spatial

gradients that can cause timing errors or even physical damage. This means that power-management techniques, in order to be used for thermal management, must directly target the spatial and temporal behavior of operating temperature. Temperature-specific design techniques to date have mostly focused on the thermal package (heat sink, fan, etc.). If the package is designed for worst-case power dissipation, they must be designed for the most severe hot spot that could arise, which is prohibitively expensive. To reduce packaging cost without unnecessarily limiting performance, it has been suggested that the package should be designed for the worst typical application [21, 22,23]. It is therefore very important to create thermal compact model depends on architecture, power maps and floor plans [21] to solve thermal management problem.



(a) (b)

Figure 5.1 Hot spots as a effect of Non uniform power (a) Intel Pentium ® III Processor and (b) Intel Itanium ® Processor [24]

5.1 Background & Motivation

Non uniform power phenomenon [25] was reported in the design of Pentium® III XeonTM processor for 4-way and 8-way server systems where significantly large L2 cache was integrated to the silicon design. Previous work has been done in understanding the thermal solutions for the non-uniform power distribution within the silicon die. Some of the previous work includes Goh et al. [26] using genetic algorithm approach, Getkin et al. [27] using simplified fin

modeling approach, Sikka et al. [28] using analytical temperature distribution method, June et al. [24] using cap-integral standoffs, Yu et al. [30] using fast placement dependent full chip thermal simulations .

Skadron and Stan [21, 22] developed a Hotspot model based on equivalent circuit of thermal resistances and capacitances that correspond to micro architecture blocks and essential aspects of thermal package**.** This approach is based on modeling thermal behavior of the microprocessor die and its package as a circuit of thermal resistances and capacitances that correspond to functional blocks at the architecture level. Wei et al [31] mathematically estimated the active power of functional units in modern microprocessors. The method leverages the phasic behavior in power consumption of programs, and captures as many power phases as possible to form a linear system equation such that functional unit power can be solved. Hamid [23] presented a multidisciplinary design and optimization methodologies in electronic packaging which includes integrated multidisciplinary CAD environment and automated design and optimization techniques. Skadron [32] in his paper “Temperature aware – GPU design” argues for a runtime approach to cooling, reducing the need for bulky and expensive thermal packages and fans. Skadron et el [21, 22] shows that there is significant peak temperature reduction potential in managing lateral heat spreading through floorplanning. It was also suggested that potential warrants considerations of the temperature-performance trade-off early in the design stage at the micro architectural level using floorplanning. It is also very important to develop a best known method to develop a compact model based on both thermal and device clock performance for a non-uniformly powered microprocessor.

CHAPTER 6

DESIGN AND MODELING

6.1 Description of a Package Assembly

A schematic diagram of a typical package shown in figure 6.1 is used in this research. It has a heat sink of 64 x 64 x 6.35 mm attached to the spreader of 31 x 31 x 1.8 mm to the silicon die with the help of Thermal Interface Material (TIM I) and TIM II with a thickness of 0.025 mm as shown in table 6.1. The various power maps used in this paper are provided by Intel corp.

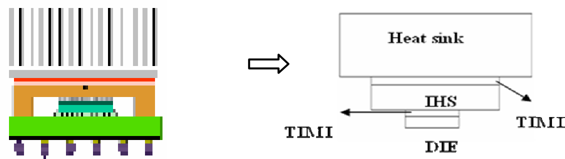


Figure 6.1 Model of a Flip Chip Package

Table 6.1 Dimensions and material properties data of flip chip package

Type	Dimensions (mm)	Thickness (mm)	Conductivity (W/m°K)
Die	10.17 x 10.62	0.75	120
TIM I (Indium)	10.17 x 10.62	0.025	50
HIS	31 x 31	1.8	390
TIM II(Thermal Grease)	31 x 31	0.075-0.125	3.5
Heat sink	64 x 64	6.35	390

6.2 Design Approach & Modeling Methodology

In this study, numerical model is developed that utilizes multi-objective optimization involves redistribution of functional blocks to improve device performance and minimize on-die temperature. The attachment consists of base of heat sink, TIM I and TIM II and heat spreader with Pentium IV die architecture is used to develop the numerical model. Current authors have developed a numerical model for thermal based optimization of non-uniformly powered microprocessors and subsequently developed design guidelines for this numerical model for [33, 34]. In this paper previously developed design guideline is used as a base line case. This baseline case is embedded into silicon floor plan to developed compact model satisfying both electrical and thermal performance. Non-uniformity is seen in Pentium processor is the case considered in this study for a more universal problem.   As shown in figure 6.2 (a) floor plan of Pentium IV architecture is the case considered for thermal performance study.

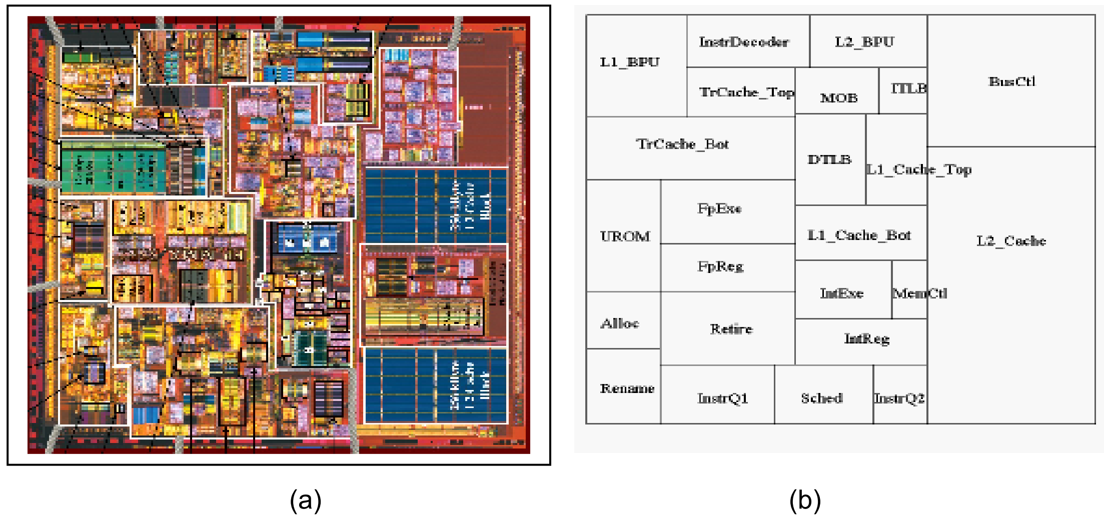
Constraint for the electrical optimization is the total wiring length for a particular configuration of functional blocks. Once positioning of the functional blocks is carried out, thermal optimization of these non-uniformly powered functional blocks is carried out to minimize on-die temperature. After this, both the parameters considered for optimizations is studied and recommendations are provided for an architecture that optimizes based on both minimization of the total wiring length and minimization of on-die temperature.

6.3 Pentium IV Architecture

Figure 7 (a) shows Pentium IV architecture [36]. It consists of the core and Cache of the microprocessor. The architecture shows the different functional blocks of the typical non-uniformly powered microprocessor. Figure 6.2 (b) shows a floor plan layout of the same architecture. These functional blocks have specific arrangements on the die according to the

transformation of the information between the blocks. The proximity of certain block to another depends on the function it does and the criticality of the information processed by it.

There are 24 functional blocks in this corresponding floor plan for Pentium IV architecture. In this study functional blocks with similar functionality are clubbed together to come up with total of 16 functional blocks as shown in figure 6.3.



(a) (b)

Figure 6.2 Pentium IV floor plan (a) Pictorial view (b) Functional block distribution [36]

15	16	13	12	3	3
14	14	10	11	3	3
6	7	9	9	2	2
6	7	5	8	2	2
1	4	5	5	2	2
1	1	1	1	2	2

Figure 6.3 Baseline case of the Pentium IV architecture - modified floor plan

Geometry is created using given dimensions for Die architecture as shown in figure 6.3 which is a Pentium IV processor of size 10 x 10 including 16 functional blocks, Spreader, Heat sink and TIMs. Die is divided into various functional blocks as shown in figure 6.3. Pro-E is used to model the given die architecture. In the Pro-E model, the each functional block may contain one or few blocks of the power map depending on the size of the functional block. Assembly is created at the end for various parts of the die (i. e. individual functional block is a part). Then the flip chip assembly is exported to Ansys Workbench.

Parameters such as thicknesses of TIM I and TIM II, thermal conductivities of TIMs and convective transfer coefficient are calculated to satisfy the given package conditions. All the material properties are applied as per the material property data table 6.1. Convection co-efficient (h) of 1200 W/m^2 °C is used on the top of package for the analysis. This (h) is an effective heat transfer coefficient applied per unit area of the heat sink base (equal to the fin average h times the fin/base area ratio). A steady state thermal analysis is carried out to calculate the maximum junction temperature (Tj) for given power distribution. Mesh sensitivity analysis is carried out with temperature varies in the range of +/- 1 ° C; coarse meshing is used for the analysis.

Once the baseline case is analyzed, different scenarios are arrived at based on the previous design guidelines [34]. Based on the following guidelines a DOE with 24 cases is obtained.

- Interchanging locations of highest power with lowest power
- Low powers are distributed over periphery as compared to high powers
- Groups of high powers, are located near the center

The maximum junction temperature (Tj) for these 24 cases is calculated using numerical simulation. The tools used for simulation is Ansys Workbench. Once the thermal simulation is

done the total wiring length is calculated using half perimeter wire length method i.e., the wire length between two blocks is given by

Wire Length = $|x1 - x2| + |y1-y2|$; Where $x1; y1; x2; y2$ are the coordinates of their centers [38]

Total wiring length is calculated using the above formula. The two parameters considered for study maximum junction temperature (Tj) and total wiring length are analyzed and recommendations are provided.

CHAPTER 7

RESULTS AND DISCUSSIONS

7.1 Pentium IV Architecture

Figure 7.1 shows the baseline case for a given Pentium IV architecture. It gives a maximum junction temperature (Tj) of 138 º C. After changing the locations of the functional blocks the junction temperature (Tj) decreases to 122.21 º C as shown in figure 7.2. This shows that changing the functional block position has significant effect on the maximum junction temperature.

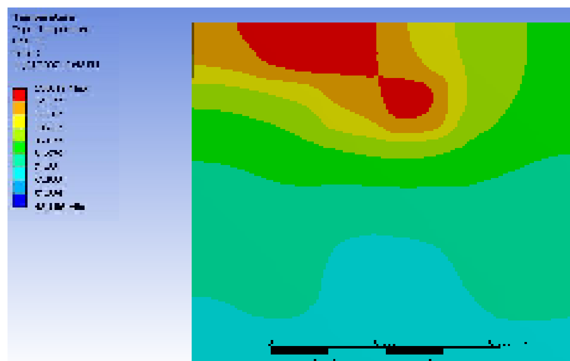


Figure 7.1 Temperature contour for baseline case

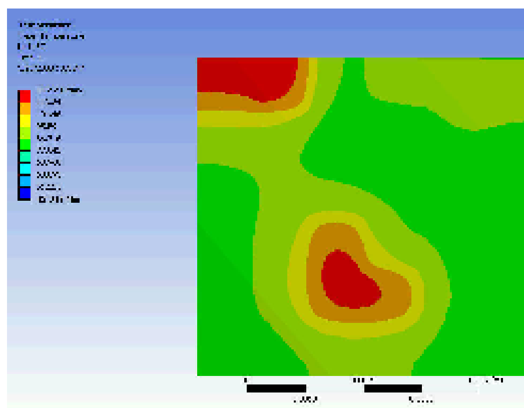


Figure 7.2 Temperature contour for the best case -18

Table 7.1 shows the functional block positions of few important cases with their Tj max and the total wiring length.

Table 7.1 Functional block position with Tj max and total wiring length

	Functional Unit	Power(W)	BL case	5	6	21	7	19	18
1	Allocation+Rename+Instruction	7	1	1	1	1	1	1	1
2	L2 Cache	12.9	2	2	2	2	2	2	2
3	Bus Control	11	3	3	3	3	3	5,8	3
4	Retire	2.5	4	4	4	4	4	4	4
5	Int Register + Integer Execution	0.5	5	5	5	5	5	3	10,11,13
6	Urom	3	6	15,16	6	6	12,13	6	6
7	Fp register + Fp execution	3.6	7	7	15,16	7	7	7	7
8	Memory Control	0.5	8	8	8	13	8	3	8
9	L1 cache	2.6	9	9	9	9	9	9	9
10	Dtlb	6.1	10	10	10	10	10	10	5
11	MOB	13.5	11	11	11	11	11	11	5
12	IITB	3.5	12	12	12	12	6	12	12
13	L2 Bpu	7.7	13	13	13	8	6	13	5
14	Tr Cache	2.5	14	14	14	14	14	14	14
15	L1 Bpu	6.8	15	6	7	15	15	15	15
16	Instruction decoder	10	16	6	7	16	16	16	16
		Maximum	**138.47**	**129.85**	**131.15**	**128.5**	**130.76**	**137.8**	**122.2**
		Minimum	**42.186**	**42.233**	**42.251**	**42.245**	**42.19**	**42.21**	**42.35**
	Total Wiring Length (mm)		**47.487**	**48.32**	**46.65**	**47.487**	**49.985**	**46.65**	**47.48**

CHAPTER 8

CONCLUSION

8.1 Summary and Future Work

The development of numerical model using multi-objective optimization for non-uniformly powered microprocessors was carried out for Pentium IV architecture. Baseline case shows the junction temperature (Tj) of 138.47°C. Table 8.1 shows the summary of results for the critical five cases with their Tj max and total wiring length values.

Table 8.1 Summary of Results

Case	**Maximum Junction Temperature (°C)**	**Total Wiring Length (mm)**	**% Change in Tj**	**% change in WL**
Base Line	138.47	47.487	-	-
5	129.85	48.32	**6.22**	**-1.75416**
6	131.15	**46.65**	**5.28**	**1.762588**
7	130.76	49.985	**5.56**	**-5.26039**
18	**122.2**	47.484	**11.74**	**0.006318**
21	128.5	47.49	**7.2**	**-0.00632**

To sum up the

- After redistribution of functional blocks the junction temperature has come down to 122.22°C with the same wiring length as the base line case
- But for the case with minimum wiring length of 46.65mm the Tj is 131.15 °C
- So the optimum case is application dependent

– From these results it can be seen that there is a trade off between the two variables considered – the junction temperature & the total wiring length

This is a parametric study and the results show that there room for proper optimization. This study can be extended to multi-core system which can also include various issues such as core hopping, leakage current, robust way of calculating the wiring length, etc., to further improve the optimization. A proper optimization code with objective function based on the application will give us the optimum design.

PART 3

RACK LEVEL COOLING

CHAPTER 9

INTRODUCTION

9.1 Why CFD

CommScope integrated cabinets provide environmentally secure enclosures for all types of electronic equipment. The cabinets optimize equipment density, heat transfer and dissipation, power reserve, environmental protection and ease of installation [40]. These types of enclosures, with their multiple equipment configurations, demand thermal performance tests and analysis.

Computational Fluid Dynamics allows quick analysis for multiple test configurations and design of experiments to be analyzed. Without a computational approach, time-consuming prototype testing must be performed. Moreover, the permutations of equipment configurations can quickly grow, leading to an extended cycle of prototype builds, testing, and test configuring. With the ever increasing time-to-market requirements, testing a large enclosure with multiple configurations can be accelerated through simulation. Such simulations are very effective for studying design alternatives and exploring viable what-if scenarios. To insure reliability and accuracy of the simulation model, high levels of detail are necessary in the regions of critical components. At the same time, non-critical areas can have reduced detail and lower mesh counts, if modeled properly.

9.2 Cabinet Description

The RBA48 cabinet considered here is amongst the mid-size cabinets of the CommScope Integrated Cabinets product line. The RBA48 cabinet dimensions measures approximately 30 inches wide, 48 inches high and 35 inches deep.

The equipment inside the cabinet is a function of application to be served. The RBA48 cabinet discussed in this study consists of the customer telecommunications, rectifier shelf, HX and inner/outer loop fan trays, TEC modules. The customer shelf itself consists of circuit cards, all of which dissipate heat into the system. Similarly, the rectifier has three rectifier modules, each rectifier module having complex electronic circuitry and two fans for cooling. The customer shelf and rectifier dissipate the majority of heat in the cabinet.

The cabinet has two fan assemblies:

1. Bay fan tray (Inner loop, 3 fans)
2. HX fan tray (Outer loop, 2 fans)

The bay fan tray creates the inner loop air flow, i.e. pulls in internal air from the bottom of the customer shelf and exhausts the hot air to the intake of the HX. So the air enters the inner loop of the HX from the top and after it has undergone cooling, is again rejected to shelf inlet from the HX exhaust. On the outer loop side, the HX fans pull ambient air from the bottom side of the HX and the flow is from bottom to top. While air is flowing through both the respective loops, heat transfer takes place following the counter-flow HX principle cooling the inner loop air. The warmer outer loop air is exhausted to the atmosphere. This cycle continues and the cooling medium (air in this case) never mixes.

Other then the above mentioned equipment, the RBA48 cabinet includes the batteries. Heater strips are used to simulate solar load. Figure 9.1 depicts a CFD model of various modules and their respective positions within the cabinet. So with this mix of components in the system, all these modules getting together in a system, it becomes a difficult task to bring about the right balance between simplification, accuracy, and shorter computation time. These components inside the system can be arranged in different configurations to get better performance.

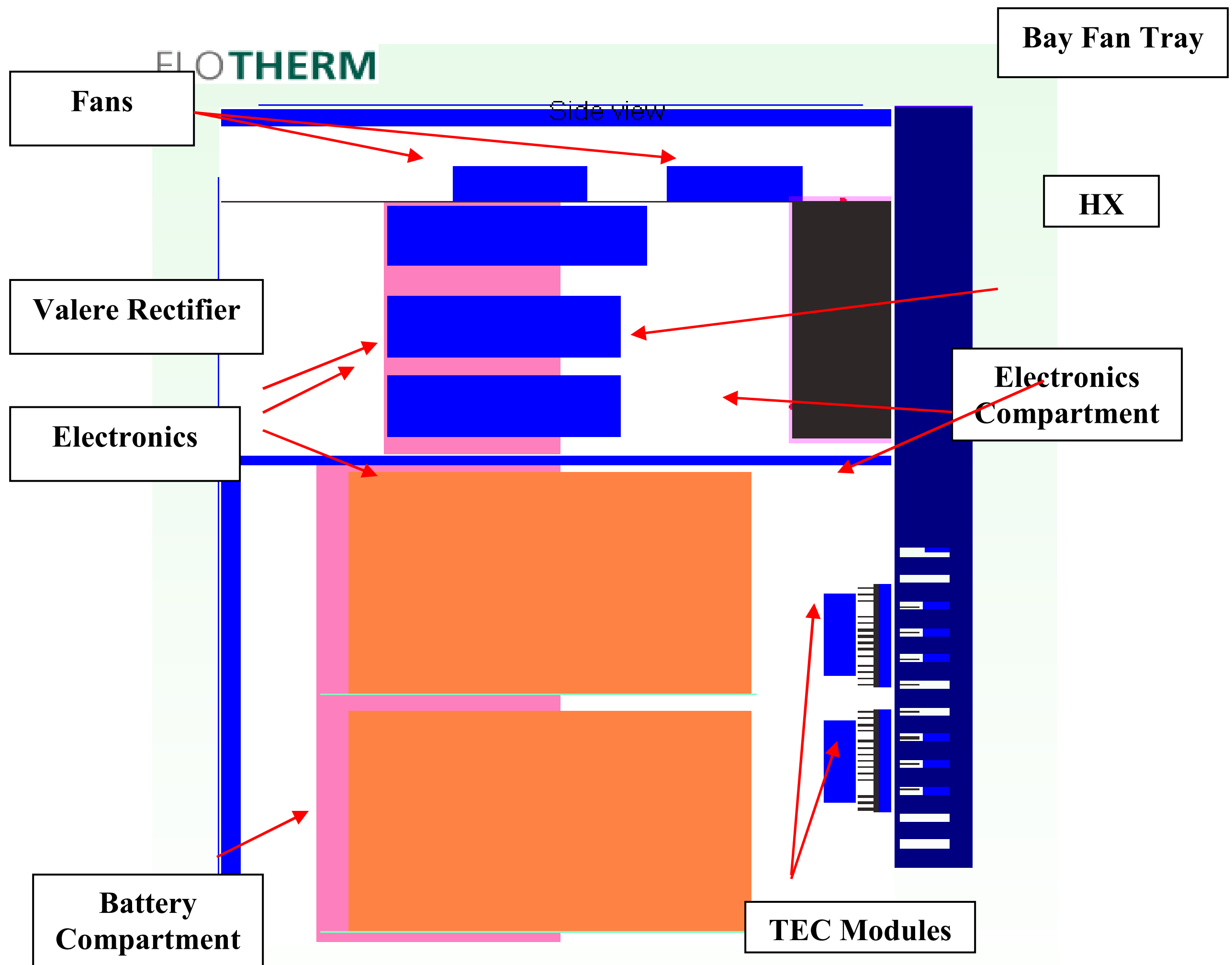


Figure 9.1 CFD model of the cabinet – Side View

CHAPTER 10

MODELING METHODOLOGY

Given the size of the cabinet with the complexity of equipment, a system level analysis would require a fairly coarse mesh to keep the grid cells within manageable levels. The model meshing can be coarsened to reduce solution time; however, coarse meshing can compromise model accuracy. In order to reliably reduce mesh counts and solution time a modeling methodology depicted in figure 10.1 comes in handy developing a system level compact model, courtesy Flomerics.

As depicted in figure 10.1, detailed models of modules used in the system level model are picked one by one. Our objective here is to capture the thermal and fluid flow data for each module, which can be accomplished in two ways:

10.1 Computational Analysis

In this method, a CFD tool such as FLOTHERM is used to collect the data. The detailed model of each module is created and placed inside a simulated wind tunnel created in FLOTHERM. This technique is frequently used as a method for flow and heat transfer characterization of thermal systems [41]. Flow corresponding to actual conditions is applied to capture the pressure drop, flow rate, and temperature values across the module. The detailed module is simplified inside the same simulated wind tunnel until we get data similar to one achieved with a detailed model. A compact model thus obtained, can be used in development of a system level model.

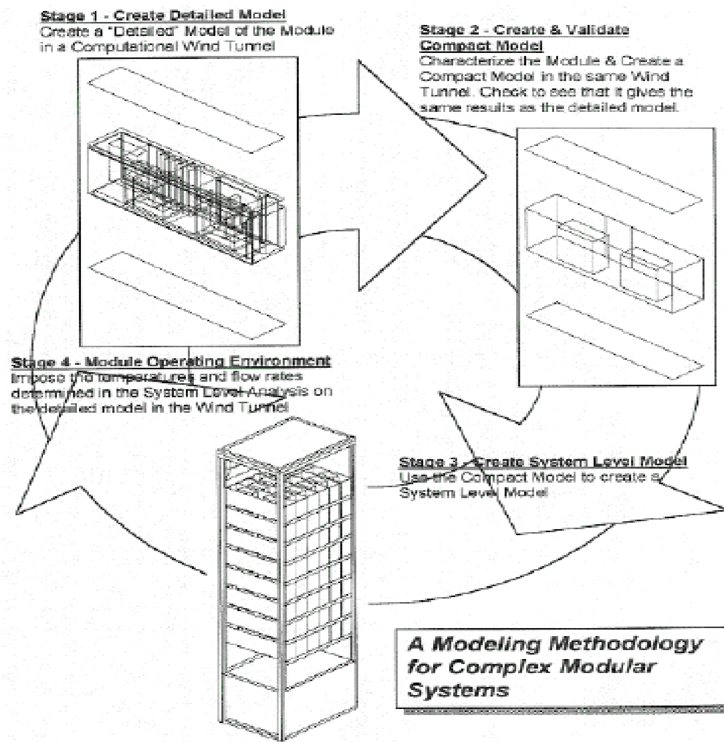


Figure 10.1 Modeling Methodology [42]

10.2 Experimental

Actual thermal components are physically tested in a wind tunnel to determine pressure drop and temperature values across the system. The data collected this way is more reliable and more precisely matches with actual working conditions. Once we have the P-Q and thermal resistance curves, these values can be added to the corresponding compact model of the given component inside the system level model [43].

CHAPTER 11

RESULTS AND DISCUSSION

11.1 Selection Of HX Fans – Outer Loop Fans

In the HX fans tray for the outer loop there are two fans placed in parallel to the cabinet wall. The following three fans were considered for the study

Fan Type	Thickness of the fan	Rated Flow Rate - cfm	Flow Type
Maltese	2.165”	307	Swirl
Patriot	2”	240	Swirl
Major XT	1.5”	203	Swirl

Taking one fan at a time and keeping all the other parameters constant the fans were simulated for their performance. For each fan two models were tested

- With a partition in between the fans in the door, shown in figure 11.1
- With out the partition in between the fans

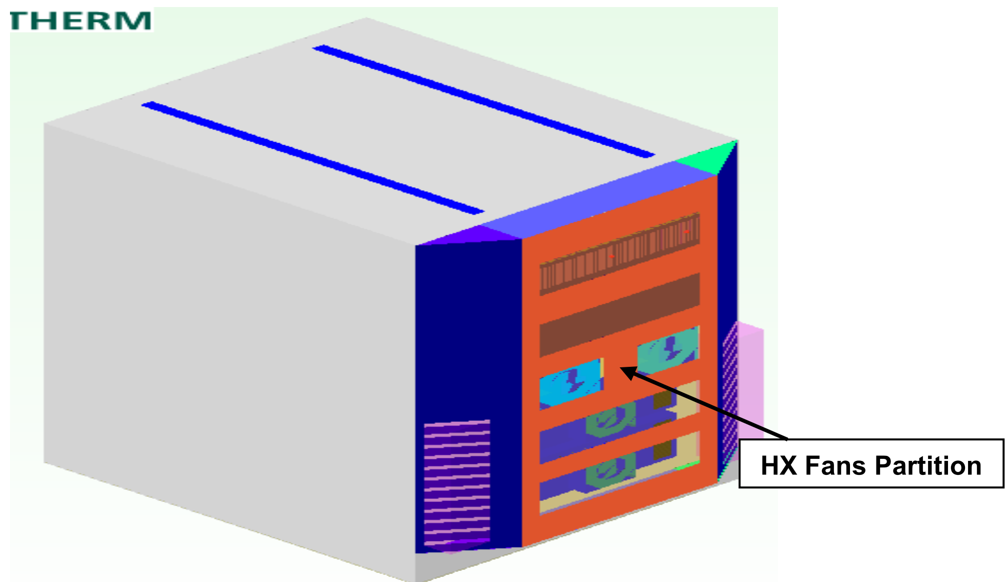


Figure 11.1 Flotherm Model with HX Fans Partition

Having different fans in the outer loop changes the flow across that loop thereby the heat transfer. Monitor points were placed in the inlet and exit of the electronics to record the temperature. The recorded temperatures are shown below in table 11.1

Table 11.1 HX Fans Performance

Case	**Maltese**	**Maltese with partition**	**Patriot**	**Patriot with partition**	**Major XT**	**Major XT with partition**
Electronics 1	84.38	**80.05**	84.59	80.17	87.74	81.11
Electronics 2	72.89	**69.09**	74.01	69.54	76.27	70.51

All temperature in degrees

11.2 Optimum Door Opening Analysis

The two TEC modules which are on the bottom part of the door remove heat from the battery compartment. To maximize the heat transfer the TEC module has heat sinks attached to it. Fans blow air in the heat sinks and in turn cool it. The air coming for the fans has to go out through the holes provided in the door as shown in figure 11.2. The free area ration considered in this case is 33% as depicts the real scenario. Holes are provided symmetrically on the door sides so to the net flow rate will be the cumulative of both the opening. The following DOE table 11.2 shows the cases considered for analysis and results.

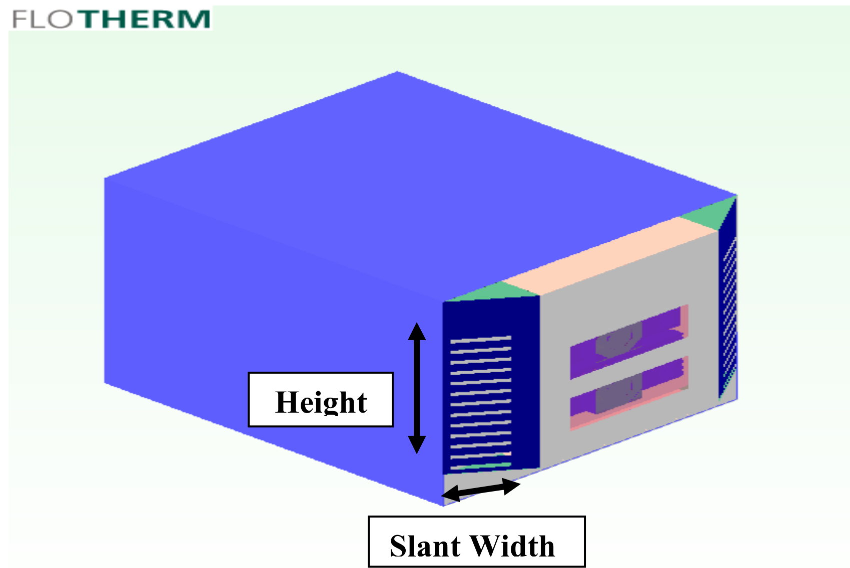


Figure 11.2 Half model for flow analysis

Table 11.2 DOE considered for Optimum Door Opening Analysis

Slant Width	Height	Flow Rate (cfm)		
		Left Region	Right Region	Cumulative
4.5"	13.2"	61.7	66	127.7
	15.2"	68	68	136
	17.2"	72	70	142
	19.2"	72	70	142
3.5"	13.2"	57	53	110
	15.2"	63	60	123
	17.2"	66	63	129
	19.2"	68	63	131
2.5"	13.2"	42.5	42	84.5
	15.2"	53	51	104
	17.2"	54	53	107
	19.2"	54	53	107

It's clear from the graph figure 11.3 the flow remains constant after it crosses 17.2" in height. Also increasing trend in flow rate is observed as the width of the hole increases.

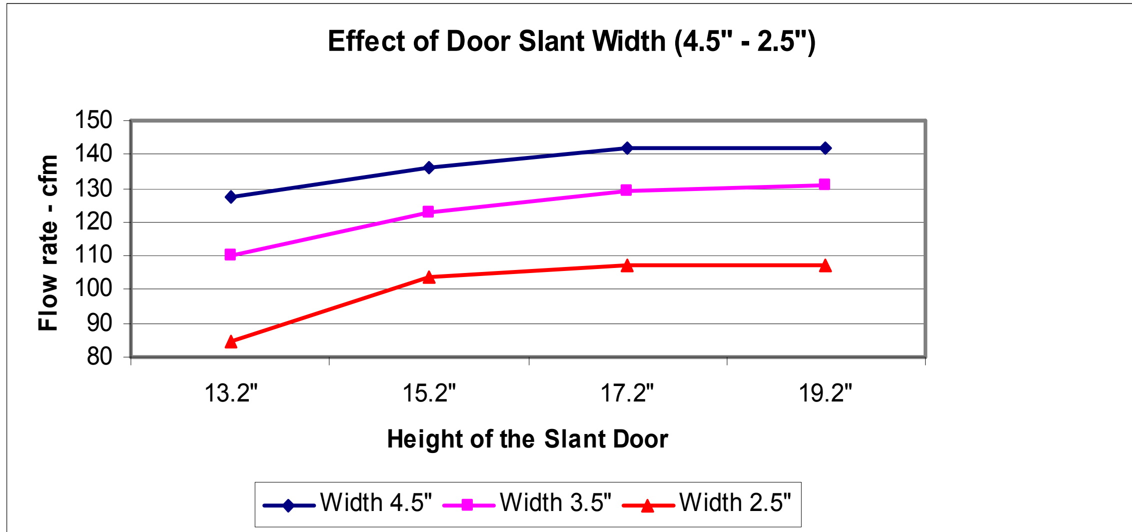


Figure 11.3 Graph for 33% Open Condition

Table 11.3 Flow Analysis for Particular Case

Width	Length	Flow Rate (cfm)		
		Left Region	Right Region	Cumulative
4.5"	**13.2"**	61.7	66	127.7
	15.2"	68	68	136
	17.2"	**72**	**70**	**142**
	18.2"	72	70	142
	19.2"	72	70	142

From the figure 11.3 its clear that hole dimensions with 4.5" X 17.2" gives maximum flow. To find the optimum dimensions this particular case is selected and further analysis is done. The results of which are shown in table 11.3 and displayed figure 11.4.

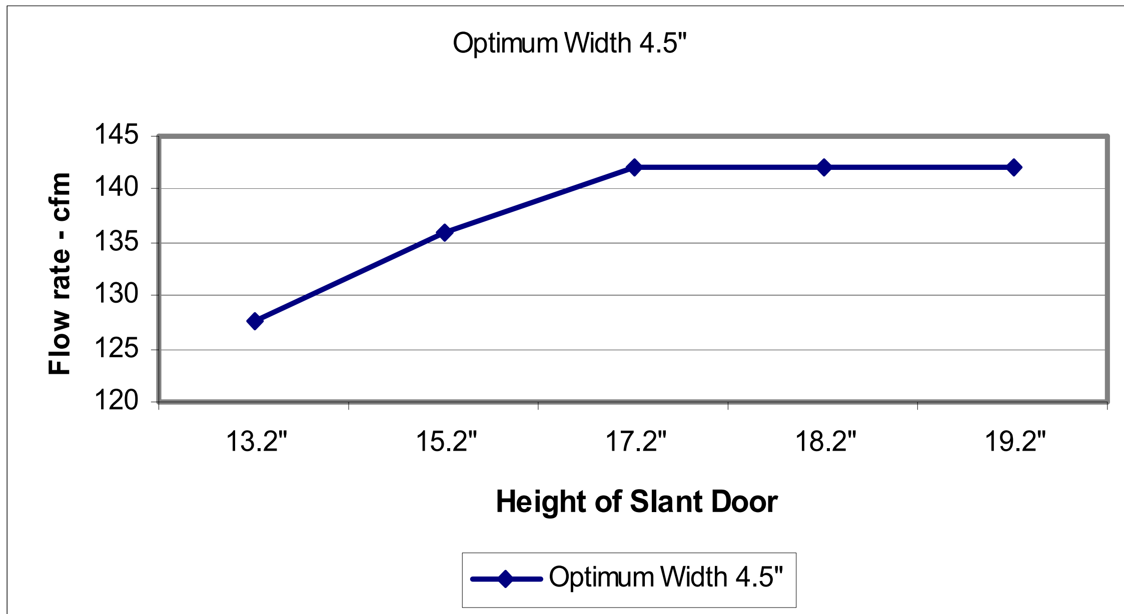


Figure 11.4 Graph displaying optimum condition (Hole Opening)

11.3 Bay Fan Tray – Optimum Fan Position Location

The bay fan tray is on the top of the electronics compartment. It has fans which helps the circulation of air in the inner loop. It pulls air from the inner loop exhaust of HX and cools the electronics and valere rectifier and forces it to the inner loop inlet of HX for cooling. The fan in the bay fan tray has an operating temperature of 72^0C so the placement of fans should be such way that it should come across any temperature greater than 72^0C.

Thermal load of 200W for electronics and 400W for rectifier are applied for the analysis. Apart form these solar load of $70W/ft^2$ is applied on three sides of the cabinet. The absorptivity factor considered for solar load calculation is 0.5 as the cabinet being painted in light color. Figure 11.5 shows the layout of electronics.

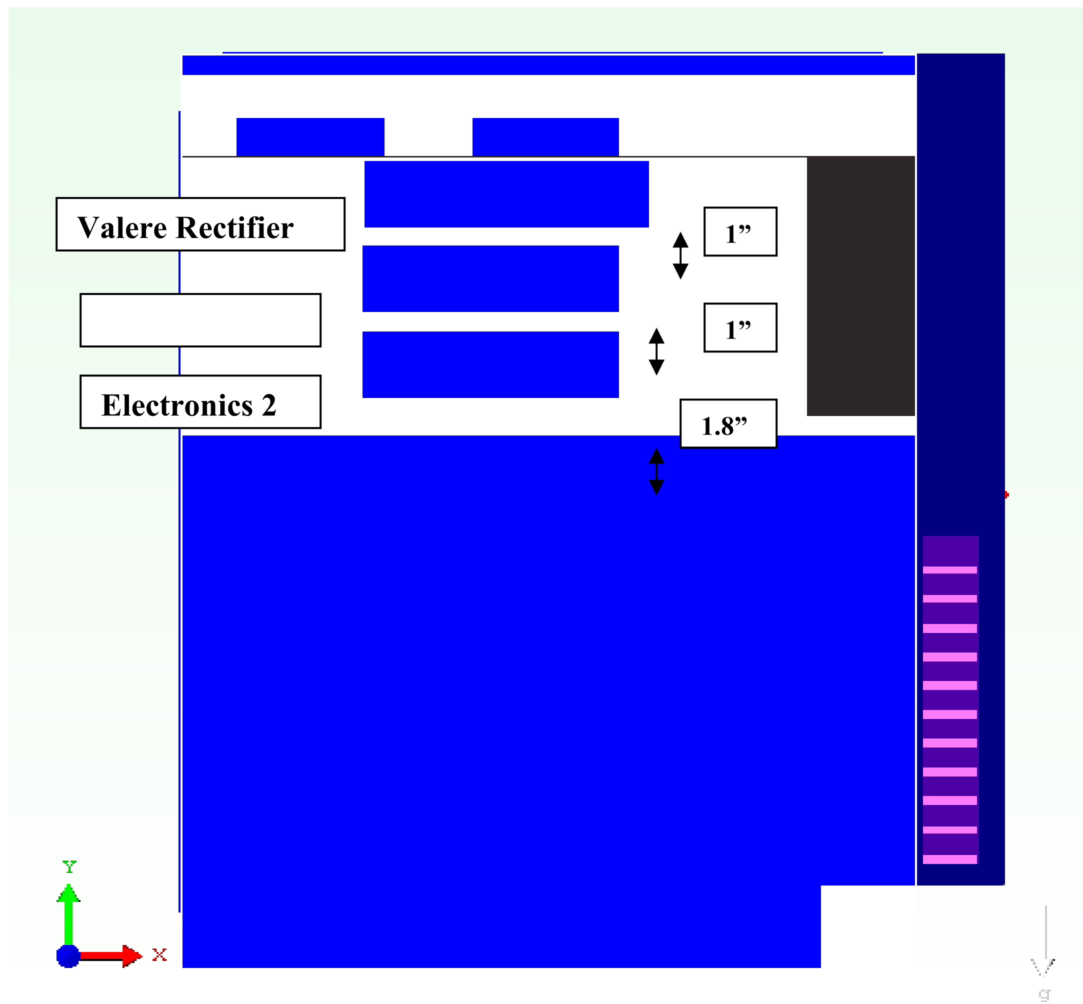
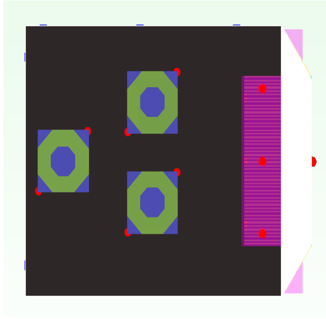


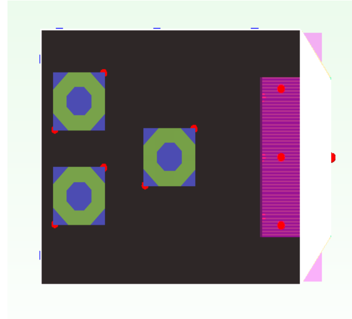
Figure 11.5 Layout of Electronics

The following are the cases considered for the study

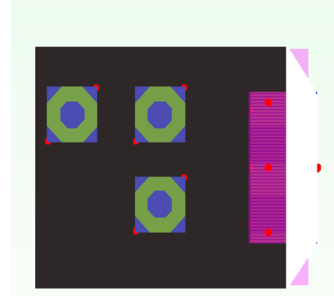
- Partition between the HX fans in the front
- Two fans in the bay fan tray instead of three
- For the best case obtained, it again tested with solar shields to see the improvement



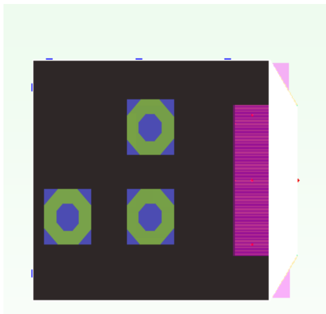
a



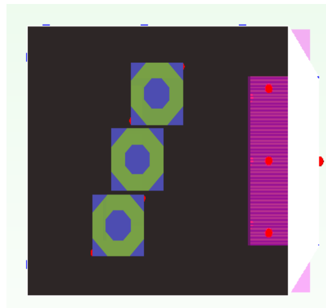
b



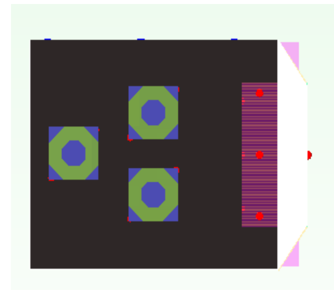
c



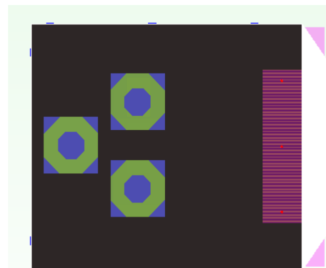
d



e

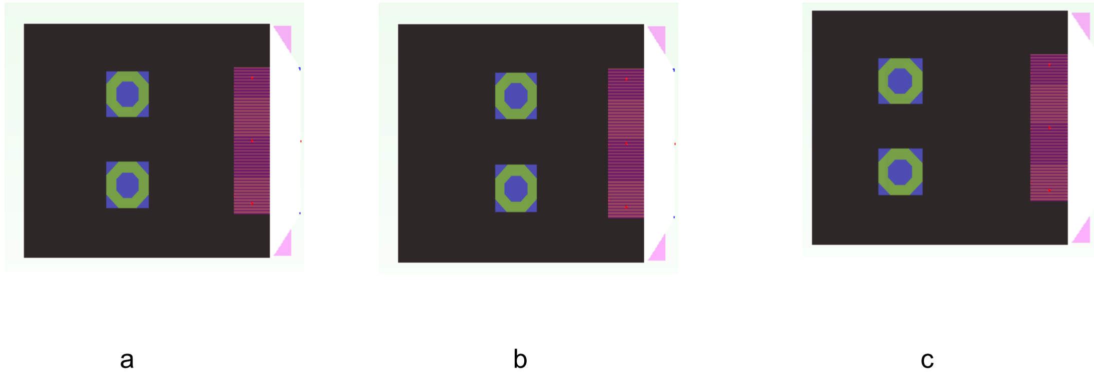


f



g

Figure 11.6 Various fan configurations considered – a to g (Case 1 to 7)



a b c

Figure 11.7 Fan configuration with two fans – a to c (Case 1A, 6A & 7A)

Table 11.4 Bay Fan Temperature for each configuration

Fan	Monitor Points	Case 1	Case 2	Case 3	Case 4	Case 5	Case 6
Fan 1	Left	86.52	77.74	86.48	86.40	78.68	87.14
	Middle	76.79	72.44	76.98	77.45	77.36	77.03
	Right	75.28	82.52	75.75	76.11	74.37	77.21
	Avg. Temp	**79.53**	**77.57**	**79.74**	**79.98**	**76.80**	**80.46**
Fan 2	Left	83.34	70.43	83.35	84.48	81.67	82.92
	Middle	86.00	70.65	86.45	86.88	88.52	84.04
	Right	83.58	85.70	83.93	84.69	81.88	82.85
	Avg. Temp	**84.31**	**75.59**	**84.58**	**85.35**	**84.02**	**83.27**
Fan 3	Left	69.95	92.15	79.30	70.81	70.23	70.17
	Middle	70.68	94.22	71.87	71.08	81.88	70.94
	Right	85.27	80.27	80.68	83.47	84.23	79.07
	Avg. Temp	**75.30**	**88.88**	**77.28**	**75.12**	**78.78**	**73.39**
	Avg Fan temp	**79.70**	**80.70**	**80.50**	**80.20**	**79.9**	**79.04**

Table 11.5 Bay Fan Temperature - with partition between HX fans

Fan	**Monitor Points**	**Case 6**	**Case 7**	**Case 1A**	**Case 6A**	**Case 7A**	**Case 1A with shield**	**Case 7A with shield**
Fan 1	Left	83.20	81.96	80.72	81.46	81.00	76.29	76.59
	Middle	72.64	74.74	72.77	72.23	73.67	68.54	69.32
	Right	73.00	76.65	72.47	73.97	74.28	67.67	70.43
	Avg. Temp	**76.28**	**77.78**	**75.32**	**75.88**	**76.32**	**70.83**	**72.11**
Fan 2	Left	80.24	75.50	73.85	75.61	66.90	70.85	63.32
	Middle	81.36	80.48	75.44	76.54	75.85	72.64	72.85
	Right	79.63	85.68	82.95	80.21	85.08	79.01	80.91
	Avg. Temp	**80.41**	**80.55**	**77.41**	**77.45**	**75.94**	**74.17**	**72.36**
Fan 3	Left	67.42	67.18					
	Middle	67.66	67.99					
	Right	75.06	80.87					
	Avg. Temp	**70.05**	**72.02**					
	Avg Fan temp	**75.58**	**76.78**	**76.37**	**76.66**	**76.13**	**72.50**	**72.3**

Based on the above specified cases the simulation is done. The fans positions for the condition without HX partition is shown in figure 11.6 (a to g) and for with HX partition in figure 11.6 (f & g) and figure 11.7 (a to c). The corresponding results are shown in tables 11.4 and table 11.5.

CHAPTER 12

RECOMMENDATIONS

Based on the results the following recommendations are provided for the betterment of the design

- For optimum door opening, the dimensions arrived at are
    - Width – 4.5”
    - Height – 17.2”
- Opening between the HX fans should be sealed as air escapes through the opening.
- For the bay fan tray with ***three Patriot fans***, configuration 6 (Case 6) can adopted as it has less average fan temperature
- With ***two Maltese fans*** in the bay fan tray, configuration 1A (Case 1A) can be selected as it has less electronics temperature
- Solar shield on top and side helps in bringing down the temperature of electronics and bay fan tray (fans) temperature
- Maltese fan would be a better choice for HX fans as the electronics and average bay fan temperature is less compared to Patriot and Major XT fans

APPENDIX A

ACRONYMS

MOSFET	Metal Oxide Semiconductor Field Effect Transistor
SOI MOSFET	Silicon On Insulator - Metal Oxide Semiconductor Field Effect Transistor
NMOS	Negative-channel Metal Oxide Semiconductor
PMOS	Positive-Channel Metal Oxide Semiconductor
DOE	Design Of Experiments
Cfm	Cubic feet per minute
HX	Heat Exchanger
CFD	Computational Fluid Dynamics

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