DESIGN AND STUDY OF PHASE LOCKED LOOP FOR SPACE APPLICATIONS IN SUB-MICRON CMOS TECHNOLOGY

by

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I dedicate my work to my parents and my uncle.

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ABSTRACT

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This work proposes a successful design of a radiation hard phase locked loop (PLL) using Silicon-on-Sapphire CMOS (SOS) technology for space applications. A fully self-bias radiation hard PLL providing frequency of 2.5 GHz has been designed for the first time on SOS technology. SOS technology is used to provide radiation hardness from Single Event Effects (SEE), an improvement over the use of commercially available bulk CMOS process. Innovative designs of VCO implemented in the PLL, architectural modifications in the use of buffers, bias stages, asynchronous dividers and optimization of fully self-bias design provide hardness from Total Ionization Dose (TID). Self-bias design, which provides noise immunity from external (Substrate and Supply) noises by incorporating symmetric load in the VCO and a biasing feedback loop, produces high internal noise, which is critical for the performance of the VCO. Thus, a novel VCO design is designed, which gives several dB of less phase noise than the typical symmetric load VCO used in the self-bias PLL for the same frequency of oscillation.

TID effects degrade the phase noise of the VCO. Thus, lowering the phase noise of the VCO as much as possible is important under radiation environment. The novelty introduced in the differential stages of the VCO cancels common mode noise (by clamped load), reduces corner

frequency of $1/f$ noise (by cross-coupled load) and reduces supply/substrate noise (by symmetric load). The substrate conduction of noise is also restricted by the use of the SOS technology.

TID effects can shift the operating region of the VCO to such a place where it may not work at all. Therefore, a huge tuning range of VCO is required, so that it can regain its proper functionality after it is displaced from its operating region. It is very critical for the proper functioning of the PLL. The new load design for the VCO provides a large tuning range. This was made possible by the use of cross-coupled load, which increases the amount of output voltage swing at certain controlling voltages. In addition, the use of clamped load in the load structure of the VCO provides a linear gain for the VCO, which in turn increases the tuning range.

Analytical expressions have been derived for phase noise of the new VCO and mathematical model has been derived for functioning of the PLL. The analytical expression is very important, as it will show the effects of different design parameters on the phase noise of the VCO.

Each block of the PLL has been developed individually for successful implementation in the radiation environment. Multiple stages of level shifters ("differential to single ended blocks") have been used between the VCO and the frequency dividers to enhance the signal levels of the produced oscillation. This is important for the next stages, which are the dividers, to work properly in the radiation environment. This implementation provides robustness against radiation effects.

Symmetric dividers are preferred for implementing frequency dividers in PLL, as they reduce "clock to Q" delay. However, in radiation environment they tend to fail, thus, frequency division in this PLL is implemented by asynchronous dividers. Five blocks of individual "divided by two" stages have been used for simplicity and robustness.

The phase frequency divider (PFD) used is specially designed to be TID tolerant as the "Voltage-Transfer-Curve" of the individual blocks in the PFD do not move much away from the fresh implementations under radiation effects.

Two self-bias stages are used. The self-bias stages provide controlling voltage and bias voltage for the current controlling stages in the VCO. This new arrangement is simple and provides stable controlling voltage to the VCO. This is very critical, as in case of any strong SEE hit at the output of the charge pump the disturbances will be dampened because of the isolation produced by the second self-bias stage.

In order to reduce the overall phase noise of the PLL capacitors are used at the controlling voltage node and the bias voltage node of the VCO. These capacitors are at least one tenth in value of the loop filter capacitance.

The simulation results for the phase noise of the different VCO designs have been presented. The plot for comparison has been presented, which shows that our VCO performs better. In addition, the plots for the functioning of each block have been presented. This is true for individual blocks and the PLL as a whole as well. The blocks required to build the self-bias PLL have been designed in schematic and drawn in layout. They have been designed to withstand radiation effects for all the process corner, temperature and voltage variations. The blocks have been simulated in schematic and layout to verify their performances. These exercises were carried out, first with fresh device model files and then with irradiated device model files.

The PLL has been successfully simulated for all the process (SS/FF/TT/SF/FS), temperature (-40ºC to +80ºC) and voltage variations. The PLL is robust and performs successfully in both fresh and radiation environment. The PLL has been simulated in Cadence-SpectreRF for schematic and layout simulations for fresh and radiation environment cases. The PLL achieves 2.5 GHz of output frequency. The VCO achieves a phase noise of -90dBc/Hz at an offset of 1 MHz. The VCO achieves tuning range of more than 2.5 GHz. The PLL locks in less than 600nS for the radiation hard design. The overall jitter is less than 12 pS for the radiation environment.

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CHAPTER 1

INTRODUCTION

Hazardous impact of radiation onto semiconductor devices/circuits/systems is one of the important concerns in space applications such as spacecrafts and airplanes. Semiconductor's deviation from normal states due to radiation can be classified into two categories: single event effect (SEE) and total induced dose (TID). SEEs are caused by penetration of highly energetic particles like heavy ions, which upset logic states of transistors in digital circuits; while TIDs represent semiconductor components' behaviors under long term exposure to radiation, including threshold voltage degradation, mobility degradation, and larger leakage current [1, 2]. This work focuses on designing radiation hard phase-locked loops (PLLs) that can be employed as accurate and robust high frequency clock generators in space applications. Both SEE and TID can potentially damage the normal functionalities of PLLs. SEE has instant effects on the logic states of frequency dividers and phase/frequency detectors in the PLLs. Also, an "SEE hit" might change the voltage level at the output of charge-pump or loop filter and would lead to erroneous output for a certain period of time or completely throw the PLL out of lock. TID may drift the threshold voltages or mobility and leakage currents in voltage controlled oscillators (VCOs), level shifters, and buffers, which could eventually cause the PLL to malfunction [1, 2]. Therefore, special design must be carried out to achieve radiation hard PLLs. Specifically, the following characteristics are the most critical for PLL design in radiation environments.

(i) Stability criteria of PLL should always be sustained, when threshold voltages and mobility of semiconductor devices are drifted by radiation [3].

(ii) The PLLs are required to have small *frequency-hop lock time* and *power-up/reset lock time*. Frequency-hop lock time denotes the time for PLL to go back to its desired frequency from another frequency. Apparently, a short frequency-hop time would quickly bring the PLL back to normal oscillation when it is shifted to an undesired frequency by radiation. As its name indicates, power-up/reset lock time is the time for PLL to lock with its reference clock after power-up or reset. In case radiation makes the PLL completely out of lock, the PLL must be reset and power-up/reset lock time dictates how fast the PLL regains its operation. Typically, lock time is required to be less than 100 cycles of the reference clock period in radiation environments [4].

(iii) VCOs in PLL must exhibit large frequency tuning ranges, in order to accommodate possible frequency shifts produced by radiation. As shown in [5], tuning range in excess of 50% of the operating frequency is necessary for PLL to maintain reliable operation under radiation.

(iv) In addition to the above three major concerns that are unique to radiation applications, it is always desirable for PLLs to demonstrate low jitter (low phase noise) and low power consumption.

Complementary metal–oxide–semiconductor (CMOS) is a desirable solution to implement mixed signal circuits like PLL as it offers low power and high compactness. Nevertheless, bulk CMOS process is vulnerable to radiation (especially SEEs), as shown by extensive research [6-13]. It is widely believed that, silicon on insulator (SOI) and silicon on sapphire (SOS) processes have better radiation tolerance and hardness than bulk CMOS [14], [15]. However, radiation hard CMOS circuit design (including PLL design) using SOI and SOS is still far from mature up to now [16], [17]. For instance, the LC-PLLs designed on SOI process in [5], [18] fail to lock when exposed to radiation. Radiation hard SOI wafer is successfully accomplished in [19] through annealing, shallow trench isolation, and guard rings; and it is later made use of in [20], [21]. In [22], enclosed layout techniques based on SOI are developed to significantly diminish leakage currents. The specialized processes in [19], [22] inevitably result

in high costs hence do not constitute the optimal solutions. In [23], a radiation hard SOI PLL is realized by taking advantage of voting scheme. Major drawback associated with voting scheme is that the required real estate is at least three times as normal PLL circuitries, which not only creates extra noise and power consumption but also makes it hard to operate in high speed/frequency applications. An all-digital PLL using SOS process robust to SEE is proposed in [4]. Although good at low frequencies, it is very difficult to be extended beyond GHz range. A high frequency PLL is designed in [24] with 0.25 μm SOS process; but under radiation, the designed oscillating frequency is out of the tuning range of VCO.

In this work, a radiation hard PLL is designed at 2.5 GHz. It adopts commercial SOS-CMOS process and does not require any specialized layout techniques. Radiation hardness is achieved through improving circuit design without sacrificing real estate. Stability of the proposed PLL is guaranteed by a fully self-bias architecture [25]. The lock time of PLL is minimized by maximizing the loop bandwidth subject to stability criteria [3]. Frequency tuning range and phase noise of VCO are significantly enhanced by a novel load configuration in the VCO buffers to maximize output voltage swing and improve linearity of VCO gain. In addition, multiple bias stages isolating the VCO control voltage from charge pumps and asynchronous frequency divider with high tolerance of threshold voltage change jointly make the proposed PLL more radiation hard. SOS process, with its inherent radiation hardness properties [14], [15] also facilitates the robust performance of the PLL in radiation environments. Layout of this PLL is simulated by Cadence SpectreRF under both SEE and TID radiation effects. Simulation results demonstrate excellent stability, lock time < 600 ns, frequency tuning range [1.57 GHz to 3.46 GHz], and jitter < 12 ps. Through comparison with PLLs in literatures, the PLL in this work is especially superior in terms of lock time and frequency tuning range performances.

CHAPTER 2

RADIATION EFFECTS AND SOS PROCESS

2.1 Total Ionization Dose effects

Total ionization dose (TID) effects on active devices are a long term exposure of electronic components to radiation. The total amount of ionization dose depends on the intensity of radiation and the period of exposure time. As reported in [14] T. Liu et. al. at Southern Methodist University (SMU) has preliminary TID results for Silicon-On-Sapphire technology based upon testing of an initial prototype chip. From the experimental results, TID resulted in a PMOS and NMOS threshold voltage shift, and an unexpected back-channel current leakage was observed.

2.1.1 Threshold voltage shift on PMOS

The TID test was carried out in the Brookhaven National Laboratory using Co-60 gamma source on 32 types of transistors [14]. Their I-V curves were measured before and after the irradiation, and during the month long annealing period. The total dose is 100 krad at 1.2 krad/hr. The width and length ratio of PMOS transistor is 40µm/0.25um with 4 fingers on the layout. From the measurement and calculation, it is found out that the TID effects increased the threshold voltage of PMOS transistors by about “+ 0.2” V.

2.1.2 Threshold voltage shift on NMOS

During this experiment, the total dose is 100 krad at 1.2 krad/hr [14]. The width and length ratio of NMOS transistor is 40µm/0.25µm with 4 fingers on the layout. From the measurement and calculation, it is found out that the TID effects increased the threshold voltage of NMOS transistors by about “+0.2” V.

2.1.3 Gate leakage current on PMOS

The gate current leakage in MOS transistors is increased after irradiation. Gate leakage occurs when electrons tunnel through the thin gate oxide layer. The trapped charges in the oxide act as an intermediate state in the transfer of electrons through the oxide [14], [1], [2]. The trap assisted tunneling is the reason for the increased gate current leakage after irradiation.

From the preliminary results, leakage current changed from below 100 nA before irradiation to 10 µA soon after irradiation but reduced back to below 800 nA after a 40 day annealing period. These results are with sapphire substrate floating during the experiment. This is with sapphire substrate floating.

2.1.4 Gate leakage current on NMOS

From preliminary results of [14], leakage current increased from 30 nA to 3 µA after irradiation but after annealing it went back to 90 nA after 40 days. This is with sapphire substrate floating.

According to the experimental results from [14], the gate leakage current on PMOS is much greater than on NMOS after irradiation and a 40-day annealing period. In addition, the impact of back-channel radiation-induced leakage on PMOS transistors is of more concern. This may cause undesirable behavior to the phase-locked loop. Some of the undesirable behaviors are unachievable lock, longer time to achieve lock, ringing, etc.

2.1.5 Annealing

A radiated device can recover from the effects of radiation by annealing. A fast PMOS leakage current anneals in 10 days at room temperature [14]. In addition, slow annealing is on going after 40 days. PMOS still has more of leakage current than NMOS after a 40 day annealing cycle [14].

2.2 Single Event Effects

Single Event Effects (SEEs) are caused by a single, energetic particle, and can take on many forms, by striking on a semiconductor device. The particle transfers the energy to the device material when it traverses through the device. Single Event Upsets (SEUs) are soft

errors, and non-destructive. They normally appear as transient pulses in logic or support circuitry, or as bit flips in memory cells or registers. Several types of hard errors, potentially destructive, can appear. Single Event Latch up (SEL) [1], [2] results in a high operating current above device specifications, and in most of the cases must be cleared by a power reset. Other hard errors include Burnout of power MOSFETS [1], [2], Gate Rupture, frozen bits, and noise in CCDs.

Single event phenomena can be classified into three effects (in order of permanency):

a) Single event upset / Single event transients (soft error)

b) Single event latchup (soft or hard error)

c) Single event burnout (hard failure)

CHAPTER 3

CHARGE PUMP PHASE LOCKED LOOP

A Phase Locked Loop (PLL) is a closed-loop feedback control system that generates a signal in relation to the frequency and phase of an input ("reference") signal. The output of phase-locked loop circuit compares with both frequency and phase of the input reference signals, automatically raising or lowering the frequency in a controlled oscillator until the output signal is matched to the reference in both frequency and phase [3]. Both analog and digital PLL circuits include three fundamental elements: A phase detector, a variable oscillator, and a feedback path. The feedback path is often employed as a sequence of frequency dividers. It divides the higher output frequency by a multiplication factor N to match the reference frequency.

The block diagram of a typical charge pump PLL [3] is shown below:

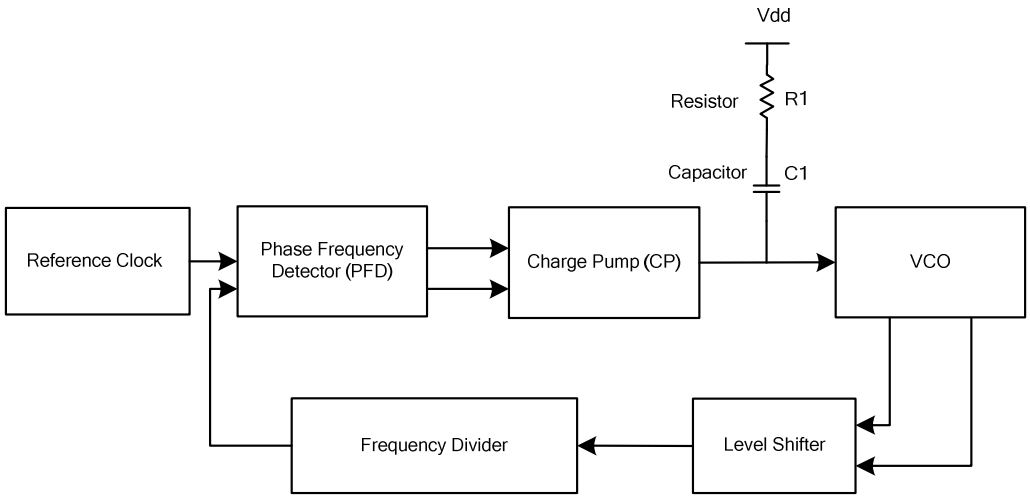


Figure 3.1 Diagram of typical 2nd order charge pump PLL

3.1 PLL Close Loop Transfer Function

It is imperative to understand the behavior of each building block and the overall closed-loop behavior in the PLL. The following sections focus on Charge Pump PLL (CP-PLL). The charge pump PLL (CP-PLL) with frequency multiplication model is illustrated below in Figure 3.2.

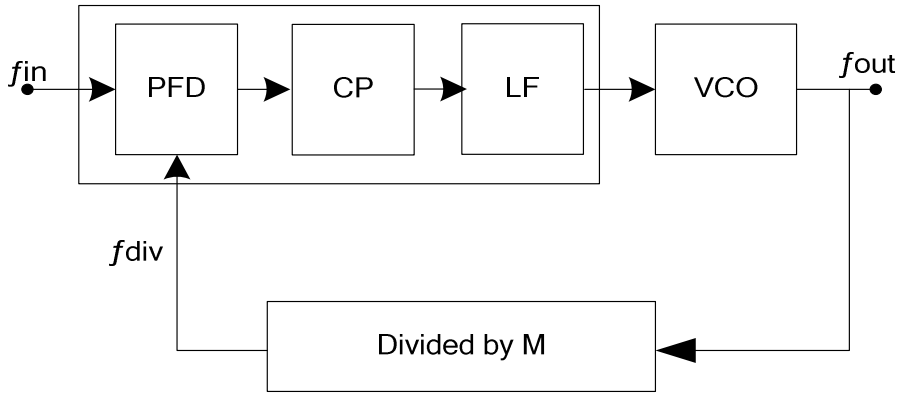


Figure 3.2 CP-PLL with frequency multiplication model

K_{PFD} is the gain of PFD block. *Icp* is the charge pump current. R_1 is the resistor and C_1 is the capacitor in the loop filter (LF) in Fig. 3.1 that provide the zero and pole in the transfer function. The transfer function of the PFD/CP/LF combination block can be expressed as $\frac{Icp}{2\pi}(\frac{1}{s \cdot C_1} + R_1)$. The forward gain (open loop) transfer function is

$$G_1(s) = \frac{Icp}{2\pi}(\frac{1}{s \cdot C_1} + R_1)\frac{Kvco}{s} \tag{3.1}$$

The loop gain is

$$G_2(s) = \frac{Icp}{2\pi M}(\frac{1}{s \cdot C_1} + R_1)\frac{Kvco}{s} \tag{3.2}$$

The transfer function of the PLL can be written as

$$H(s) = \frac{G_1(s)}{1 + G_2(s)} \tag{3.3}$$

Now substituting the forward gain and the loop gain into the PLL transfer function we get the following expression:

$$H(s)=\frac{G_1(s)}{1+G_2(s)}=\frac{\frac{I_{cp}}{2\pi}(\frac{1}{s\cdot C_1}+R_1)\frac{K_{vco}}{s}}{1+\frac{I_{cp}}{2\pi M}(\frac{1}{s\cdot C_1}+R_1)\frac{K_{vco}}{s}} \tag{3.4}$$

$$H(s)=\frac{\frac{I_{cp}}{2\pi}\frac{K_{vco}}{s}(\frac{1+s\cdot C_1R_1}{s\cdot C_1})}{\frac{2\pi M\cdot s^2\cdot C_1}{2\pi M\cdot s^2\cdot C_1}+\frac{I_{cp}}{2\pi M}\frac{K_{vco}}{s}(\frac{1+s\cdot C_1R_1}{s\cdot C_1})} \tag{3.5}$$

$$H(s)=\frac{\frac{I_{cp}}{2\pi}\frac{K_{vco}}{C_1}(s\cdot C_1R_1+1)}{s^2+s\frac{I_{cp}K_{vco}R_1}{2\pi M}+\frac{I_{cp}K_{vco}}{2\pi MC_1}} \tag{3.6}$$

The standard second-order transfer function can be written in another form as

$$H(s)=\frac{\omega_n{}^2+2s\xi\omega_n}{s^2+2s\xi\omega_n+\omega_n{}^2}\frac{M}{1} \tag{3.7}$$

Where the natural frequency ω_n of the system is

$$\omega_n=\sqrt{\frac{K_{VCO}\cdot I_{CP}}{2\pi\cdot M\cdot C_1}} \tag{3.8}$$

And the damping factor ξ is

$$\xi=\frac{R_1}{2}\sqrt{\frac{K_{VCO}\cdot I_{CP}\cdot C_1}{2\pi\cdot M}}=\frac{R_1C_1\omega_n}{2} \tag{3.9}$$

A PLL may be stable or unstable depending on the damping factor ξ and natural frequency ω_n. The criteria for designing a stable charge pump PLL is given below. There are upper and lower bounds for the two parameters mentioned above. For the damping factor, it has a lower bound of 0.5 and a usual upper bound of 2.0 (though in some cases it may go upto

20 or 30). For the natural frequency, which also corresponds to the loop bandwidth, it should be at least one-tenth of the reference frequency (input frequency) or less. This is required to keep the PLL stable [3]. Again, it should be more than $1/50^{th}$ of the reference frequency.

3.2 Voltage Controlled Oscillator

For proper functioning of a PLL, the frequency of the signal generator (VCO) in the PLL must be adjustable. An oscillator is an inseparable part of a PLL. This is the block, which generates the signal with required frequency for the PLL. The frequency of an oscillator is usually controlled by controlling the current flowing through the block or by the voltage. In this work, a voltage-controlled oscillator (VCO) is designed. This is because of the less current consuming property of a VCO than an equivalent current controlled oscillator (CCO). Although, a CCO is supposed to be more stable and tend to produce less phase noise.

The VCO is a circuit, which can tune the oscillator output frequency from the control voltage. The expression relating the frequency of the VCO with controlling voltage is given below.

$$\omega_{out} = \omega_o + K_{VCO} V_{CTRL} \tag{3.8}$$

Where ω_o is the free running frequency and K_{VCO} is the gain of the VCO, expressed in rad/s-V. The ω_{out} in the linear function indicates that, for the practical range of V_{CTRL}, ω_o may not approach zero. In other words, V_{CTRL} creates a change around ω_o. Figure 3.3 shows the VCO transfer characteristic.

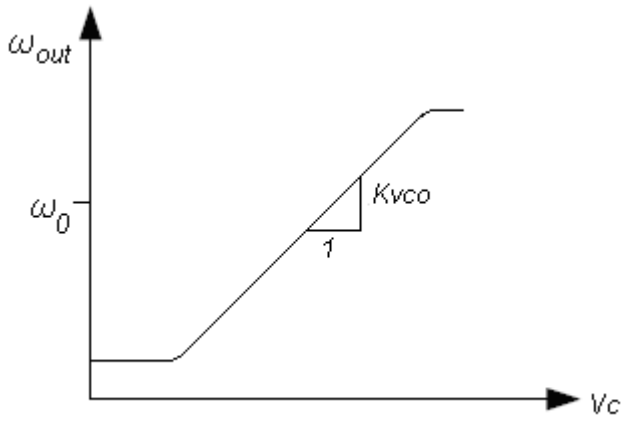


Figure 3.3 VCO transfer characteristic

There are two types of VCOs that one may choose to design.

1) Waveform oscillators

2) Resonant oscillators

Waveform oscillators have two topologies:

1) Ring oscillator topology

2) Relaxation oscillator (which has poor phase noise performance)

Resonant oscillators usually have two topologies:

1) LC tank oscillator topology

2) Crystal oscillator (which cannot be tuned and cannot achieve high frequency)

Ideally, a VCO topology should be able to meet all of the specifications such as

- High frequency (GHz for RF applications)
- Wide tuning range
- Low phase noise
- Low power
- Integrated
- Small die area occupancy

The following table shows the advantages and disadvantages of the ring oscillator VCO or LC tank VCO topologies.

Table 3.1 Ring Oscillator VCO vs. LC Tank VCO

	Ring Oscillator VCO	LC Tank VCO
Advantages	1) highly integrated in VLSI 2) low power 3) small die area occupancy 4) wide tuning range	Excellent phase noise and jitter performance at high frequency.
Disadvantages	As frequency increases, performance degrades because phase noise or jitter increases.	1) Inductor and varactor (variable capacitor) have large area in the die. 2) high power consumption 3) small tuning range

The ring oscillator oscillation frequency is given by $f_{osc} = \frac{1}{2 \cdot n \cdot T_{delay}}$ and LC oscillator oscillation frequency is given by $f_{osc} = \frac{1}{2\pi\sqrt{LC}}$.

The frequency of a ring VCO is determined by the number of stages and the delay per stage. The expression to determine frequency of one voltage controlled oscillator based on ring type configuration is $f_{osc} = 1/ (2*n*T_{delay})$. In the above equation, f_{osc} is the frequency of oscillation. n is the number of stages and T_{delay} is the delay of each stage. As can be deduced from the equation, the frequency of oscillation decreases with the increase in number of stages and delay per stage. In our case, the frequency of oscillation required is high in GHz range. Thus, the number of stages chosen is three, which is the minimum possible in a ring type configuration. The optimum time delay of each stage was calculated by noting the output current of each stage and the output capacitor in each stage. The calculation involves finding out the propagation delay of each stage. By definition, propagation delay of each stage is the time difference between 50% of transition at the input and 50% of output transition. This is formulized as $(0.69*R_{node}*C_{node})$, where R_{node} is the output resistance of the stage and C_{node} is the output capacitance. R_{node} is inversely proportional to the output current and hence can be figured out from the output current.

The three-stage ring oscillator is formed by placing one stage after another and connecting the output of the previous stage to the input of the next. Therefore, the output of the

final stage has to be connected to the input of the first stage in order to complete the connections. A voltage-controlled oscillator is an oscillator where the output frequency of the oscillator is controlled by an input voltage. This is done as following, the change in input voltage helps in changing the current flowing through each stage in the oscillator, which in turn changes the delay of each stage and finally the frequency of the whole oscillator is changed. This is significant because, in almost all the practical high frequency oscillators, with the change in environmental factors the operating condition of an oscillator circuit is changed and it is required to change the operating condition to bring the circuit to its original condition where it will produce the desired output frequency. This is done by changing the input voltage and hence the name. This is particularly true in harsh environment like radiation environment.

The block diagram of a three-stage ring type VCO is shown below.

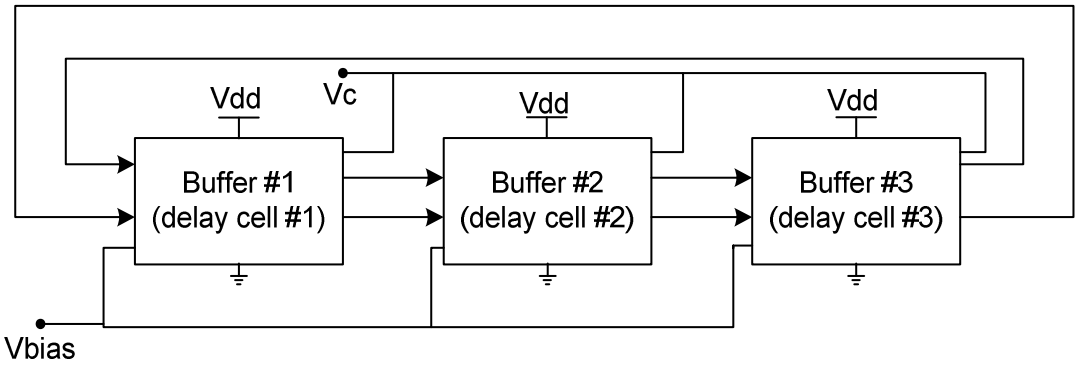


Figure 3.4 Block diagram of three-stage ring type voltage controlled oscillator. In the figure Vc is control voltage, Vbias is for bias control of three stages.

Tuning range and phase noise are two important parameters of characterizing a voltage controlled oscillator.

3.2.1 Tuning range

A large tuning range is desired since it will guaranty the return of the voltage-controlled oscillator to the original operating condition once it drifts away due to any change. This is essential in radiation environment as it is certain that under radiation environment the original operating point of a semiconductor circuit will change. This is because of change in each

radiation-affected device, which contributes to the change in the operating point of the whole circuit. It is also desirable that the voltage-controlled oscillator be a linear one or has linear conversion gain. This means that the voltage-controlled oscillator has constant change in output frequency due to linear change in input frequency. This can be formulized as K_{vco} = ("delta of frequency"/ "delta of voltage"). A linear conversion VCO gain is desirable because any other behavior of the VCO gain will reduce the effective tuning range and make the VCO more sensitive to extrinsic noise. For instance, any change in voltage at the control input of the VCO will change its frequency exponentially in case its K_{vco} curve is exponential. A linear gain is also desirable from implementation point of view. The VCO is ultimately integrated in a PLL. Any change in frequency will be corrected by the PLL using a negative feedback loop. The loop will come to a steady state gradually without much trouble if the K_{vco} gain is linear. Else, the PLL loop will have to encounter a nonlinear VCO gain and should be able to handle that and ultimately come to a steady state.

3.2.2 Phase noise

Phase noise of a VCO tells how accurate the VCO is with regard to its output frequency generation. Usually for a VCO the output frequency should correspond to a single tone at the desired frequency if it is generating sinusoidal (pure) signal, or at the most its other harmonics in the frequency spectrum. However, the practical VCOs are not as accurate and they produce several other frequency components close to the fundamental due to noise. This is known as phase noise in the frequency domain and corresponds to jitter in the time domain. In the frequency domain it looks like an accompanying skirt superimposed on the tone signal. The lesser the phase noise better is the VCO with regard to its noise aspects.

In an oscillator, phase noise is random fluctuations in the phase of a wave caused by time domain instabilities. The noise source may be internal or external to the oscillator, and noise can influence the output signal frequency and amplitude. Phase noise is usually characterized in the frequency domain. Figure 3.5 shows the ideal oscillator with an ideal

sinusoidal output at carrier frequency (ω_c). However in the real world, oscillators exhibit random fluctuations with noise spreading around both sides of the carrier signal.

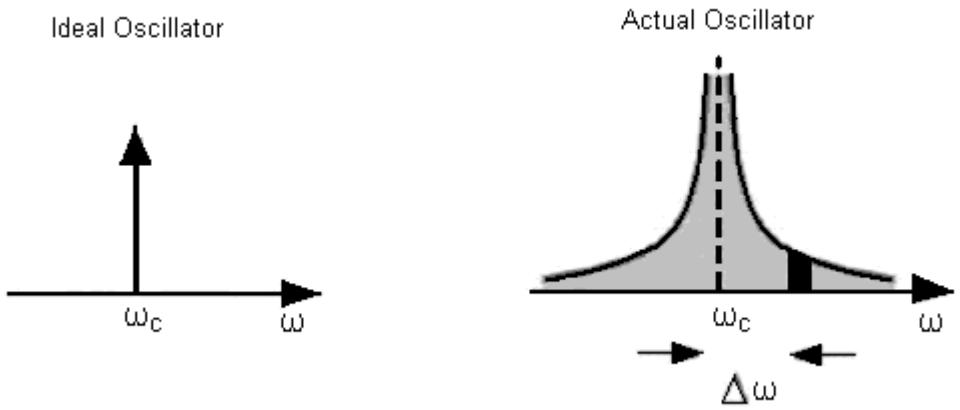


Figure 3.5 Output spectrum of ideal and actual oscillators. [26]

To calculate the quantity of the phase noise, it is needed to consider a unit bandwidth at an offset frequency ($\Delta\omega$) from the carrier frequency (ω_c), then within this bandwidth, noise power divided by carrier power is the phase noise.

Each of the elements in the PLL contributes noise to the overall phase noise on the output. The biggest noise contributor in the PLL are the oscillators (which is essentially true at low offsets from fundamental). The phase noise of the crystal oscillator, which creates the reference frequency and the VCO are a bottleneck for the total phase noise of the PLL. They determine the minimum possible phase noise of the PLL. The crystal oscillator cannot be controlled by a designer, but a VCO can be. Therefore, we attempted to minimize overall PLL noise by reducing oscillator phase noise as much as possible.

The concept of phase noise is relevant when judged from frequency domain perspective. On the other hand, a similar concept is widely considered from time domain perspective, especially for digital circuit. This is also known as jitter (as mentioned above). Jitter is an unwanted variation of one or more characteristics of a periodic signal. This is

characterized by the variation of the signal transition during zero crossing. Thus, this gives us an important design lead for lowering the jitter in any signal. Hence, to keep jitter to a minimum level, signals with fast transitions are needed to be produced.

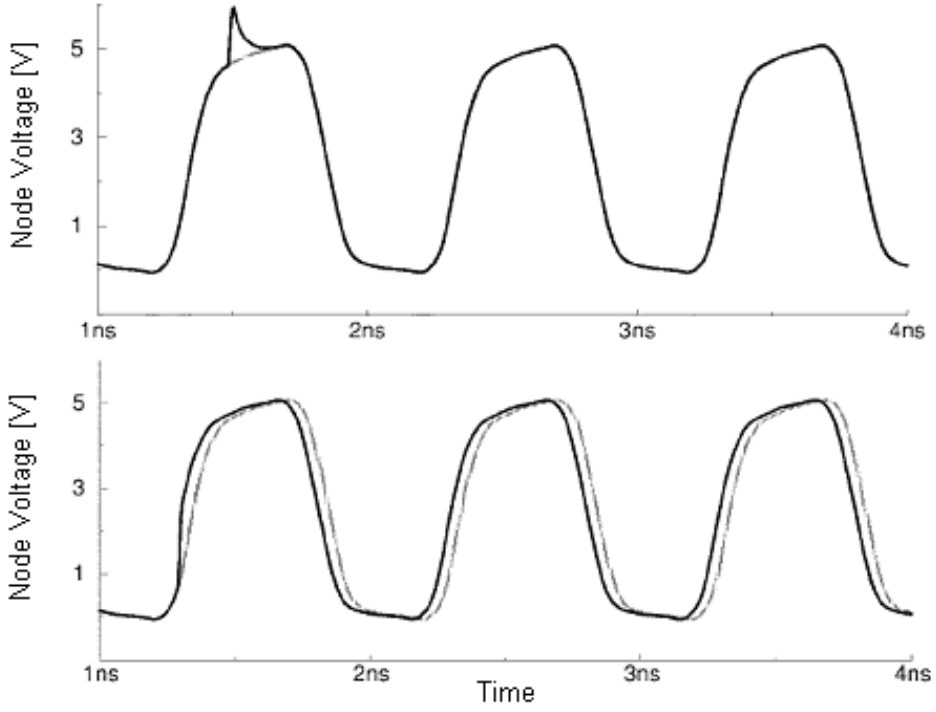


Figure 3.6 Effect of impulses injected during transition and peak. [27]

This can be seen clearly in the figure 3.6 above. An impulse injected introduced during the saturated response of a ring oscillator does not create any phase noise (as the oscillator recovers from its amplitude distortion), but, in the second case when the impulse is introduced during the transition of the signal it becomes a permanent harm and the signal cannot recover. Thus, a sloppy transition will always be prone to phase noise while a fast transition is tolerant of this effect to some extent

3.2.3 Reference Spurs

The input reference frequency modulates the VCO, and generates sidebands around the carrier frequency. In the ideal case, the UP and DOWN signals from the phase frequency detector to the charge pump would have identical and opposite outputs. However, in the real

world, because of mismatch in shapes of both the pulses, these spurs will be created. They will be increased by mismatched up and down currents from the charge pump, charge-pump leakage, and inadequate decoupling of supplies. The spurious tones will get mixed on top of the desired signal and reduce receiver sensitivity.

3.2.4 Amplitude of the output signal

The output peak-to-peak (p-p) signal produced by a VCO is also a parameter of concern. Usually the rule of thumb is more the p-p value better it is. However, it usually depends on several other factors like power consumption, frequency of operation etc. A large p-p amplitude is also desirable from phase noise perspective. This is because phase noise is quantified as the amount of noise with respect to the amplitude of the carrier signal. Thus, if amplitude increases phase noise decreases. This will increase power consumption though.

3.3 Voltage level shifters

Voltage level shifters [28] are not necessary in digital oscillators or in those oscillators where output is from rail to rail. However, in the analog type oscillators where the output signals usually do not reach the rail-to-rail amplitudes, level shifters are used to bring the output signals to desired operating range. In our case, the single-ended output of the differential VCO do not reach rail-to-rail, which is followed by digital divider circuits. The digital divider circuits usually require rail-to-rail inputs with the exception of CML dividers. Thus, it is essential to amplify the output signals of the single ended output from the VCO before being fed into the divider circuits. It is also important that the common mode voltage level of the output of the VCO is properly maintained for the input of the divider circuits. This is a necessity for CML dividers, but may be ignored in other kind of digital dividers where the rail-to-rail voltage level is maintained. This also provides isolation.

3.4 Divider circuits

High frequency divider circuits are always critical from design point of view. The output of the Voltage level shifters are fed into these blocks. In our case, the dividing factor, which is required to realize the operation, is 32. There are several ways of implementing this divide ratio.

For instance from architectural point of view there are synchronous dividers which have low "clock to q" delays, also how many dividers are to be used vary from design to design. In our case five divided by two circuits are used to give the ultimate divide ratio of 2^5 = 32. The choice of going for such a configuration is because implementing each “divided by 2” circuit is very simple and they would be able to tolerate huge change in the operating condition for being robust in nature. The con of using this configuration is that it will have a large “clock to Q” delay.

3.5 Phase/Frequency Detector

The PFD detects both phase and frequency difference of the divided feedback signal to that of the reference signal. Figure 3.7 illustrates the typical PFD operation. When the input frequency *A* is leading another input frequency *B*, the output signal Q_A generates the positive pulse, while Q_B remains at lower level. Otherwise, when the input frequency *A* is lagging another input frequency B, the output signal Q_B generates the positive pulse, while Q_A remains at lower level. When the frequencies of both input *A* and *B* are equal, the circuit generates pulses equal to the phase difference between the two inputs at both Q_A and Q_B. Hence, the outputs Q_A and Q_B are generally called the “*UP*” and “*DOWN*” signals. Figure 3.8 shows the PFD state machine diagram.

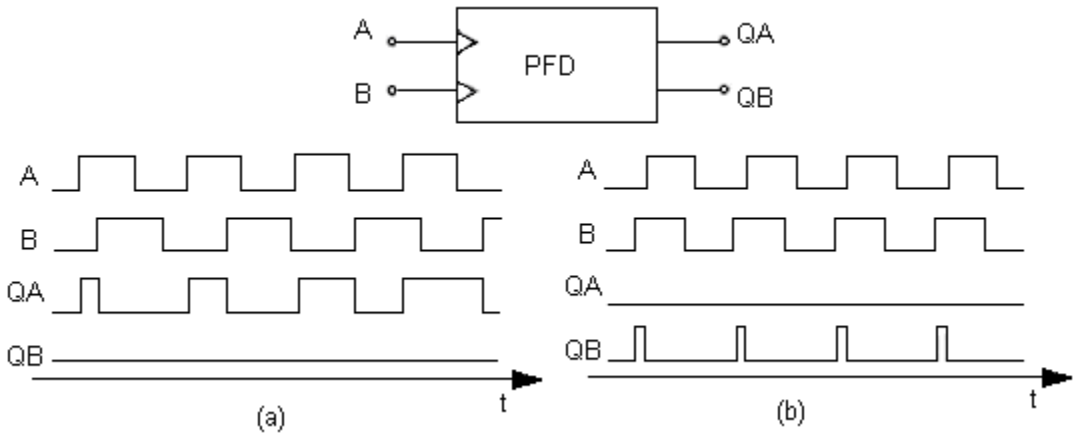


Figure 3.7 Phase/Frequency Detector (PFD) response (a) A leading B (b) A lagging B [26]

A PFD uses a simple state machine to determine which of the two signals has a zero-crossing earlier or more often.

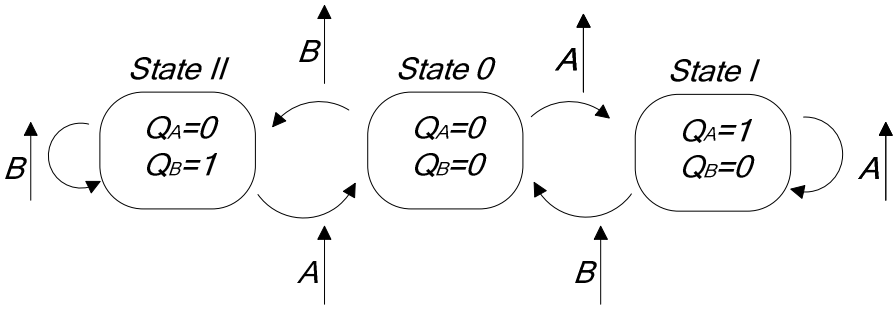


Figure 3.8 The figure showing the state machine diagram, which determines the functionality of a phase frequency detector.

Figure 3.9 illustrates the generic Phase/Frequency Detector. Usually a delay is used in between the output of the nand gate and the reset terminal in the practical cases. This is because the delay helps in producing equal shaped "*Up*" and "*Down*" pulses (Q_A and Q_B). This is necessary for the charge pump stage.

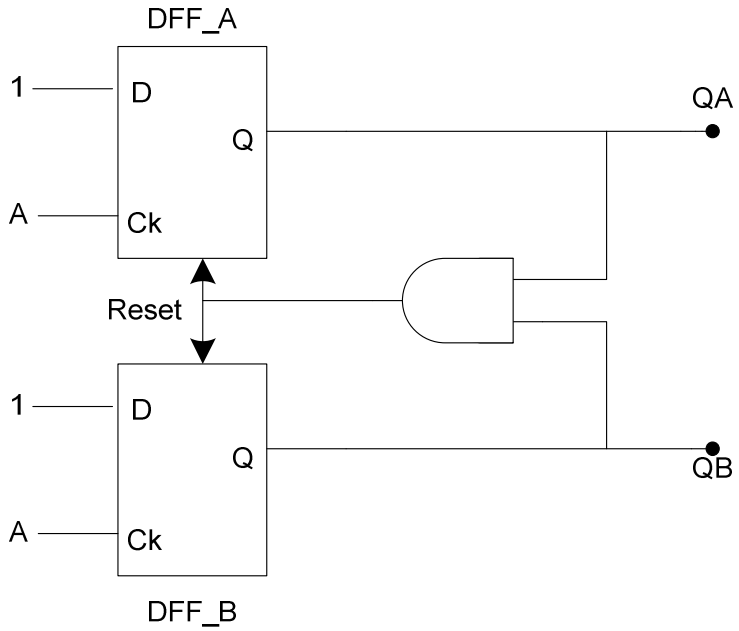


Figure 3.9 Phase/Frequency Detector (PFD) implementation

3.6 Charge Pump and Loop Filter

The charge-pump output stage of the PFD is shown in Figure 3.10. The charge pump output supplies current to the loop filter that generates control voltage for the frequency operation of the VCO.

The *UP* signal is high when the input reference signal is operating at a higher frequency than the feedback signal. The charge-pump forces current into the loop filter and causes the VCO control voltage to increase the VCO frequency and causes the feedback frequency to move towards the input reference signal.

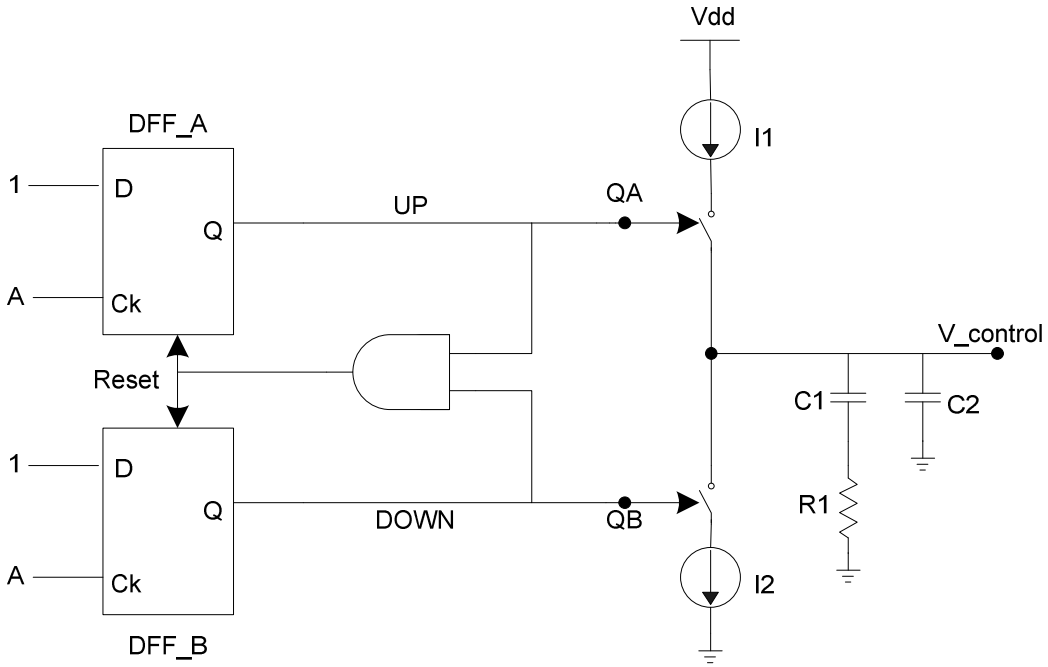


Figure 3.10 PFD with charge pump

Likewise, the *DOWN* signal is high when the input reference signal is operating at a lower frequency than the feedback signal. The charge pump sinks current out of the loop filter and causes the VCO control voltage to decrease. Then it decreases VCO frequency and brings the feedback frequency to match with the input reference signal. The loop filter is used to integrate the current pulses that flow from / to the charge pump and convert them to voltages.

There are several types of loop filter. The one shown in the figure above is having two poles (capacitors) and one zero (resistor).

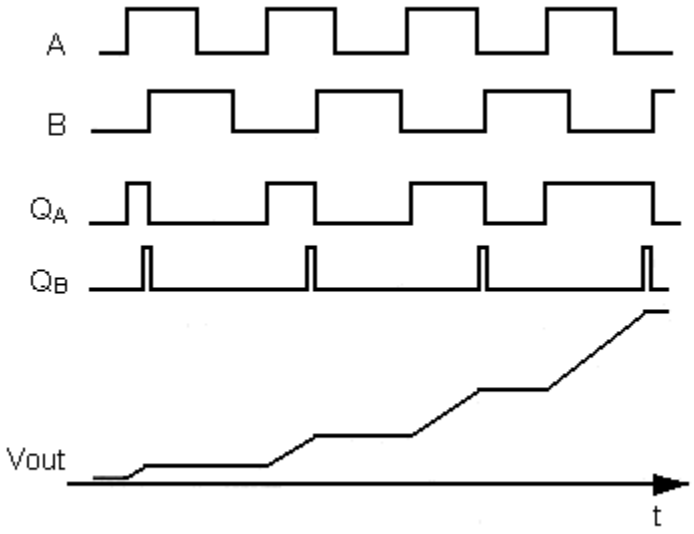


Figure 3.11 PFD with charge pump timing diagram [26]

The interaction between the PFD, charge pump, and loop filter is shown in Figure 3.11. Here the *UP* signal is high and forces the current into the loop filter. Hence, the VCO control voltage Vout is rising.

CHAPTER 4

SOS VERSUS OTHER PROCESSES

In this work, a PLL design has been proposed, which can tolerate changes in circuit behavior due to radiation effects and still can maintain its functionality and its performances. This type of high frequency PLL can be employed to build clock generators, which can be used in satellites and other space applications. This type of circuits can also be employed in data acquisition system circuits in high-energy physics experiments, e.g. in Large hadron collider as was the focus in [14]. Normal circuits will fail miserably as they cannot handle such large changes in circuit (/ device) behaviors. In addition, due to scaling, standard CMOS devices are getting smaller everyday. They show failures even at sea levels in terrestrial environments. Thus, it is very important that the circuits have radiation hard qualities.

The performances and functionalities of the semiconductor devices of a particular process in radiation environment are measured in terms of its hardness against several effects due to radiation exposure. When a CMOS (semiconductor) device is exposed to radiation, it suffers threshold voltage variations and gate leakage current due to total ionization dose [14]. These two effects of TID are devastating for circuits built with semiconductor devices used in radiation. One of the most important degradation is the change in leakage current. A huge excess leakage current can destroy the functionality of a MOS device. These faulty devices collectively destroy the functionality of a circuit in which they are used. Thus, it is important to have devices, which exhibit low leakage currents under radiation exposure. A comparison of leakage current in standard CMOS devices and SOS CMOS devices are given below:

The results of [29] show that the sub-threshold IV curves of the normal standard bulk CMOS is not good for radiation hard practices. The plot is given below:

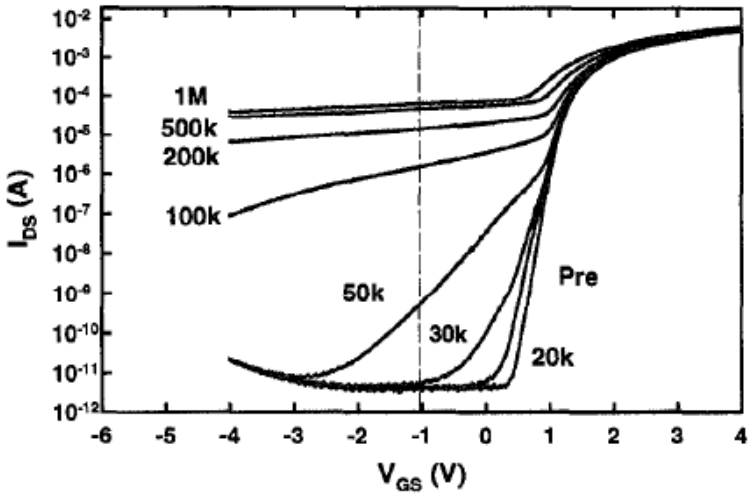


Figure 4.1 Subthreshold I-V curves for n-channel transistors irradiated at room temperature in steps to 1 Mrad(Si02) using 10 keV x-rays at 167 rad(Si02)/s. The devices used have 0.75um minimum gate length [29].

The results of [30] shows that the sub-threshold IV curves of the normal standard CMOS for 0.5um devices are even worse and concur with the previous data. They will give away under radiation effects. Leakage result is after 40 krad of radiation.

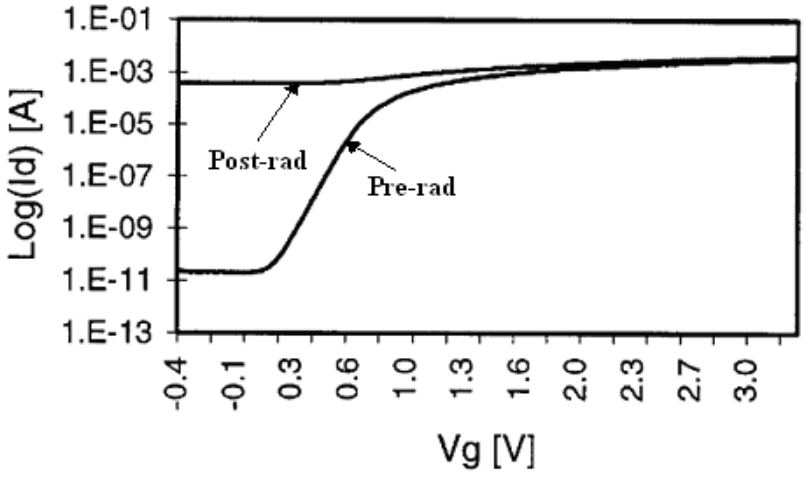


Figure 4.2 10/0.5um device leakage current. Pre rad and post rad for standard CMOS [30]

Similar test results done with 0.25um SOS CMOS shows that the change in I-V curves for heavy radiation (upto 100k rad) are much better for SOS process. T. Liu et.al. in [14] carried out the test. The plot is given below. The results are with floating sapphire substrate.

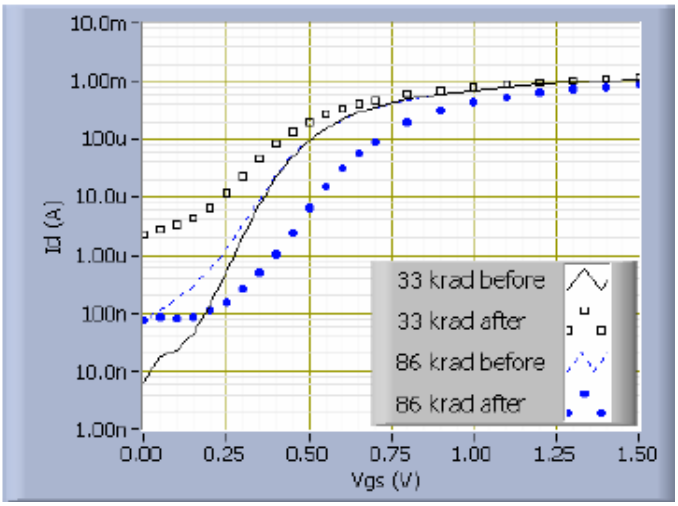


Figure 4.3 The I-V curves of NMOS (Sapphire floating). For enclosed layout technique [14].

Similar test results, done with 0.25um SOS CMOS with grounded sapphire substrate, show that there is no change in leakage currents for heavy radiation (upto 100k rad) [14]. The result is same irrespective of the use of enclosed layout technique. There is a change in threshold voltage though.

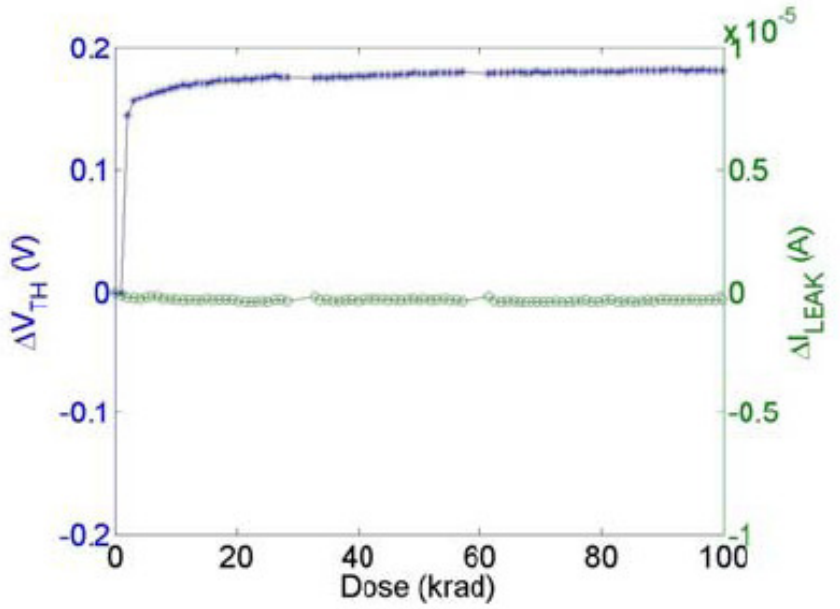


Figure 4.4 NMOS threshold voltage change (left) and leakage current after 100Krad irradiation. NMOS W/L=40/0.25 16 fingers. [14].

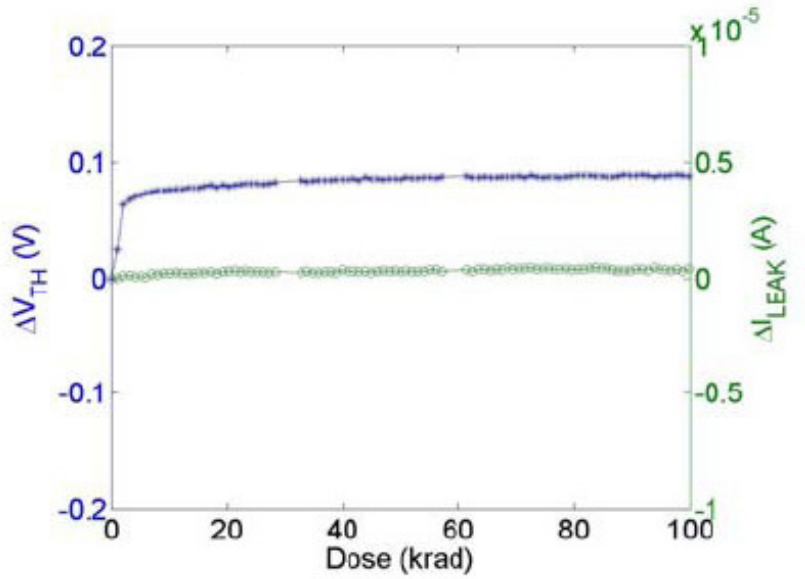


Figure 4.5 PMOS threshold voltage change and leakage current after 100Krad irradiation. PMOS W/L=40/0.25 16 fingers. [14]

The PLL circuit here is proposed to be designed in SOS CMOS process. A PLL usually have both digital and analog circuits in them. The digital circuits are employed in the dividers

and phase frequency detectors, which are usually made with D flip-flop circuits. VCO, voltage level shifters, charge pump, loop filter are analog circuits.

It should be noted that the digital circuits are more prone to SEE errors, whereas the analog circuits are vulnerable to both SEE and TID errors. The digital circuits like the dividers and phase frequency detectors, which are made of D flip-flops, should therefore have as less SEE effects as possible.

SOS bears inherent radiation hardened qualities. SOS is purely single event latch-up (SEL) free as reported in [14]. In addition, it is better than standard CMOS process from other SEE perspectives like single event upsets, single event transients and single event burnouts. A comparison of different circuits, made in standard CMOS and SOS that were irradiated as reported in [14], [31] has been presented here. The results of [14] are given below. These are SOS results.

Table 4.1 Results of SEE effects on SOS circuits

Test Element Type	Fluence (proton/cm2)	Error Count #	Cross-Section (cm2/bit)
Std Shift Register	1.8*10^12	0	<5.6*10^-13
ELT Shift Register	1.8*10^12	0	<5.6*10^-13
Res. Hard Shift Register	1.8*10^12	0	<5.6*10^-13
SET free logic latch	1.8*10^12	0	<5.6*10^-13

The results of [31] are given below. These are bulk CMOS results. These are with specially laid out bulk CMOS with special epitaxial layers and guard rings.

Table 4.2 Results of SEE effects on bulk CMOS circuits

Flip flop	Error rate (error/bit-day)	Fluence	Cross section (cm2/bit)	Onset LET (MeV-cm^2/mg)
DFF	8.1*10^-9	1.00 * 10^7	2.8*10^-7	19
LDFFM	2.0*10^-9	1.00 * 10^7	2.0*10^-7	23
LDFAPCM	1.9*10^-9	1.00 * 10^7	2.5*10^-7	29
SDFFM	<1.6*10^-12	1.00 * 10^7	2.3*10^-8	55
SDFFAC1M	<1.7 * 10^-10	1.00 * 10^7	1.2*10^-8	23
SRAM	2.7*10^-9	1.00 * 10^7	1.3*10^-7	19

T. Liu et.al. in [14] group carried out the SEE tests with 0.25um SOS CMOS process. The results above show that SOS CMOS process results are far better than the regular CMOS results. The SEE cross section has been measured. It has been found to be much less than the bulk CMOS SEE cross section. It is important to note here that the results of the designs in 0.25um standard CMOS reported in [31] and presented in the above table are done with various changes in design and layouts. They are presented below:

1. Annular transistors are used
2. Transistor guard rings are used
3. Enhanced well and substrate tie-down design rules are used
4. Transistor sizing for drive strength / nodal capacitance is used
5. Wide metal bussing at cell and die level coupled with package designs is utilized

In addition, the 0.25um CMOS process used is an advanced one having features like epitaxial wafers and shallow trench isolation. This will enhance the cost of fabrication.

A number of experimental procedures [32 -37] and computer simulation techniques [38-42] have been done to understand the SEE (SET) phenomenon on semiconductor devices and circuits. Single Event Effects (SEE), which includes SEL, SET, SEU, SEB, etc, can disrupt the proper functionality of a PLL and can lead to erroneous results for several cycles before the PLL

can get back its lock. This study was done intensively by T. D. Loveless et. al. in [43]. Some of their results are presented below.

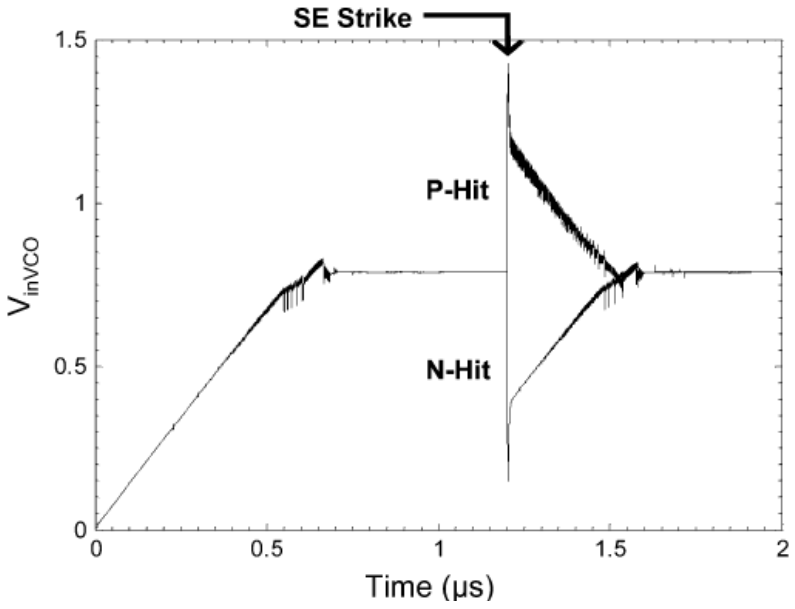


Figure 4.6 Vinvco vs. time for 700 MHz operation. SE strikes occur at 1.2 us and span over approximately 280 clock cycles, resulting in approximately 120 erroneous clock pulses.

The above result shows that the PLL is in error for 120 cycles. This is a typical charge pump PLL built with standard bulk CMOS devices. The charge pump stage, which supplies the current to the loop filter in a typical second order charge pump PLL, is the most sensitive stage with respect to SEE strikes as has been identified by [44]. The group in [43] built a radiation (SET) tolerant PLL by changing the current sink / source charge pump to a voltage level tri-state charge pump. They used standard bulk CMOS devices. The result of the improvements is shown below:

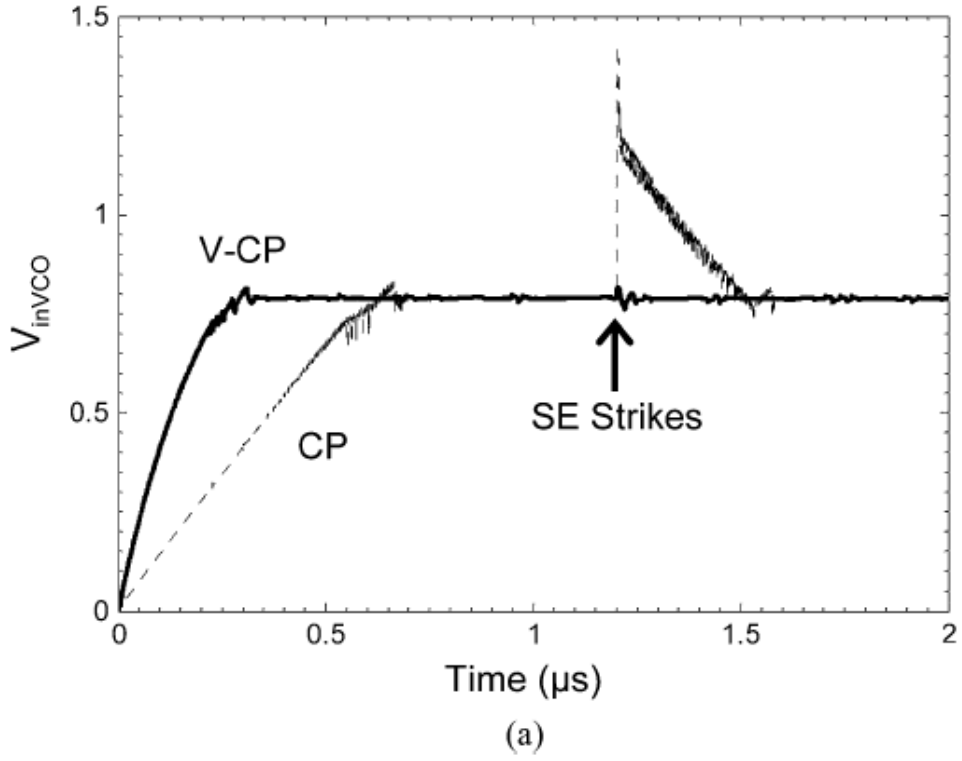


Figure 4.7 Vinvco vs. Time. The acquisition curves illustrating the voltage perturbation resulting from SE strikes depositing 200 fC of charge in the V-CP and the CP for 700 MHz operation. The CP exhibits a voltage perturbation of 0.64 V and a time to recovery of 400 ns while the V-CP exhibits a voltage perturbation of 42 mV and a time to recovery of 98 ns.

It should be noted here that even though there is a considerable improvement in the performance of the V-CP PLL proposed by [43], it is not completely free from SEE strikes and thus prone to error. As can be seen from the above result there is a 98 nS of erroneous result produced by the PLL for one SEE strike. This can be completely got rid off using SOS devices as has been noted in the NASA guidelines in [45]. Presented below is a comparison of SOS CMOS built synthesizer with synthesizers built with other technologies [46].

Table 4.3 Parameters used in Calculating single Event upset Rate for Candidate Synthesizer Devices [46]

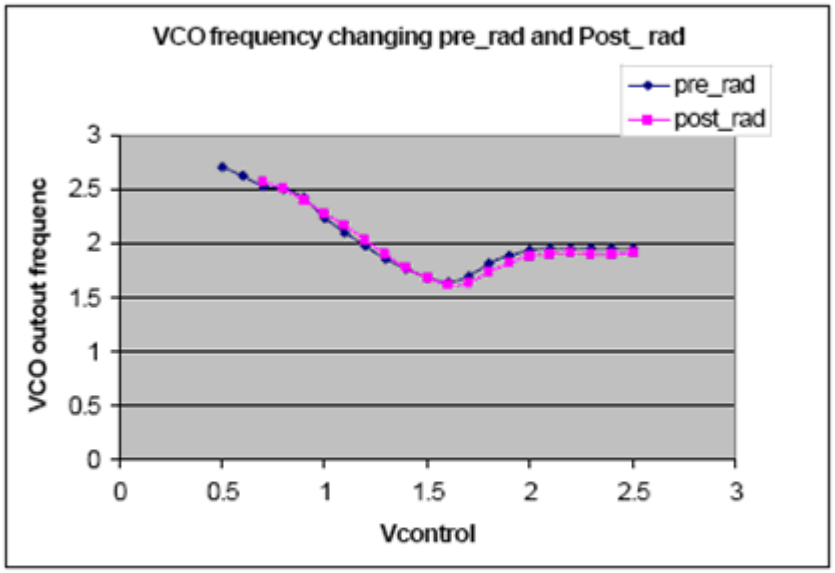
Device type	Manufacturer and Technology	Saturated cross section (cm^2)	length and width of sensitive region (microns)	depth of sensitive region (microns)	LET at 25% of saturated cross-section (MeV-cm^2 mg^-1)	Critical charge (pC)
PE 3282A	Peregrine CMOS-SOS	6.5*10^-7	8.06	0.1	39.2	0.04
LMX2315	National Bi-CMOS	5.0*10^-5	70.7	1	22.5	0.229
Mitel SP8855	Mitel BJT - HE Process	1.1* 10^-5	33.2	2	5.5	0.112
Mitel SP8858	Mitel BJT - HE Process	3.66*10^-5	605	2.5	7	0.112

Table 4.4 SEU Rate of Candidate Synthesizer Devices Using CREME Code [46].

Device type	Manufacturer and Technology	Solar Minimum Environment	Solar Minimum Environment	90% Worst Case Environment	90% Worst Case Environment
		Number of Upsets/device /day	Time for one upset/ device	Number of Upsets/device/day	Time for one upset/ device
PE 3282A	Peregrine CMOS-SOS	9.13*10^-8	30008years	1.5*10^-7	18264 years
LMX2315	National Bi-CMOS	3.09*10^-5	88.7 years	5.07*10^-5	54.04 years
Mitel SP8855	Mitel BJT - HE Process	1.18*10^-4	23.2 years	1.97*10^-4	13.9 years
Mitel SP8858	Mitel BJT - HE Process	2.80*10^-2	35.7 years	4.76*10^-2	21 days

Since the SOS devices do not have any soft error (free of single event transients (SET) and SEU) or hard error (free of single event latch ups (SEL) and single event burnouts (SEB)), the SOS PLL should work properly with regard to its functionality and should have less jitter. The functionality will remain maintained since it is SEL / SEU / SEB / SET free. It is also free of

leakage current changes due to TID effects. The important thing that needs to be taken care of is the threshold voltage changes due to TID effects. P. Zhu et. al. in [47] did an experiment to show the TID effects (change in threshold voltage) on the tuning range of a VCO built with 0.25um SOS-CMOS. The results is shown below.



when Vbias = 0.6 V

Figure 4.8 VCO output frequency versus control voltage Vc when biasing voltage Vbias is 0.6v [47]

The design of a self bias PLL on SOS CMOS process has been discussed later with a focus on TID effects. It is claimed here that the PLL designed on this process will have no degradation in its performances with regard to the radiation effects upto 100 Krad. This will be presented later and verified by characterizing each block and the PLL as a whole. A simulation case of SEE effect on the PLL is also presented later.

4.1 Silicon on Sapphire

The 0.25 micron SOS process has been made commercially available by Peregrine Semiconductor since 2005. The decision to use this process (technology node) is because of the absence of substrate in SOS, so less SEE effect. Since, substrate is replaced by sapphire in

SOS, the power supply and ground are not affected by noises and disturbances that are generated in the substrates as is the case in regular CMOS processes.

Silicon On Sapphire (SOS) is a hetero-epitaxial process for integrated circuit manufacturing that consists of a thin layer (typically thinner than 0.6 micrometers) of silicon grown on a sapphire (Al_2O_3) wafer. SOS is part of the Silicon on Insulator (SOI) family of CMOS technologies. Figure 4.9 shows the Silicon-On-Sapphire (SOS) structure in a CMOS technology. SOS is primarily used in aerospace and military applications because of its inherent resistance to radiation. The advantage of sapphire is that it is an excellent electrical insulator, preventing stray currents caused by radiation from spreading to nearby circuit elements. SOS has seen little commercial use to date because of difficulties in fabricating the very small transistors used in modern high-density applications.

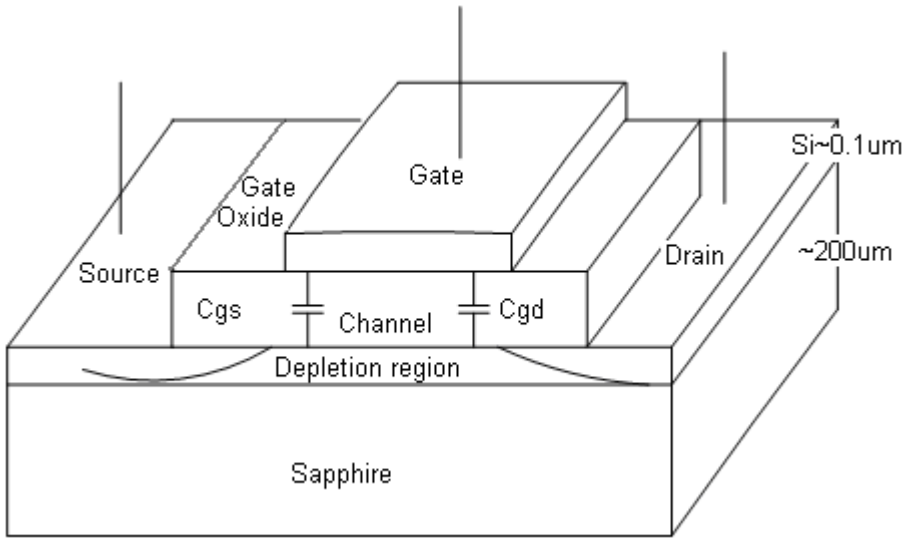


Figure 4.9 Silicon-on-Sapphire process technology

Peregrine semiconductor has announced a 0.25 µm Silicon-On-Sapphire (SOS) process in August 2004. The two new single poly, triple metal processes, designated as GA and GC, complement the existing 0.50 µm FA and FC processes and will push the transistor performance beyond the 100 GHz maximum oscillation frequency. While the GA is aimed at analog/digital circuits, the GC with low-loss high Q passives (L and C) capability is tailored for

RF and mixed-signal designs. Reference [14] selected GC process from Peregrine semiconductor in a Link-On-Chip (LOC) ASIC design, which they were using, because the low electron mobility at the Si-Sapphire interface causes the reduction of the back-channel leakage current in NMOS device. Additionally, the high Q capability on inductors and capacitors is a beneficial consequence for the LC-VCO design.

4.2 Difference between SOS CMOS and regular CMOS

The structural and operational differences between regular CMOS devices and SOS CMOS devices and their pros and cons are noted below.

The regular CMOS is grown on a silicon substrate. For instance, the NMOS is grown on a P- substrate and PMOS is grown on N-well (similar to substrate. The reverse is true in some processes.) [48]. On the other hand, the SOS CMOS does not have a silicon substrate. The silicon substrate is replaced by resistive sapphire. The CMOS grown on the sapphire is usually 0.6um in thickness or less [7]. There are several advantages and disadvantages of SOS CMOS over regular CMOS. Some of them are listed below.

The SOS CMOS is usually faster than the regular CMOS. This means they have larger f_t (cut-off frequency) and f_{max} (maximum frequency of oscillation) than that of regular CMOS. This happens because of the absence of substrate in case of SOS CMOS, which helps it with less or no parasitic capacitance with respect to the body. The other advantage is that there is no body bias effect in SOS CMOS. This also gives isolation. Thus if any device is affected by noise, glitch or radiation effects, other part of the circuit is not affected.

The disadvantage of SOS CMOS devices are that they hold some charges in them during the fast transitions of signal. This happens because there is no path (capacitive path through the substrate) for the charges to drain out. This produces memory effects. The other effect is that they tend to be noisier than the regular CMOS.

The design of self-bias charge pump PLL circuit (blocks of the PLL) for radiation environment is given below.

CHAPTER 5

SELF BIAS PLL CIRCUIT DESIGN

The self biased PLL [25] is chosen for its advantages to achieve process technology independence, fixed damping factor, fixed bandwidth to operating frequency ratio, broad frequency range, input phase offset cancellation, and most importantly low input tracking jitter. Self biasing avoids the necessity for external biasing, which can require special band-gap bias circuits, by generating all of the internal voltages and currents from each other so that the bias levels are completely determined by the operating conditions [25].

Self-bias PLL tolerates changes in process / technology/ voltage etc due to radiation or other environmental factors. This is possible as the parameters for determining stability criteria (ξ and ω_n / ω_{ref}) are determined solely by ratio of two capacitors, which are not adversely affected by radiation.

The self-biased PLL [25] designed here, have low supply / substrate noise sensitivity because of the following reasons. The self-bias generator [25] shown in the Fig. 5.14 and Fig. 5.15 produces the bias voltages V_{c1} and V_{bias} form the control voltage V_c. Its primary function is to continuously adjust the buffer bias current in order to provide the correct lower swing of the VCO buffer stages. The figure of a typical buffer stage is shown in Figure 5.6. In so doing, it establishes a current independent of supply voltage. It accomplishes this task by using a differential amplifier and a half buffer stage (which will be shown later while describing the self-bias stage). The amplifier adjusts V_{bias} so that the voltage at the output of half buffer is equal to the lower swing limit. If the supply voltage changes, the amplifier will adjust to keep the swing and thus the bias current constant. The bandwidth of the bias generator is typically set equal to the operating frequency of the buffer stages so that the bias generator can track all supply and substrate voltage disturbances at frequencies that can affect the PLL design. Use of SOS

CMOS helps by isolating the transistor from the substrate (as substrate is replaced by resistive sapphire). However, in radiation environment, the drift of threshold voltage and increased gate leakage current may change the operating bias of the circuit. The self-biased PLL having the above-mentioned advantages is an excellent candidate for working in radiation environment.

The block diagram of the self-bias PLL design is given in Figure 5.1. The output frequency is generated by the Voltage Control Oscillator (VCO). The output of the VCO goes into the voltage level shifter (differential input single output stage), which in turn goes into the frequency divider block. The frequency divider block consists of five “divided by two” stages. The output of this stage is fed back to one of the inputs of the phase frequency detector (PFD). The other input of the PFD is connected to the reference signal or input signal. The reference signal (or the input signal) is generated by a crystal oscillator. This is because the reference clock is supposed to be very stable. A crystal oscillator can generate a very stable frequency clock signal, as it does not vary much with temperature and other environmental changes.

Depending on the lead or lag of the feedback signal with respect to the reference signal, the PFD generates corresponding up and down signals. These signals are input to the charge pump (CP), which generates the control voltage (Vc1) for the VCO by charging or discharging the loop filter (LF). For the LF, the circuit does not use any passive resistor but uses the output stage of the self-bias circuit as described in [25] and shown in Figure 5.1. The self-bias circuit is shown in Figure 5.15. The PLL will have two charge pump circuits, which provide the same current to the capacitor and resistor individually. CP1 charges (/ discharges) the capacitor, CP2 charges (/ discharges) the resistor by the same amount of current. Thus, the function of the LF is maintained as it acts as if the capacitor and resistor are in series.

The block diagram of self-bias PLL [25] is given below.

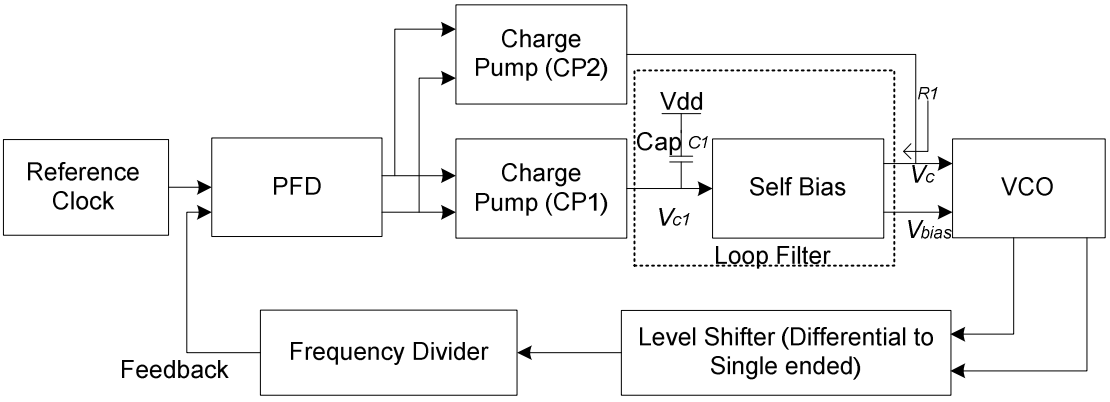


Figure 5.1. Diagram of self bias PLL

The blocks which are required to make phase locked loop are:

1) Voltage controlled oscillator

2) Voltage level shifter

3) Divider circuits

4) Phase frequency detector

5) Charge pump

6) Loop filter

7) Self bias circuit

The difference between typical charge pump PLL and self-bias PLL is given below. A typical charge pump PLL is implemented with a loop filter, which is a combination of discrete resistor and capacitor. In a self-bias PLL, the loop filter is constructed by using the output stage of the self-bias stage as a resistor. Doing this helps the PLL to track the changes in operating conditions and cancels out the drift by an opposite change. In addition, it should be noted that a self-bias stage is totally absent in a typical charge pump PLL and so a typical PLL does not usually track the supply and ground disturbances as effectively as the self-bias PLL.

5.1 Voltage controlled oscillator

The voltage-controlled oscillator used for this particular purpose is a ring oscillator. The ring oscillator has three stages. Each stage of the ring oscillator in a self-bias PLL is typically a

differential type buffer having symmetrical loads [25]. The motivation to use symmetric load comes from the fact that radiation environments are inherently noisy. In this environment, symmetric load configuration will be most effective because of its excellent supply-noise rejection capability. Symmetric load buffers for VCO sets the platform for a self-bias PLL.

The symmetrical load is formed by putting together a parallel combination of a PMOS transistor and a diode connected PMOS transistors. This is shown in the figure 5.2 below. This type of load is linear resistive in characteristic and so used to track any noise on the power supply line. They follow the power supply changes very well as mentioned by J. Maneatis in his paper [25].

This particular combination is known as symmetric load because of the compensation of currents through two different branches. The total current that flows through this kind of load is supposed to be linear or near linear as it moves around a linear path. This will be clear with the illustrations below. The diode-connected load produces almost the opposite current characteristic than the PMOS load for the same voltage across their drain and source. The diode-connected load produces a current, which has square polynomial like characteristic. On the other hand the PMOS load creates an inverted square polynomial like characteristic. Thus, they merge in the end and produces the near linear type current characteristic. It has been illustrated later in the diagram of current compensation.

The symmetric load was simulated separately to verify the linearity of its I-V characteristic. The circuit was swept for its current characteristic by sweeping the voltage across the drain and source while the control voltage Vc was kept, first at 1.25 volts and then at 2.5 volts. The plots in the simulations concur with the theory and show a nice linear (or near linear) characteristic for its current versus voltage variation. These are shown in the figures below.

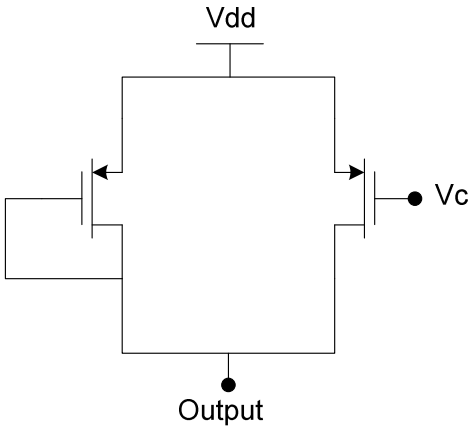


Figure 5.2 symmetrical load

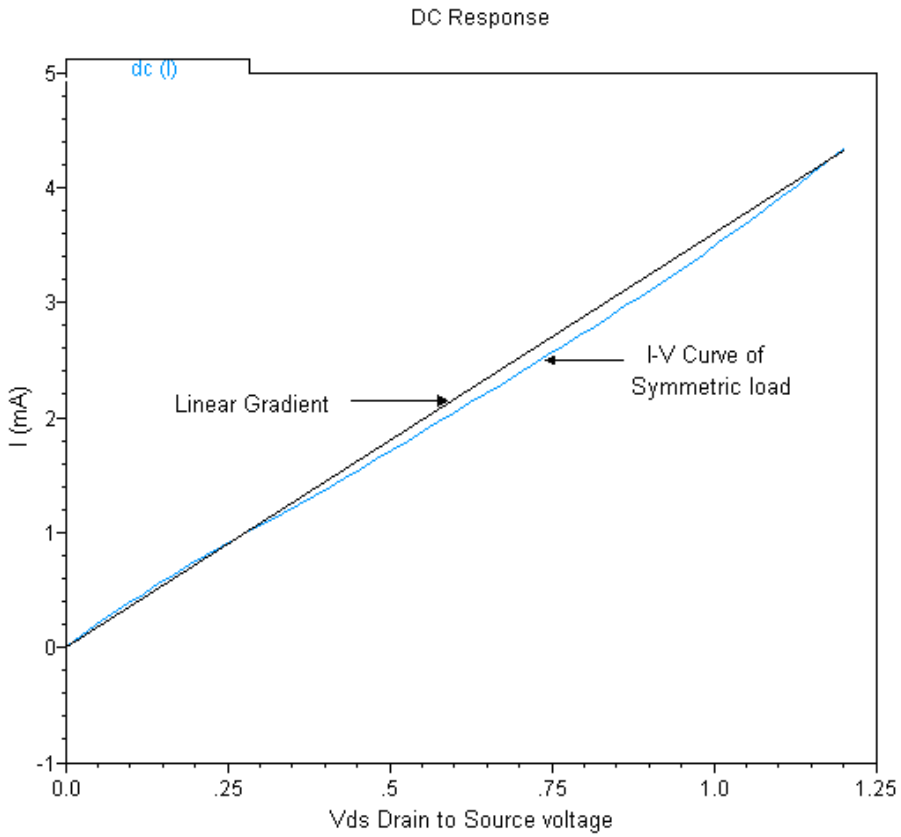


Figure 5.3 Diagram of I-V characteristic of Symmetrical load for voltage upto 1.25 volts when Vc is at 1.25 volts.

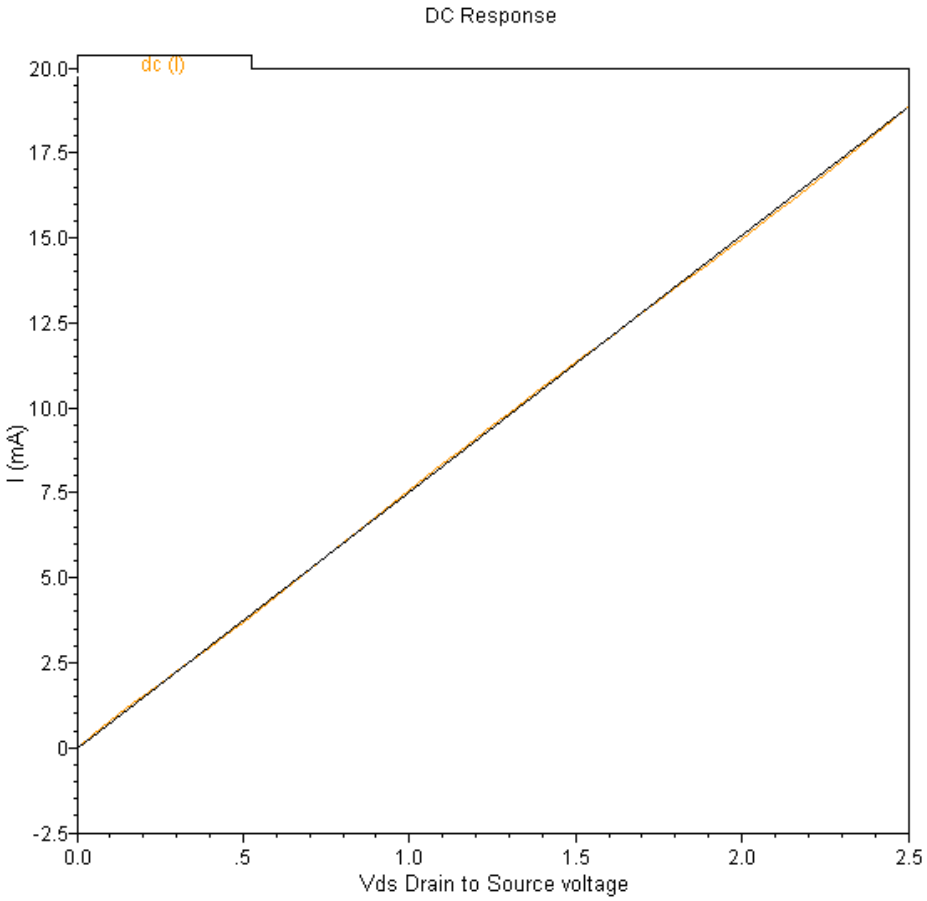


Figure 5.4 Diagram of I-V characteristic of Symmetrical load for voltage upto 2.5 volts when Vc is at 2.5 volts.

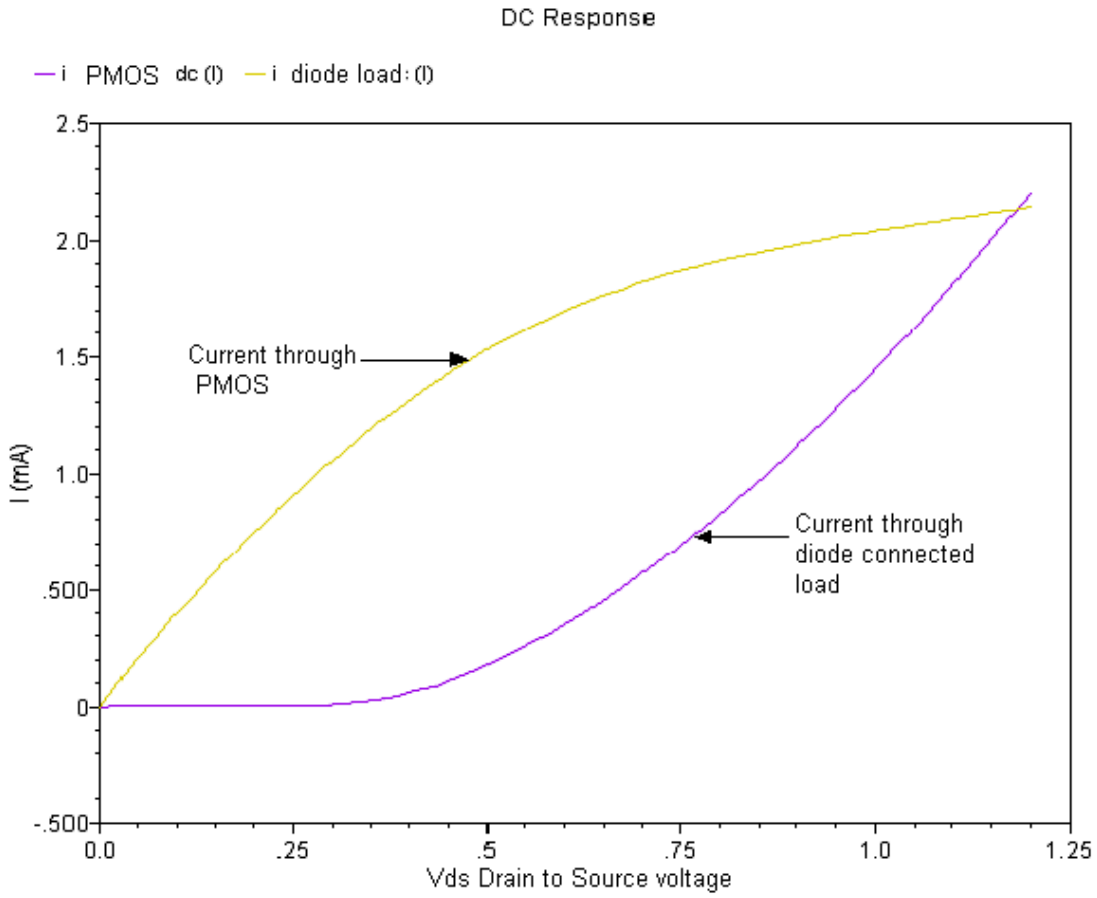


Figure 5.5 The compensation of symmetric load.

The differential configuration is used as an obvious choice because of its common mode noise cancelling properties. In the radiation environment, the circuits are bombarded with high-energy particles and they create a lot of noise in the power supply lines. This type of noises show up as common mode noises in the circuit and the differential structures are good in those environments for noise rejection.

The figure of one differential VCO buffer stage, with symmetric load is shown below.

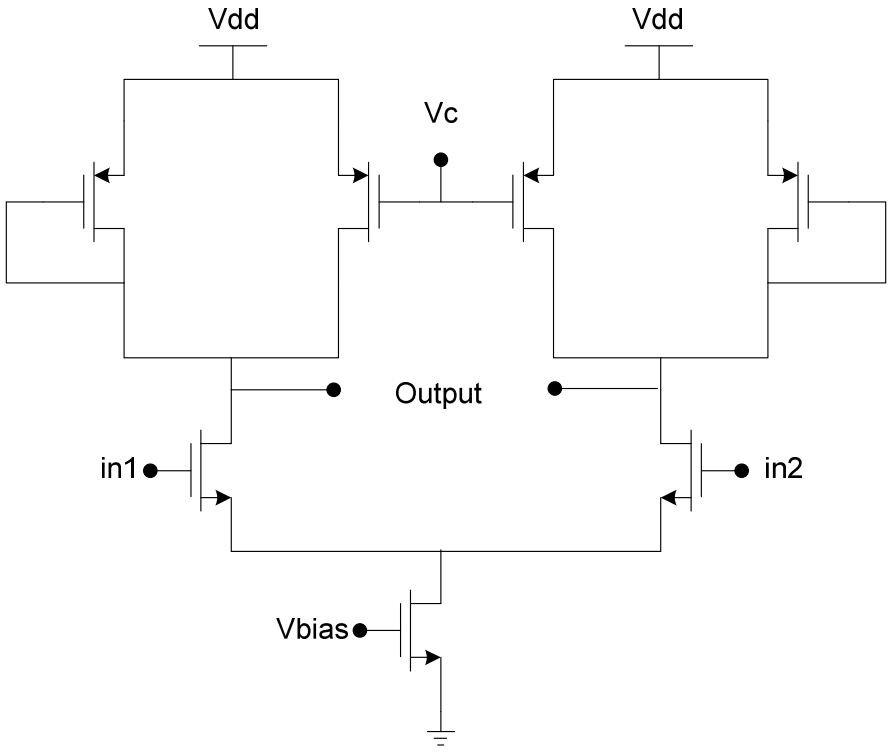


Figure 5.6 VCO buffer stage with symmetric load

The VCO is coupled with another stage called self-bias stage. This stage generates the required operating voltages for the VCO when the circuit behavior changes the self-bias stage will generate the operating voltages depending on the circuit behavior. The self-bias stage gives enough flexibility to the VCO to track any change in the power supply or control voltage.

The VCO should be very robust as is the required criterion for the radiation environment. The radiation effects create enough harm to the devices to make them sway away from their usual behavior with regard to the IV curve and other operating conditions. Thus, it is a requirement for the circuit to tolerate the changes that will happen in a radiation environment. The VCO in our case is thus designed to tolerate these effects and still work effectively. The VCO's tuning range and phase noise are two important parameters that are affected by the radiation effects and thus the VCO designed will be shown to effectively handle these things.

The VCO was designed with fresh transistors and characterized with regard to its tuning range and phase noise. Since, the VCO will be irradiated in harsh environments and a lot of its

parameters would change, the design of the ring oscillator was done considering that the tuning range should be very large. This is done so that the VCO can work properly in the radiation environment around its desired operating point even after the radiation.

The phase noise is another parameter that needs to be characterized well, which has been done with the fresh transistors. The phase noise is a measure of how accurate a VCO is. The lesser the phase noise better is the VCO. The known effect of radiation on the phase noise is that they degrade. Thus, the phase noise of the VCO is supposed to be as low as possible as the radiation effects will certainly degrade its performance.

The change in threshold voltage (v_t) and gate leakage current degrade the phase noise of VCO. Thus, it is required to lower the phase noise as much as possible. There is a need to introduce a few novelties in order for the VCO to work better in the radiation environment.

It has been found that the simple symmetric load VCO fails to oscillate at certain voltages of the controlling voltage producing low tuning range and produce high internal phase noise as can be seen below.

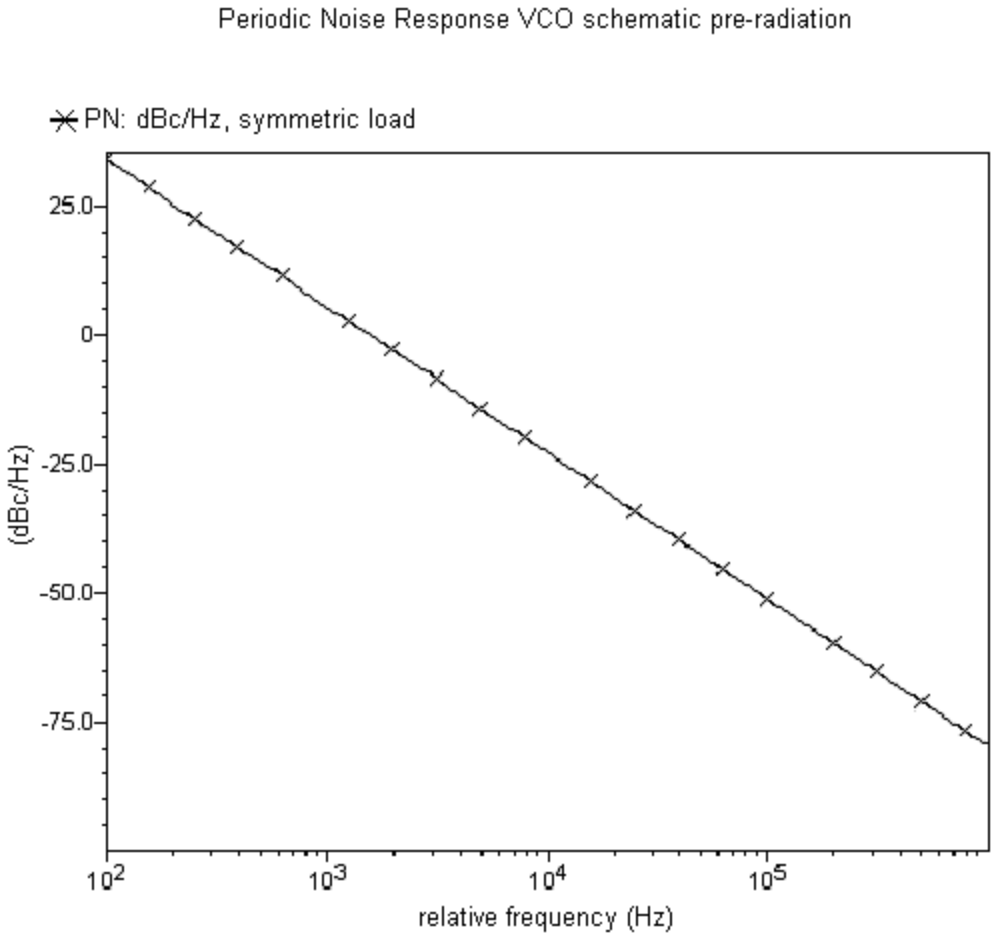


Figure 5.7 Phase noise of the buffer with symmetrical load.

5.1.1 The development of the new architecture for the VCO

It has been noted in the previous section that one critical parameter of the voltage controlled oscillator phase noise is a bit high for the required application. The desired phase noise for the application is -90dBc/Hz at an offset of 1 MHz. The VCO here with symmetrical load exhibits a phase noise of around -80dBc/Hz at an offset of 1 MHz. Thus, it is obvious to reduce the phase noise for the particular structure. Hence is the need for modification. It should be mentioned here that it was pointed out earlier that the differential configuration of the VCO along with the symmetrical load and self-bias configuration helps tremendously under noisy radiation environment. This is particularly true since the self-bias configuration acts well to track

supply and substrate jitter and the symmetric load configuration is essential in building the self-bias PLL. As is the case, it is obvious that the design should not deviate far from the basic self-bias (symmetric load) configuration.

In order to choose an optimum configuration of the VCO that can be employed in a self-bias PLL and still performs superiorly from phase noise perspective (phase noise / jitter arising from the internal circuit and device noises) several architectures of VCO have been studied and simulated. Reference [50] explains its finding about three different VCO configurations, differential VCO with clamped load [49], differential VCO with symmetric load [25] and differential VCO with cross-coupled load [50]. The figure of the three different configurations is given below for illustration purposes. Reference [50] establishes that the phase noise of the cross-coupled load configuration is better than the other types of the VCO, particularly for lower frequency offset values. This is because the cross-coupled load can provide better symmetrical rise and fall time of the output signal and in effect produces a low phase noise by lowering the $1/f^3$ corner frequency.

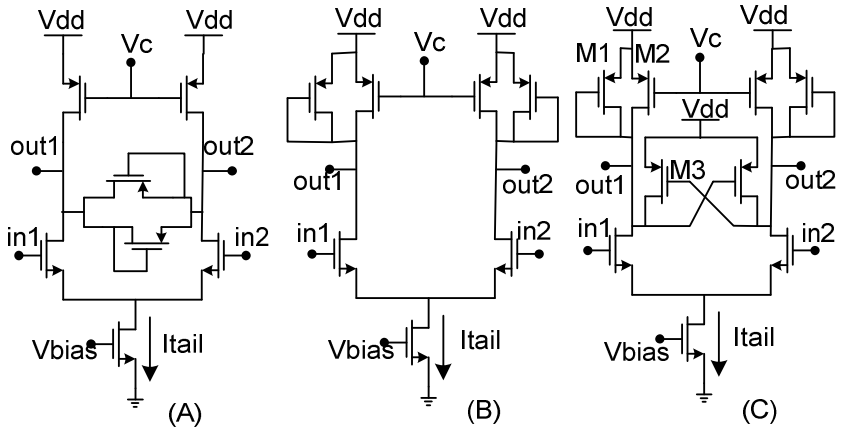


Figure 5.8 Differential buffer cells (a) VCO1, clamped load (b) VCO2, symmetric load (c) VCO3, cross-coupled load

Here, we extended the work by incorporating a clamped load into a cross-coupled design and symmetric load, and hence coming up with a novel load structure for the VCO buffers. The figure for the modified design is given below.

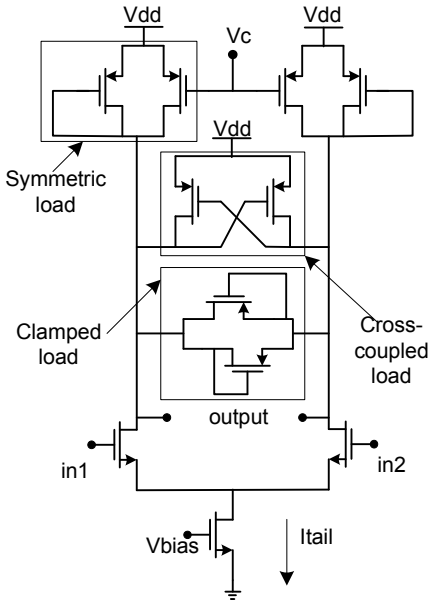


Figure 5.9 Diagram showing the schematic of one buffer stage of the new VCO

As mentioned in the [50] in order to maintain maximum symmetry widths of M1 and M2 should be equal to M3 (in the figure below). The addition of the cross-coupled load makes the rise time and the fall time symmetric as well as helps in faster transition of the output signal. The clamped load decreases the common mode noise by cancelling them. An expression for the phase noise of the VCO has been derived and given below.

The single side band power spectrum due to a white noise current source is given by [51]:

$$L\{f_{off}\} = \frac{\Gamma_{rms}^2}{8 \cdot \pi^2 \cdot f_{off}^2} \cdot \frac{\bar{i_n^2}/\Delta f}{q_{\max}^2} \tag{5.1}$$

In the above equation, Γ_{rms} is the rms value of impulse sensitivity factor (ISF), $\bar{i_n^2}/\Delta f$ is the single side band power spectral density of the noise current source f_{off} is the frequency offset from the carrier. "q_{max}" is the maximum charge stored at the node concerned. "q_{max}" is given by the following equation:

$$q_{\max} = c_{node} \cdot V_{swing} \tag{5.2}$$

In the case of multiple noise sources injecting into the same node, represents the total current noise due to all the sources and is given by the sum of individual noise power spectral densities [52].

For CMOS transistors, the drain current noise (for thermal noise) spectral density is given by:

$$\frac{\bar{i}_n^2}{\Delta f} = 4 \cdot K \cdot T \cdot \gamma \cdot g_{do} = \left(4 \cdot K \cdot T \cdot \gamma \cdot \mu \cdot C_{ox}\right) \cdot \left(\frac{W}{L}\right) \cdot \Delta V \tag{5.3}$$

In the above equation, K is the Boltzmann constant, T is the absolute temperature, γ is the channel noise factor, μ is the mobility, C_{ox} is the gate oxide per unit area, W is the width of the transistor, L is the length of the transistor and ΔV is the gate overdrive voltage.

For differential CMOS ring oscillators the total power dissipation is:

$$P = N \cdot I_{tail} \cdot V_{dd} \tag{5.4}$$

In the above equation, *P* is power consumption, I_{tail} is the current flowing through the current mirror transistor in a differential amplifier, N is the number of stages, V_{dd} is the power supply source.

The fundamental frequency of the oscillation can be given by the following equation:

$$f_0 = \frac{1}{2 \cdot N \cdot t_d} \approx \frac{1}{2 \cdot \eta \cdot N \cdot t_r} \approx \frac{I_{tail}}{2 \cdot \eta \cdot N \cdot q_{\max}} \tag{5.5}$$

In the above equation, f_0 is the fundamental frequency of oscillation of a ring oscillator, *N* is the number of stages of the ring oscillator, t_d is the time delay of each stage, η is proportionality constant, t_r is the rise time, I_{tail} is the current flowing through the current mirror transistor, qmax is the charge at the node concerned given by the equation 5.2.

The total current noise on each single ended node is given by:

$$\frac{\bar{i}_n^2}{\Delta f} = \left(\frac{\bar{i}_n^2}{\Delta f}\right)_{M1} + \left(\frac{\bar{i}_n^2}{\Delta f}\right)_{M2} + \left(\frac{\bar{i}_n^2}{\Delta f}\right)_{M3} + \left(\frac{\bar{i}_n^2}{\Delta f}\right)_{M4} + \left(\frac{\bar{i}_n^2}{\Delta f}\right)_{M5} \tag{5.6}$$

Or,

$$\sum\left(\frac{\overline{i_n}^2}{\Delta f}\right) = 4 \cdot K \cdot T \cdot \gamma \cdot C_{ox} \cdot \left\{\mu_n \cdot \left(\frac{W}{L}\right)_1 \cdot \Delta V_1 + \mu_p \cdot \sum_{i=2}^{5}\left(\frac{W}{L}\right)_i \cdot \Delta V_i\right\} \tag{5.7}$$

In the above equations M_1, M_2, M_3, M_4, M_5, are the transistors in the figure below, μ_n / μ_p are the mobility of the NMOS and the PMOS. The figure below helps us with the illustration.

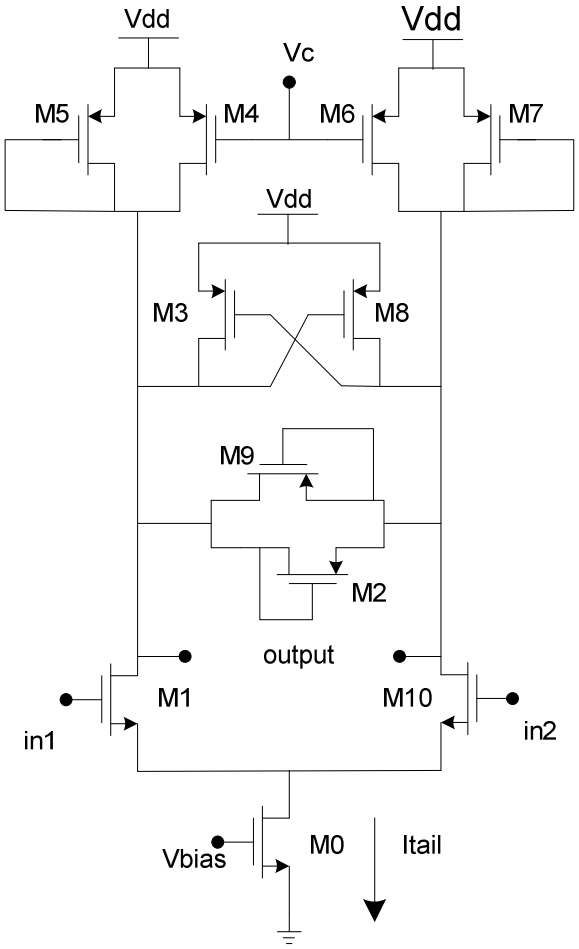


Figure 5.10 Schematic of the buffer stage used in the new VCO showing the transistor names used in the equations.

The phase noise of the circuit in the figure above is given by the following equation which is a modification of the above equation 5.1 for more than a single noise source:

$$L\{f_{off}\} = \frac{\Gamma_{rms}^2}{8 \cdot \pi^2 \cdot f_{off}^2} \cdot \frac{\sum_i \left(\overline{i_n^2} / \Delta f\right)}{q_{\max}^2} \tag{5.8}$$

The rms value of the term, impulse sensitivity factor (Γ_{rms}), is given by the following equation [51], [52]:

$$\Gamma_{rms} = \frac{1}{N^{\frac{1}{5}}} \sqrt{\frac{2 \cdot \pi^2}{3 \cdot \eta^3}} \tag{5.9}$$

Combining the two equations, the following equations have been derived:

$$L_{\min}\{f_{off}\} = \frac{2 \cdot \pi^2}{3 \cdot \eta^3} \cdot \frac{1}{N^{\frac{2}{5}}} \cdot \frac{1}{8 \cdot \pi^2 \cdot f_{off}^2} \cdot \frac{\sum \left(i_n^2 / \Delta f \right)}{c_{node}^2 \cdot V_{\max}^2} \tag{5.10}$$

$$L_{\min}\{f_{off}\} = \frac{1}{12 \cdot \eta^3} \cdot \frac{1}{N^{\frac{2}{5}}} \cdot \frac{1}{f_{off}^2} \cdot \frac{\sum \left(i_n^2 / \Delta f \right)}{c_{node}^2 \cdot V_{\max}^2} \tag{5.11}$$

The above equation gives the lower bound of the phase noise provided by the differential VCO used in the PLL. It can be seen from the above equation that the phase noise reduces as the node capacitance increases. In addition, the maximum swing at the output nodes will also reduce the phase noise. The above equation gives the idea that if the maximum transition frequency can be improved while increasing the node capacitance, the phase noise can be reduced.

The phase noise equation provided above is due to internal thermal noise from the transistors and does not account for the phase noise for external noises. The increase in nodal capacitance will make the design vulnerable in picking up external noises. Thus, the symmetric load differential buffer stages have been chosen for the VCO, which can track the supply/substrate noises. Equation (5.7) can be extended to include flicker ($1/f$) noise and other noises produced by the transistors, by including their contributions in the noise current spectral density in (5.7).

The simulation results of the phase noise for the different configurations are shown below. The channel lengths have been varied to keep the frequency constant.

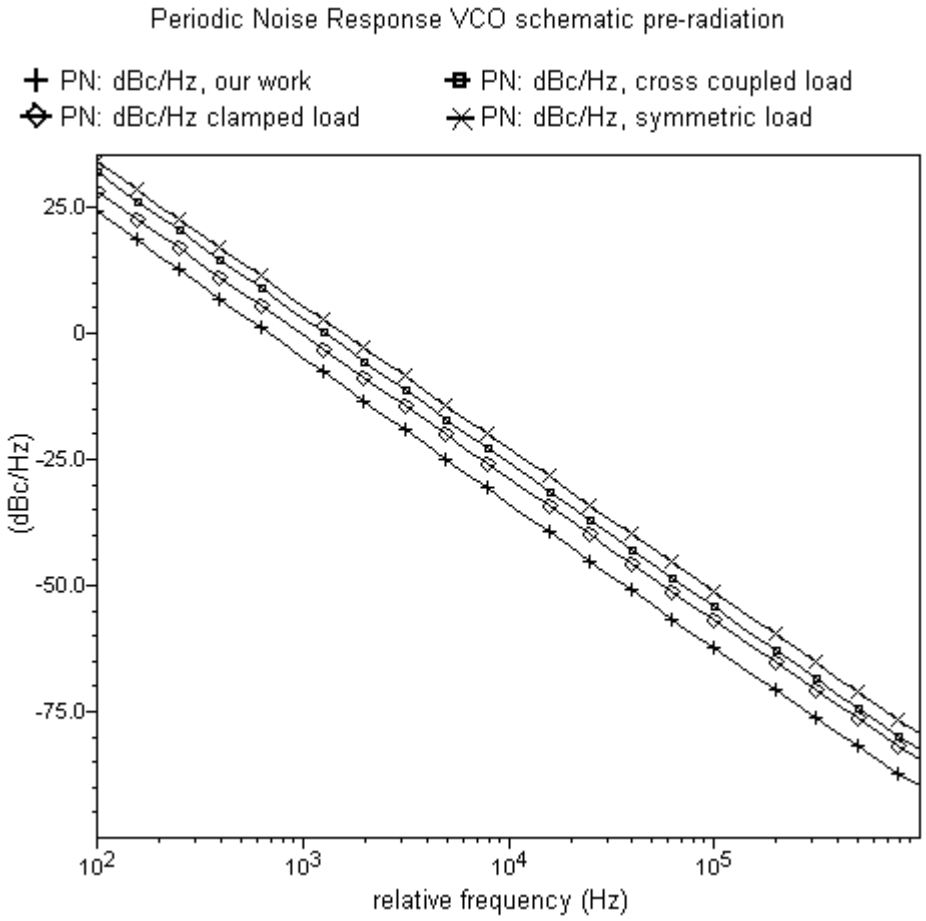


Figure 5.11 Comparison of phase noise generated by different VCOs

The above plots for the phase noise show that the new modification gives a better performance as far as the phase noise (contributed by internal noises) is concerned. There is an improvement of the phase noise for moving from the simple symmetric load design to the combination of cross-coupled and clamped load by more than 10 dB.

As can be seen from the plot the phase noise of the simple symmetric load circuit is around -80dBc/Hz at an offset of 1 MHz and the phase noise of the new modified circuit is around -93dBc/Hz at an offset of 1 MHz. There has been a considerable improvement in the overall phase noise from the previous design, along with the improvement around lower frequency offsets.

During radiation, because of several mentioned phenomena, the VCO (& hence the

PLL) may deviate from the operating frequency. Thus, a very wide range VCO is needed in order for the PLL to work properly. The developed VCO with a novel load structure in each of its buffer stages (delay cells) as shown in Fig. 5.9. The new load structure consisting of symmetric load in conjunction of cross-coupled load [50] and clamped load [49] improves the tuning range in two ways.

(i) Maximization of single-ended output voltage swing. Typically, wide-band VCO's output voltage swing changes with control voltage; and the VCO may fail to sustain oscillation due to small swing at certain control voltages. (For example, with the increase of V_c, output voltage swing of the symmetric load VCO in [25] drops.) Therefore, enlarging output voltage swing helps with frequency tuning range, which is achieved by large I_{tail} and the usage of cross-coupled load together with symmetric load in Fig. 5.9. Specifically, large I_{tail} is ensured by increasing the aspect ratio of transistor M0 (Fig. 5.10); and it enhances the linearity of buffer stages in the VCO and output voltage swing. At the same time, the usage of cross-coupled load exploits positive feedback to make the voltage swing approach its asymptotic levels, which are dictated by V_c and V_{dd}.

(ii) Improvement of linearity of VCO gain K_{VCO}, to avoid frequency saturation when control voltage approaches zero. The clamped load in Fig. 3 increases the linearity of each buffer stage by reducing the even harmonics of the VCO output, which in turn makes K_{VCO} more linear [49].

The plot is given in Figure 5.13. Pre radiation tuning range for our VCO is from 0.741 GHz to 3.497 GHz.

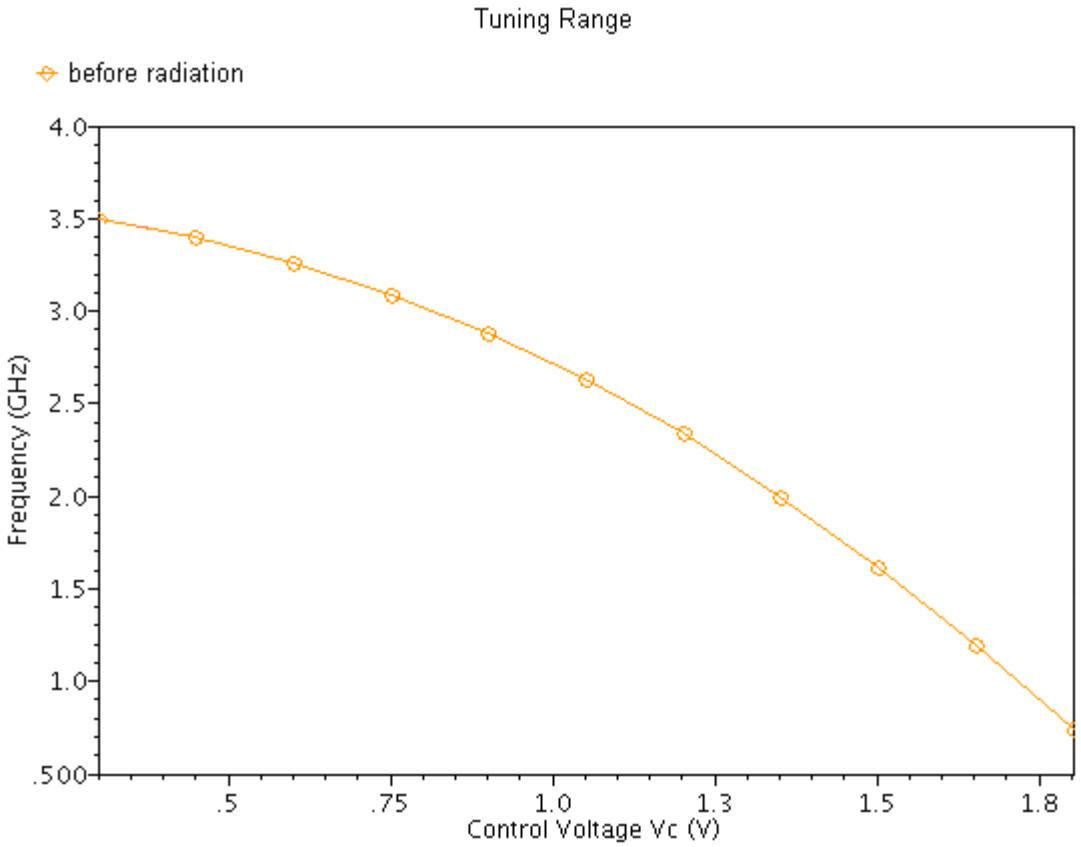


Figure 5.12 Tuning Range of the VCO

The layout of one buffer stage of the VCO is shown below.

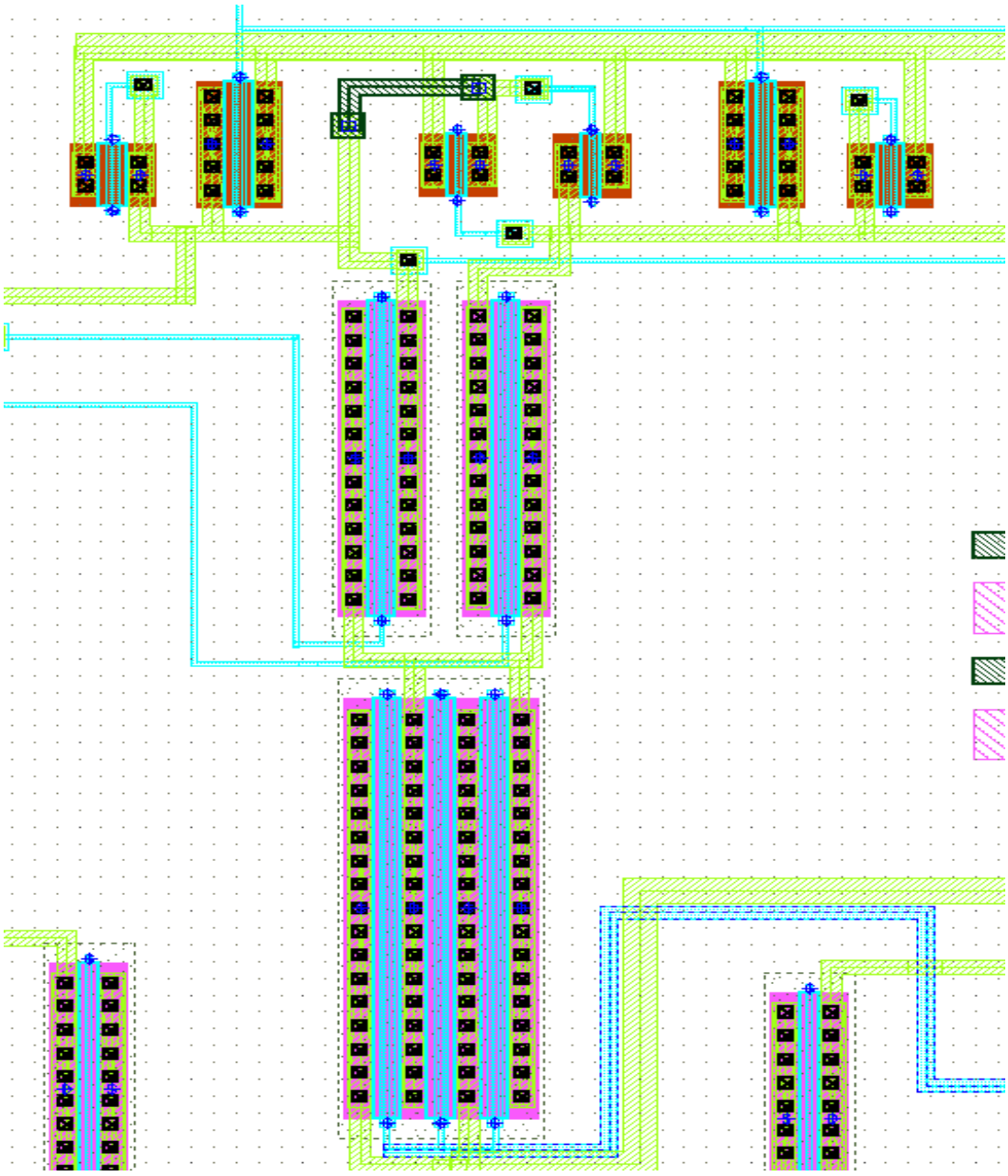


Figure 5.13 The layout of the three buffer stages of the ring oscillator

The VCO is the most important block of the PLL as it generates the frequency required. Thus, optimization of the VCO is an important step to building a PLL.

5.2 Self Bias Circuit

The self-bias circuit generates voltage levels for V_{c1}, the control voltage for the VCO buffer stage and V_{bias} the voltage required for driving the current controlling transistors in each buffer. The basic functioning of the self-bias stage circuit is described below. A half buffer stage circuit is used in conjunction with a differential stage amplifier to construct the self-bias stage. A simple configuration of the self-bias stage is illustrated below and will be referred to explain its functioning. The half buffer stage is constructed by using one leg (half) of the buffer stage used in the ring oscillator. The transistor dimensions are either multiple or fractional ratio of the transistor dimensions used in the ring oscillator. This is important to keep the ratio of currents flowing through the half buffer and the buffer stage in the ring oscillator rational. Keeping the transistor dimensions in such a way will help in monitoring the control voltage of the VCO and the output swing of the ring oscillator (as mentioned above). The output of the half buffer stage, which is incidentally the output of the self-bias stage, is constantly monitored, as it is fedback to the amplifier stage. If the control voltage changes for any reason, it changes the current flowing through the half buffer stage. The change in current changes the gain of the stage and hence changes the output voltage of the stage. This new voltage is referred against the positive input of the amplifier, which is also V_c. The amplifier then changes its output, which is fedback to V_{bias} terminal of the half buffer stage. Therefore, any change in the control voltage is monitored well and tracked, which is reflected well in the corresponding V_{bias} voltage. Again, if there is any change in the power supply voltage, the current through the half buffer stage changes. This changes the output voltage of the stage. This goes back to the amplifier, which is referred to the original control voltage. The amplifier then outputs a new V_{bias} voltage from the error voltage produced to change the current flowing through the half buffer stage, in order to correct the control voltage. Hence, the self-bias stage tracks the changes in both the control voltage and the power supply voltage and make necessary corrections in the circuit.

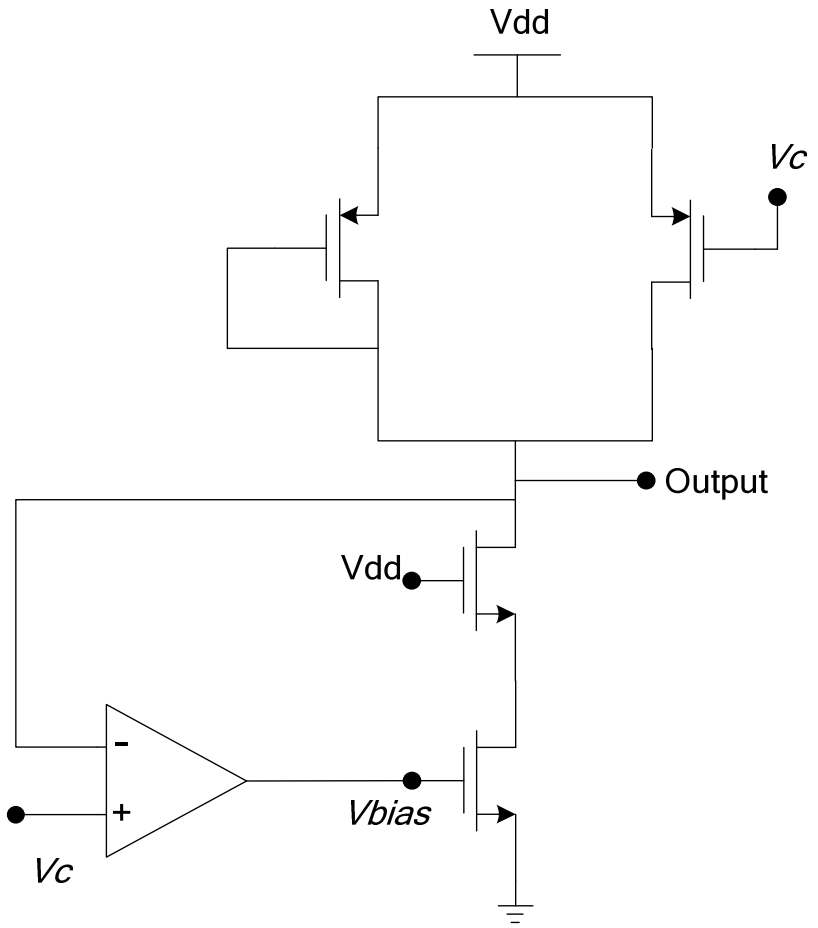


Figure 5.14 Schematic describing the basic functionality of the self-bias circuit.

The self-bias circuit shown above is for illustration purposes only. This is a simpler version of the original circuit to be used in the phase locked loop. The original schematic that has been designed is shown below. The circuit shows an implementation of the differential amplifier stage in terms of transistor level circuits. In addition, the circuit has current mirror and amplifier stage. Further, it is equipped with another half buffer circuit. The last stage used is for isolation purposes and has a true diode connected stage as load and it can smooth out any ripple that is generated in the other part of the circuit.

In this work, two self-bias circuit stages have been employed. The decision to employ two stages of the self-bias circuits stemmed from the fact that in a noisy environment if there are any undesirable changes in the control voltage or ripples, they will be filtered out at the output of

the second self-bias stage. This is the case as the final stages of the self-bias circuit provide isolation. The undesirable side effect that arises from the use of two stages is the delay introduced by the stage and decreasing the loop bandwidth. The decreased loop bandwidth means worse phase noise of the PLL. However, the frequency response of the self-bias circuit is kept at the operating frequency of the VCO. Under this circumstance, the stage delay offered by the second stage is negligible compared to the loop time period.

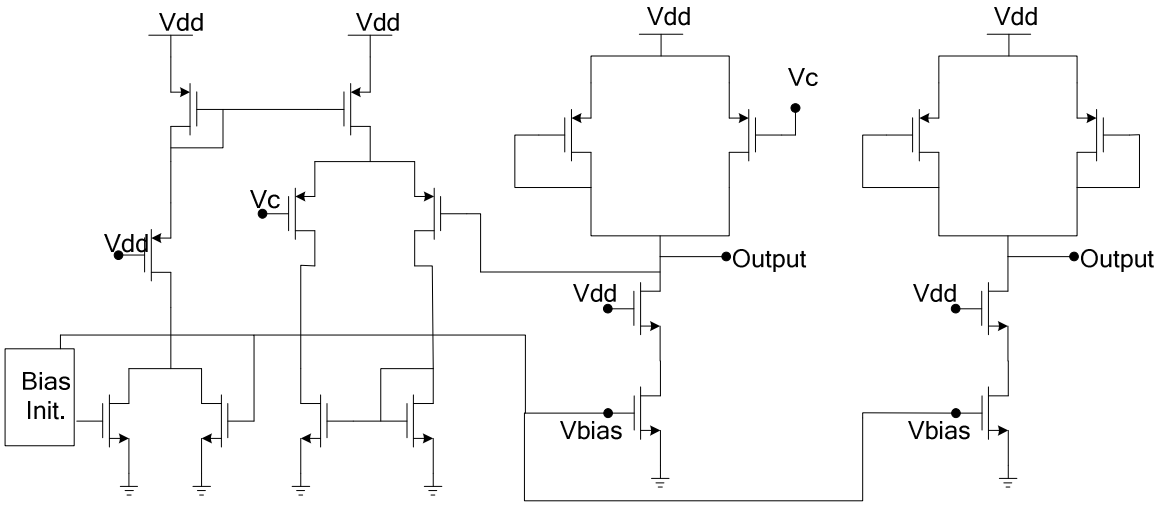


Figure 5.15 Schematic of the original self bias circuit.

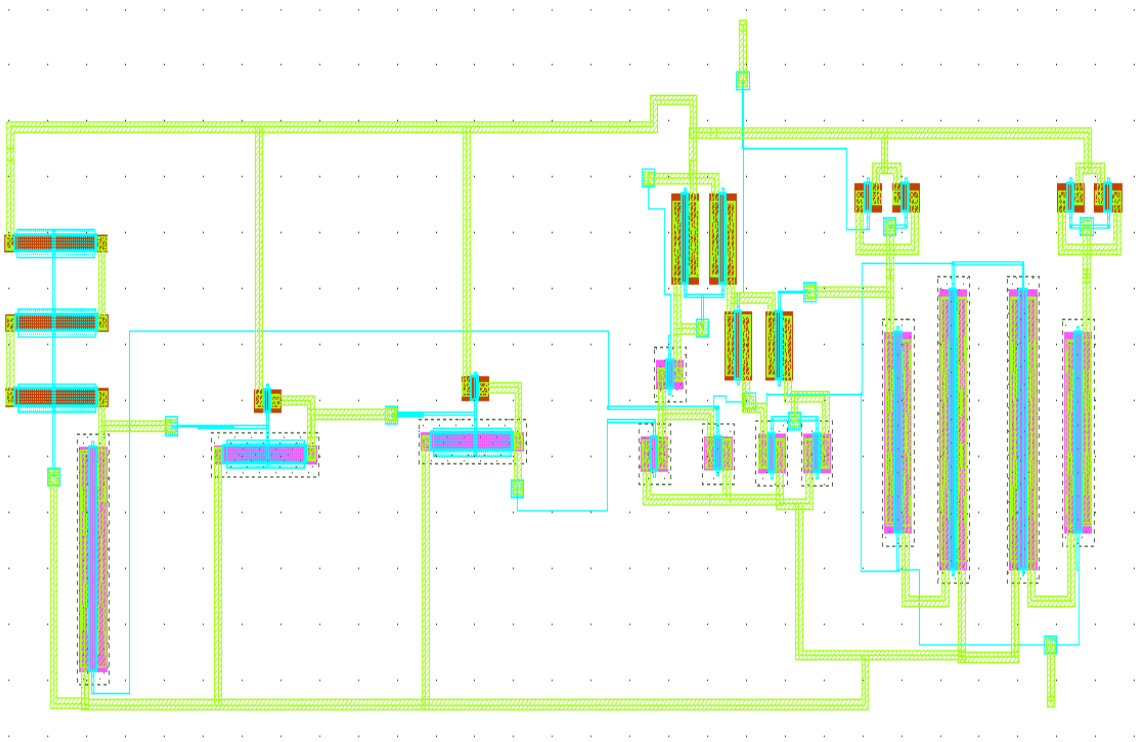


Figure 5.16 Layout of 2 self bias stages

5.3 Voltage level shifter

The level shifter (differential input single ended output) stage is based on the circuit of [25]. It not only converts the differential output of the VCO to single ended one, but also provides rail-to-rail output for the next stage. Its biasing is also controlled by the self-biased section. For proper functioning of the asynchronous dividers, which follow this stage, it is important to provide rail-to-rail swing of the output. Under radiation environment due to threshold voltage variation and mobility degradation the output may not reach rail-to-rail for high frequency signals. So, the differential to single output stage has been designed to have multiple stages to boost the output from rail-to-rail.

Block diagram of voltage level shifter is shown below.

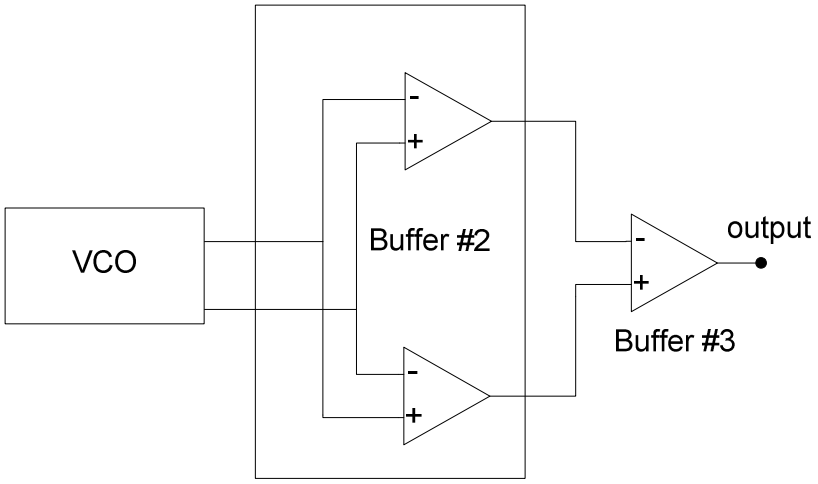


Figure 5.17 block diagram used in [25]. Diagram showing the arrangements of buffers (level #2 and #3) to convert differential output signal from the VCO to single ended output that will be fed to the dividers. This also gives rail-to-rail output.

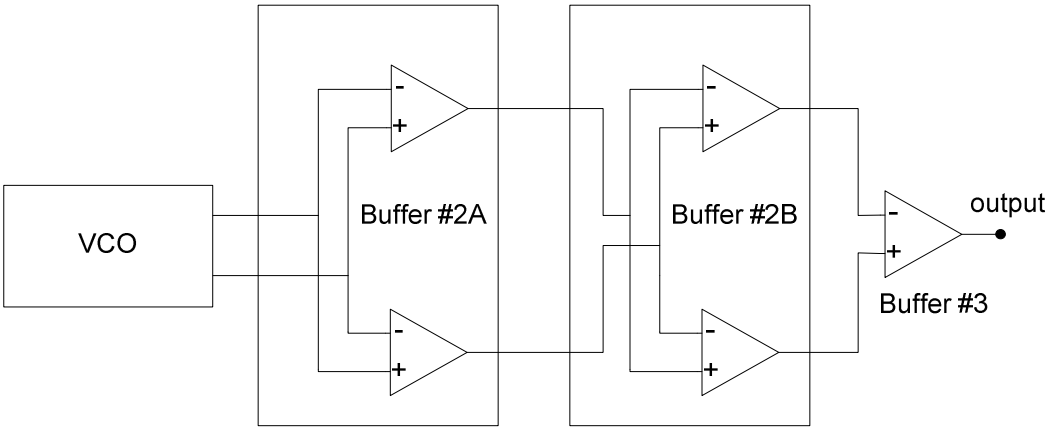


Figure 5.18 Introduction of two stages of buffer

The level-shifter buffer stage has been designed using multiple buffer stages. The idea of using two buffer stages is to provide enough gain so that, even under duress, because of the change in threshold voltage due to radiation effect, the circuit provides rail-to-rail voltage swing. The above figure shows the necessary modifications for the radiation environment. The circuit level implementations of the level shifter stages and their layouts are given below.

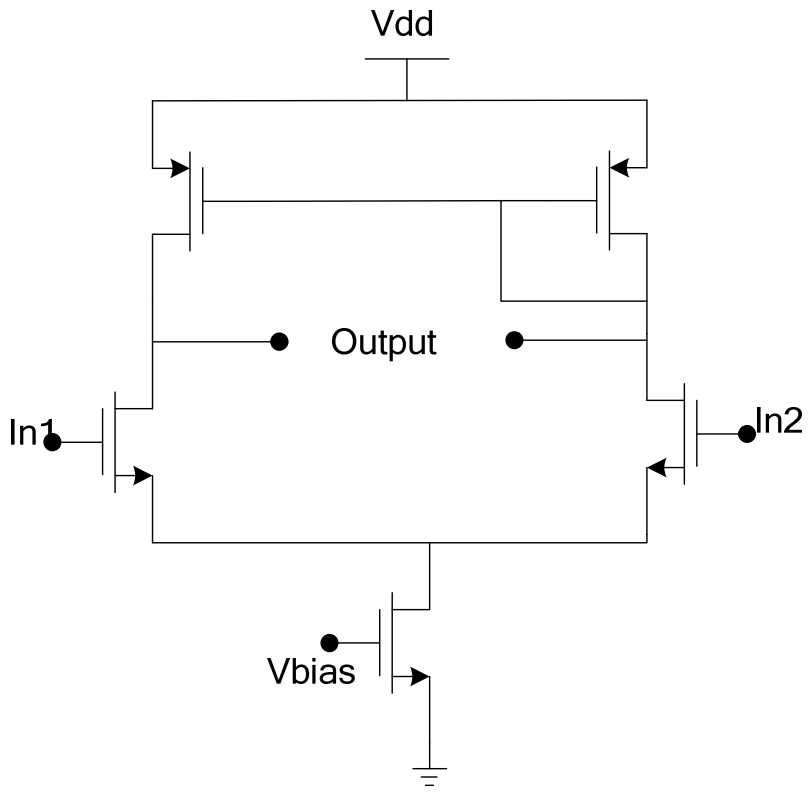


Figure 5.19 Buffer #2A: The diagram showing the schematic of buffer #2A.

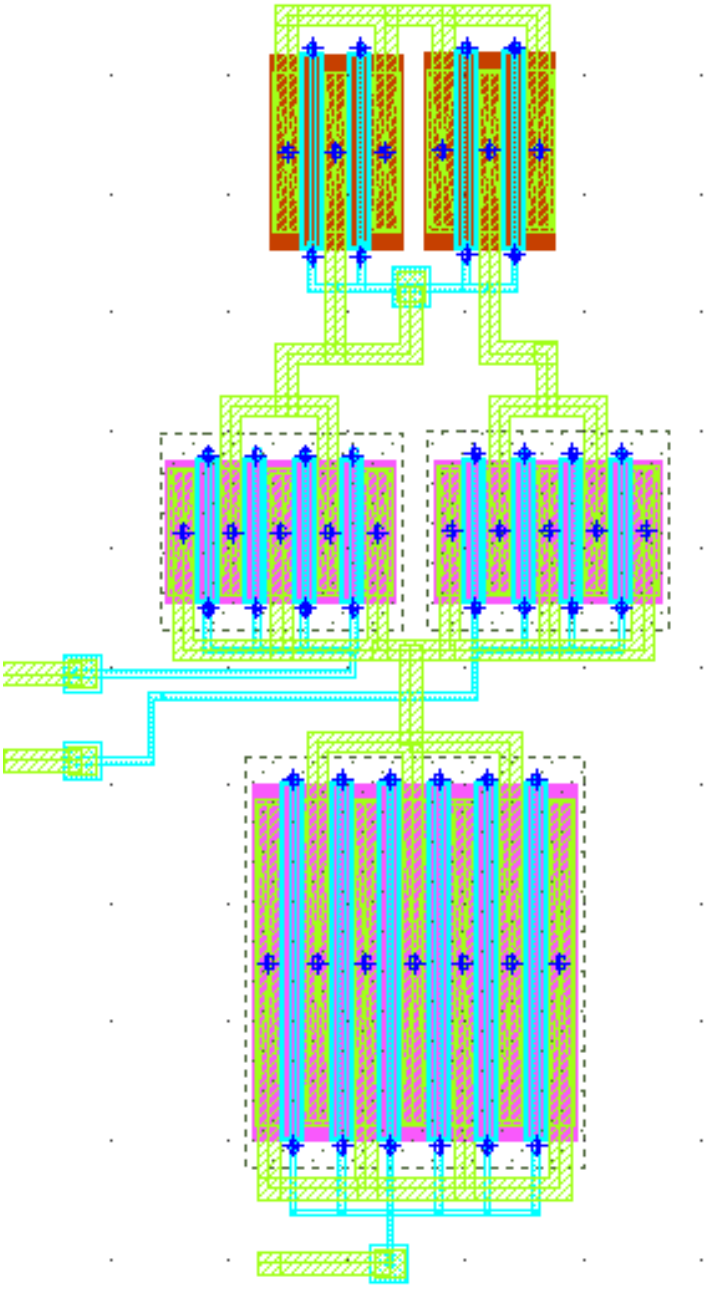


Figure 5.20 Layout of buffer #2A

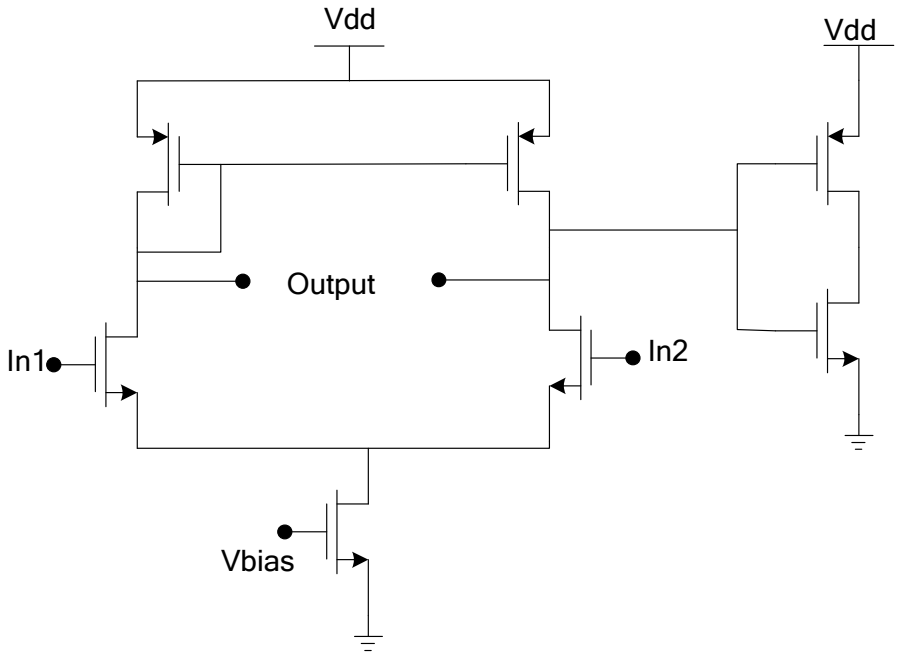


Figure 5.21 Buffer #2B: The diagram showing the schematic of buffer #2B.

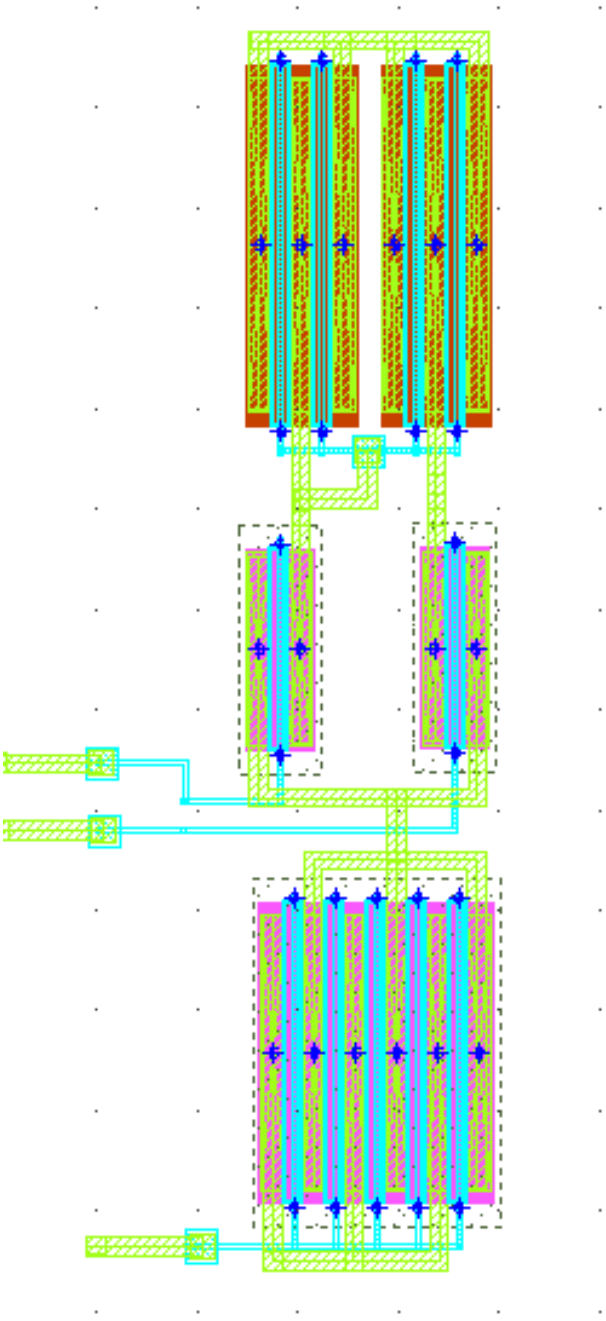


Figure 5.22 Layout of buffer #2B.

5.4 Divider circuits

The VCO is supposed to generate a nominal frequency of 2.5 GHz. The input frequency signal that is supposed to be referred by the phase frequency detector is around 78 MHz. Thus, the output signal of the VCO has to be divided by 32 in order to achieve the frequency which can be referred to the input signal. The dividers used are asynchronous dividers. There are five divided by two dividers. The choice of using asynchronous dividers stemmed from the fact that due to radiation effects, the dividers have to wither a lot of performance, or sway from their optimum-performing region and synchronous dividers are not reliable enough to perform under these circumstances. In addition, for the proper functioning of the PLL, the dividers should be able to process the maximum frequency of the available signal from the output of the VCO.

Each “divided by two” circuit is made of True Single Phase Clock (TSPC) D-flip-flop [53] type dividers. The choice of TSPC dividers are also influenced by the fact that at high frequency there is clock skew especially when two different phases of clock are used for circuit operation. Since, TSPC design is chosen there is no worry about the clock skew, which is usually predominant in the GHz regime. In addition, TSPC dividers have low “clock to Q” propagation time and are easy for implementation. However, TSPC dividers are not as robust as the complementary logic gates as in the TSPC designs not all the nodes reach rail voltages. This is a concern as due to radiation effects the logic designs may tend to move away from their originally designed operating point. Thus, it is important that the preceding stage maintains rail to rail voltage swing in order to ensure that the input voltage of the dividers stay at more or less constant voltage even after radiation exposure. The TSPC dividers are ratioed logic so designing them for high frequency is critical. Hence, they are optimized for the operating frequency range. The other advantages of the TSPC dividers are that they take less area. This is because the number of logic stages required in a TSPC divider to implement a logic are less than other types of D flip-flops e.g. master slave configuration type D flip-flops.

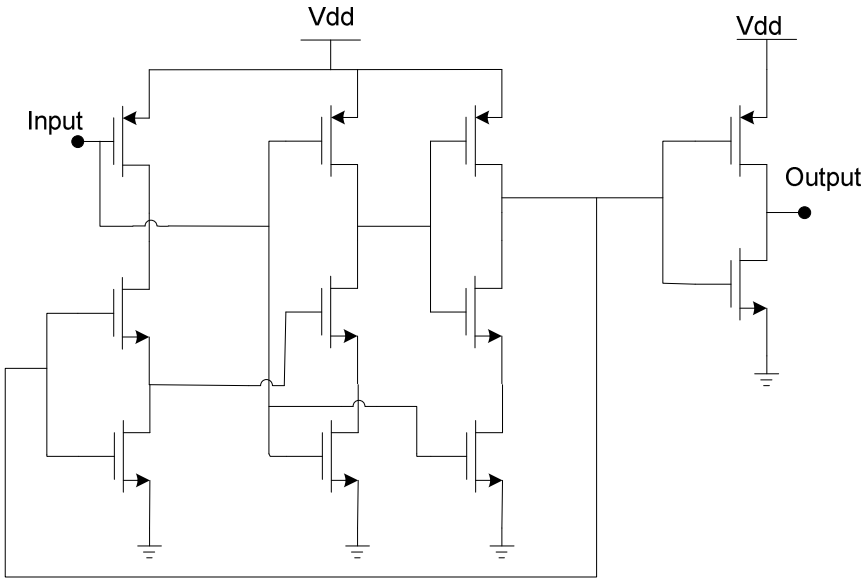


Figure 5.23 Figure of schematic of divider

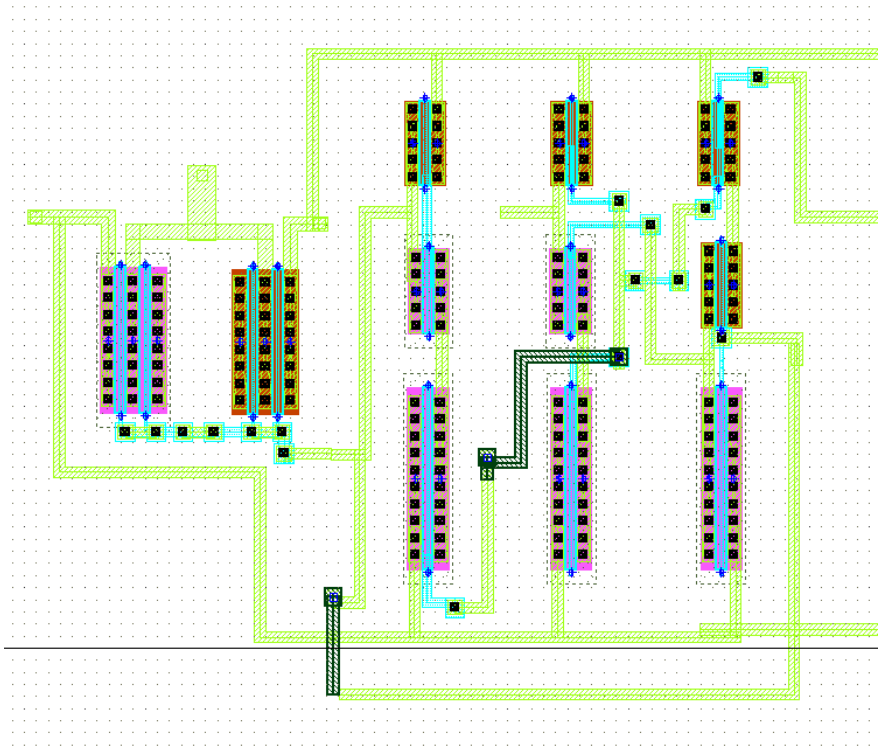


Figure 5.24 Layout of D flip flop employed in the divider

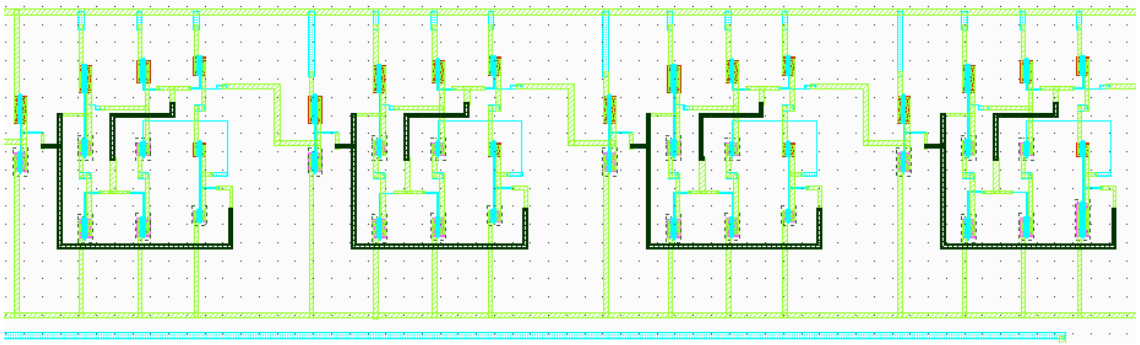


Figure 5.25 Layout of the dividers.

5.4.1 Implementation of the Dividers

The dividers are TSPC dividers, which have three logic levels. The first divider used is supposed to divide a frequency of more than 3 GHz depending upon the frequency generated by the voltage-controlled oscillator. Thus, the dividers should be designed to accommodate frequencies up to 3.5 GHz, just in case. In order for the divider to work at 3.5 GHz, it has to be designed in such a way that it satisfies the following equation:

$$T > T_{c\text{-}k} + T_{su} + jitter \tag{5.12}$$

In the above equation, T is the time period of the incoming clock frequency, which is the data input signal in our case as the D flip-flop is being used as a divider. T_{c_k} is the time required for the flop to produce the output signal from the input signal once the clock is available. In other words, the time required for a change in signal to flow at the output once the clock edge triggers the flop transparent. T_{su} is the set up time for the flop or it is the time required for the data at the input to stay constant before the clock edge triggers the flop transparent. Jitter is the uncertainty in the clock transitions. Operation of the divider is shown below for 3.5 GHz frequency.

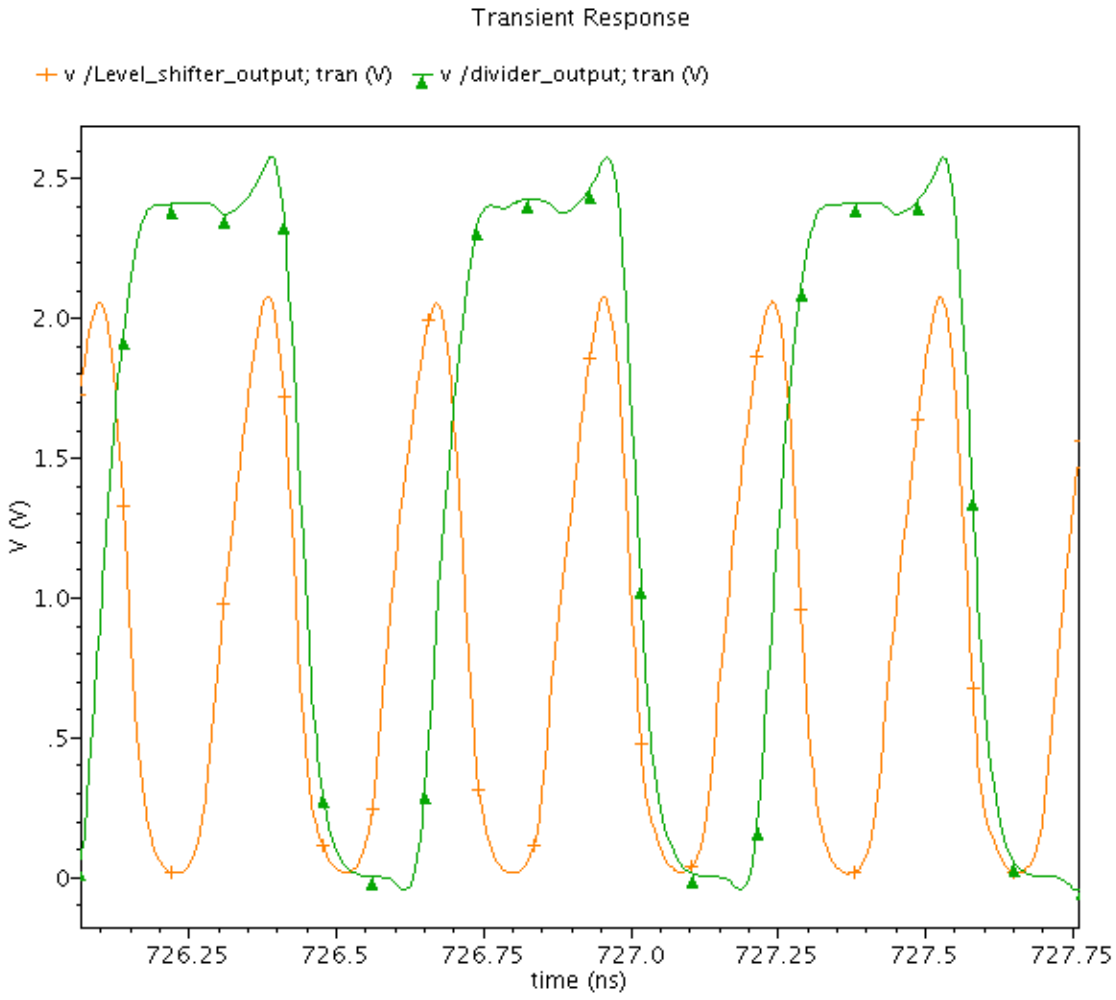


Figure 5.26 Performance of the divider at 3.5 GHz.

5.5 Phase / Frequency Detector

The basic inverter circuit is shown in Figure 5.27 [1]. It can be seen, that [1] has presented the transfer curve of the basic inverter after irradiation. The most important changes are the switch point, the decreased output rail voltage, and the increased leakage current. If radiation becomes strong enough, proper PFD operation may fail. Several solutions have been proposed by J. P. Colinge in [1]. When V_{IN} is low and NMOS cuts off, it may turn back on during irradiation. The inverter connects between V_{IN} and the NMOS source terminal. When V_{IN} is low, the NMOS source terminal becomes high and V_{gs} becomes negative. The main idea is to

maintain the output voltage by making V_{gs} negative when the NMOS cuts off. Figure 5.28 shows the radiation hardened inverter circuit.

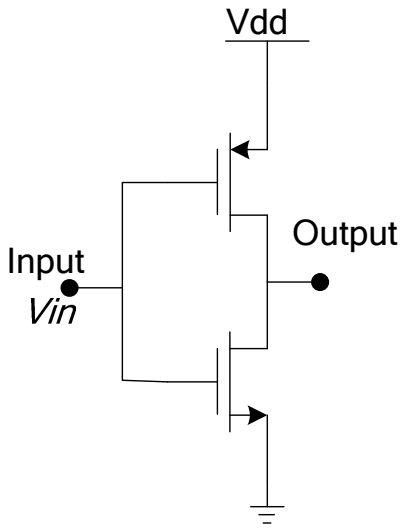


Figure 5.27 Standard Inverter Circuit [1]

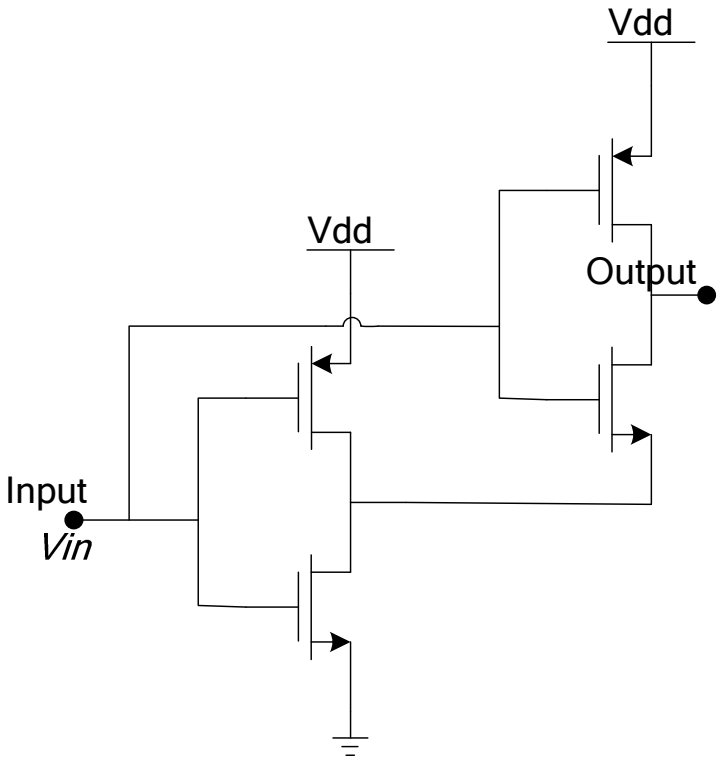


Figure 5.28 Radiation Hardened Inverter Circuit [1]

The basic phase frequency detector circuit is shown in Figure 5.29 [1]. In order to redesign the circuit for radiation resistance, the above radiation hardened inverter circuit is implemented in each PFD gate. An additional inverter is also added for each NMOS to radiation harden the NAND gate and AND-NOR gate. Figure 5.29 shows the schematic of the radiation hardened phase frequency detector in this phase locked loop.

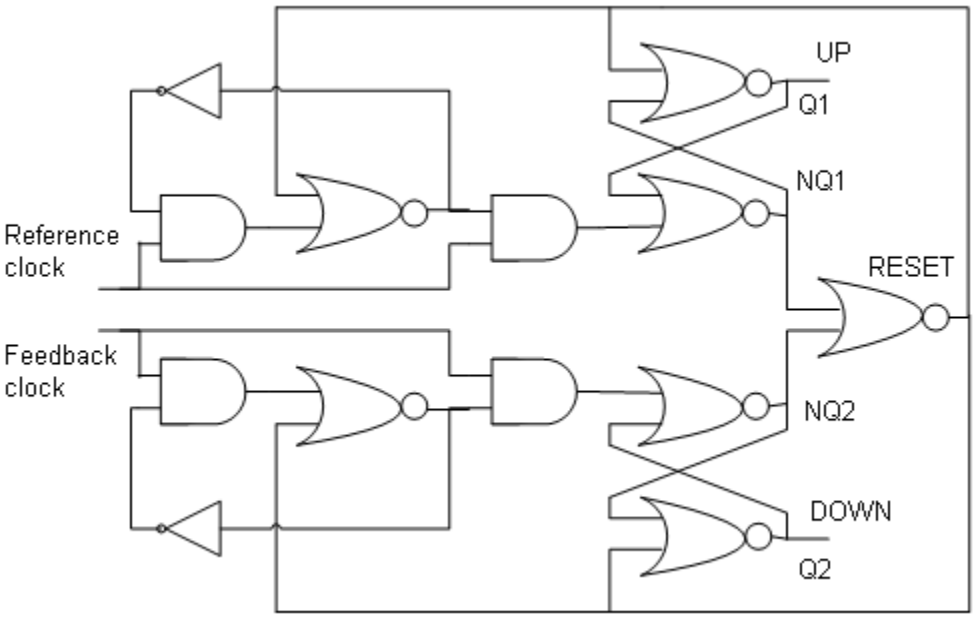


Figure 5.29 Phase/Frequency Detector circuit [1].

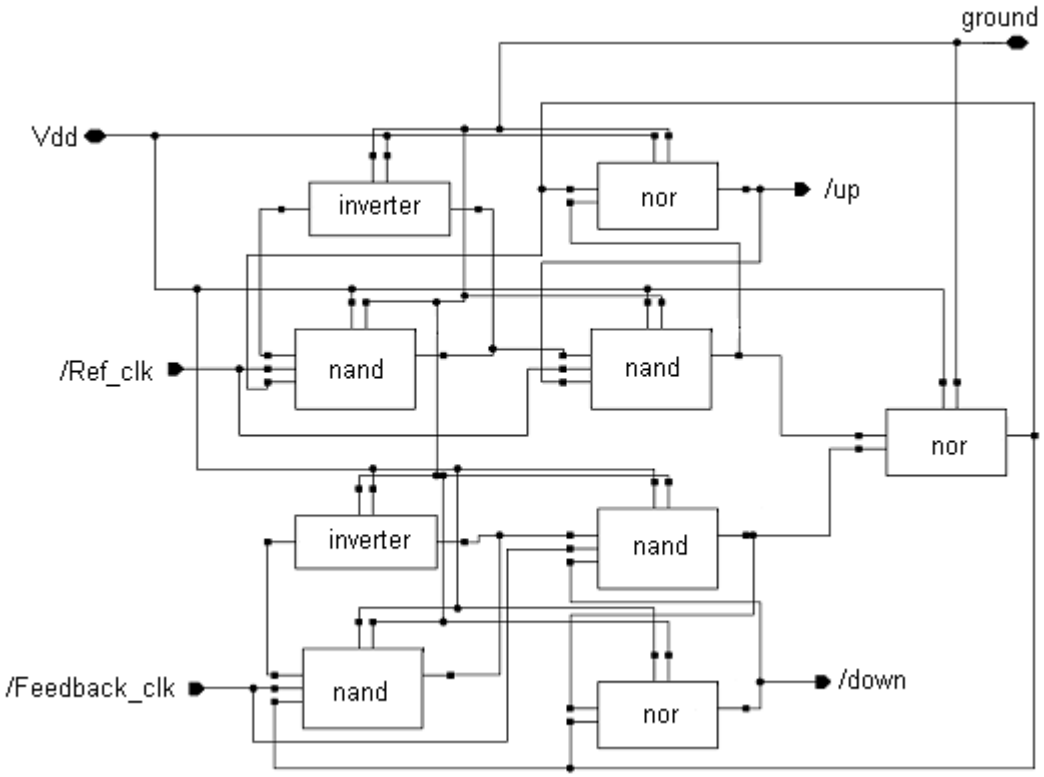


Figure 5.30 Schematic of Phase/Frequency Detector circuit in Cadence.

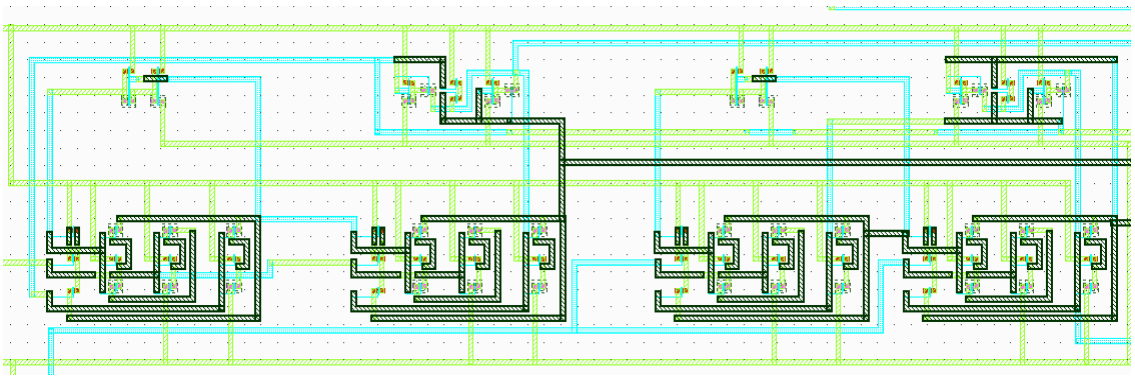


Figure 5.31 Layout of phase frequency detector.

5.6 Charge Pump

The charge pumps used are zero-offset charge pump used in [25]. There are two charge pumps used in the PLL. Both the charge pumps are same in design. One charge pump provides current to the capacitor and the other charge pump provides current to the output buffer stage of the self-bias circuit, which acts as the resistor of the loop filter.

Maneatis's self-biased zero offset charge pump design was used which adds two inverters to the UP bar and DOWN bar at the charge pump inputs [25]. Figure 5.32 is the zero offset charge pump schematic. The UP and DOWN output signals from PFD have single ended outputs. Charge will be transferred from or to the loop filter connected to the output when the UP input or DOWN input is switched high respectively.

5.6.1 Linear Charge Pump

To obtain a linear charge pump that operates without a dead-zone the charge pump was designed with devices that have non-minimum channel lengths. This design choice has several implications. First, the problem of dead-zone appearing from the non-linearity of the charge pump can be avoided by using non-minimum channel length devices. Second, non-minimum channel lengths will slower down the speed of operation of the charge pump circuit. Therefore, optimum design lengths for the channel should be chosen. Third, because of an increase in the length of the channels of the devices secondary effects such as non-quasi-static effects can appear. These effects are very pronounced at devices in processes with minimum lengths less than 100nm.

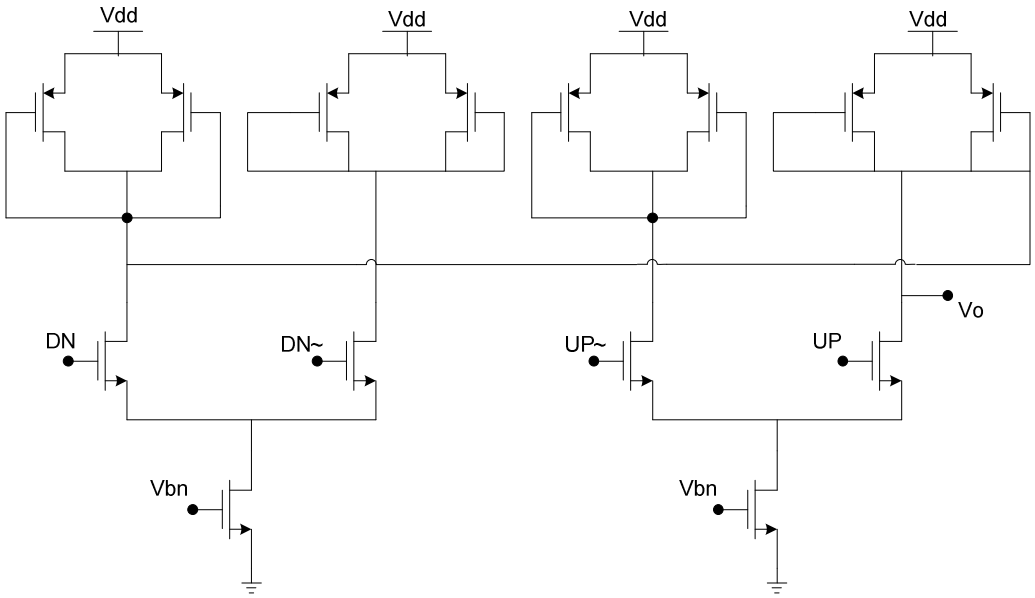


Figure 5.32 Schematic of Maneatis Charge Pump.

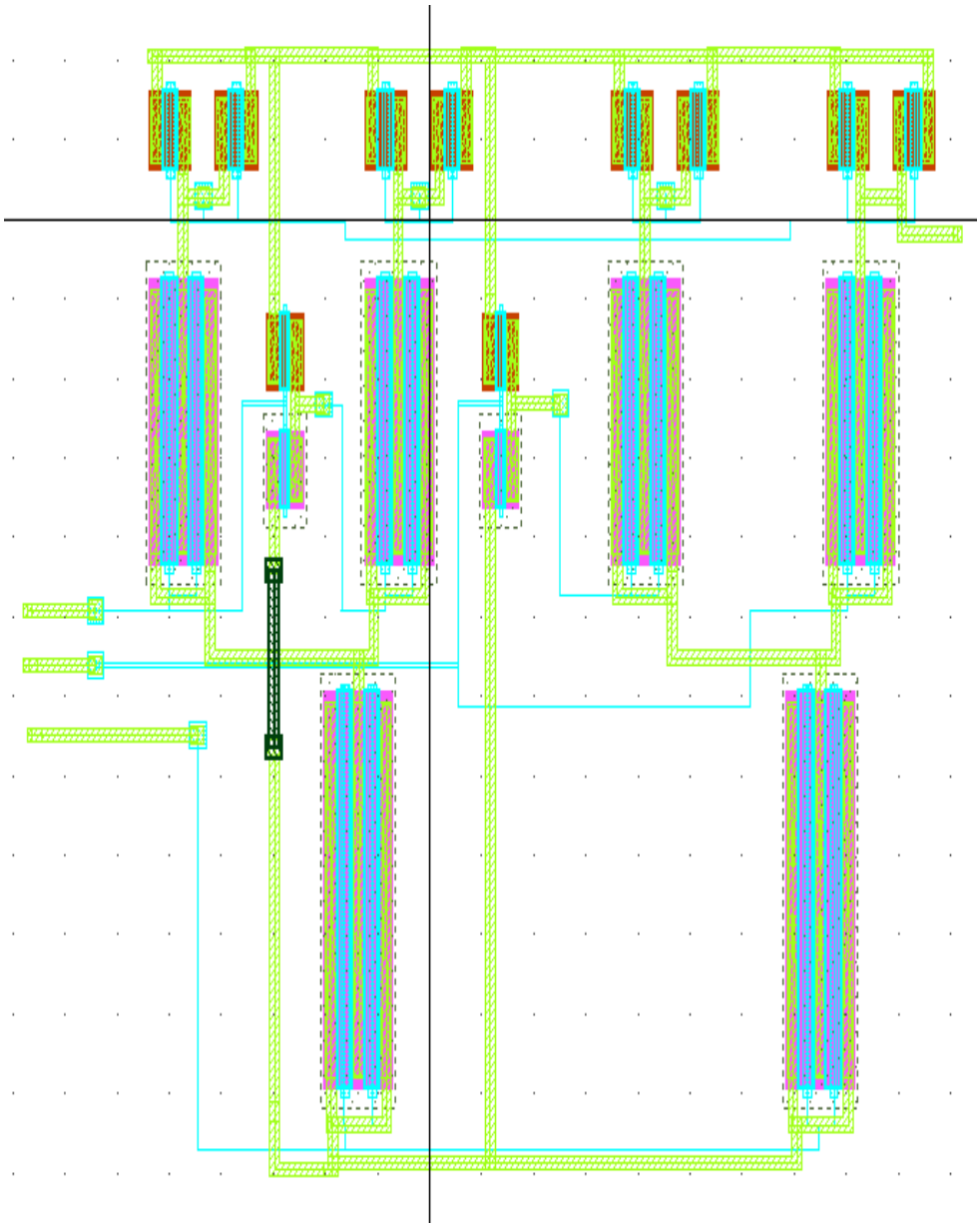


Figure 5.33 Layout of charge pump.

5.6.2 Phase/ Frequency detector - Charge Pump performance

The response of phase frequency detector is shown in Figure 5.34, 5.35 and 5.36. The reference clock frequency is 78.125 MHz. Figure 5.34, 5.35 and 5.36 show the reference clock lags the feedback clock, the reference clock leads the feedback clock, and both clocks are in phase respectively in pre-radiation simulation.

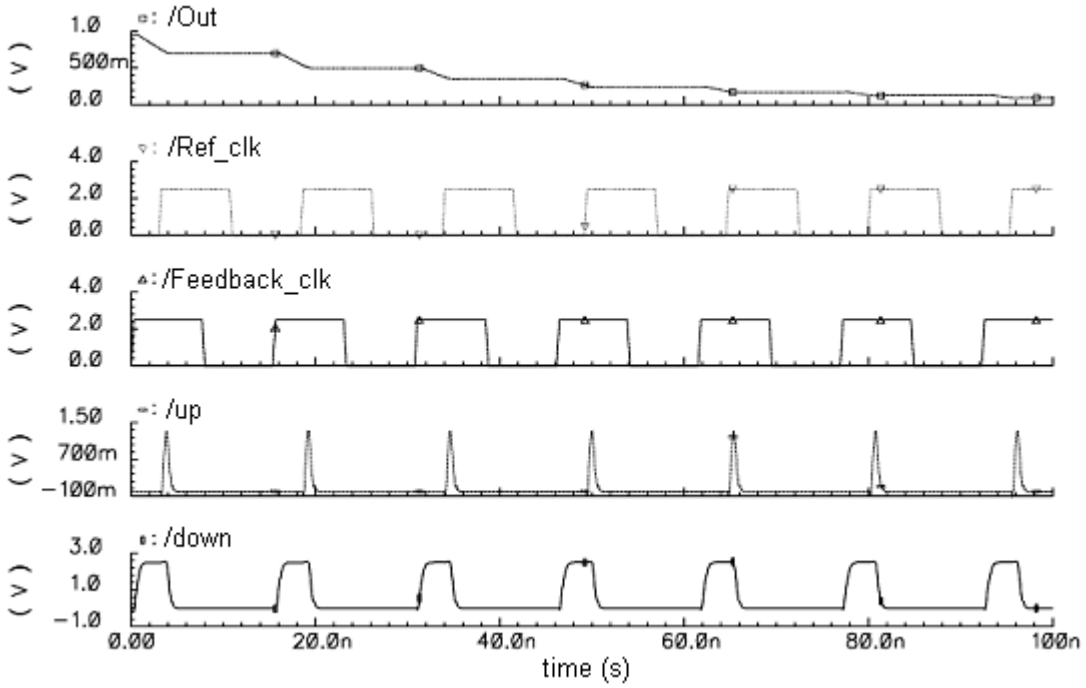


Figure 5.34 PFD and charge pump output when reference lags feedback clock in pre-radiation simulation.

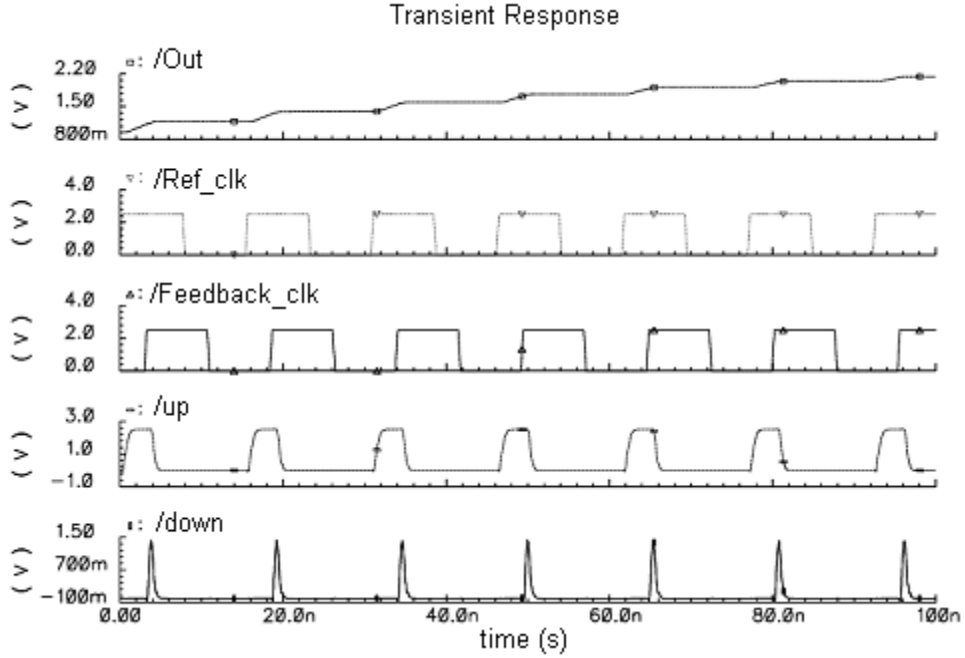


Figure 5.35 PFD and charge pump output when reference leads feedback clock in pre-radiation simulation.

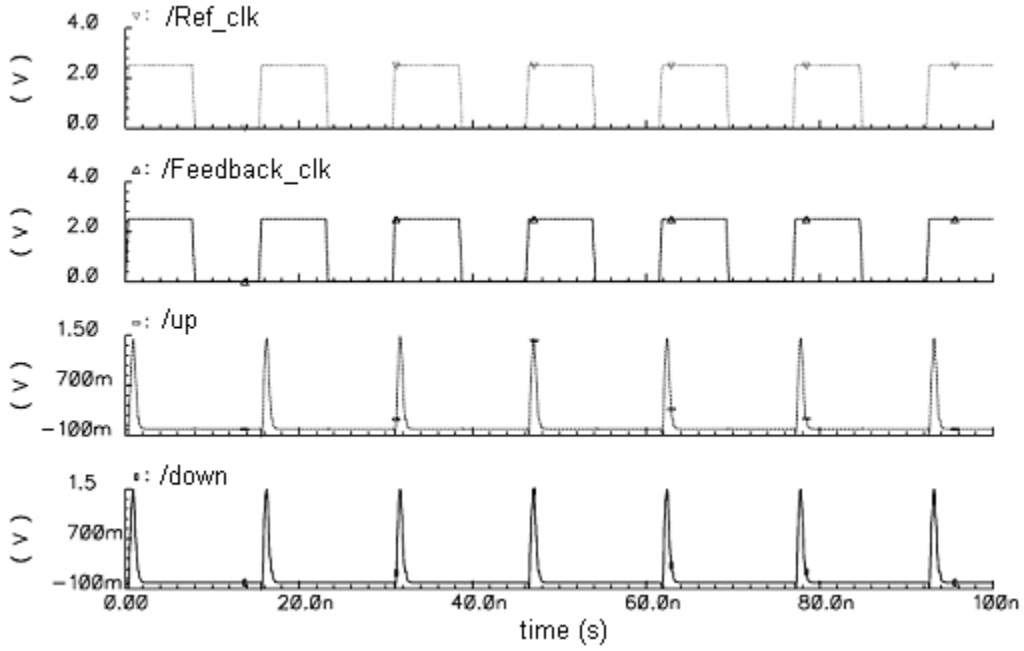


Figure 5.36 PFD and charge pump output when reference and feedback clock are in phase in pre-radiation simulation.

5.7 Loop Filter

The loop filter is the most important part in a phase locked loop as far as achieving the lock of a PLL is concerned. The loop filter is usually a low pass filter that helps in acquisition of the lock. For charge-pump PLLs there are usually at least one capacitor at the output of the charge pump, which integrates the short pulses of currents produced by the phase difference of reference and feedback clock. The capacitor in the loop filter adds one pole in the circuit operation, which together with the feedback loop of the PLL make it a second order PLL. In practice, the use of only one capacitor is avoided, as this will decrease the speed of lock acquisition. Hence, the usual way is to add a zero in the form of a resistor. The addition of the loop filter is clearly shown in the block diagram of the charge pump PLL. The pole is contributed by the capacitor and the zero is contributed by the series resistor. The loop filter hangs from the V_c (control voltage) terminal to the power supply terminal (Vdd, it can be connected to the ground too, depending upon design requirements). In practice (and in this work), a small parallel capacitor is also used to smooth out any ripple. The addition of this extra capacitor (in parallel

with the original loop filter and not shown in the figure of the PLL block diagram) makes the calculations a little bit complicated as it is no more a 2nd order PLL but a third order PLL. Thus, in order to keep the calculations easy and the PLL under the influence of the original loop filter the extra capacitor is usually kept at one-tenth the value of the main capacitor.

In case of the self bias PLL the loop filter is employed in a different way than the usual series R-C connection. It should be mentioned here, that despite the differences that appear in the configurations, the two are same from electrical connections point of view. The basic functionality of implementation of the loop filter is shown and explained below:

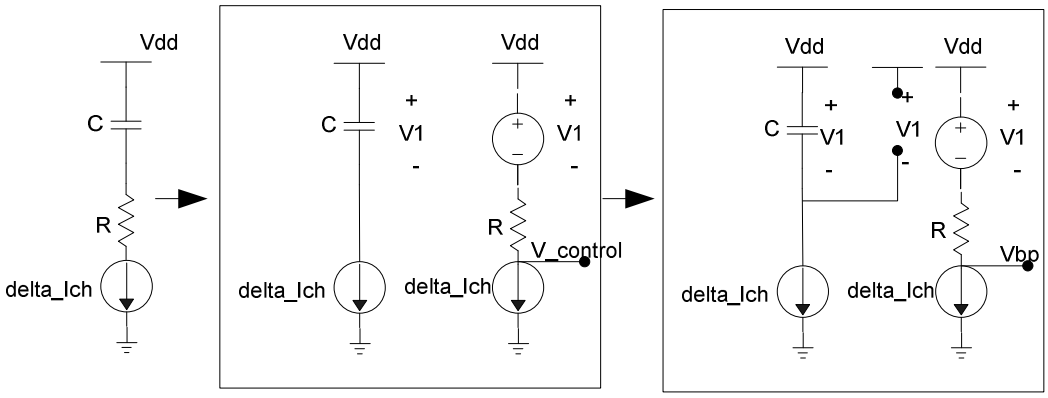


Figure 5.37 Transformation of the loop filter for integration of the loop filter resistor [25].

It may seem difficult to obtain a resistor for the loop filter that varies inversely proportionally to the square root of the buffer bias current. However, this resistor can be formed from the small-signal resistance for a diode-connected device, which is proportional to the square root of the buffer bias current. The integration of such a resistance into the loop filter can be accomplished by applying a transformation to the loop filter as illustrated in Figure 5.30. The loop filter for a PLL is typically a capacitor in series with a resistor that is driven by the charge pump current. The control voltage is then the sum of the voltage drops across the capacitor and resistor. The voltage drops across the capacitor and resistor can be generated separately, as long as the same charge pump current is applied to each of them. The two voltage drops can then be summed to form the control voltage by replicating the voltage across the capacitor with

a voltage source placed in series with the resistor. It just so happens that the bias generator can conveniently implement this voltage source and resistor since it buffers to form with a finite output resistance. Referring back to the buffer bias circuit in Figure 5.14, it is evident that this resistance is established by a diode-connected symmetric load or, equivalently, a diode-connected PMOS device. Thus, the resistance is equal to or inversely proportional to the square root of the buffer bias current. Thus, the self-biased PLL can be completed simply by adding an additional charge pump current [25] to the bias generator's output as shown in Figure 5.1. Therefore, this PLL design is completely self-biased.

5.7.1 Design of the loop filter

The loop filter determines the loop bandwidth of the PLL. This is essential because it gives a low filter response for the PLL by eliminating the high frequency noise. The essential parameters for the loop filter are determined by following the key equations given below to calculate natural frequency ω_N and damping factor ξ.

$$\xi = \frac{1}{2} \cdot \sqrt{\frac{1}{M} \cdot I_{cp} \cdot K_{vco} \cdot R_1^{\,2} \cdot C_1} \tag{5.13}$$

$$\omega_N = \frac{2 \cdot \xi}{R \cdot C_1} \tag{5.14}$$

The self-bias architecture in Fig. 5.1 helps maintain the PLL stable. The dynamics of the PLL can be approximated (by neglecting parasitic capacitances) using the standard second-order transfer function in Laplace domain [3], derived earlier and given here for reference:

$$H(s) = M \frac{(\omega_n)^2 + 2s\xi\omega_n}{s^2 + 2s\xi\omega_n + (\omega_n)^2} \tag{5.15}$$

As mentioned earlier, the two stability criteria for the PLL are $\xi \geq 0.5$ and $\eta = \omega_n / (2\pi f_c) < 0.1$. In the architecture in Fig. 5.1, values of ξ and η are almost solely determined by the output node capacitance of VCO buffers and C_1, which are usually not heavily affected by radiation effects [25]. Consequently, stability performance of the PLL in Fig. 5.1 is robust against radiation. It is known that, wide loop bandwidth for the PLL is essential to

achieve low lock time [3]. Thus in this work, loop bandwidth is maximized to be 7.7 MHz, subject to stability criteria ($\xi \approx 0.51$ and phase margin maintained greater than 50º).

CHAPTER 6

RADIATION HARD PLL ARCHITECTURE

After the design of the loop filter is done the whole PLL has been designed by putting together all the blocks, which were designed individually. The ultimate structure of the radiation hard PLL has been given below in the form of block diagrams:

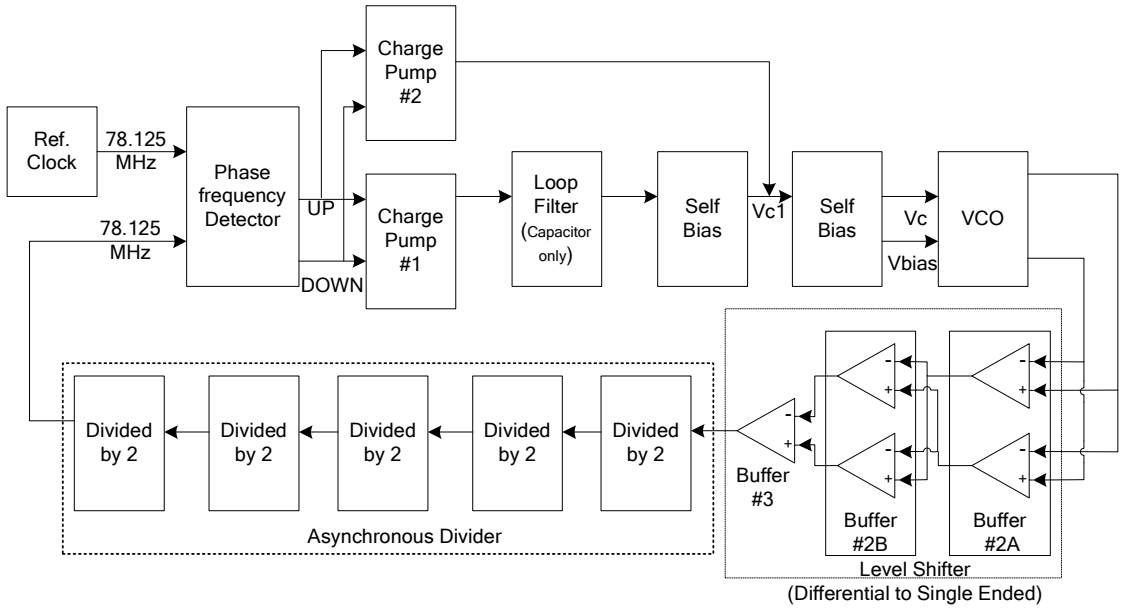


Figure 6.1 PLL architecture.

In order to show the PLL works properly when integrated together the following exercise has been performed. First, the PLL has been run in the simulation for fresh devices to show that all the signals at the critical nodes of point of interest are working properly. Then, a similar exercise has been performed with irradiated devices making up the PLL. The findings are presented below:

The first diagram shows the output of control voltage of the VCO for a simulation time of 700nS. It can be seen from the plots that the control voltage output settles down after around 400 nS. This gives an idea that the PLL locks around that time. This has to be confirmed by

looking at the signals of output of the phase frequency detectors and the reference and feedback signals.

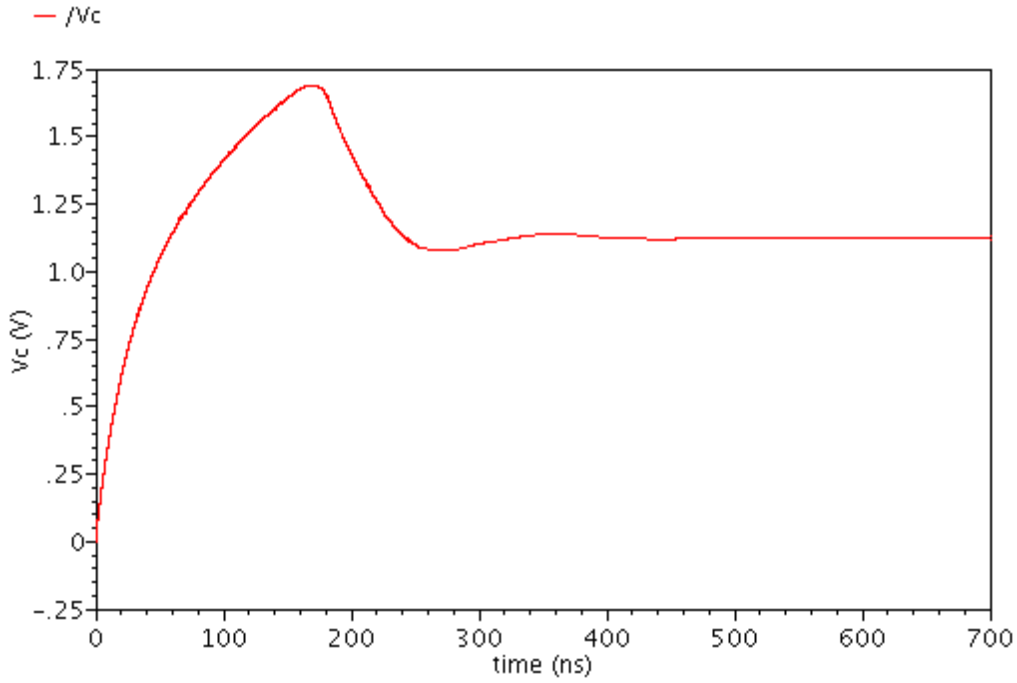


Figure 6.2 VC, control voltage output.

The second diagram shows the output of the phase frequency detectors and the charge pump output and the control voltage. This shows that *up* and *down* signals at the output of the phase frequency detector are providing approximately same short pulses simultaneously, canceling the effect of each other. This corroborates the idea hinted by the previous plots of the control voltage that the PLL is in lock. For further confirmation, the plots of the reference and feedback signals are to be noted.

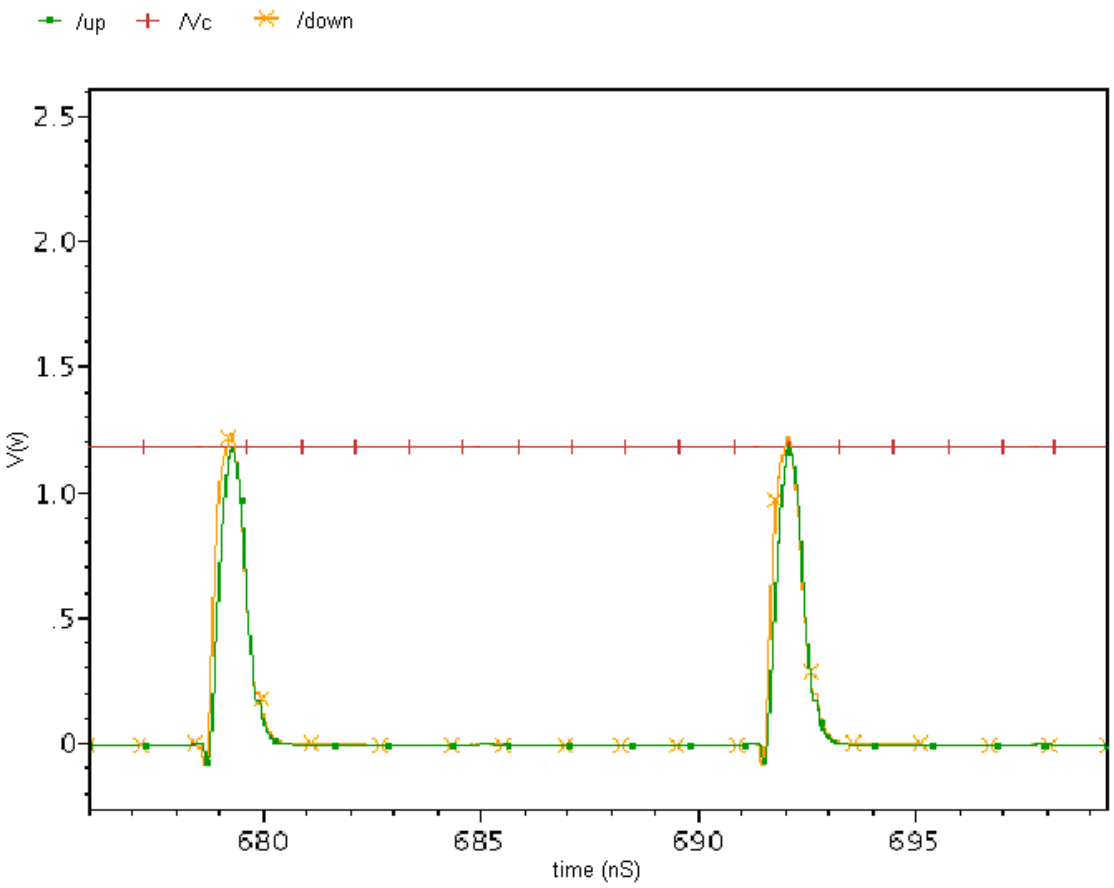


Figure 6.3 Plot of up and down pulses along with Vc output.

The following diagram shows that the reference signal and the feedback signal coming out of the divider output of the PLL almost coincide with each other this shows that the PLL is in lock with respect to phase and frequency. For illustration, the plots of up-down, control voltage and VCO output buffer have been given in the same figure.

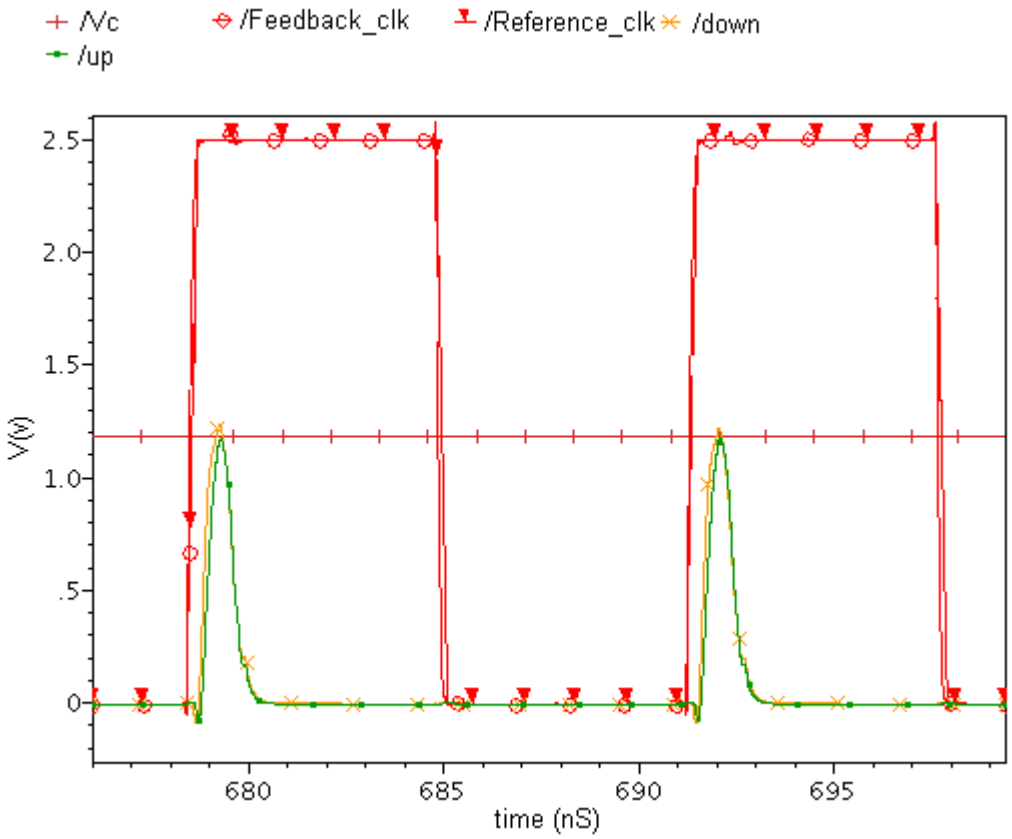


Figure 6.4 Plot of coincident reference and feedback signals along with up/down, control voltage output after the PLL locks.

The diagram to show how the up and down signals behave when the PLL is trying to achieve the lock is shown in the following figure. As can be seen during the region when the PLL is not locked the up and down signal goes high and low and then after a period of time settles down with equal short pulses.

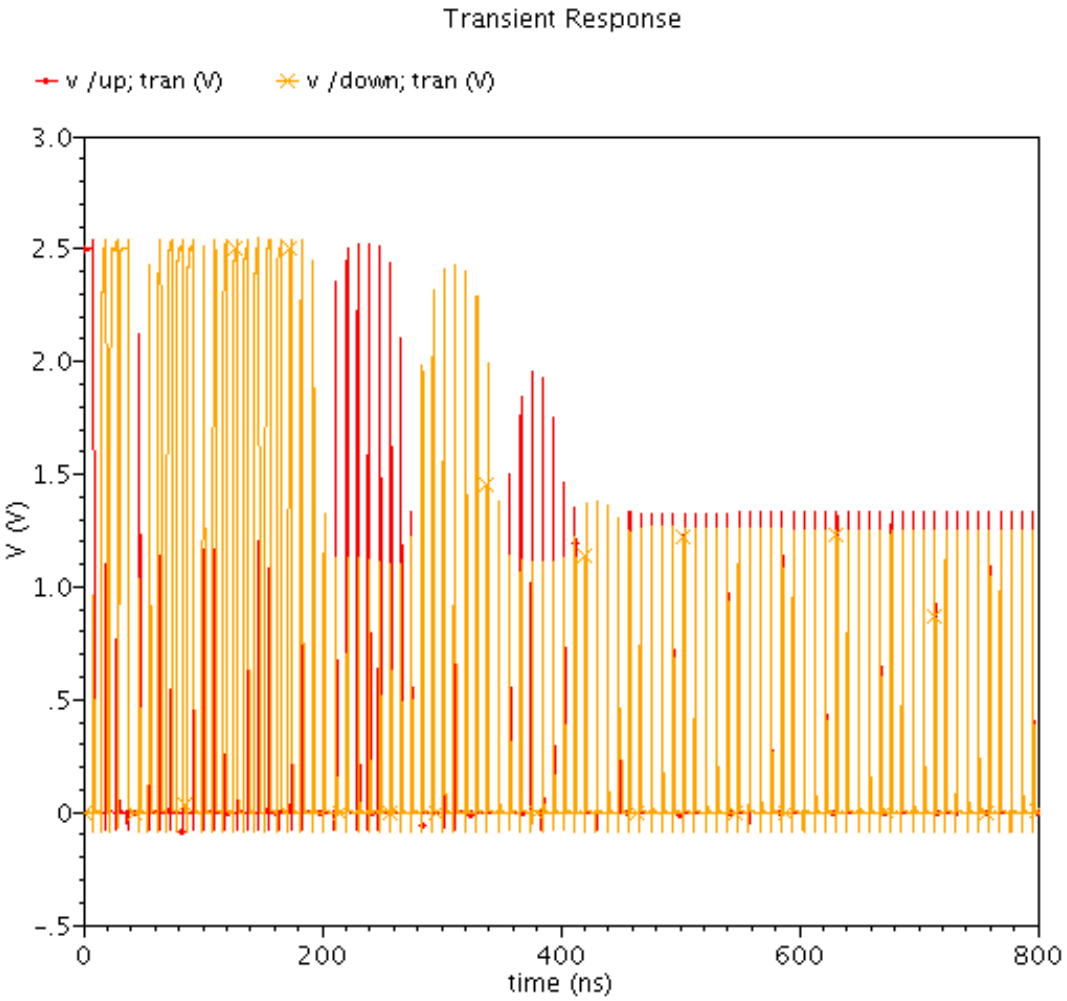


Figure 6.5 UP and Down signals before, after and during the time when PLL locks.

The following plot shows the transient response of the voltage controlled oscillator after the PLL settles down to steady state. The output of the VCO is shown to have a time period of the 400pS. This gives a frequency of 2.5 GHz as predicted and desired as can be seen from the plot on the right, where the frequency of the PLL settles at 2.5 GHz.

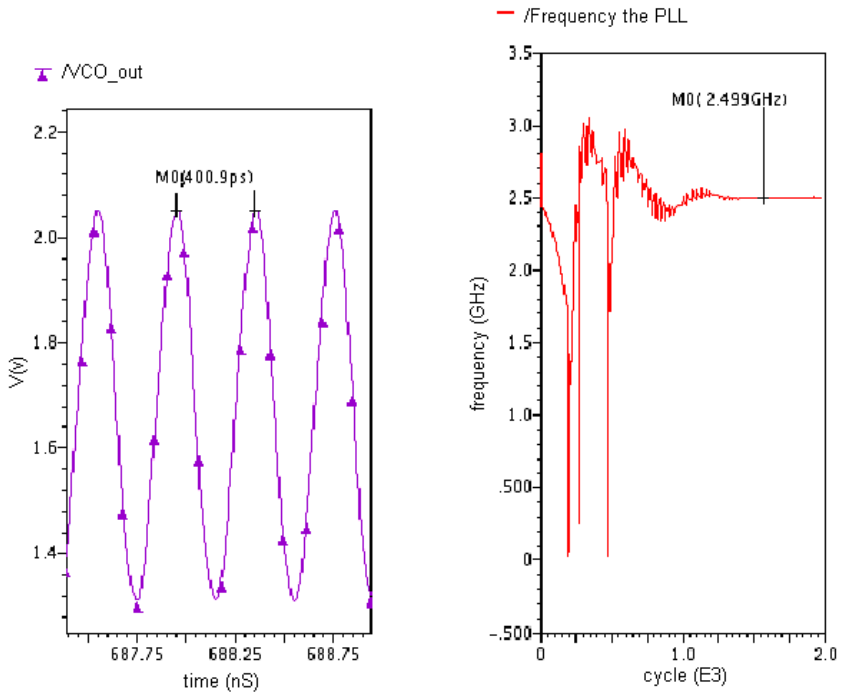


Figure 6.6 Stable VCO output after PLL locks.

The following plots will be the plots for results after the radiation exposure:

The simulation for the PLL was rerun with irradiated device models and the PLL was checked if its functioning was ok.

The first plot shows that the up and down signals are approximately same short pulses indicating a lock for the PLL.

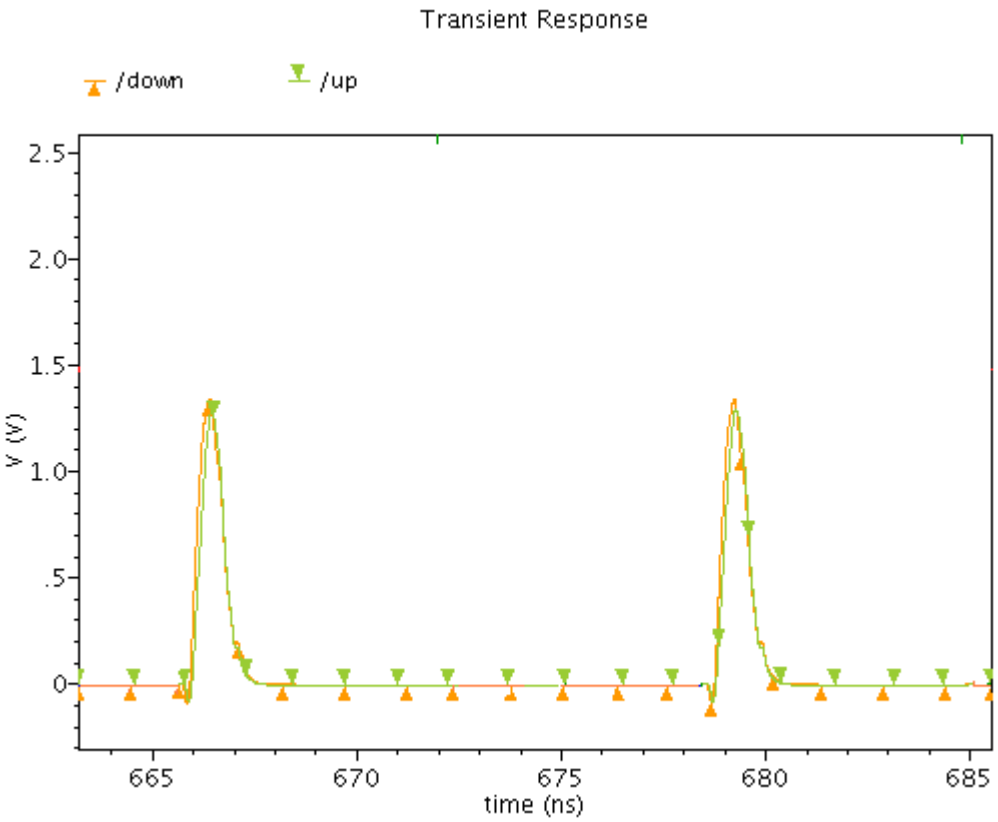


Figure 6.7 Up and down pulses for irradiated PLL after the irradiated PLL reaches lock.

The second plot provides the signal responses of the outputs of the self bias stage (control voltage Vc). The signal settles down to a steady voltage suggesting that the lock has been achieved by the PLL after around 500nS. The voltage settles down at around 1.483 volts.

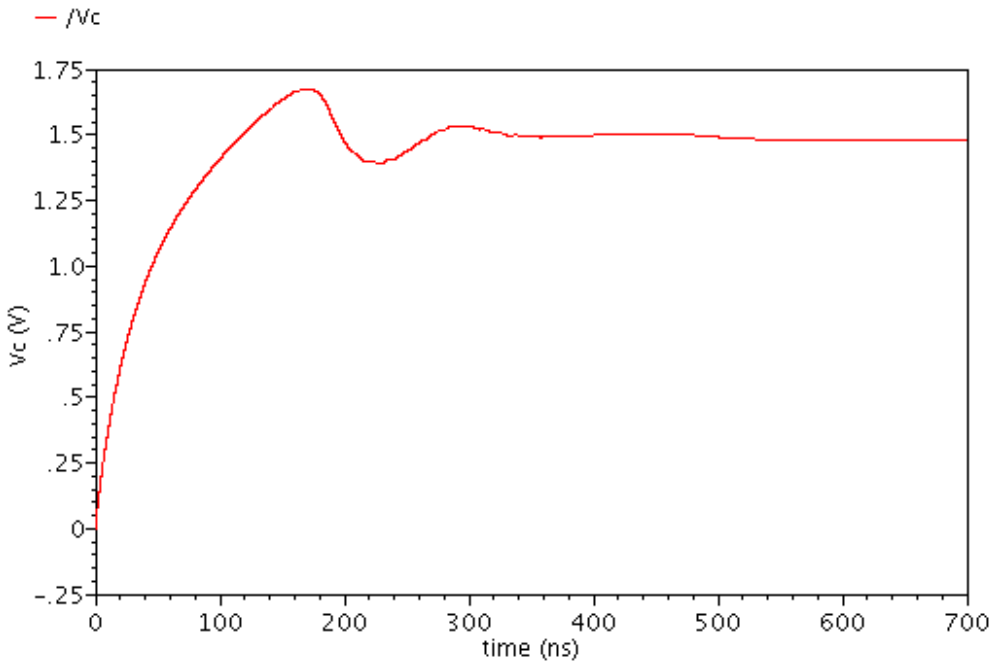


Figure 6.8 Plot of charge pump output and control voltage output for whole region during, before and after irradiated PLL locks.

The next plots show the performance of the level shifters once they are fed by the output voltage of the VCO. The level shifters are used for two purposes. First, they change the common mode or average value of the signals and then they increase the swing level of the signals. It is important because the analog VCO used do not provide rail to rail swing and for the proper functioning of the dividers. This is essential for the overall working of the PLL. The plots are given below: The first plot shows the output signal of an intermediate stage and this shows that the output does not reach the full Vdd level. On the other hand the output signal of the final level shifter (buffer) reaches full Vdd, which is 2.5 volts here.

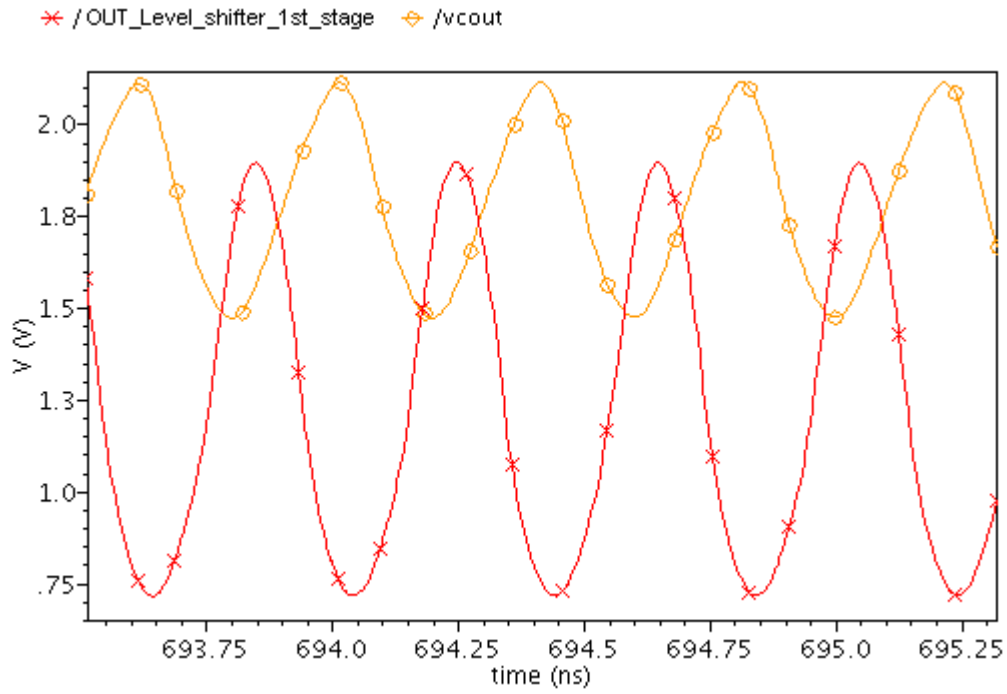


Figure 6.9 Plot of irradiated VCO output and output of the first level shifter stage.

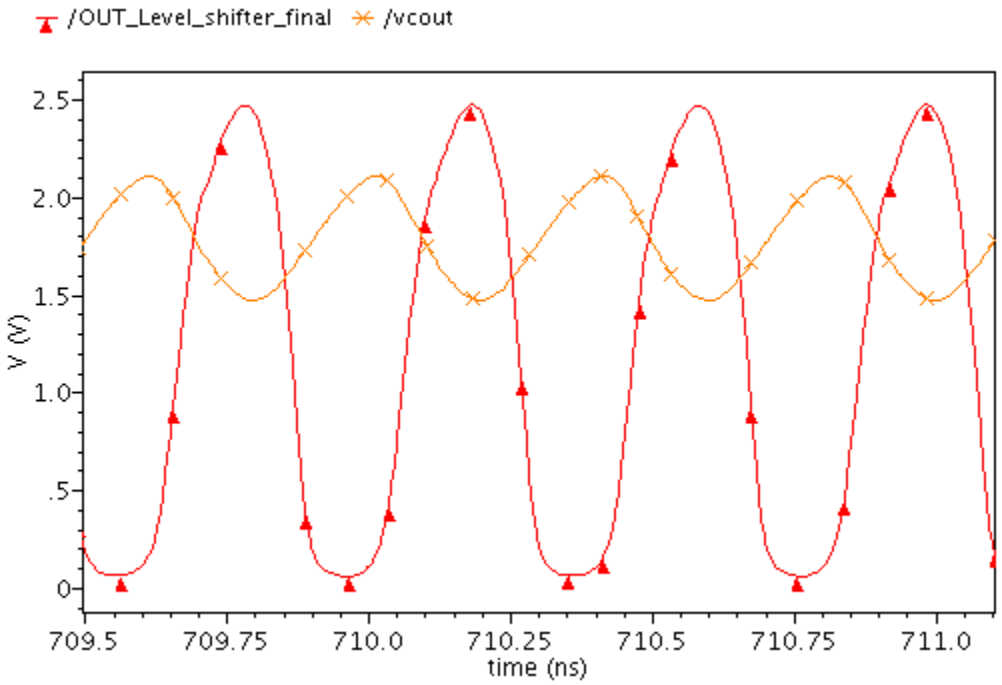


Figure 6.10 Plot of irradiated VCO output superimposed on the output of the final level shifter stage.

For confirmation of the PLL lock the signals of the reference, feedback along with up and down signal from the phase frequency detector have to be examined. The plots are given below:

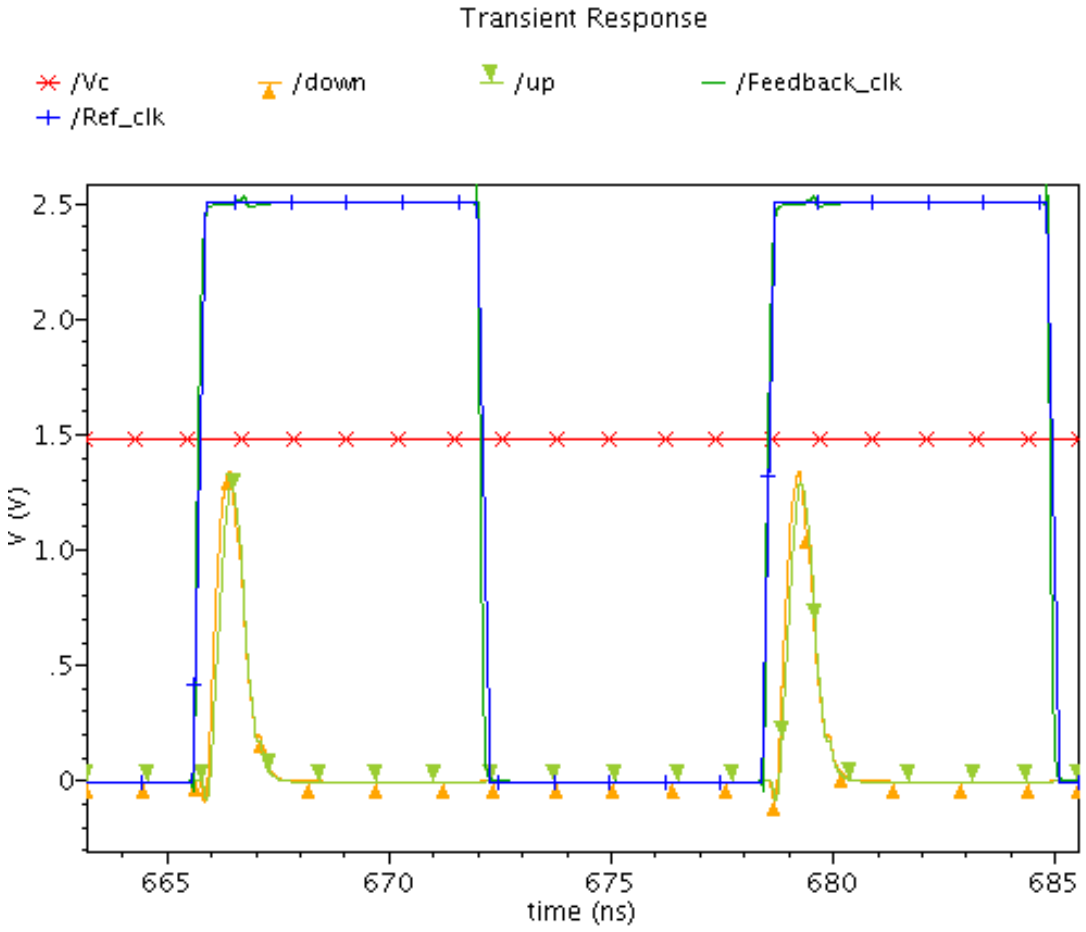


Figure 6.11 Plot of up and down signals along with coincident reference and feedback signals for the irradiated PLL after it locks.

As can be seen from the above plots, the reference and the feedback almost coincide with each other. In addition the up and down signals are superimposed here to show the lock. Given below is the plot of the reference, feedback, the up, down and the output of the VCO. It can be seen that after the PLL achieves lock all the signals reach steady state behavior. The time period of the VCO output shows that it is close to 400pS or 2.5 GHz of frequency.

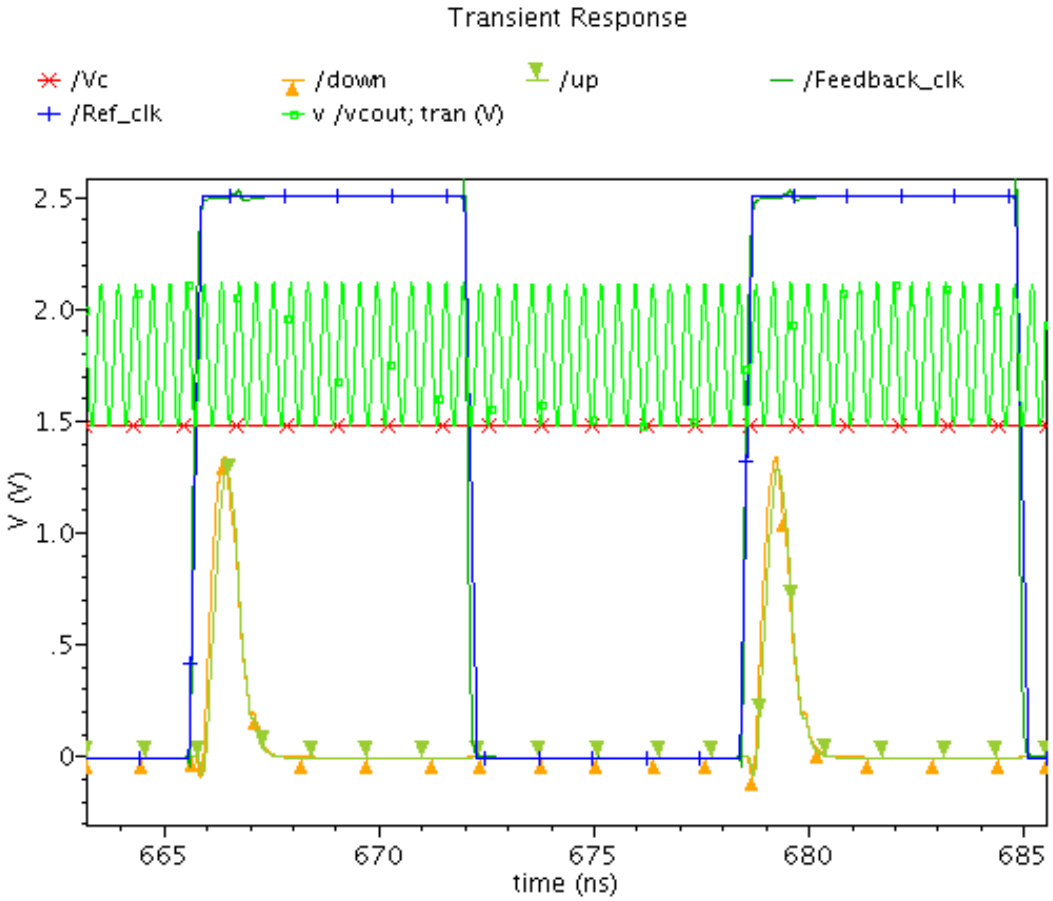


Figure 6.12 Plot of output of all the relevant nodes after the irradiated PLL locks: reference/feedback, up/down, control voltage.

The behavior of the up and down signal for the period during before, after and during lock is shown below:

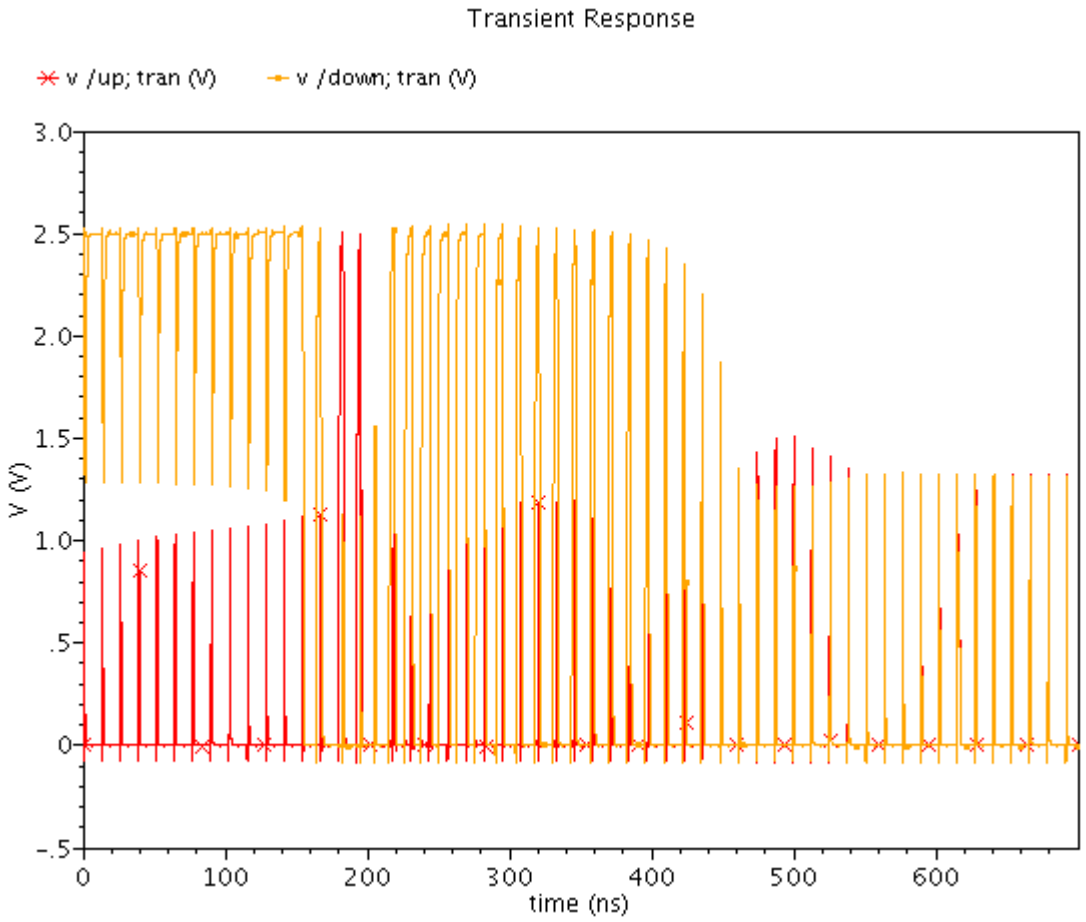


Figure 6.13 Behavior of up/down signals, during and after the irradiated PLL locks.

The methodology used for the analytical calculations and simulations in order to design a phase locked loop is given below. The PLL is supposed to be used for a radiation hard environment to generate clock signals of frequency 2.5 GHz.

CHAPTER 7

DESIGN AND SIMULATION METHODOLOGY

The methodology used for the analytical calculations and simulations in order to design a phase locked loop is given below. The PLL is supposed to be used for a radiation hard environment to generate clock signals of frequency 2.5 GHz. The choice of the topology is therefore most important. A configuration that can tolerate high noise both intrinsic and extrinsic, tolerate changes in its operating conditions and still can generate the required clock signal, is needed. A self-bias PLL [25] provides stability. It does that by keeping the critical parameters for stability (ξ and ω_n) constant even in radiation environment. The low phase noise and large tuning range were achieved using a VCO with novel load structure. In addition, the loop bandwidth (or natural frequency) is maximized to achieve low lock time.

Next is the exercise of looking for the right kind of active devices that would tolerate radiation effects and still can work properly. A charge pump PLL is a very sensitive circuit as it is a second order circuit and it has some constraints to achieve lock. If the characteristic of the active devices change a lot then there is a great possibility that the PLL, designed for a particular operating condition, may not achieve lock at all under the changed circumstances and not work properly. Thus, several CMOS processes were studied and SOS CMOS process was chosen for their inherent qualities against radiation environments. This is because the SOS CMOS process was better than regular CMOS from SEE perspective.

The SOS process is fairly new and relatively exotic. Thus a full review of the process was necessary before it could be implemented to build circuits. [14] carried out a series of experiments to determine the characteristic of the SOS process and how far it changes upon radiation. Several devices of different dimensions were irradiated and their characteristic noted.

For our purpose, all the blocks of the PLL were designed in schematic with fresh transistor model files using Cadence Spectre. They were then simulated to find out their performances for all the corners and change in temperature and process. The fresh model files were then replaced with model files extracted from irradiated devices. The layouts of all the blocks have been drawn using Cadence Virtuoso and the same exercises have been carried out to verify the performances of the blocks under radiation environment.

CHAPTER 8

UNIQUENESS OF THE PLL

The PLL built is robust and performs from -40ºC to 80ºC for all process corners (SS-SF-TT-FS-FF) while providing stable 2.5 GHz of output frequency. The PLL built is on 0.25um Silicon On Sapphire (SOS) technology. The PLL is made radiation hard by the use of SOS–CMOS technology and several improvised design hardness which were explained. The PLL has several unique features from performance point of view and radiation hardness point of view. Several solutions have been proposed to improve the performance of the PLL to work under radiation environment. They will be discussed later. The unique features of the PLL are:

a) large tuning range for the new VCO used in the PLL

b) Low phase noise for the VCO

c) Very low lock time for the self bias PLL

d) Low overall jitter of the PLL

The large tuning range for the VCO and very low lock time for the PLL will prove enormously useful in radiation environment. This is because there is change in operating point of the devices due to radiation effects, which drives sensitive circuits like PLLs out of lock and make them to provide erroneous output frequency. Thus, a large tuning range will prove useful in order to bring the PLL back to providing correct output frequency. In addition low lock time will help the PLL to lock quickly if it goes out of lock. This will be shown later while showing the performance results of the PLL.

Further, low overall jitter and phase noise is needed to provide correct output without accompanying erroneous frequencies. This is very important in radiation environment, since, radiation environments are inherently noisy.

A new VCO design has been presented here, which provides a large tuning range and lowers down the phase noise by several dBs.

8.1 Large Tuning Range For The New VCO Used In The PLL

The tuning range of the VCO is increased by optimizing the output oscillation of the VCO for each control voltage point. Increasing the oscillation swing at each control voltage point by increasing the current gain of the individual delay cells helped in increasing the tuning range of the VCO used in the PLL. The tuning range of the new VCO developed here is from 0.741 GHz to 3.497 GHz (tuning range = 2.757 GHz). The plot for the tuning range is shown below.

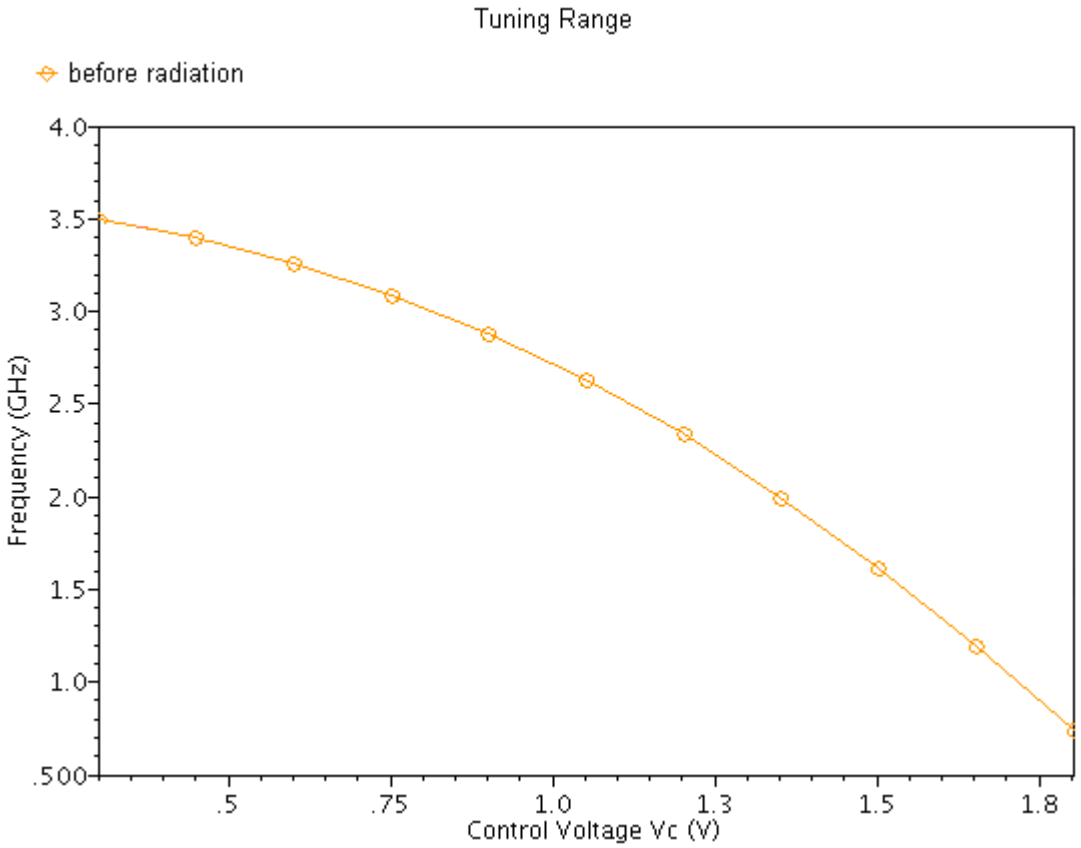


Figure 8.1 The plot of tuning range of the new VCO, which provides 0.5 GHz to 3.1 GHz of output frequency, for a change in control voltage from 300mV to 1.85V.

The performance of the new VCO has been compared with the other contemporary VCOs designed in the 0.25um CMOS, 0.18um CMOS and 0.25um SOS-CMOS. The table of

comparison has been provided below. A figure of merit has been calculated for the compared VCOs and the expression for the same is also given.

Table 8.1 Comparison table for the tuning range of different VCOs

Sr. No	ref	tech	freq	tuning range (linear region)	FOM1
1	[54]	0.18u	1.2G	1.2 - 2.5 GHz (1.3GHz)	114
2	[55]	0.18u	4.0G	3.1 - 4.6 GHz (1.5GHz)	120.33
3	[56]	0.18u	3.6G	2.75 - 4.6 GHz (1.85GHz)	120.78
4	[57]	0.25u	3.0G	2.11 - 3.4 GHz (1.29GHz)	119.85
5	[58]	0.18u	2.4G	0.5 - 2.5 GHz (2.0GHz)	119.36
6	[59]	0.18u	5.0G	4.3 - 6.1 GHz (1.8 GHz)	122.00
7	[60]	0.25u	500M	3.125 - 500MHz (0.496GHz)	107.95
8	[61]	0.25u	1G	0.484 -1.23 GHz (0.746GHz)	112.7
9	[62]	0.25u	1.25G	30M - 2GHz (1.97GHz)	117.8
10	[63]	0.25uSOS	2.5G	2.25 - 3.25GHz (1 GHz)	117.95
11	this work	0.25uSOS	2.5 G	0.741 - 3.497 GHz (2.6 GHz)	122.1

The Figure of merit (FOM1) is calculated by using the following expression:

$$FOM1 = 10\log\left(Frequency * tuning\_range * \min\_process\_length\right)$$

The figure of merit of this VCO is highest. The tuning range is also more than any other VCO compared here.

8.2 Low Phase Noise Of The VCO

To compare the performance of the VCO with respect to the other similar architectures of differential VCO designs, on a common platform, four types of differential VCOs have been designed in 0.25um SOS CMOS process. They are optimized to provide the same output frequency while having similar level of power consumption.

The first design is of a VCO with symmetric load:

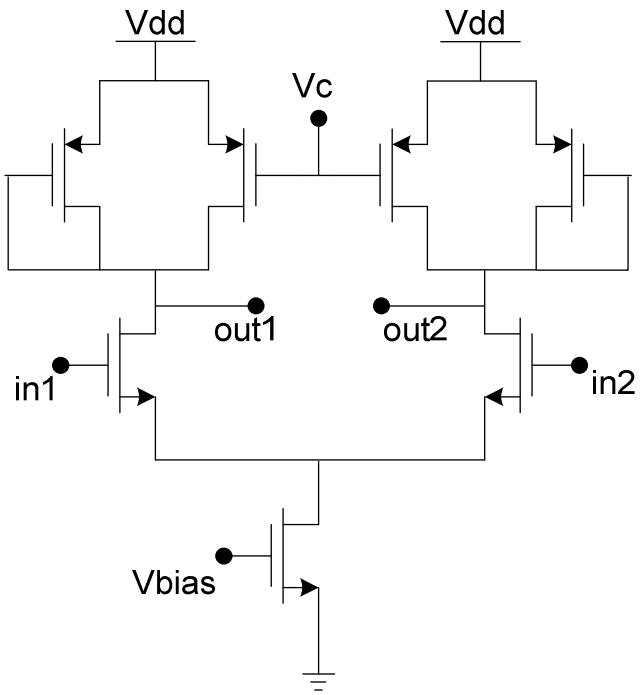


Figure 8.2 Diagram of the schematic of the differential delay cell with symmetric load used in the three stage VCO.

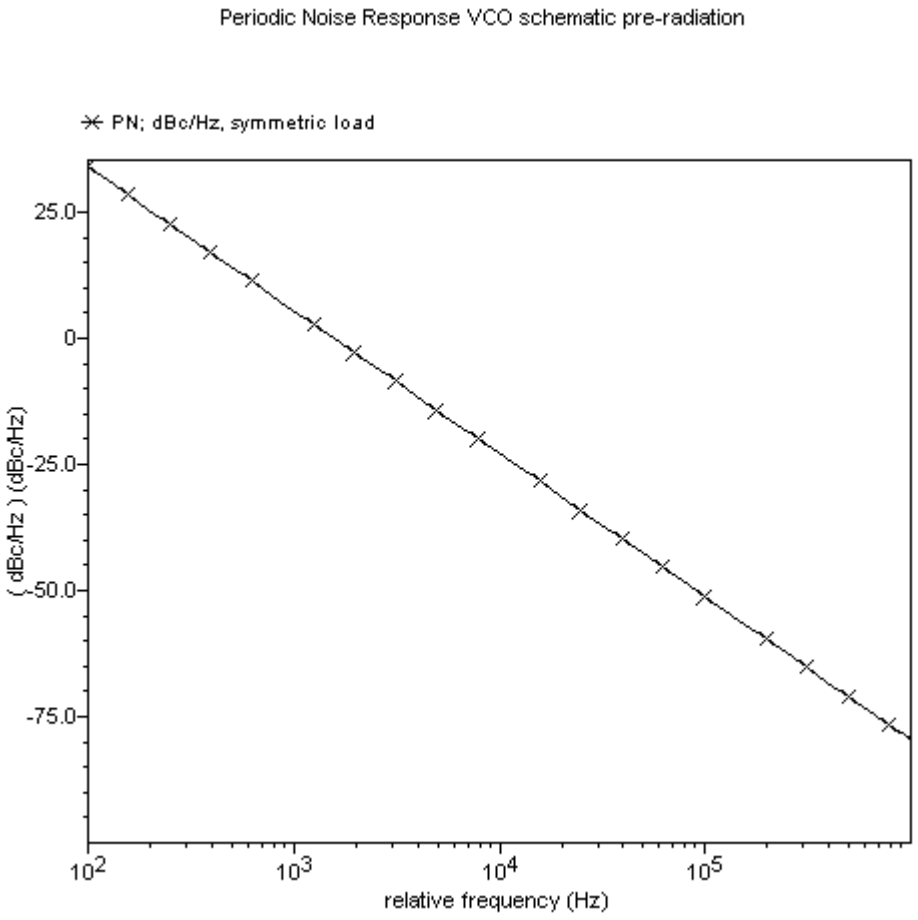


Figure 8.3 The phase noise of the differential VCO with symmetric load is shown above. The phase noise of the VCO for 2.5 GHz fundamental frequency at an offset of 1 MHz is -80dBc/Hz.

The second design is of a differential VCO with cross-coupled load:

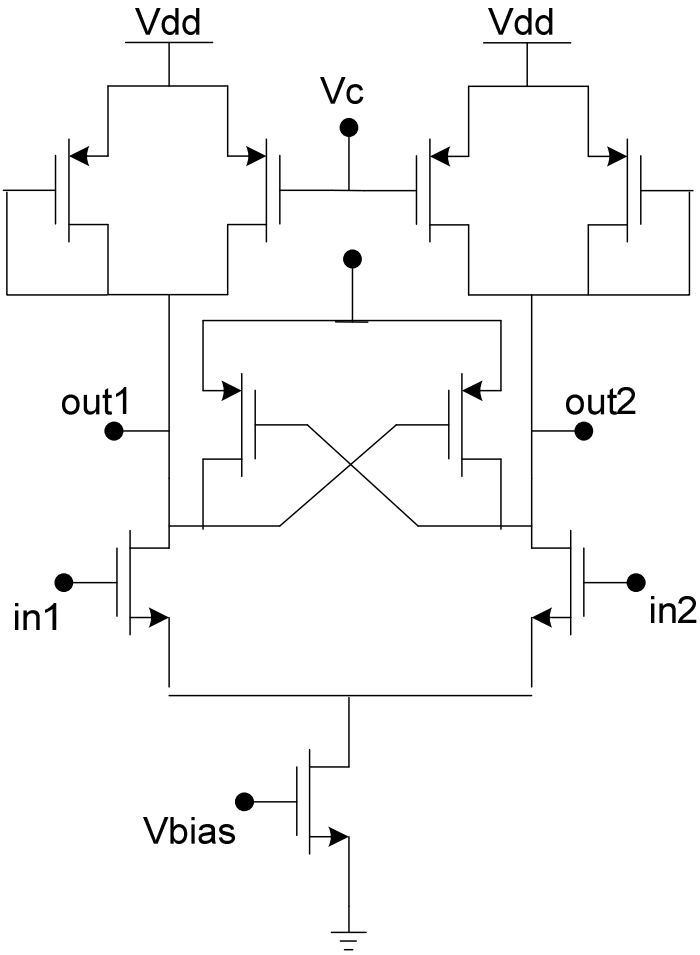


Figure 8.4 Diagram of the schematic of the differential delay cell with cross coupled load used in the three stage VCO.

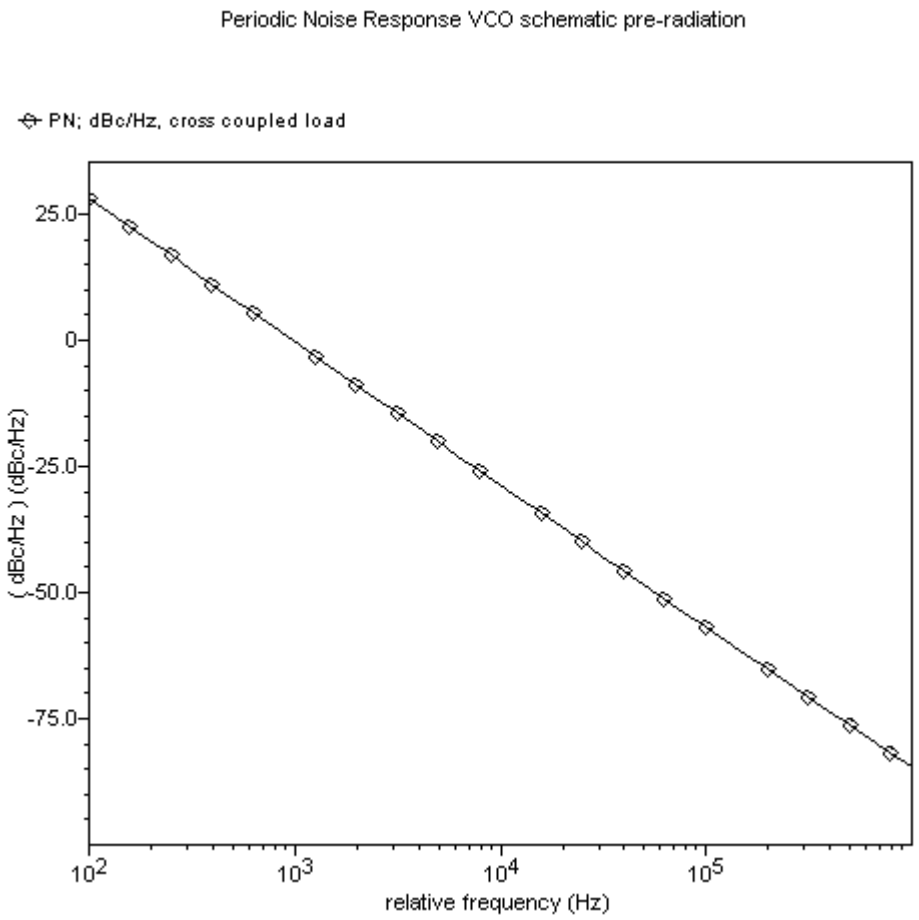


Figure 8.5 The phase noise of the differential VCO with cross-coupled load is shown above. The phase noise of the VCO for 2.5 GHz fundamental frequency at an offset of 1 MHz is -85 dBc/Hz.

The third design is of a differential VCO with clamped load:

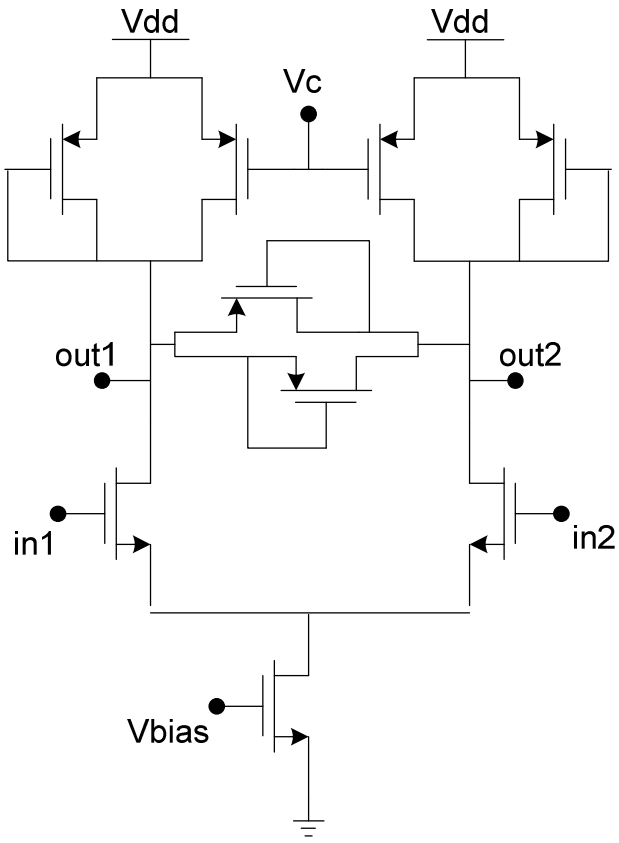


Figure 8.6 Diagram of the schematic of the differential delay cell with clamped load used in the three stage VCO.

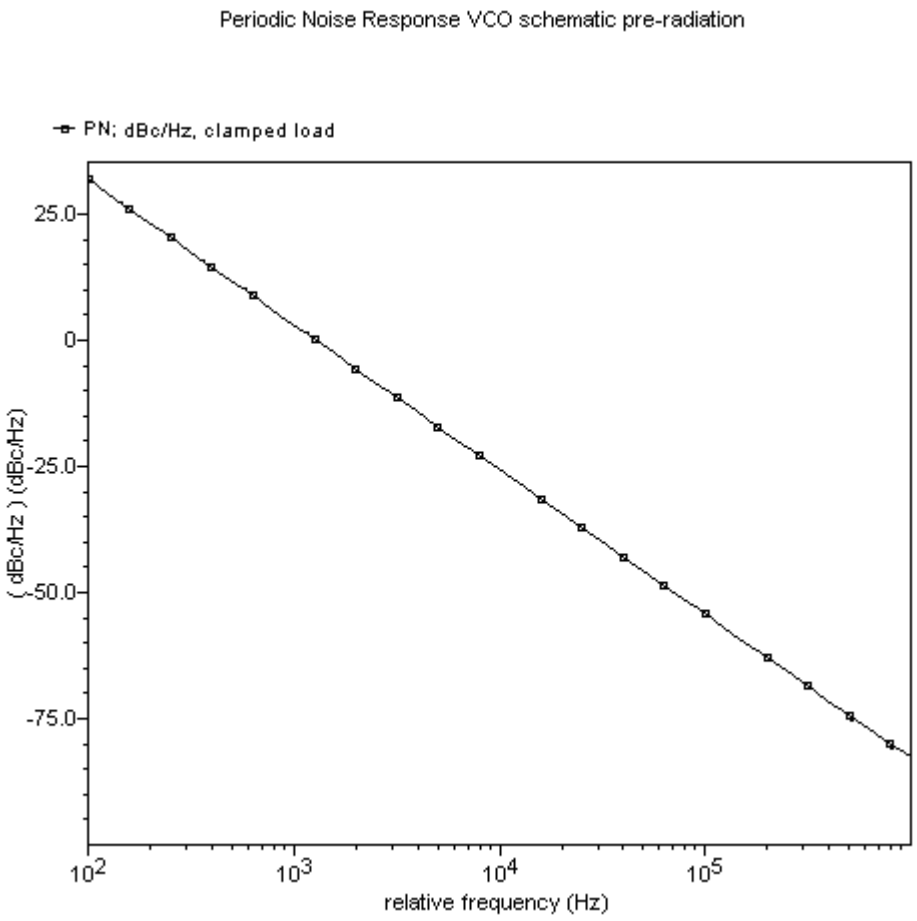


Figure 8.7 The phase noise of the differential VCO with clamped load is shown above. The phase noise of the VCO for 2.5 GHz fundamental frequency at an offset of 1 MHz is -82 dBc/Hz.

The last design is of the new VCO developed here.

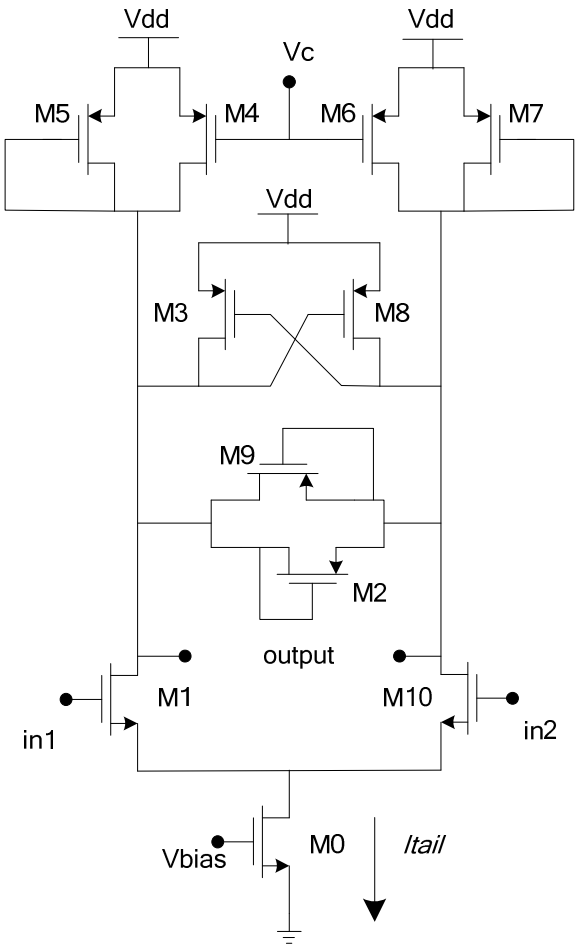


Figure 8.8 Diagram of the schematic of the differential delay cell with a combination of clamped, cross-coupled and symmetric load used in the three stage VCO. The dimension of M4 = M3 + M5, to maintain maximum symmetry.

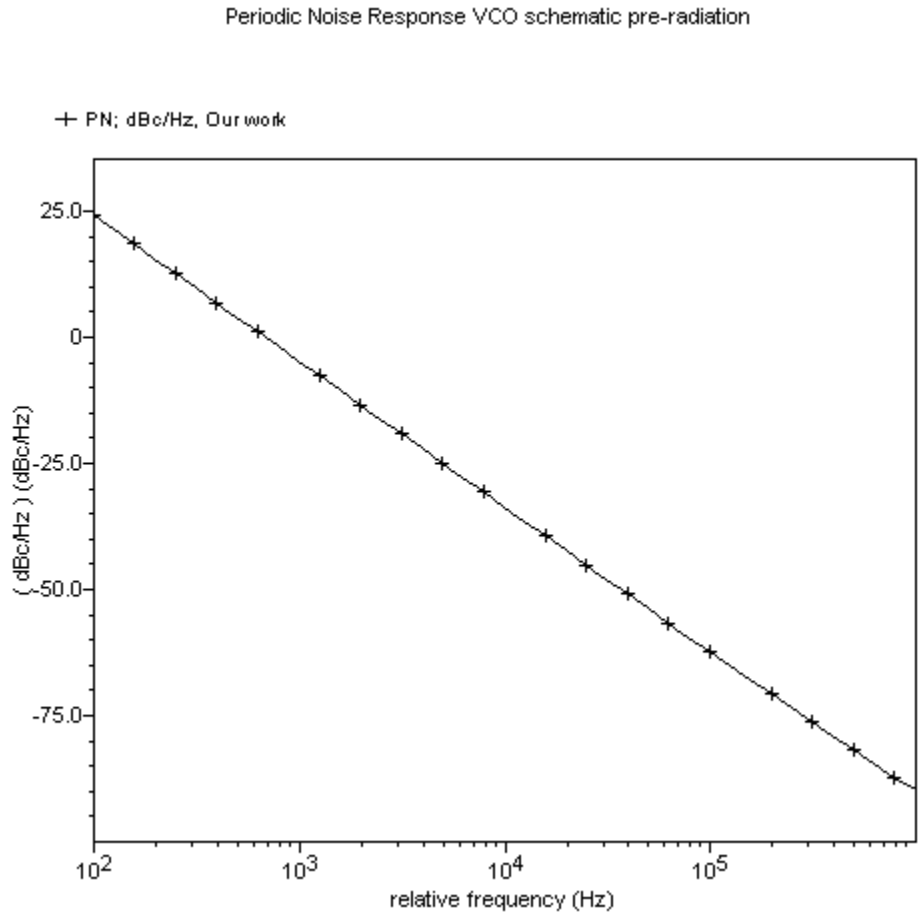


Figure 8.9 The phase noise of the new differential VCO developed in this work is shown above. The phase noise of the VCO for 2.5 GHz fundamental frequency at an offset of 1 MHz is -93 dBc/Hz.

For comparing the performance of the above VCOs, which provide 2.5 GHz for similar power consumption level all the phase noise plots have been shown on the same graph. This is shown below:

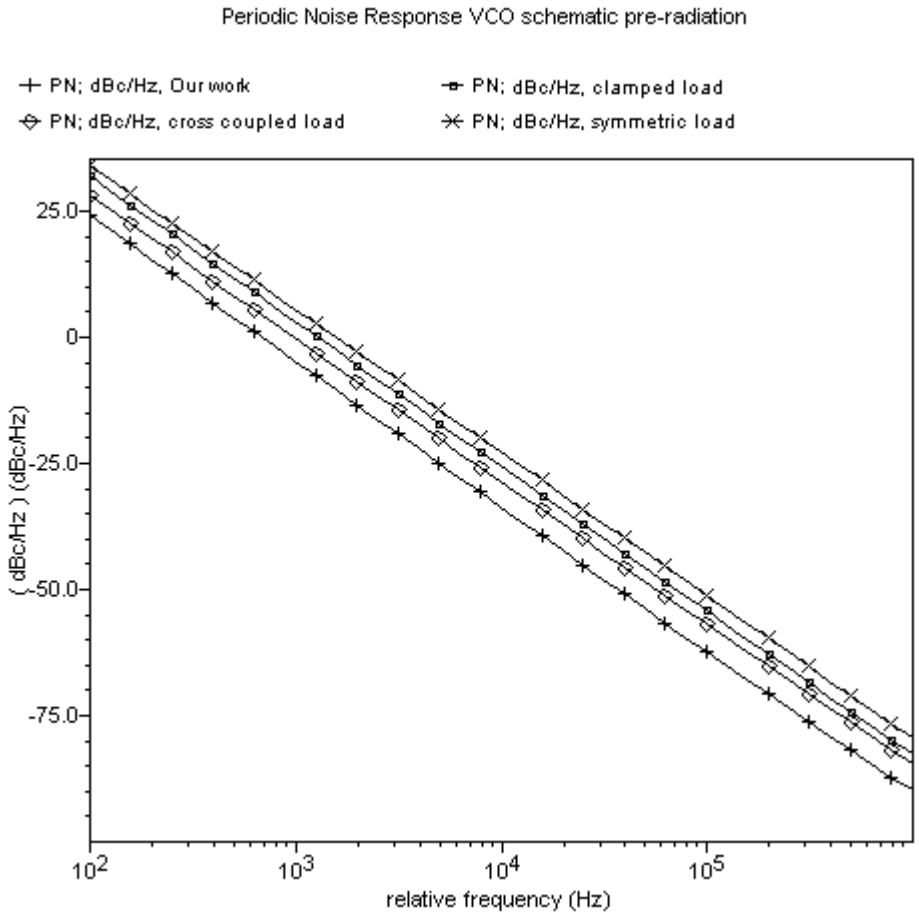


Figure 8.10 Comparison of phase noise of all the four VCOs explained above

The above graph shows that the new VCO developed has a lower phase noise than all the other comparable types. The phase noise of the new VCO has phase noise, which is 13 dB lower than the simple symmetric load VCO, 10 dB lower than the phase noise of the clamped load VCO and 8 dB lower than the phase noise of the cross-coupled load.

8.3 Very Low Lock Time For The Self Bias PLL

A very low lock time has been achieved for the PLL designed here. This is a very critical performance parameter for the PLL as it will determine when the PLL will come back to lock once it is thrown out of lock. This is even more important in radiation environment as mentioned before.

The PLL in this case achieves low lock time as it is a self-bias architecture and it has a nonlinear transition for approaching towards lock . In addition two startup circuits have been introduced to jump-start the PLL when need arises. The lock time for the PLL (with fresh devices) for stable 2.5 GHz output frequency is 412nS. This is shown in the plot below. This is a huge improvement as it is one of the lowest lock times achieved among today's PLLs.

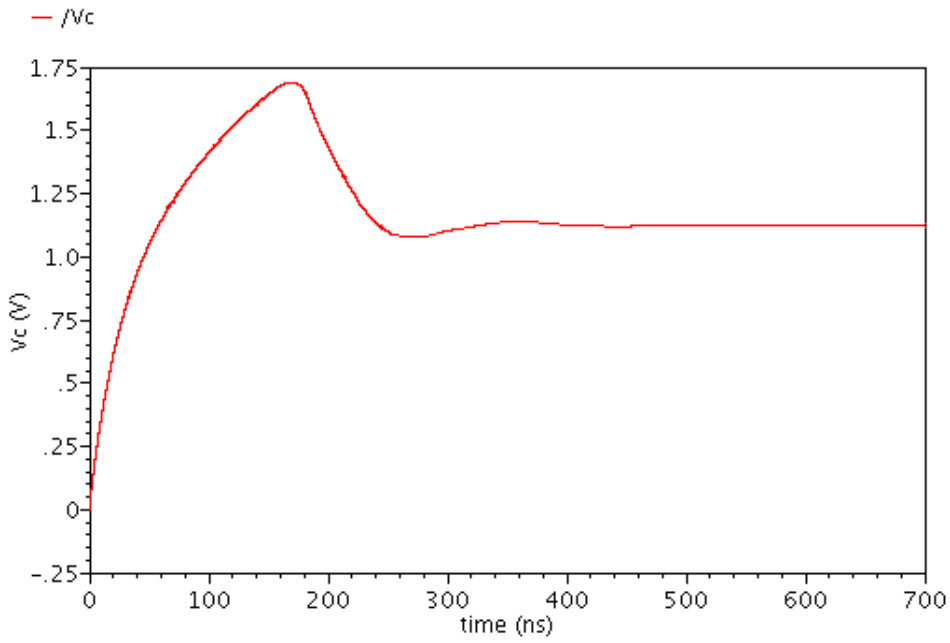


Figure 8.11 The plot for achieving lock. The plot shows that the PLL has a stable control voltage after 412nS. The transition time for the PLL shows that the control voltage has a sharp rise towards the stable voltage. This shows the ability of the PLL to achieve lock quickly.

The lock time of the PLL designed here, has been compared with the other PLLs designed in advance submicron technology and generating high GHz range frequencies. This is shown in the table below:

Table 8.2 Comparison of lock time for different PLLs

Sr. No.	ref	tech	freq	lock
1	[64]	0.25um	5.8GHz	13uS
2	[65]	0.18um	800M	6.5uS
3	[66]	0.18um	5.1GHz	3.88uS
4	[67]	0.12um	4GHz	125uS
5	[68]	0.13um	2.4GHz	150uS
6	[69]	0.13um	1.22GHz	1.5uS
7	[70]	0.25um	1.5GHz	1mS
8	[62]	0.25um	1.25GHz	15uS
9	[61]	0.25um	1GHz	1mS
10	this work	0.25umSOS	2.5GHz	412nS

The above table shows that none of the PLLs designed comes close to the locking time achieved by this PLL. This is a huge advantage in the radiation environment as will be shown below while comparing radiation effects on the PLL.

8.4 Low Overall Jitter Of The PLL

The PLL designed here achieves a very low peak to peak jitter as will be shown later. The low jitter was achieved because of several reasons, which are explained below. The VCO designed which has been incorporated in the PLL has low phase noise and more importantly the PLL designed has a loop bandwidth of 7.7 MHz which helps in correcting errors quickly. In addition, the self-bias stages designed have bandwidths comparable to the operating frequency of the PLL. This helps in tracking any noise that are present in the circuit operating at that frequency. The plot of the peak to peak jitter is available from the eye-diagram of the output frequency taken from VCO output. This is shown below.

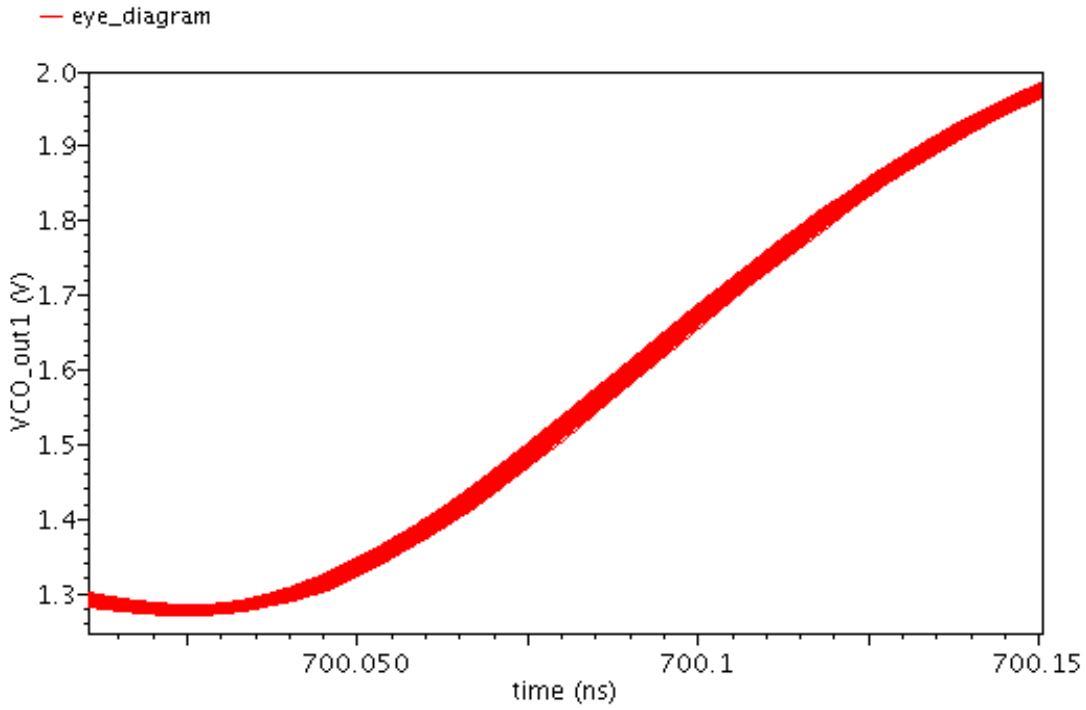


Figure 8.12 The plot of peak to peak jitter of the PLL taken from the VCO output providing frequency of 2.5 GHz.

A similar peak to peak jitter plot taken from the output of the buffers that are placed between the VCO and the dividers is shown below:

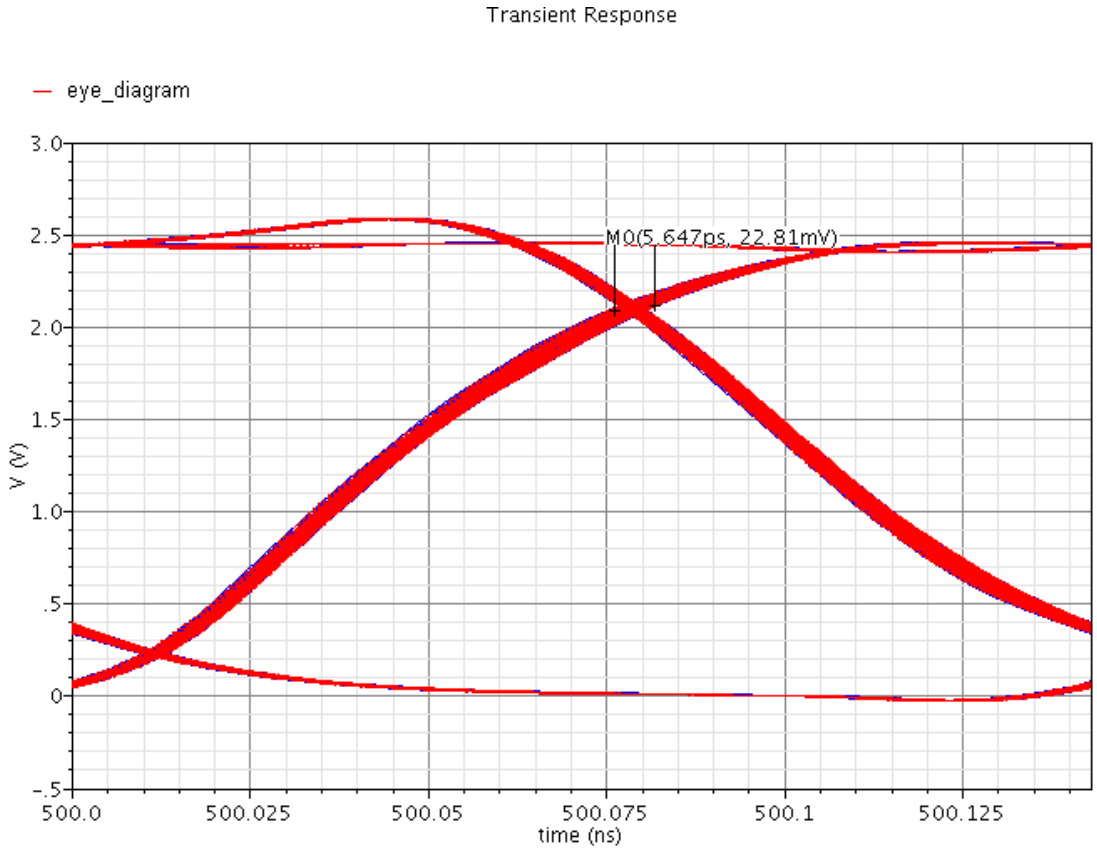


Figure 8.13 The plot of peak to peak jitter of the PLL taken from the buffer output providing frequency of 2.5 GHz.

To compare the performance of the PLL with other contemporary PLLs from the perspective of jitter a comparison table has been made and shown below:

Table 8.3 Comparison of Peak to Peak jitter for different PLLs

ref	tech	frequency	Peak-Peak jitter	comment
[17]	90nm CMOS	2.5 GHz	14.9 pS	
[72]	130nm CMOS	2.5 GHz	9pS (rms)	P-P jitter will be more
[73]	0.25umSiGe biCMOS	2.5 GHz	14.4pS	
[74]	0.25um CMOS	360MHz	25pS	
[68]	0.18um CMOS	2.5 GHz	25.2pS	
[75]	0.24um CMOS	2 GHz	35pS	
[76]	0.25um SOS	2.4 GHz (max.)	48pS	
this work	0.25um SOS	2.5 GHz	4.873pS*	Simulation

The comparison table shows that the PLLs built in different technologies, 0.25um CMOS and other much-advanced technologies and providing 2.5 GHz are much worse than the jitter performance achieved by the PLL designed here. As can be seen from the plots above and the comparison table, a very low overall jitter of 4.873 pS has been achieved from this PLL. This is a critical parameter, since, in radiation environment the jitter performance will degrade. Therefore, a very low jitter is desired for radiation environment.

CHAPTER 9

PLL PERFORMANCE COMPARISON WITH AND WITHOUT RADIATION

The PLL designed here is for radiation environment. Therefore the PLL has been compared for before and after radiation, with regards to its different specifications. The comparisons are given below in terms of plots.

9.1 Frequency Of Operation

The frequency of operation of the PLL for before and after radiation is 2.5 GHz. The PLL locks in both the conditions and so is able to provide the desired frequency without much trouble. This is shown below in the two plots:

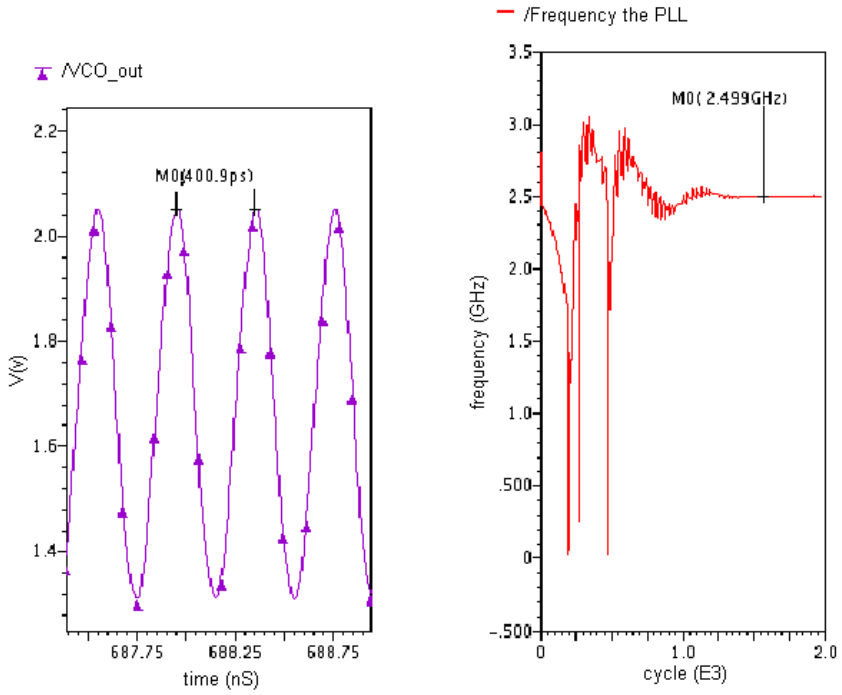


Figure 9.1 Plot of transient waveform of the output of the PLL showing the time-period of one cycle, which shows that the output frequency is 2.5 GHz. This plot is without radiation effects.

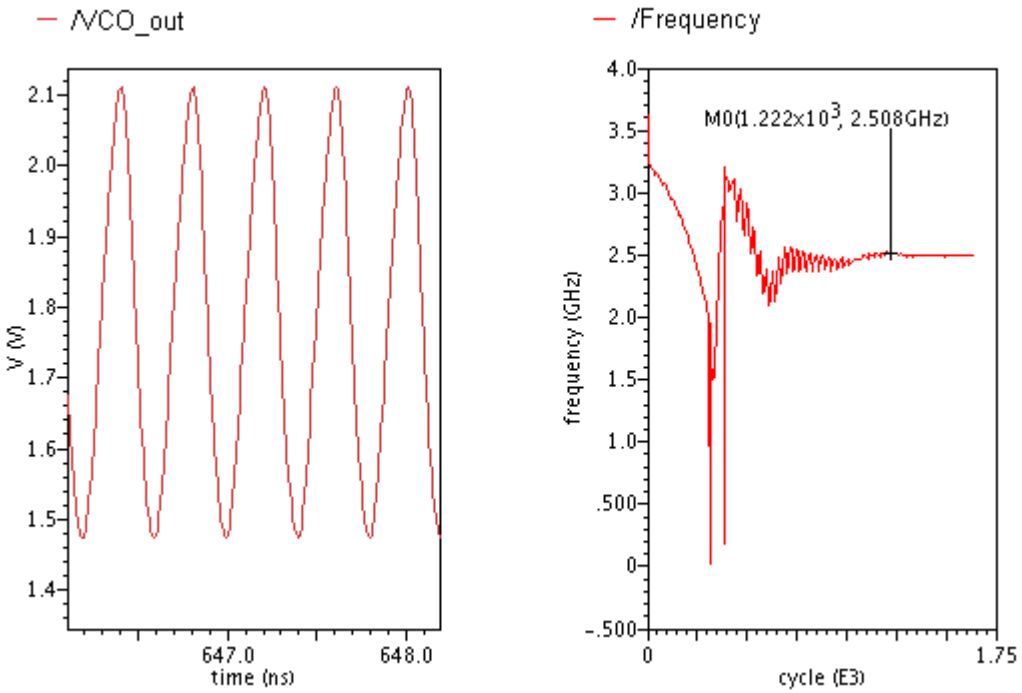


Figure 9.2 Plot of transient waveform of the output of the PLL showing the frequency of the PLL getting settled after it locks, which shows that the output frequency is 2.5 GHz. This plot is with radiation effects.

The two plots show that the frequency of the output of the PLL remains the same at 2.5 GHz though the voltage level changes.

9.2 Tuning Range Of The VCO Incorporated In The PLL

The tuning range of the VCO achieved is from 0.741 GHz to 3.497 GHz i.e. 2.756 GHz for fresh devices. The tuning range of the VCO degrades under radiation effects. This can be seen from the plot below. The tuning range of the VCO after radiation is from 1.57 GHz to 3.46 GHz. The range after radiation is 1.89 GHz, which is around 0.9 GHz less than the range for the fresh case. In addition, the linearity of the tuning range has also deteriorated as can be seen from the plot below:

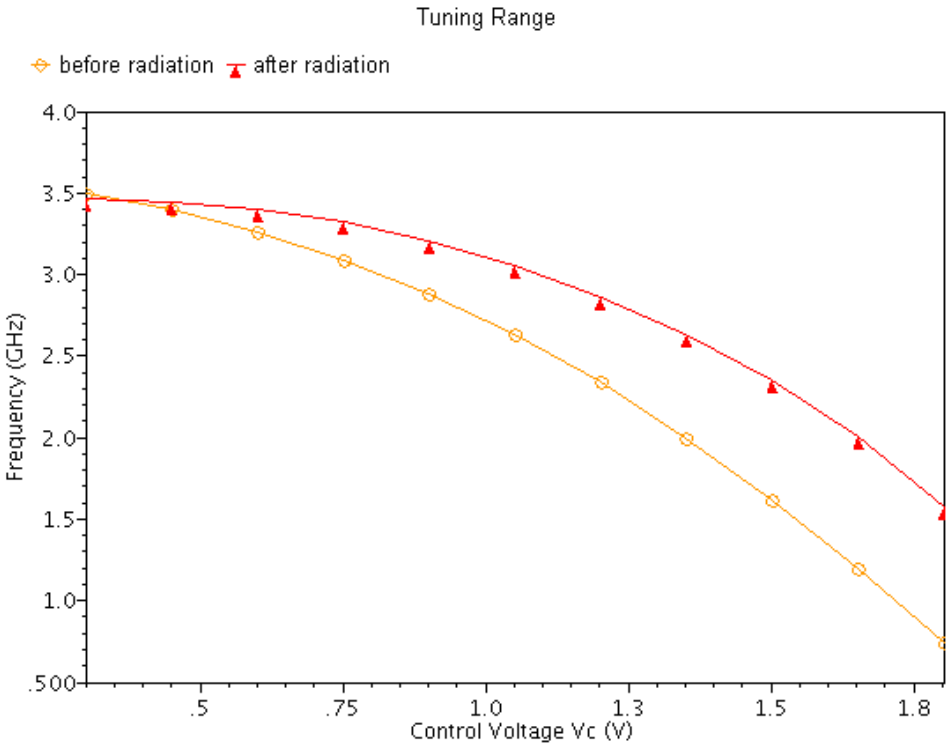


Figure 9.3 The plot for tuning range of the VCO, before and after radiation.

9.3 Phase Noise Of The VCO Incorporated In The PLL

The phase noise of the VCO is an important parameter and is very critical as has been mentioned above. The phase noise of the VCO degrades by some factor as can be seen in the plot below. The degradation is of 3 dB at an offset of 1 MHz from the fundamental frequency of the VCO. The phase noise of the VCO was -93 dBc/Hz at an offset of 1 MHz from the fundamental frequency of 2.5 GHz for fresh devices. The phase noise is more by 3 dB, i.e., the phase noise became -90dBc/Hz at an offset of 1 MHz from the fundamental frequency of 2.5 GHz for irradiated devices. This can be seen from the plot below:

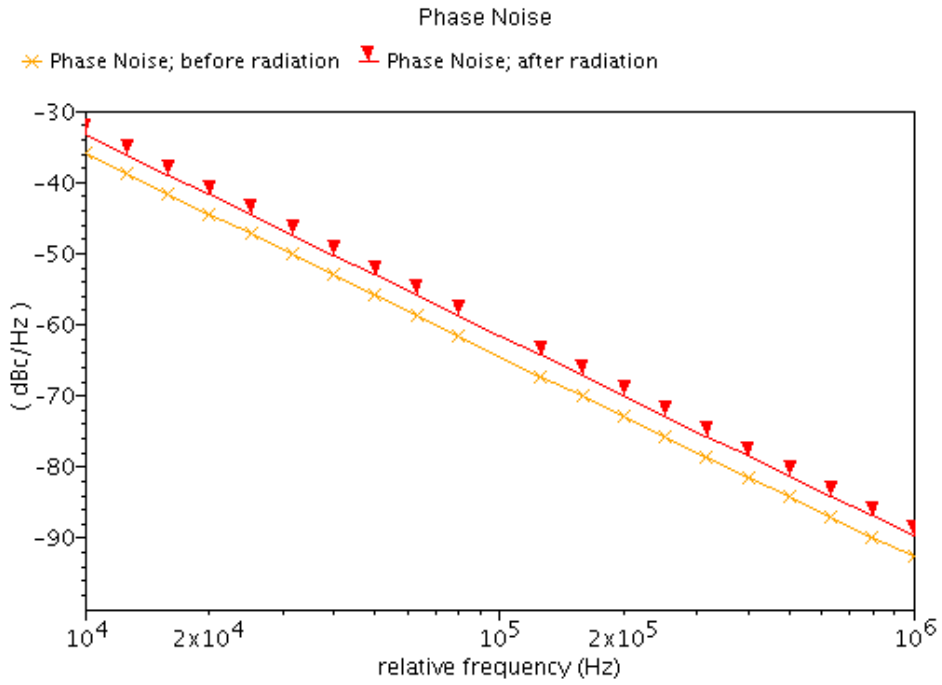


Figure 9.4 The plot for the phase noise of the VCO for fresh and irradiated case. The top one is for after radiation and the bottom one is for fresh case. The degradation is clearly visible here.

9.4 Lock Time Of The PLL

The lock time is an important parameter of performance for the PLL as has been mentioned above. This is even more critical in a radiation environment. This will help the PLL to get back to lock once it is driven out of lock. A low lock time is thus desired. The comparison of lock time for the PLL before and after the radiation is shown below:

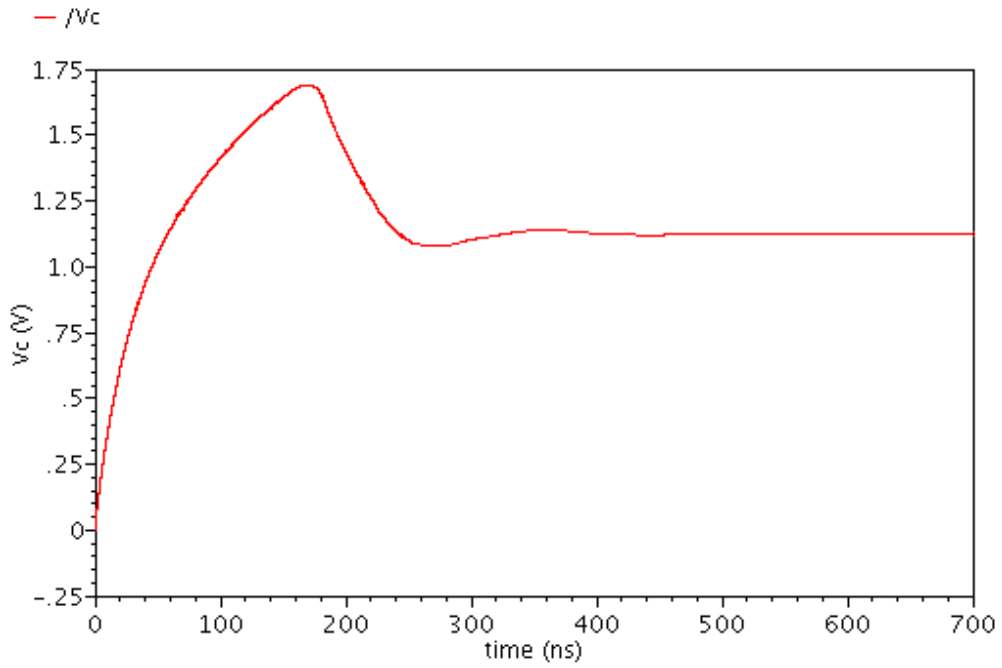


Figure 9.5 The plot of control voltage Vc which shows that the PLL achieves lock after 412 nS. This plot is for the PLL with fresh devices.

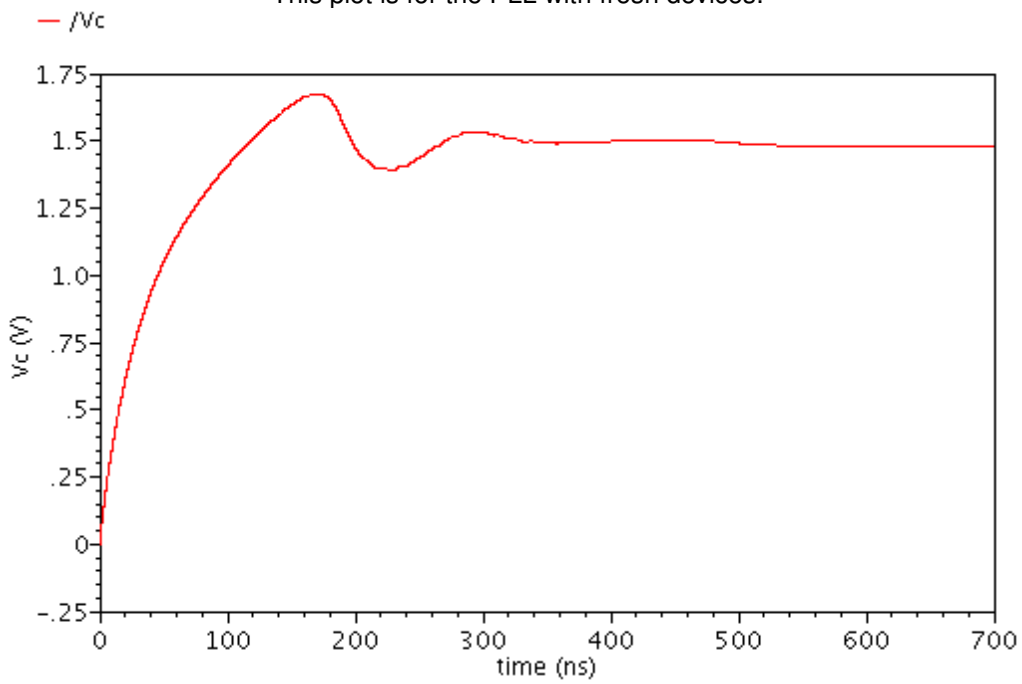


Figure 9.6 The plot of control voltage Vc which shows that the PLL achieves lock after 525nS. This is the plot for the PLL after radiation.

The two plots show that there is a degradation in the lock time of the PLL because of radiation effects. The degradation is around 90nS. The plot shows that even after radiation the PLL maintains a very good lock time.

9.5 Amplitude Of The VCO Output Used In The PLL

The amplitude produced by the VCO is also compared for the before and after radiation. The single ended VCO output is of concern and is shown in the plots below:

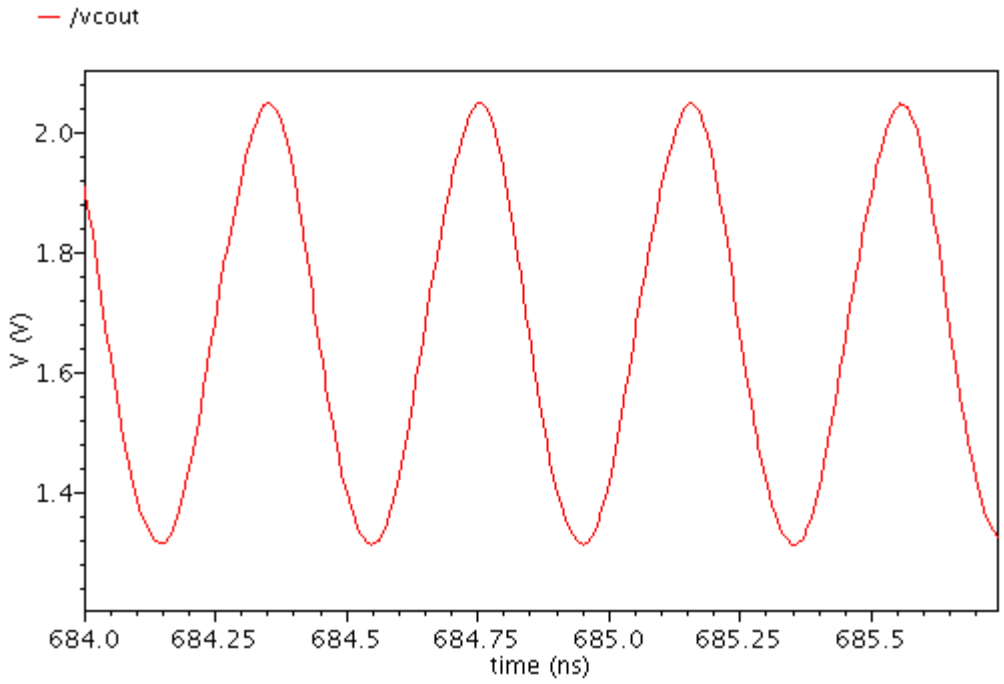


Figure 9.7 The plot of single ended VCO output amplitude for fresh devices operating at 2.5 GHz. The amplitude is 720mV.

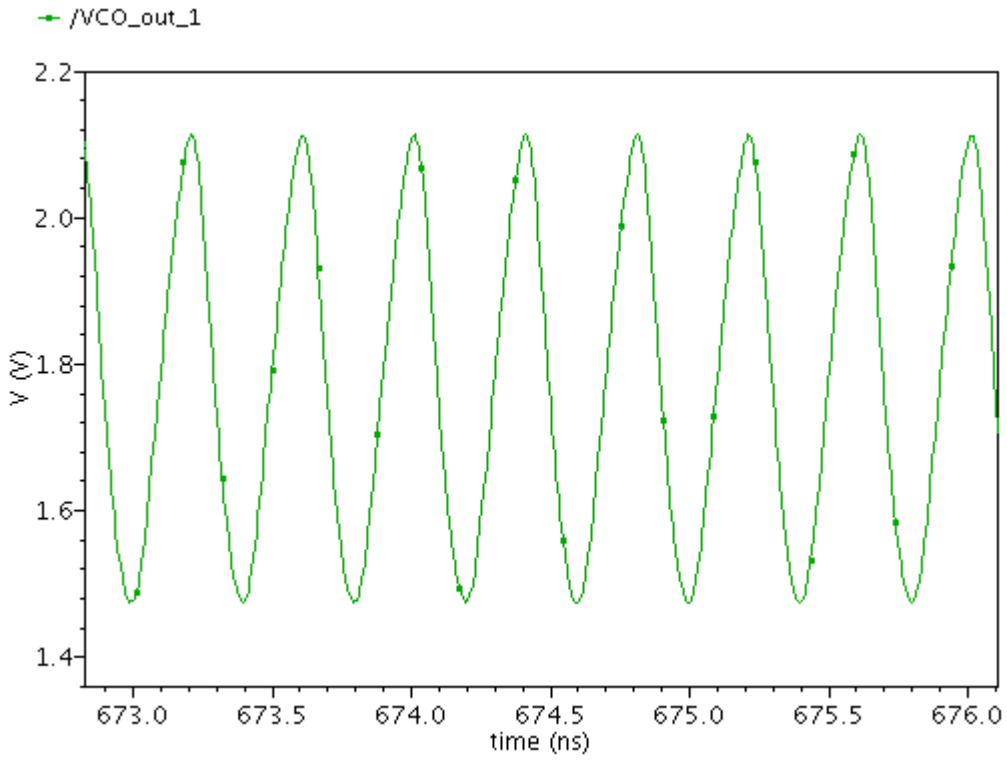


Figure 9.8 The plot for the single ended VCO output after radiation. The plot shows that the amplitude after radiation is 630mV.

The amplitude is degraded by around 100mV for the same output frequency generated by the PLL (VCO) due to radiation. This is mainly because the inherent characteristic of the self-bias PLL to reach an optimum point if there is a change in the operating condition of the circuit. In this case, the control voltage, which controls the lower swing of the output, reached 1.8 V and clamped the VCO output swing to that value.

9.6 Jitter In The Output Frequency Produced By The PLL

The jitter produced by the PLL is of concern. The lower the jitter better it is for the PLL. The PLL designed here produce a very low peak to peak jitter as was mentioned earlier. The jitter of the PLL is compared for the fresh versus irradiated case and is shown below.

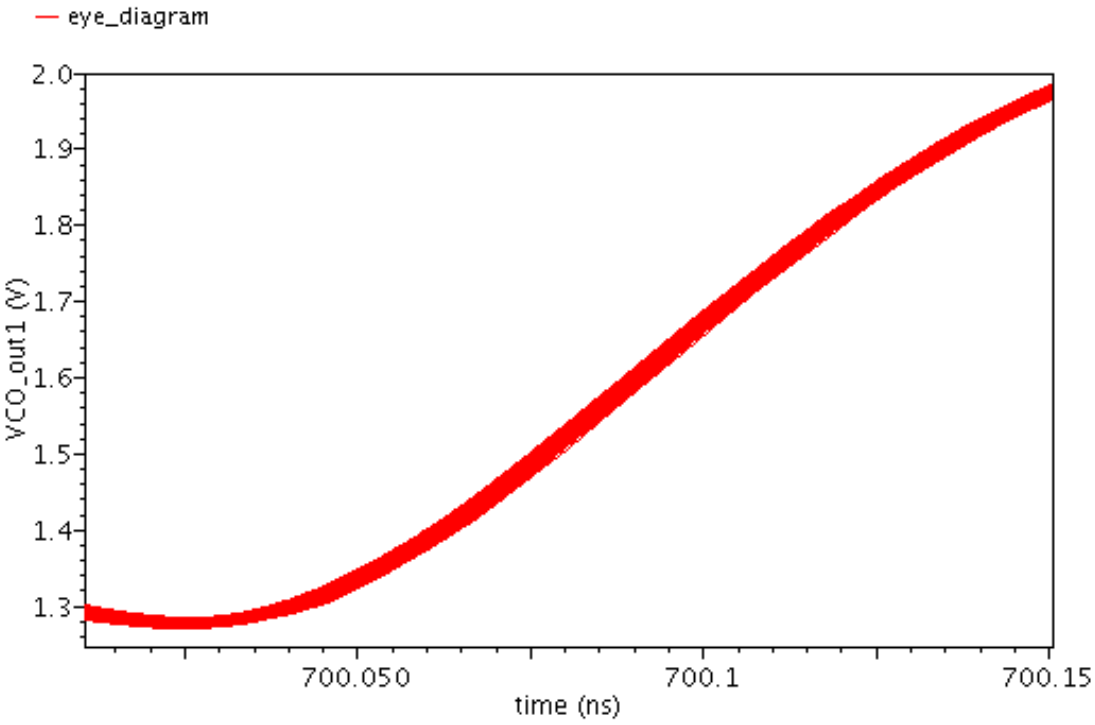


Figure 9.9 The plot for peak to peak jitter of the PLL output for 2.5 GHz frequency for fresh devices. The peak-to-peak jitter is 4.873pS.

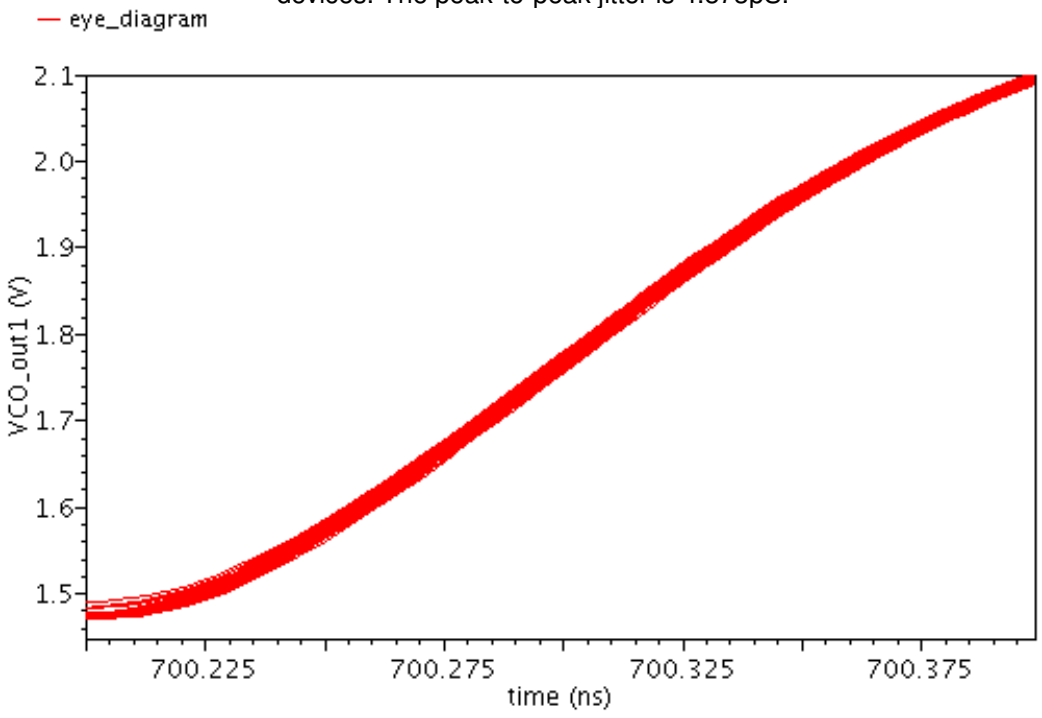


Figure 9.10 The plot for the jitter produced by the PLL after radiation. The jitter in this case is 11.61 pS.

The two plots above show that after radiation the jitter produced by the PLL is increased from 4.873pS to 11.61 pS. The degradation is of around 7 pS.

9.7 Power Consumption

The power consumption of the whole PLL under locked condition for fresh devices is 71.8mW and for the radiated PLL is 57.5mW. Reduction in power is due to mobility, threshold voltage degradation and the lower voltage swing of the VCO in the radiated PLL.

9.8 SEE Effects On The PLL

Single Event Effects can disrupt the functioning of a PLL. Though single event effect has virtually no adverse effect on the Silicon On Sapphire CMOS devices (as mentioned previously), a simulation has been done to capture the behavior of the PLL if there was a bad SEE hit on our PLL. The simulation has been done by first identifying the most vulnerable point in the circuit and then depositing an amount of charge at that point for a short period of time. This is usually the case when SEE hit takes place in bulk CMOS devices. The output of the charge pump stage is the most vulnerable position in a charge pump PLL, as has been mentioned in [43]. The plots obtained after the simulation is given below.

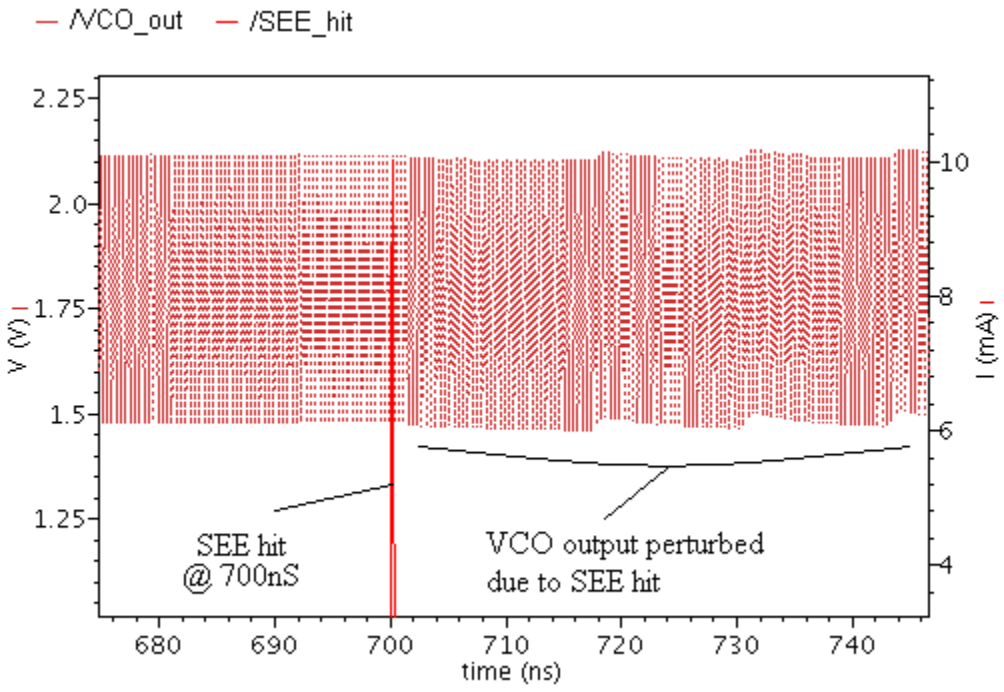


Figure 9.11 The plot for SEE effects on the PLL. The SEE hit takes place at 700nS after the PLL locks and there is a perturbation starting at 700nS, which takes some time to settle down.

The next plot shows that the control voltage of the VCO takes around 184.3nS to settle down. The maximum change in the voltage level of the control voltage is 7.48mV, which is very less and shows the ability of the robust PLL to deal with this kind of situation. The charge deposition in this case was 1.5 pC, which generated more than 10mA of peak current.

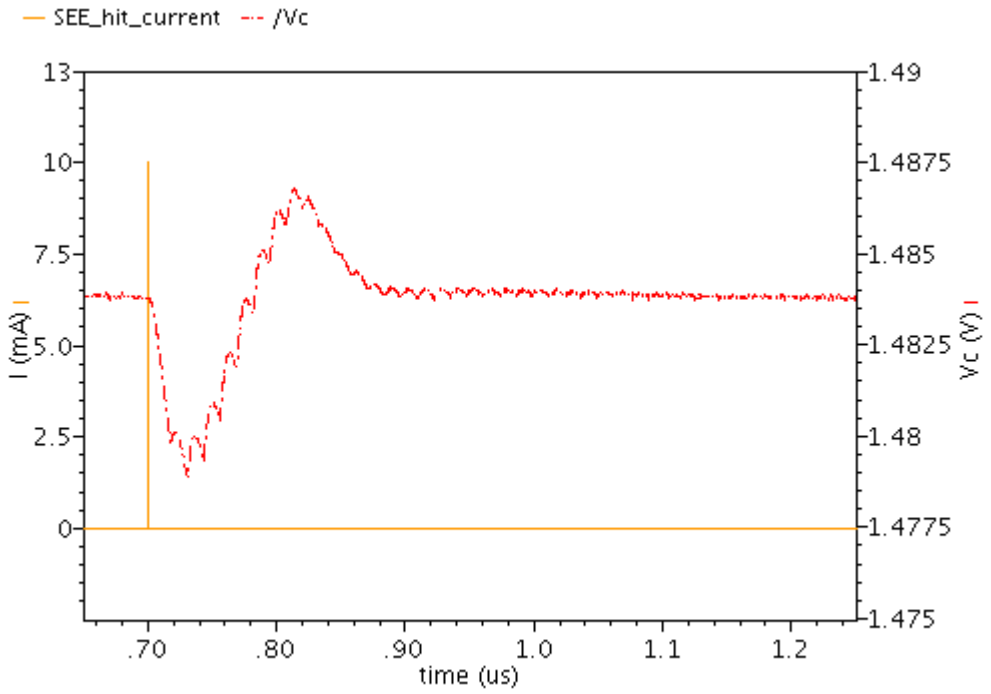


Figure 9.12 The plot of the control voltage after SEE hit. 1.5pC of charge deposition due to SEE creates a perturbation of 7.48mV and 184.3 nS. The PLL quickly goes back to the original operating condition.

This will be compared with the other PLLs, which are used in the radiation environment. The plots of those PLL under SEE effects are shown below.

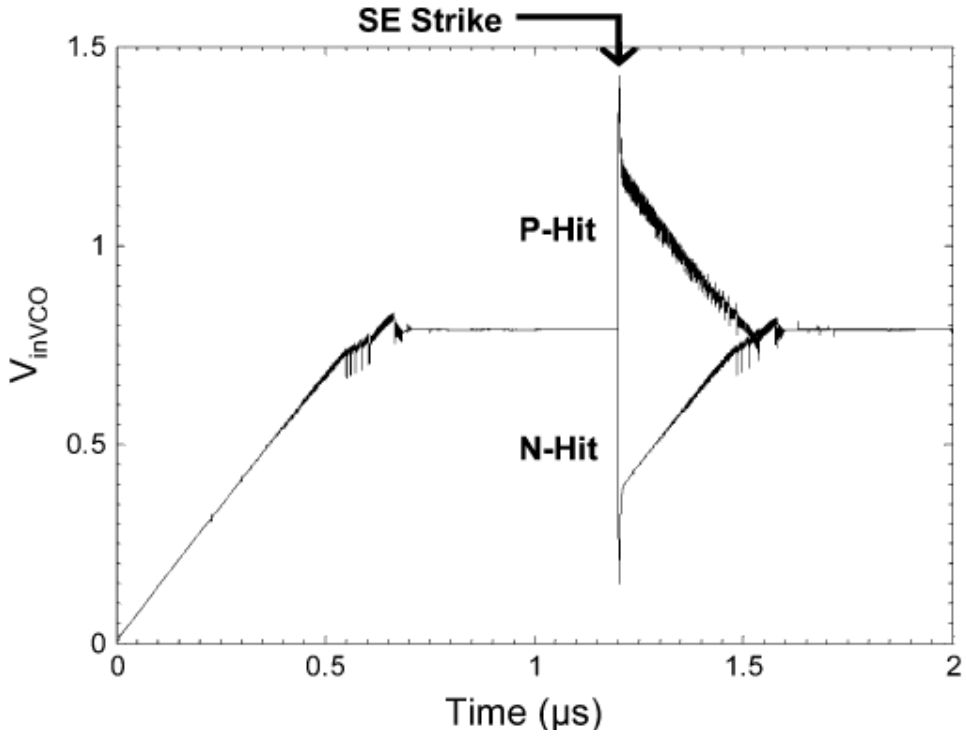


Figure 9.13 SEE hit on a voltage charge pump PLL shows a voltage perturbation of 0.62 volts and a recovery of 400nS for output frequency of 700Hz [43]

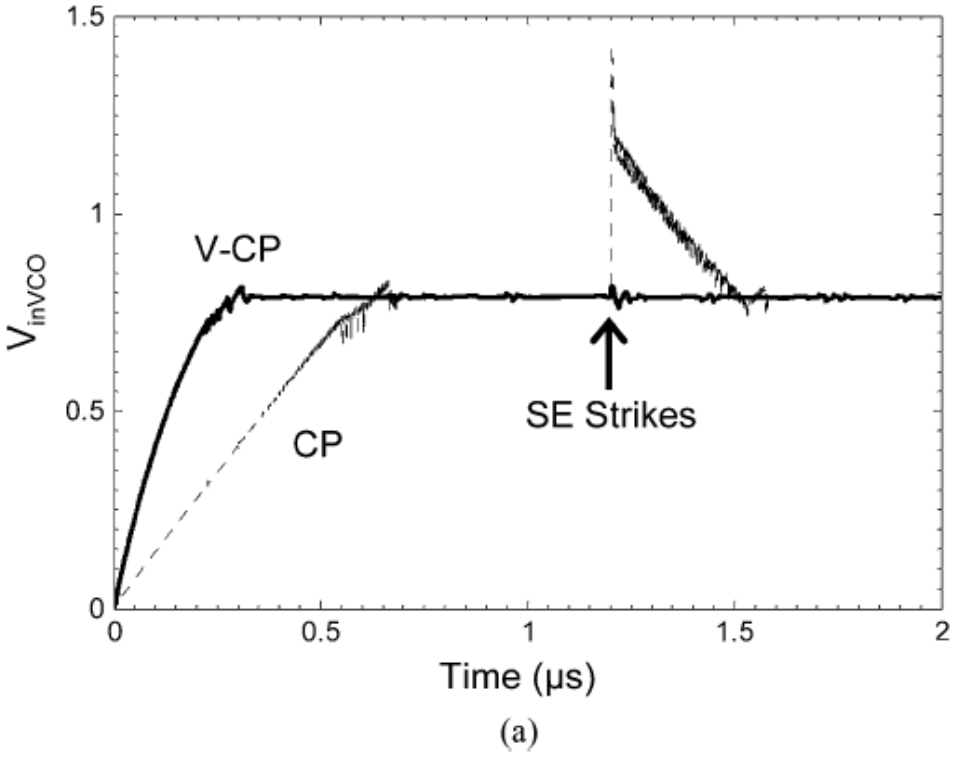


Figure 9.14 The acquisition curves illustrating the voltage perturbation resulting from SEE strikes depositing 200 fC of charge in the V-CP and the CP for 700 MHz operation. The CP exhibits a voltage perturbation of 0.64 V and a time to recovery of 400 ns while the V-CP exhibits a voltage perturbation of 42 mV and a time to recovery of 98 ns [43].

This shows the level of improvement achieved by the new PLL. The new PLL operates at a much higher frequency of 2.5 GHz compared to 700 MHz for the above PLLs, it can withstand a sudden SEE hit and charge deposition of 1.5pC compared to 200fC for the compared PLLs. In addition, the perturbation for our PLL is only 7.48mV compared to 42mV and 600mV for the other PLLs. The time to recovery for the new PLL is 184nS compared to 91nS for the voltage charge pump PLL and 400nS for the current injection charge pump PLL.

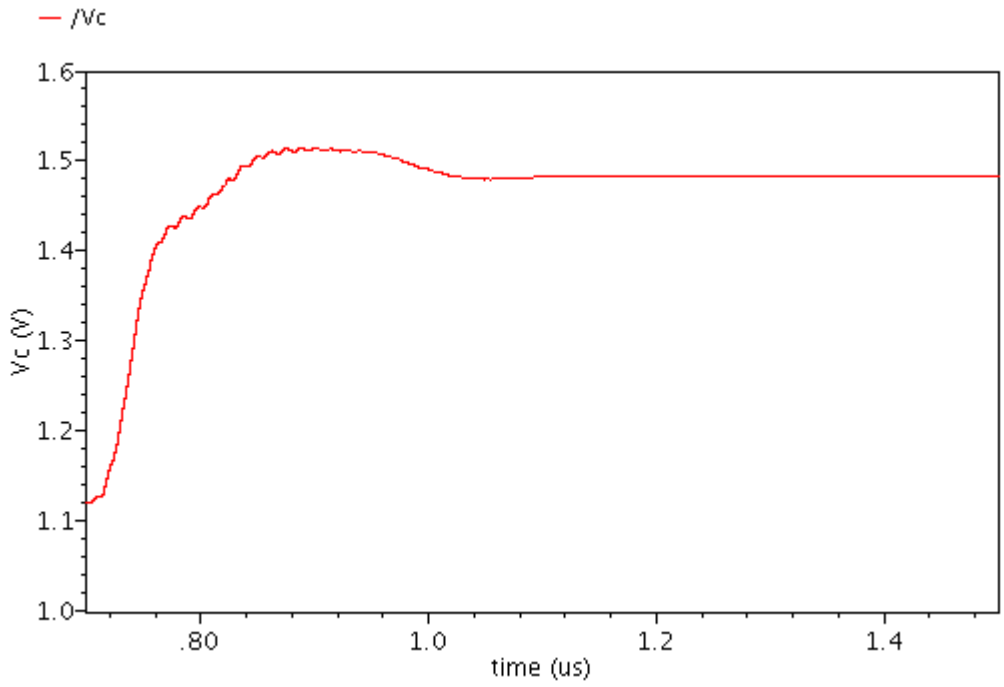


Figure 9.15 Frequency hop time of the PLL

Although, it is clear from the previous results that the PLL designed here does not lose lock or slip cycle due to SEE hits, an exercise has been performed to see how it would behave if a strong SEE disturbance throws it out of lock. For instance, let us assume that the SEE hit causes the PLL to produce an erroneous frequency of 3.1 GHz corresponding to 1.12V of V_c in the Fig. 9.15 above. It is clear from the figure that the PLL quickly goes back to the normal operation to produce 2.5 GHz corresponding to 1.483 V of V_c in Fig. 9.15. The PLL takes around 386.8 NS to hop from 3.1 GHz to 2.5 GHz, which is a spacing of 0.6 GHz.

CHAPTER 10

COMPARISON OF 0.25UM SOS PLL WITH NEWER TECHNOLOGY PLL

The 0.25um SOS CMOS technology is used because of its inherent radiation hardness characteristic as mentioned previously. The SOS process has better radiation hardness than the bulk CMOS, Bi-CMOS, BJT, SOI processes. This was shown before.

The reason for the use of 0.25um technology node on SOS process is given below. The frequency of operation required for this operation is 2.5GHz from the output of the PLL. In addition, the tuning range of the VCO incorporated in the PLL can go upto 3.1 GHz for the typical corner. It is important to consider the frequency of oscillation a particular circuit will produce during a design. This is because to choose a particular process the cut-off frequency (ft) and the maximum oscillation frequency ($f$max) of the process are to be noted. More the ft and $f$max of the process, better gain and bandwidth can be achieved. A table of comparison with the other available advanced technologies given below will show that in addition to radiation hardness, the 0.25um SOS CMOS has excellent RF characteristics.

Table 10.1 Comparison of technologies for cut-off and maximum oscillation frequency

ref	Tech	Ft	Fmax
[77]	0.25um SiGe HBT Bi-CMOS	47 GHz	> 65 GHz close to 95 GHz
[78]	0.25um CMOS NMOS	29 GHz	46 GHz
[78]	0.25um CMOS PMOS	14 GHz	27 GHz
[79]	0.18um CMOS	62 GHz	76 GHz
[80]	0.35um SiGe HBT Bi-CMOS	36 GHz	68 GHz
[81]	0.25um SOS CMOS	35 GHz	100 GHz

The above table shows that the 0.25um SOS has better ft than the bulk CMOS, while better $f$max than any other contemporary processes. This makes it an excellent RF process

candidate. $f$max acts as the figure of merit of a device beyond which an active device does not oscillate and becomes a passive device. The other advantages of SOS are given below.

0.25um SOS process has 30% more packing density than 0.25um bulk CMOS [82].

The table given below shows the advantage of 0.25 um SOS CMOS process over an advanced 130nm bulk CMOS process.

Table 10.2 Comparison of 0.25um SOS CMOS and 130nm bulk CMOS process [82]

Parameters	SOS 0.25um CMOS	130nm bulk CMOS
Leakage	Reduced substrate junction capacitor leads to lower leakage current	Higher leakage current because of substrate junction capacitor
Power	Lower power dissipation due to reduced capacitance	Higher power dissipation for similar operating frequency
Cross-talk / Substrate noise	Minimum cross-talk due to reduced substrate capacitance. high isolation > 50 dB	Substrate noise causes cross-talk between channels

Finally the PLL designed here in 0.25um SOS technology has been compared with other PLLs designed on contemporary and advanced technologies. The comparison table is shown below.

Table 10.3 Comparison of PLL performance on 0.25um CMOS and advanced technologies with PLL on 0.25um SOS CMOS.

ref		freq	tuning range	Pnoise /Jitter	power	lock	FOM1	FOM2
[64]	0.25um cmos	5.8 GHz	5.65 - 5.9 GHz	-115	33 mW	13uS	360	245
[65]	0.18um	800 MHz	0.5 - 1.1 GHz	N/A	25.15mW	6.5 uS	N/A	244.7
[66]	0.18um	5.1 GHz	4.5 - 5.4 GHz	-81.12	6.7mW	3.88u S	343	262
[67]	0.12um	4 GHz	3.8 - 4.05 GHz	-110	10.2 mW	125u S	348	238.9
[68]	0.13um	2.4GHz	2.42-2.22 GHz	-96	85mW	150u S	321	225.7
[69]	0.13um	1.22GHz	700MHz	-115	5.5 mW	1.5u S	375	260.1
[83]	90nm	200MHz	625MHz	2.68pS	4.9mW	1.3u S	N/A	252.9
[70]	0.25um cmos	1.5 GHz	1 - 2 GHz	N/A	200mW	1mS	N/A	218.8
[60]	0.25um cmos	500MHz	3.125 - 500 MHz	N/A	N/A	N/A	N/A	N/A
[62]	0.25um cmos	1.25 GHz	30 MHz - 2GHz	35 pS	300mW	15uS	N/A	237.4
[61]	0.25um cmos	1GHz	0.484-1.23 GHz	N/A	200mW	1mS	N/A	215.7
This work	0.25um SOS	2.5 GHz	0.5 - 3.1 GHz	-93/ 4.873 pS	71.8mW	525 nS	385	292

Two expressions of “figure of merit” have been derived for comparing the performances of the PLLs.

$$FOM1 = 10\log\left(\frac{Frequency * tuning\_range}{power * lock\_time}\right) - phase\_noise$$

$$FOM2 = 10\log\left(\frac{Frequency * tuning\_range}{power * lock\_time}\right)$$

They are tabulated on the last two columns of the previous table. The comparison table shows that the PLL designed here has the best figure of merits when compared to the other PLLs mentioned above.

CHAPTER 11

CONCLUSION

In this work a radiation hard PLL has been designed and laid out in 0.25um SOS CMOS technology. The simulator used is Cadence Spectre and the layout tool used is Cadence Virtuoso. The PLL designed provides a frequency output of 2.5 GHz. The PLL is designed for radiation environment. Therefore, several improvisations have been incorporated to improve the functionality and performance of the PLL under radiation environment. The first improvement is the development of a new VCO design, which has been used in the PLL. The VCO has a large tuning range of 2.76 GHz. For an output frequency of 2.5 GHz the tuning range is more than 100% of the operating frequency. The new VCO also provides an improvement in the phase noise of the VCO. The new VCO has -93dBc/Hz @ 1 MHz offset from the fundamental frequency of 2.5GHz. The new VCO has shown an improvement of 13 dB of phase noise over the simple symmetric load VCO. The use of SOS process facilitated the frequency of operation since it has a huge maximum frequency of oscillation and cut off frequency. The large cut off frequency also helps in reducing the overall noise. The PLL designed has a large loop bandwidth of 7.7 MHz. The phase frequency detector has a very high bandwidth and the charge pump designed has high level of linearity. In addition, the self-bias stage has bandwidth of more than 2.5 GHz. All these help in correcting any noise accumulation in the PLL. All these measures help in keeping the overall jitter of the PLL down to only 4.873pS for peak-to-peak jitter. The low cross talk through the substrate of the SOS process also plays a role in keeping the jitter down. After radiation, several performance parameters of the PLL are degraded. The VCO tuning range degrades by 0.9 GHz, the phase noise degrades by 3 dB, the amplitude of the output degrades by 200mV, the jitter of the PLL degrades by 6pS and the lock time of the

PLL degrades by around 90nS. An SEE simulation was done by depositing a 1.5pC of charge on the most vulnerable portion of the PLL, the output stage of the charge pump. This is an overly pessimistic choice as the SEE effects on SOS process is negligible and even in bulk CMOS process, such a high charge deposition does not happen for SEE hit. The SEE simulation shows that the PLL is a robust one as it never loses lock, since the perturbation on the control voltage was only of 7.48mV. In addition, the PLL recovers in only 184nS. The results of this simulation are far better than the other similar simulations carried out as was mentioned earlier.

CHAPTER 12

FUTURE WORK

It is required to fabricate the designed PLL in 0.25um SOS CMOS. Thereafter, the chip should be tested for performance for fresh and irradiated design. PLLs with frequencies higher than 2.5 GHz for radiation environment are under investigation. Other mixed signal circuits like ADC, DAC etc. for space applications are also under investigation. To achieve a drastic improvement in the phase noise, the operation of LC-PLL under radiation environment has to be investigated. LC-PLLs are good for low phase noise applications, but they do not have good tuning range and are not preferred in radiation environment, as they fail to achieve lock. LC-PLL with VCO having large tuning range adequate for radiation environment is needed to be developed for further improvement in performance.

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