DEVELOPMENT OF THREE BLOCK THERMAL COMPACT MODEL AND VERIFICATION OF MODIFIED LINEAR SUPERPOSITION TECHNIQUE FOR STACKED DIE

by

SURESH G. NIKALAJE

Presented to the Faculty of the Graduate School of

The University of Texas at Arlington in Partial Fulfillment

of the Requirements

for the Degree of

MASTER OF SCIENCE IN MECHANICAL ENGINEERING

THE UNIVERSITY OF TEXAS AT ARLINGTON

August 2006

"My final word of advice to you is educate, agitate and organize; have faith in yourself.
With justice on our side I do not see how we can lose our battle.
For ours is a battle not for wealth or for power.
It is a battle for freedom.
It is battle for the reclamation of the human personality"
– Dr. Babasaheb Ambedkar

This thesis work is dedicated to Dr. B. R. Ambedkar,
The Architect of Indian Constitution.

ACKNOWLEDGEMENTS

Firstly, I express my deep sense of gratitude to Dr. Dereje Agonafer, my supervising professor, guide and mentor for his never ending inspiration, guidance and support. He has been a great source of motivation through out my study at The University of Texas at Arlington. His valuable suggestions have made this work a success. Thanks to Dr. Agonafer for everything.

I thank Dr. A.Haji-Sheikh for serving in my committee. My sincere thanks to Dr. Seiichi Nomura, Dr. Kent Lawrence and Dr. Brian Huff for their encouragement and extensive cooperation through out my master's study. I take the opportunity to thank my graduate advisor Dr. Bo Ping Wang for his valuable guidance and immense support through out my master's study at The University of Texas at Arlington.

I acknowledge my parents Aai, Kaka and brother Dadya by respecting them. Thanks to god for giving me really great parents and my family especially my elder brother Uttam Dada, Vahini, Usha, Jaya, my love Sonia (Jaan) and my niece Rashmita who have always been with me and their loving care, encouragement and support has made me fulfill one of my dreams. Thanks to Ashok Mama, Ramesh Mama, Mahendra Dada, Avitatya, Anil, Sunil, my Guru Aai and all other Nikalaje family members for their support. I will always remember my brothers Late Babasaheb and Ravi and my little sister Poonam for their love.

I also take this occasion to thank my friends Amol, Pravin, Nitin, Prakash, Vikas, Milind, Dhananjay, my teachers and Dhale, Waghmare, Jadhav, Khan family and all relatives for being with me.

Thanks to EMNSPC research team, my colleagues at Ransom Hall and my friend Aravind for their help. Thanks to Divija for her never ending support, guidance and encouragement during my study at The University of Texas at Arlington. Thanks to Government of Maharashtra, India for the financial support towards my education.

July 24, 2006

ABSTRACT

DEVELOPMENT OF THREE BLOCK THERMAL COMPACT MODEL

AND VERIFICATION OF MODIFIED LINEAR

SUPERPOSITION TECHNIQUE

FOR STACKED DIE

Publication No. _____

Suresh G. Nikalaje, M.S.

The University of Texas at Arlington, 2006

Supervising Professor: Dereje Agonafer

Over the last few years an impressive amount of progress has been achieved in the field of thermal compact modeling of chip packages. But available thermal compact modeling methods could not address the issue of limitation on the mesh statistics which is major concern while modeling in FEM softwares with limited number of nodes and elements. It is not possible to attain convergence of solution for thermal simulation of detailed model with the constraint on the number of nodes and elements. In this thesis, a

simple and straight forward three block (3B) thermal compact modeling method is developed.

3B thermal compact modeling method has been implemented for numerous packages for verification of modified linear superposition technique and concluded that modified linear superposition technique is a good option for thermal characterization of stacked die with reduced modeling and simulation efforts and utilizing limited set of data from the standard thermal test.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1

INTRODUCTION

1.1 Introduction

New generation of wireless products need more functionality, lighter weight and reduced size with low cost. System in Package (SiP), a latest promising technology fulfills the current market needs. It is a functional system or a subsystem containing one or more ICs, passives and other components mounted together on the substrate to create customized and highly integrated product. SiP provides excellent solution for ease of manufacturability without compromising for cost and performance [14 to 18].

SiP solutions are increasingly found in broad range of market segments including consumer electronics, automotive, aerospace and other (medical and military) areas as shown in fig. 1.1. Fig. 1.2 shows the overall advantages of SiP solutions [13 and 15].

SiP can be defined as a Multichip module (MCM) or Multichip package (MCP) with a number of functional die attached directly to substrate or stacked in Z-direction to minimize XY package dimensions. Stacked logic plus memory or two or more memory chips on a laminated substrate in a single package is one of the fast increasing application of SiP. This stacked configuration not only reduces the system size and cost but also improves the signal transmission time and as an additional benefit, reduces power by minimizing the capacitive loads between ICs [14, 17, 18 and 19].

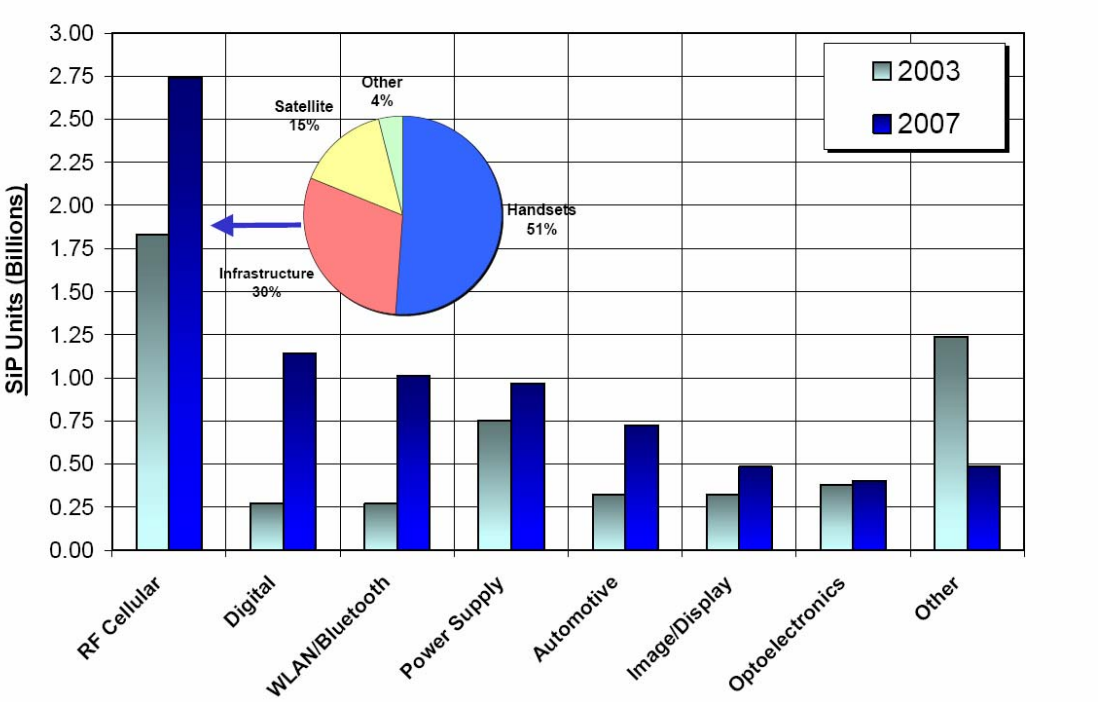


Figure 1.1: SiP market segments – 2003 [13]

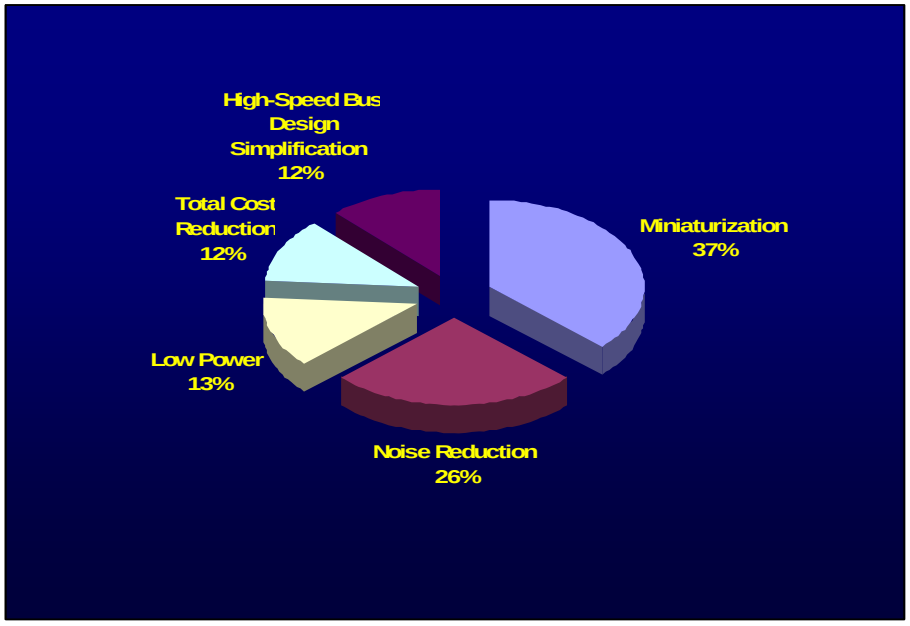


Figure 1.2: Advantages of SiP solution [15]

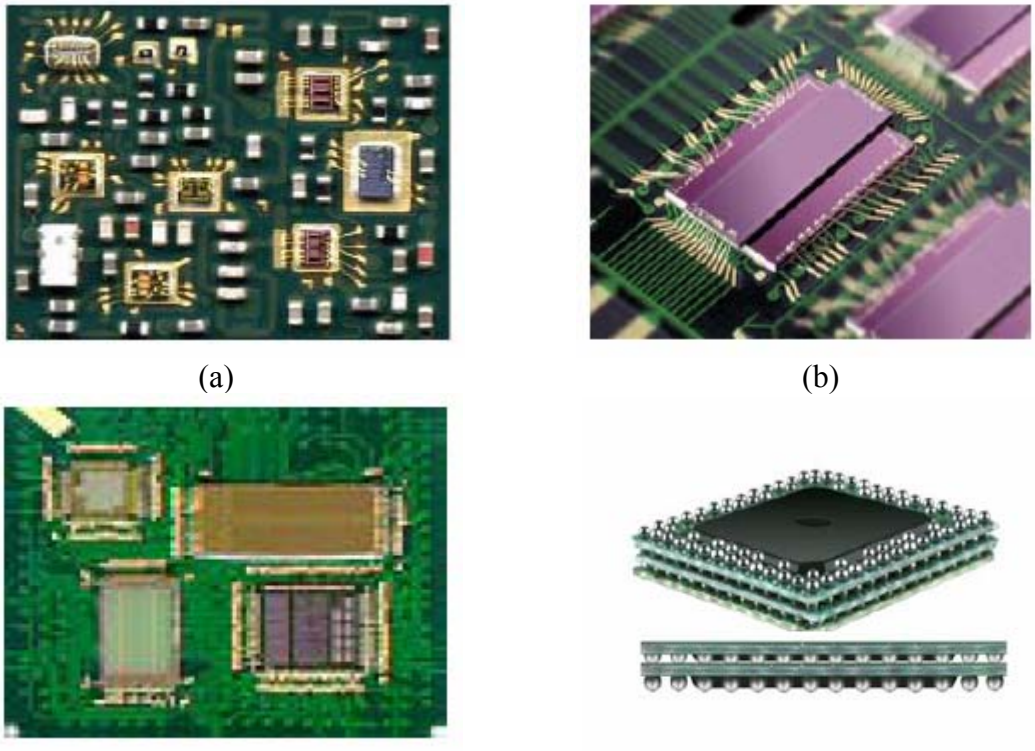


Figure 1.3: Types of SiP: (a) Module, (b) Stacked die package, (c) Multichip module, (d) 3D Packaging [14]

Based on the application, four different types of SiP namely Module, Stacked die, Multichip module and 3D-Package are currently in high demand [13]. Module is a fully functional subsystem package containing one or more chips, passive and active components on one substrate (shown in fig. 1.5(a)). In stacked die packages two or more die are vertically coupled with chip level interconnects on a single substrate (fig. 1.5(b)). In MCM two or more die are horizontally coupled with chip level interconnects on a

single substrate (fig. 1.5(c)). In 3D packaging one or more packages are vertically coupled with package level interconnects (fig. 1.5(d)).

Measuring thermal performances of stacked SiP or MCM provides additional challenges due to existence of numerous power dissipation devices on a single substrate.

Thermal resistance of a single chip package is ratio of temperature rise about reference to the total heat flow from the junction to reference.

$$R_{JX} = \frac{T_J - T_{\mathrm{Re}f}}{P} \quad \text{---------- (1)}$$

where,

R_{JX} = Junction to reference thermal resistance (ºC/ W)

$T_{\mathrm{Re}f}$ = Temperature of reference point (ºC)

T_J = Temperature of junction (ºC)

P = Heat flow rate (W)

In case of multichip module, calculation of junction to reference thermal resistance by eq (1) is complicated. MCM comprises of several die attached to substrate either laterally or stacked on one anther, and several power dissipating die confirm the additional challenges to calculate the thermal performance [1, 2, 5, 6, 7 and 8]. By using eq (1), the thermal resistance goes to infinity when power on any of the die is zero.

However, Bruce Guenin [4] developed a process to calculate temperature in MCM based on resistor network. But it can only be used when the power split ratios between various reference points in the network are known.

Linear superposition technique is effective method for thermal characterization of stacked die. Temperature distribution on any die for a given power combination, can be computed if we know the temperature on that die when each die is set to total power.

Past studies are limited to specific package configuration with an error of 2 to 20% and with limitation on total power.

It is essential to validate the linear superposition technique and determine the range of error for numerous package configurations.

Numerical analysis poses numerous troubles and issues if there is limitation on the number of nodes and elements. Finer geometries in package such as solder ball assembly and vias requires higher CPU time and greater mesh. Extended number of nodes and elements cause the general error inside the Solver module, and then it becomes necessary to reduce the number of nodes and elements to fall within the allowable limit for arriving at the numerical solution.

Model simplification, mesh control and compact modeling are some of the options to deal with the situation. For example, mesh control by sizing or any other effective method can reduce the number of nodes and elements but this approach does not result in a significant mesh reduction and corresponding CPU time. It may be possible to reduce number of elements and nodes still further by other approaches, but solution accuracy will be lost as it depends on the mesh size.

Also simplifying model to half, quarter or octane geometry with all details can reduce the number of nodes and elements but the resulting mesh reduction (although significant) still poses CPU issues.

On modeling side, research efforts are to create effective and easy to build thermal compact model, without the detailed model and that will result in a considerable mesh reduction.

1.2 Outline of Thesis

Present thesis is documented into seven chapters.

Chapter Two is focused on modified linear superposition technique for temperature prediction for thermal characterization of stacked die.

Chapter Three is emphasized on the concept of thermal compact modeling and various methods to generate thermal compact model and their validation.

Chapter Four emphasizes on 3B thermal compact modeling method developed in this research work for sub-modeling of solder ball array.

Chapter Five discusses step by step approach for modeling and thermal simulation of electronic packages in Pro-E and Ansys workbench.

Chapter Six gives results and summary of this thesis. One single chip package and 5 sets of stacked die packages with different die configurations modeled in Pro-E and simulated in Ansys Workbench for validation of 3B thermal compact model and verification of modified linear superposition technique.

Chapter Seven presents the conclusions and future work.

CHAPTER 2

MODIFIED LINEAR SUPERPOSITION TECHNIQUE

2.1 Introduction

Thermal testing of stacked die packages is a critical procedure requiring repetitive measurement of temperature on die at different power distributions. It is impractical to test temperature on each die for every possible power combination that the package may experience during the use [2, 3, 7 and 8].

Another major problem is lack of experimental setup to power more than one die at a time [8]. So currently, thermal model validated by single chip powering is utilized for thermal characterization. Application of these thermal models for thermal characterization in stacked die packages, when multiple die are powered up is again matter of concern [6 and 8].

Application of the modified linear superposition technique is very good substitute for thermal characterization of multichip packages [2, 3, 6, 7 and 8]. Limited sets of data obtained from experimental setup will give thermal performances of package for all possible power combinations. Fig. 2.1 summarizes the two processes described above for documenting thermal characteristics of MCM.

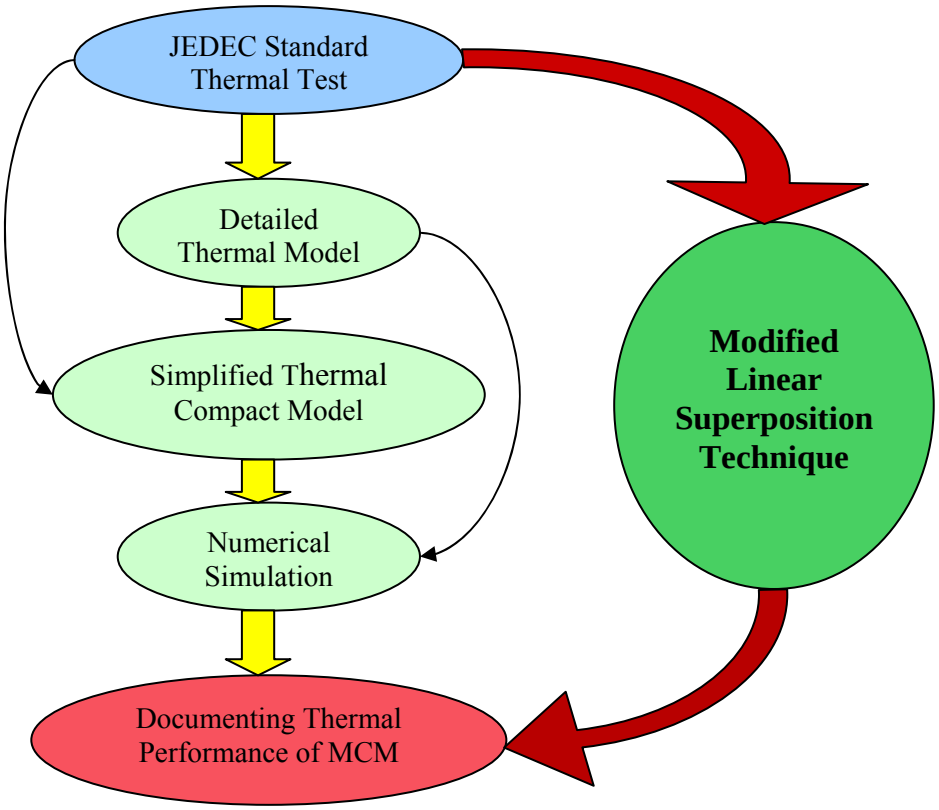


Figure 2.1: Application of the modified linear superposition technique

2.2 Temperature Prediction by Modified Linear Superposition Technique

The basic governing equations of a system with fluid flow and heat transfer [10] are:

Equation of conservation of mass:

$$\frac{D\rho}{Dt} + \nabla.(\rho V) = 0$$

Equation of conservation of momentum:

$$\frac{D(\rho u)}{Dt} + \nabla.(\rho V u) = -\nabla p + \nabla.(\mu \nabla u) + S_j$$

Equation of conservation of energy:

$$\rho c_p \frac{DT}{Dt} + \nabla.(\rho u T) = \nabla.(k \nabla T) + P$$

Here ρ is the density, V is the velocity field, p is the pressure, T is the temperature, S_j is the body force, P is the source of heat, μ is the viscosity, u is the velocity in x-direction, k is the thermal conductivity and c_p is specific heat at constant pressure.

Decoupling convective heat transfer from conduction by assuming h, and assuming that the thermal properties of material remain linear, the governing equation for steady state heat transfer through the interior package is obtained from the energy equation [1, 8, 10 and 12], and is given by:

$$k\nabla.(\nabla T) + P(X) = 0 \quad \text{-------- (1)}$$

The thermal boundary condition is as follows:

$$-k\frac{DT}{Dn} = h(T - T_o) \quad \text{-------- (2)}$$

Here T is the temperature on the boundary, T_o is the reference temperature, h is the heat transfer coefficient, k is the thermal conductivity and n is the normal to the surface. All the nonlinearities appear only at the solid/fluid boundary in the system and the mode of heat conduction inside the package is linear in nature [8]. The total heat source when two die are powered is given by:

$$P(X) = P[a\delta(X_1) + b\delta(X_2)] \quad \text{-------- (3)}$$

Here P represents the total amount of heat dissipation, a and b being the power dissipation ratio or percentage ratios of the power generation for first and second die respectively. X_1, X_2 give the location of the heat sources.

Using eq (3), eq (1) becomes modified as follows:

$$k\nabla.(\nabla T) + P[a\delta(X_1) + b\delta(X_2)] = 0 \quad \text{-------- (4)}$$

Now, we consider that only one die is applied total power at a time. When Die 1 is powered with P watt, the governing equation becomes:

$$k\nabla.(\nabla T(P,0)) + P\delta(X_1) = 0 \quad \text{-------- (5)}$$

When Die 2 is powered with P watt, the governing equation becomes:

$$k\nabla.(\nabla T(0,P)) + P\delta(X_2) = 0 \quad \text{-------- (6)}$$

Here $T(P, 0)$ is the temperature when Die 1 is given total power and Die 2 has no power applied. $T(0, P)$ is temperature when Die 1 has no power and Die 2 is fully powered.

Multiplying eq (5), eq (6) and the boundary condition in eq (2) with a and b respectively, we have

$$k\nabla.(\nabla aT(P,0)) + Pa\delta(X_1) = 0 \quad \text{-------- (7)}$$

$$-ak\frac{DT}{Dn} = ah(T - T_o) \quad \text{-------- (8)}$$

$$k\nabla.(\nabla bT(0,P)) + Pb\delta(X_2) = 0 \quad \text{-------- (9)}$$

$$-bk\frac{DT}{Dn} = bh(T - T_o) \quad \text{-------- (10)}$$

Adding eq (7) and eq (9), we get

$$k\nabla.(\nabla(aT(P,0)+bT(0,P)))+P[a\delta(X_1)+b\delta(X_2)]=0 \text{ -------- (11)}$$

Adding eq (8) and eq (10), we get

$$-(a+b)k\frac{DT}{Dn}=(a+b)h(T-T_o) \text{ -------- (12)}$$

But the total power dissipation ratio is 1 i.e.

$$a+b=1$$

So let

$$T=aT(P,0)+bT(0,P) \text{ -------- (13)}$$

Now eq (11) becomes same as eq (4), which we are solving. This implies that solution to eq (4) can be obtained from eq (13) if *T (P, 0)* and *T (0, P)* are known.

Hence the modified linear super position method says that, the temperature field *T* when Die 1 and Die 2 are powered with total power coming to *P* [8], is given by:

$$T=aT(P,0)+bT(0,P) \text{ -------- (14)}$$

More conventional form is

$$T^x(P_1,P_2)=a[T^x(P_t,0)]+b[T^x(0,P_t)] \text{ ------- (15)}$$

where x is die under consideration (top or bottom), as shown in fig. 2.2

$$a=P_1/P_t$$

$$b=P_2/P_t \text{ and}$$

$$P_t=P_1+P_2$$

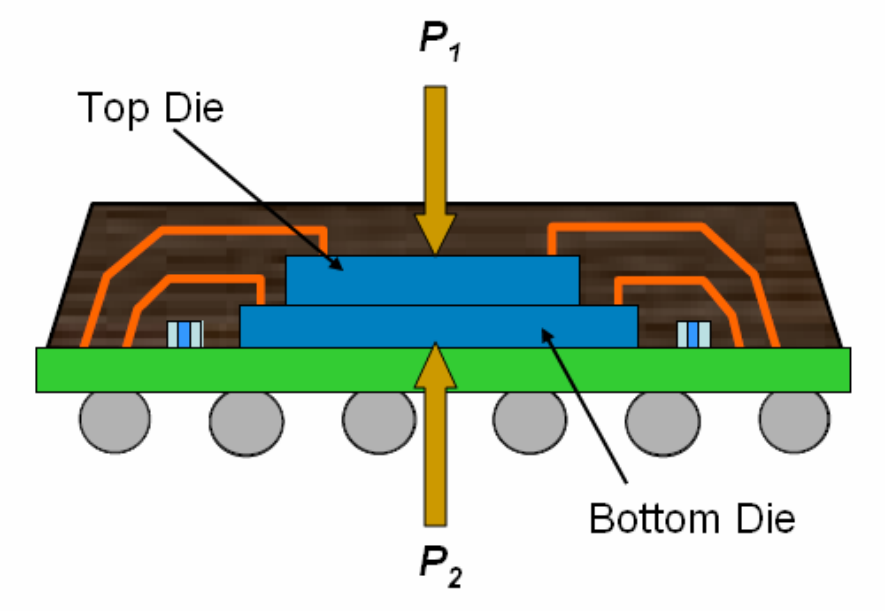


Figure 2.2: An example of two die stacked package [18]

Temperature distribution on any die with any power combination, P_1 and P_2 can be computed if we know the temperature at (P_t, 0) and (0, P_t) on die of interest by using eq (15).

CHAPTER 3

THERMAL COMPACT MODELING

3.1 Introduction

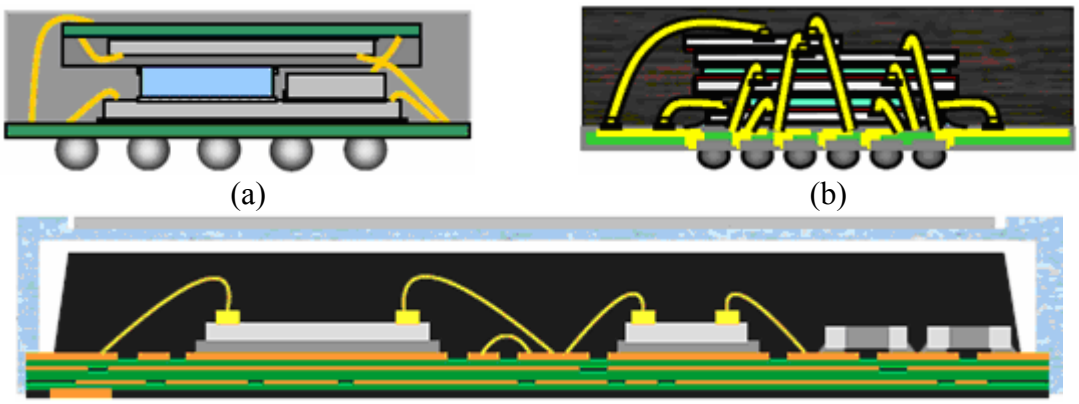
Detailed numerical analysis poses numerous troubles and issues if there is limitation on the number of nodes and elements. Finite element tool such as Ansys has wide variety of products as per the user application. For an instance, Ansys university advanced version limits the maximum number of nodes and h- elements to 128,000 and the p-elements up to a limit of 32,000 [21].

Extended number of nodes and elements cause the general error inside the solver module, and then it becomes necessary to reduce the number of nodes and elements to fall within the allowable limit for arriving at a numerical solution. Model simplification, mesh control and thermal compact modeling are some of the options to deal with this situation.

3.2 Model Simplification

Symmetry of package makes it possible to use detailed 1/2, $1/4^{th}$ and $1/8^{th}$ symmetrical models which immediately reduces the maximum node and element requirement or simply say drastically increases the computational efficiency. Due to the continued increase in complexity of package and its size, model simplification based on the planar symmetry is insufficient, especially in case of MCM with die modeled laterally

and also for the case of stacked die and package on package (PoP). For instance, special configuration shown in fig. 3.1 makes difficulty for detail or symmetric modeling of the package.



(a) (b)

(c)

Figure 3.1: Different configurations of SiP (a) LFBGA PiP [18], (b) LFBGA SD-6[18], (c) PBGA-MCM [37]

3.3 Mesh Control

FEM softwares allow mesh control by number of ways. For example in Ansys Workbench, mapped face meshing, mesh sizing, mesh sweeping and contact sizing are some of the options available [21]. Mesh control by sizing or any other method can reduce the number of nodes and elements, but this approach does not result in significant mesh reduction and corresponding CPU time. It might be possible to reduce the number of nodes and elements still further by other means, but solution accuracy will be lost as it depends on the mesh size.

3.4 Thermal Compact Modeling Methods

A thermal compact model is a simplified numerical model that has major features of the detailed model, with the advantage of low CPU usage.

There are two methods of thermal compact modeling.

1. 2R –Model
2. Delphi Boundary Condition Independent method, multiple resistor network

3.4.1 2R –Method

Junction to board resistance and junction to case resistance from the detailed model are applied to the blocks, at top and bottom of the junction block, as shown in fig. 3.2.

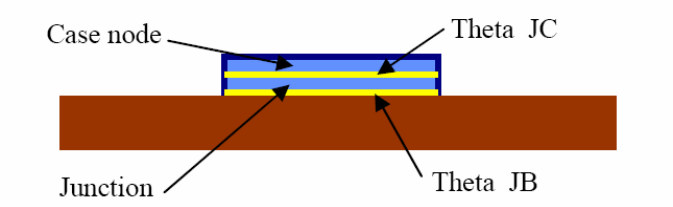


Figure 3.2: Representation of 2R- Model [29]

The equivalent thermal conductivity 'k' of lumped blocks is calculated by

$$k = L_X / (R_{JX} A_)$$

where 'L_X' is height of top or bottom block, such a way that total height of the two blocks matches closely to the total height of the package. Adiabatic boundary condition is applied on the sides of the block. This arrangement eliminates the possibility of heat

transfer through the sides of the package. 'A' is the cross section area of the block. 'R_{JX}' is junction to reference thermal resistance. A case node is modeled at top to estimate case temperature [27, 29 and 32].

3.4.2 Delphi BCI Method

Simply saying this is multi-resistor model where, number of reference points or nodes is considered on the detailed model to define the thermal resistance network and an example of Delphi model structure is as shown in fig. 3.3. The accuracy of Delphi BCI model is still a matter of dispute as it is still unclear as to what accuracy it should be compared [30, 31 and 32].

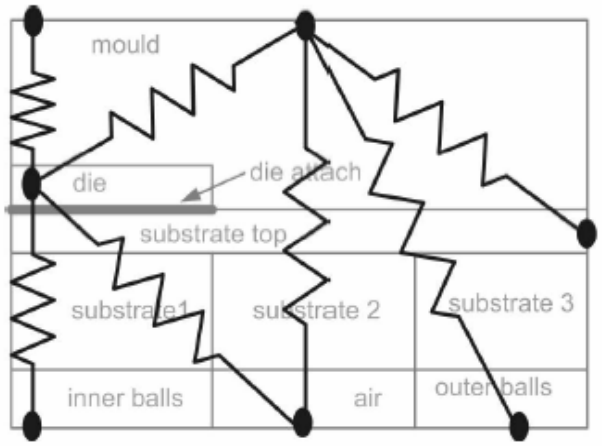


Figure 3.3: Thermal resistance network for Delphi BCI Model [30]

Approach for Delphi BCI model generation

1. create detailed model
2. apply set of all possible boundary conditions that a package may encounter in practice and calculate junction temperature and heat flow rate through each side on detailed model to define multi-resistor network

3. define “cost function” to be minimized
4. Optimize thermal network which characterizes the thermal behavior of package within the required accuracy range [33, 34 and 35].

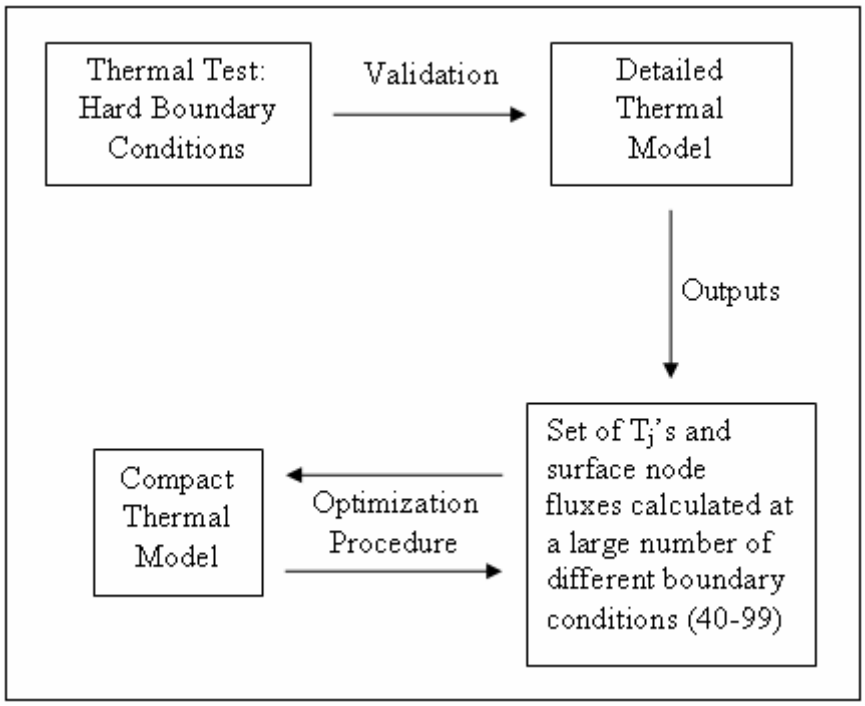


Figure 3.4: Flowchart for Delphi BCI compact model generation [35]

3.5 Validation of Thermal Compact Model

Following are the stages to validate the thermal compact model by traditional method.

1. Package is tested in hard boundary condition (environment which has conduction as well as convection) [35].
2. Outputs of all tests should be standard matrices such as Theta JA, Theta JB and Theta JC.

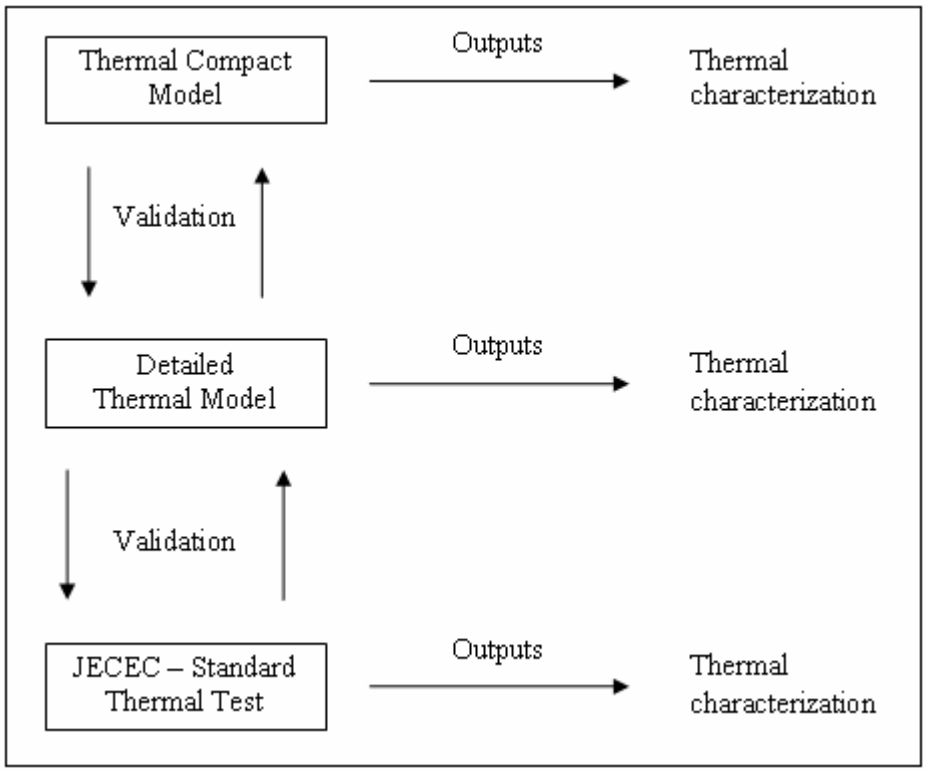


Figure 3.5: Flowchart for validation of thermal compact model [35].

CHAPTER 4

3B THERMAL COMPACT MODELING

4.1 Introduction

Solder Ball and Thermal Vias are very crucial elements for better thermal performance of the electronic packages. Finer geometric details of these elements require excessive CPU, modeling and simulation time [25]. In numerical analysis, we can replace this finer, complex and critical to built geometry with simplified or approximate shapes such as block or plate with effective thermal properties by thermal compact modeling method [25, 26, 27 and 28]. Motivated from the effective thermal compact models developed by Loh et al [26], the 3B thermal compact model is developed in the current research and applied for sub modeling of solder ball array for PBGA packages.

4.2 Desired Features of 3B Thermal Compact Model

The 3B thermal compact modeling approach developed in the current research work has been based on the following desired feature.

The thermal compact model must

1. Be independent of the detailed model.
2. Have simple geometric design requiring fewer mesh elements thereby reducing solution time with reasonable accuracy of results.
3. Perform accurate thermal behavior.

4. Model for detailed thermal features hiding the detailed geometry. Or simply say no more complexity of the model.
5. Thermal performance not affected by variation of environment.

4.3 Methodology to Build 3B Thermal Compact Model

Detail understanding of package structure is essential to implement 3B method. Based on the geometric features and design complexity, the complex components in a package need to be replaced with blocks having same thermal features.

The general steps are discussed as follows:

1. Build 3D finite element unit model showing a detail assembly of components sandwiched between 2 square blocks.
2. Apply uniform heat flux (less than 1000 W/m^2) on the top surface of upper block and convection on the bottom face of the lower block.
3. Extract thermal resistance of detailed assembly of the component.
4. Replace this complex component with an arbitrary square block and apply same boundary conditions.
5. By using Design of Experiments, determine dimensions or thermal conductivity of block to get the equivalent thermal resistance as that of detailed assembly.
6. For equivalent contact area model, modify the dimensions of block having the unchanged thermal conductivity of the component.
7. For equivalent thermal conductivity model keep the dimension stable and vary the thermal conductivity.

4.4 Solder Ball Sub Modeling by 3B Thermal Compact Modeling Method

Solder Ball Sub modeling can be done by two approaches.

- Equivalent contact area model

  - Replacing solder ball by square block or cylindrical block with thermal conductivity of solder ball.

- Equivalent thermal conductivity model

  - Replacing solder ball array by cuboidal block / plate with equivalent thermal conductivity.

4.4.1 Equivalent Contact Area Model

A unit solder ball assembly (fig. 4.1) is modeled and simulated using Pro-E and Ansys Workbench. Solder ball is sandwiched between the two blocks, with width equal to pitch of solder ball and height equal to the exact height of components. For instance top block is considered as substrate and bottom block as PWB. Applying uniform power at top of substrate block and convection at bottom of PWB, the maximum thermal resistance of solder ball is extracted.

In second stage solder ball is now replaced with cylindrical block or square block with same material properties as solder ball and maximum thermal resistance is extracted by changing the dimensions (fig. 4.2).

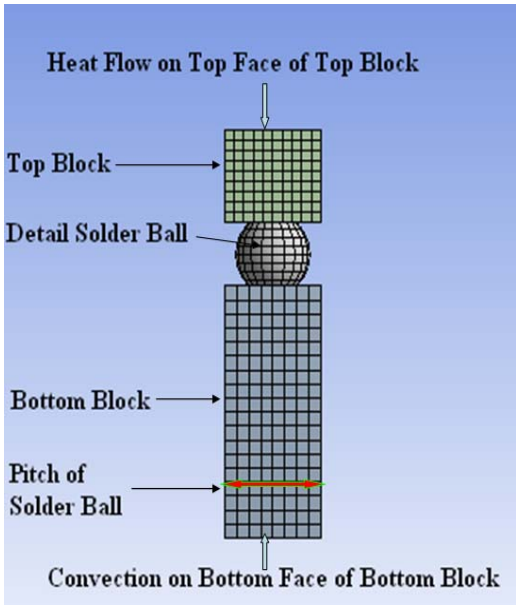


Figure 4.1: Geometry details and boundary conditions

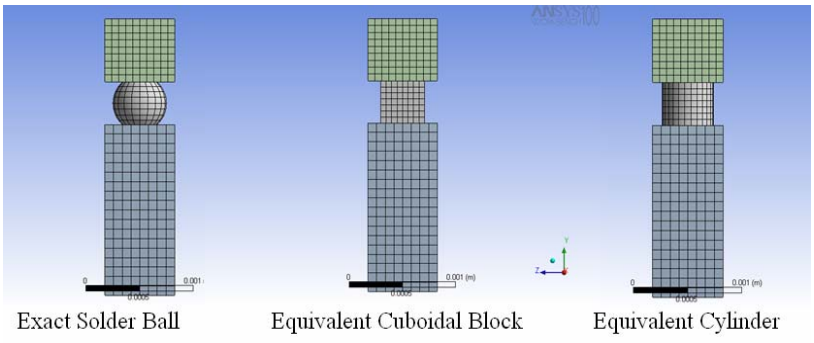


Figure 4.2: Unit cell representation of solder ball, square block and cylindrical block assembly

4.4.2 Equivalent Thermal Conductivity Model

Similar approach is adopted for the equivalent thermal conductivity model. Solder ball is replaced with a block having height same as mentioned for equivalent contact area model and width equal to the width of two blocks. Thermal conductivity is varied from 10 to 55 W/m ºC to calculate the equivalent thermal resistance across the solder ball.

4.4.3 Alternate Approaches

Instead of sub modeling for solder ball, another approach is to model the complete geometry of solder ball assembly such as top and bottom copper pad as well as solder mask as shown in fig.4.3.

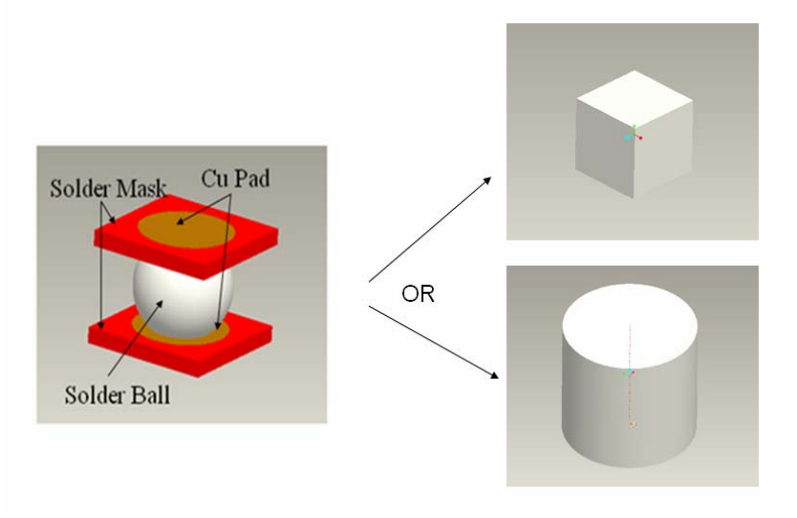


Figure 4.3: Alternate approaches to sub modeling

4.5 Advantages of 3B Method

1. It is independent of detailed model.
2. Boundary conditions and thermal conductivity of blocks are dependent on end users applications.
3. This method can be applied to copper traces in multilayer substrate or in the PWB, solder mask, copper pad, solder ball array, thermal vias in package.

CHAPTER 5

MODELING AND SIMULATION

5.1 Test Package

A single chip package (SCP) is considered for comparison with the thermal compact model and 5 sets of stacked die packages with different die configuration are considered for the simulation for verification of modified linear superposition technique.

All these 6 types of die configurations are assembled as four layers 18 X 18 mm Molded Array Plastic Ball Grid Array package, having 449 solder with 0.65 mm pitch [1 and 9] connected with 36 through thermal vias (assumed). Dimensions of package are given in table 5.1. These packages are mounted on 100mm x 100mm x 1.6mm FR4 Printed circuit board containing two copper layers for heat spreading purpose [36]. Such kind of packages are widely used in ASIC, DSPs and memory, microprocessors /controllers /graphics, PC chipsets, and other advanced applications requiring enhanced thermal and electrical performance [37].

The symmetry of package makes it possible to use 3D $1/4^{th}$ symmetrical model, which immediately reduces the maximum nodes and elements requirement. Fig. 5.1 shows a one fourth detail model built in Pro-E. It is very critical to create copper trace in the detail model, so for thermal analysis copper traces are represented with effective thickness [22 and 36]. For simplicity of model wire bonding is not considered because

thermal effect of gold wire bonding is negligible [28]. Thermal vias are modeled as solid cylinders with 0.1 mm diameter.

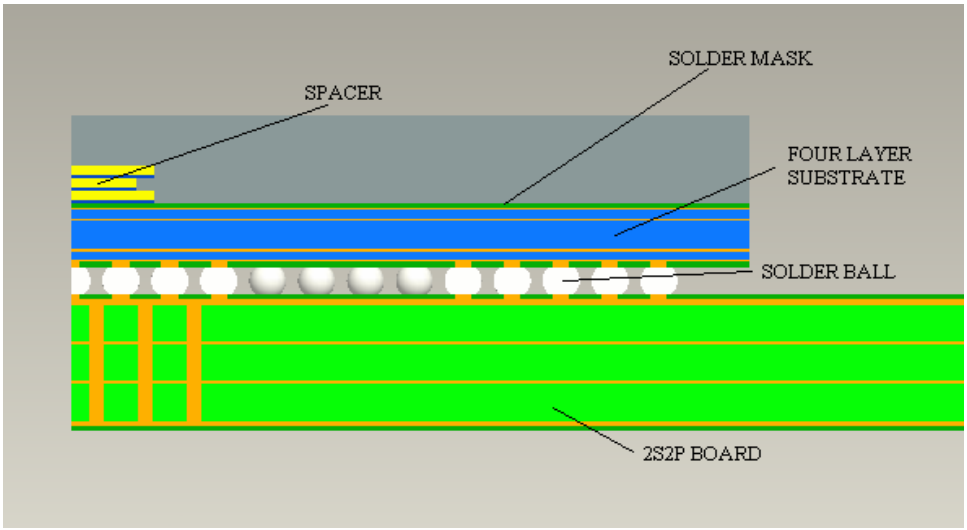


Figure 5.1: Pro – E detail model of 449 MAP PBGA

Table 5.1: Package dimensions

Components	Dimension
Die	1.7 mm x 3.1 mm x 0.14 mm 2.2 mm x 3.6 mm x 0.14 mm 4.4 mm x 7.3 mm x 0.14 mm 8.5 mm x 9.5 mm x 0.14 mm
Die Attach Paste Thickness	0.03 mm
Die Attach Film Thickness	0.03 mm
Mold Cap Thickness	0.8 mm
Solder Ball	Total 449 , Pitch 0.65 mm
Solder Mask thickness	0.075 mm
Spacer	1.7 mm x 3.1 mm x 0.14 mm 4.4 mm x 7.3 mm x 0.14 mm
Substrate	4 layer substrate size 18 mm x 18 mm Cu layer 0.025 mm thick Two layer of Epoxy Glass, 0.12 mm thick Middle 0.4 mm thick BT core layer.
PWB	100 mm x 100 mm x 1.60 mm Cu layer, 0.035 mm thick Vias 0.1 mm dia.

Thermal simulation is carried out in Ansys workbench. Total one watt power is applied on die and maximum junction temperature is measured under natural and forced convection boundary conditions.

5.2 Modeling and Simulation Methodology

Every single part need to be build separately and then assembled together into the package. Selection of sketch plane and reference plane plays an important role while combining parts in to assembly. With clear understanding of geometrical feature, dimension, units and by efficient use of parent child relation one can make very critical and complex shape in reasonable time. Simple method with general steps is defined in table 5.2 [23].

Table 5.2: Simple method for the modeling of package components

COMPONENT	GEOMETRY	METHOD
Die, Die Attach, Mask, Layers in Substrate and PWB, Mold Compound, etc	Rectangular, Square Block, Plate, etc.	Draw Rectangle > Extrude & define thickness
Solder Ball	Sphere and plane cut from top and bottom	Draw Semicircle > Revolve > Extrude to remove material from spheres top and bottom
Vias	Solid or Hollow cylinder	Draw Circle > Extrude to Height > use hole for hollow cylinder.
Cu Pad	Circular Plat	Draw Circle> Extrude
Substrate layer with holes for vias	Plate with Hole	Draw Rectangle > Extrude> Define thickness> Use hole tool or draw another circle and extrude to remove material to form vias

5.2.1 Major steps while creating parts using Pro-E

- Create each part as solid
- Set units, use consistent set of unit for each part as well as for assembly
- Define or assign material and save
- Start with basis feature such as Extrude or Revolve tool
- Define sketch, reference and orientation planes for sketch. It's very important at time of assembly
- Define thickness, angle of rotation; Select add or remove material in placement panel
- Change the color for appearance and save

5.2.2 Major steps while Assembly Design using Pro-E

- Set units, same system as defined for each part
- Start with 'Add components to assembly' tool
- Import first item and set to default location using component placement window
- Import subsequent part and assemble together using constrains as mate, align, insert, etc.
- Use surface, axis, plane, vertex, curve end, or edge on one part for constrain
- Constrain till the component placement window shows "fully constrain" placement status
- Save the changes

5.2.3 Simulation using Ansys Workbench

Save and close all Pro-E applications and launch the new Ansys workbench project. Single click on geometry icon in start window. Design Modeler will open up. Set the unit system and then import the Pro-E assembly along with the material properties. Define the symmetry and carry geometry to workbench simulation. Fig. 5.2 represents the Pro-E modeling process and the steps in Ansys workbench project [24].

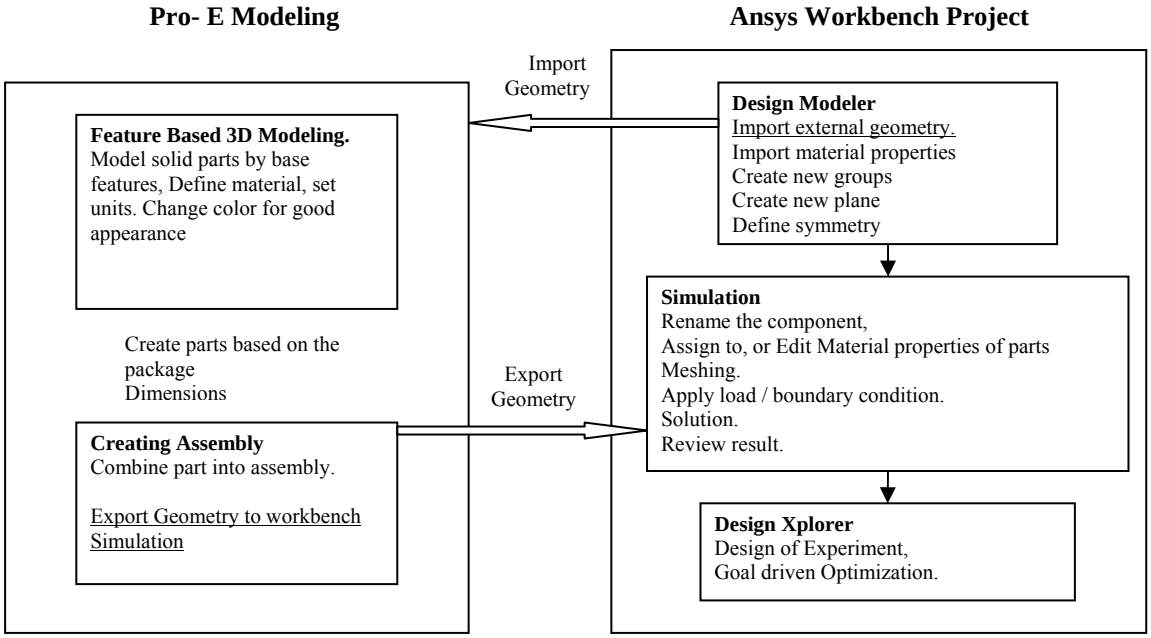


Figure 5.2: Pro-E modeling process and steps in Ansys workbench [23 and 24]

It's worthwhile to rename each part in simulation and then assign proper material properties. Only thermal conductivity is enough for steady state thermal analysis. Right click and select preview mesh, and wait. After default mesh is created, apply the thermal load and run the solution [24].

CHAPTER 6

RESULTS AND SUMMARY

In current research work 3B thermal compact modeling approach is used to build one single chip package (SCP) and 5 sets of stacked die packages with different die configuration are modeled using Pro-E and simulated in Ansys workbench for verification of the modified linear superposition technique. 3B thermal compact model is validated by comparing with the detail SCP.

6.1 3B Thermal Compact Modeling Approach for SCP (Package 1)

Single chip 449 MAP PBGA (Package 1) is built in Pro-E, as described previously and successfully imported into workbench. At beginning of the solution, the number of node was 147081 and number of elements 22850 which was greater than the allowable limit. It was drastically reduced to 93563 and 12680 respectively by mesh sizing.

Table 6.1: Material properties

Component or Material	*Thermal Conductivity W/m ºC*
Silicon	120
Die attach paste	0.3
Die attach film	0.2
Mold compound	0.9
Bt Substrate	0.34
Copper	360
Solder Mask	0.25
FR4	0.34
Solder Ball	50

SOLID87, SOLID90, CONTA174 elements were used for data processing in the FEM solver. The maximum junction temperature obtained is 59.6ºC in natural convection. The material properties used for detail model simulation are given in table 6.1.

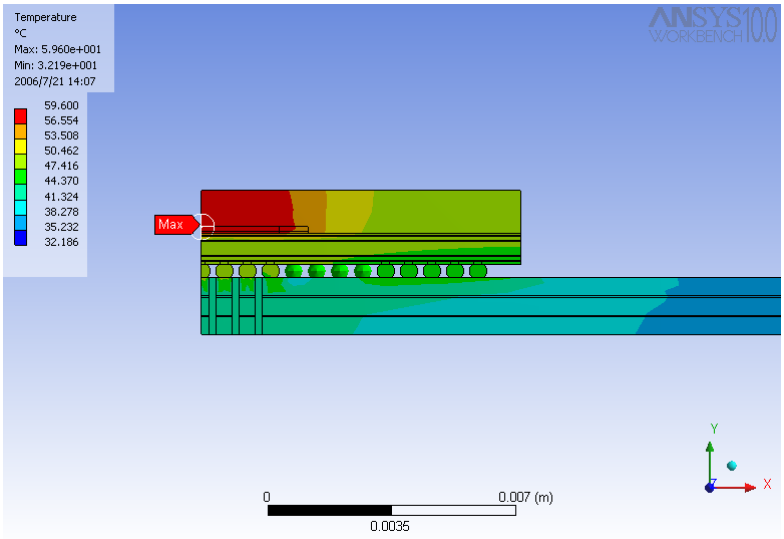


Figure 6.1: Temperature profile for detailed SCP

6.2 Equivalent Contact Area Model by 3B Method

Solder ball is now replaced with square block (fig. 6.2) and cylindrical block (fig. 6.4) with same material properties as solder ball and maximum thermal resistance is extracted by changing the dimensions.

For square block, results obtained from this approach are tabulated in table 6.2 and plotted in fig. 6.3. Similarly the results for cylindrical block are given in table 6.3 and fig. 6.5. It has been observed that as the contact area increases thermal resistance gets

reduced. Equivalent thermal resistances for square block and cylinder are summarized in table 6.4.

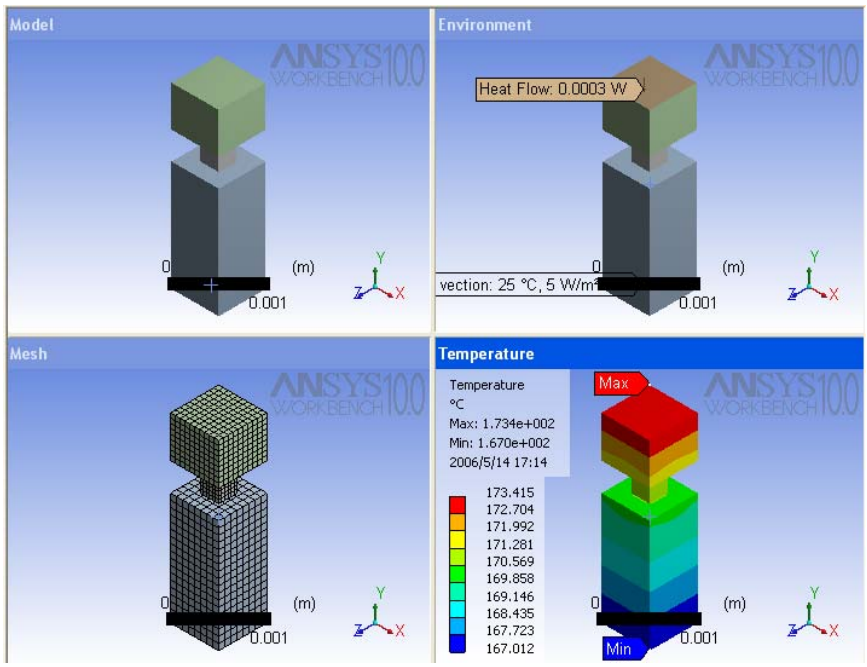


Figure 6.2: Solder ball as square block

Table 6.2: Thermal resistance for varying block side

Block Side (mm)	Thermal Resistance (ºC/W)
0.25	360
0.3	280
0.35	190
0.4	156
0.405	146.66
0.41	133.33
0.412	130
0.413	123.33
0.415	113.33

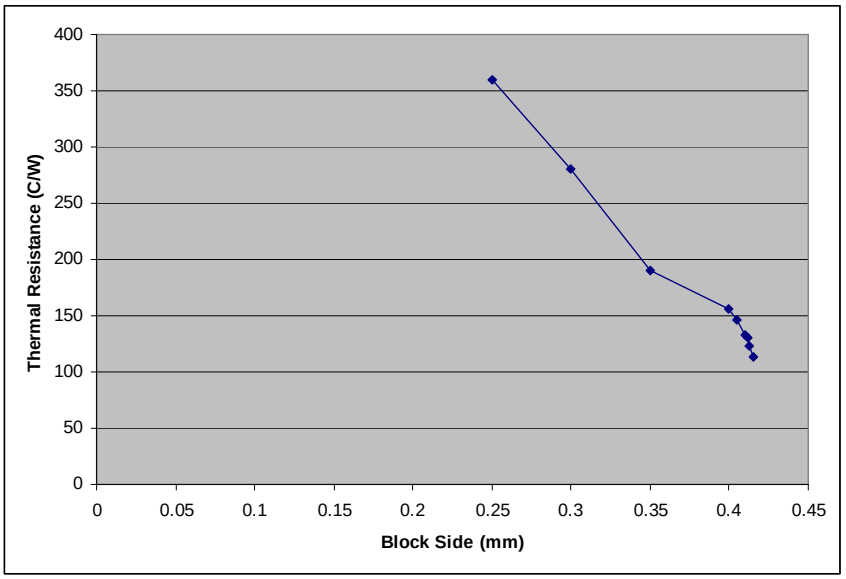


Figure 6.3: Variation of thermal resistance with block side dimension

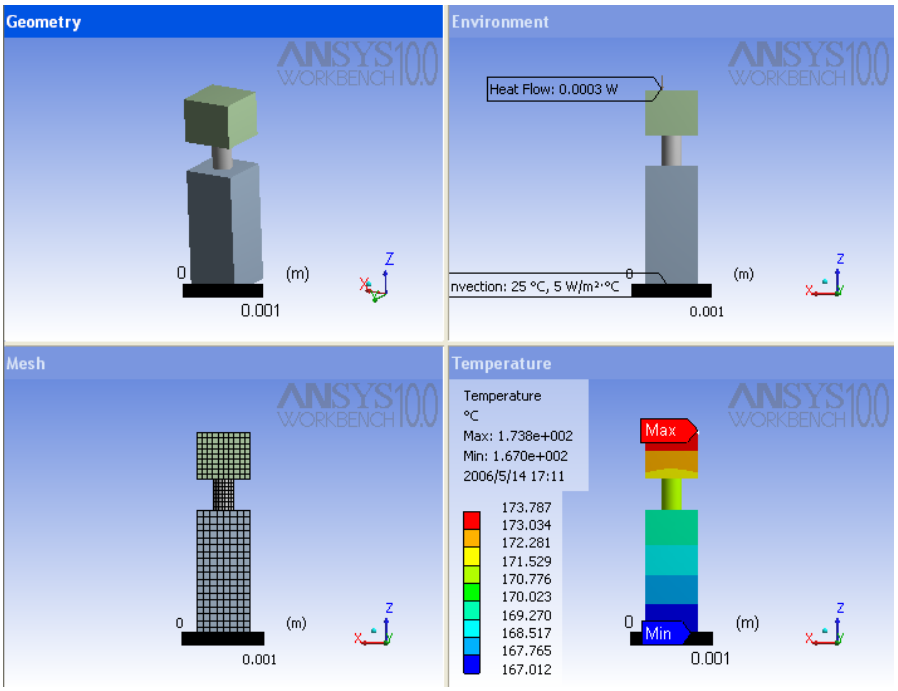


Figure 6.4: Solder ball replaced with cylindrical block

Table 6.3: Thermal resistance for varying cylindrical block dimension

Cylinder Diameter (mm)	Thermal Resistance (ºC/W)
0.25	310
0.26	310
0.28	280
0.3	230
0.33	206
0.38	150
0.4	150
0.41	156
0.42	150.333
0.43	136.66
0.44	120

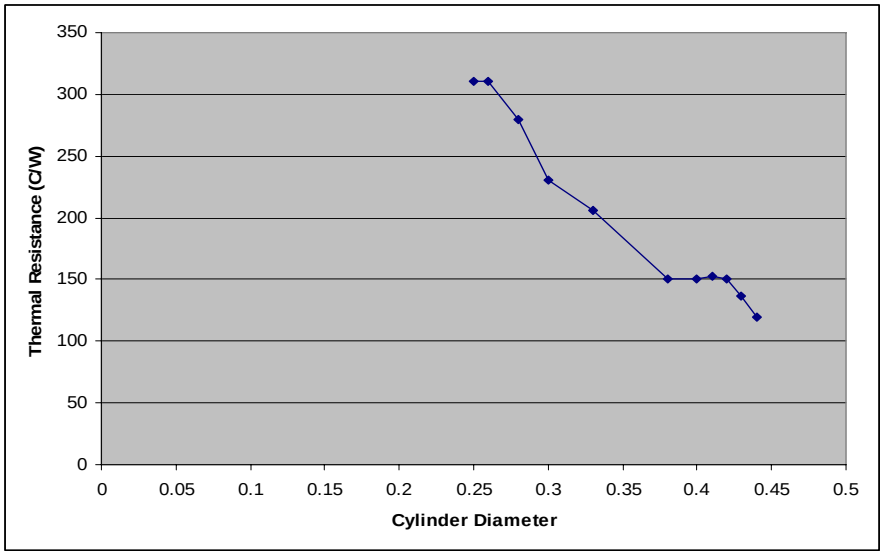
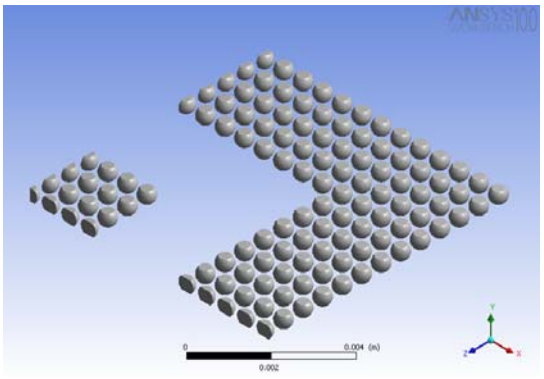


Figure 6.5: Variation of thermal resistance with cylindrical block dimension

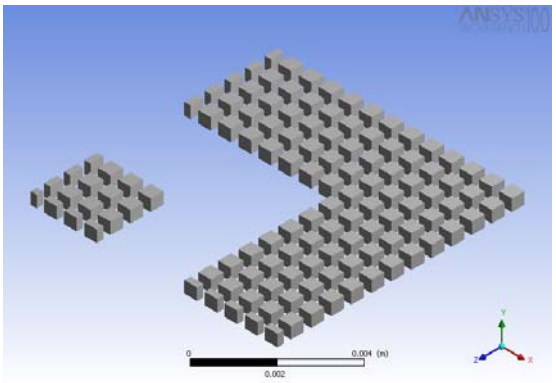
Table 6.4: Result summary for equivalent area model

Geometry	Dimensions (mm)	Thermal Resistance (^{o}C/ W)
Solder Ball	r = 0.16, R = 0.25 & h=0.38	120.00
Cylinder	D = 0.44 & h=0.38	120.00
Block	(a) ^{2} = (0.413) ^{2} & h=0.38	123.33

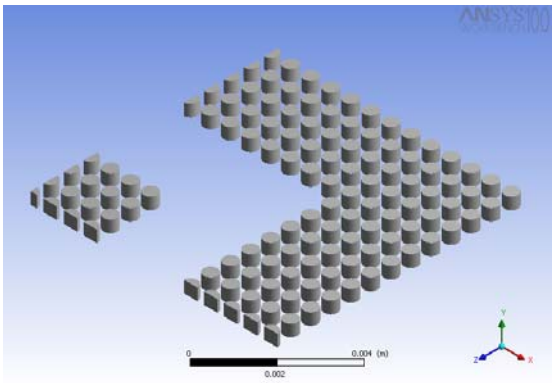
Graphic representation of solder ball array when solder ball is replaced by square or cylindrical block as per the dimension obtained from table 6.4 are shown in fig. 6.6.



(a)



(b)



(c)

Figure 6.6: Solder ball arrays by equivalent contact area model (a) solder ball, (b) square block, (c) cylindrical block

6.3 Equivalent Thermal Conductivity Model

In the equivalent thermal conductivity model, solder ball, bottom solder mask and bottom copper pad are now replace with a block. Top solder mask and top copper pad are modeled as a single plate with equivalent thermal conductivity (fig. 6.7). Dimensions are same as mentioned for equivalent contact area model. Thermal conductivity is varied

from 10 - 55 W/m ºC to calculate the equivalent thermal resistance across the solder ball using DOE Optimization module in Ansys workbench [24].

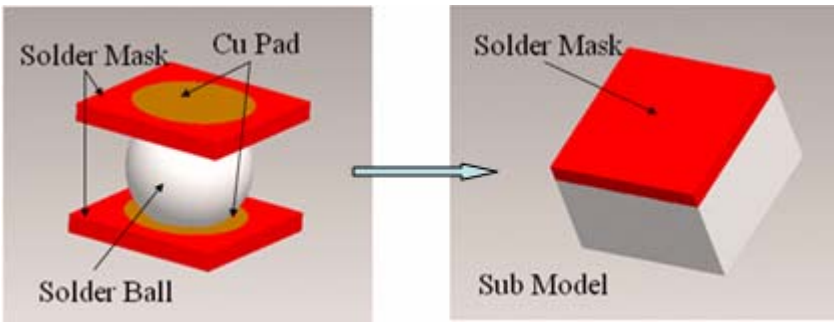


Figure 6.7: Sub modeling approach for equivalent thermal conductivity model

6.3.1 DOE Optimization Module in Ansys Workbench, for 3B Thermal Compact Modeling Method

- Goal driven optimization is carried out for the thermal resistance of solder ball.
- Thermal conductivity of solder ball is defined as input parameter.
- The lower and upper bounds are set to 10 W/m ºC and 55 W/m ºC respectively.
- New derived parameter (solder ball thermal resistance) is defined as the ratio of temperatures difference between top and bottom faces of block to the power applied at the top of substrate.

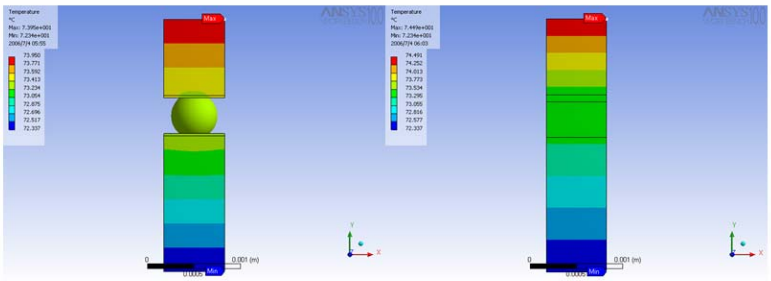


Figure 6.8: 3B Thermal compact model for equivalent thermal conductivity

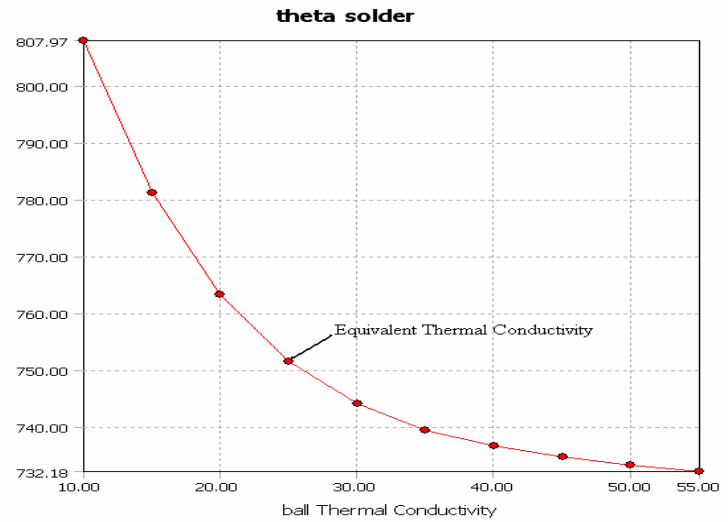


Figure 6.9: DOE result for equivalent thermal conductivity

Graphic representation of solder ball array when solder ball is replaced by cuboidal block with equivalent thermal conductivity is shown in fig. 6.10.

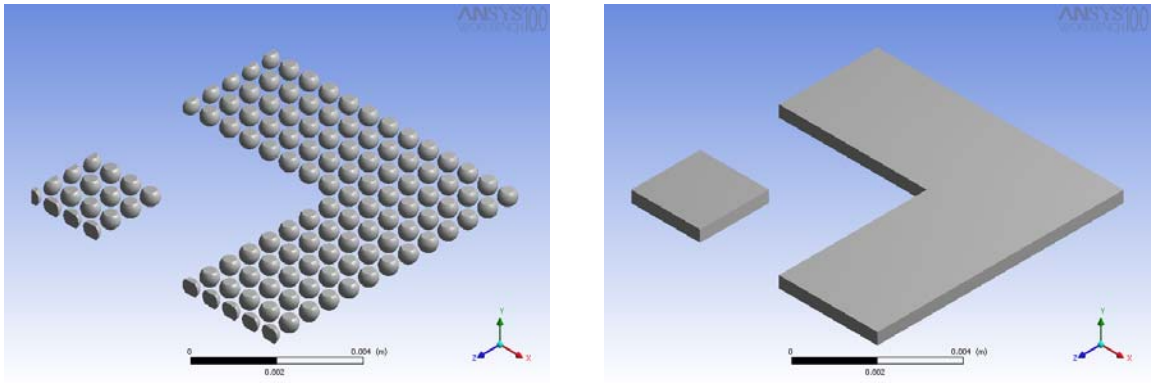


Figure 6.10: Solder ball array replaced by cuboidal block

Table 6.5: Mesh statistics for different solder ball arrays

Geometry	*No. of Elements*	*No. of Nodes*
Solder Ball	7669	16614
Cylinder	1943	5914
Block	1368	4127
Plate	55	151

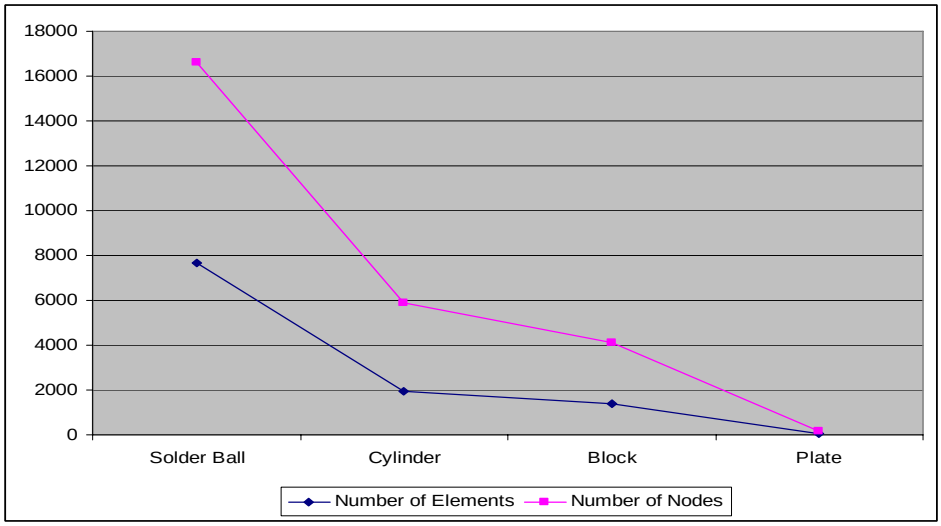


Figure 6.11: Mesh statistics for different solder ball array at constant element size

It can be observed from table 6.5 and fig. 6.11 that number of nodes and elements for cuboidal plate are very small when compared to square or cylindrical block.

SCP with die dimensions 4.4 mm x 7.3 mm x 0.14 mm is now modeled with cuboidal plate (fig. 6.12) and maximum junction temperature of 57°C is obtained at natural convection (fig. 6.13). Table 6.6 gives the percentage gain obtained in different areas by implementation of 3B model for SCP.

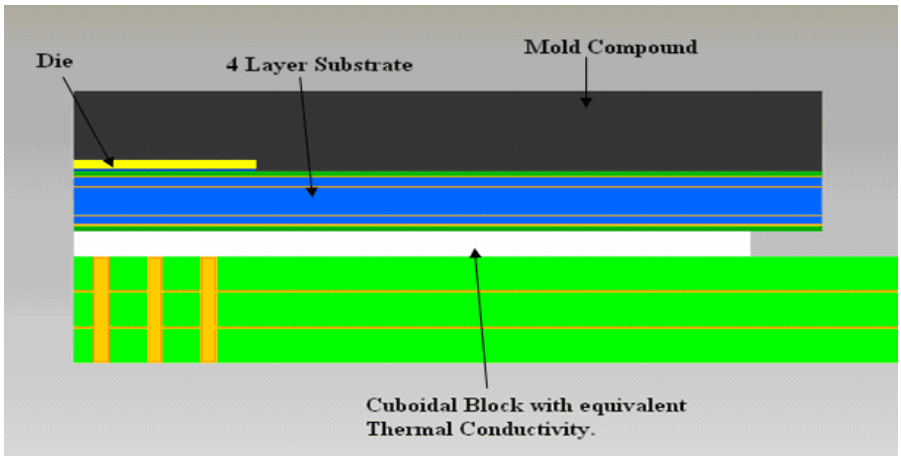


Figure 6.12: Single chip package with cuboidal block (Package 1)

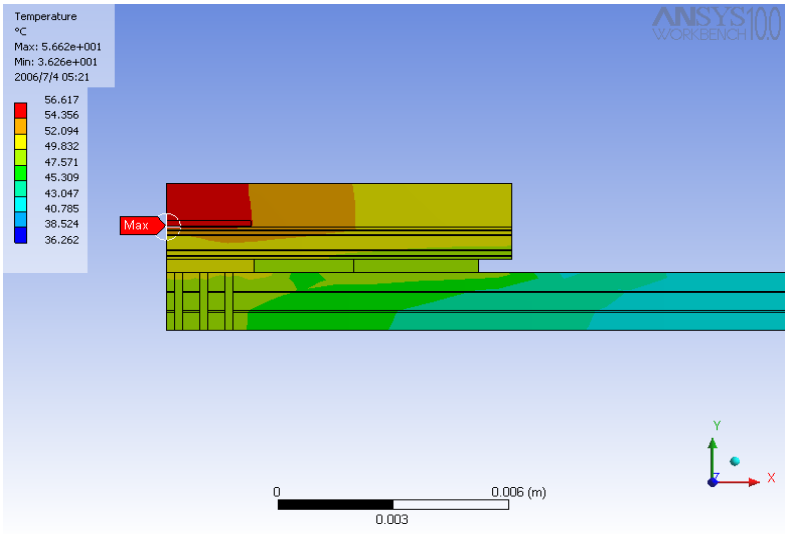


Figure 6.13: Temperature profile of SCP (Package 1)

Table 6.6: Observations for SCP

	Mesh control	*3 B Thermal Compact Model*	*Advantages*
No of Nodes	93563	43242	53.8 % Reduction
No of Elements	12680	6324	50.1 % Reduction
Solution Time	5 min 17 sec	2 min 36 sec	54.2 % Saving
Max. Temp. (°C)	59.60	56.61	5 % Error

Similar approach is adopted for 3B model of same size die on die stacked package. Observations are tabulated in table 6.7.

Table 6.7: Observations for same die on die stacked package

	Mesh control	*3 B Thermal Compact Model*	*Advantages*
No of Nodes	83646	42984	48 % reduction
No of Elements	10323	6245	40 % reduction
Solution Time	13.25 min	2.32 min	83 %Saving
Max. Temp. (°C)	67.22	66	1.81 % Error

6.4 Stacked 1 Functional plus 2 Dummy Die Package (Package 2)

Package with one functional die (4.4 mm x 7.3 mm x 0.14 mm) and two dummy die (8.5 mm x 9.5 mm x 0.14 mm) is modeled as shown in fig. 6.14. Total power of 1 watt is applied on top functional die. The maximum temperature observed is 55.7°C. A difference of 0.91°C is observed in the maximum temperature of this package when compared to the SCP. Hence it can be conclude that the 3B thermal compact model developed in this research can be applied to stacked die configurations,

For better accuracy of results it is essential to model each die separately while developing the thermal compact model [1].

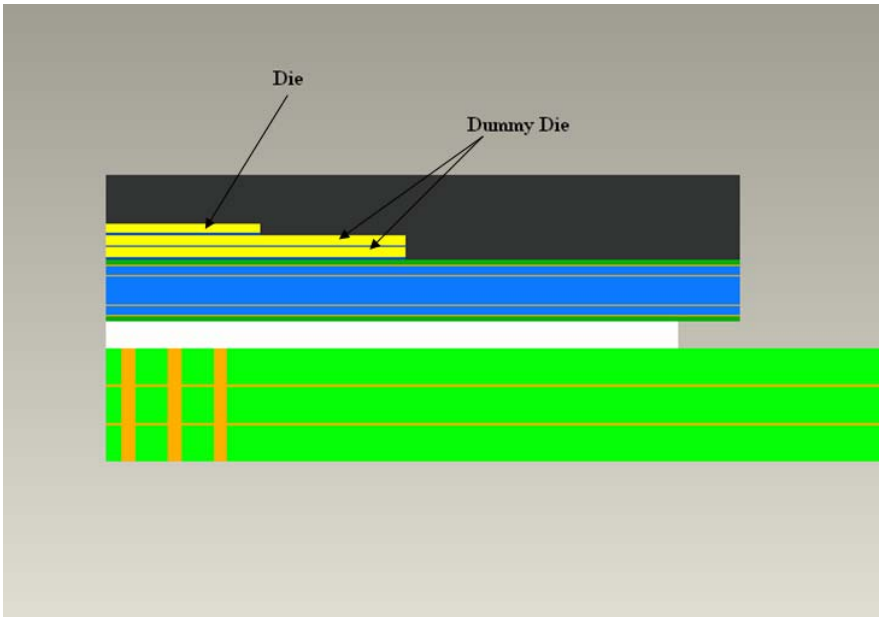


Figure 6.14: 1 Functional + 2 Dummy Die Stacked Package (Package 2)

6.5 Verification of Modified Linear Superposition Technique

Four different types of stacked die configuration are simulated for natural as well as forced convection boundary conditions and verified the modified linear superposition technique.

6.5.1 Package 3

Same size die (2.2 mm x 3.6 mm x 0.14 mm) stacked package, a spacer (1.7 mm x 3.1 mm x 0.14 mm) of thermal conductivity 0.45 W/m°C is placed between two functional die for the clearance of bottom die wire bonding (fig. 6.15). Such packages are used in memory applications like DRAM [11 and 13]. Disadvantage of the presence of spacer is increase in total height of the package [20].

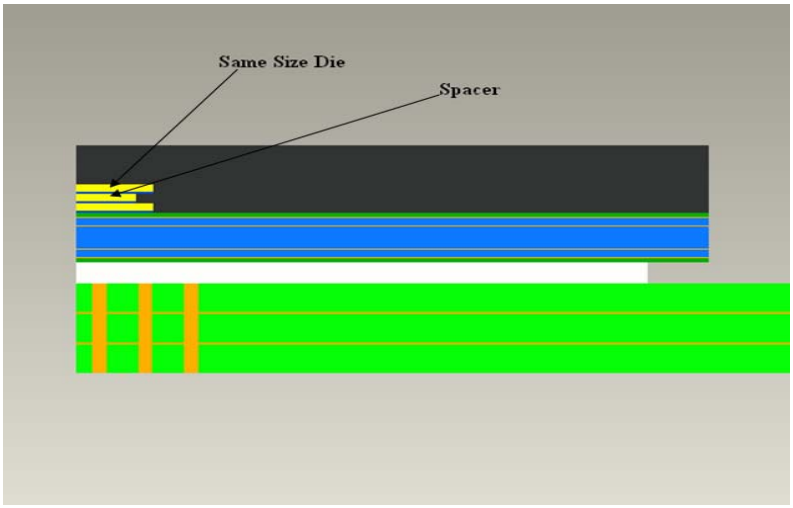


Figure 6.15: 2 Same Size Die + 1 Spacer Stacked Package (Package 3)

Boundary Conditions

Film Coefficient, h = 3 W/m^2 °C and Ambient Temperature = 22 °C

Total Power on Package =1 W

Table 6.8: Initial condition for total power 1 watt (Package 3)

Power on Top Die (W)	Power on Bottom Die (W)	Maximum Temp. on Package (°C)	Top Die Temp. (°C)	Bottom Die Temp. (°C)	Board Temp. (°C)
1	0	75.78	75.78	57.21	49.23
0	1	59.93	56.31	59.54	49.35
1	1	110.08	110.08	94.75	76.58

Table 6.9: Verification of modified linear superposition technique for total power 1 Watt (Package 3)

Power on Top Die (W)	Power on Bottom Die(W)	Maximum Temp. on Package(°C)	Top Die Temp. (°C)		Bottom Die Temp. (°C)		Board Temp. (°C)
			Ansys WB	Linear Sup.	Ansys WB	Linear Sup.	
0.25	0.75	61.17	61.17	61.18	58.96	58.96	49.32
0.5	0.5	66.04	66.04	66.04	58.37	58.37	49.29
0.75	0.25	70.91	70.91	70.91	57.79	57.79	49.26

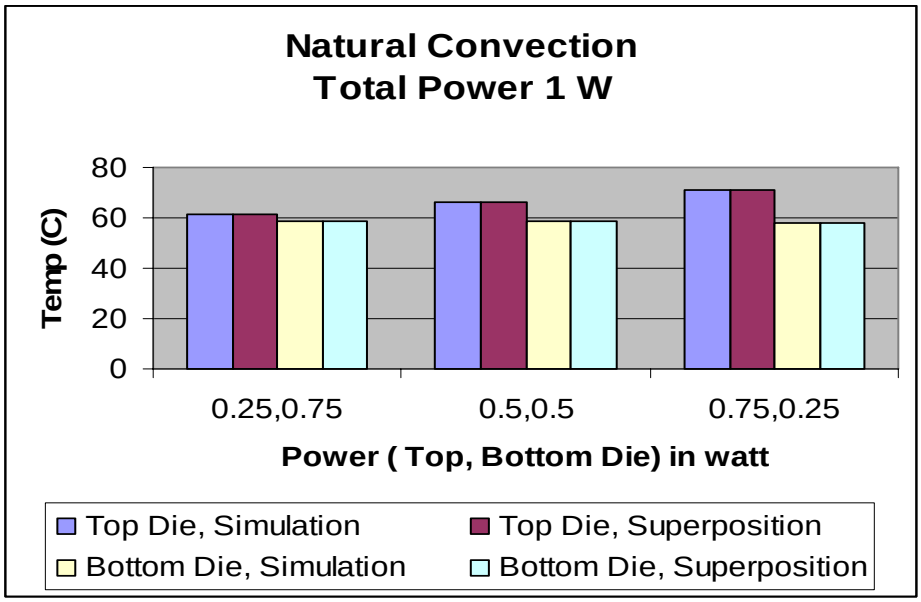


Figure 6.16: Package 3 Natural convection, Power 1 watt

Boundary Conditions

Film Coefficient, h = 3 W/m^2 °C

Ambient Temperature = 22 °C

Total Power on Package =2 W

Table 6.10: Initial condition for total power 2 watt (Package 3)

Power on Top Die (W)	Power on Bottom Die(W)	Maximum Temp. on Package(°C)	Top Die Temp. (°C)	Bottom Die Temp. (°C)	Board Temp. (°C)
0	2	97.86	90.63	97.08	76.71
2	0	129.55	129.55	92.41	76.46

Table 6.11: Verification of modified linear superposition technique for total power 2 Watt (Package 3)

Power on Top Die (W)	Power on Bottom Die(W)	Maximum Temp. on Package (°C)	Top Die Temp. (°C)		Bottom Die Temp. (°C)		Board Temp (°C)
			Ansys WB	Linear Sup.	Ansys WB	Linear Sup.	
0.25	1.75	97.24	95.48	95.49	96.5	96.5	76.68
0.5	1.5	100.35	100.35	100.36	95.91	95.91	76.65
0.75	1.25	105.22	105.22	105.23	95.33	95.33	76.612
1	1	110.08	110.08	110.09	94.75	94.75	76.6
1.25	0.75	114.95	114.95	114.95	94.16	94.16	76.56
1.5	0.5	119.82	119.82	119.82	93.58	93.58	76.53
1.75	0.25	124.68	124.68	124.68	92.99	92.99	76.49

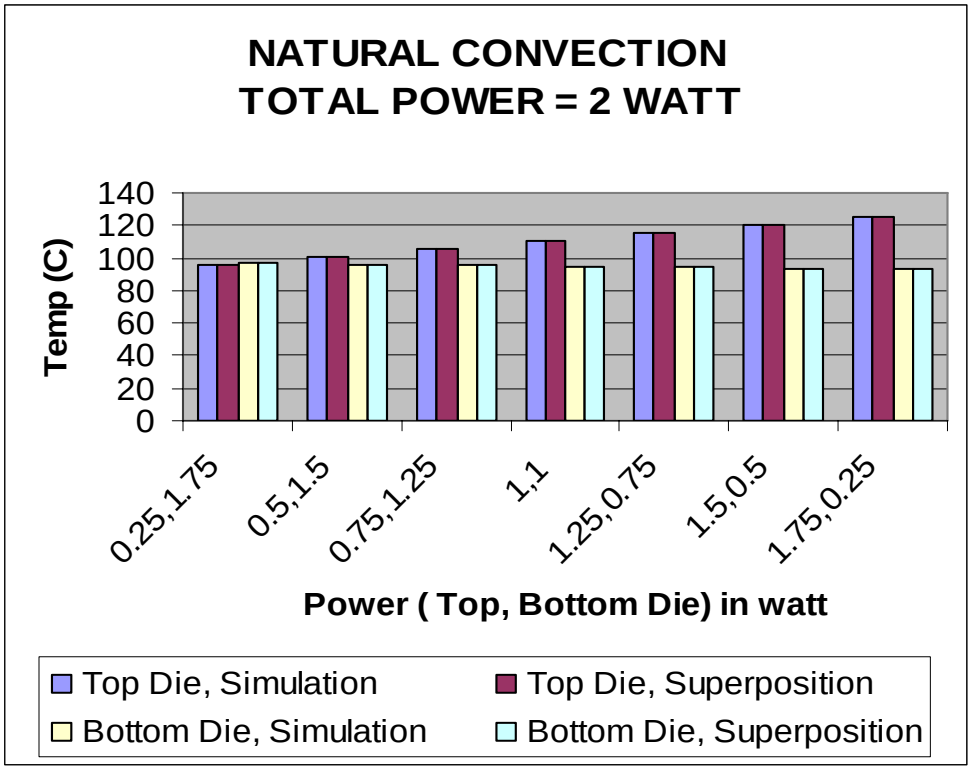


Figure 6.17: Package 3 Natural convection, Power 2 watt

6.5.2 Package 4

Pyramid stacked die configuration (fig. 6.18). Small die (4.4 mm x 7.3 mm x 0.14 mm) is placed on larger die (8.5 mm x 9.5 mm x 0.14 mm) by die attach film.

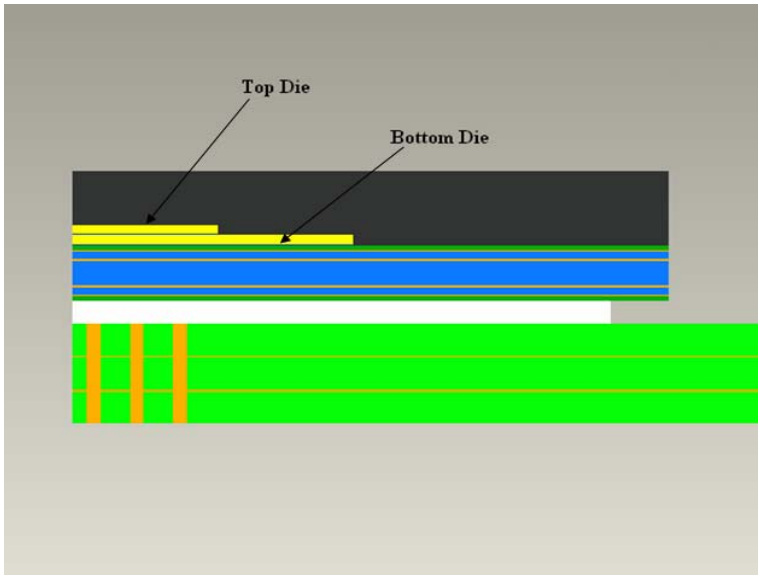


Figure 6.18: Pyramid Stacked Die configuration (Package 4)

Boundary Conditions

Film Coefficient, h = 3 W/m^2 °C

Ambient Temperature = 22 °C

Total Power on Package =1 W

Table 6.12: Initial condition for total power 1 watt (Package 4)

Power on Top Die (W)	Power on Bottom Die (W)	Maximum Temp. on Package(°C)	Top Die Temp. (°C)	Bottom Die Temp. (°C)	Board Temp. (°C)
1	0	56.64	56.64	56.61	48.61
0	1	54.96	54.95	54.96	48.51
1	1	89.59	89.59	89.56	75.12

Table 6.13: Verification of modified linear superposition technique for total power 1 Watt (Package 4)

Power on Top Die (W)	Power on Bottom Die (W)	Maximum Temp. on Package (°C)	Top Die Temp. (°C)		Bottom Die Temp. (°C)		Board Temp. (°C)
			Ansys WB	Linear Sup.	Ansys WB	Linear Sup.	
0.25	0.75	55.37	55.37	55.37	55.37	55.37	48.54
0.5	0.5	55.79	55.79	55.8	55.78	55.78	48.57
0.75	0.25	56.22	56.22	56.22	56.2	56.2	48.59

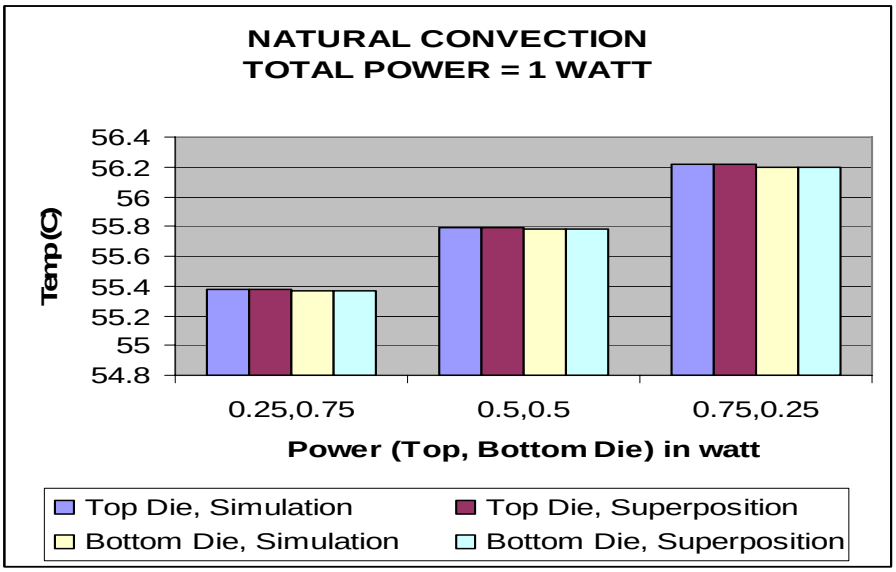


Figure 6.19: Package 4 Natural convection, Power 1 watt

Boundary Conditions

Film Coefficient, h = 3 W/m^2 °C

Ambient Temperature = 22 °C

Total Power on Package =2 W

Table 6.14: Initial condition for total power 2 watt (Package 4)

Power on Top Die (W)	Power on Bottom Die (W)	Maximum Temp. on Package (°C)	Top Die Temp. (°C)	Bottom Die Temp. (°C)	Board Temp. (°C)
0	2	87.92	87.91	87.92	75.05
2	0	91.27	91.27	91.22	75.24

Table 6.15: Verification of modified linear superposition technique for total power 2 Watt (Package 4)

Power on Top Die (W)	Power on Bottom Die(W)	Maximum Temp. on Package(°C)	Top Die Temp. (°C)		Bottom Die Temp.(°C)		Board Temp. (°C)
			Ansys WB	Linear Sup.	Ansys WB	Linear Sup.	
0.25	1.75	88.33	88.32	88.32	88.32	88.33	88.32
0.5	1.5	88.75	88.7	88.74	88.73	88.74	88.7
0.75	1.25	89.17	89.01	89.16	89.14	89.15	89.01
1	1	89.59	89.58	89.58	89.56	89.56	89.58
1.25	0.75	90.01	90	90.01	89.97	89.97	90
1.5	0.5	90.43	90.33	90.43	90.38	90.39	90.33
1.75	0.25	90.85	90.65	90.85	90.8	90.8	90.65

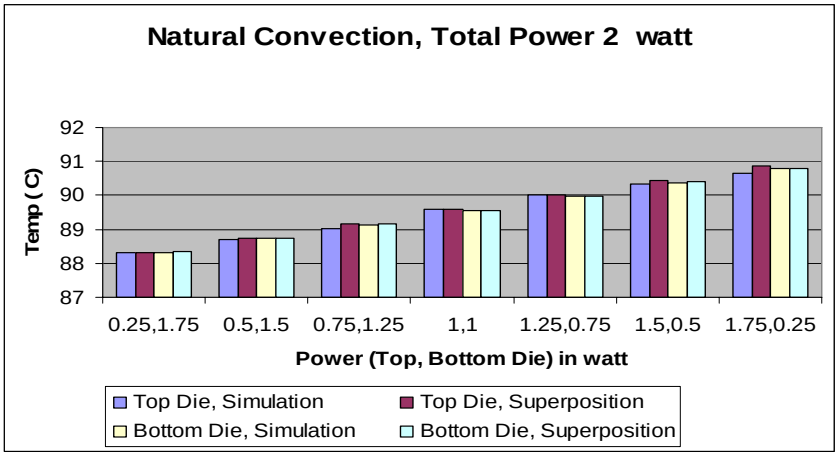


Figure 6.20: Package 4 Natural convection, Power 2 watt

Boundary Conditions

Total Power on Package =1 W and Forced Convection 1 m/sec

Mold compound: Film coefficient, h = 42.5 W/m^2 °C, Ambient temperature = 38.5 °C

PWB top surface: Film coefficient, h = 18 W/m^2 °C, Ambient temperature = 33.5 °C

PWB bottom surface: Film coefficient, h = 18 W/m^2 °C, Ambient temperature = 31 °C

Table 6.16: Initial condition for total power 1 watt and forced convection (Package 4)

Power on Top Die (W)	Power on Bottom Die (W)	Maximum Temp. on Package (°C)	Top Die Temp. (°C)	Bottom Die Temp. (°C)	Board Temp. (°C)
1	0	50.84	50.84	50.81	43.17
0	1	49.16	49.15	49.15	43.05
1	1	66.61	66.61	66.58	53.18

Table 6.17: Verification of modified linear superposition technique for total power 1 Watt and forced convection (Package 4)

Power on Top Die (W)	Power on Bottom Die (W)	Maximum Temp. on Package (°C)	Top Die Temp. (°C)		Bottom Die Temp. (°C)		Board Temp. (°C)
			Ansys WB	Linear Sup.	Ansys WB	Linear Sup.	
0.25	0.75	49.57	49.57	49.57	49.56	49.57	43.09
0.5	0.5	49.99	49.99	49.99	49.98	49.99	43.11
0.75	0.25	50.42	50.42	50.42	50.34	50.4	43.14

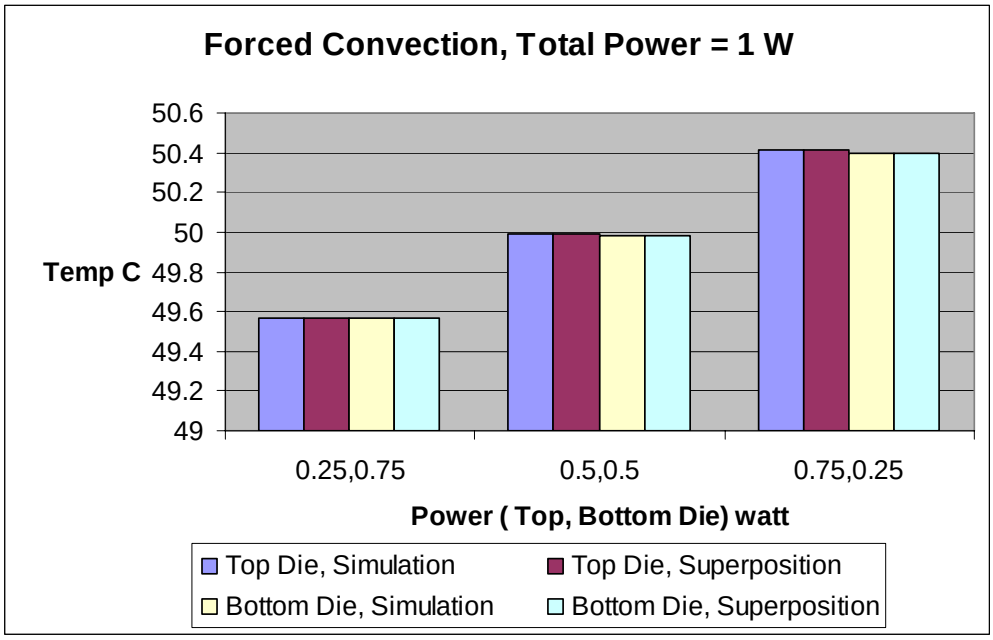


Figure 6.21: Package 4 Forced convection, Power 1 watt

Table 6.18: Initial condition for total power 2 watt and forced convection (Package 4)

Power on Top Die (W)	Power on Bottom Die (W)	Maximum Temp. on Package (°C)	Top Die Temp. (°C)	Bottom Die Temp. (°C)	Board Temp. (°C)
2	0	68.29	68.29	68.24	53.32
0	2	64.93	64.92	64.93	53.09

Table 6.19: Verification of modified linear superposition technique for total power 2 Watt and forced convection (Package 4)

Power on Top Die (W)	Power on Bottom Die (W)	Maximum Temp. on Package (°C)	Top Die Temp. (°C)		Bottom Die Temp. (°C)		Board Temp. (°C)
			Ansys WB	Linear Sup.	Ansys WB	Linear Sup.	
0.25	1.75	65.34	65.34	65.34	65.34	65.34	53.08
0.5	1.5	65.76	65.76	65.76	65.75	65.75	53.15
0.75	1.25	66.183	66.18	66.18	66.16	66.17	53.19
1	1	66.61	66.61	66.6	66.58	66.58	53.18
1.25	0.75	67.03	67.03	67.03	66.99	67	53.19
1.5	0.5	67.45	67.45	67.45	67.41	67.41	53.26
1.75	0.25	67.87	67.87	67.87	67.82	67.83	53.26

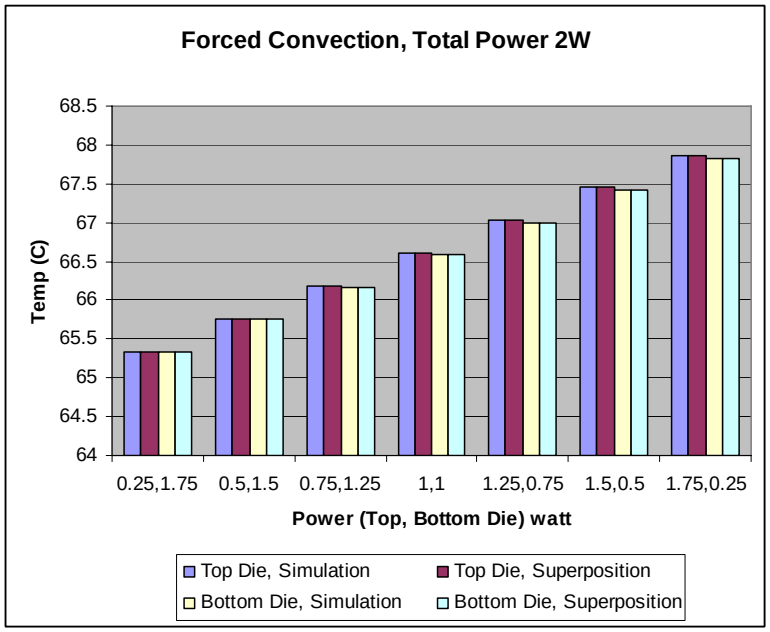


Figure 6.22: Package 4 Forced convection, Power 2 watt

6.5.3 Package 5

3 functional die (one 4.4 mm x 7.3 mm die and two 8.5 mm x 9.5 mm die) and one spacer (4.4 mm x 7.3 mm x 0.14 mm) are stacked together in this package (fig. 6.23).

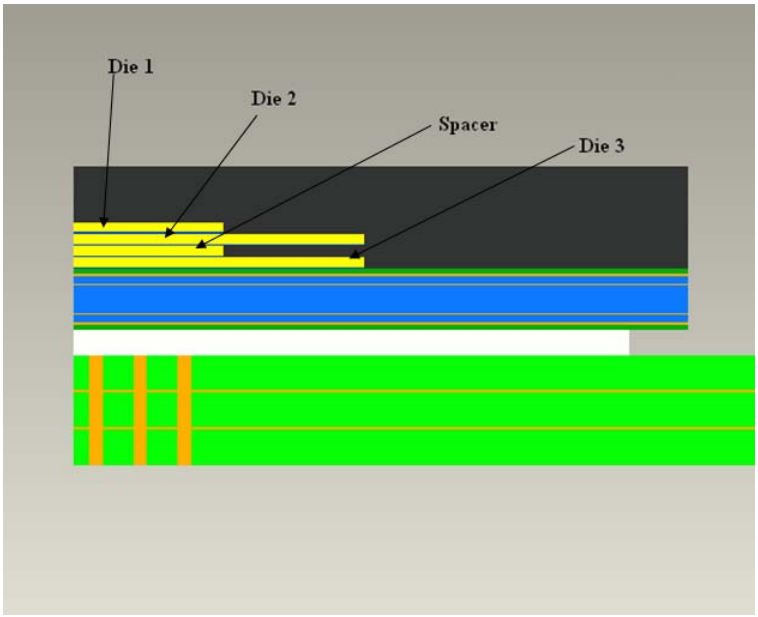


Figure 6.23: 3 Functional + 1 Spacer Stacked Die (Package 5)

Boundary Conditions

Film Coefficient, h = 3 W/m^2 °C and Ambient Temperature = 22 °C

Total Power on Package =1.5 W

Table 6.20: Initial condition for total power 1.5 watt (Package 5)

Power Distribution on Die1, Die2, Die3 (W)	Temp. on Die1 (°C)	Temp. on Die2 (°C)	Temp. on Die3 (°C)
1.5,0,0	76.86	76.84	71.25
0,1.5,0	74.36	74.36	70.75
0,0,1.5	70.61	70.66	71.32

Table 6.21: Verification of modified linear superposition technique for total power 1.5 Watt (Package 5)

Power Distribution on Die1, Die2, Die3 (W)	Temp. on Die1 (°C)		Temp. on Die2 (°C)		Temp. on Die3 (°C)	
	Ansys WB	Linear Sup.	Ansys WB	Linear Sup.	Ansys WB	Linear Sup.
0.25,0.25,1	72.27	72.27	72.27	72.27	71.2	71.22
0.25,1,0.25	74.15	74.15	74.14	74.14	70.92	70.95
1,0.25,0.25	75.4	75.4	75.39	75.39	71.16	71.18
0.5,0.5,0.5	73.94	73.94	73.93	73.93	71.08	71.12

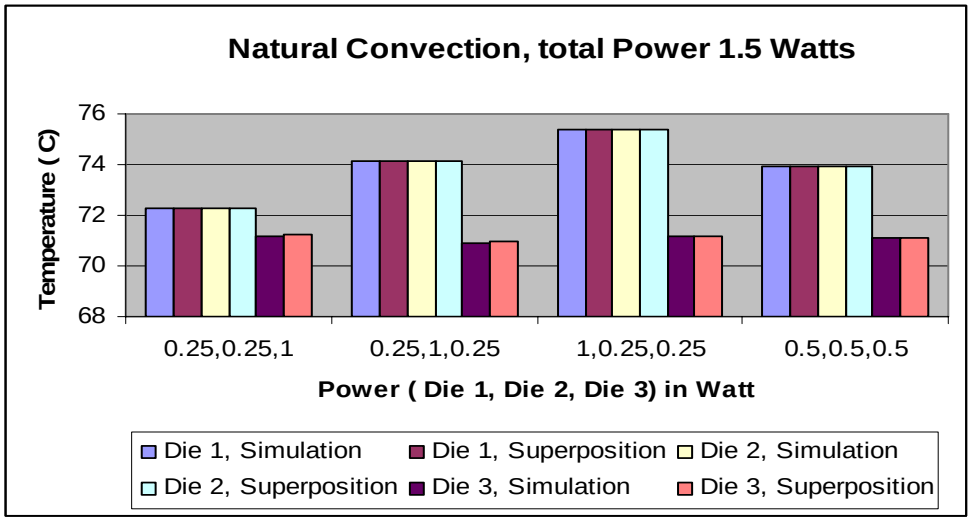


Figure 6.24: Package 5 Natural convection, Power 1.5 watt

Table 6.22: Verification of modified linear superposition technique for total power 1.5 Watt (Package 5)

Power Distribution on Die1, Die2, Die3 (W)	Temp. on Die1 (°C)		Temp. on Die2 (°C)		Temp. on Die3 (°C)	
	Ansys WB	Linear Sup.	Ansys WB	Linear Sup.	Ansys WB	Linear Sup.
0,0.375,1.125	71.54	71.54	71.54	71.54	71.16	71.19
0.375,0,1.125	72.17	72.17	72.16	72.16	71.3	71.3
1.125,0.375,0	76.23	76.23	76.22	76.22	71.1	71.13
0,1.125,0.375	73.42	73.42	73.42	73.42	70.89	70.92
1.125,0,0.375	75.29	75.29	75.28	75.28	71.26	71.26
0.375,1.125,0	74.98	74.98	74.98	74.98	70.87	70.9

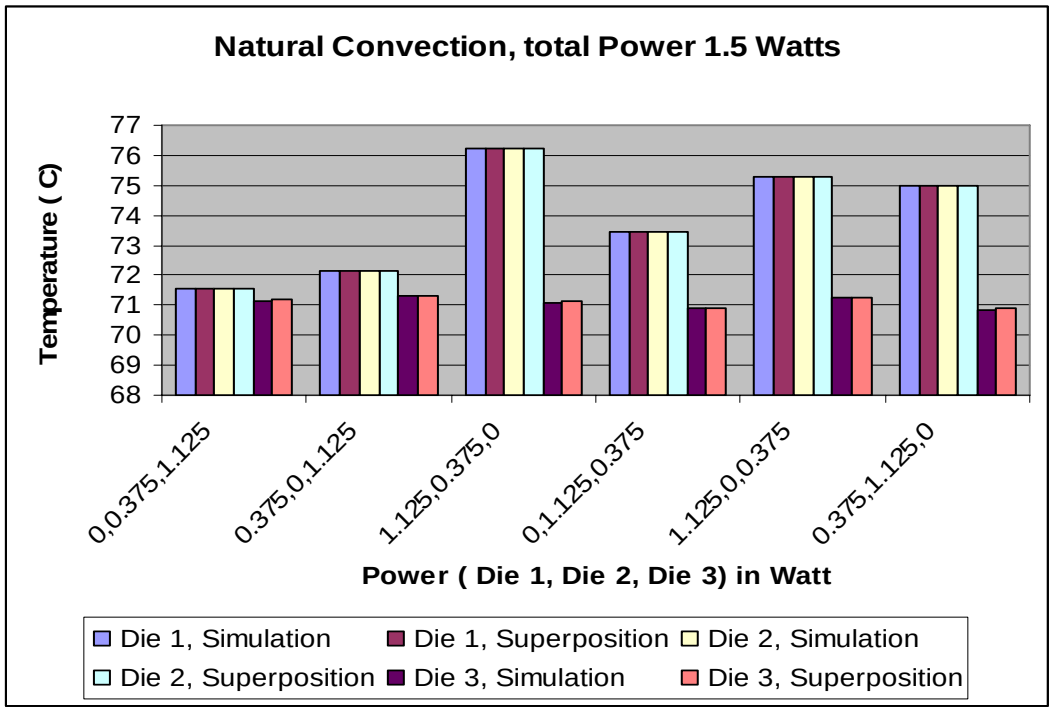


Figure 6.25: Package 5 Natural convection, Power 1.5 watt

Table 6.23: Verification of modified linear superposition technique for total power 1.5 Watt (Package 5)

Power Distribution on Die1, Die2, Die3 (W)	Temp. on Die1 (°C)		Temp. on Die2 (°C)		Temp. on Die3 (°C)	
	Ansys WB	Linear Sup.	Ansys WB	Linear Sup.	Ansys WB	Linear Sup.
0,0.75,0.75	72.48	72.48	72.48	72.48	71.01	71.05
0.75,0,0.75	73.73	73.73	73.72	73.72	71.28	71.28
0.75,0.75,0	75.61	75.61	75.6	75.6	70.06	71.02

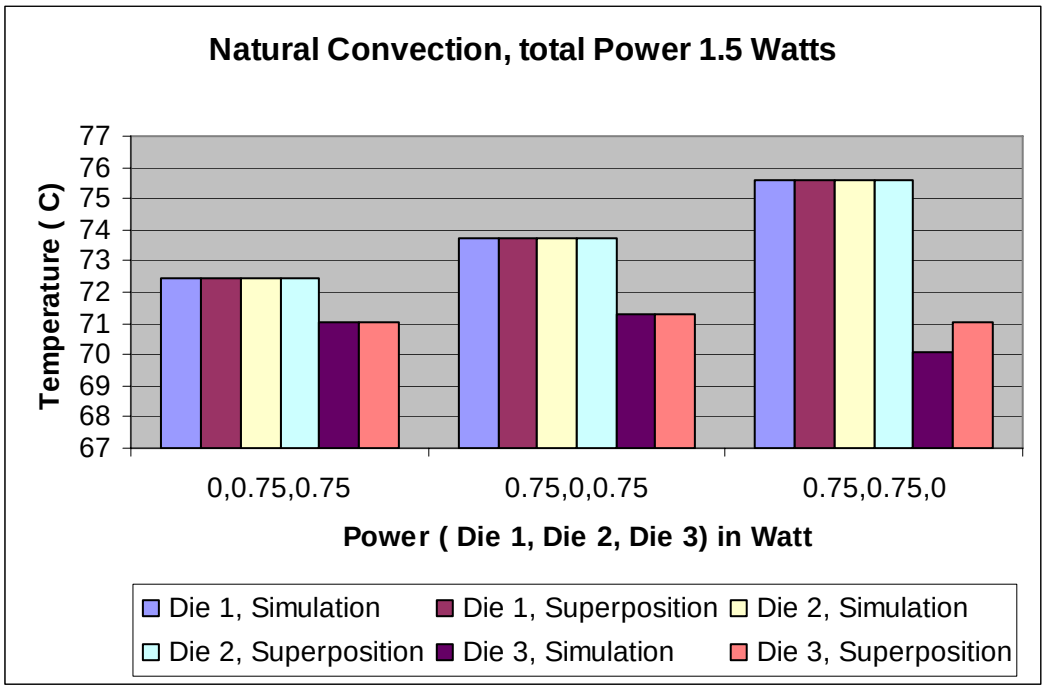


Figure 6.26: Package 5 Natural convection, Power 1.5 watt

Table 6.24: Verification of modified linear superposition technique for total power 1.5 Watt (Package 5)

Power Distribution on Die1, Die2, Die3 (W)	Temp. on Die1 (°C)		Temp. on Die2 (°C)		Temp. on Die3 (°C)	
	Ansys WB	Linear Sup.	Ansys WB	Linear Sup.	Ansys WB	Linear Sup.
0.75,0.45,0.3	74.86	74.86	74.85	74.85	71.09	71.12
0.75,0.3,0.45	74.48	74.48	74.47	74.47	71.15	71.18
0.45,0.3,0.75	73.23	73.23	73.23	73.23	71.17	71.19
0.45,0.75,0.3	74.35	74.36	74.35	74.35	70.99	71.03
0.3,0.75,0.45	73.73	73.73	73.73	73.73	71	71.04
0.3,0.45,0.75	72.98	72.98	72.98	72.98	71.11	71.14

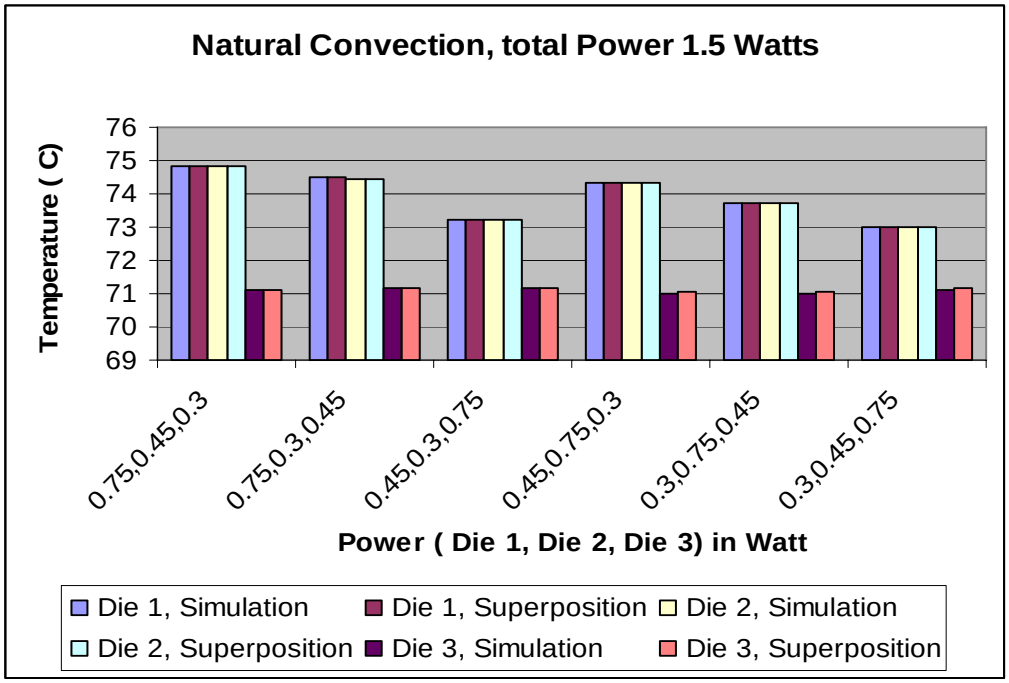


Figure 6.27: Package 5 Natural convection, Power 1.5 watt

6.5.4 Package 6

4 functional die (one 2.2 mm x 3.6 mm, 4.4 mm x 7.3 mm and two 8.5 mm x 9.5 mm die) and one spacer (4.4 mm x 7.3 mm) are stacked together in this package (fig. 6.28).

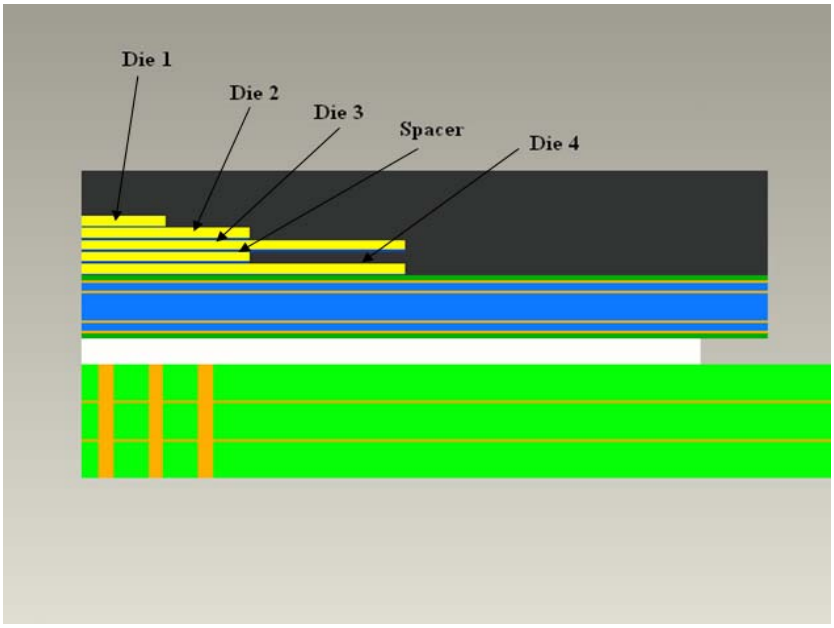


Figure 6.28: 4 Functional + 1 Spacer Stacked Die (Package 6)

Boundary Conditions

Film Coefficient, h = 3 W/m^2 °C and Ambient Temperature = 22 °C

Total Power on Package =2 W

Table 6.25: Initial condition for total power 2 watt (Package 6)

Power Distribution on Die1, Die2, Die3, Die4 (W)	Temp. on Die1 (°C)	Temp. on Die2 (°C)	Temp. on Die3 (°C)	Temp. on Die4 (°C)
2,0,0,0	100.02	99.64	99.60	88.45
0,2,0,0	94.96	94.96	94.9	84.66
0,0,2,0	91.76	91.76	91.76	87.05
0,0,0,2	86.79	86.79	86.79	87.76

Table 6.26: Verification of modified linear superposition technique for total power 2 Watt (Package 6)

Power Distribution on Die1, Die2, Die3, Die4 (W)	Temp. on Die1 (°C)		Temp. on Die2 (°C)		Temp. on Die3 (°C)		Temp. on Die4 (°C)	
	Ansys WB	Linear Sup.	Ansys WB	Linear Sup.	Ansys WB	Linear Sup.	Ansys WB	Linear Sup.
0.33,0.33, 0.34,1	91.16	91.17	91.1	91.1	91.08	91.08	87.27	87.74
1,0.33, 0.33,0.34	95.57	95.57	95.38	95.33	95.33	95.33	87.88	87.97
0.33,1, 0.33,0.34	93.88	93.88	93.8	93.82	93.77	93.77	87.61	87.7
0.33,0.33, 1,0.34	92.8	92.8	92.74	92.74	92.72	92.72	87.34	87.5
0.5,0.5, 0.5,0.5	93.38	93.38	93.28	93.29	93.25	93.25	87.6	87.73

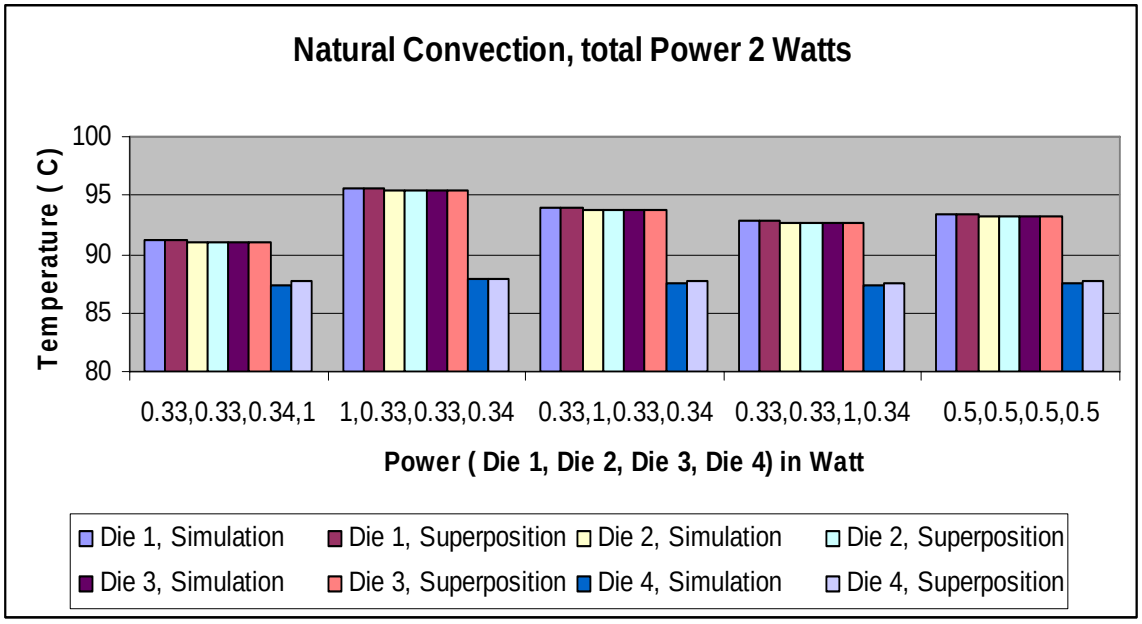


Figure 6.29: Package 6 Natural convection, Power 2 watt

Table 6.27: Verification of modified linear superposition technique for total power 2 Watt (Package 6)

	Power Distribution on Die1, Die2, Die3, Die4 (W)	Temp. on Die1 (°C)		Temp. on Die2 (°C)		Temp. on Die3 (°C)		Temp. on Die4 (°C)	
		Ansys WB	Linear Sup.	Ansys WB	Linear Sup.	Ansys WB	Linear Sup.	Ansys WB	Linear Sup.
1	0,0.5,0.5,1	90.07	90.07	90.07	90.08	90.06	90.06	87.52	87.56
2	0,0.5,1,0.5	91.31	91.31	91.32	91.32	91.3	91.3	87.32	87.38
3	0,1,0.5,0.5	92.12	92.12	92.12	92.12	92.09	92.09	87.49	87.53
4	0.5,0,0.5,1	91.34	91.34	91.24	91.25	91.72	91.23	87.61	87.75
5	0.5,0,1,0.5	92.58	92.58	92.48	92.49	92.47	92.47	87.34	87.58
6	1,0,0.5,0.5	94.65	94.65	94.45	94.46	94.42	94.42	87.81	87.93
7	0.5,0.5,0,1	92.14	92.14	92.04	92.05	92.01	92.01	87.84	87.91
8	0.5,1,0,0.5	94.18	94.18	94.08	94.09	94.04	94.04	87.83	87.88
9	1,0.5,0,0.5	95.45	95.45	95.25	95.26	95.2	95.2	88.04	88.08
10	0.5,0.5,1,0	94.62	94.62	94.52	94.53	94.49	94.49	87.36	87.55
11	0.5,1,0.5,0	95.42	95.42	95.32	95.33	95.28	95.28	87.59	87.71
12	1,0.5,0.5,0	96.69	96.69	96.49	96.5	96.44	96.44	87.95	87.9
13	0,0,0.5,1.5	88.03	88.03	88.03	88.03	88.04	88.04	87.55	87.58
14	0,0,1.5,0.5	90.52	90.51	90.52	90.52	90.52	90.52	87.19	87.23
15	0,0.5,0,1.5	88.83	88.83	88.83	88.83	88.82	88.82	87.73	87.73
16	0,1.5,0,0.5	92.92	92.92	92.92	92.92	92.87	92.87	87.68	87.68
17	0,0.5,1.5,0	92.56	92.56	92.56	92.56	92.55	92.55	87.16	87.2
18	0,1.5,0.5,0	94.16	94.16	94.16	94.16	94.11	94.11	87.47	87.5
19	0.5,0,0,1.5	90.1	90.1	90	90	89.98	89.99	87.85	87.93
20	1.5,0,0,0.5	96.71	96.71	96.43	96.43	96.37	96.37	88.25	88.28
21	0.5,0,1.5,0	93.82	93.82	93.72	93.73	93.71	93.71	87.19	87.4
22	1.5,0,0.5,0	97.95	97.95	97.67	97.67	97.61	97.61	88	88.1
23	0.5,1.5,0,0	96.22	96.22	96.12	96.13	96.06	96.06	87.82	87.85
24	1.5,0.5,0,0	98.75	98.75	98.46	98.47	98.39	98.39	88.24	88.25

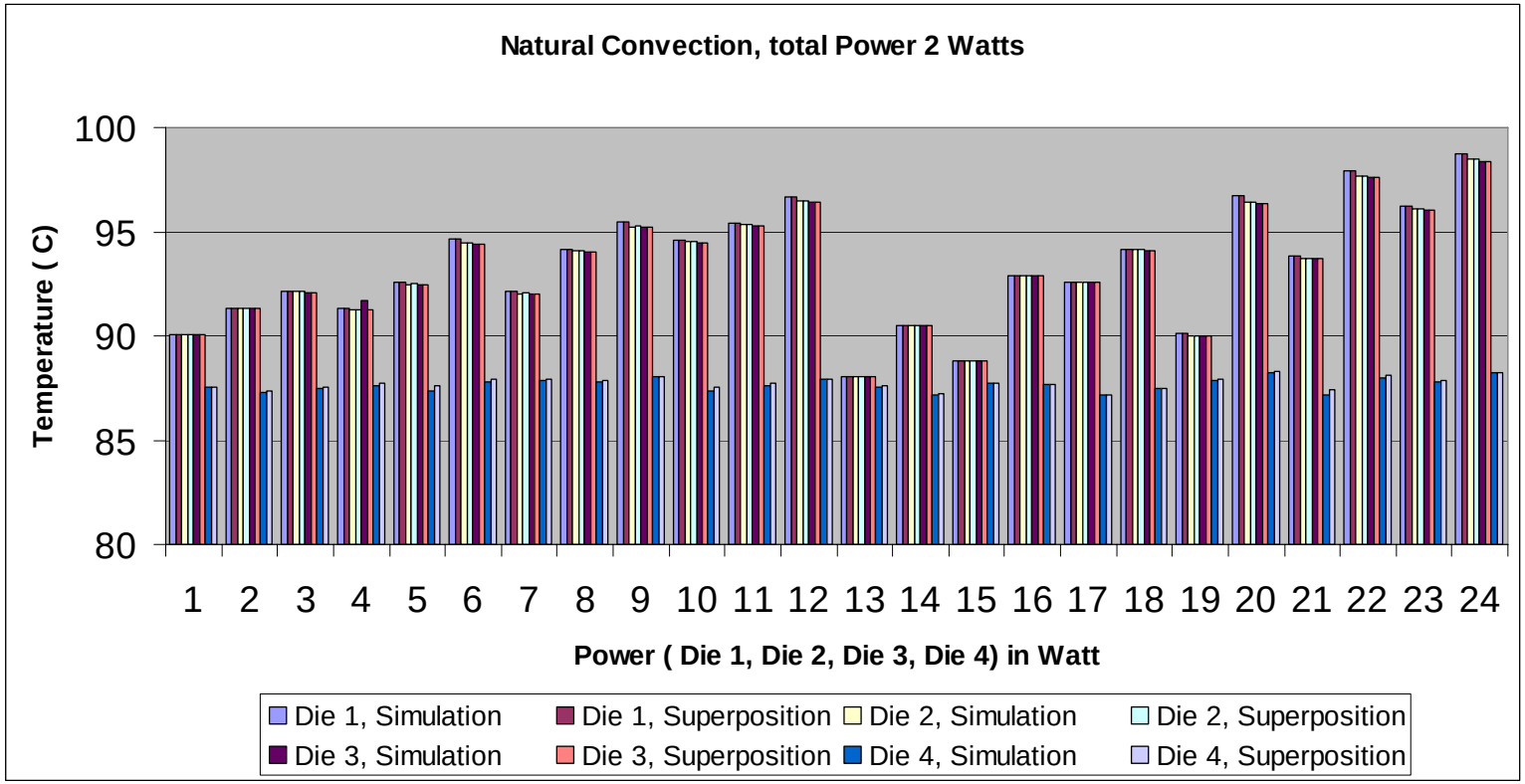


Figure 6.30: Package 6 Natural convection, Power 2 watt

Table 6.28: Verification of modified linear superposition technique for total power 2 Watt (Package 6)

	Power Distribution on Die1, Die2, Die3, Die4 (W)	Temp. on Die1 (°C)		Temp. on Die2 (°C)		Temp. on Die3 (°C)		Temp. on Die4 (°C)	
		Ansys WB	Linear Sup.	Ansys WB	Linear Sup.	Ansys WB	Linear Sup.	Ansys WB	Linear Sup.
1	0.2,0.4,0.6,0.8	91.24	91.24	91.19	91.20	91.18	91.18	87.5	87.59
2	0.2,0.4,0.8,0.6	91.73	91.73	91.69	91.70	91.68	91.68	87.41	87.52
3	0.2,0.6,0.4,0.8	91.56	91.56	91.51	91.52	91.50	91.50	87.57	87.65
4	0.2,0.6,0.8,0.4	92.55	92.55	92.51	92.51	92.49	92.49	87.4	87.51
5	0.2,0.8,0.6,0.4	92.87	92.87	92.83	92.83	92.8	92.80	87.48	87.57
6	0.2,0.8,0.4,0.6	92.37	92.37	92.33	92.34	92.3	92.31	87.56	87.64
7	0.4,0.2,0.6,0.8	91.74	91.74	91.66	91.67	91.65	91.65	87.53	87.67
8	0.4,0.2,0.8,0.6	92.24	92.24	92.16	92.17	92.14	92.14	87.44	87.60
9	0.4,0.6,0.2,0.8	92.38	92.38	92.3	92.31	92.28	92.28	87.7	87.80
10	0.4,0.6,0.8,0.2	93.87	93.87	93.79	93.80	93.77	93.77	87.42	87.58
11	0.4,0.8,0.6,0.2	94.19	94.19	94.11	94.12	94.08	94.08	87.51	87.64
12	0.4,0.8,0.2,0.6	93.2	93.20	93.12	93.13	93.08	93.09	87.7	87.78
13	0.6,0.4,0.2,0.8	92.89	92.89	92.77	92.78	92.74	92.74	87.78	87.87
14	0.6,0.4,0.8,0.2	94.38	94.38	94.26	94.27	94.23	94.23	87.5	87.66
15	0.6,0.2,0.4,0.8	92.57	92.57	92.45	92.46	92.43	92.43	87.69	87.81
16	0.6,0.2,0.8,0.4	93.56	93.56	93.44	93.45	93.42	93.42	87.5	87.67
17	0.6,0.8,0.2,0.4	94.52	94.52	94.4	94.41	94.36	94.36	87.78	87.85
18	0.6,0.8,0.4,0.2	95.02	95.02	94.9	94.91	94.86	94.86	87.68	87.78
19	0.8,0.4,0.6,0.2	95.2	95.24	95.05	95.05	95.01	95.01	87.7	87.80
20	0.8,0.4,0.2,0.6	94.21	94.21	94.06	94.06	94.02	94.02	87.86	87.94
21	0.8,0.6,0.4,0.2	95.53	95.56	95.37	95.37	95.32	95.32	87.76	87.86
22	0.8,0.6,0.2 0.4	95.03	95.03	94.87	94.88	94.83	94.83	87.86	87.93
23	0.8,0.2,0.6,0.4	94.39	94.39	94.23	94.24	94.2	94.20	87.67	87.81
24	0.8,0.2,0.4,0.6	93.89	93.89	93.74	93.74	93.7	93.70	87.77	87.88

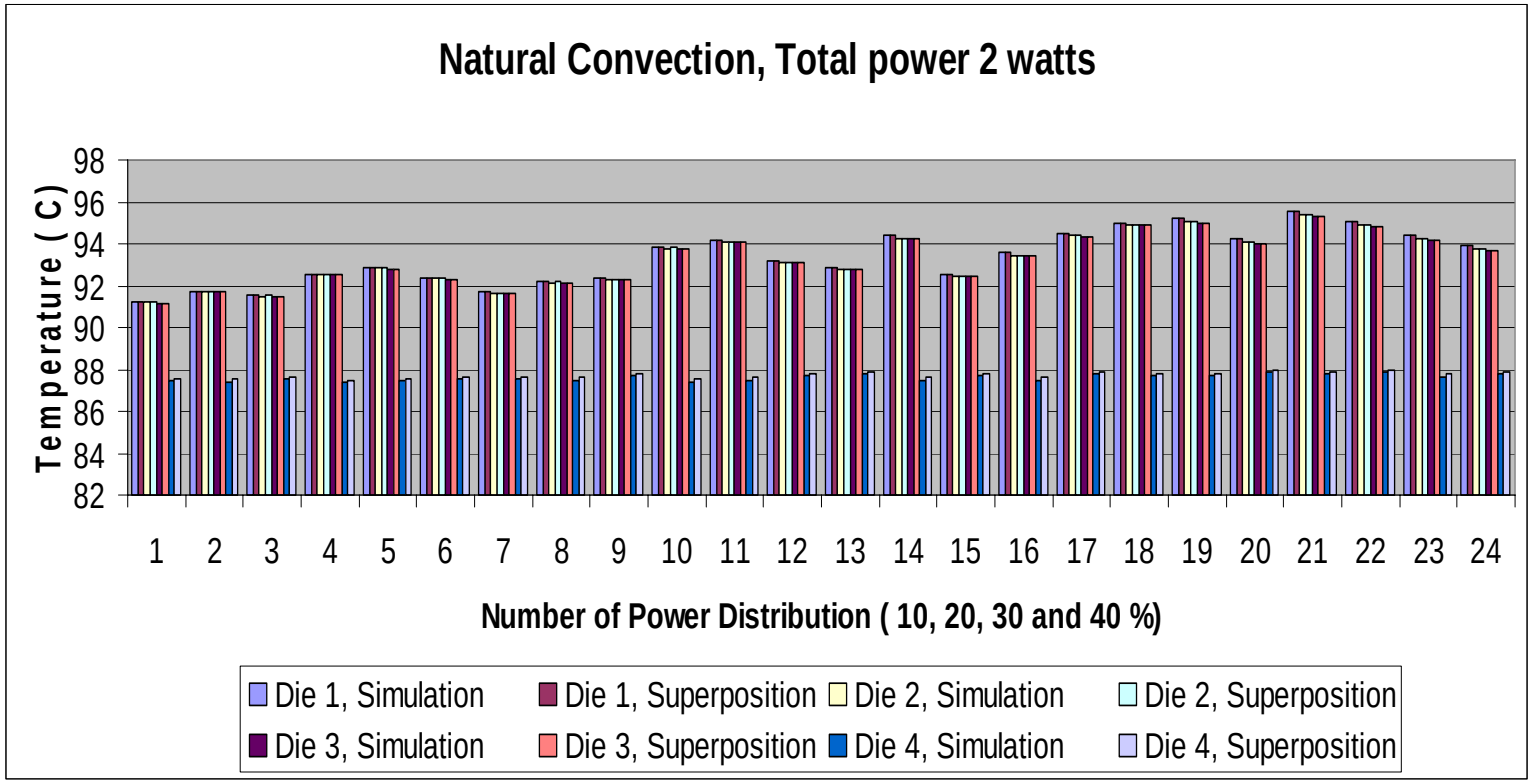


Figure 6.31: Package 6 Natural convection, Power 2 watt

6.6 Overall Observations

- ✓ Number of nodes and elements for cuboidal plate are very small when compared to square or cylindrical block.
- ✓ 3B thermal compact model reduces the number of nodes and elements as well as solution time.
- ✓ For better accuracy of results it is essential to model each die separately while developing the thermal compact model for stacked die.
- ✓ Results obtained from the Ansys workbench simulation are very much accurate to those calculated from modified superposition technique.
- ✓ The maximum error is 1.35 %.
- ✓ Board temp remains almost constant at each power distribution for the case in hand.

6.7 Summary of Thesis

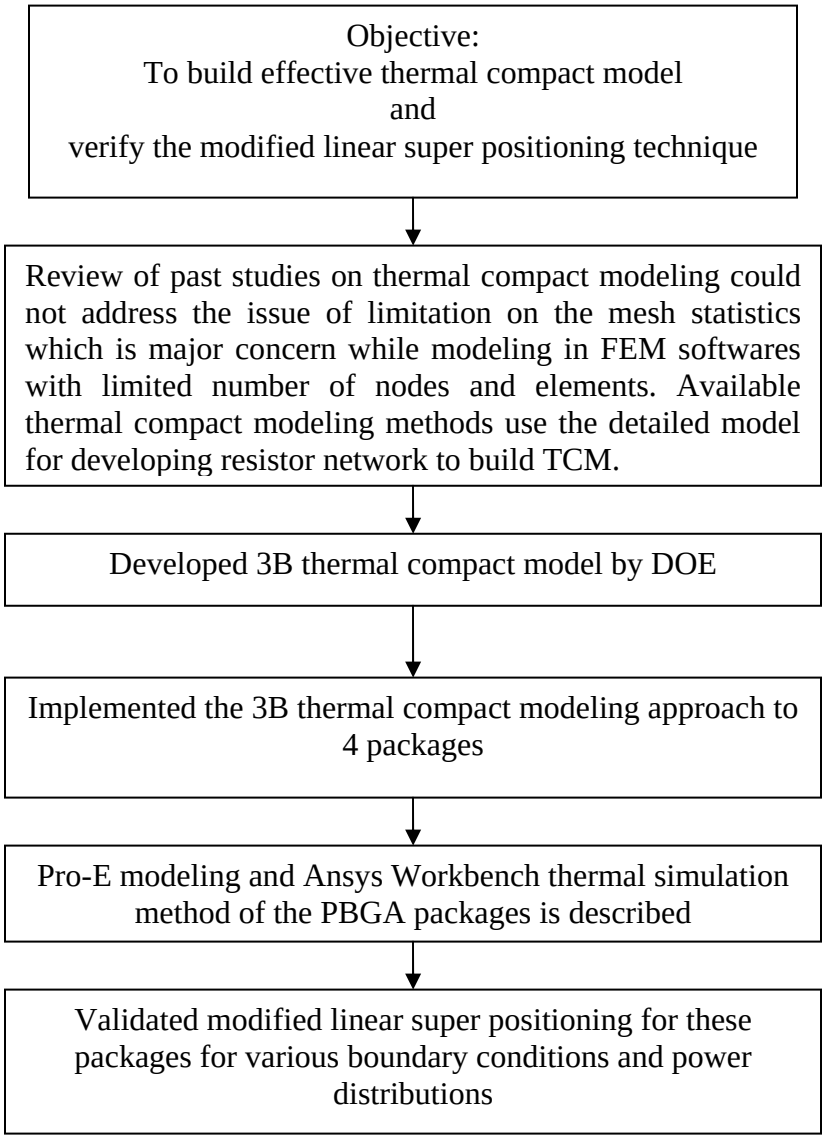


Figure 6.32: Flow chart of summary of thesis

CHAPTER 7

CONCLUSIONS AND FUTURE WORK

7.1 Conclusions

3B Thermal Compact modeling by Design of Experiments has been successfully developed and implemented for mesh reduction in stacked die packages. Almost 50 to 55% reduction in number of elements and node is obtained, maximum 5 % error observed in junction temperature of thermal compact model when compared to detailed model. Significant achievement is marked with the reduction of CPU time by 55 to 80 %.

For steady state analysis most of the electronic packaging material's thermal properties at 77ºC are assumed linear up to temperature of 125ºC. Thus irrespective of the total power if the junction temperature is below 125ºC and the board temperature remains constant for any distribution of the power, ensures the validity of modified linear superposition technique.

Application of the modified linear superposition technique is very good substitute for thermal characterization of multichip packages. Limited sets of data obtained from standard thermal test will give thermal performances of package for all possible power combination while reducing the modeling and simulation efforts.

7.2 Future Work

Future work can be done towards verification of 3B thermal compact modeling method for various elements such as thermal vias and copper traces in substrate. As well as finalize the percentage error in thermal matrices of numerous packages such as Package on package (PoP) and Package in package (PiP).

REFERENCES

[1]. Joiner, B., Montes de Oca, J., Neelakantan, S., 2006, “Measurement and simulation of stacked die thermal resistances,” Semiconductor Thermal Measurement and Management Symposium, Twenty-Second Annual IEEE March 14-16, 2006, pp.210 – 215.

[2]. Zhang, L., Howard, N., and Gumaste, V., 2004, "Thermal characterization of stacked-die packages," 20th Annual IEEE Semiconductor Thermal Measurement and Management Symposium - Proceedings 2004, Mar 9-11 2004, Anonymous Institute of Electrical and Electronics Engineers Inc, San Jose, CA., United States, 20, pp. 55-63.

[3]. Lall, B. S., Guenin, B. M., and Molnar, R. J., 1995, "Methodology for Thermal Evaluation of Multichip Modules," IEEE Transactions on Components, Packaging, and Manufacturing Technology Part A, 18(4) pp. 758-764.

[4]. Bruce M. Guenin, 2002, “Thermal Calculations for Multi-chip Modules,” Calculation Corner, Electronics Cooling Magazine, November 2002, Vol.8, No. 4

[5]. Rencz, M., 2005, "Thermal issues in stacked die packages," 21st Annual IEEE Semiconductor Thermal Measurement and Management Symposium, Mar 15-17 2005, Anonymous Institute of Electrical and Electronics Engineers Inc., Piscataway, NJ 08855-1331, United States, San Jose, CA, United States, pp. 307-312.

[6]. Zahn, B. A., 2004, "Thermal testing of a 3-die stacked chip scale package including evaluation of simplified and complex package geometry finite element models," Proceedings of the 5th International Conference on Thermal and Mechanical Simulation and Experiments in Microelectronics and Microsystems, EuroSimE 2004, May 10-12 2004, Anonymous Institute of Electrical and Electronics Engineers Inc., New York, United States, Brussels, Belgium, pp. 491-498.

[7]. Zahn, B. A., 1998, "Steady state thermal characterization and junction temperature estimation of multi-chip module packages using the response surface method," Proceedings of the 1998 6th Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems, ITHERM, May 27-30 1998, Anonymous IEEE, Piscataway, NJ, USA, Seattle, WA, USA, pp. 76-80.

[8]. Fan, X., 2003, "Development, validation, and application of thermal modeling for a MCM power package," Nineteenth Annual IEEE Semiconductor Thermal Measurement And Management Symposium, Mar 11-13 2003, Anonymous Institute of Electrical and Electronics Engineers Inc, San Jose, CA, United States, pp. 144-150.

[9]. Adams, V. H., Chiriac, V. A., and Lee, T. -. T., 2000, "Thermal Assessment and Enhancement of Molded Array (MAP) PBGA Packages for Handheld Telecommunication Applications," American Society of Mechanical Engineers, Manufacturing Engineering Division, MED, 11pp. 433-442.

[10]. Patankar, Suhas V., “Numerical heat transfer and fluid flow,” Washington: Hemisphere Pub. Corp.; New York: McGraw-Hill, c1980.

[11]. Lee, H., Park, S., and Back, J., 2005, "Thermal characterization of high performance MCP with silicon spacer having low thermal impedance," 21st Annual IEEE Semiconductor Thermal Measurement and Management Symposium, Mar 15-17 2005, Anonymous Institute of Electrical and Electronics Engineers Inc., Piscataway, NJ 08855-1331, United States, San Jose, CA, United States, pp. 322-326.

[12]. James CC Lee., Kei GD Luo Meicer, "Design Characteristics of High Performance and Reduced Cost Chip Scale. Package – μBGA," 10th International Flotherm User Conference. 1.
http://www.flomerics.com/flotherm/technical_papers/t280.pdf

[13]. Karnezos, M., 2004, "3D packaging: where all technologies come together," Electronics Manufacturing Technology Symposium, 2004. IEEE/CPMT/SEMI 29th International, Jul 14-16, 2004, pp.64 – 67.

[14]. James Mark Bird., "System in Package: Identified Technology Needs from the 2004 iNEMI Roadmap,"
http://thor.inemi.org/webdownload/newsroom/apex2005/iNEMI_SiP_RoadmapJMB_paper.pdf

[15]. Karen Carpenter, Jan Vardaman., 2006, "SiP Emerges," Cover Story ,CircuiTree, January 25, 2006, pp 1-5
http://www.sychip.com/PUB/Sip-circuitrees.pdf

[16]. Miettinen, J., Mantysalo, M., and Kaija, K., 2004, "System design issues for 3D system-in-package (SiP)," 2004 Proceedings - 54th Electronic Components and Technology Conference, Jun 1-4 2004, Anonymous Institute of Electrical and Electronics Engineers Inc., Piscataway, NJ 08855-1331, United States, Las Vegas, NV, United States, 1, pp. 610-615.

[17]. Brown, K. M., 2004, "System in Package "the rebirth of SIP"," Proceedings of the IEEE 2004 Custom Integrated Circuits Conference, CICC, Oct 3-6 2004, Anonymous Institute of Electrical and Electronics Engineers Inc., Piscataway, NJ 08855-1331, United States, Orlando, FL, United States, pp. 681-686.

[18]. http://www.statschippac.com/

[19]. Wu, L., Wang, Y. -., and Kee, S. C., 2000, "The advent of 3-D package age," 2000 IEEE/CPMT 26th International Electronics Manufacturing Technology Symposium, Oct 2-3 2000, Anonymous Institute of Electrical and Electronics Engineers Inc., Piscataway, NJ 08855-1331, United States, Snata Clara, CA, United States, pp. 102-107.

[20]. http://www.siliconfareast.com/diestacking.htm

[21]. http://www.ansys.com/

[22]. Chang, T., Cheng, P.H., Huang, H.C., Lee, R.S., Lo, R., 1998, “Parasitic characteristics of BGA packages,” IC/Package Design Integration, IEEE Symposium on 2-3 Feb 1998, pp124 – 129.

[23]. Pro-E user manual

[24]. Ansys user manual 10.0

[25]. Pinjala, D., Iyer, M.K., Chow Seng Guan, Rasiah, I.J., 2000, “Thermal characterization of vias using compact models”, Electronics Packaging Technology Conference, 2000. Proceedings of 3rd , Dec 2000, pp 144 – 147.

[26]. Loh, C.V., Toh, K.C., Pinjala, D., Iyer, M.K., 2000, “Development of effective compact models for depopulated ball grid array packages”, Electronics Packaging Technology Conference, 2000. . Proceedings of 3rd, Dec 2000,pp 131 – 137.

[27]. Garcia, E. A., and Chiu, C., 2003, "Compact modeling approaches to multiple die stacked chip scale packages," Nineteenth Annual IEEE Semiconductor Thermal Measurement And Management Symposium, Mar 11-13 2003, Anonymous Institute of Electrical and Electronics Engineers Inc, San Jose, CA, United States, pp. 160-167.

[28]. Ming Xie., Kok Chuan., Toh, Pinjala. D., 2002, “An adaptable compact thermal model for BGA packages”, Electronics Packaging Technology Conference, 4th, Dec. 2002, pp 304 – 311.

[29]. Garcia, E. A., and Chiu, C., 2005, "Two-resistor compact modeling for multiple die and multi-chip packages," 21st Annual IEEE Semiconductor Thermal Measurement and Management Symposium, Mar 15-17 2005, Anonymous Institute of Electrical and Electronics Engineers Inc., Piscataway, NJ 08855-1331, United States, San Jose, CA, United States, pp. 327-334.

[30]. Huang, W., Stan, M. R., and Skadron, K., 2005, "Parameterized Physical Compact Thermal Modeling," IEEE Transactions on Components and Packaging Technologies, 28(4) pp. 615-622.

[31]. Lasance, C. J. M., 2003, "Recent progress in compact thermal models," Nineteenth Annual IEEE Semiconductor Thermal Measurement And Management Symposium, Mar 11-13 2003, Anonymous Institute of Electrical and Electronics Engineers Inc, San Jose, CA, United States, pp. 290-299.

[32]. Nelemans, W., 2002, “Thermal simulation of telecom racks”. Proceedings of FIOTHERM Design-Class ‘thermal analysis for electronics, June 18th 2002, pp. 14-43.

[33]. Lasance, C. J. M., 2001, "Two Benchmarks to Facilitate the Study of Compact Thermal Modeling Phenomena," IEEE Transactions on Components and Packaging Technologies, 24(4) pp. 559-565.

[34]. Lasance, C. J. M., den Hertog, D., and Stehouwer, P., 1999, "Creation and Evaluation of Compact Models for Thermal Characterization using Dedicated Optimization Software," Annual IEEE Semiconductor Thermal Measurement and Management Symposium, pp. 189-200.

[35]. Bruce M. Guenin, 2001, “Component thermal characterization,” Electronics Cooling Magazine, February 2001, Vol.7, No.1

[36]. JEDEC51-9 specifications are available from JEDEC at http://jedec.org.

[37]. http://www.amkor.com/

BIOGRAPHICAL INFORMATION

Suresh G. Nikalaje, the youngest son of Smt. Shalan and Shri. Ganpati I. Nikalaje is born on 4th August, 1979. He finished his Bachelor's degree in Mechanical Engineering from Rajarambapu Institute of Technology, Shivaji University, Kolhapur in Maharashtra, India in May 2001. He received his Master of Science degree in Mechanical Engineering with specialization in CAD/CAM/CAE from The University of Texas at Arlington, USA in August 2006.