ASSESSMENT OF THE MECHANICAL INTEGRITY OF CU/LOW-K DIELECTRIC IN A FLIP CHIP PACKAGE

by

THIAGARAJAN RAMAN

Presented to the Faculty of the Graduate School of

The University of Texas at Arlington in Partial Fulfillment

of the Requirements

for the Degree of

MASTER OF SCIENCE IN MECHANICAL ENGINEERING

THE UNIVERSITY OF TEXAS AT ARLINGTON

DECEMBER 2012

ACKNOWLEDGEMENTS

I would like to thank my advisor, Prof. Dereje Agonafer, for his guidance and support. I thank him for guiding me in each and every second of my graduate student life. It is impossible to accomplish the milestones without his mentoring and support.

I would also like to thank Prof. Haji-Sheikh and Prof. Seiichi Nomura for serving on my committee.

I also want to thank Fahad Mirza for his support throughout my graduate studies and all other EMNSPC members for their constant support and help at the time of need. I would like to thank Ms Sally Thompson, for patiently assisting me in all matters.

I would like to thank all my friends who have supported me and helped me through these years and made my life at UTA a memorable one. It is their well wishes that supported me throughout my career.

Finally, I would like to dedicate this work to my parents, Saroja and Raman and my sister Priyanka Raman, for without their love and sacrifice I would not have been in a position to complete this work.

November 7, 2012

ABSTRACT

ASSESSMENT OF THE MECHANICAL INTEGRITY OF CU/LOW-K DIELECTRIC IN A FLIP CHIP PACKAGE

Thiagarajan Raman M.S

The University of Texas at Arlington, 2012

Supervising Professor: Dereje Agonafer

Miniaturization and more recently convergence have been driving the industry since the invention of the transistor and integrated circuit (IC). Though the gate delay has decreased with transistor scaling, the increase in the resistive capacitive (RC) interconnect delay due to shrinking interconnect dimensions has become a serious concern for the development of future-generation electronics. To reduce the delay due to resistance R, a major technology change was the replacement of Aluminum (Al) with Copper (Cu) interconnect layers in the BEoL (Back-end-of-line). Recently, some investigators have suggested using low-k dielectric (having dielectric constant less than 4) instead of SiO_2 (k= 3.9) to reduce the capacitive component in the RC delay. Low-k dielectric materials have characteristics such as low mechanical strength, hardness and adhesion, thereby making it imperative to characterize their thermo-mechanical response. Integration of Cu/low-k interconnects has become a critical reliability issue from the foundry's standpoint as well as package reliability. The thermo-mechanical stresses are induced

inside the chip during various fabrication processes, field use, etc. The CTE mismatch between the various components leads to significant warpage and stresses in the metal/dielectric region of the die. Very little work in this area has been done for metal/dielectric stability. In this study, a 3-D multi-level finite element (MLFE) approach has been used to examine the mechanical integrity of the Nano-scale inter-layer-dielectric (ILD) when the package is subjected to thermal shock. Since thickness of each layer in the metal/dielectric region is few orders of magnitude lower than that of the chip/substrate (at least 3 orders) it is almost impossible to analyze it at the global level. Therefore, sub-modeling technique has been leveraged to conduct a relatively accurate estimation of the mechanical behavior of the Cu/low-k region under thermal shock condition. A comparative analysis of the mechanical response of the Cu/low-k region is done for 2 cases – 1) ILD taken as linear material (commonly used industry practice to save computational time) 2) temperature dependent non-linearity of the ILD is implemented and creep and plastic response is captured. The creep model was implemented to represent its realistic mechanical behavior. This study demonstrates the variation in the thermo-mechanical response between the 2 cases thereby addressing the importance of a non-linear analysis for such systems. The developed framework is further utilized to perform a parametric analysis for the number of BEoL layers and to study the effect of underfill properties on the structural integrity of the dielectric layers. Further the model is parameterized to study the effect of the die thickness and the number of interconnect layers in a flip chip package.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

Figure Page

LIST OF TABLES

NOMENCLATURE

IC	Integrated Circuit
DCA	Direct chip attach
FC	Flip chip
UBM	Under bump metallization
RC	Resistive capacitive delay
CMP	Chem-mech polishing
CTE	Coefficient of Thermal expansion (ppm/°C)
ULK	Ultra low-k
Lok	Low dielectric constant material
ILD	Inter layer Dielectric
BEoL	Back End of line interconnects
ν	Poisson's ratio
E	Young's Modulus (GPa)
Tg	Glass transition temperature (°C)
(σ_{xz})	Shear stress (MPa)
σ_y	Normal stress (MPa)

CHAPTER 1

INTRODUCTION

1.1 Introduction to Flip chip package

1.1.1 Flip chip package: An Introduction

The development of technology and the never-ending customer demand for versatile and faster electronic gadgets has resulted in semi-conductor miniaturization. Electronic packages are getting smaller in order to be integrated within the end product/system, which by itself, is getting smaller and lighter every day. Over the last 50 years, electronic technology has been driven by Moore's law – transistors on a chip doubling every 18 months [1]. While gate delay has decreased with transistor scaling, the increase in Resistive Capacitive delay due to shrinking interconnect dimensions has become a serious concern for the development of future-generation electronics. To reduce the delay due to resistance R, a major technology change was the replacement of Aluminum (Al) with Copper (Cu) interconnects. Recently, some investigators have suggested using a low-k dielectric (having dielectric constant k less than 4) instead of SiO_2 (k~4) to reduce the capacitive component in the RC delay [3]. In order to integrate low-k with the state of the art packages and be a part of the main stream electronics industry, extensive research is required to study its mechanical and thermal integrity under standard user conditions.

The term flip chip describes the method of electrically connecting the die to the package substrate. Flip chip microelectronic assembly is the direct electrical connection of face-down (or flipped) integrated circuit (IC) chips onto substrates, circuit boards, or carriers, using conductive bumps on the chip bond pads. In contrast to wire bonding technology, the interconnection

between the die and carrier in flip chip packaging occurs when using a conductive bump placed directly on the die surface. The bumped die is then flipped and placed face sown so that the

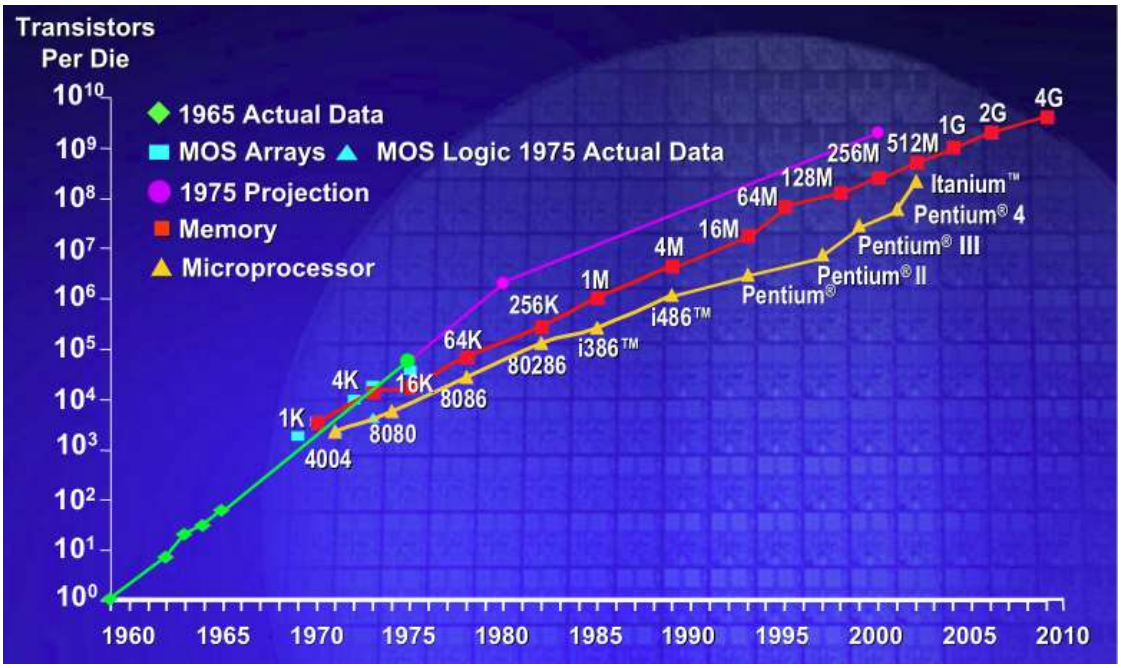

Figure 1.1 Moores Law [1]

bumps connect directly to the carrier. Flip chip components are predominantly semiconductor devices; however components such as passive filters, detector arrays, and MEMs devices are now used in flip chip form. A more descriptive term, direct chip attach (DCA), is used when the chip is directly attached to the printed circuit board or carrier by the conductive bumps. The advantages of flip chip interconnect include reduced signal inductance, power/ground inductance, and package footprint, along with higher signal density and die shrink. [2]

1.1.2 Flip chip technology

Flip chip packaging is a commonly used technology, as a packaging strategy because of the various benefits available. The wire bond package usually limits the number of interconnects with the package and substrate. But in the case of the Flip chip package the entire surface of the die is used for the interconnect purpose so eventually the package size can be scaled down with increased features. The flip chip assemblies consist of three stages.

- Bump the die or wafer
- Attach the bumped die to the substrate
- Fill the remaining space under the die with an electrically non-conductive material

The various factors for deciding the flip chip assembly are the conductive bump, the attachment materials and the process used. Depending on the cost, performance and space constraints of the application, the common bumping and attaching methods varies described in the following section. [4]

Bump Requirements

In a flip chip package the bump performs several functions. In electrical part, the bump serves as the conductive path from chip to substrate. Thermally the bump provides the thermal conductive path to carry heat from the chip to substrate. Mechanically it acts as the pillar to mount the die to the substrate. They also act as the spacer between the chip and substrate to prevent electrical contact between these electrical contacts in turn they act as a short lead to relieve mechanical strain between board and substrate.[4]

Solder Bump Flip chip

In the first step, an under bump metallization (UBM) be placed on the chip bond pads, by sputtering, plating to replace the insulating aluminium oxide layer and to define and limit the solder-wetted area. In the second stage solder is deposited over the UBM by evaporation, electroplating, screen printing solder paste, or needle depositing. In the next stage after bumping the wafer is sawn into bumped die. Then the bumped die is placed on the substrate pads, and the assembly is heated to make a solder connection. [4]

Plated Bump flip Chip

Wet chemical process is used to remove the aluminium oxide and plate conductive metal bumps onto the wafer bond pads. Plated nickel-gold bumps are formed on the semiconductor wafer by electroless nickel plating of the aluminum bond pads on the chips. An immersion gold layer is added for protection and the wafer is sawn into the die. The final

attachment is by solder or adhesive, applied to the bumps or the substrate bond pads by various techniques.

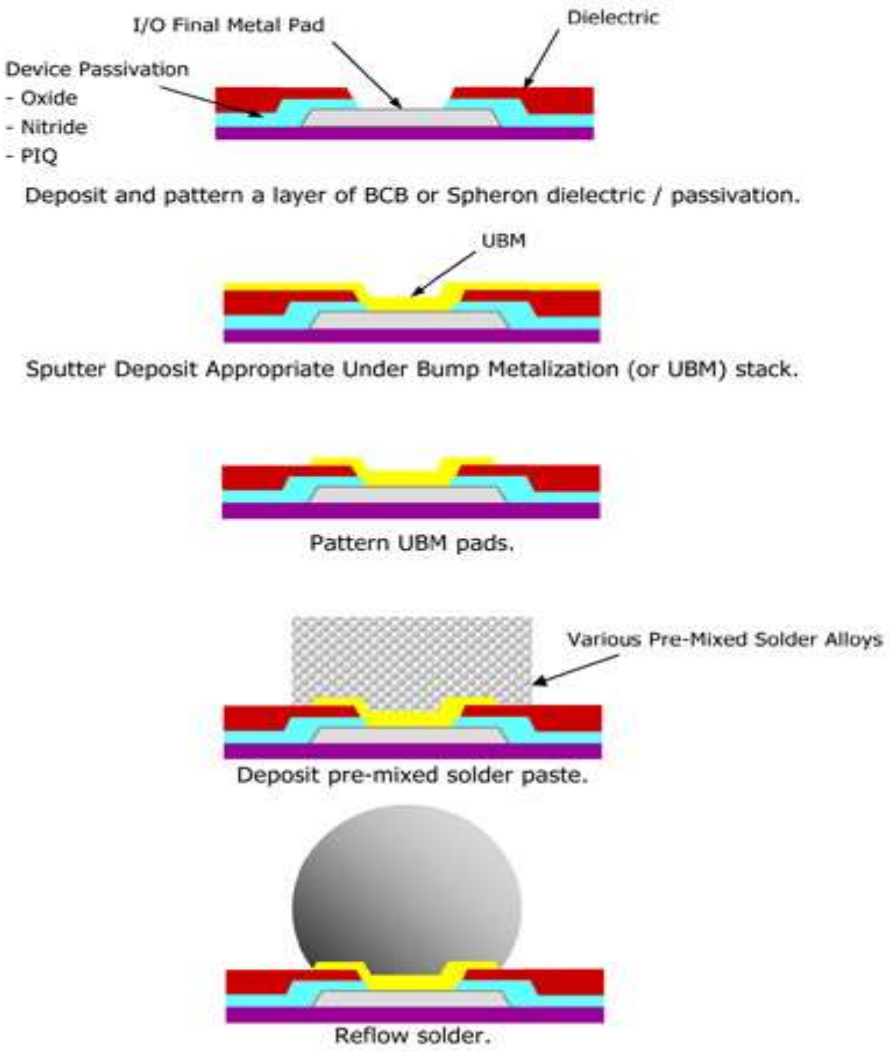

Figure 1.2 Flip chip packaging process [5]

Flip chip packaging process as described in the figure 1.5. In the first step, called the wafer bumping, passivation layer is coated on the top of the wafer and then the under bump metallization layers are electroplated on the patterned passivation layer. The UBM (under bump metallization) layers provide good solder wettability, good adhesion, and adequate electrical

and mechanical connection between the device and solders. In the next stage, the unwanted UBM metal layers are etched away. After this the solder alloy is deposited on the top of the patterend UBM layers. Then the whole layer is heated at reflow temperature to form a spherical shape of the bumps. Then the wafer is sliced into individual dies for packaging. The bumped die is flipped over and aligned with the substrate and then solder reflow process is undergone to form the C4 solder interconnections. Finally an underfilling process is done in the gap between die and substrate to strengthen the solder joints. [3]

1.1.3: Interconnect technology

Migration to new material alternatives has led to the high performance multifunctional microprocessors. For the continuation of this process to produce high performance devices, the features like gate length, dielectric thickness and interconnect line width should be scaled down. The reduction of the scale size of these features will affect the resistive-capacitive delay (RC delay) and the cross talk between the metal lines is the limiting design factors. [3]

In considering the RC delay feature, to reduce the resistance part, copper which has low resistivity has already replaced aluminum. After intensive development, this has been accomplished and the product was sold since 1998 fall. The various critical fabrication process for this accomplishment include electroplating process for the copper network, dual-damascene chem-mech polishing(CMP), and effective liner material for copper diffusion barrier and adhesion promotion. The effective resistivity of Cu wire is 45 % lower than Al lines. [6]

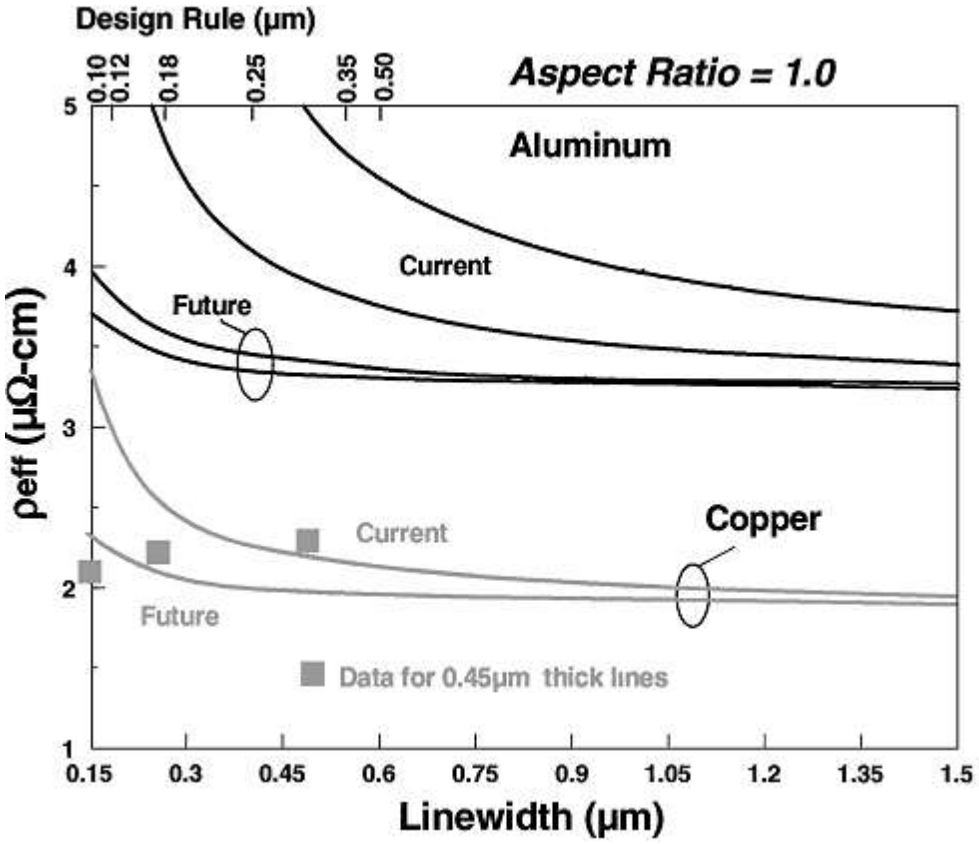

Figure 1.3 Resistivity change with line width for Cu and Al [6]

The capacitance component in the RC delay increases with the scaling of the component size. This in turn will increase the noise level and crosstalk between the metal lines and affect the performance of the device [3]. The two components in the interconnect capacitance are interline capacitance (C_{L-L}) and line to ground capacitance (C_{L-G}) as shown in Figure 1.3.

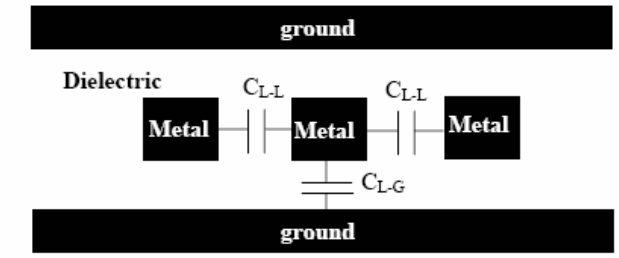

Figure 1.4 Interline capacitance and line to ground capacitance [6]

With reference to the Figure 1.4, when the size of the component reduces, there is a rapid increase in the interline capacitance which in turn affects the total capacitance for interconnect size less than 1 μm. Since the interline capacitance is proportional to the dielectric constant of the inter-metal dielectric, using interconnects with low dielectric constants we can reduce the interline capacitance and the total capacitance.

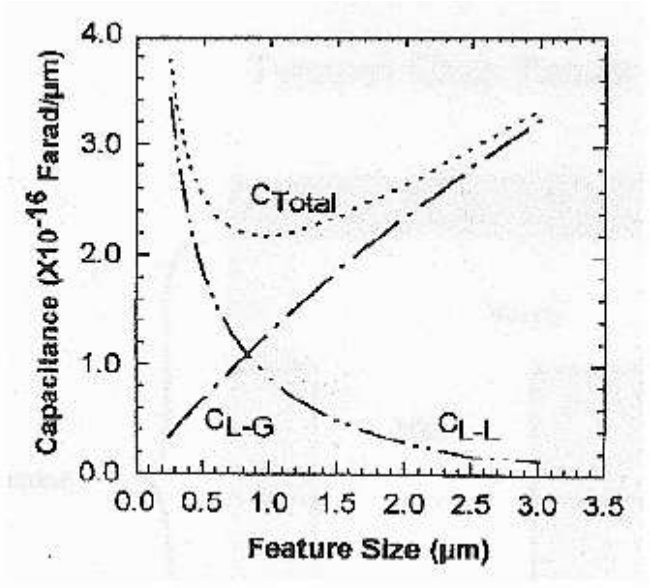

Figure 1.5 Variation of line to ground, inter-line and total capacitance with Feature size [6]

1.2 Reliability Issues

Although with the development of the interconnects and employment of organic substrates to improve the electrical performance, they raise the mechanical reliability concerns in solder joint and the Cu/low-k interconnects. The main factor which causes the reliability issue is the coefficient of thermal expansion (CTE) mismatch between the silicon die and the organic substrate. There are various parts of flip chip package are typically high modulus and cured at temperatures from 100 to 200 ^{o}C. When the package cools down from such a high curing temperature, coefficient of thermal expansion mismatch translates into bending of the die, resulting in the warpage in the package. Due to this warpage the stacked low-k metal layers which is located in the bottom surface of the die is also subjected to the bending stresses.

These stresses in turn induce adhesive or cohesive fracture of the nano low-k films. As the technology advances, in order to further reduce the RC delay ultralow-k (ULK) dielectric material which has dielectric constant k less than 2.5 are being researched to implement it. However with the increase in porosity, mechanical properties get degraded and the Cu/low-k interconnects integration with the package becomes a problem. Due to this reliability issue, the wafer fabrication process with low-k interconnects becomes a major challenge. The two types of failure in the low-k interconnect layers are,

- Cohesive fracture due to brittleness of the low-k materials
- Interfacial delamination due to poor adhesion between the low-k and surrounding materials.

The assembling of the package with the low-k interconnects also affects the reliability of these stacked films. While sawing the wafer into individual dies using mechanical blades cracks are generated at the edges of the die. This crack will propagate into the low-k layers. The other area were the reliability comes into play is at the time of underfilling process. This can be prevented by customizing the mechanical properties of the underfill to achieve low stress in the die. This in turn will reduce the stress in the low-k layers in during thermal cycling to improve the mechanical integrity of the low-k stack.[3]

1.3 Motivation of the work

The processing and materials of the packaging are the areas to be researched to reduce the stress in the low-k layers. To reduce the crack growth and interfacial delamination film adhesion of the metal and low-k layers should be analyzed. Since the crack initiates in the corner of the die, we need to optimize the design of the flip chip to reduce the mechanical stress induced in the stacked low-k layers due to the thermal cycling load. When the number of layers in the Cu/low-k stack is changed it will affect the induced stress, so this factor should be optimized to compensate the electrical performance at the same time to keep the stacked layers mechanically stable. Since underfilling is an important process in packaging process, the

properties of underfill should be chosen such that it keeps the solder bumps mechanically stable at the same time reduce the stress in Cu/low-k layers.

1.4 Objective and scope

In this study, a 3-D multi-level finite element (MLFE) approach has been used to examine the mechanical integrity of the nano-scale inter-layer-dielectric (ILD) when the package is subjected to thermal shock. Since thickness of each layer in the metal/dielectric region is few orders of magnitude lower than that of the chip/substrate (at least 3 orders) it is almost impossible to analyze it at the global level. Therefore, sub-modeling technique has been leveraged to conduct a relatively accurate estimation of the mechanical behavior of the Cu/low-k region under thermal shock condition. A comparative analysis of the mechanical response of the Cu/low-k region is done for 2 cases – 1) ILD taken as linear material (commonly used industry practice to save computational time) 2) temperature dependent non-linearity of the ILD is implemented and creep and plastic response is captured. The creep model was implemented to represent its realistic mechanical behavior. This study demonstrates the variation in the thermo-mechanical response between the 2 cases thereby addressing the importance of a non-linear analysis for such systems. The developed framework is further utilized to perform a parametric analysis for the number of BEoL layers and to study the effect of underfill properties on the structural integrity of the dielectric layers. Further, low-k dielectric is compared with SiO_2.

CHAPTER 2

LITERATURE REVIEW

Zhai et al [7] demonstrated that the Chip package interaction (CPI) related risk will increase dramatically as the low-k inter-layer dielectric migrates toward lower-modulus materials with modeling and experimental results. Usage of hybrid BEoL stack was proved to be solution for the reduction of the chip packaging interaction delamination. The analysis indicates that package level solution with the choice of the underfill material. The usage of the lower modulus of the underfill lowers the corner delamination. But the BEoL is subjected to a interface delamination. It was also figured out that higher CTE of the underfill leads to greater probability of Cu/low-k film delaminaiton. The die size is also not a limiting factor for the low-k stack failure.

Mercado et al [8] studied the effect of having either the low-k or SiO_2 at the last metal layer, with the fracture mechanics based finite element analysis. As the critical interface is the last metal/passivation interface, when a low-k layer is placed it will impact the reliability of the low-k stack. They also studied the impact of increasing the number of metal layers. They evaluated that crack driving force in the upper level increase with the increase in the number of metal layers. The failure does not always occur on the interface and sometime it occurs in close proximity to the interface. The low-k material in the upper layers is more prone to fracture. Replacement of low-k layer with SiO_2 in the last layer will reduce the fracture of the low-k layers and improve package reliability.

Edelstein et al [9] performed significant finite element modeling, to determine the reliability of low-k layers in chip package interaction. The package module stress was determined for wire-bond and flip chip packages. The defect at the chip edges initiates the

delamination in the low-k layers. The molding compound or the underfill creates high tensile forces at low temperatures, highest in the chip corners. They developed a adhesion improvement which will help for wider safety margins, as do low-stress molding compounds.

Wang et al [10] performed a sub model analysis for thermo-mechanical problems that involve path dependent characteristics. The procedure was bench marked using a biomaterial strip composed of the silicon and eutectic solder alloy. When they compared the results of both the global model and sub model which contained more detailed parts predicted a thermal fatigue life closer to that of experimental values. According to St. Venant's principle, boundaries of the sub model should be away from the local stress region. For capturing the path dependent thermo-mechanical problem they introduced the method of using a APDL command to map the temperatures at each and every load step from global to the submodel to accurately predict the thermal fatigue life of the package.

Che et al [11] carried out simulation result comparison for both 2D and 3D models to verify the accuracy of the 2D model. Reliability test and result analysis were conducted for low-k stacks with different structures. They also observed the delamniation failure of the low-k interface for a 13 layer low-k structure from reliability analysis. They also conducted a paramentric study for different solder bump materials, low-k stacks, UBM thickness, barrier layer material properties and shear heights. It was analyzed that although different low-k structures lead to a similar shear force, more low-k stacks can reduce the stress along the critical low-k interface.Thinner UBM can reduce the interfacial stress induced by the solder bump deformation and improve the low-k reliability.

Harman et al [12] discussed the various reliability problems of replacing the wire bonds in the package with the Cu/LoK stacks. It was analyzed the reliability problems like cracking, spalling and crazing of the LoK materials and bond pad indentation. LoK materials with high expansion coefficients and low thermal conductivities increase the stress and extend the

damage to the barrier. They concluded that well designed LoK and underpad structures should have no negative effect on bonding parameters and be invisible to the bonding process.

Jimmy et al [13] performed a 2D strain analysis to investigate the Cu/low-k chips in FCBGA package. They parameterized the model with the replacement of one FSG layer with polymer encapsulated dicing lane technology (PEDL), variation of Cu post height, die thickness, and underfill selection. The results like reduction of stress in low-k stacks and the inelastic energy in the solder bumps was used to formulate the design guidelines for packaging of dies. They also performed the 3D simulation for three cases (A) all rows with spherical solder joints (B) 10 hourglass joints followed by 10 spherical joints (C) 10 Spherical joints followed by 10 hourglass joints. It was finally concluded that case C gave the lowest inelastic strain energy dissipation implying that the solder joints for case C will have long fatigue life and it also gave the lowest stress in the low-k stacked region.

Kuo et al [14] investigated the thermo-mechanical and mechanical properties of polyimide materials used in micro-electronic packaging. The stress-strain curve and young's modulus of polyimide material present a visco-plastic behavior. The power law stress or normalized stress exponent expressions was not useful to formulate the steady state strain rate of creep dependence on temperature and stress level. The power law breakdown phenomenon occurs at a higher normalized stress regime as the temperature increases. They formulated a hyperbolic since power law with the normalized stress and steady-state strain rate expression to counter this problem. In addition it was analyzed that the cyclic creep strain rate observed is higher than that of static creep strain rate, which reveals the cyclic softening and less creep resistance. Polyimide materials, when subjected to cyclic loading exhibit cyclic softening.

Yuan et al [15] developed a robust and rapid design procedure of the novel 3D stacking packaging. They proposed the design procedure for a 3D-WLCSP structure with two chips arranged on top of each other, with a wire bonding for the electrical interconnection between them. After validating the finite element model, screen analysis of fractional factorial ANOVA

with seven factors was used to determine the reliability of the test vehicle. Further three most significant factors was determined with the control of parametric analysis with the control of mesh density at the corner most solder joint.

Che et al [16] performed a calibration study between the global-local modeling method containing submodeling and global local beam modeling technique. It was determined that reasonable submodel with hybrid solid which includes solder joint, PCB and component gives more accurate result than submodel with only solder joint. From the finite element analysis it was concluded that solid-beam-solid GLB model leads to accurate results when compared with shell-beam-shell GLB model. Based on this GLB theory the ball shape solder joint can be replaced with effective solder joint with the cubic block cross section with the same stiffness. This effective block can be used to calculate the plastic deformation in a reasonable method.GLB model is reasonable for small deformation problem and modal analysis because it captures only the elastic behavior of the solid.

Oon et al [17] demonstrated a three dimensional finite element analysis to determine the reliability of the solder joint when subjected to accelerated thermal cycling. They used the ANSYS finite element simulation tool to capture the solder joint fatigue life. Plasctic strain is generated during each of the accelerated thermal cycle in the solder. Since this parameter influences low-cylce fatigue it was used as the evaluation parameter to study the solder joint integrity. Artificial neural network was also used to consolidate the parametric studies and the results were evaluated to study the parameters to give fatigue life.

Kuo et al [18] developed a novel test methodology to determine reliable time temperature dependent mechanical properties of thin film materials. Specimen fabrication procdure, test program, modeling and analysis are included in this test methodology. Further this test can be extended to other polymer or metal thin films or solder material characterization. The investigation proved that mechanical behavior of underfill materials display strong temperature and strain rate dependent. Similarly the cyclic creep strain rate is found to be

higher than that of static creep strain rate which reveals the cyclic softening behavior. In all the cases after preconditioning the fracture surfaces occur between solder mask and FR4 substrates. The interface of solder mask/FR4 is sensitive to temperature and moisture. The failure mode shifts from combined “adhesive and cohesive failure” to cohesive failure when test rate decreases.

Qiang et al [19] performed tensile tests for Pb free 95.5Sn4.0Ag0.5Cu solder with different temperatures and strain rates. It was found that the tensile strength and yield stress of this particular type of material has been directly related to temperature. The young’s modulus is approximately expressed as a linear function of temperature. In order to fit stress-strain curves more perfectly, modification of the material parameters of the Anand model are verified to see if it can predict the visco elastic deformation behavior. Finally it was estimated that Anand model can indeed fit much better than the initial Anand model. They also developed a user defined subroutine code, since the input Anand parameters in ANSYS have no function of both temperature and strain rate for modified Anand model.

Lai et al [20] verified the submodelling technique applied in the reliability assessment of a FCBGA under accelerated thermal cycling. Steady state creep model was implemented for solder bump to better represent its realistic mechanical behavior and sub modeling procedures were developed specifically for path-dependent thermo mechanical problems. They built a detailed global model to verify submodeling solutions and used that model as the benchmark to determine solution discrepancies cause by simplification of global model. It was concluded that if one can afford to conduct a comprehensive 3D analysis of the whole FCBGA, submodeling may not be efficient because path dependent problems require numerical iterations and application of the submodeling requires more iterations which increases the computation time.

Wang et al [21] summarized both experimental and modeling results of the analysis of chip package interaction and the impact of low-k interconnects. The 3D FEA analysis on a multi level submodeling approach was performed in combination with high resolution moiré

interferometry to investigate the chip package interaction for low-k interconnects. After the die is assembled, the thermal deformation at the package level is directly coupled into the interconnect structure, which in turn increases the possibility of interfacial delamination and can affect the chip reliability. Interfaces in the interconnect structures parallel to die surface were found to be most affected area to the packaging effect. When packaging effect was analyzed as a function of line width, energy release rate did not change with decreasing the line width.

Zhang et al [3] investigated the reliability of Cu/low-k chips in both the chip level and package level using high resolution moiré interferometry and finite element analysis. Their simulation results demonstrated that the crack will propagate from global level interconnect towards Si substrate under CPI. By adding dummy copper structures into the low-k interconnect, the energy release rate was decreased. And it was also found that by implementing crack stops, m-ELT results revealed that the fracture resistance of the package was increased. Finally the flip chip package was optimized based on the die thickness, UBM opening diameter, passivation thickness and different types of underfill.

Kao et al [22] demonstrates the use of submodeling technique with thermo mechanical path dependency for examining thermal cycling reliability of flip chip package with tunnel type DLA heat spreaders of different lead widths, which is connected to the chip through different thermal interface materials. From the analysis it was figured out that the adoption of different thermal interface materials did not significantly affect the fatigue reliability of the solder bumps. They also proposed a submodeling technique conducive to the thermo mechanical reliability of solder interconnects, which has a very mechanical strength and numerous in number.

Peng et al [23] demonstrated significantly improved mechanical performance with both reworkable and a non-reworkable underfill. They also demonstrated a rework process which improved the drop test performance due to mechanical abrasion of the solder mask surface during rework and improved underfill adhesion. When the fine pitch BGA’s were tested in thermal shock condition all samples crossed 1000 cycles without failure. By using underfill, it did

not make much alteration in the performance. The voids at the base of the solder joint caused due to the thermal residue are expected to have limited the thermal cycle performance of the underfilled BGA. When nitrogen reflow environment is used it increases the underfill void content compared to reflow in air.

Vishal et al [24] determined the importance of different parameters which will affect the reliability of the solder bump due to electromigration. The effect of Al trace thickness, UBM thickness, UBM diameter and PO diameter on the current density in AL trace and bump is studied. Al trace width and UBM thickness are found to be the most important factors affecting the electro migration. Solder design with Al trace of 60 micrometer, UBM of 7 micrometer thickness, UBM of 120 micrometer diameter and PO of 60 micrometer diameter was found to produce the minimum current density in Al trace. It was also analyzed that bumps with small PO diameter will be subjected to high stress. In order to have minimum current density the solder design should be of large trace width and UBM thickness at the same time smaller UBM and PO diameter.

Barti et al [26] presents the numerical computation of thermally induced stress and strain. Submodeling technique was used to counter the feature size of the passivation layer when compared to the global size. The FEA model results were closely matching with the experimental results inspite of the extremely small structures. The location of maximum stress showed a good relation to the crack position observed experimentally. Simulation of the influence of the passivation topology on the maximum stress can be executed and recommendations for new design rules could be formulated.

Mallick et al [26] conducted tensile and fatigue tests on injection molded polyamide nano composites containing silicate clay particles. The temperature and strain rate dependence was represented by the eyring equation. For polyamide nanocomposite tested at the same cyclic frequency, fatigue failures resulted at low stress level and thermal failures were observed

at high stress levels. It was observed that the fatigue failure was initiated at agglomerated nanoparticles, which was an artifact of the processing method used for the materials.

Park et al [27] addressed the importance of the power cycling analysis for the qualification of PBGA package. They performed a proper and accurate method of modeling so that the fatigue life of the solder joints of identical geometry can be predicted through empirical relationships under different environmental conditions. Their analysis proved that power cycling method of predicting the fatigue life is more severe than accelerated thermal cycling for a certain organic flip chip package. They recommend comparing the difference in ATC and PC for each and every type of PBGA package to accurately predict the solder life.

Morgan et al [28] discussed some of the material characterization techniques and the material properties of the low dielectric constant materials. From their material characterization analysis it was shown that the amount of porosity should be minimized and with pores preferable in closed form. The characterization results showed that for several types of porous and low density silica films, there is not a simple relationship between density and dielectric constant. The porosity, pore structure, surface area, and surface chemistry on the pore walls all affect the dielectric constant and also the mechanical stability of the low-k dielectric layers.

Popps et al [29] tested the reliability results of a flip chip plastic ball grid array cycle under power cycling and thermal cycling conditions. It was analyzed that the power cycling simulated better temperature gradients of actual applications when compared to the thermal cycling. The flip chip PBGA solder joint life was 45 % longer in power cycling. First BGA failure was at 7303 cycles during thermal cycling compared to 8778 cycles during power cycling. And solder joint failure occurred at the die center in thermal cycling and for power cycling it was along the die edge.

Maseeh et al [30] demonstrated the creep behavior of the polyimide thin film below its glass transition temperature by using a circular membrane bulge test. Since the membranes are edge free this in turn is less prone to cracks is the main advantage of this circular membrane

technique to uniaxial techniques. It has been determined that the creep compliance of PI2525 is a very nonlinear function of stress and also requires a threshold strain before creep begins.

Lee et al [31] performed a finite element analysis for estimating the solder joint life of the package under accelerated thermal cycling. Ansys finite element analysis with Anand's constitutive law was used to solve the solder fatigue life for all the twelve die configurations. From the analysis it was recommended to have smaller die size and spacer die architecture had better solder joint reliability. In stacked packages, the performance of the whole package increases with the reduction in the die size. The importance of the nonlinear analysis was discussed in detail to capture the nonlinear behavior of the solder ball to predict the accurate life of the same.

CHAPTER 3

FINITE ELEMENT MODELING

3.1 Introduction to Finite Element Method (FEM)

Among the various numerical methods, Finite element method is the most popular and widely used method. Other than this it is considered as the most sophisticated tool for solving engineering problems. In this method, the whole continuum is divided into a finite number of elements of geometrically simple shape. These elements are made of a number of nodes. The unknown are the displacements of these nodes. To describe the unknown displacements at each point a polynomial interpolation function is used. The entire force applied to the structure is replaced by an equivalent system of forces applied to the nodes. [33] The result of the entire displacement of the structure is obtained by assembling the governing equation

$$\{F\} = [K]\{u\} \text{ ,where}$$

{F} = Nodal Load Vector

[K] = Global Stiffness Matrix

{u} = Nodal Displacements

3.2 Historical Background of FEM

- Finite Element Analysis (FEA) was first developed in 1943 by R.Courant who utilized Ritz method of numerical analysis.

- The name Finite Element was coined by Clough in the year 1960, who also introduced plane problems in FEA.
- The basic ideas of FEM were presented in the papers of Turner, Clough, Martin & Topp and Argyis And Kelsey.
- By the early 1970's, FEA was limited to expensive mainframe computers generally owned by the aeronautics, automotive, defence and nuclear industries and the scope of analysis were considerably limited.
- People such as Zeinkiewicz & Cheung further enhanced finite element technology during 1970's, when they applied the technology to general problems described by Laplace & Poisson's equations.
- 1971 – First release of ANSYS.
- During 1980's micro computers were employed in the development of Finite Element Method.
- By the early of 1990's FEM is being used for analysing larger structural systems.
- Now-a-days the Finite Element Method has its roots in many disciplines.

3.3 Applications of FEM in Engineering

- Aerospace/Mechanical/Civil/Automobile Engineering
- Structural Analysis(Static/Dynamic/Linear/Non-Linear)
- Thermal/Fluid flows
- Nuclear Engineering
- Electromagnetic
- Biomechanics
- Geomechanics
- Biomedical Engineering
- Hydraulics

- Smart structure

3.4 Engineering Analysis Discipline

- Structural analysis (Motion of solid bodies, pressure on solid bodies etc.,)
- Thermal Analysis
- Magnetic Analysis
- Electric Analysis
- Fluid Analysis (Motion of gases/fluids)
- Coupled-Field Analysis (Combination of any of the above)

3.5 Structural Analysis

To compute the deformations, internal forces and stress of a particular object, the structural analysis is used. In order to perform a structural analysis we should first determine the structural loads, geometry, support conditions and material properties. This type of analysis can be used to capture the static response of the structure.[32]

Example: Computation of deformations, internal forces, stresses and strains.

The following are the areas in which structural analysis play a major role,

- Static Analysis – Under static loading conditions, determining the displacements and stresses.
- Modal Analysis – For determining the mode shapes and natural frequencies of a structure.
- Harmonic Analysis – Under time varying loads, determining the harmonic response of the structure.
- Transient Dynamic Analysis – Under random time varying loads, determining the response of the structure.
- Spectrum Analysis – Due to a response spectrum or a random vibration input, calculating the stresses and strain of the structure.

- Buckling Analysis – For calculating the buckling loads and determining the buckling load shape.
- Advance Structural Analysis – This examines the dynamic response, stability and non-linear behaviour of the structure.

Linear Static Analysis

In most of the analysis when assumptions like small deformation, perfectly elastic material and loads are assumed to be static, the analysis can be treated as a specific linear problem.

3.6 Thermal Analysis

In a thermal analysis we will be able to calculate the temperature gradients, heat transfer and thermal flux of an object. Three modes like conduction, convection and radiation analysis can be performed on the desired model [32]. The thermal analysis can be performed in two areas:

- Steady State Thermal Analysis – Under static loading conditions they are used to determine the temperature gradient and other thermal quantities.
- Transient Thermal Analysis – Under time varying loading conditions, they are used to determine the temperature gradient and other thermal quantities.

Table 3.1 Available commercial FEA Software packages [33]

FEA s/w packages	Introduced	Comments
ANSYS	1971	General purpose FEA, Coupled-field, Multidisciplinary FEM program
I-DEAS		Complete CAD/CAM/CAE packages

Table 3.1 – *Continued*

NASTRAN		General purpose FEA on mainframes
ABAQUS	1978	Non-linear & Dynamic analysis
COSMOS		General purpose
PATRAN		Pre/Post processor
Hyper Mesh		Pre/Post processor
Ls-Dyna		Crash/Impact analysis
PROMECHANICA		
NISA	1973	General purpose FEM program
STARDYNE	1967	World's first available commercial FEA s/w packages
ADINA	1975	

3.7 Steps in Finite Element Method

There are several steps in order to complete an analysis by finite element method. These methods are in coincidence with the matrix method. The theoretical approach is given to each and every step below [33],

3.7.1 Discretization

Initially to start with, the problem has to be divided into several elements, connect with nodes. This process is called discretization. Each and every element and their corresponding node should be numbered so that matrix of connectivity can be set up. The figure in the bottom shows the discretization process of a frame into beam elements and discretization of a plane stress problem to quadrilateral elements.

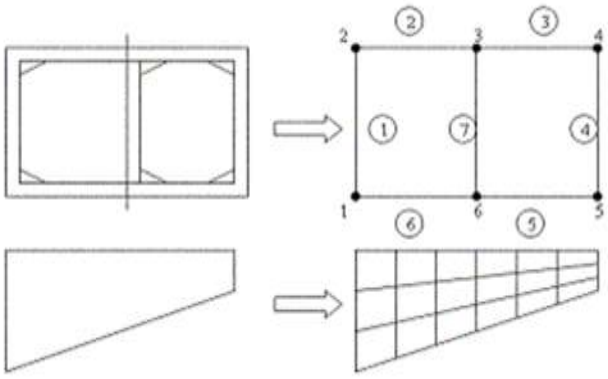

Figure 3.1 Discretization of frame and plane stress problems [32]

The orders in which the nodes and elements are numbered are more important because it greatly affects the computation time. The reason is because we get a symmetrical, banded stiffness matrix, whose bandwidth is dependent on the difference in the node numbers for each element, and this bandwidth is in turn connected to the number of calculations that has to be done in the computer to solve the problem. Usually FEM programs perform an internal numbering option to optimize this bandwidth to a minimum by renumbering these nodes if they are not optimal.

3.7.2 Element Analysis

To perform the element analysis there are two key components, one is expressing the displacements with in the elements and maintaining the equilibrium of the elements. Additionally the stress-strain relationship should be maintaining compatibility. The final result we obtain is the element stiffness relationship S=kv. These results could be obtained from the governing differential equation and boundary condition of the elements. For plane stress problems, the displacement within the elements are expressed as shape functions scaled by the node displacements. The displacement in an arbitrary point within the element is calculated by the nodal point displacement by assuming expression for shape functions. The section of the structure, which is made up of number of elements by which it is represented is kept by the stresses along the edges. Usually in finite element analysis it is easy to work with nodal point

forces. The stress acting in the edge of the structure is replaced by the equivalent nodal point forces by making the element to be in an integrated equilibrium using work or energy considerations. This method of replacement is often called lump the edge forces to nodal forces. Thus the relationship between the nodal point displacements and forces are expressed as $S = kv + S^o$ where,

- S – Generalized nodal point forces
- K – Element stiffness matrix
- V – Nodal point displacements
- S^o – Nodal point forces for external loads

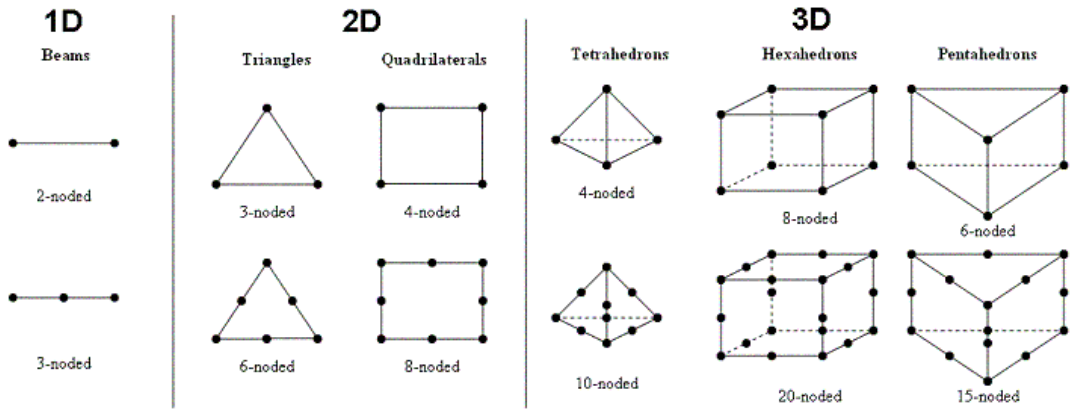

Figure 3.2 Different 1D, 2D and 3D elements [32]

3.7.3 System Analysis

A relationship between the load and nodal point displacements is established by demanding the equilibrium for all nodal points in the structure:

$$R = kr + R^o$$

By adding the contributions from the element stiffness matrices we can establish the global stiffness matrix. Similarly the load vector R is obtained from the known nodal forces.

3.7.4 Boundary Conditions

Boundary conditions are given to the structure by setting nodal displacements to known values of spring stiffness are added.

3.7.5 Finding Global Displacements

By solving the linear set of equations we can calculate the global displacements,

$$r = K^{-1}(R - R^{0})$$

3.7.6 Calculation of stresses

From Hooke's law, the stresses can be determined by the strains. Strains are in turn derived from the displacement functions within the element combined with Hooke's law. This can be expresses as,

$$\sigma (x, y, z) = D\, B(x, y, z)\, v$$

Where

$v = a\, r$

D - Hooke's law on matrix form

B - Derived from u(x, y, z)

Finally the post processors help users to sort the output and display it in the graphical form.

3.8 FEM Notation

Finite element method treats the continuous problem domain as a collection of individual finite elements. The problem parameters are defined at each node of the element. The commonly used definitions of the FEM notation are [33],

• *Dimensionality:* The elements can be defined differently depending on the problem context. Dimensionality indeed expresses whether the element has 1, 2 or 3 space dimensions.

• *Nodal Points:* Every element is described by its nodal points. Frequently the nodal points are chosen to be the corners of the element. However in case of nonlinear geometries nodal points are also defined on the edges.

• *Geometry:* This term is used to describe the domain on which finite element discretization needs to be applied. It can be smooth a regular (e.g. a rectangular plate), or complex (e.g. surface of a machine part). The geometry is defined by the placements of the nodal points.

• *Degrees of Freedom:* The degree of freedom is the number of ways in which the original problem domain can change its state. In the case of the continuous problem domain, the DOF is infinite, because problem characteristics can be defined in each point on the domain. In the discrete FEM domain, instead, the DOF is limited by the number elements, because problem characteristics can only be defined on the nodal points.

• *Nodal Forces:* A set of nodal forces (or any other actions depending on the problem) are defined on each nodal point. From the mathematical point of view this corresponds to the non-homogeneous right hand side of the governing DE.

3.9 Submodeling

The following introduction for sub-modeling technique is taken from ANSYS manual with minor changes [32].

In finite element analysis, the mesh developed in the element is too coarse to produce satisfactory results. Therefore a method called submodeling is introduced to generate finer meshes in the specific region of interest.

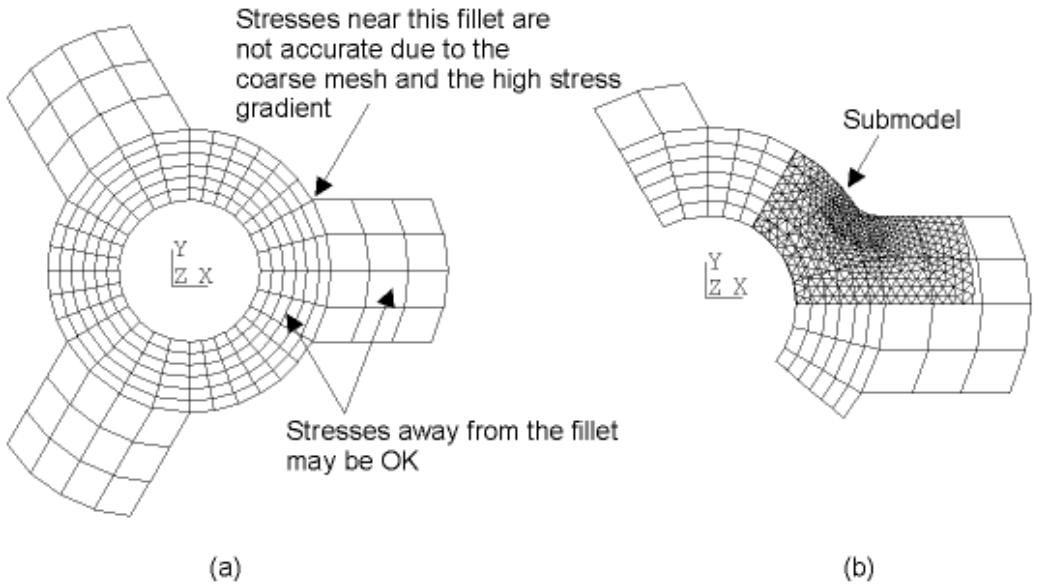

Figure 3.3 submodeling of a pulley hub and spokes : (a) coarsely meshed model, and (b) finely meshed submodel [32]

Submodeling is commonly known as cut boundary displacement method or the specified boundary displacement method. The cut boundary is the boundary of the submodel which represents a cut through the coarse model. Displacements calculated on the cut boundary of the coarse model are specified as boundary conditions for the submodel.

Submodeling is based on St. Venant's principle, which states that if an actual distribution of forces is replaced by a statically equivalent system, the distribution of stress and strain is altered only near the regions of load application. The principle implies that stress concentration effects are localized around the concentration; therefore, if the boundaries of the submodel are far enough away from the stress concentration, reasonably accurate results can be calculated in the submodel.

The ANSYS program does not restrict submodeling to structural (stress) analyses only. Submodeling can be used effectively in other disciplines as well. For example, in a magnetic field analysis, you can use submodeling to calculate more accurate magnetic forces in a region of interest.

Aside from the obvious benefit of giving you more accurate results in a region of your model, the submodeling technique has other advantages:

- It reduces, or even eliminates, the need for complicated transition regions in solid finite element models.
- It enables you to experiment with different designs for the region of interest (different fillet radii, for example).
- It helps you in demonstrating the adequacy of mesh refinements.

Some restrictions for the use of submodeling are:

- It is valid only for solid elements and shell elements.
- The principle behind submodeling assumes that the cut boundaries are far enough away from the stress concentration region. You must verify that this assumption is adequately satisfied.

CHAPTER 4

FINITE ELEMENT MODELING AND METHODOLOGY

4.1 Modeling of Flip chip package

In this chapter, finite element modeling of the package is discussed in detail to study the impact of the CPI on the reliability of the interconnects. Finite element method is used because it is the most widely used method to solve the thermo mechanical deformation and stress distributions in electronic packages. During the chip assembly process, when the die is placed o into the flip chip package, the deformation inside the package increases the thermo mechanical stress in the interconnect structures. The entire analysis in this study has been executed in the commercially available code ANSYS Workbench v13.0. In finite element modeling of a flip chip package there is a very big challenge due to the large dimensional difference between the packaging and interconnects structures. Since the ILD thickness is couple of orders of magnitude less than that of the other components in the package we will not be able to solve the model efficiently (even in a high speed computer). To overcome this problem, multilevel sub modeling technique has been implemented to investigate the chip-package interaction (CPI). Motorola first introduced the concept of sub modeling technique to counter this problem of dimension difference between the structures. In this project a 3D finite element model is developed in 3-level sub modeling technique. A flip chip package with 12 mm x 12 mm die size, 482 um bump pitch, 60 um bump height on a 24 mm x 24 mm substrate was built and was subjected to thermal shock analysis to determine the thermo mechanical behavior. In the finite element analysis, the following assumptions have been made,

- Underfill used in the model is temperature dependent material.

- Aanands viscoplastic constitutive relation was used for the solder bumps.
- All parts in the package were assumed to be perfectly bonded to each other.
- Temperature change during the cycling was assumed to be same throughout the package.
- Except dielectric layers and solder bumps all other materials in the package are assumed to behave elastically.

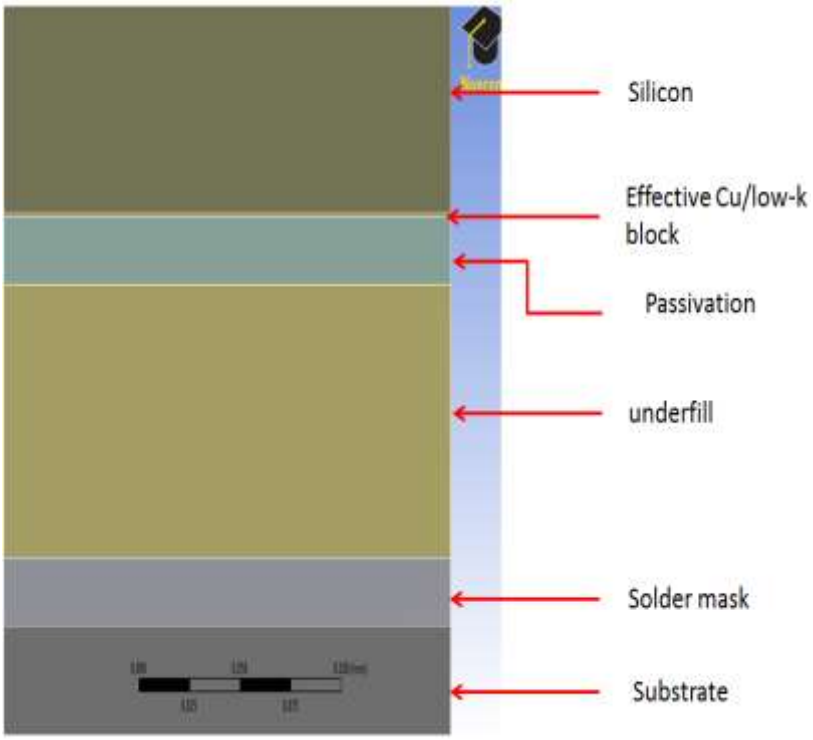

Figure 4.1 Package Components (Global)

4.2 Multilevel submodeling

In the first level model, thermal deformation of the whole package is determined. In this level, using the symmetry conditions in Ansys, a quarter symmetry of the global model is analyzed. Since the ILD thickness was too small when compared to other package dimensions, the interconnect was not modeled in this level. Instead an effective Cu/low-k block with effective properties is incorporated in this global model.

After the global model has been analyzed in detail, the most critical bump is identified and in the second level, the sub model 1 is modeled focusing on the critical solder bump with increased mesh density when compared to the global model. The thickness of the sub model is considered as one pitch distance [20]. The cut boundary technique in Ansys is used to determine the displacements at the cut boundary surfaces.

In the third level, the sub model 2 is modeled with the metal dielectric layers. This is a representative model of the BEoL (Back-End-Of-Line) region. There are 5 metal layers and 5 low dielectric layers. Metal vias in the dielectric layers or via layers have not men modeled for simplification purpose. Similarly as in the previous level, the cut boundary technique in Ansys is used to determine the displacements from the sub model 1 and input that as the boundary condition in this model, i.e. sub-model2.

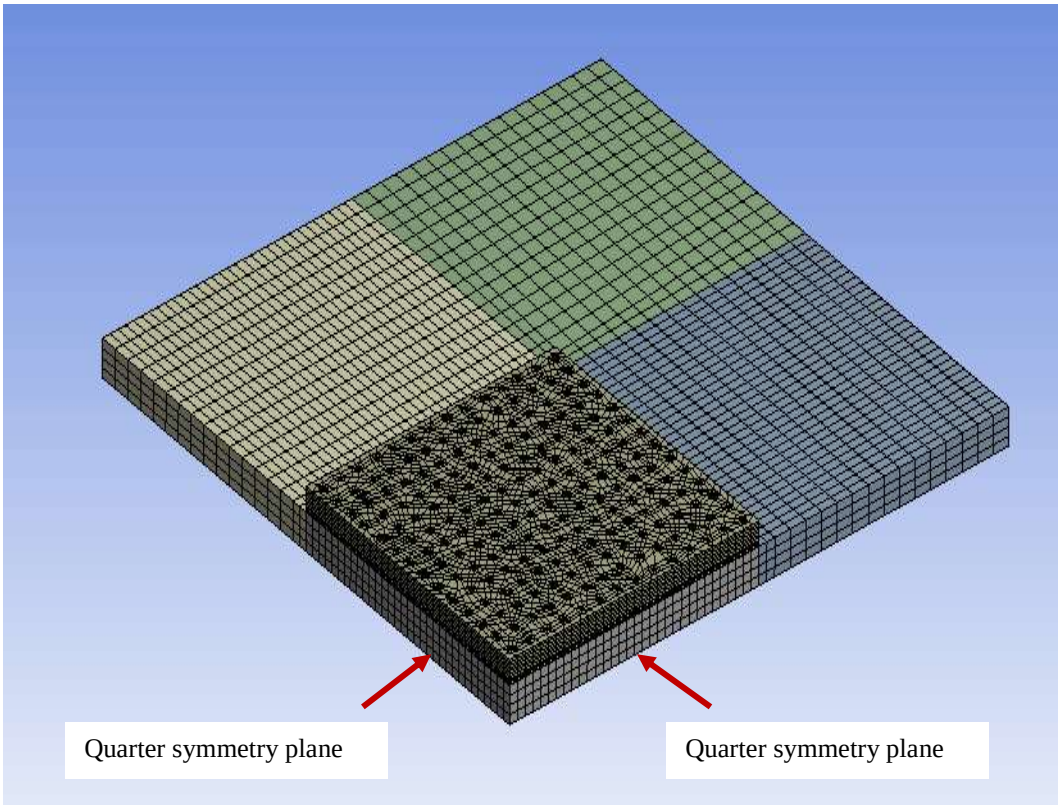

Figure 4.2 Global model (Meshed)

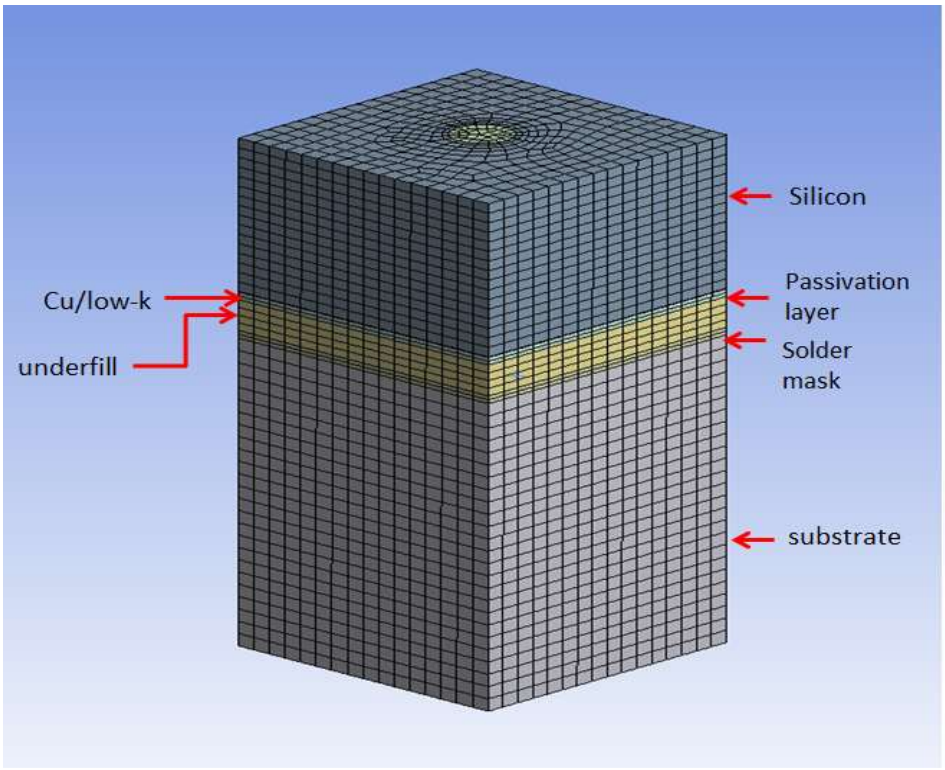

Figure 4.3 Sub model 1 (corner bump joint)

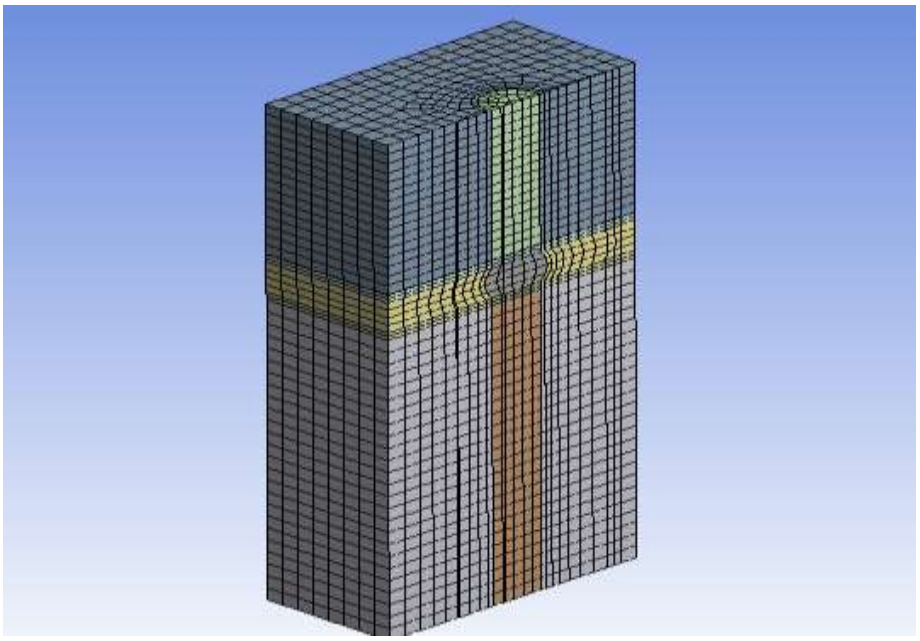

Figure 4.4 Sliced view of Sub model 1 (corner bump joint)

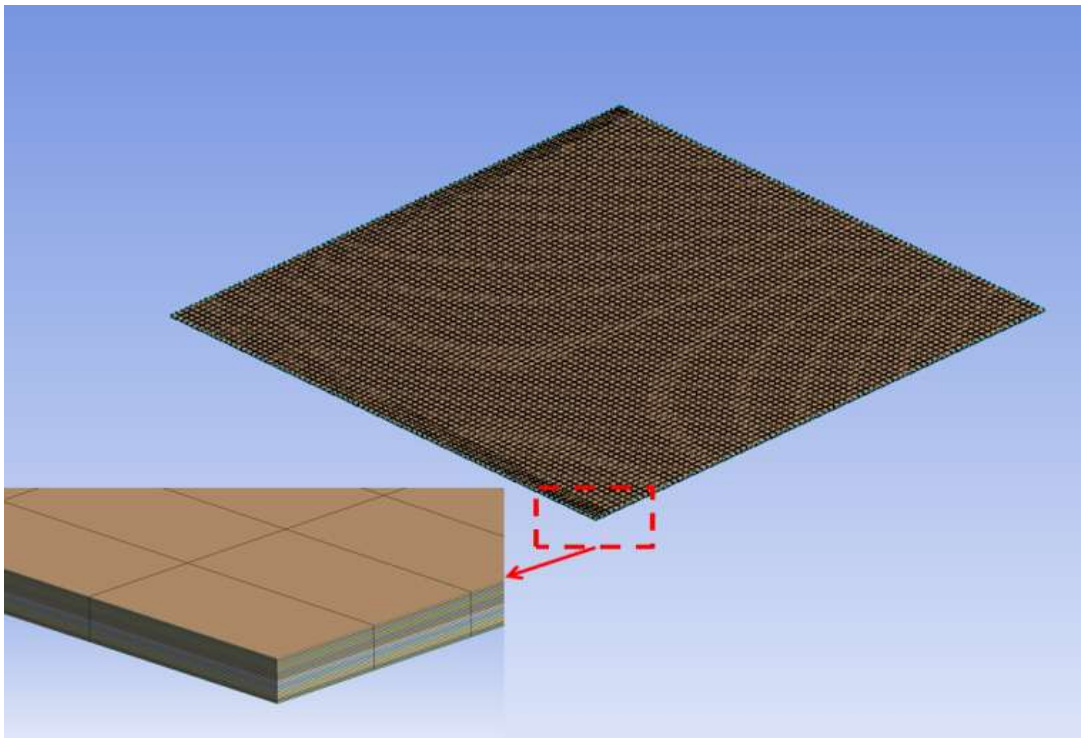

Figure 4.5 Sub model 2 (Cu/low-k region)

4.3 Meshing and Boundary conditions

The model was discretized with fine meshing option (Workbench v13.0) and the mesh continuity was maintained between different components for all the cases. Figure 4.2 shows the global meshed model. Symmetry boundary conditions were applied at the symmetry faces. Each layer in the package is assumed to be perfectly bonded to each other. To formulate quarter symmetry, deformation along the global X and Z directions is constrained at the respective symmetry faces and one common vertex of the substrate was fixed (all Degrees of Freedom zero). According to the JEDEC standard for thermal shock (TS), the model was simulated under TS loading of -55^{o} C to 125^{o} C as shown in Figure 4.6.

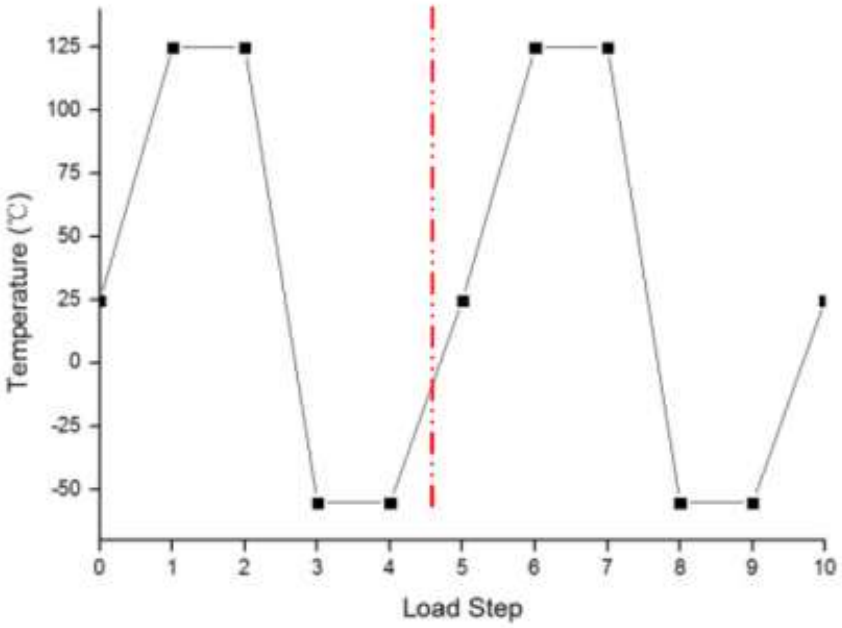

Figure 4.6 Thermal shock loading

The Garofolo creep model in ANSYS, given below is used to capture the creep behavior of the polyimide dielectric.

$$\frac{d\varepsilon_{cr}}{dt} = \mathrm{C}_1[\sinh(C_2\sigma)]^{C_3}\, e^{-C_4/T} \tag{1}$$

Kuo et.al. [14] Proposed the use of the hyperbolic sine equation to determine the creep strain rate in the power-law breakdown region. Creep constants C1, C2, C3, and C4 used in this study are mentioned in Table 1.

Table 4.1 Creep Constants for the Low-Dielectric material (polyimide) [14]

Temperature(^{o}C)	**C1**	**C2**	**C3**	**C4**
-40	1.22E+09	3.69E-14	1.49	2.265E+27
0	9.73E+08	3.94E-14	1.49	2.265E+27
25	8.54E+08	4.11E-14	1.49	2.265E+27
75	6.68E+08	4.5E-14	1.49	2.265E+27
125	5.29E+08	4.97E-14	1.49	2.265E+27
150	4.71E+08	5.24E-14	1.49	2.265E+27

4.4 Package dimensions and properties

The quarter symmetry package dimensions and material properties for each of the components are derived from the literature [34], [35], [36], [37] and are given in the Tables 2 and 3, respectively. Both the time and temperature dependent nonlinear properties are used for the solder to capture the creep and plastic behavior (by using Anand's constants for SAC [19], Table 4). For the dielectric, different cases featuring linear and non-linear properties (time and temp dependent) have been implemented. This would lead to a comparison in the CPI response when the dielectric is treated as a linear material and a non-linear material, respectively. This work is an effort to determine the feasibility of using ILD as a linear material that would lead to immense reduction in computational time and cost, however maintaining reasonable accuracy.

Table 4.2 Full Package Dimensions (mm)

Substrate	24 x 24 x 0.6
Under fill	12 x 12 x 0.06
Passivation layer	12 x 12 x 0.015
Low-k	12 x12 x 100e-6
Silicon	12 x 12 x 0.300
Copper pad diameter	0.085
Copper Pad Thickness	0.015
Solder ball diameter	0.100
Solder ball height	0.060
Solder ball pitch	0.482

Table 4.3 Material Properties

Material	**E (GPa)**	**Poisson's Ratio (υ)**	**CTE (ppm/°C)**
Substrate	25.9 (x or z);11(y)	0.39	17e-6(x or z);52e-6(y)
Passivation layer	57	0.17	1.30E-07
Die	150	0.3	3.00E-06
Cu Pad	82.7	0.34	1.27E-05
Solder Mask	2.4	0.4	6E-5
Underfill	4.76	0.3	3.5E-5
low-k (Polyimide)	5.32	0.34	2.42E-06

Table 4.4 Anand's constants for lead free solder [19]

Variable	**Sn4Ag0.5Cu**
S_o (MPa)	20
Q/R (1/K)	10561
A (1/s)	325
A	10
M	0.32
h_o (MPa)	8.0E5
S^(MPa)	42.1
N	0.02
A	2.57

4.5 Design of Experiments

In the first DOE the number of layers in the Cu/low-k stack is varied from 10 to 14 (Table 4.5). The effect of number of Cu/low-k layers on the mechanical behavior of the Cu/low-k region is analyzed. In the second DOE the effect of thermo mechanical properties of the underfill on the bump stress-strain and the Cu/low-k mechanical response is investigated. (Table 4.6 and 4.7) Different combination of the parameters CTE and E were incorporated so that not only the effect of their combinations but also the effect of individual parameters can be examined. In the DOE 3, the effect of number of layers on the interconnects is analyzed (Table 4.8). In DOE 4, the effect of die thickness is investigated (Table 4.9).

Table 4.5 DOE 1 (Feasibility of Linear and Non-Linear analysis)

CASES	Number of layers	Di-electric Properties
L1	10 layers	linear properties
NL1	10 layers	non-linear properties
L2	14 layers	linear properties
NL2	14 layers	non-linear properties

Table 4.6 DOE 2 (Effect of Underfill properties)

Constant CTE and Tg

Underfill	E (GPa) (@ 22 °C)	CTE (ppm)	Tg (^{o} C)	Poisson's Ratio
1	6.3	30	125	0.3
2	10.0	30	125	0.3
3	15.0	30	125	0.3

Table 4.7 Constant E and Tg: CTE variation

Underfill	E (GPa) (@ 22 °C)	CTE (ppm)	Tg (^{o} C)	Poisson's Ratio
1	6.3	20	125	0.3
2	6.3	30	125	0.3
3	6.3	40	125	0.3

Table 4.8 DOE 3 (No. of Cu/low-k layers)

CASES	Number of layers	Di-electric Properties
1	10 layers	non-linear properties
2	14 layers	non-linear properties
3	18 layers	non-linear properties

Table 4.9 DOE 4 (Die Thickness)

CASES	Number of layers	Die Thickness(microns)
1	10 layers	100
2	10 layers	300
3	10 layers	500

In order to optimize the design of the 24 x 24 mm die low-k flip chip package, a numerical study of the effect of various parameters such as number of Cu/low-k layers, the thickness of the die and the thickness of the substrate and their effect on reliability of the package was carried out. The parameterization is done to improve the reliability performance by reducing the corner stress in the Cu/low-k layers.

CHAPTER 5

RESULTS AND DISCUSSION

5.1 Background and Methodology

Thermo-mechanical analysis under thermal shock condition has been completed for the package with polyimide (low-k) dielectric using commercial code ANSYS. The dielectric layers have been parameterized and simulated to analyze the stress strain distribution in the structure. Comparative study between the linear and non-linear dielectric properties has been done for 10 and 14 layers. DOE 2 addresses the effect of underfill material properties on the CPI, specifically the joint stress and the response of the Cu/low-k region. The idea is to understand if there was any significant effect of the underfill properties on the mechanical response of the Cu/low-k region. The global model was first analyzed to study the maximum stress region so that an accurate submodel can be formulated. The critical bump is determined and the sub-model 1 is formulated accordingly (it was the diagonal corner most joint). In the sub-model 1 the bump pitch (482um) was taken as the length and width of the sub model. In both the global and sub-model 1 the Cu/low-k region was simplified as a block with effective properties (linear only). In sub-model 2, the layers were discretized into metal/dielectric and the analysis was completed as per the DOE. All the data reported for the bump/underfill is from submodel-1, and for the Cu/low-k region it is from submodel-2, unless otherwise stated. As shown in Figure 5.1, the maximum stress in the sub-model 1 was at the interface of the copper pad and the Cu/low-k region. In the sub model-2 the Cu/low-k region has been modeled in detail with the Cu and dielectric layer alternatively arranged. Only in sub-model 2 the dielectric layers have been analyzed with linear and non-linear material properties and to analyze their feasibility.

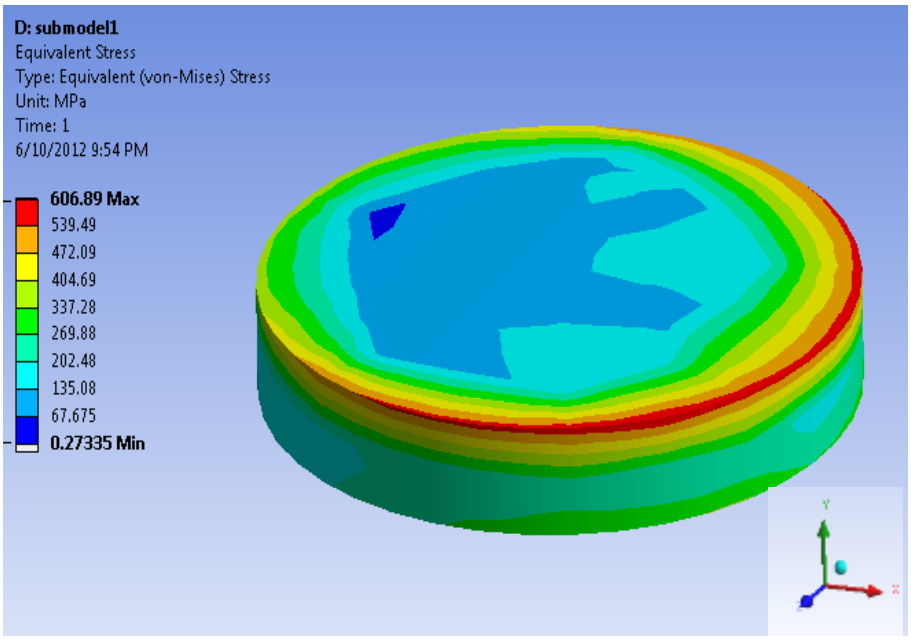

Figure 5.1 Maximum Equivalent stress in Cu Pad in the diagonal corner bump (submodel-1)

5.2 Feasibility of Non-Linear Analysis

Table 5.1 shows the mechanical response comparison between the linear and non-linear model for 10 and 14 layers. As expected, it is clearly evident that the von-mises stress reduced and strain increased from linear to the non-linear case.

Table 5.1 Stress and strain distribution in Cu/low-k region in submodel-2 (Dielectric layers)

		Equivalent von-mises stress (MPa)	**Equivalent Strain (μ-strains)**	**Shear stress (σ_{xz}) (MPa)**	**Normal stress (σ_y) (MPa)**
CASE I (10 layers)	Linear	472.2	61330	22.5	284
	Non-Linear	155.8	76278	8.9	97.9
CASE II (14 layers)	Linear	498.8	64784	26.3	274.6
	Non-Linear	153.7	84604	8.8	94.1

The equivalent von Mises stress showed a 67 % reduction in the stress value from linear to non-linear analysis. This reduction is due to the fact that stress relaxation during creep significantly affects the thermo-mechanical response. Even the location of the maximam changed from top-most (chip side) low-k layer to bottom most (substrate side) low-k layer between linear and non-linear analysis. The effect of number of Cu/low-k layers on von-mises stress is not very significant but strain increased by 10%. (higher strain for 14 layers).

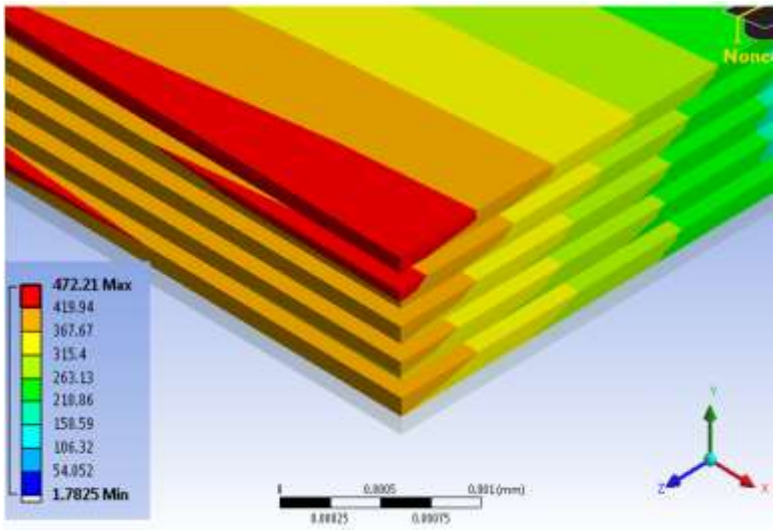

Figure 5.2 Case L1 – Equivalent stress (MPa) in low-k layers (submodel-2)

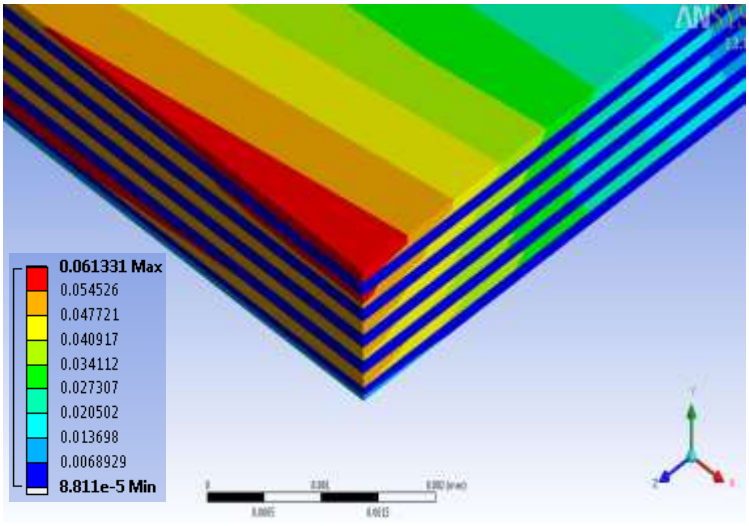

Figure 5.3 Case L1 – Equivalent strain (mm/mm) in Cu/low-k layers (submodel-2)

The maximum equivalent strain in the Cu/low-k region showed a drastic increment of 25% in the non-linear analysis. The location of the maximum equivalent strain followed the same pattern as that of von-mises stress for all design points (Fig 5.3 and 5.5). Likewise the von-mises stress, even the normal stress (Sy) significantly reduced by 3X. Table 5.1 shows the stress-strain variation in the Cu/low-k region for all the design points of DOE 1.

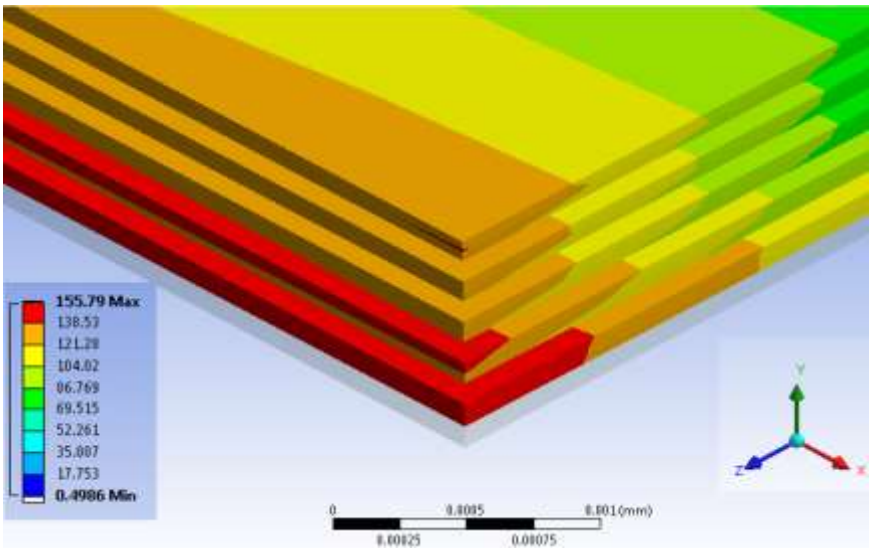

Figure 5.4 Case NL1 – Equivalent stress (MPa) in low-k layers (submodel-2)

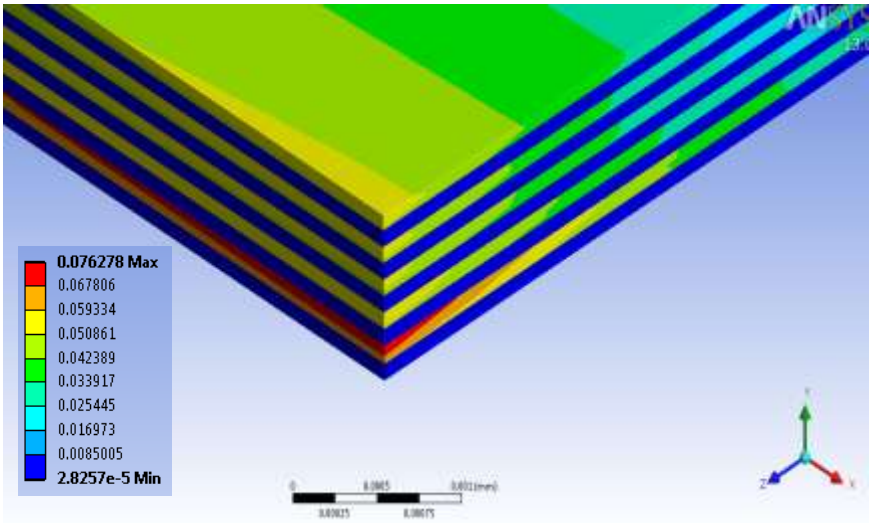

Figure 5.5 Case NL1 – Equivalent strain (mm/mm) in Cu/low-k layers (submodel-2)

During the product life, there is increasing concern over the reliability of flip chip packages with low-k dielectric. Therefore the selection of an underfill is important because it should not only provide low stresses in solder joint but also in low-k dielectric layers. The failure criteria considered is the delamination at the low-k layer which usually occurs at the interface between the low-k layer and the passivation layer at the outer edge of the die. To determine this delamination at the low-k layer, the normal stress (σ_y) and the principal stress between the Cu/low-k layers is analyzed. This is the most critical region to be considered for the package reliability because peeling stress in low-k and shear stress in the solder bump play a vital role during thermal shock analysis.

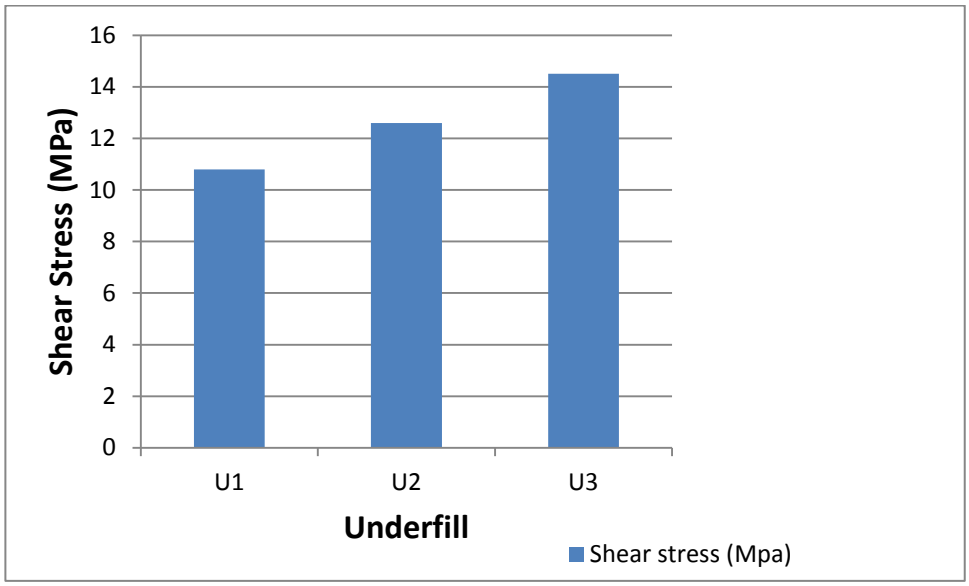

Figure 5.6 Shear stress in the solder bump (submodel 1)

5.3 Effect of Young's Modulus in underfill selection

FEA was performed on the package with the die thickness of 300um and a substrate thickness of 0.6 mm. As explained in Table 4.6, three underfills with different elastic modulus value and the same coefficient of thermal expansion (CTE) values were choosen to figure out the effect of E on bump and BEoL damage.The peeling stress (Sy) is transferred from the solder bump into the pad structure and then to the silicon die and significantly affects the BeOL.

It can be inferred from Fig 5.7, as the underfill becomes stiffer (U1- U3), the normal stress in the bump and the low-k layers increases, thereby making the underfill selection an important step.

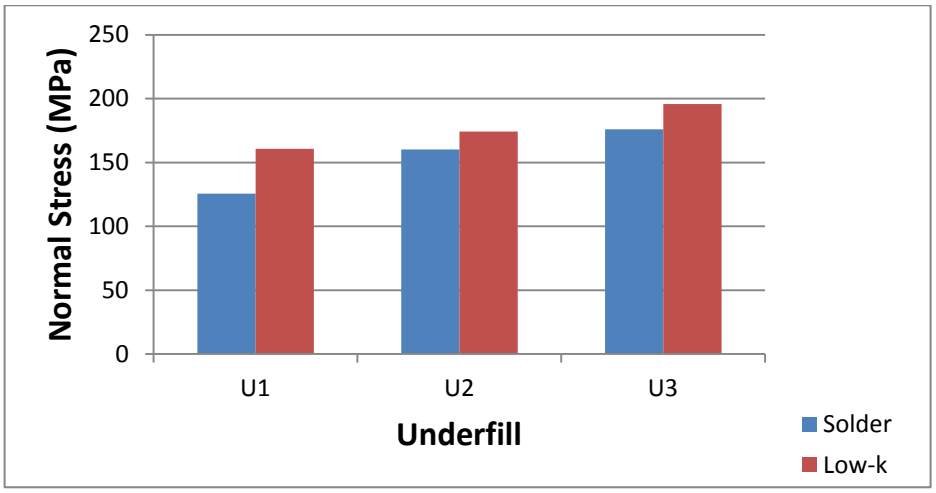

Figure 5.7 Normal stress in the solder bump (submodel 1) and low-k layer (submodel 2)

From Fig 5.8, it can be inferred that there is gradual increase in the stress value indicating that the value of E will plays a significant role in the selection of underfill. From this simulation it can be inferred that the normal stress in the low-k layers increased by 18 %, when the E value increased from 6.3 GPa to 15 GPa. An optimized E value for the underfill should be chosen such that it protects the solder bump and also reduce the damage to the low-k region.

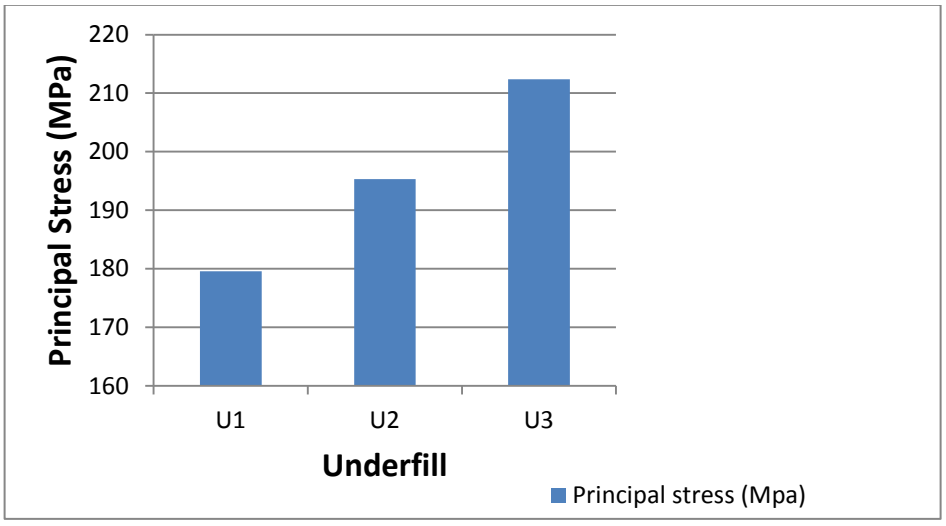

Figure 5.8 Principal stresses in the low-k layers (submodel 2)

5.4 Effect of Coefficient of Thermal Expansion in underfill selection

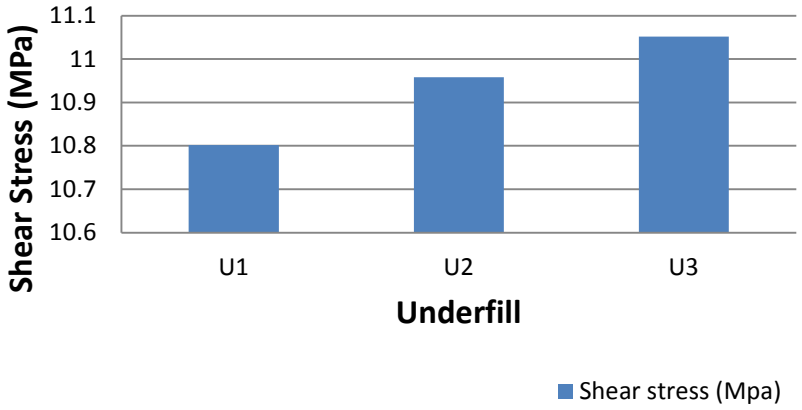

Figure 5.9 Shear stresses in the solder bump (submodel 1)

Similar to the above DOE, in the next case shown in Table 4.7, three underfills were choosen such that they have the same elastic modulus value but varying CTE. It can be inferred from Figure 5.10 that as the CTE value increases the peeling stress in low-k layers increase (U1-U3). In the solder region we can see a 14 % increase in the normal stress, when comparing the two extreme CTE's used (U1 and U3). For the metal/dielectric region, the variation is huge, 60% increase in normal stress for the two extreme cases (U1 and U3).

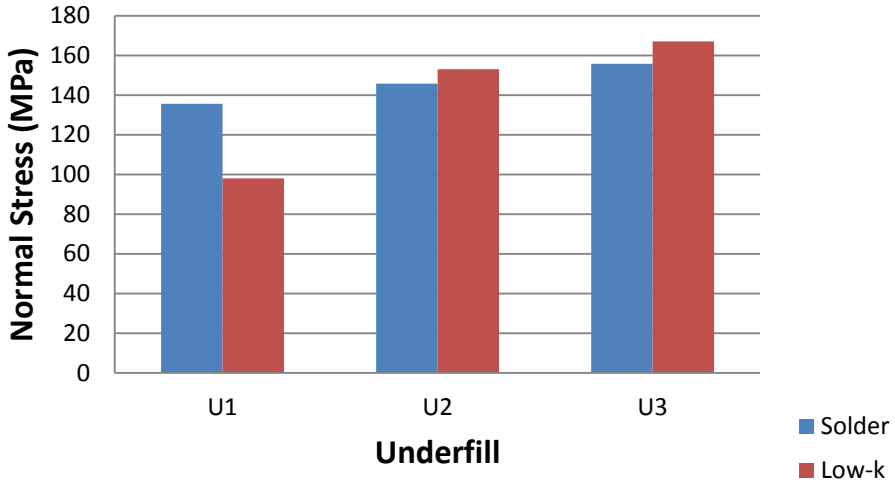

Figure 5.10 Normal stress in the solder bump (submodel 1) and low-k layer (submodel 2)

While considering the principal stress in Figure 5.11, there is a 39 % increase in the principal stress for the two extreme cases of underfill materials used. This analysis indicates that while choosing a underfill material, the lower the CTE of the underfill, the lower will be the stress induced in the low-k layers.

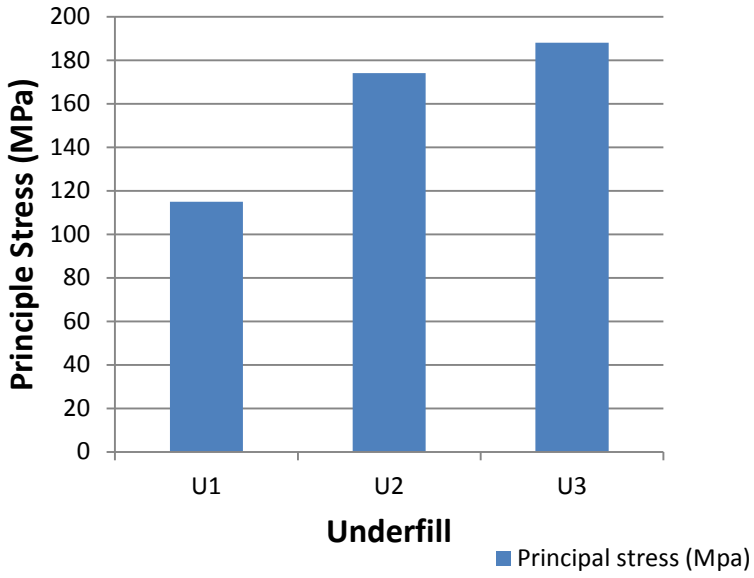

Figure 5.11 Principal stresses in the low-k layers (submodel 2)

By comparing the above set of results it can be concluded that, under thermal shock analysis of a flip chip package, underfill properties should be optimized in such a way that it improves the reliability of the package at the same time it doesn't affect the solder bump fatigue life. If we decrease the value of the E, we can reduce the delamination of the Cu/low-k layers and at the same time reducing the CTE to the smallest possible will yield to a better package performance.

5.5 Effect of Die thickness

A parametric FEA study was performed to study the effect of the die thickness on the delamination/peeling stress of the Cu/low-k layers in the package. As discussed in Table 4.9, the analysis consists of three different die thickness 100,300 and 500 um for the 12 x 12 mm die package. The FEA analysis (Fig 5.12 and Fig 5.13) indicates that as the die gets thinner the

normal stress and the principal stress in the Cu/low-k material decreases. These results are expected because the delamination stress in the package reduces because the thinner die yields when compared to the thicker die.

Figure 5.12 Normal stress in the low-k layer (submodel 2)

Table 5.2 Warpage in the Cu/low-k region

CASES	Number of layers	Die Thickness(microns)	Out of Displacement metal/dielectric region (um)
1	10 layers	100	81.1
2	10 layers	300	72.2
3	10 layers	500	53.4

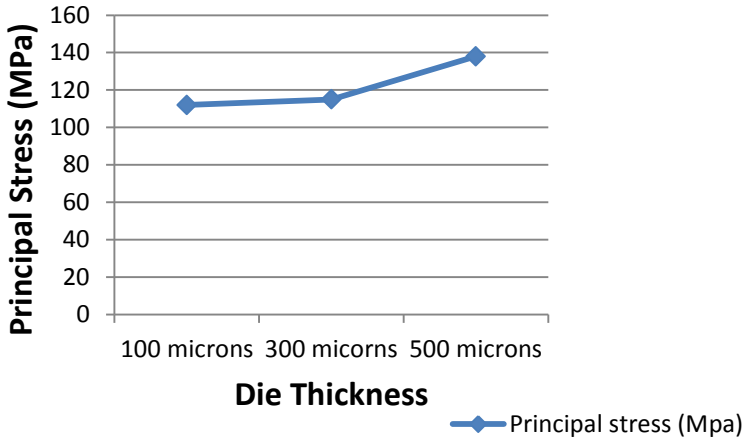

Figure 5.13 Principal stress in the low-k layer (submodel 2)

5.6 Effect of Number of layers

The next parametric study was based on the effect of the number of layers as discussed in Table 4.8. In the same flip chip package with 12 mm x 12 mm die, the number of BEoL metal/dielectric layers was varied in three cases 10, 14 and 18. From the results in Figure 5.14 it can be inferred that as the number of layers increase the normal stress induced in the Cu/low-k region decreases.

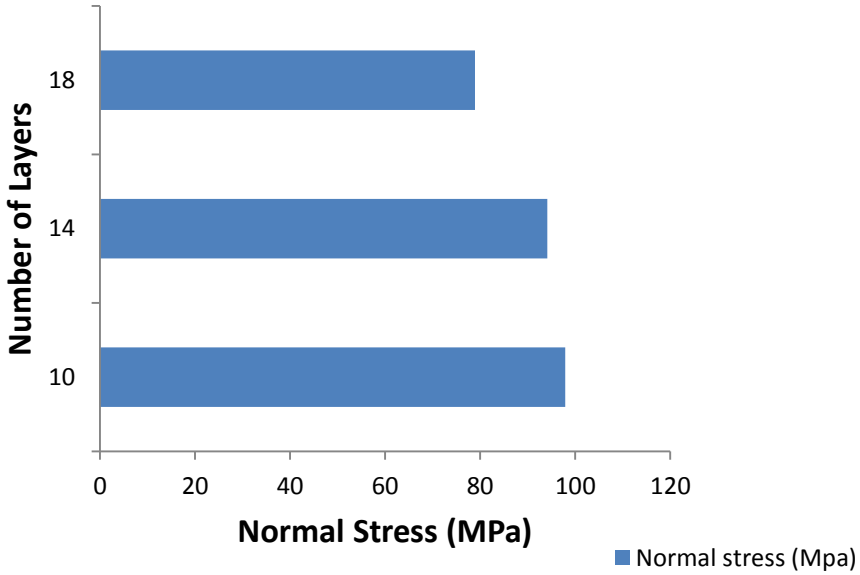

Figure 5.14 Normal stress in the low-k layer (submodel 2)

It appears that as the number of interconnect BEoL layers increase; they act as a better cushion to reduce the stresses in the low-k layer during thermal loading. This increase should have a limitation based on the application to optimize the manufacturing cost.

CHAPTER 6

CONCLUSION

6.1 Conclusion

Parametric thermo-mechanical analysis of the package with Cu/low-k BEoL layers has been performed in this work. A methodology that accurately estimates the mechanical integrity of the BEoL region has been formulated using the multi-level FE modeling technique with non-linear dielectric. Non-linear analysis, as expected, demonstrated a significant difference in the thermo-mechanical response of the Cu/low-k region and looks to be more realistic. While maximum von-mises stress decreased by 3X from linear analysis to non-linear, the linear model under predicted the equivalent strain by 25%. This feasibility study indicates that the non-linear analysis is a more realistic methodology to perform the CPI analysis of such technologies. Though the linear analysis is much faster, it could lead to a BEoL design that is not optimal (in terms of metal/dielectric dimensions, no. of layers, etc.), thereby resulting in performance and reliability hit. Increase in the number of metal/dielectric layers significantly affects the maximum equivalent strain in the Cu/low-k region, thereby putting a constraint on the maximum number of metal layers. More layers act as a cushion to reduce the stress in the metal/dielectric region during thermal loading and at the same time it has to be optimized from the cost perspective.

As expected, the solder joint normal stress (Sy) increased with the underfill stiffness resulting in a 20% increment in the principal stresses in the dielectric region. The underfill material is used to provide good protection for the solder bumps and metal/dielectric region, thereby making its selection an important design step. A thin die is recommended to reduce the delamination stress in the low-k material, which will also leads to improved solder joint reliability due to the fact that thinner die is more compliant.

6.2 Future work

- Investigate the interface delamination and cracking of the of the low-k layers in flip chip packages under temperature cyclic loading using finite element analysis. The total energy release rate can be used as fracture parameter to describe the energy flow into the crack tip per unit fractured area.
- Investigation of the chip package interaction when the flip chip package is subjected to a reflow process for attachment to substrate, and examine the mechanical integrity of the BEoL region against white bumping, etc.,

REFERENCES

1. Computer Measurement Group website : http://www.cmg.org/measureit/issues/mit41/m_41_2.html
2. Flip chip package reference guide – Literature Number – SPRU811A, May 2005, TI.
3. X. Zhang, “Chip package interaction (CPI) and its impact on the reliability of flip chip packages”, Dissertation, The University of Texas at Austin, Dec 2009.
4. Flip chip website: http://flipchips.com/tutorial/other/introduction-to-flip-chip/.
5. Flip chip International :http://www.impress-creative.com/flipchip/bump_heights-130um.php
6. R. Rosenberg, D.C. Edelstein, C. K. Hu, and K.P. Rodbell, “Copper Metallization for high performance silicon technology”, Annual Reviews 2000.
7. C.J. Zhai, U. Ozkan, A.Dubey, Sidarth, R.C. Blish II and R.N. Master, “Investigation of Cu/low-k Film delamination in flip chip packages”, ECTC 2006.
8. L.L Mercedo, S. Kuo, T. Lee, and S.K. Pozder, “Analysis of Flip chip packaging challenges on copper/Low-k interconnects”, IEEE Transactions on Device and Materials Reiliability, VOL. 3, NO.4, DEC 2003.
9. D. Edelstein, H. Rathore, C. Davis, L. Clevenger, A. Cowley, T. Nogmni, and B. Agarwala, “Comprehensive Relaibility Evaluation of a 90 nm CMOS Technology with Cu/PECVD Low-k BEOL”, IEEE 2004.
10. T.H. Wang, and Y. Lai, “Submodeling Analysis for Path-Dependent Thermo-mechanical Problems”, Journal of Electronic Packaging, 2005 ASME.

11. F.X. Che, X. Zhang, W.H Zhu, and T.C. Chai, “Reliability Evaluation for Copper/Low-k Structures Based on Experimental and Numerical Methods”, IEEE Transactions Sep 2008.
12. G.G. Harman, and C.E. Johnson, “Wire Bonding to Advanced Copper, Low-k Integrated Circuits, the Metal/Dielectrics Stacks, and Materials Considerations .
13. O. Jimmy, “Structural Desgin and Optimization of 65nm Cu/low-k Flip chip package”, Thesis Defense, 2008.
14. C. Kuo, M. Yip, K. Chiang and C. Tsou, “Characterization Study Time and Temperature-Dependent Mechanical Behaviour of Polyimide Materials in Electronic Packaging Applications”, Journal of Electronic Materials, Vol 34, No. 3, 2005.
15. C.Yuan, C.N. Han, M. Yew, C. Chou, and K. Chiang, “Design, Analysis, and Development of Novel Three-Dimesnional Stacking WLCSP”, IEEE Transactions of Advanced Packaging, Vol., 28, NO., 3, August 2005.
16. F.X. Che, H.L.J Pang, W.H. Zhu, A.Y.S Sun, and C.K. Wang and H.B. Tan, “Development and Assessment of Global-Local Modeling Technique Used in Advanced Microelectronic Packaging.
17. L.K. Oon, “Solder Joint Reliability of Flip chip BGA Package”, Thesis, March 2004.
18. C. Kuo, M. Yip, and K. Chiang, “Time and Temperature-Dependent Mechanical Behavior of Underfill Materials in Electronic Packaging application”, Microelectronics Reliability 44 (2004) 627-638.
19. W. Qiang, L. Lihua, C. Xuefan, and W. Xiaohong, “Experimental Determination and Modification of Anand Model Constants for Pb-Free Material 95.5Sn4.0Ag0.5Cu”.
20. Y. Lai, and T.H. Wang, “Verification of Submodeling Technique in Thermo-mechanical reliability assessment of Flip chip Package Assembly”, Microelectronics Reliability 45 (2005) 575-582.

21. G. Wang, C. Merrill, J. Zhao, S.K. Groothuis, and P.S. Ho, “Packaging Effects on Reliability of Cu/Low-k Interconnects”, IEEE Transactions on Device and Materials Reliability, Vol., 3, No. 4, December 2003.
22. C. Kao, Y. Lai and T.H. Wang, “Numerical Evaluation of Thermal Cycling Reliability of High Performance Flip Chip Package Assembly using Submodeling Analysis”, Journal of Chinese Institute of Engineers, Vol., 30, No. 2, pp. 349-352(2007).
23. H. Peng, R.W. Johnson, G. Flowers and A. Rickettes, “Underfilling Fine Pitch BGAs”.
24. V. Nagaraj, “Flip Chip Back End Design Parameters to Reduce Bump Electromigration”, Thesis, University of Texas at Arlington, August 2008.
25. E. Barti and M. Stecher, “Using Submodeling Technique to Understand Passivation Cracks in Microelectronic Devices Pre-processing with ANSA”, 2nd ANSA and ETA International Congress, 2007.
26. P.K Mallick and Y. Zhou, “Yield and Fatigue behavior of polypropylene and polyamide-6 nan0composites”, Journal of Materials Science 38 (2003) 3183-3190.
27. S.B. Park, and I.Z. Ahmed, “Shorter Field Life in Power Cycling for Organic Packages”, Transactions of ASME, Vol. 129, March 2007.
28. M. Morgen, E.T Ryan, J. Zhao, C. Hu, T. Cho, and P.S. Ho, “Low Dielectric Constant Materials for ULSI Interconnects”, Annu. Rev. Mater. Sci. 2000. 30:645-80.
29. D.E.H. Popps, A. Mawer, and G. Presas, “Flip Chip PBGA Solder Joint Reliability: Power Cycling versus Thermal Cycling”.
30. F. Maseeh, and S.D. Senturia, “Viscoelasticity and Creep Recovery of Polyimide Thin Films”, IEEE 1990.
31. Y.J. Lee, “Viscoplastic Finite Element Simulation to Predict the Solder Joint Fatigue Life of Different Flash Memory Die Stacking Architectures”, Thesis, The University of Texas at Arlington, May 2006.
32. Ansys Help File, “www.ansys.com”.

33. J.N. Reddy, “Introduction to Finite Element Method”.
34. D. Shamiryan, T. Abell, F. Lacopi, , K. Maex, ”Low-k dielectric materials", Materials Today, January 2004.
35. D. Wang, X. Ma, and D. Guo, “Reliability analysis of lead free flip chip solder joint”, IEEE 2007.
36. A. Menon, S. Karajgikar, D. Agonafer, “Thermally design optimization of a package on package”, 25th IEEE SEMI-THERM Symposium, 2009.
37. Website:www.amkor.com

BIOGRAPHICAL INFORMATION

Thiagarajan Raman completed his Bachelors of Engineering in Mechanical Engineering from Anna University, Chennai, India. He completed his Master of Science degree in Mechanical Engineering in December 2012. He was part of the Electronics, MEMS, Nano-electronics Systems Packaging (EMNSPC) research team from January 2011. His research primarily deals with device level packaging of a flip chip with BEoL interconnects. He has authored and coauthored five conference papers related to electronic packaging.