FLIP CHIP BACK END DESIGN PARAMETERS TO REDUCE BUMP ELECTROMIGRATION

by

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ABSTRACT

FLIP CHIP BACK END DESIGN PARAMETERS TO REDUCE BUMP ELECTROMIGRATION

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The advancement in flip chip technology has enabled us to meet the requirement of smaller die size along with the increased functionality. Due to this development in flip chip packaging technology along with higher current carrying requirement of solder bumps, electromigration has now become a reliability concern.

In this research, a commercially available finite element tool is adopted in order to study the distribution of current density in eutectic solder bump for variety of back end design parameters. Geometries needed were generated by using Pro/Engineer® Wildfire™ 3.0 as a Computer-Aided-Design (CAD) tool and were transferred to ANSYS® 10.0, where meshed analysis was conducted.

Parameters such as passivation opening (PO) diameter, trace width, under bump metallurgy (UBM) thickness and UBM diameter were studied in detail. The results were evaluated for input currents of 0.1 A and 0.5 A. Based on the results, a guideline for solder bump configuration is proposed.

In the metallization, the most important design attribute found is the Al trace width. In the metallization of the structures used in our study, current density varied from $5x10^5$ A/cm^2 to $7x10^5$ A/cm^2 and from $2.5x10^6$ A/cm^2 to $3.5x10^6$ A/cm^2 at 0.1 and 0.5 A per bump, respectively.

In the solder bump, the most important parameters found are Al trace width and UBM thickness. In the solder of the structures used in our study, current density varied from $2.8x10^3$ A/cm^2 to $4.2x10^4$ A/cm^2 and from $1.4x10^4$ and $2.1x10^5$ A/cm^2 at 0.1 and 0.5 A per bump, respectively.

Simulation was done to show the effect of stress on passivation opening of the solder bump. Results show that bumps with small PO diameter show higher stress levels. Also, maximum stress is noted at the same location where current crowding occurs.

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CHAPTER 1

INTRODUCTION

1.1 Background

Present day market demands shorter product life cycles with increased product complexity. The union of broadband communications and digital technology has increased product opportunities [1].

Integrated Circuits (IC's) have encompassed almost all aspects of modern technology. Wireless communication and computing products constitute over 75% of the world's semiconductor consumption. Consumer electronics market is demanding reduction in size, weight, cost and power. The reduction of the minimum dimensions enables the integration of more number of transistors on a single chip, as described by Moore's Law. This cannot be met without technical innovation. Of the enabling technologies, System-in-a-Package (SiP) and System-on-a-Chip (SoC) have emerged as drivers. On the other hand, many functional requirements, such as power consumption, wireless communication (RF), passive components, sensing and actuating, and biological functions do not obey Moore's Law. Figure 1.1 graphically represents Moore's Law. Since the beginning of this decade, there has been an increased concern for the reliability of micro-electronic packages. Primary reason for this has been the demand for smaller pitch devices along with harsh operating conditions (higher temperature, current, *etc.*).

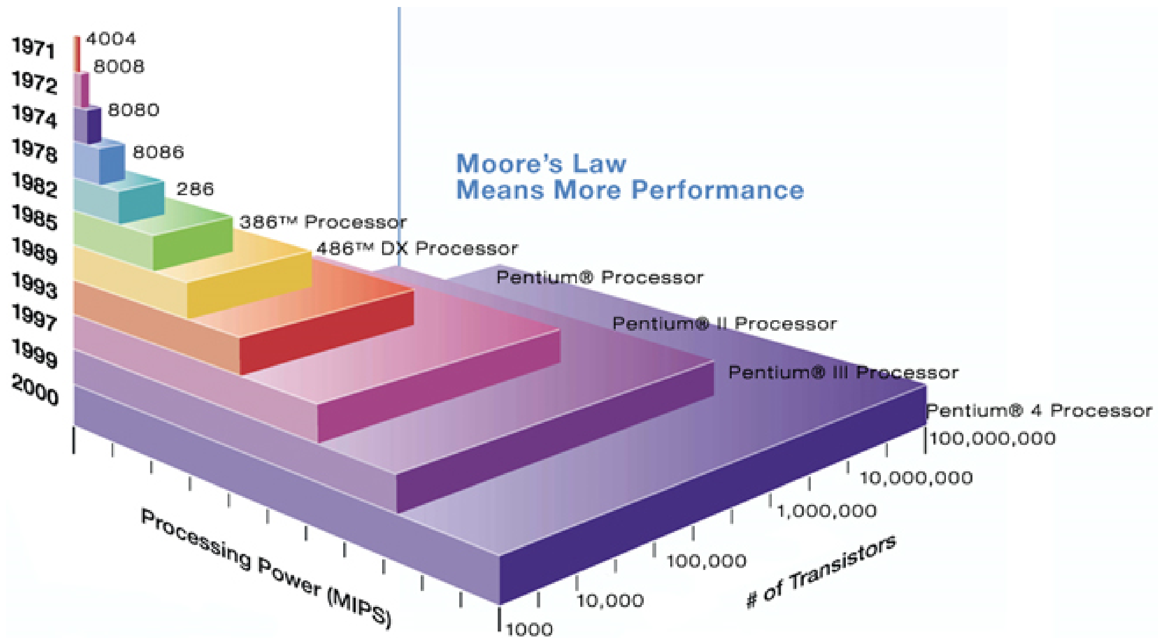


Figure 1.1: Moore's Law [2]

1.2 Flip Chip Technology

1.2.1 Introduction to Flip Chip Technology

To keep up with the ever increasing I/O demand, the solder-bump flipchip interconnection is increasingly used by the semiconductor industry. Flip-chip technology was developed in the early 1960s to improve the reliability and productivity as well as reduce cost of manual wire bonding. This type of interconnection is also called controlled-collapse-chip connection (C4) which utilizes solder bumps deposited on wettable metal terminals on the chip and joined to a matching footprint of solder terminals on the substrate [3-5]. Because the entire chip area can be used for the bump array, the I/O density is greatly increased. Figure 1.2 is an illustration of a flip chip package. The upside down chip (flip chip) is aligned to the substrate, and all connections are made simultaneously by reflowing the solder.

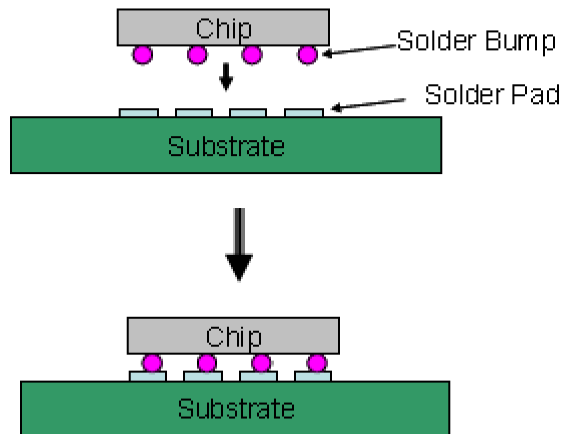


Figure 1.2: Illustration of Flip-chip package

Shown in Figure 1.3 is the schematic view of the cross-section of a reflowed solder bump. Because the solders usually do not wet the bare silicon or dielectric materials such as SiO_2, an under-bump metallization (UBM) layer is deposited on these substrates first in order to make the connection. The UBM usually consists of three layers:

(1) An adhesion layer, such as Cr or Ti, capable of forming a strong bond with the passivation such as SiO_2, and with the terminating Al pad.

(2) A solder wetting layer, such as Ni or Cu, which must remain at least partially intact throughout the assembly and test process. An additional requirement of the adhesion and/or wetting layer is to form a barrier system to preclude the penetration of solder into the chip wiring or under the passivation.

(3) An oxide-resistant layer, Au or other noble metal, to retain wettability for the solderable layer when vacuum is broken.

In the example in Figure 1.3, the adhesion layer is the Ti. A thin layer of Cu is then sputtered on top of the Ti layer to act as the electrode for electroplating of the next layer of Ni. The final Ni layer ensures good solder wettability with the solder alloy and act as a robust solder diffusion barrier to guarantee that the bump metals and bond pad metals do not react with each

other to degrade the reliability of the system. There was a protective layer of Au which dissolved into the solder during the reflow process.

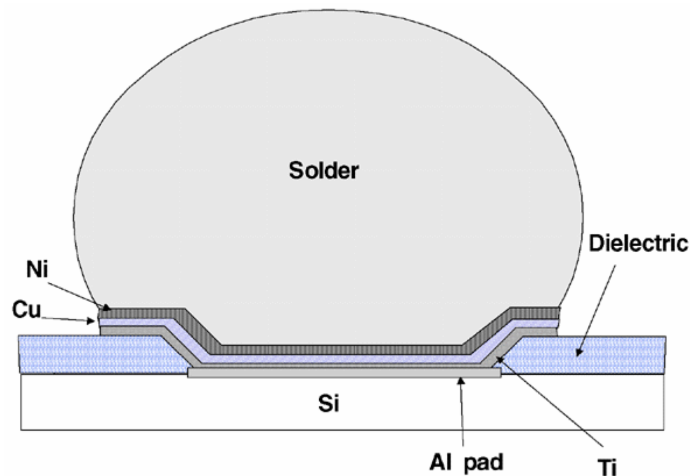


Figure 1.3: Typical structure of flip chip solder bump [6]

The solder bump serves as the interconnection between the silicon chip and the rest of the electronic system. The solder self-centers and collapses when fully reflowed, making assembly less difficult and enhancing the reliability of the joint. The solder bump can take the shape of an hourglass, barrel, and drum depending on the distance between the chip and the substrate, pad size, and the volume of the solder. The two types of processes which are normally used to form the solder bump on silicon chip are the evaporative process and the electroplate process. These methods are shown in Figure 1.4 [3].

Solder bumps are deposited selectively in the evaporative process Figure 1.4 (a) through a molybdenum (Mo) shadow mask. The initial process step is to define the bump pad area with photolithography. This is followed by the evaporation of the under bump metallization. The next step is to evaporate the bump alloy to form the bulk of the bump. Finally, the bump is reflowed to homogenize the solder and allow the alloy to form an intermetallic compound with the UBM. This provides the necessary adhesion between the die and the bump.

The electroplate process begins with depositing the bump's UBM base structure on the wafer in blanket form using sputtering. A process that involves thick photo-resist coating, alignment, exposure, and development is used to define the remaining bump structures that are to be selectively electroplated on top of the sputtered UBM. The solder bump alloy of choice is plated to form the structure after the photo process. The photo-resist is stripped and the UBM layers are wet etched away after plating is finished. Ashing, fluxing, reflowing, and cleaning complete the process Figure 1.4 (b).

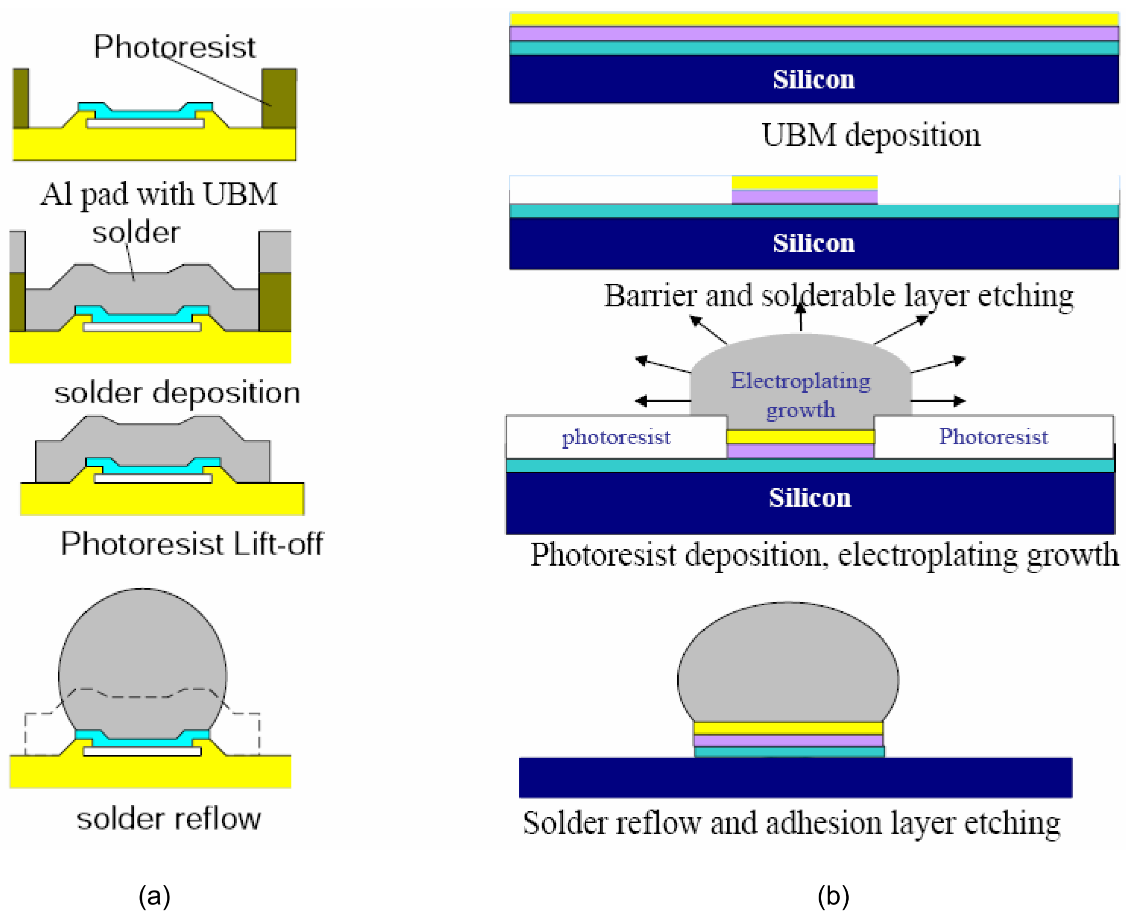


Figure 1.4: Two typical forming processes of flip chip solder bumps (a) Evaporative (b) Electroplated

1.2.2 Typical Solder Alloys Used for Flip Chip Bumps

Pb-Sn alloy has been used for soldering material for a long time. The first C4 bump was made with Pb-Sn alloy with over 90wt% Pb. It is still the most commonly used solder alloy in flip chip applications. Typically two types of Pb-Sn systems are used. The high-Pb solder (95-97% by weight) has the melting temperature of 305-320°C. It is normally jointed with ceramic substrates since the solder reflow process requires a peak temperature around 360°C to ensure complete melting of the bump. The eutectic Pb-Sn alloy (37wt%Pb-63wt%Sn) has a melting point of 183°C, and is used more often on organic substrates which can not survive temperature over 240°C.

The employment of Pb-free alloys is greatly increased due to the environmental legislation for the past few years. Most of the Pb-free alloys so far are Sn-based with small amount of additive elements. One example is the Sn-Ag alloy. The eutectic Sn-Ag alloy (96.5wt%Sn-3.5wt%Ag) has a melting point of 221°C, which is lower than the high-Pb alloy but higher than the eutectic Pb-Sn alloy. Data in the literature suggests that the thermo-mechanical reliability of Pb-free alloy can be as good as or better than eutectic Sn/Pb [7-13]. At the same time, new reliability issues may also arise with the introduction of Pb-free alloys. For example, due to Pb-free alloy's higher yield strength and lower ductility, electronic packages with Pb-free interconnect tend to have reduced mechanical robustness, a property critical for hand-held applications.

1.2.3 Failure classification and mechanisms in a Flip Chip package

The failures in Flip Chip package are not unique to Flip Chip technology but relative rate of occurrence may be influenced by the use cases and operational environment for Flip Chip. Classification of failures and failure mechanism are listed in Table 1.1 below.

Table 1.1: Failure Classifications and Mechanisms [14]

Basic failure mechanisms	#	Failure origins and driving forces	Failure examples	Fault isolation and failure analysis methods
A: Coherent crack formation	1	Thermo-mechanical mismatch	Chip solder fatigue BGA solder ball fatigue Fracture of an embedded passive component Die-to-die spacer crack Underfill crack IC metal line open	**Stress analysis**: by Thermoire-Interferometry, Speckle Interferometry (ESPI), Deformation analysis by image correlation, x-ray diffraction **Fault isolation**: by Magnetic microscopy, Time domain reflectance, Lock in thermography, TIVA, OBIRCH **Crack detection**: by Scanning Acoustic Microscopy, Cross section analysis with light microscopy, SEM or FIB/SEM
	2	Mechanical loading (application- or process-induced)	IC dielectric crack Organic substrate crack Solder ball crack (drop)	
	3	Hygroscopic swelling	Mold compound cracking, die cracking, substrate cracking	
	4	Reaction-induced volume shrink or expansion (e.g. curing)	Mold compound cracking, die cracking	
	5	Internal pressure (e.g. moisture vaporization at increased temperature)	Mold compound cracking, die cracking	
B: Interfacial delamination	1-5	Same as 1-5	IC dielectric delamination Underfill delamination Delamination between stacked dies Organic substrate delamination Mold compound delamination	**Stress analysis**: by Thermoire-Interferometry, Speckle-Interferometry (ESPI), Deformation analysis by image correlation, x-ray diffraction **Crack detection**: by Scanning Acoustic Microscopy, Cross section analysis with light microscopy or SEM, FIB/SEM, FIB/TEM
	6	Interface reactions causing loss of adhesion (e.g. moisture-, oxidation-, contamination-related)	Underfill delamination Mold compound delamination Organic substrate delamination	**Crack detection**: by Scanning Acoustic Microscopy, Cross section analysis with light microscopy or SEM, FIB/SEM, FIB/TEM **Surface analysis**: by TOF-SIMS, XPS, AES, TEM+EDX, TEM+EELS

Table 1.1 - Continued

Basic failure mechanisms	#	Failure origins and driving forces	Failure examples	Fault isolation and failure analysis methods
C: Void and pore formation	7	Mechanical creep	IC Solder ball fatigue BGA solder ball fatigue	**Fault isolation**: by Magnetic microscopy, Time domain reflectance, Lock in thermography, TIVA, OBIRCH **Void detection**: by x-ray microscopy or x-ray tomography Cross section analysis with light microscopy, SEM or FIB/SEM (with EDX,WDX, EBSD and x-ray diffraction for analysis of intermetallics)
	8	Diffusion (Kirkendall void formation) and Intermetallics formation	IC UBM lift Void in IC interconnect or in via Wire bond lift BGA solder ball lift	
	9	Electromigration	Void in IC metal line or solder, Void in solder, metal line or via in the BGA substrate	
	10	Thermomigration	Void in IC metal line or solder, Void in solder, metal line or via in the BGA substrate	
D: Material decomposition and bulk reactions	11	Chemical corrosion	Bond wire lift	**Fault isolation**: by Magnetic microscopy, Time domain reflectance, Lock in thermography, TIVA, OBIRCH **Failure analysis**: by Cross section analysis with light microscopy or based on FIB/SEM with EDX or WDX, TEM, TOF-SIMS, XPS, FTIR spectroscopy, , mechanical testing, TGA, DMA, DSC (ageing), EBSD (grain analysis)
	12	Galvanic corrosion	Bond wire lift	
	13	Ageing (UV, …)	Organic substrate cracking or delamination Underfill cracking or delamination	
	14	Grain coarsening, phase separation	Wire bond rupture IC solder ball fatigue BGA solder ball fatigue	

CHAPTER 2

ELECTROMIGRATION

2.1 Introduction to Electromigration (EM) mechanism

EM in interconnects has been studied the late 1960's when it was first observed in wide Al-based interconnects [15]. As one of the main IC failure mechanisms, EM performance will continue to be one of the main issues in integrated circuit reliability for a relatively long time. Modern microelectronic devices use either Al or Cu thin films as interconnection materials, both of which are susceptible to physical failure by EM. Although the signal current itself is small, due to the sub- micron scale of the interconnects, current density is sufficient to induce EM. A small amount of EM in the interconnect can result in catastrophic circuit failure by void formation or hillock formation. Therefore, it is of great importance to accurately assess the effect of EM on interconnect reliability.

2.1.1 Mechanism of Electromigration (EM)

The EM refers the phenomena of atomic transportation in a conductor under the influence of high electrical current density. High current density provides driving force to atoms migrate to the direction of electron flow. The driving force for EM consists of the two forces acting on metal atoms [15-19]. The first is the interaction of the applied electric field and the metal ions. This electrostatic force contains the interaction of the ion with valence Z and applied field as well as any electrostatic shielding from the surrounding electrons. This contribution is often referred to as the "direct" force. The direct force can be written as,

$$F_D = Z(1 - \tilde{k})\, eE$$

$$= Z_D^*\, eE \qquad (2.1)$$

Where, k describes the electrostatic shielding and Z_D^* is the effective charge caused by the electrostatic force F_D^*, $Z_D^* = Z\ (1-k)$. The second contribution to the total force, F, arises from the momentum transferred to the ions from the electrons. This contribution is often referred to as the "electron wind" force.

The simple theoretical description of the wind force can be seen from the following discussion. In a given conductor, the number of collision per unit time between the electrons and diffusion ions, $n_{collision}$, is approximately given by,

$$n_{collision} = n_e\ v_e\ \sigma_e \qquad (2.2)$$

Where, n_e is the number density of electrons, v_e is the average electron velocity, and σ_e is the cross section for scattering between an electron and a diffusion ion. In the scattering process, the electron transfers all of the momentum it gained since its previous collision. The average momentum transferred per collision is given by

$$\Delta p = eE\ l_e / v_e \qquad (2.3)$$

Where e is the charge of an electron, E is the electric field and l_e is the mean free path of the electrons. The product of these two equations is the wind force

$$F_{wd} = -\ n_e\, \sigma_e\, |e|\ E\, l_e \qquad (2.4)$$

As defined in eq.2.4 the wind force is directly proportional to the electric field applied to the metal. It is traditional to define an effective charge of the metal ions

$$F_{wind} = Z_{wd}\ ^*\ eE \qquad (2.5)$$

Where, Z_{wd} is the valence of the diffusion ion. The total force, F, is simply the sum of these two components.

$$F = F_D + F_{wd} \qquad (2.6)$$

$$= (Z_D + Z_{wd})\ eE$$

$$= Z^*\ eE \qquad (2.7)$$

Where Z^* is the effective charge number for the migrating metal ions describe in this system. Z* can be either positive or negative depending on the direction along which migrating ions diffuse. Depending on which of the force is stronger, metal atoms toward the cathode or

anode end of the conductor. However, for a good conductors Z* is found to be in the range of ~ -10, indicating that the direct force is small compared to the wind force. It is generally believed that the contribution of the direct force is reduced substantially by screening effects by free electrons. Therefore, electron "wind" force is dominant and metal atoms migrate in the same direction as the electron flow [15-19].

Under the given driving force, the metal atoms move with rate controlled by the diffusivity. The atomic EM flux can then be obtained through the relation J=μF, where μ the atomic mobility. The atomic mobility is related to the atomic diffusion coefficient, *D,* by the Nernst-Einstein equation, $v=nD/kT$, where n is the mass density of the metal, k is the Boltzmann's constant and T is the absolute temperature [20].

By substituting the applied electric field with the product of the current density, j, and the metal resistivity, ρ, the following equation is derived.

$$J_e = n\,(D / kT)\, Z^* \underset{.}{e}\, \rho\, j$$
$$= n\, v_e \qquad (2.8)$$

Where, J_e is the atomic flux due to EM and V_e is the drift velocity due to EM. Drift velocity is a product of the mobility (D / kT) times EM driving force F:

$$v = (D / kT)\, F \qquad (2.9)$$

Hence, the drift velocity due to the EM force is give by,

$$v = (De\, \rho\, j\, Z^*) / kT \qquad (2.10)$$

The atomic diffusion coefficient D is a function of temperature in Arrhenius equation as follows [21]:

$$D = D_o \exp(-E_a / kT) \qquad (2.11)$$

Where D_O is a proportionality constant (m^2/sec), E_a is the activation energy (eV) associated with the diffusion mechanism (or path). At fixed temperature, the value of D is different for different diffusion paths.

Since the dependence of ρ on T is nearly linear, v / j follow Arrhenius behavior. Therefore, the EM flux becomes,

$$J = (n/kT)\, D_o\, e^{-Q/kT}\, e\, \rho\, j\, Z^* \qquad (2.12)$$

It can be seen that EM flux is determined by temperature in addition to electric current applied.

2.2 Electromigration in interconnects

The interconnects of modern semiconductor are highly dense and intricate networks containing millions of line segments terminating with vias and contacts. As the interconnect dimension becomes smaller, they become more susceptible to EM induced failures due to increase in current densities and surface/interface fraction. EM itself in interconnects can occurs through several different diffusion paths. These paths include diffusion through the bulk, grain boundaries, interfaces, and surfaces.

With several mechanisms contribute to EM mechanism, the activation energy (Ea) for EM failure in interconnects can be a function of temperature since a particular diffusion mechanism dominated a temperature range. The bulk diffusion term can be ignored because the temperatures of practical importance are too low for the bulk diffusion to be significant compared to others. Thus, the most important diffusion mechanisms to be considered for Cu interconnects are the grain boundary diffusion and interface diffusion [22-24].

Another important consideration of EM in interconnects is the presence of the stress-induced back flow, namely the 'Blech' effect [25, 26]. If the particular metal line of interest is embedded in a stiff dielectric material like SiO_2 the back flow force is created which opposed to the EM force. This force arises as atoms are depleted from the cathode and accumulated at the anode. The accumulation and depletion of mass in confined space creates the stress. In places where mass is accumulated, compressive stress is induced. In the opposite case, tensile stress is developed. In interconnects, these two places are closely spaced, resulting in a steep stress gradient. This stress gradient counteracts the EM force and reduces the net atomic flux, as illustrated in Figure 2.1.

In this configuration, $\Delta\sigma$ is the local gradient in the hydrostatic stress in Cu and its maximum value is a function of the surrounding structure. For stiff surroundings, $\Delta\sigma$ can reach a higher value than for a more compliant structure.

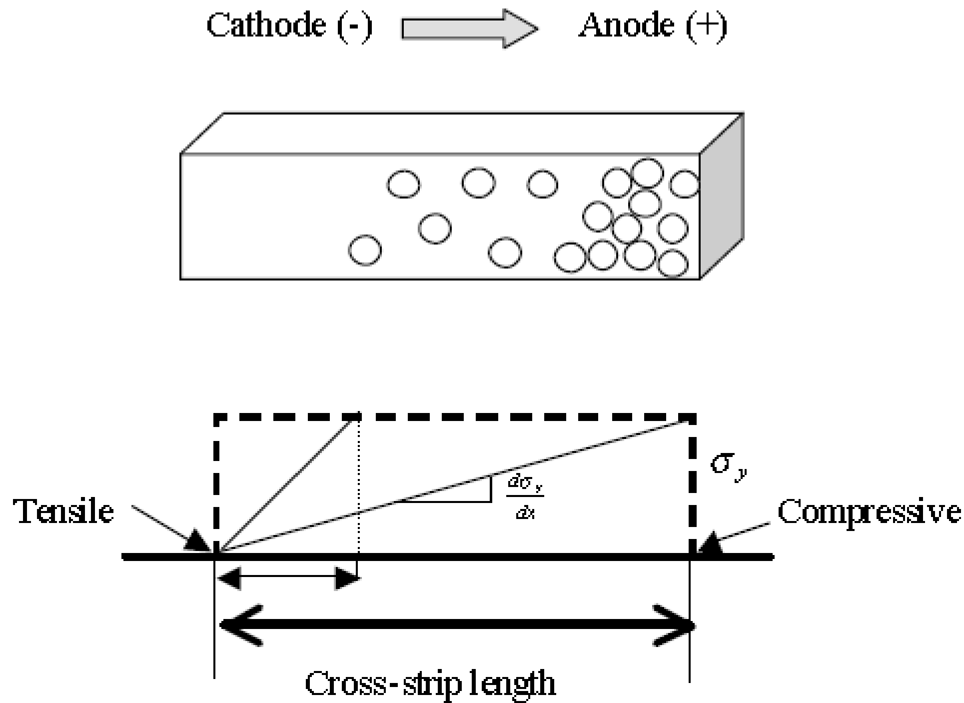


Figure 2.1: The schematic diagram illustrating net atomic flux and stress gradient

2.3 EM failure in interconnects

2.3.1 EM lifetime testing

The most common method for evaluating the EM reliability is a lifetime measurement under accelerated conditions (high temperature and high current density). EM performance is characterized by the mean time to failure (MTTF) that is the time at which 50% of the test sample has failed cumulatively, and σ that is the dispersion of time-to-failure distribution.

In 1969, Black conducted a series of accelerated testing designed to evaluate the temperature and current density dependence of the time to failure [27, 28].

MTTF is defined as,

$$MTTF = Aj^{-n}e^{(\frac{Q}{kT})}$$

Where, A is technology-dependent and structure-dependent pre-exponential factor and is dependent on the material and conductor geometry, j is the current density (A/cm^2), n is the current density exponent, where n varies between 1 and 2 depending on the mode of failure (during void formation or void growth). Q is the activation energy of the EM associated with the diffusion mechanism, k is Boltzmann's constant and T is the absolute temperature. The MTTF and σ are obtained from the log-normal curve that is the best fit for EM time-to failure.

High MTTF and low σ are desired for good EM performance. The chief benefit of lifetime test is the ability to test large numbers of specimens at the same time. However, it would be difficult to determining the mechanisms of EM failure solely using this method.

The main purpose of the EM lifetime testing is to determine the activation energy and current dependence of the failure rate for given interconnect structure. Such testing is necessary because the prediction of the interconnect reliability under use condition needs to be conducted for any given set of interconnects produced. In addition, the testing is conducted to identify the weak part of interconnects that needs to be improved for better reliability.

The latter part is especially important for interconnect development because EM failure rate is affected greatly by many factors in interconnects and the reduction of the potential failure site can be achieved by EM testing. Many factors contributing to the EM failure rate, and such factors are related to site for flux divergence. Such places include locations with a change in current density and direction, interface between different materials, defects such as grain triple points, conductive and non-conductive contaminants, dopant precipitate and segregation, grain size variations, and so on.

2.4 Why is Electromigration a Concern in Flip Chip Solder Joints?

The demand for a higher number of functions on a single chip requires the integration of an increased number of transistors or bits (memory cells) for each product generation. Typically, the number of pads and pins necessary to allow Input/Output (I/O) signals to flow to and from an integrated circuit increases as the number of transistors on a chip increases [14]. Future trends in flip chip pad pitch are shown in Figure 2.2.

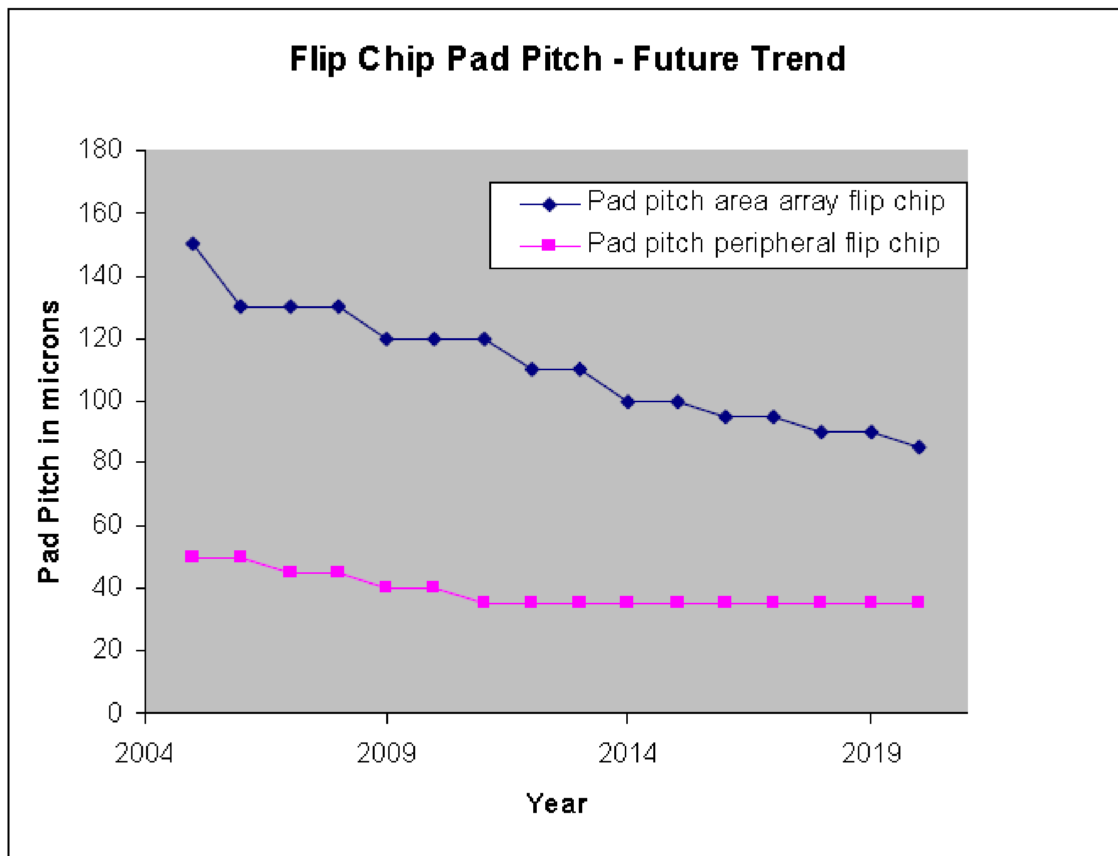


Figure 2.2: Flip Chip Pad Pitch – Future Trends

Electromigration in flip chip solder joints is of great concern in current and future products. Currently, each solder joint carries approximately 0.2 A which is likely to be doubled in the near future due to performance requirement. In addition, the diameter of the solder bump will be significantly reduced to approximately 50 um as compared to the current bump diameters in the range of 100 - 150 um. The number of I/Os can thus be increased by using smaller solder bumps with tighter pitches without increasing the package size, allowing for smaller and lighter products.

The current design rule of packaging requires that each bump must carry up to 0.2–0.4 A, resulting in a current density of approximately 10^4 A/cm^2. This current density is about two orders of magnitude smaller than that in Al and Cu interconnects.

Eutectic Sn/Pb and Pb-Free SAC alloys have a resistivity that is one order of magnitude larger than those of Al and Cu. The Young's modulus of eutectic Sn/Pb is ~ 30 GPa and that of lead free SAC alloy is ~ 20 GPa, which is 2–4 times smaller than Al ~69 GPa and Cu ~110 GPa. The effective charge number of solder is also about one order of magnitude larger than Al. It is clear that for solder joints in a flip chip package, current densities in the magnitude of 10^4 A/cm^2 can cause failures due to electromigration [29, 30]. Hence, electromigration in future flip chip packages should be considered as a serious reliability concern.

Another important characteristic of a flip chip solder bump is its unique geometry making it even more susceptible to electromigration induced failures. The electron flow through a solder bump is highly non-uniform. This non-uniform current distribution in a solder bump can be attributed to the transition in current densities at the interface between the metal line at the die side and the bump.

As shown in Figure 2.3, electrons flow through the Al traces and then enter into the solder bump at which interface the maximum current crowding occurs. This is because the current density in the Al traces will be 0.2 / (2 x 100) = 2 x 10^5 A/cm^2 whereas the current density in the solder bump will be 0.2 / (100 x 100) = 2 x 10^3 A/cm^2 based on the assumption that the Al

trace thickness and width are 2μm and 100 μm respectively and the interface window of solder bump is 100 μm x100 μm [32]. This clearly shows a significant change in current densities when the electrons enter the solder bump hence causing current crowding issues.

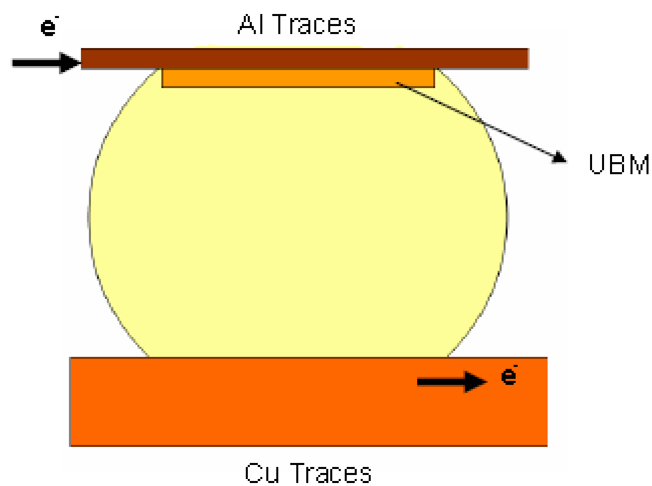


Figure 2.3: Electron Flow in Solder Bump

As the electrons flowing in the thin film wiring of an IC approaches the edge of solder bump, the electric field, E, rotates from horizontal to vertical, as shown in Figure 2.4. The electrons enter the solder bump at the via edge, creating a localized high current density called current crowding. Since the rate of electromigration damage is roughly proportional to the square of the current density, void nucleation will occur at the via edge. In these high current density areas void nucleation will occur due to the electromigration phenomena. The growing void blocks the primary current path, forcing the electrons to flow further along the conductor before entering the solder. Solder has fairly low thermal conductivity and, when used as solder bumps, it is poorly bonded, thermally, to the substrate. Thus, joule heating and thermal gradients are very important [31].

Since current density is inversely proportional to the cross sectional area, the push for reduced bump sizes will pose a reliability threat due to electromigration. Figure 2.5 shows that with a reduction in bump sizes, the current density increases significantly.

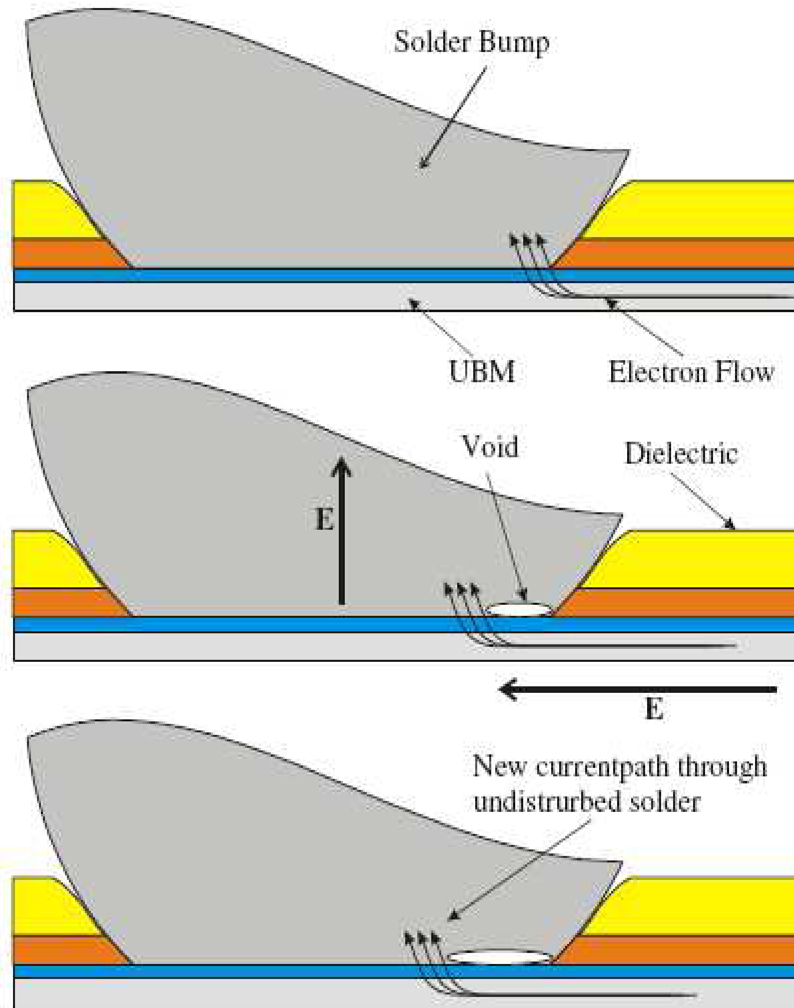


Figure 2.4: Current Flow Pattern [31]

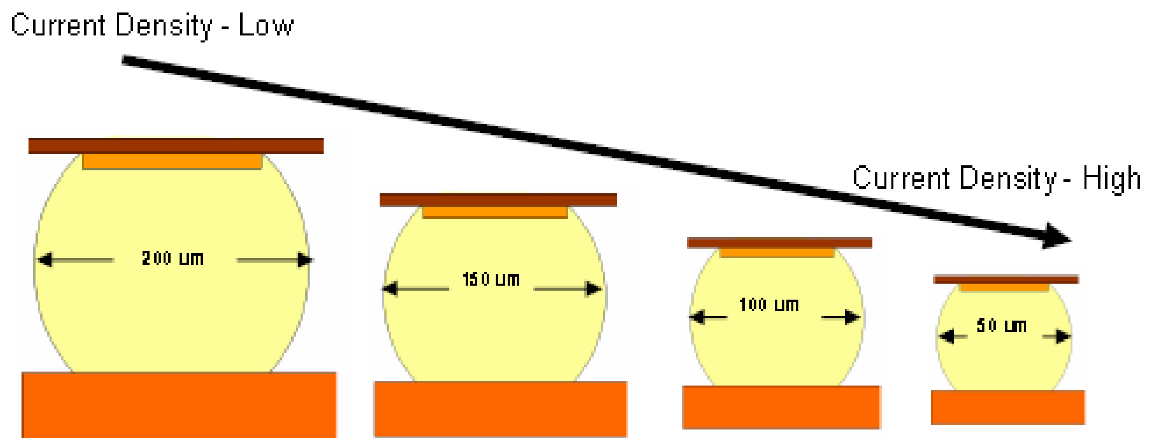


Figure 2.5: Current density as a function of bump size

Joule heating occurs due to an increase in temperature of a conducting body due to its resistance to electrical current flowing through it. Joule heating was named after James Prescott Joule who studied the Joule effect also named Joule's law in 1840. Joule's law is usually expressed as,

$$Q = I^2 R t$$

Where Q is the heat generated by a constant current I flowing through a conductor of electrical resistance R, for a time t. This heating effect of the conductors carrying electric current through them is called the Joule effect.

2.5 Problem and Objective

With the advent of 50-100 μm diameter solder bumps, the susceptibility to bump degradation will be greatly increased. One of the most important reliability concerns will be degradation due to electromigration. When a high current around 0.2-0.4A is passed through these smaller solder bumps, voids and intermetallic compounds (or IMCs) will be formed at a higher rate due to the electromigration phenomenon explained in the previous section.

The objective of this research was to study the distribution of current density in the solder bump for variety of back end design parameters. Parameters such as passivation opening (PO) diameter, trace width, under bump metallurgy (UBM) thickness and UBM diameter were studied in detail.

One of main concerns in electromigration testing is measuring the actual bump temperature since the parameter used in Black's equation is the bump temperature. The actual bump temperature in a flip chip package will always be greater than the oven temperature due to Joule heating which occurs due to an increase in temperature of a conducting body because of its resistance to electrical current flowing through it. The impact of Joule heating on the degradation of the bump has to be analyzed. Once the MTTF of the solder bump is calculated, the raw data is fitted to a distribution function and then the activation energy and current density exponent values are determined.

2.6 Summary

Scaling of microelectronics products due to the demand for smaller, lighter and more powerful components will see the emergence of high I/O, high-density, ultra-fine pitch flip chip devices in the near future.

Earlier, electromigration was not a reliability concern in flip chip products due to larger sized bumps and lower power applications. There will be a significant increase in current density in future products due to the demand for increasing power in the chip along with reduced bump sizes.

Hence, in the future, it is anticipated that electromigration will pose a serious reliability threat for flip chip products. The objective of this research was to study the distribution of current density in the solder bump for variety of back end design parameters. Parameters such as passivation opening (PO) diameter, trace width, under bump metallurgy (UBM) thickness and UBM diameter were studied in detail. Based on the results, a guideline for solder bump configuration is to be proposed.

CHAPTER 3

LITERATURE REVIEW

Since the beginning of this decade, there has been an increased concern for the reliability of micro-electronic packages. Primary reason for this has been the demand for smaller pitch devices along with harsh operating conditions (higher temperature, current, *etc.*). In a flip-chip package, as the current passes through different cross-sections and changes direction, a phenomenon called current crowding is observed. As a result of this, certain areas of the interconnect are subjected to high magnitude of current densities which result in a catastrophic (nucleation dominated) failure known as electromigration.

According to Black's equation [27, 28], the mean time to failure (MTTF) is given by,

$$MTTF = Aj^{-n}e^{(\frac{Q}{kT})}$$

where, A is a pre-exponential constant, j is the current density, Q is the activation energy, k is the Boltzmann constant, T is the temperature of the interconnect and n is constant. Based on the above equation, it can be said that failure rate exponentially depends on temperature and has power dependence on current density. Although parameters of concern are current density and temperature, it should be noted that ratio of current to cross-sectional area can only be called apparent current density. The actual current density will depend on current crowding.

Zhao [33] in his work has explained the impact of afore mentioned parameters on electromigration. He describes electromigration in interconnects as self-accelerated thermal runaway process. He mentions that, at early stage of electromigration, voids or cracks in the metallization are small when compared to the line width. As the crack propagates, cross-sectional area decreases causing local rise in current density. This phenomenon is known as current crowding, which in turn results in temperature rise due to Joule heating. The elevated

temperature accelerates the growth of cracks due to its exponential dependence which in turn further increases the current crowding effect, eventually leading to catastrophic failure.

Present trends in micro-electronics packaging shows that fine pitch devices have now become a package of choice. It can be seen that many applications have bump pitch between 100 μm and 500 μm [34-38]. This implies that devices will now have smaller bump diameter, stand off height (SOH), PO diameter, UBM diameter and trace width. Thus, optimization of these parameters to minimize the current density leading to electromigration is needed.

Agarwala *et al* [39] and Cho *et al* [40] showed effect of trace width on electromigration life time. In their work, they have also explained how grain size affects the dependence of electromigration life time on trace width.

More recently significant effort was concentrated on effect of bump technology on bump electromigration in industry [41]. In patents issued in 2004 and 2006, Pekin *et al* [42] claimed the trace designs that minimize current crowding and bond out methodology for using those traces.

Yiping *et al* [43] studied the effect of different Ni/Au UBM thickness on electromigration in Sn/3.5Ag/0.5Cu solder bumps. UBM consisted of electroplated nickel (5/10 μm) on copper as diffusion barrier layer and gold (0.1 μm) on the surface as an anti-oxidization layer and concluded that MTTF for UBM with 10 μm thickness is longer than that of UBM with 5 μm thickness.

Liang *et al* [44] studied effect of 5 μm, 10 μm and 20 μm thick copper UBM on the current density distribution for the Sn63Pb37 solder joint. They used 3D Finite Element Analysis (FEA) for their analysis. Based on their modeling results, they concluded that solder joints with thicker Cu UBM has lower current density inside the solder.

Lai *et al* [45] studied effect of current crowding for four different flip-chip assemblies. Their study included parameters such as passivation opening, UBM diameter, bump diameter and Cu pad diameter. They concluded that current crowding is due to the geometry of the structure and is independent of magnitude of applied current. In another study,

Lai *et al* [46] tested 96.5Sn3Ag0.5Cu solder with T/Ni(V)/Cu UBM on copper and Au/Ni/Cu substrate surface finish and reported that copper surface finish offers better

electromigration resistance then the Au/Ni/Cu one, although more voids are created in copper metallization. In their study, they applied a constant electric current of 0.32 A, which resulted in an average current density of about 5,000 A/cm^2, considering the area of passivation opening to be 90 μm^2 as a reference. It should be noted that this is the apparent current density.

Su *et al* [47] tested Sn10Pb90 (high lead) and Sn96.5Ag3.5 (Pb-free) solders with TiW/Cu and Ti/Cu/Ni UBM under 3.5- 4.1 x 10^4 A/cm^2 current density. The current density was calculated as a ratio of applied current (0.85-1 A) to the area of via opening (2.42×10^{-5} cm^2). Thus, this is also apparent current density. They concluded that electromigration performance can be increased by increasing the UBM thickness or reducing the current crowding near the UBM.

Chiu *et al* [48] studied the effect of Al trace dimension on electromigration lifetime. They concluded that Al trace dimensions play a crucial role in determining electromigration lifetime. Longer and wider Al traces exhibit better resistance to electromigration.

Master *et al* [49] studied the effect of bump pitch on bump electromigration for organic and ceramic packages. Their study included bump pitch of 225 μm, 200 μm and 150 μm. They concluded that ceramic package showed better resistance to failure than organic packages. Also, electromigration was significant with pitch less than 200 μm.

Mistry *et al* [50] studied effect of different passivation and polyimide structures on bump stresses. They showed that bond pads with large PO are more reliable.

Nah J-W *et al* [51] considered SnPb and SnAg solder with copper column and concluded that copper column increases the electromigration resistance by decreasing the current crowding in the solder and that the copper column bump with SnPb eutectic has lower reliability.

After reviewing the literature it can be seen that, no clear guidelines exist which will assist design engineers in deciding bump dimensions that will result in minimum current density. Most common conclusion was regarding the positive effect of UBM thickness on electromigration. To the best of our knowledge, it was noted that most of the researchers have studied effect of different bump parameters on electromigration independently. However, all the parameters play a

significant role in determining the MTTF due to electromigration, and their combined effect should be considered.

CHAPTER 4

DESIGN OF EXPERIMENTS

Design of Experiment (DOE) is a structured, organized method that is used to determine the relationship between the different factors affecting a process and the output of that process. This method was first developed in the 1920s and 1930, by *Sir Ronald A. Fisher,* the renowned mathematician and geneticist [52].

Design of Experiment involves designing a set of experiments, in which all relevant factors are varied systematically. When the results of these experiments are analyzed, they help to identify optimal conditions, the factors that most influence the results, and those that do not, as well as details such as the existence of interactions and synergies between factors.

4.1 Full Factorial Design of Experiments:

A full factorial design of experiments (DOE) was employed to study the effect of back end design rules on current crowding which was demonstrated by using 3D modeling based on FEA.

Four parameters of the back end design rules, each with two values were studied. These attributes and their ranges were

- Passivation Opening (PO) diameter with 60 and 100 μm
- Under Bump Metallurgy (UBM) diameter with 120 and 160 μm
- Under Bump Metallurgy (UBM) thickness with 2 and 7 μm
- Aluminum trace width with 10 and 60 μm

The full factorial design of experiments consists of 16 different cases (or legs) consisting various combination of the 4 different parameters. Table 4.1 shows a full factorial design of experiments.

Table 4.1: Full Factorial Design of Experiments

Leg #	Passivation Opening	UBM Size	UBM Thickness	Trace Width
1	60	120	2	10
2	60	120	2	60
3	60	120	7	10
4	60	120	7	60
5	60	160	2	10
6	60	160	2	60
7	60	160	7	10
8	60	160	7	60
9	100	120	2	10
10	100	120	2	60
11	100	120	7	10
12	100	120	7	60
13	100	160	2	10
14	100	160	2	60
15	100	160	7	10
16	100	160	7	60

CHAPTER 5

MODELING METHODOLOGY

5.1 Modeling in Pro/Engineer® WildFire™ 3.0

Modeling was done using Pro/Engineer® WildFire™ 3.0 [52] and analysis was done in Ansys® 10.0. Figure 5.1 shows the schematic of the solder bump pair considered for analysis. The metal traces on the chip side and substrate side are considered to be made up of Al and Cu respectively. The UBM is comprised of Cu, Ni and Ti metal layers. Thickness of Cu, Ni and Ti metal layers are 1.08, 0.4 and 0.52 μm respectively.

The solder bump configuration considered is $SnAg_3Cu_{0.5}$. A thin layer of Ni which acts as a barrier layer for electromigration is considered between the bump and Cu trace.

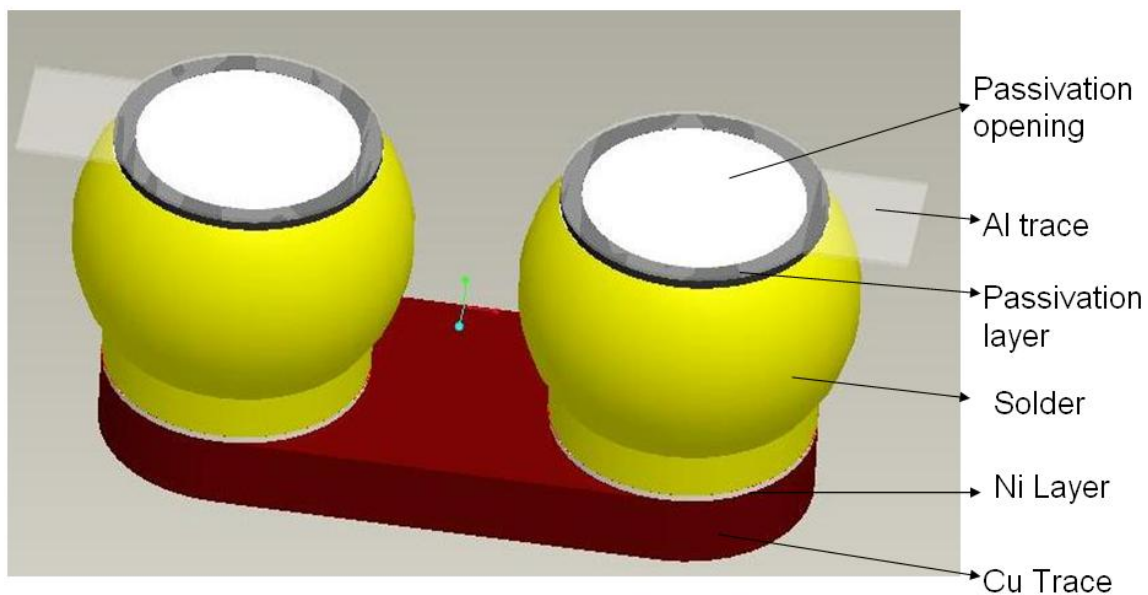


Figure 5.1: Schematic representation of solder bump

Thickness of passivation layer, Ni layer, Al trace and Cu trace was kept constant for all the cases. The dimensions were 8 μm, 5 μm, 2 μm and 32 μm respectively. Dimensions of all other parameters are shown in figure 5.2. The schematic representation of the UBM structure is shown in figure 5.3. Figure 5.4 shows the schematic representation of the model when the UBM diameter is 160 microns.

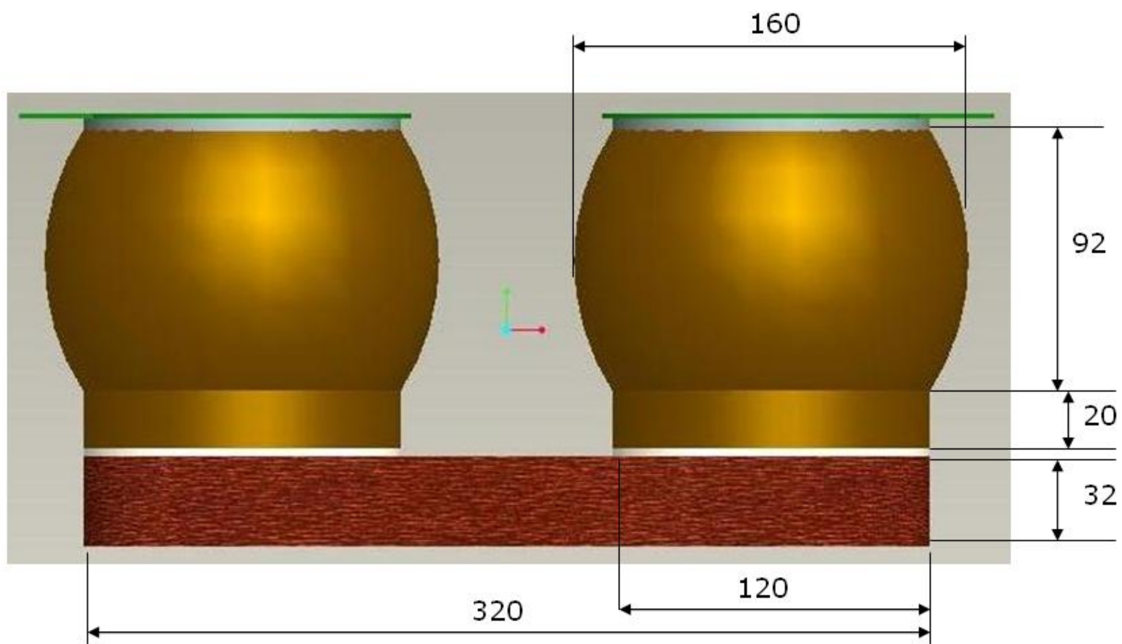


Figure 5.2: Dimensions of each parameter considered for analysis *(All dimensions in microns)*

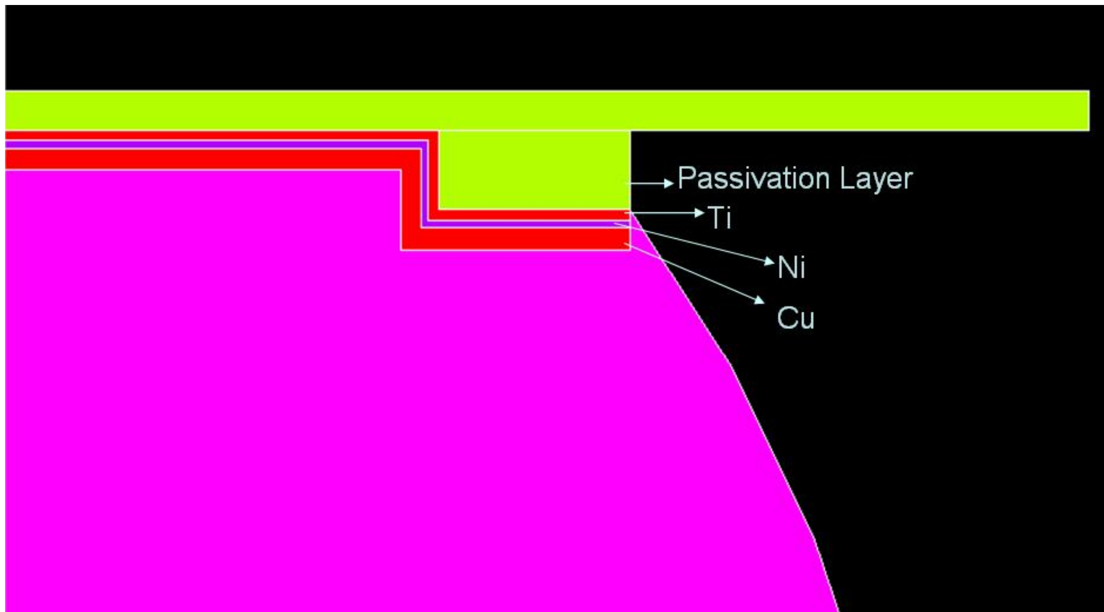


Figure 5.3: Part of the solder bump showing the UBM structure

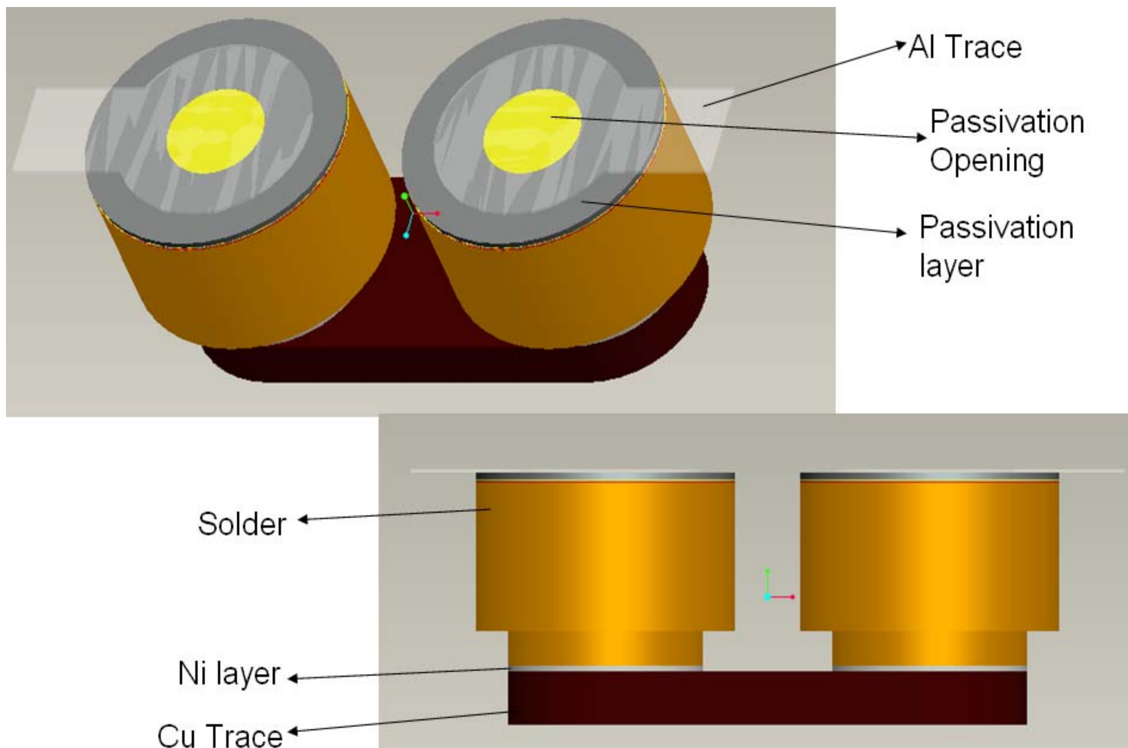


Figure 5.4: Schematic Representation of the Model for UBM diameter of 160 micron

5.2 Simulation in Ansys® 10.0

Numerical analysis was performed using ANSYS [53]. SOLID 69 element was considered owing to its ability to do electro-thermal coupled analysis. The model was meshed in order to generate approximately 122,000 elements. Analysis was performed for input currents of 0.1 A and 0.5 A. The current was defined on one of the Al trace while zero voltage was defined on the other Al trace. A constant temperature boundary condition was defined at the bottom of the Cu trace. Material properties considered for analysis are as shown in table 5.1 [55].

Table 5.1: Material properties considered for analysis

Material	Electrical resistivity x10-8 (Ω-m)	Thermal conductivity (W/m K)
Aluminum	2.7	210
Copper	1.7	385
SnAg(3.0)Cu(0.5)	12.1	57.26
Titanium	55.4	17
Nickel	6.4	60.7

CHAPTER 6

RESULTS AND DISCUSSION

Effect of Al trace thickness, UBM thickness, UBM diameter and PO diameter on current density in both Al trace and the solder bump are studied. It has been stated that electromigration is also impacted by the stress present in the bump [56]. It is also known that stress in the bump depends on its location in the bump array [57]. Effects of stress for bumps with small and large PO diameter are studied.

A full factorial DOE matrix along with the results is shown in table 6.1. The maximum temperature and the maximum current density for each leg are tabulated in table 6.1. The maximum global temperature is found to be at the entrance of the Al trace where the current is applied. The maximum global current density is found to be in the Al trace.

6.1 Effect of different parameters on current density in Al trace

Figures 6.1 and 6.2 show the variability chart for maximum current density in the Al trace for an input current of 0.1 A and 0.5 A respectively. In Al trace, when the current was increased from 0.1 A to 0.5 A, the maximum current density also increased by a factor of five. Al trace width, PO diameter and UBM diameter were found to have significant contribution in deciding the current density in Al trace. However, the variation in current density with respect to UBM thickness was insignificant.

Figures 6.3 and 6.4 show the vector plot of current density for leg 1 (passivation opening of 60 μm, UBM size of 120 μm, UBM thickness of 2 μm and trace width of 10 μm) and leg 2 (passivation opening of 60 μm, UBM size of 120 μm, UBM thickness of 2 μm and trace width of 60 μm), respectively. The effect of Al trace width on current density in metallization can be seen from figs. 6.3 and 6.4. It is observed that as Al trace width increases, the maximum current density decreases. This agrees with the result reported by Chiu *et al* [48].

Table 6.1: Full Factorial DOE with the results

Leg #	Pad Size	Passivation Opening	UBM Size	UBM Thickness	Trace Width	Current 0.1 amp, Voltage 1 volt		0.2amp, 2 volts		0.3 amps, 3 volts		0.4 amps, 4 volts		0.5 amps, 5 volts	
						Temp	current density	Temp	current density	Temp	current density	Temp	current density	Temp	current density
1	120	60	120	2	10	127.169	65.48 x E4	133.677	131 x E4	144.522	196 x E4	159.706	262 x E4	179.229	327 x E4
2	120	60	120	2	60	127.039	51.86 x E4	133.156	104 x E4	143.351	156 x E4	157.624	207 x E4	175.975	259 x E4
3	120	60	120	7	10	127.17	65.11 x E4	133.679	130 x E4	144.528	195 x E4	159.716	260 x E4	179.244	326 x E4
4	120	60	120	7	60	127.042	50.62 x E4	133.168	101 x E4	143.377	152 x E4	157.67	203 x E4	176.047	253 x E4
5	120	60	160	2	10	127.117	67 x E4							177.916	335 x E4
6	120	60	160	2	60	126.971	56 x E4							174.273	284 x E4
7	120	60	160	7	10	127.111	66.78 x E4							177.786	334 x E4
8	120	60	160	7	60	126.994	55.55 x E4							173.593	278 x E4
9	120	100	120	2	10	127.162	66.75 x E4	133.647	134 x E4	144.455	200 x E4	159.586	267 x E4	179.041	334 x E4
10	120	100	120	2	60	127.032	54.23 x E4	133.128	108 x E4	143.288	163 x E4	157.512	217 x E4	175.799	271 x E4
11	120	100	120	7	10	127.16	66.2 x E4	133.639	132 x E4	144.438	199 x E4	159.556	265 x E4	178.993	331 x E4
12	120	100	120	7	60	127.026	54.65 x E4	133.103	109 x E4	143.233	164 x E4	157.414	219 x E4	175.646	273 x E4
13	120	100	160	2	10	127.14	71.2 x E4							178.498	356 x E4
14	120	100	160	2	60	127	58.18 x E4							175.201	291 x E4
15	120	100	160	7	10	127.131	70.78 x E4							178.265	354 x E4
16	120	100	160	7	60	126.989	58.83 x E4							174.733	294 x E4

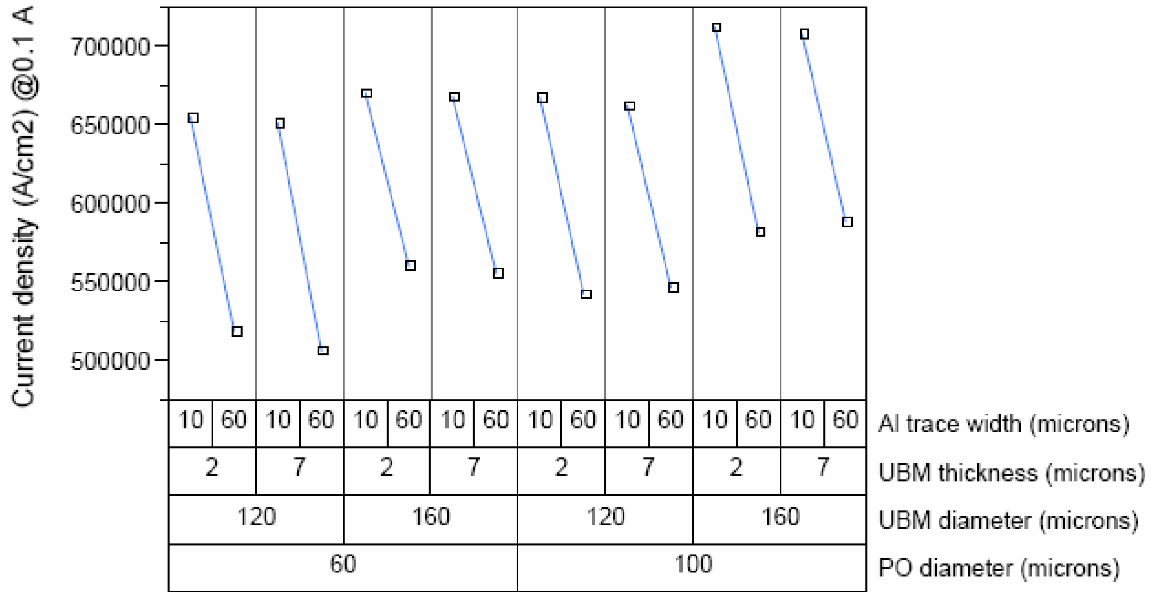


Figure 6.1: Variability chart for maximum current density at 0.1 A in Al trace width

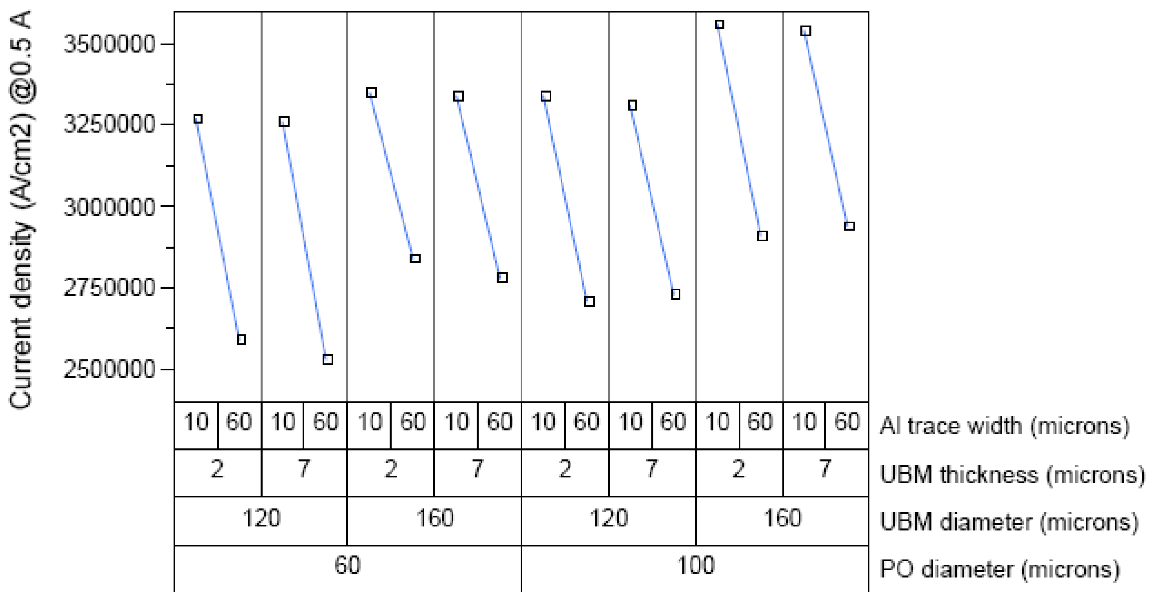
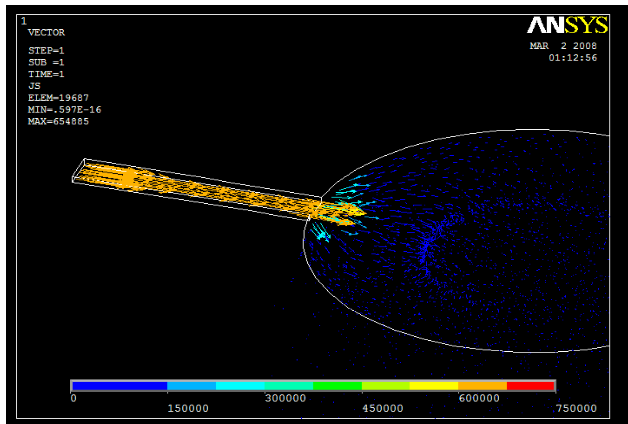


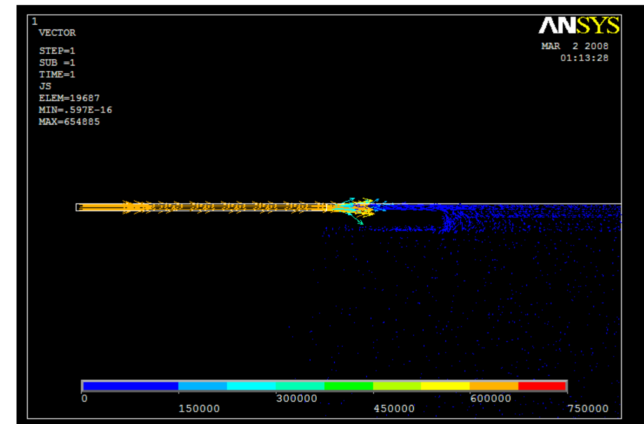
Figure 6.2: Variability chart for maximum current density at 0.5 A in Al trace width

Figure 6.3 shows that for narrow trace width, the current density is uniform in the Al trace. However, current density in the Al trace is approximately twice of that observed in the pads or UBM opening. Thus there is a very large change in current density at the junction of Al trace and the UBM. This sudden change results in current crowding which enhances void formation and may reduce the life of the solder bump. This current crowding effect can be reduced by increasing the Al trace width. Thus, when the Al trace width is increased from 10 μm to 60 μm, there is a gradual change in current density at the interface of Al trace and UBM. This phenomenon is clearly observed in figure 6.4. As mentioned earlier variation in current density is insignificant when the UBM thickness was changed from 2 μm to 7 μm. This can be observed in figure 6.1.

For solder bumps with higher PO diameter (100 μm) and UBM diameter (160 μm), higher current density is observed when compared to other bump configurations. This is because when the passivation opening is bigger and in this case is of the same size as that of voltage pad, the current directly passes into the UBM and does not spread in the pads as seen in other cases. This phenomenon can be clearly seen in figs. 6.5 and 6.6. Thus, smaller UBM diameter and PO diameter yield lower current density. However, it is recommended to have larger PO diameter in order to reduce stress on the bump during fabrication and reflow process [50]. In our study, we have not considered effect of stress on the current density in Al trace as well as in the bump. Similar trends were observed for input current of 0.1 A and 0.5 A, as seen in figures 6.1 and 6.2.



(a)



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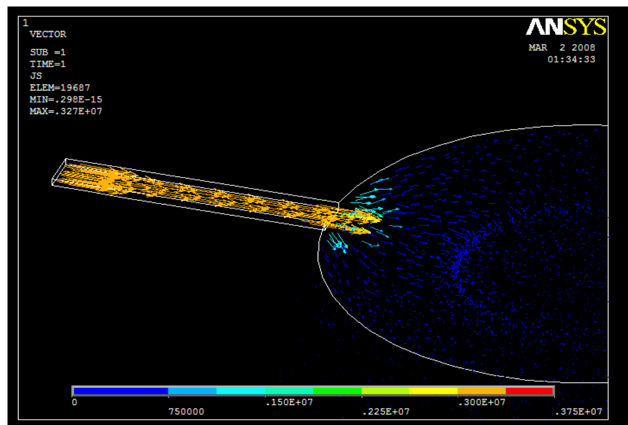

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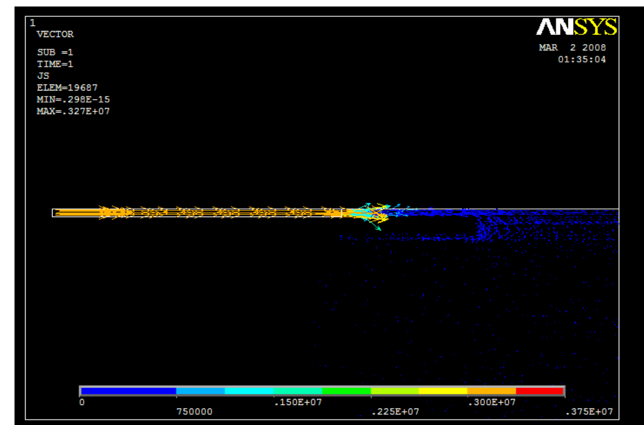
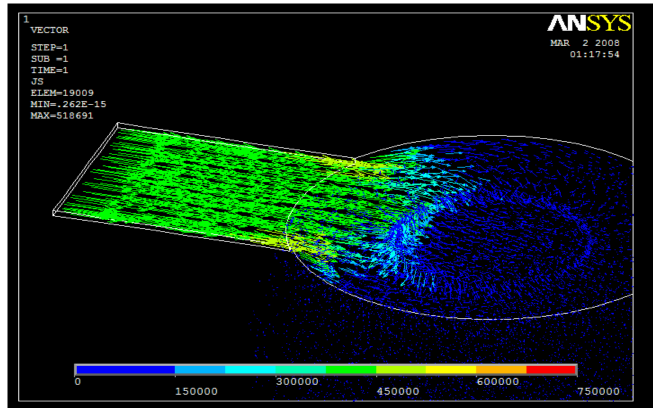
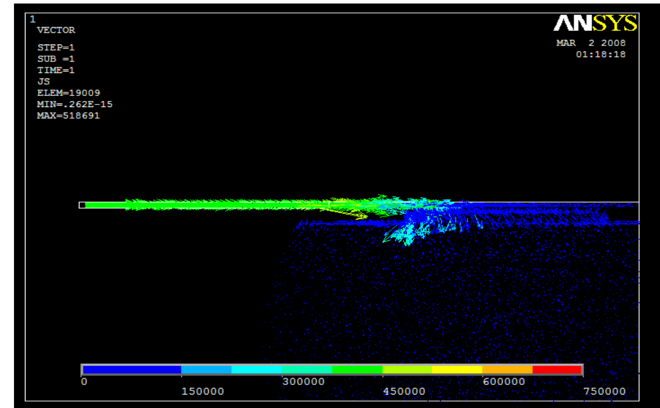


(d)

Figure 6.3: Vector plots of current density for an input current of 0.1 A and 0.5 A for leg 1 (a) 3D view of current density for input current of 0.1 A (b) 2D view of current density for input current of 0.1 A (c) 3D view of current density for input current of 0.5 A (d) 2D view of current density for input current of 0.5 A



(a)



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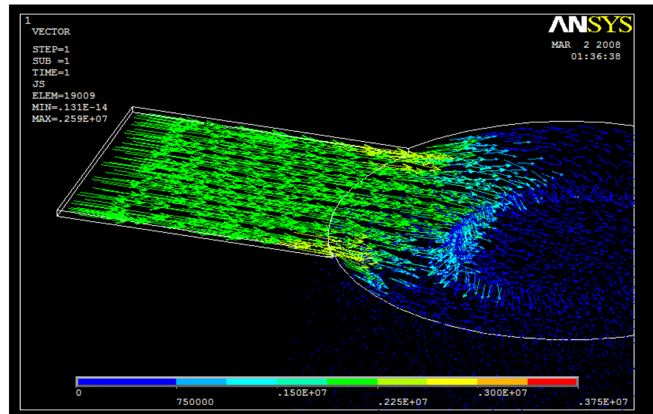

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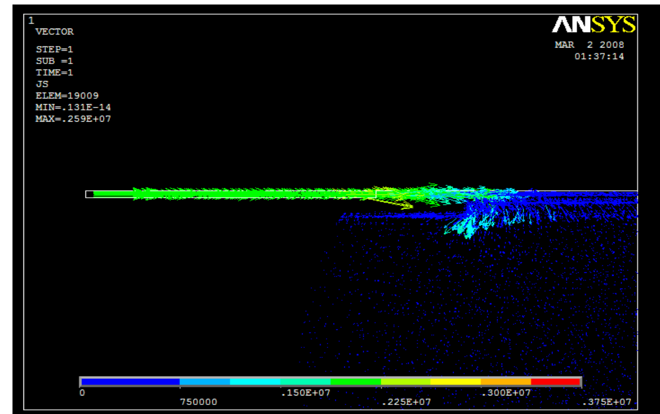
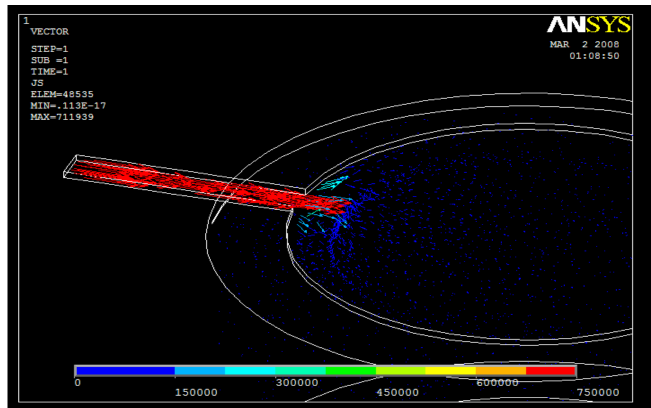
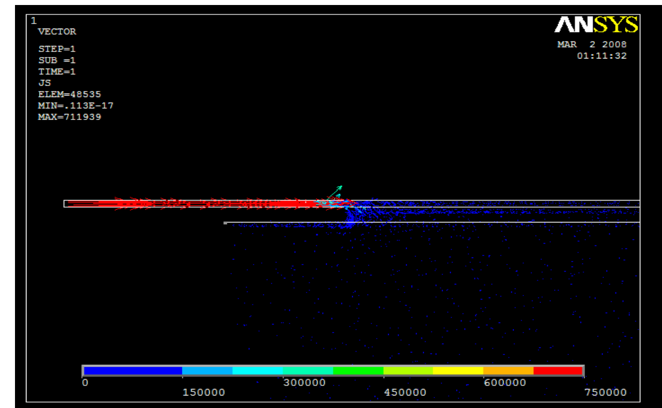


(d)

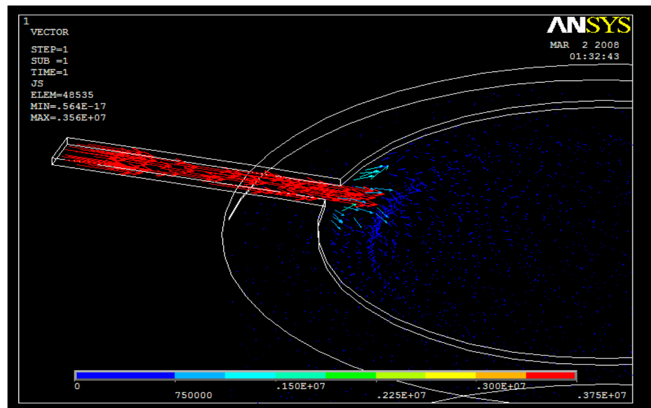
Figure 6.4: Vector plots of current density for an input current of 0.1 A and 0.5 A for leg 2 (a) 3D view of current density for input current of 0.1 A (b) 2D view of current density for input current of 0.1 A (c) 3D view of current density for input current of 0.5 A (d) 2D view of current density for input current of 0.5 A



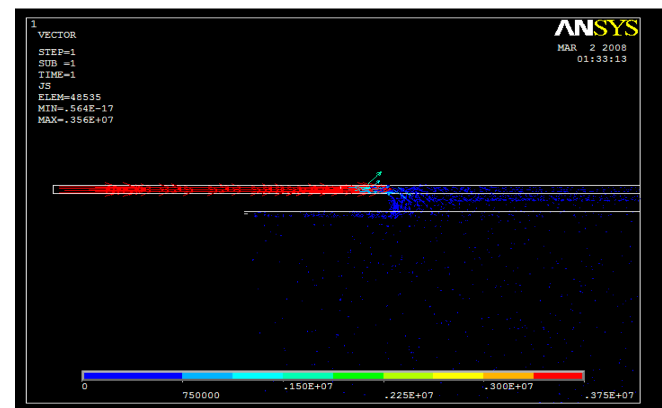
(a)



(b)

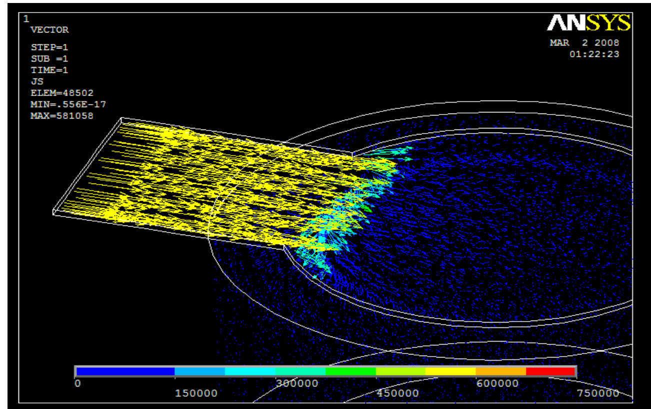


(c)

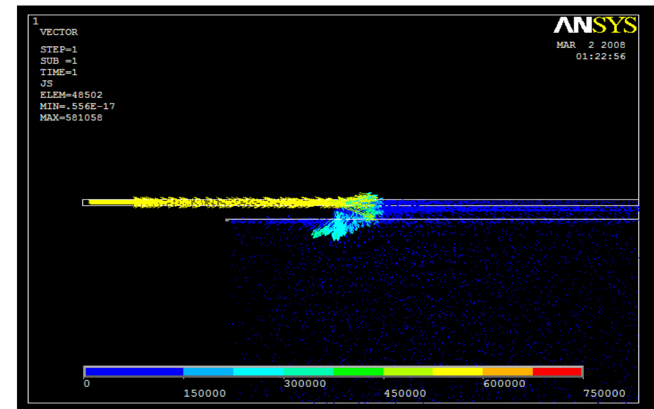


(d)

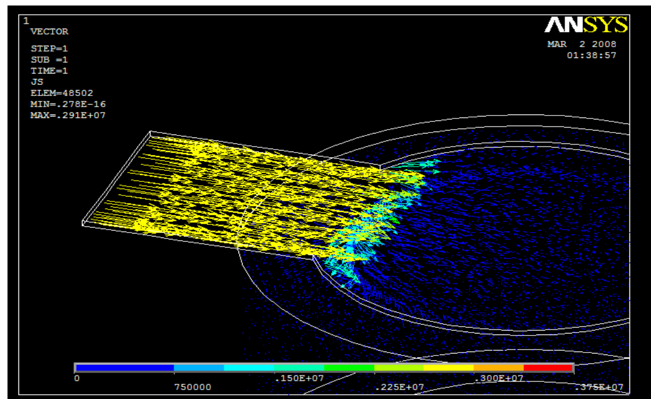
Figure 6.5: Vector plots of current density for an input current of 0.1 A and 0.5 A for leg 13 (a) 3D view of current density for input current of 0.1 A (b) 2D view of current density for input current of 0.1 A (c) 3D view of current density for input current of 0.5 A (d) 2D view of current density for input current of 0.5 A



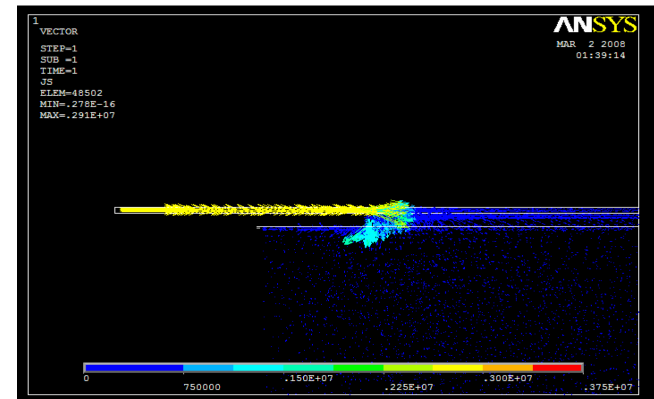
(a)



(b)



(c)



(d)

Figure 6.6: Vector plots of current density for an input current of 0.1 A and 0.5 A for leg 14 (a) 3D view of current density for input current of 0.1 A (b) 2D view of current density for input current of 0.1 A (c) 3D view of current density for input current of 0.5 A (d) 2d view of current density for input current of 0.5 A

6.1.1 Summary of factors contributing the current density in Al Trace

The importance of each factor is shown in figure 6.7, where it is clear that trace width, UBM size, and passivation opening are the most important factors for the current density and hence failure due to electromigration respectively. UBM thickness is the least important of the four factors studied.

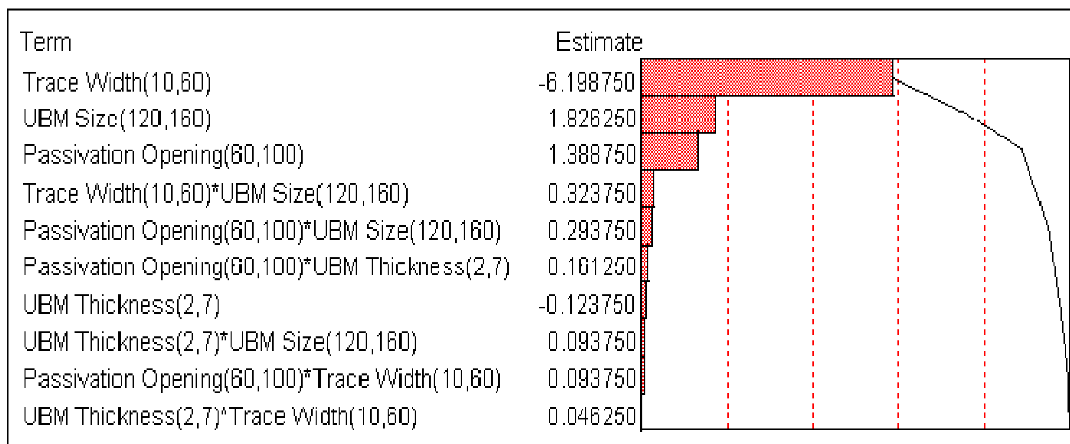


Figure 6.7: Important factors contributing the current density in Al Trace

6.2 Effect of different parameters on current density in Solder Bump

The results obtained for various simulation cases are discussed below.

Figures 6.8 and 6.9 show the variability chart for maximum current density in the solder bump for an input current of 0.1 A and 0.5 A respectively. Similar to Al trace width, in case of bump, when the current was increased from 0.1 A to 0.5 A, the maximum current density also increased by a factor of five. However, current density in solder bump was noted to be significantly less than current density in Al trace. This is due to the large volume of the bump compared to that of Al trace. Al trace width and UBM thickness were found to have significant contribution in deciding the current density in the bump. Variation in current density with respect to PO diameter and UBM diameter was insignificant.

Figures 6.8 and 6.9 show the effect of Al trace width on maximum current density in the bump. It is observed that current density in the bump increased with increase in Al trace width. This contradicts with the findings reported by Chiu *et al* [48]. However, their conclusion was based on Joule heating effect in Al trace. In the present study, for wider Al trace, a zone of crowded current is observed in the solder. This can be clearly seen in fig. 6.4 and 6.6.

Change in UBM thickness from 2 μm to 7 μm lowers the current density in the bump. This agrees with the result reported by Liang *et al* [44] and Su *et al* [47]. As mentioned earlier, variation in current density with respect to PO diameter and UBM diameter is insignificant.

Similar trends were observed for input current of 0.1 A and 0.5 A., as seen in figures 6.8 and 6.9.

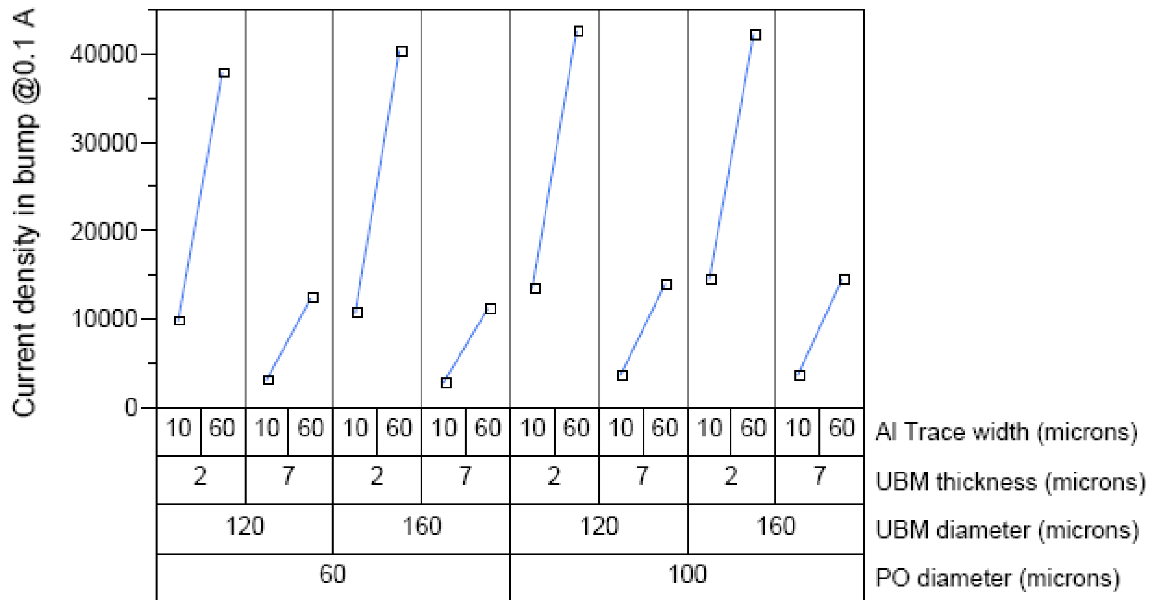


Figure 6.8: Variability chart for maximum current density in solder bump for input current of 0.1 A

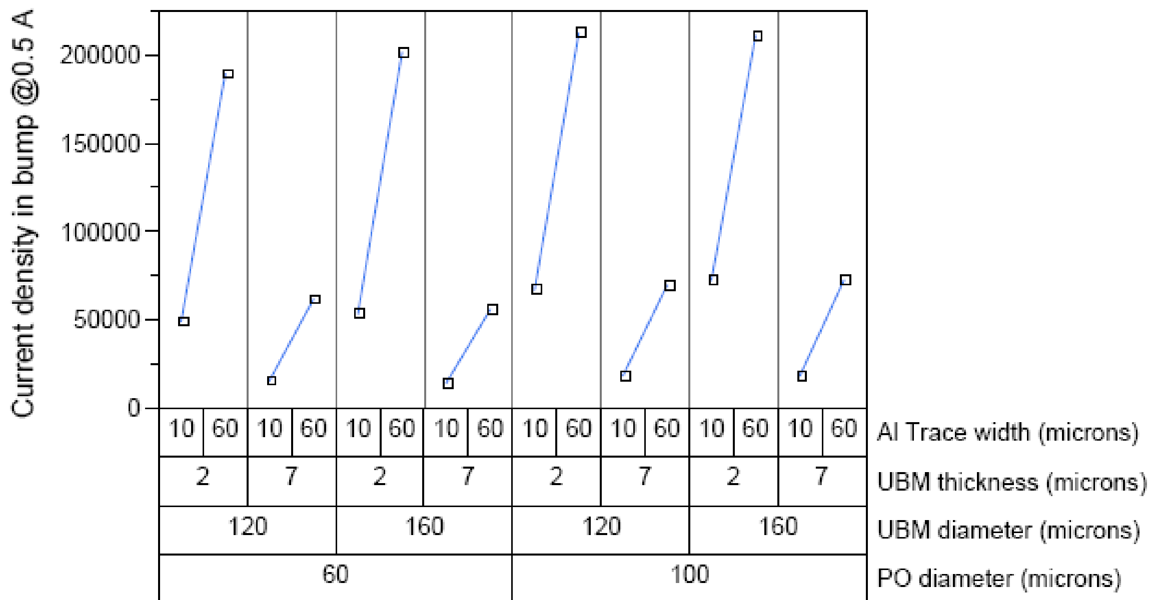


Figure 6.9: Variability chart for maximum current density in solder bump for input current of 0.5 A

6.3 Effect of stress on passivation opening (PO)

It has been stated that electromigration is also impacted by the stress present in the bump [56]. It is also known that stress in the bump depends on its location in the bump array [57].

Thus, results shown above may be affected by the stress acting on the bump and hence it is necessary to consider effect of stress within the PO. Figs. 6.10 and 6.11 show the stress state for bump configuration of legs 1 (PO of 60 μm) and 9 (PO of 100 μm) under the same tensile loading. Bumps with small PO diameter show higher stress levels. Also, maximum stress is noted at the same location where current crowding occurs. This will impact MTTF and experimental results may deviate from the results shown earlier.

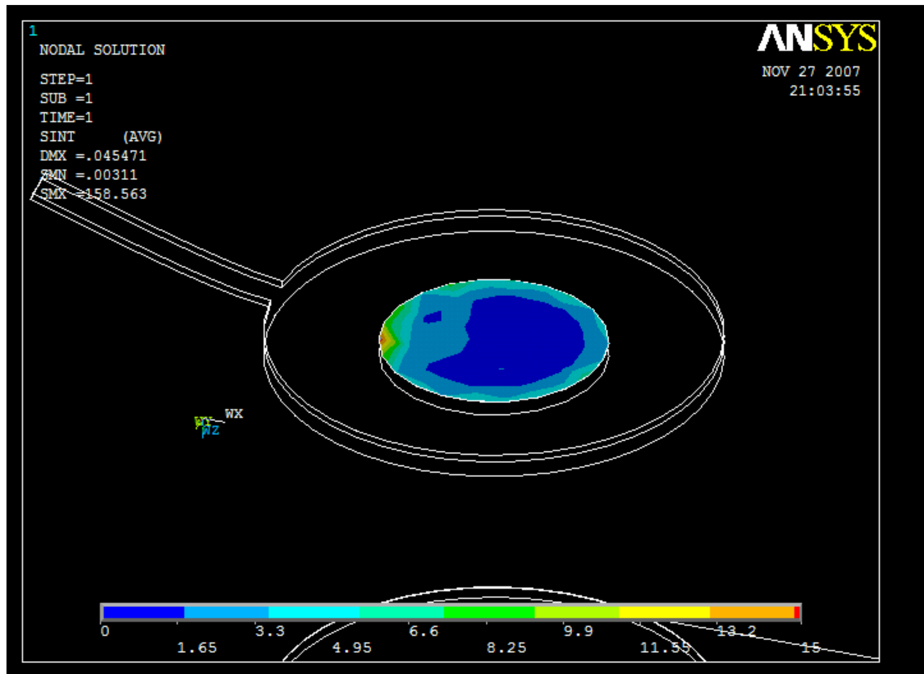


Figure 6.10: Stress plot for small PO diameter (leg 1)

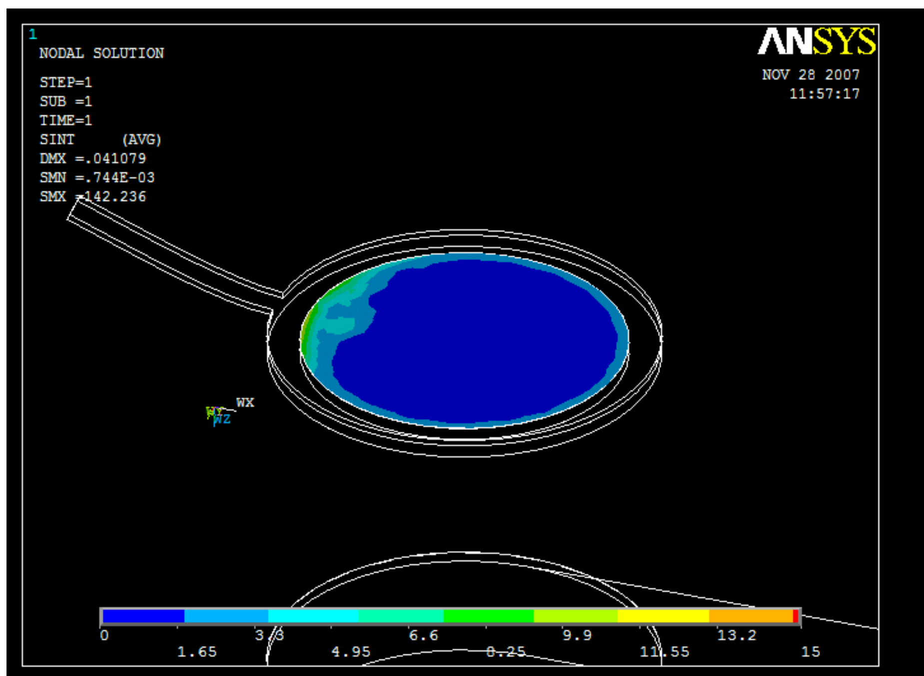


Figure 6.11: Stress plot for large PO diameter (leg 9)

6.4 Conclusion

In this research, an effort is made to determine the importance of different parameters which will affect the reliability of solder bump due to electromigration. A full factorial DOE was developed and effect of each parameter was studied. Based on the results it was observed that the Dimensions of trace width largely determines the maximum current density and hence the temperature.

The effect of Al trace thickness, UBM thickness, UBM diameter and PO diameter on current density in Al trace and the bump is studied. Maximum current crowding is always observed in the metallization. In the metallization, the most important design attribute found is the Al trace width. In the solder bump, the most important parameters found are Al trace width and UBM thickness. Solder configuration with Al trace of 60 µm, UBM thickness of 7 µm, UBM diameter of 120 µm and PO diameter of 60 µm yielded minimum current density in Al trace. Whereas, solder configuration with Al trace of 10 µm, UBM thickness of 7 µm, UBM diameter of 120 µm and PO diameter of 60 µm yielded minimum current density in bump. However, it is also shown that bumps with small PO diameter will be subjected to higher stresses.

In general, larger trace width and UBM thickness while smaller UBM diameter and PO diameter yields minimum current density.

6.5 Scope of Future Study

In future studies, incorporating the stress and Joule heating into the model should be considered. Both stress and joule heating should be coupled together in order to get the exact results with which we can reduce the Electromigration phenomenon.

Other study would be the optimization of the results to reduce the Bump Electromigration. Also, the experimental validation of the parametric analysis presented in the current thesis will provide an insight into the accuracy of the simulation carried out.

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