EXPERIMENTAL/COMPUTATIONAL ANALYSIS OF ACTIVE COOLING OF STACKED DEVICE USING MULTIDIMENSIONAL CONFIGURED THERMOELECTRIC MODULES

By

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ABSTRACT

EXPERIMENTAL/COMPUTATIONAL ANALYSIS OF ACTIVE COOLING OF STACKED DEVICE USING MULTIDIMENSIONAL CONFIGURED THERMOELECTRIC MODULES

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Stacked devices are currently used widely because of their smaller footprint and corresponding ability to accommodate heterogeneous devices such as memory and logic and enable a silicon efficiency greater than 100%. This configuration will results in thermal management challenges due to the torturous heat dissipation path. In addition, the non-uniformity in chip power distribution results in an increased spreading resistance as well as temperature gradient at the device level that can degrade performance and reliability. In this study the Thermoelectric Modules were configured in a multidimensional form surrounding a three dimensional cold core. The corresponding Computational Fluid Dynamics model is validated using the experimental data.

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NOMENCLATURE

COP	Coefficient of Performance
TEC	Thermoelectric Cooler or module
CFD	Computational Fluid Dynamics
3D-IC	Three Dimensional Integrated Circuit
MHTS	Multi-Dimensional Heat Transfer System
R	Electric Resistivity
I	Current
L	Length
A	Cross-sectional Area
α	Seebeck effect
k	Thermal Conductivity
T_c	Cold Side Temperature
T_h	Hot Side Temperature
ΔT	Temperature difference
TE	Thermoelectric Pallet

CHAPTER 1

INTRODUCTION

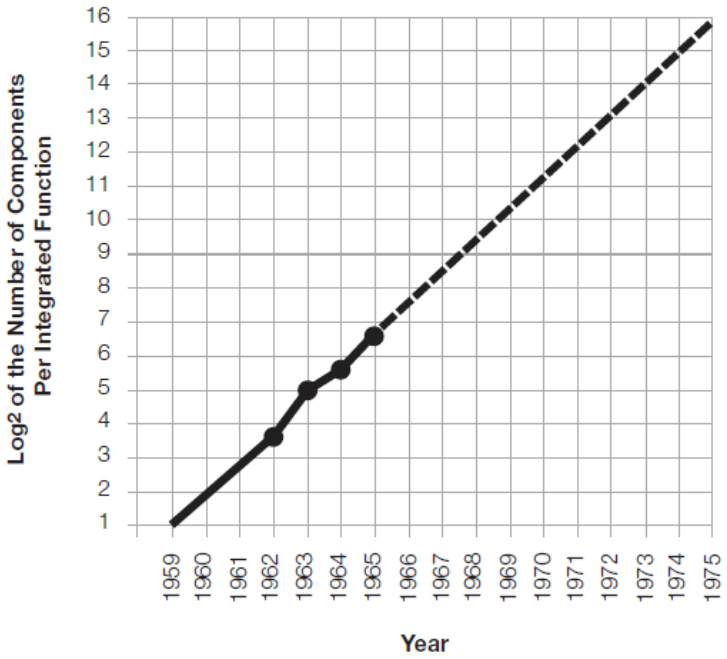

Figure 1.1 Moore's Law Prediction from Year 1959 to 1075

According to Moore's law [5], performance of micro-processor doubles every two years. With improvement in performance the size of stacked devices has shrink significantly. As a result, the issue of thermal management arises. The high non-uniform power density distribution in stacked device creates localized hot spot. This in long run can leads to material degradation which reduces the performance and affects the reliability of the stacked device and then finally leads to device failure. Methods of cooling used normally are force or natural convection (passive cooling) with the help of heat sink, phase change cooling can only bring the temperature of stacked device to room temperature. Also, it can be proved as non-reliable

source of cooling with increase in performance which in long run will affect its reliability [2]. The most conventional method used is heat sink with or without fan where the heat sink is in direct contact with stacked device with the help of thermal grease or clamps. The main disadvantage of this method is that only the surface of IC is cooled down, leaving hotspots inside the chip. Again, this also has issues regarding the volume, weight and more area required for heat transfer.

The sub-ambient cooling methods in form of refrigeration cooling or Nano-fluid cooling and solid state devices like thermoelectric or thermal diode give the advantage of high chip performance at low junction operating temperature. It was able to maintain low junction temperature when high heat flux is dissipated from stacked device with reduction in junction leakage [2]. This leads to more power saving than consumed which indirectly increases the reliability in the stacked device [3]. But, this technology is little costlier than conventional method. In mid-1990s, IBM used KryoTech super G computer used vapor compression refrigeration cooling system for cooling to sub-ambient condition. Along with the advantage of sub ambient cooling, their main disadvantage is moisture condensation on exposed surface when temperature goes below dew point of surrounding point. Thus, all exposed surfaces needs to be insulated [2]. For cooling, refrigerant like CFC is needed which is not environmentally friendly. The size and weight of the refrigeration cooling system creates problem for its placement in a system as it requires more space. Also, due to many parts, increase in chance of individual parts maintenance is seen which reduces Reliability of the system.

While, the solid state devices like TEC is non-directional giving freedom to place in any direction. Thus, it can cool the chip without requiring more space for its placement. Also, it is reliable because it has no moving parts, making it work it work for 100,000 hours in steady state operation even in harsh conditions[4].It does not require any working fluid, so there is no fear for

leakage. Even though it has COP of around 0.25 to 0.4, it can efficiently bring chip temperature in sub-ambient condition [4].

Here, the Multi-Dimensional Heat Transfer System (MHTS) proposed by Phan and Agonafer [1] is studied to understand cooling efficiency of thermoelectric module and reduce the temperature of devices at chip level to a sub-ambient value. The numerical model was setup along with an experimental model for its validation. A cold core is used similar to the previous configuration to and multiple heat sinks are added to increase the fin area for improved heat dissipation. As a result more uniform heat transfer can take place between the thermoelectric modules and stacked device reducing the risk of creating hot spots in the chip. The thermoelectric are placed vertically to make sure that there is no violation of space allocated to chip on the motherboard.

CHAPTER 2

THERMOELECTRIC MODULE

In 1834, Jean Peltier, discovered the thermoelectric cooling effect, named after him as Peltier cooling effect. He found out that passing current through a junction of two dissimilar materials causes a temperature difference. Thermoelectric cooler (TEC), or Peltier Cooler is a solid-state heat pump that uses the Peltier Effect to move heat. As seen in figure 2.1 it consists of two ceramic plates, which act as the hot and cold sides of the module, and has superior thermal conductivity and electrical insulation as compared to metals. Multiple p and n type semiconductor legs are paired together to make TE pallets which are connected in series electrically and in parallel thermally. These paired legs are sandwiched between the two ceramics plates. By changing the polarity of D.C. current, the direction of heat pump can be switched and can work as a cooler as well as a heater. This thermoelectric technology has many applications in aerospace, military as well as consumer industry.

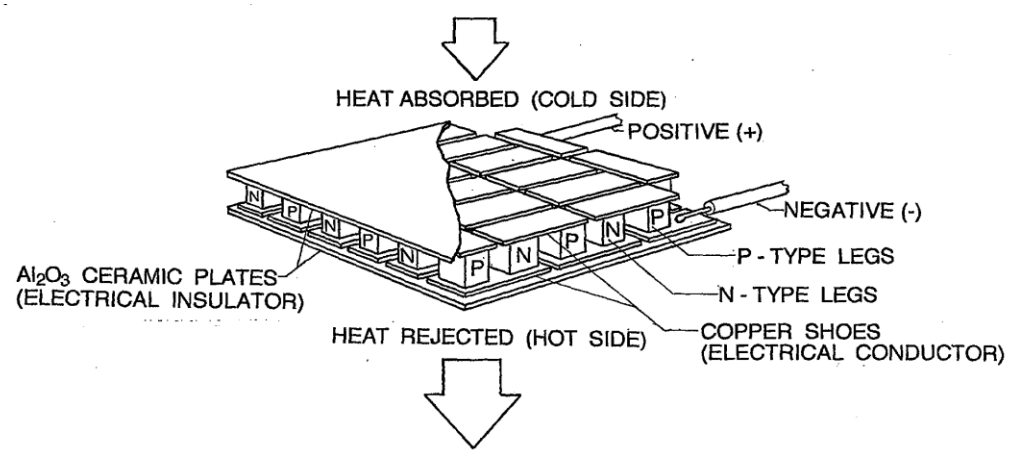

Figure 2.1 Bi-Te Single-Stage Thermoelectric Module

2.1 Operating Principle

When an electric current is passed through a thermocouple, a difference in potential of charged carrier is created at the junctions of two dissimilar materials. According to Peltier effect, due to this movement of charge carrier at the junction, energy is either generated or rejected to the surrounding from the junction. This phenomenon results in energy transportation i.e. heat transfer from cold junction to hot junction of thermocouple.

There are two types of semiconductor material used in a thermoelectric module: one is positively charged p type of semi-conductor which has deficiency of electrons, while the other is negatively charged n type of semi-conductor having excess of electrons. These semiconductors are connected together by an electrically conductive copper tab to make a pair for a thermoelectric pallet i.e. TE pallet.

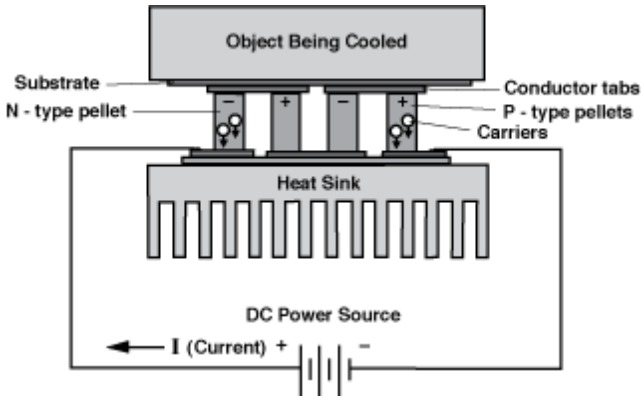

Figure 2.2 Thermoelectric Module Cooling Principle

As shown in figure 2.2, when an electrical current is passed through a TE pallet, electrons moves across junction from p type to n type and leaps to higher energy state level. This causes heat absorption and the temperature reduces at this junction which makes that side of thermoelectric module cold. Again, the electrons continue to move across the junction from n-type to p-type of semiconductor causes electrons to drop in energy level. Thus, energy in the form of heat is expelled creating increment in temperature at that junction, making that side hot

(where heat sink is attached). A rate at which different heat loads dissipated in thermoelectric module is proportional to the electrical current provided and the number of thermocouples in a module.

2.1.1 Comparison with Conventional Refrigeration cycle

As illustrated in figure 2.3, in a conventional refrigeration cycle, the fundamental parts are evaporator, compressor, condenser and liquid refrigerant. The evaporator is a part where the refrigerant is pressurized to expand and then evaporate. Due to this change in state of matter from liquid to gaseous, heat is absorbed. The compressor acts like a refrigerant pump and recompresses the refrigerant from gas to liquid. The condenser releases heat absorbed by the evaporator and also the heat produced by compressor are pumped out into the surrounding environment.

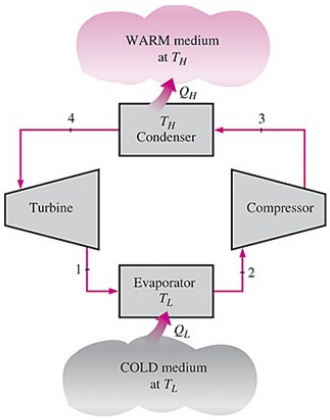

Figure 2.3 Conventional Refrigeration Cooling Cycle

Similarly, in thermoelectric, doped semi-conductor material acts functionally as liquid refrigerant. The cold side acts as evaporator where heat is absorbed. The DC current acts as a compressor, so when current is applied to the thermoelectric, heat absorbed on the cold side is pumped to the hot side where the fined heat sink are attached. This heat sink works as condenser and releases its own heat energy into the surrounding environment.

2.2 Principle Theories of Thermoelectricity

Thermoelectric cooling is govern by three identical effects which are reversible interchange of thermal energy as well as electrical energy i.e. See beck effect, the Peltier effect and the Thomson effect .Besides this effects there are two more effects which have irreversible effect or the residual effect of heat generation namely Joule Effect and Fourier Effect.

2.2.1 Seebeck Effect

The Seebeck effect was given by Thomas Seebeck. It states than an electric potential or voltage is generated when the two junctions formed by two dissimilar materials are held at different temperatures. This gives

$$dV = \alpha_{12}\, dT \qquad 2.1$$

Where α is called Seebeck coefficient having units in *V/°C*. α_{12} can be either positive or negative. It is positive, if p type of conductor is electrically positive with respect to n type of semiconductor, when the thermocouple is open at cold junction. Thus,

$$\alpha_{12} = \alpha_1 - \alpha_2 \qquad 2.2$$

2.2.2 Peltier Effect

Given by Jean Peltier, it states that heat is generated or rejected at the junction of two different materials when a current is applied. Thus, the amount of heat pumped to thermoelectric is

$$q_P = \pi_{12} I \qquad 2.3$$

$\pi_{12}$is known as Peltier coefficient. The amount of this heat is proportional to the current.

The relationship between Seebeck effect and Peltier effect was given by William Thompson as

$$\pi = \alpha T \qquad 2.4$$

$$\therefore q_P = \alpha_{12} IT \qquad 2.5$$

2.2.3 Thomson Effect

Lord Kelvin (William Thompson) discovered that Seebeck effect and Peltier effect are dependent on each other for working of thermoelectric and named this dependency as Thompson Effect. This effect depends on temperature gradient along the electric conductor. It states that, heat is generated or rejected per unit length in the conductor when electric current flows through closed circuit. This heat is expressed as

$$q_T = \zeta I \frac{dT}{dx} \qquad 2.6$$

ζ is known as Thompson effect. The principal behind this effect is that electrons try to achieve equilibrium in conductor by either rejecting or absorbing heat.

2.2.4 Joule Effect

Joule effect states that the heat generated by an electrical current is equal to the product of square of current and electrical resistance in the conductor. The Joule heat generated is given by

$$q_J = I^2 R \qquad 2.7$$

Where the resistance, *R=ρ (L/A)* and *ρ (Ω.cm)*.s the electrical resistance.

2.2.5 Fourier Effect

The Fourier effect or Fourier conduction law states that heat rate is proportional to the area normal to the heat flow and temperature along the conducting path. It is given by

$$q_F = -kA \frac{dT}{dx} \qquad 2.8$$

k is known as thermal conductivity of material having area as A and conducting length as x.

2.3 Thermoelectric Cooling Theory

The TE pallet is consist on two branches namely p type of semiconductor having positive α_1 while the n type of semiconductor has negative α_2.The heat is conducted in each

branch through Peltier cooling current. Change in the direction of this current at the junction of two dissimilar materials causes heat to liberate or generate. Thus, the total heat flowing in each leg cold side to hot side (i.e. flow from source to sink) in Thermoelectric will be sum of Peltier heat and Fourier conduction heat which is residual heat flown back from hot side to cold side, given by

$$Q_P = \alpha_1 IT - kA\frac{dT}{dx} \tag{2.9}$$

$$Q_n = -\alpha_2 IT - kA\frac{dT}{dx} \tag{2.10}$$

Here, the Peltier current flow is considered as positive. Hence, the heat flow to the cold side is given by

$$q_c = \left|Q_p + Q_n\right| \tag{2.11}$$

Also, the Joule heating is generated in the branches of TE pallet. To balance Joule heat, there is non-constant thermal gradient given by Fourier conduction.

$$\frac{I^2\rho}{A} = -kA\frac{dT}{dx} \tag{2.12}$$

Here, the Thompson effect is considered as zero. Now, taking boundary conditions as $T=T_C$ at $x=0$ and $T=T_H$ at $x=L$. This gives solution as

$$-kA\frac{dT}{dx} = -\frac{I^2\rho}{A}\left(x - \frac{1}{2}L\right) + \frac{(T_h - T_c)kA}{L} \tag{2.13}$$

Substituting equation 2.13 in 2.11 and using 2.9 and 2.10 gives net heat flow or the cooling capacity as

$$q_{net} = (\alpha_1 - \alpha_2)T_C I - \frac{I^2 R}{2} - \frac{(T_h - T_c)kA}{L} \tag{2.14}$$

Where thermal conductivity for parallel connection is

$$K = \frac{k_1 A_1}{L_1} + \frac{k_2 A_2}{L_2} \tag{2.15}$$

And electrical resistivity for series connection is

$$R = \frac{L_1\rho_1}{A_1} + \frac{L_2\rho_2}{A_2} \qquad 2.16$$

From the above equations, the thermoelectric materials must have following properties:

- Higher Seebeck coefficient, α to generate lager amount of power in TEC.
- Low electrical resistivity, R for reducing Joule effect.
- Low thermal conductivity, *K* in order to maintain large temperature gradient in TE pallet

2.4 Figure of Merit

Altenkirch in 1911 combined the above mentioned thermoelectric properties and named it as figure of merit, Z.it is given by

$$Z = \frac{\alpha^2}{k\rho} \qquad 2.17$$

It has unit of $^oC^{-1}$ and is taken as measurement of usefulness of material in TEC device. The material for the thermoelectric is selected with the help of figure of merit. The value of product of *ZT* has to be one or higher than one.

Pure metal has low α which translates into low thermal conductivity. While, in insulators electrical resistivity is low, so more Joule heating is seen in this material. The value of *k* or ρ cannot be changed in metals or insulators. Thus, the figure of merit for them is always low. While in semiconductors, values of *k* or ρ can be adjusted individually by doping to match the requirements of TEC. Bi_2Te_3/Sb_2Te_3 combination of semiconductors are used commercially in present state as it has ZT value around 2.4.

Peltier effect varies linearly with current and also Joule heat varies with current. Thus, it can be said that for a particular current, there is maximum cooling power. The maximum cooling power is reached when $\frac{d(q_{net})}{dI}$=0 and the current will be

$$I_{max} = \frac{(\alpha_1 - \alpha_2)T_c}{R} \quad 2.18$$

Thus, maximum cooling power is

$$(q_{net})_{max} = \frac{(\alpha_1 - \alpha_2)^2 {T_C}^2}{2R} - (T_h - T_c)k \quad 2.19$$

Maximum temperature difference is being recorded when $(q_{net})_{max}$=0 i.e. cold side is thermally insulated. Hence,

$$(T_h - T_c)_{max} = \frac{(\alpha_1 - \alpha_2)^2 {T_C}^2}{2KR} \quad 2.20$$

As comparing equation 2.20 with 2.17, gives

$$Z = \frac{(\alpha_1 - \alpha_2)^2}{KR} \quad 2.21$$

This figure of merit is useful with the application of thermoelectric power generation.

The heat rejection at hot side is given by sum of heat pumped (cooling power capacity) and heat required for pumping out heat i.e.

$$q_{hot} = q_{net} + P_e \quad 2.22$$

This equation and gives

$$q_{net} = (\alpha_1 - \alpha_2)T_C I + \frac{I^2 R}{2} - \frac{\left[(k_1\rho_1)^{\frac{1}{2}} + (k_2\rho_2)^{\frac{1}{2}}\right](T_h - T_c)k}{R} \quad 2.23$$

2.5 Coefficient of Performance

The coefficient of performance for refrigeration is ratio of cooling power (cooling capability) to the required input power, i.e.

$$COP = \frac{q_{net}}{P_e} \quad 2.24$$

The required input power depends on electrical energy supplied to the thermoelectric. This input power is sum of Joule effect and Seebeck effect. Thus, the total required power input is

$$P_e = I^2R + (\alpha_1 - \alpha_2)(T_h - T_c) \quad 2.25$$

Therefore, COP can be written as

$$COP = \frac{(\alpha_1 - \alpha_2)T_C I - \frac{I^2R}{2} - \frac{(T_h - T_c)kA}{L}}{I^2R + (\alpha_1 - \alpha_2)(T_h - T_c)} \quad 2.26$$

The optimum current is found when the COP is maximum. The maximum COP is obtained when $\frac{d(COP)}{dI} = 0$.This leads to

$$COP_{max} = \frac{T_C}{(T_h - T_c)}\left[\frac{\left(1 + ZT_{Avg}\right)^{\frac{1}{2}} - \frac{T_h}{T_c}}{\left(1 + ZT_{Avg}\right)^{\frac{1}{2}} + 1}\right] \quad 2.27$$

Giving optimum current as

$$I_{opt} = \frac{(\alpha_1 - \alpha_2)(T_h - T_c)}{R\left(1 + ZT_{Avg}\right)^{\frac{1}{2}} - 1} \quad 2.28$$

Where, $T_{Avg} = \frac{T_h - T_c}{2}$.

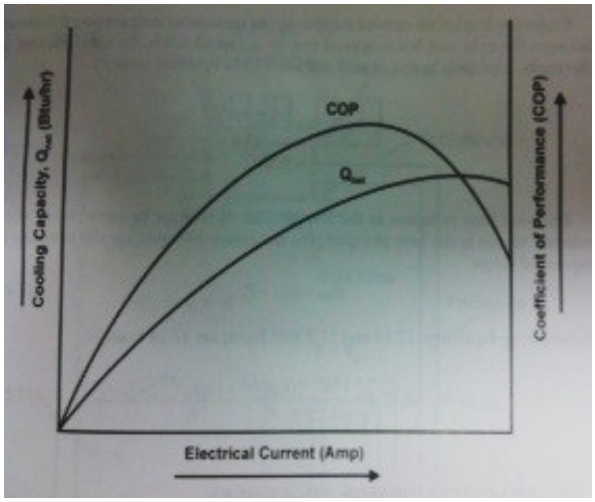

Figure 2.4 Cooling Capacity of Typical TEC

From the above figure 2.4, it indicates that with increase in current applied, COP will be increased until it reaches optimum current. The COP is maximum at this value of current. Beyond this point the Cop will start declining.

2.6 Advantage and Disadvantage of Thermoelectric Module

2.6.1 Advantage of Thermoelectric Module

The advantages of thermoelectric module are as follows:

- Direction of thermoelectric's heating pump is reversible by changing the polarity of current.so; it can work as cooler and heater too.
- Thermoelectric module does not have moving part to wear and tear; therefore there is no need of any maintenance.
- It has capacity to work for more than 200,000 hours in steady state
- It resists shock and vibration.
- It can work in too severe or sensitive environment.
- It does not contain any harmful material like chlorofluorocarbons (CFCs) which can damage environment.
- It does not dependent on gravity. Thus, it can be placed in any direction.
- Temperature can be maintained in fraction of degree, even below ambient temperature using thermoelectric module by controlling the power load provided to the module.
- Temperature can work between 100ºC to -100ºC of heat sink temperature.
- It can work at extremely low acoustic level by choosing proper heat sink and fan.
- It can be tailored to any size as per the requirement of application.

2.6.2 Disadvantage of Thermoelectric Module

- The main disadvantage of thermoelectric module is lower efficiency when compare to non-thermoelectric modules when working as power generator. It is usually 0.3 or lower.
- Also it has lower co-efficient of production (COP) with range 0f 0.4 to 0.7.

CHAPTER 3

THERMAL MANAGEMENT OF 3D-ICs

Dr. Gordon Moore, co-founder Intel™ predicted in 1960s that the numbers of transistors incorporated in a chip will approximately double every 24 months [5]. The figure 3.1 illustrates the Moore's law.

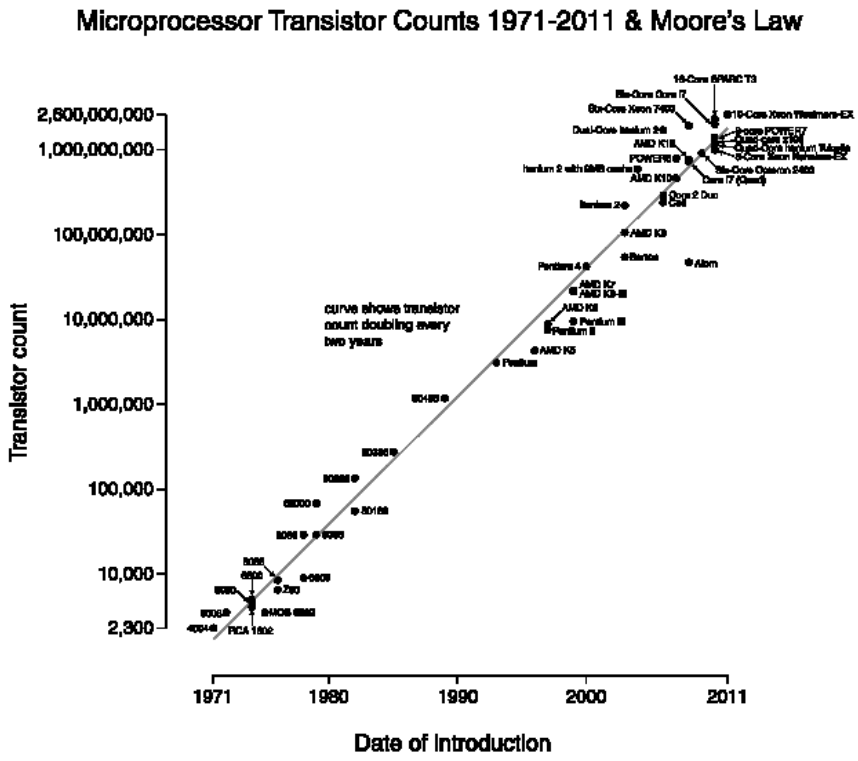

Figure 3.1 Moore's Law Prediction from Year 1971 to 2011

This forecast in silicon industry became so true that it is known as Moore's law. The initial idea of saying that was to describe the business model for the semiconductor industry with a challenge of increasing the functionality and performance while decreasing the size of the device and cost.

This changed the entire point of view of the semiconductor industry and as we can see the increasing transistor count on an IC will increase the complexity of it. To keep up with the Moore's Law, the transistor packaging technologies evolved exponentially by the time from small scale integration (SSI) to Medium scale integration (MSI) to large scale integration (LSI) to very large scale integration (VLSI). The latest highest transistor count in a commercially available CPU is 2.5 billion transistors in Intel's 10-core Xeon Westmaster-EX compared to very first Intel 4004 had 2300 transistor in 1971 [6]. From this we can see the increase in the compactness for the packaging which forced the packaging technology to compete with the need and to evolve at the same pace. There is also implied here that the new compact IC will required higher processing power due to the higher transistor count.

The exponential growth in the transistor count doesn't mean that it will translate linearly into the practical CPU performance. It is obvious to say that the required power will grow linearly with the transistor count. Based on the example described on the Wiki, with the every new generation of technology allowing transistor density doubles, IC will become only 40% faster than its previous version while the power consumption will double.

This new trend of Nano packaging also presents the great challenge to the thermal management team of the IC production. The greatest challenge is that will it be possible to remove all the heat generated by these tens of thousands of components or transistors in a single IC? Since the Integrated Circuits structures are layer formation (3D IC has 3 layers on each other), they have surfaces available for cooling very close to each center of heat generation. See the figure 3.2 for the illustration of 3D IC.

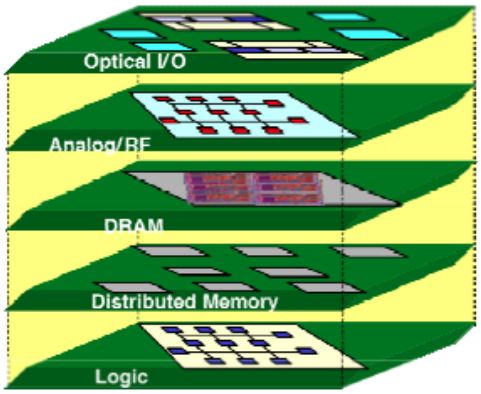

Figure 3.2 Schematic of 3D-IC Structure

The figure 3.2 illustrates the 3D stack of ICs. We can see that the average distance between the system components is reduced to improve the performance but the downside is the challenge to dissipate the heat produced by these components. The very large System on Chip (SoC) such as shown in the figure will dissipate about 50-100 W/cm^2 average heat.

The heat generated by Integrated Circuits (IC) must be dissipated or flowed away from the components in order to improve the reliability, performance and to avoid any kind of functional failures. The traditional techniques used for the heat dissipations are use of heat sinks and fans for the air cooling. The following figure 3.3 illustrates one of the traditional heat sink on the CPU with fan attached to it to remove the heat.

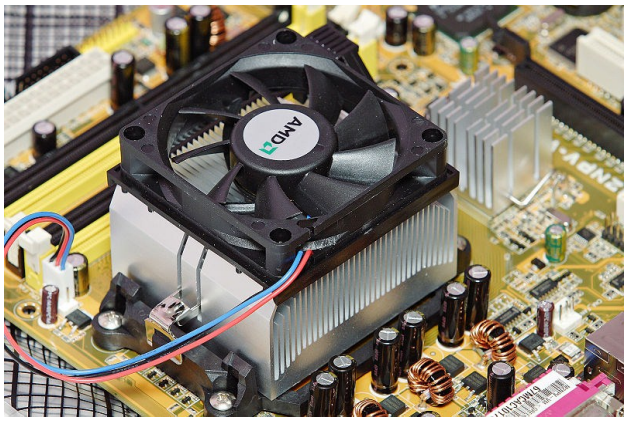

Figure 3.3 CPU Heat Sink with Fan

To look into more about the heat management challenge, let's look more detailed view of the heat generation. The heat generated in the Integrated Circuits is most likely transferred to the other components by means of convection and conduction heat transfer and very little due to radiation. The heat sinks function on basic principle of the heat transfer by efficiently transferring the heat from a component at high temperature to the component at lower temperature with the greater heat capacity. The most common design of the heat sinks are seen in the industry is a metal device with many fins. The heat transfer by this means works if you have larger surface area and that will result into the rapid heat transfer to the surrounding, cooler air.

There is heat sink effective for the 1D-IC which will not work for the 3D stacked IC. As we stack the additional 2 layers of silicon wafers on the 1D-IC to accommodate more components on each other without sufficient space between the layers. If we try to put the heat sink same as used for the 1D-IC on this new created 3D-IC, it will eventually fail to dissipate the heat generated by all the components and which may result in catastrophic failure of the IC. The reason behind this is the surface area of the heat sink will remain same while the heat generated inside the IC almost tripled its values from the original 1 layer of IC. Due to the evolution and challenge of making electronic devices more compact you can't put the separate heat sinks for each layer on 3D stacked IC. The traditional heat transfer techniques will fail for

this newly developed stacked 3D-IC. Also it would require more space for the implementation which will pose the space issue on the compactness as we are trying to fit more components on the IC.

The research and development is going on how to tackle heat challenge that comes along with the compactness and stacked 3D-IC [7]. The one of the ongoing research on the heat dissipation of 3D-ICs is using the microchannels cooling elements placed into the lower face of each chip to remove heat at local level on each layer. There can be different types of coolants used for heat removal, water based Nano-fluid and an environmentally friendly or two-phase evaporating refrigerant. The temperatures with the 3D-IC system have to stay below 90° C during the operation to avoid damage to the chip. The objective of the coolant is to maintain the chip's temperature below this value while dissipating heat per layer up to 100-150 W/cm^2 and targeting the inlet coolant temperature of 30-40° C.

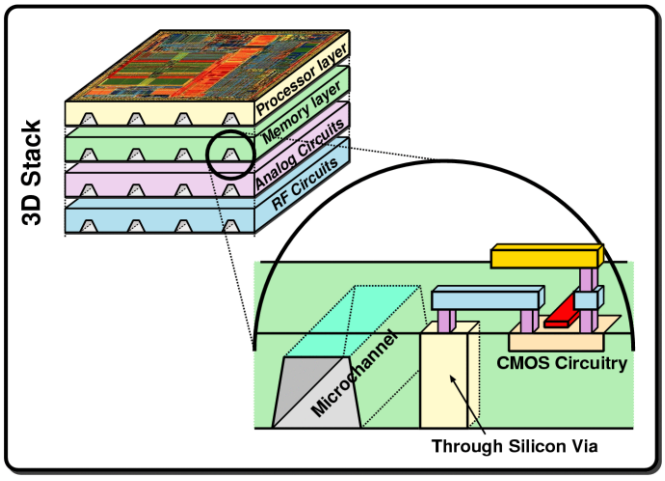

Figure 3.4 Schematic of target 3D-IC stack

The above figure illustrates the possible solution of the heat dissipation for 3D-IC with using the microchannel concept described above. We can see the microchannels running through each silicon layer of the 3D stack and the coolant fluid will be running through each of the layer and provide the local heat transfer which will be more effective compared to the conventional heat transfer techniques.

Thus, to summarize, the Moore's prediction is coming pretty much true and will be in the future from looking at the trend in the Semiconductor industry. The increase in the compactness requires the increase in the required power and will produce the double heat as much. In order to provide the efficient heat dissipation for 3D stacked IC and prevents any premature failures we have to come up with the nontraditional techniques that could be accommodated with the Nano packaging technologies.

CHAPTER 4

THERMOELCTRIC COOLING SYSTEM

From chapter 3, it can be said that more reliable cooling method is required to improve the chip performance by reducing thermal management issues and bringing the temperature of chip below ambient condition. Today, commercially used methods are passive methods and active methods. In passive method, generally heat sinks are used while in active cooling method, thermoelectric module is used.

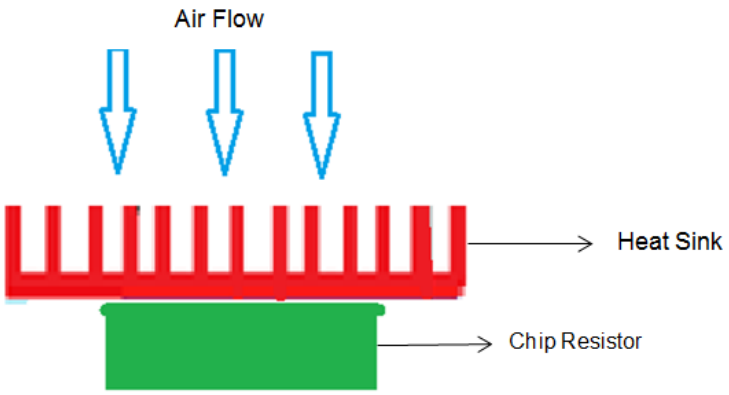

Figure 4.1 Passive Cooling Method

Using Phan and Agonafer [1] work, both of these methods are evaluated in Ansys Icepak. For passive cooling, the chip resistor is taken instead of 3D-IC. For chip resistor, model CPD 230-1B (8.890x5.842x1.016mm) manufactured by Component General, Inc is used. As illustrated in figure 4.1 the heat sink by AlphaNovaTech Inc., model LPD 70-25B (70x70x25mm) is placed directly above the chip resistor. The flow of air is set parallel to the fins of the heat sink and it has value of 22.05CFM. For power in chip resistor varying from 25W to 100W, the temperature values in chip resistor were found to be as shown in figure 4.2.

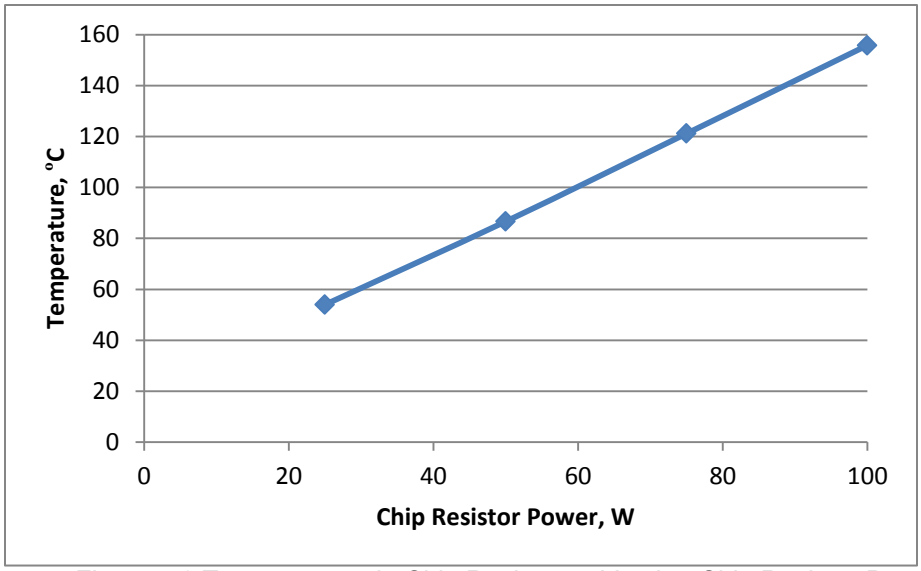

Figure 4.2 Temperatures in Chip Resistor at Varying Chip Resistor Power

In modeling of active cooling method, thermoelectric model, CP 1.4-127-10L (40x40x4.7mm), rated at 3.9A, 15.4V, and 33.4W max at temperature, T=0ºC is selected. It is placed between heat sink and chip resistor as shown in figure 4.3. The flow of air is set parallel to fins of heat sink with value taken as 22.05CFM. For thermoelectric working from 25W to 200W with change in chip resistor power of 25W to 100W, the corresponding temperature values (figure 4.4) in chip resistor are obtained.

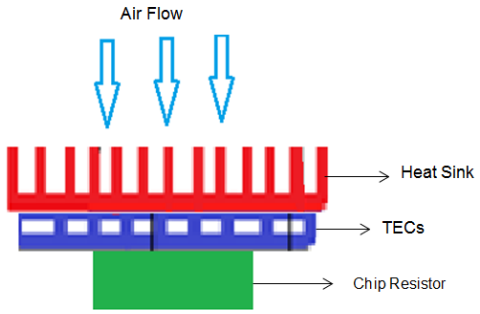

Figure 4.3 Active Cooling Method

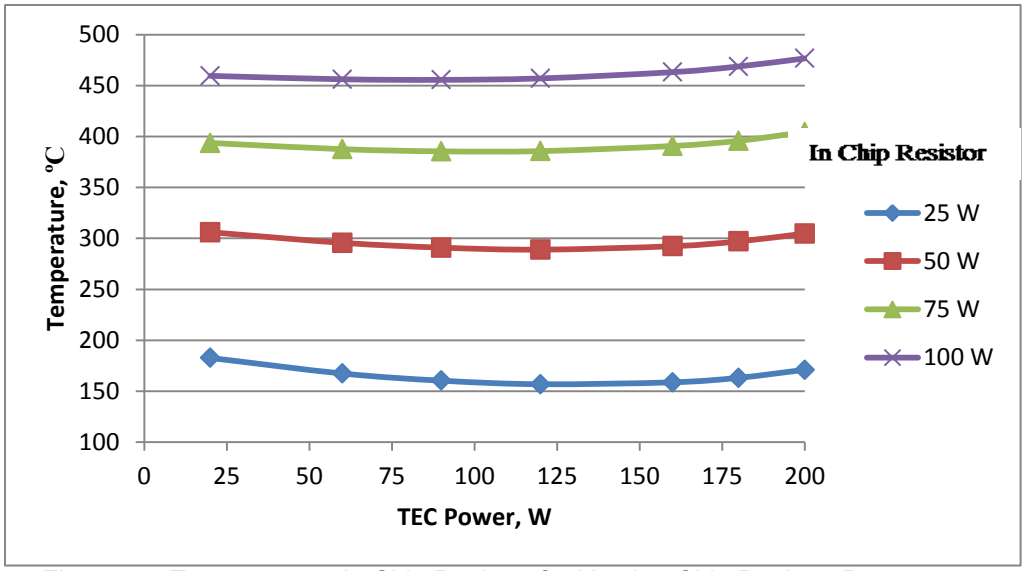

Figure 4.4 Temperatures in Chip Resistor for Varying Chip Resistor Power

From Figure 4.2 and 4.4, it can be observed that temperature of chip resistor using Thermoelectric is more than a chip resistor with only a heat sink. This is due to additional power supplied to the thermoelectric module for cooling chip resistor. Again, none of the above mentioned methods were sufficient enough to cool the chip resistor below ambient conditions (in these cases, ambient temperature was taken as 24.5°C).

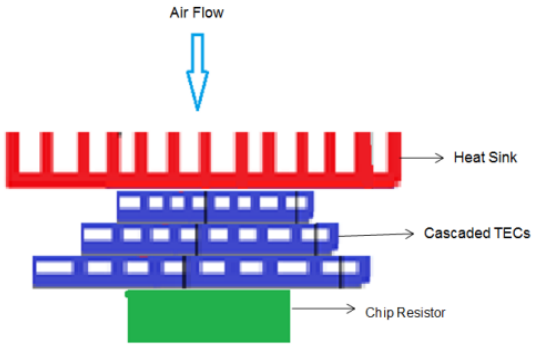

Figure 4.5 Cascading Thermoelectric Modules

This gives rise to use multiple thermoelectric modules to bring temperature of chip resistor lower than ambient temperature. Cascading thermoelectric modules consecutively on top of each other as shown in figure 4.5, results in higher thermoelectric power. Thus, need for

bigger heat sink arises to handle large heat flux coming from thermoelectric module [8]. Also, more horizontal footprint on motherboard is needed to accommodate the complete setup which is commercially not possible. This structure gives rise to stability issues too. Hence, staking thermoelectric modules consecutively is not a good option for higher performance electronic cooling application.

Placing thermoelectric module vertically in three dimensional fashion, gives more surface contact with the chip for more heat transfer between chip and thermoelectric module. Thus, more heat will be pumped out of a chip for any given thermoelectric module power. Moreover, the thermoelectric module is non-directional and gravity free which make it possible to place the model vertically. As a result, fewer footprints are needed and no stability issues will occur.

CHAPTER 5

MULTI-DIMENSIONAL HEAT TRANSFER SYSTEM (MHTS)

As per previous work by Phan and Agonafer [1], Multi-Dimensional Heat Transfer System (MHTS) was developed. This system consists of copper core in the center surrounded by four thermoelectric coolers which are further attached to four heat sinks as shown in figure 5.1. A chip resistor used as a 3D-IC is embedded in the bottom surface of copper core. The copper core acts as a heat spreader increasing the total surface area available for conducting the heat away from the source. In this chapter, the Computational-Fluid-Dynamic (CFD) and experimental of the Multidimensional-Heat-Transfer-System (MHTS) were investigated

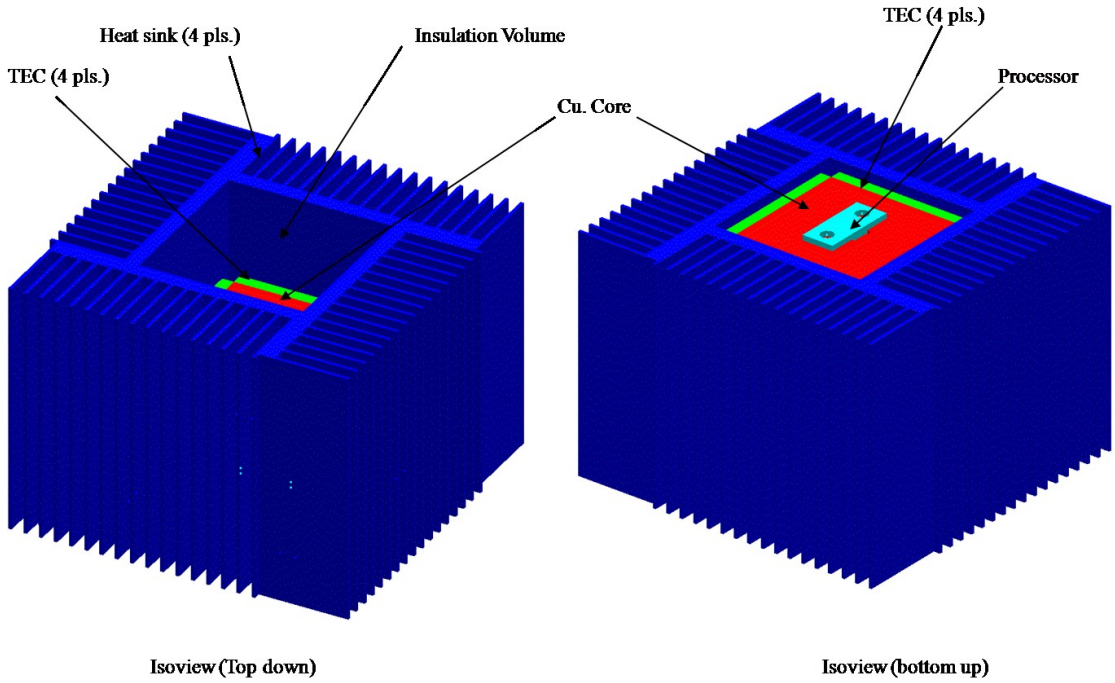

Figure 5.1 Schematic Diagrams of MHTS [9]

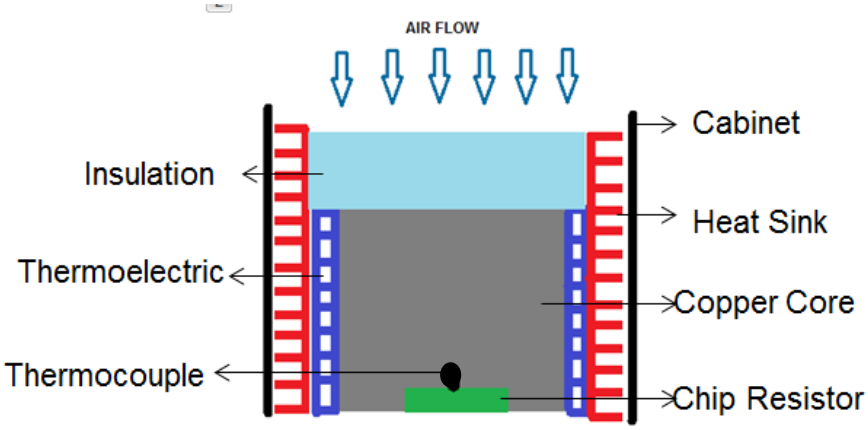

Figure 5.2 Thermocouple Placement in MHTS

The Dimensions and the Thermal properties of all material used for MHTS are given in table 5.1 and table 5.2.

Table 5.1 Components and its Dimensions

Components	**Dimensions(*mm*)**
Chip Resistor (heater)	8.890x5.842x1.016
Heat Sink	70x70x25
Copper Core	40x40x40
Thermoelectric Module(TEC)	40x40x4.7
Insulation form(Top)	49.4x49.4x30
Insulation form(Bottom)	49.4x49.4x1.97

Table 5.2 Components and its Material Properties

Component	Material	Thermal Conductivity (*W/m-K*)	Density (*kg/m*^{3})	Specific Heat (*J/kg-K*)
Chip heater	Beryllium Oxide	230	2880	1088
Heat Sink	Aluminum	240	2700	900
Copper Core	Copper	387.6	8933	381
Insulation form	Polystyrene-rigid-R12	0.0.4	56	1300
TEM Material	Nano-Diamond particle Thermal Compound	5.3	2200	-
	Nano-Silver particle Thermal Adhesive	350,000 *W/m².ºC*	-	-

5.1 Experimental Model

The experimental model was tested in the air flow chamber, which was designed in accordance with AMCA 210-99/ASHRAE 51-1999 shown in figure 5.3. T-type of thermocouples was embedded in the copper core above the chip resistor (figure 5.2) and the airflow rate data was recorded through a data acquisition system. Air is forced through the air flow bench by an axial fan, through a flow straightener to ensure that the air flow approaching the nozzle area is

laminar flow. Depending on specific air flow rate, different nozzle size inside using rubber stoppers (figure 5.4). For this experiment the flow rate was set at 22.05CFM, thus 1 *in* nozzle is used while other nozzles are blocked.

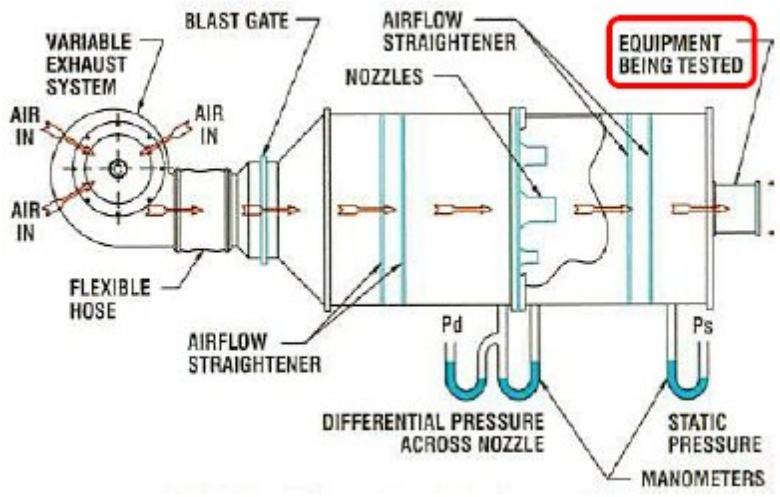

Figure 5.3 Air Flow Bench Set Up

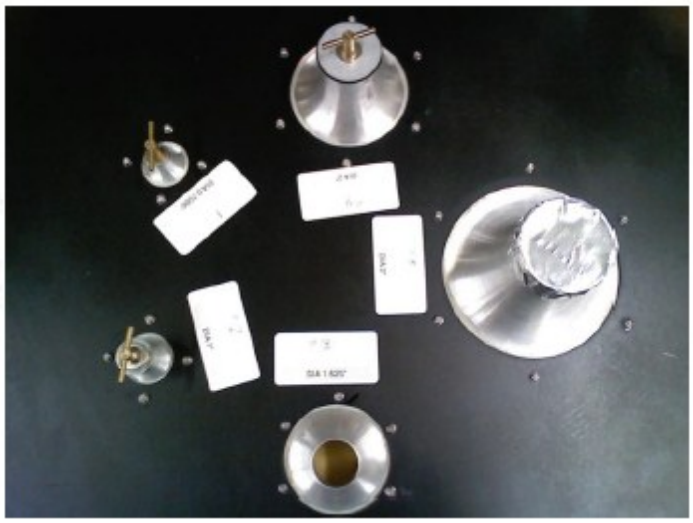

Figure 5.4 Air Flow Bench Array

The air flow rate can be calculated using

$$Q = V \times A$$

Where *Q* is the air flow rate (*m^3/min),* A is the nozzle sectional area (m^2) and *V* is the average flow velocity through the nozzle (*m^2/s)*.From above equation, the flow for Ansys Icepak's cabinet was calculated as 1.04 *m/s* with area of the cabinet cross-section taken as 100x100 mm^2.

The average air flow through the nozzle can be obtained using Equation below:

$$V = \left(\frac{2gP_n}{r}\right)^{1/2}$$

Where *g* is the gravitation acceleration, 9.8 *m/s^2*, *Pn* is the differential pressure, and *r* is specific gravity of air, 1.2 *kg/m^3*at 20°*C*, 1 *atm*.

The large end opening of the air flow bench was reduced down to a smaller square opening, which is exactly the same size as the devices to be tested to ensure that the air flow does not bypass the heat sinks, figure 5.5.The cabinet for MHTS is constructed out of polycarbonate sheet to ensure that the air entering the testing device is adiabatic.

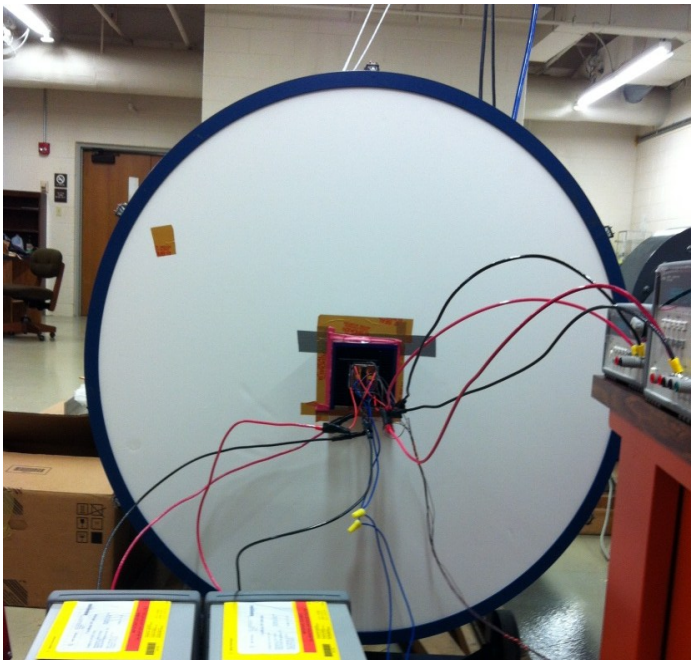

Figure 5.5 MHTS on Air Flow Bench

The construction of MHTS is explained in below subsection.

5.1.1 Stacked Device

The chip resistor, CPD 230-1B (8.890x5.842x1.016mm) manufactured by Component General, Inc. is taken instead of 3D-IC, to replicate the heat generation in stacked devices, while working at different power output. It is rated at maximum power of 150W and ±10%Ω tolerance. The solid state heater has a polished silicon surface, so it does not require polishing.

Figure 5.6 Chip Resistor, CPD 230-1B

As Shown in figure 5.6, the electrical wire of 16AWG are solder to the silver tabs on the bottom surface of chip resistor for electrical connection with power supply. The 96/4 silver-

bearing solid wire solder is used and the wires are soldered with the help of Butane micro flame torch. The tolerance in actual chip was found out to be 10.3Ω, when checked.

The power is applied to chip resistor of magnitude of 25W, 50W and 75W.

5.1.2 Copper Core

The copper core (40x40x40mm) is made up of copper C11000 material having thermal conductivity of approximately 388 to 391 *W/m·K*. A groove as the same size of chip resistor is cut at center of the bottom surface of the copper core as shown in figure 5.8.The chip resistor is embedded in this groove. All the surfaces of the core are sanded in order to make smooth surfaces and eliminate the microscopic imperfection of flat contact with the thermoelectric. The copper core was cleaned with isopropyl alcohol to remove any dirt particles from the surfaces.

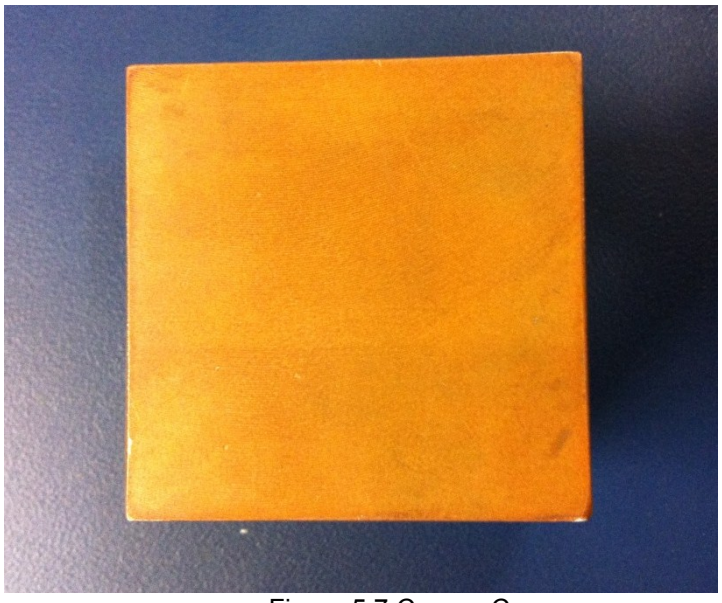

Figure 5.7 Copper Core

Figure 5.8 Bottom Surface of Copper Core Showing Recess Portion for Chip Resistor and Thermocouple

A slit is grooved for placing thermocouple through the center of already recessed portion on the bottom surface of core as illustrated in figure 5.8, in order to take temperature reading on the surface of the chip resistor. Also, holes are drilled on the opposite corners, perpendicular to the slit made for thermocouple to secure the chip resistor with the help of metal strip (40x9x1mm) and bolts.

The bottom surface of copper core is sprayed with polystyrene-rigid-R12 insulation form for insulating it thermally as well as electrically.

5.1.3 Thermoelectric Module

The thermoelectric modules are placed between copper core and heat sink as shown in figure 5.8. The thermoelectric modules used, are made by Lairds Technology, shown in figure 5.10. The model selected was CP 1.4-127-10L (40x40x4.7mm), rated at 3.9A, 15.4V and 33.4W max at temperature, T=0ºC.The power is supplied as a product of current, I and Voltage, V i.e. P=VI, passed through thermoelectric.

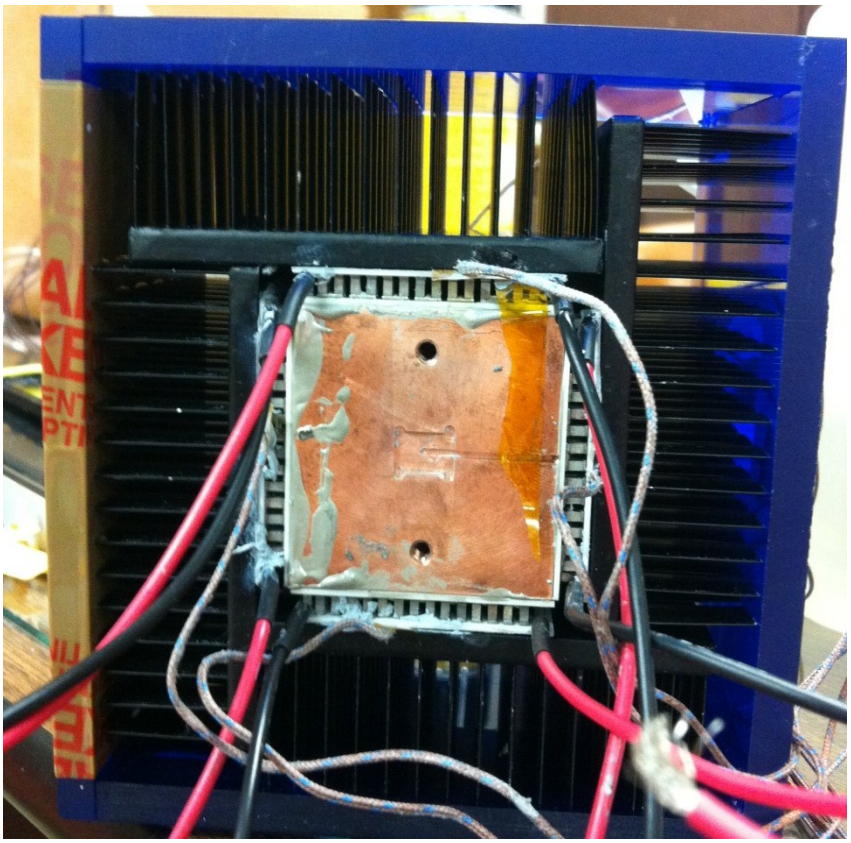

Figure 5.9 Thermoelectric Placed between Copper Core and Heat sink

Figure 5.10 Thermoelectric Module, CP 1.4-127-10L

The top and bottom surface of the thermoelectric are made of ceramic material; therefore there is no need to sand them. The total power in the thermoelectric modules, i.e. 4 thermoelectric is being varying from 20W to 180W.

5.1.4 Heat Sinks

Heat sinks by AlphaNovaTech Inc., model named LPD70-25B (70x70x25mm) are placed vertically as shown in figure 5.9. They are attached to the thermoelectric module. Their bottom surface is sanded and cleaned with isopropyl alcohol for smooth and cleaned contact with thermoelectric module. Again, they are placed offset to each other (figure 5.9 and figure 5.12) and stood affixed with the help of screws at the base with another heat sink to hold them together.

5.1.5 Contact Resistance

As the surface of any object cannot be perfectly smooth and imperfection free, a contact resistance is made between two surfaces by applying thermal grease or adhesive. This thermal grease helps in filling up the imperfections and makes a surface smooth enough to lay flat on another surface. To make sure that there is proper contact resistance between the cold core and the thermoelectric module, Nano-silver particles thermal adhesive compound produced by Arctic Silver Incorporated, is used to bond their surfaces. The thermal conductance of this compound is greater than 350,000 $W/m^{2.}°C$ per 0.001 inch layer. Also, Nano-diamond particle thermal compound by the same company is used for proper contact resistance between heat sink and thermoelectric, and chip resistor and thermoelectric module. It has thermal conductance of 5.*3W/m-K*. First, the silver thermal adhesive is applied on the surface of core and thermoelectric and left to cure for five hours. During the time for curing, the core and thermoelectric are held by C-clamps. This whole procedure is again repeated for attaching heat sink with the thermoelectric, and chip resistor with the core, by using Nano-diamond thermal grease.

5.1.6 Inlet and Outlet Grill

The top surface of the MHTS is taken as inlet of air flow in a manner that the flow is parallel to the heat sink's fins (fig 5.2).

While the bottom surface of MHTS is taken as the outlet.

5.1.7 Cabinet

A tight cabinet is constructed out of polycarbonate sheet of 6mm thickness having dimensions of 100x100mm², to make sure that there is no gap between MHTS and the cabinet (figure 5.11).The top and the bottom portion are kept open. The MHTS is placed inside this cabinet in such a fashion that the air is allowed to flow parallel to the fins of heat sink without any obstructions.

Also, the open surfaces on the top of the copper core are insulated by polystyrene-rigid-R12 insulation form.

Figure 5.11 MHTS

5.2 Computational Fluid Dynamic Model

For CFD analysis, commercially available software Ansys Icepak is used. Every component is placed as per their order in MHTS (figure 5.12) and their dimensions and properties taken from table 5.1 and table 5.2.

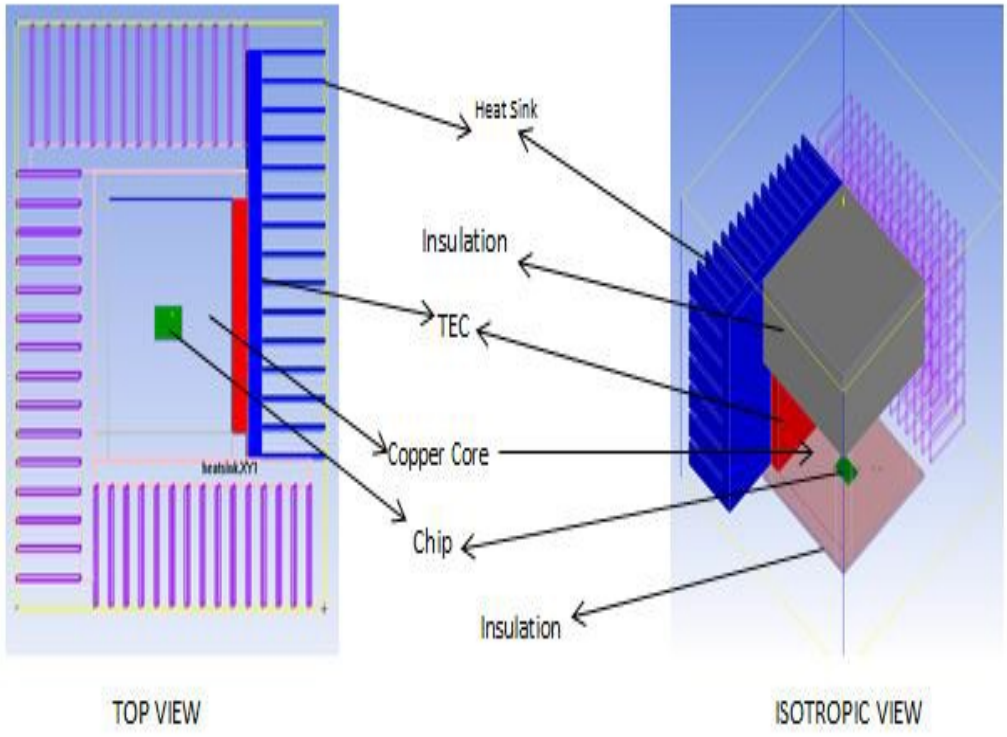

Figure 5.12 CFD Models of MHTS

5.2.1 Stacked Device

A block of Beryllium Oxide as material is constructed with the dimensions of chip resistor to work like a stacked device. The power supplied in this block varies from 25W to 75W with increment of 25W.

5.2.2 Copper Core

A block of copper as material is taken with dimensions 40x40x40mm. A groove of chip resistor's dimension is recessed from the bottom surface of copper block.

5.2.3 Thermoelectric Module

A pre-made thermoelectric, CP 1.4-127-10L from Ansys Icepak Macro library is taken with electrical properties already provided by Lairds Technology,Inc. to the software and is placed vertically. The power was applied to thermoelectric in terms of P=VI, where voltage, V=15.4*V* is kept fixed, and the current is changed in accordance with the value of the power. The value of the current was specified in macro window as shown in figure 5.13 with its G factor as 0.007*cm* and number of thermocouple as 127 in thermoelectric module. G factor is the ratio of area of thermoelectric to the length of TE pallet. The total power in Thermoelectric varies from 20W to 200W.

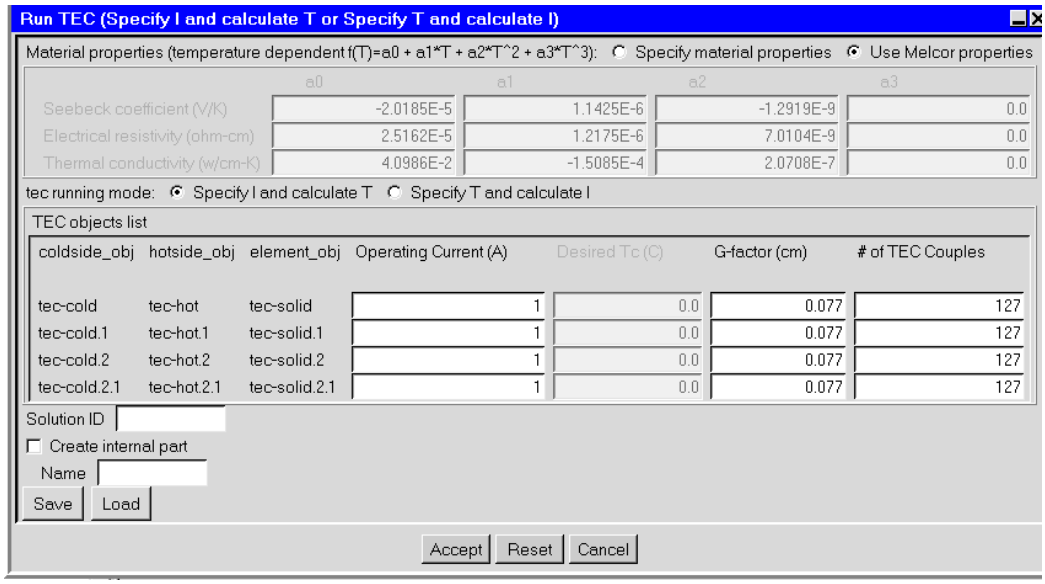

Figure 5.13 Macro Window for Specifying Current for TEC in Ansys Icepak

5.2.4 Heat Sinks

The heat sinks were made up of pure aluminum as material and the number of fins were taken as assigned by AlphaNovaTech, Inc. for the specific model number LPD70-25B. The extruded type of fins was selected with flow of air kept in Y-direction as seen in figure 5.12.

5.2.5 Contact Resistance

A thin conducting plate is taken in place of thermal grease as contact resistance for the CFD model by specifying thermal conductivity of thermal grease.

5.2.6 Inlet and Outlet Grill

The top surface of the MHTS is chosen as inlet and velocity of 1.04m/s is taken. The flow is set parallel to the fins of heat sink. The bottom surface of the MHTS is kept as outlet grill.

5.2.7 Cabinet

The default material for the Icepak is taken as cabinet material and the cabinet is kept tight so that there is no gap between cabinet surface and MHTS.

CHAPTER 6

RESULTS

The experimental model and CFD model were setup to run for total TEC power within the range of 20W to 200W,while varying power in chip resistor from 25W to 75W.Comparision were being made between these two model for validating the results. The Coefficient of Performance for 50W power in chip resistor is calculated using the same CFD model setup.

6.1 Experimental Result

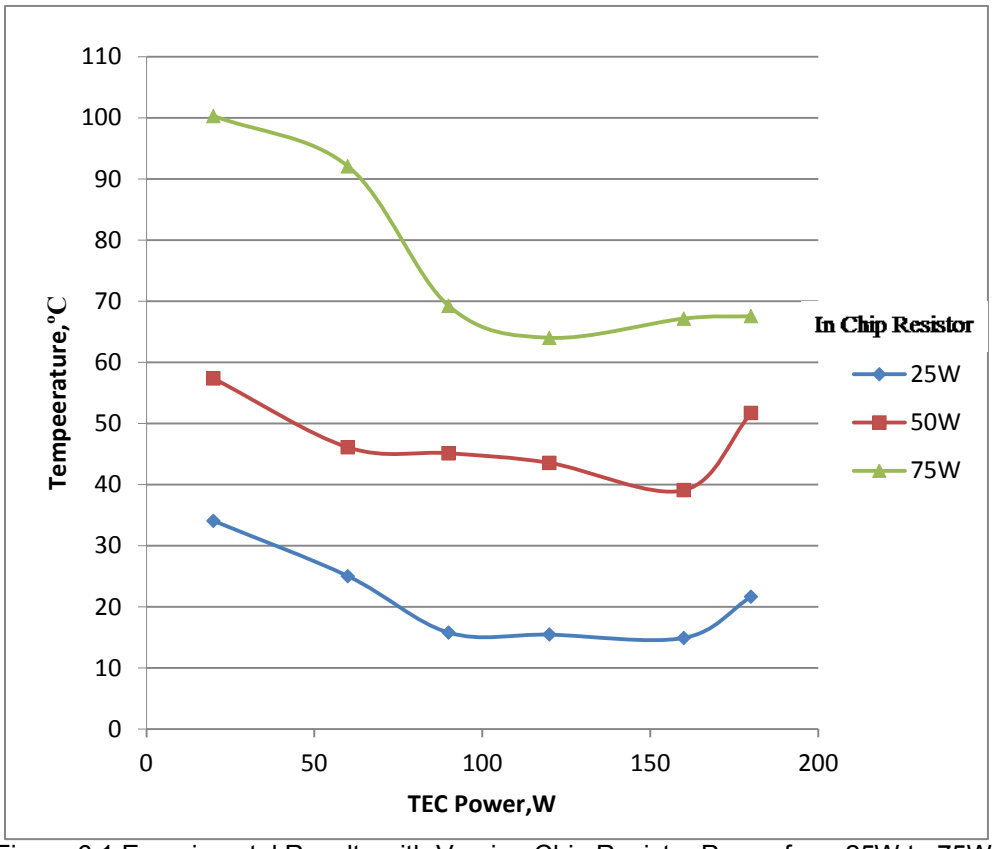

Figure 6.1 Experimental Results with Varying Chip Resistor Power from 25W to 75W.

As seen in figure 6.1, the lowest temperature is recorded at 160W of total power in TEC, when the chip resistor was supplied power of 25W. The documented temperature at this point is 14.9ºC.It can also be seen that MHTS was able to bring temperature below ambient condition from 90W to 160W of total TEC power, with chip resistor power of 25W held constant. The temperature drops initially until certain point after which it starts increasing. This phenomenon is observed because of the Fourier conduction effect and Joule heating effect. The cooling power in TEC is directly proportional to current applied to it. When the current is increased after a certain point, the Peltier cooling effect is overtaken by Fourier and Joule heating effect. Thus, the heat will start penetrating the cold side, decreasing the efficiency of TEC and therefore, the temperature starts rising at chip resistor.

For varying heat load in chip resistor, this point may vary, figures 6.1 and 6.2 (on next page) illustrates the mentioned effect. The lowest temperature for 25W chip resistor power is 14.9ºC with total TEC power of 160W i.e. 40W in each of TEC. For 50W power in chip resistor, its 39.05ºC with also TEC power of 160W. Again, the lowest temperature of 64ºC was recorded when the chip resistor power is 75 W and total TEC power is of 120w.

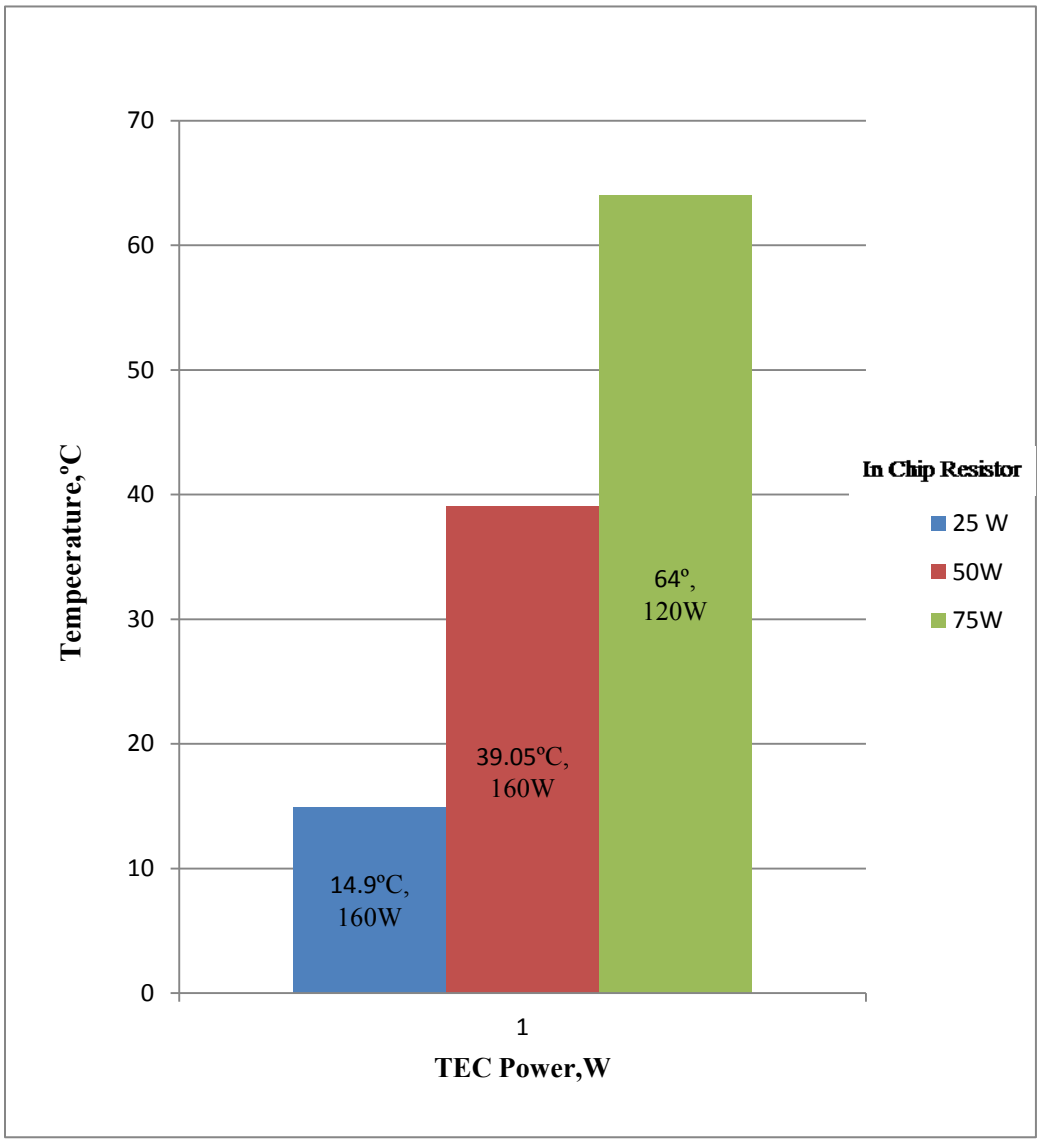

Figure 6.2 Lowest Temperatures in Chip Resistor for Different Power in Chip Resistor.

6.2 Computational Fluid Dynamics Result

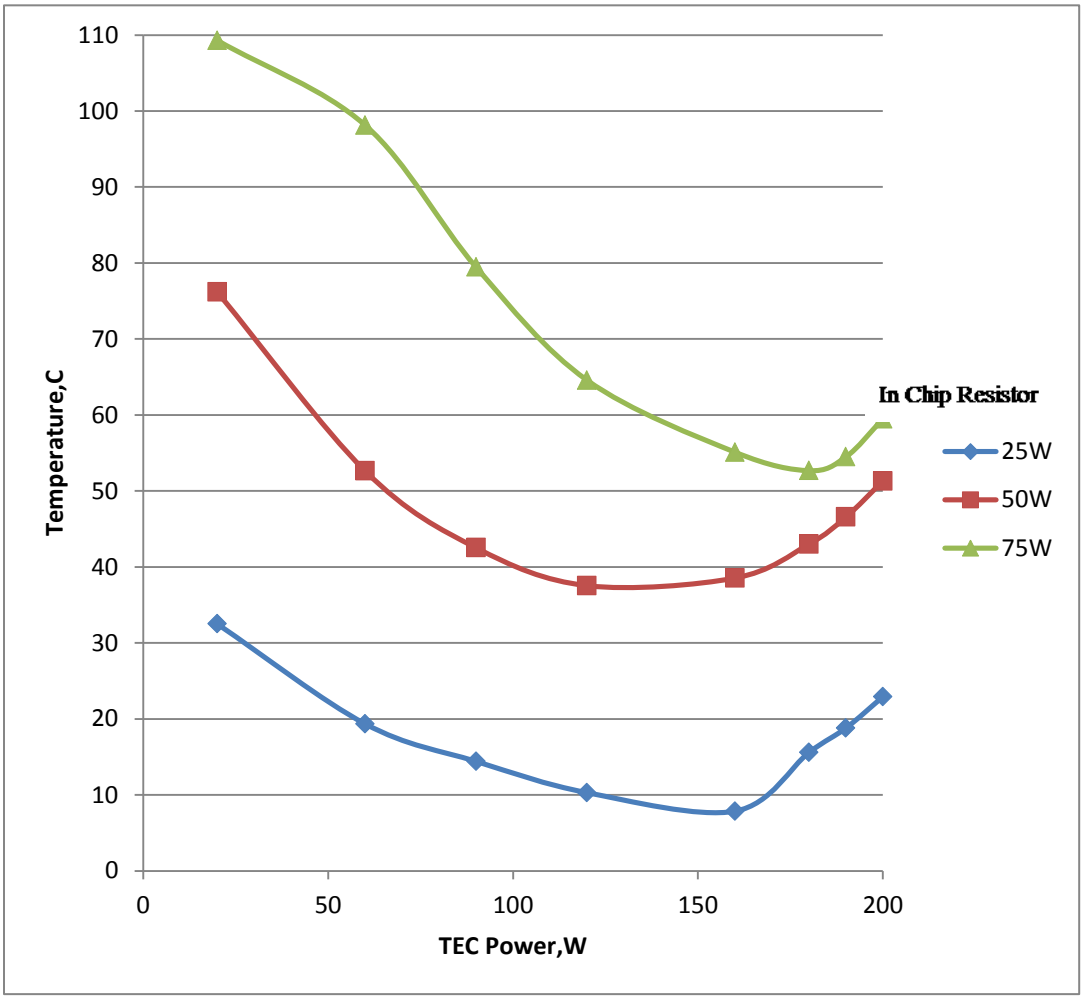

Figure 6.3 CFD Results with Varying Chip Resistor Power from 25W to 75W

In figure 6.3, the corresponding computational results are given. The same temperature effect or phenomenon as shown in experimental result, figure 6.1 is seen. But, the temperature values were different from corresponding experimental results. The temperature graph of experimental model as well as CFD model have similar curve, which confirms that the MHTS constructed for experimental work is working properly. The lowest temperature recorded is 7.85°C in Chip Resistor at power 25W with total TEC power of 160W. Also, the temperature below ambient condition is documented from 60W to 180W of total TEC power at chip resistor

power of 25W. For 25W and 75W chip resistor power, temperature below ambient condition is not recorded.

In figure 6.4, the lowest temperature values for varying chip resistor power are mentioned. The lowest temperature is 7.85ºC for 160W total TEC power n 25W chip resistor power. For 50W chip resistor power, temperature is 37.53ºC for total TEC power of 120W. While for 75W chip resistor power, the lowest temperature is 52.66ºC.

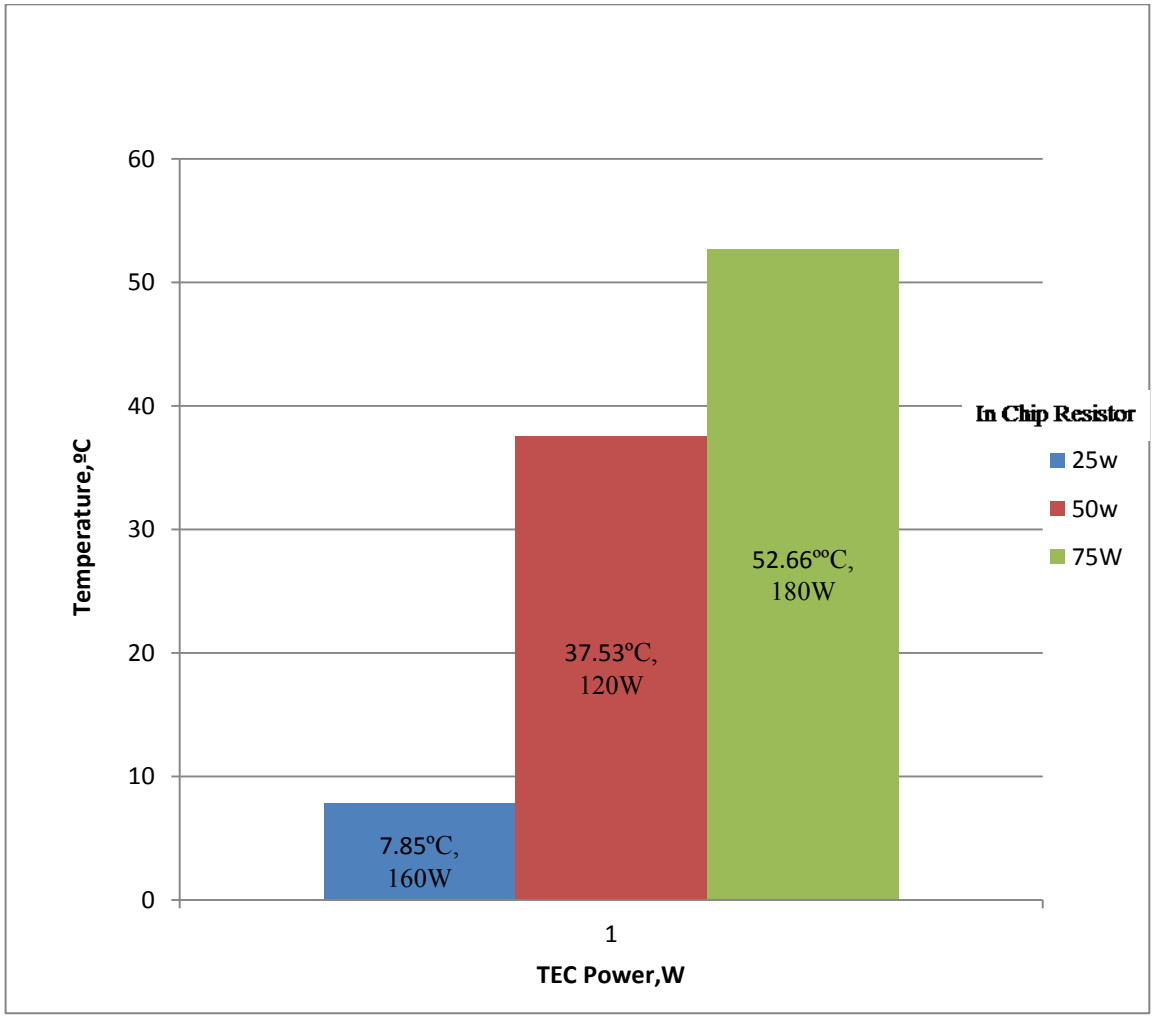

Figure 6.4 Lowest Temperature for Different Power in Chip Resistor

6.3 Comparison of Experimental and CFD Result

The following illustrations Figure 6.5, Figure 6.6 & Figure 6.7 shows the comparison between the experimental result and CFD result at 25W, 50W and 75W respectively. It is found out the corresponding temperature values for experimental results and CFD results are quiet close to each other, which confirms that the CFD model was able to imitate the phenomenon observed while running experimental model. The next step is to find out what percentage error is, to validate both models.

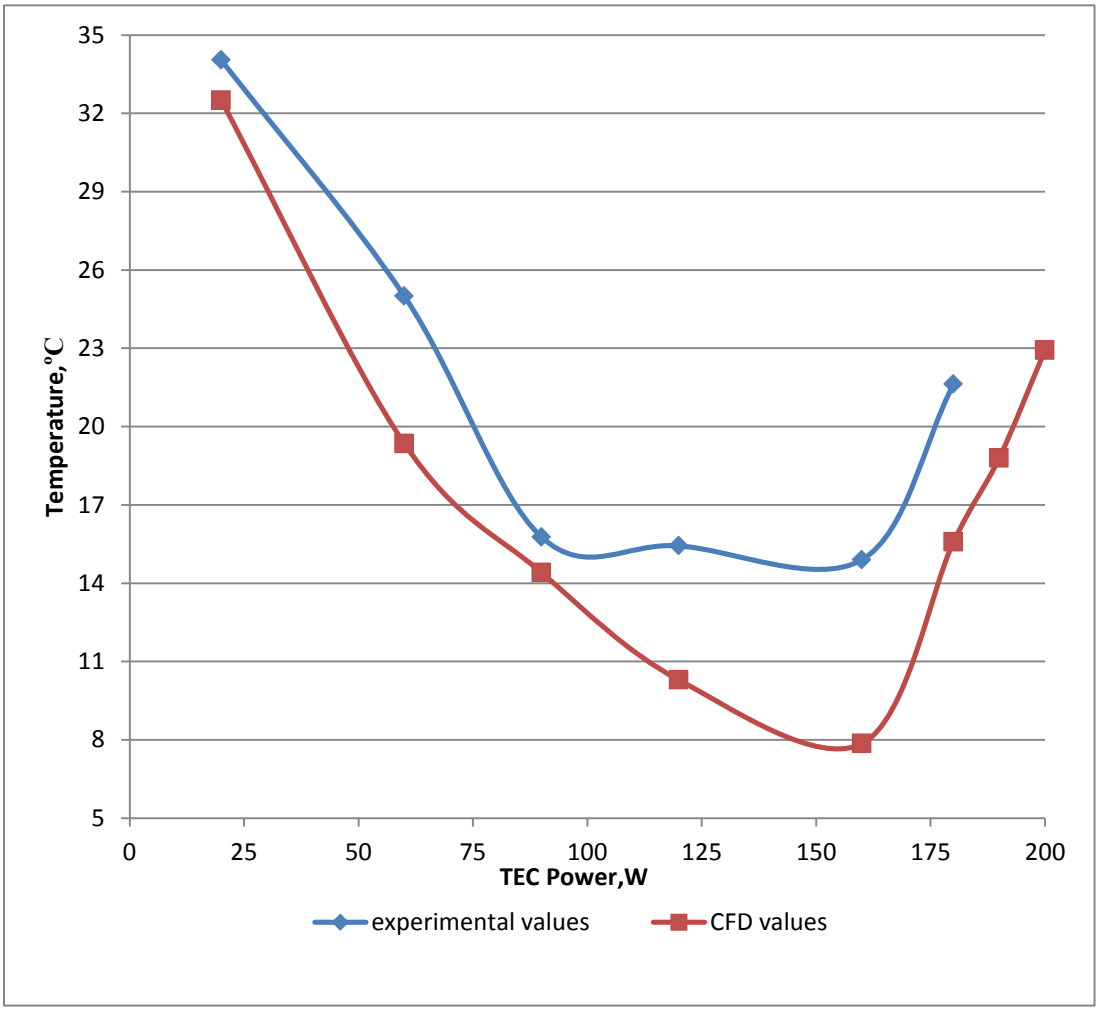

Figure 6.5 Comparison of Experimental and CFD Model for 25W Chip Resistor Power

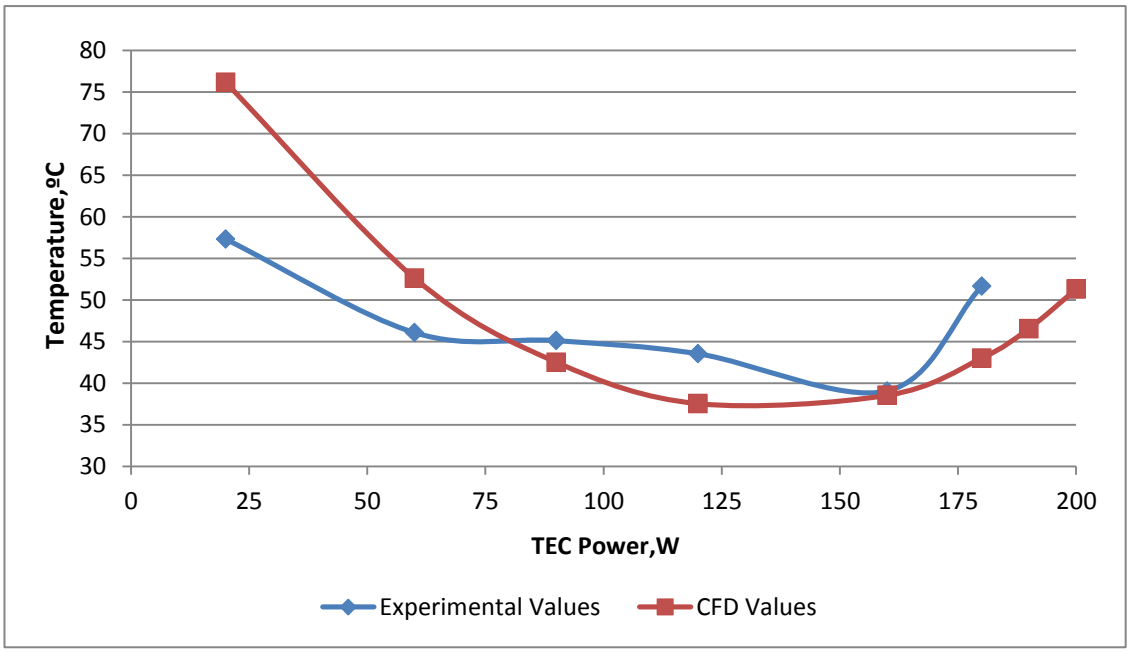

Figure 6.6 Comparison of Experimental and CFD Model for 50W Chip Resistor Power

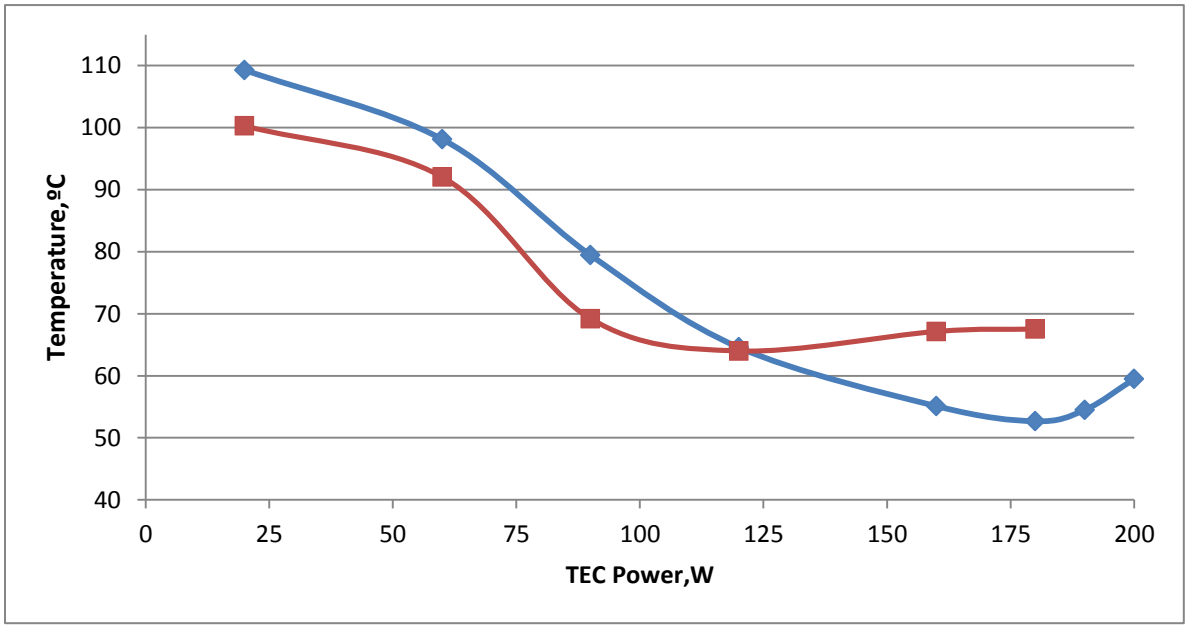

Figure 6.7 Comparison of Experimental and CFD Model for 75W Chip Resistor Power

The percentage error for each corresponding values for the experimental results versus the CFD results was calculated and is given below in figure 6.8. The temperature values are

converted to the Kelvin from degree Celsius in order to achieve more accurate results. The range for percentage error in temperature is between 0% and 11% for all the cases (25W, 50W and 75W TEC power). If we look at the results from the CFD simulations, the percentage error in temperature is about 20% [18]. Also the experimental results show the percentage error in temperature being maximum of 10% [18] which includes thermocouple reading error and contact resistance. This concludes that the model used for the work is appropriate as the percentage error in temperature being maximum of 10.79% which is very close to the CFD simulation results as well as the actual experimental results. Thus, the CFD model is validated with experimental model.

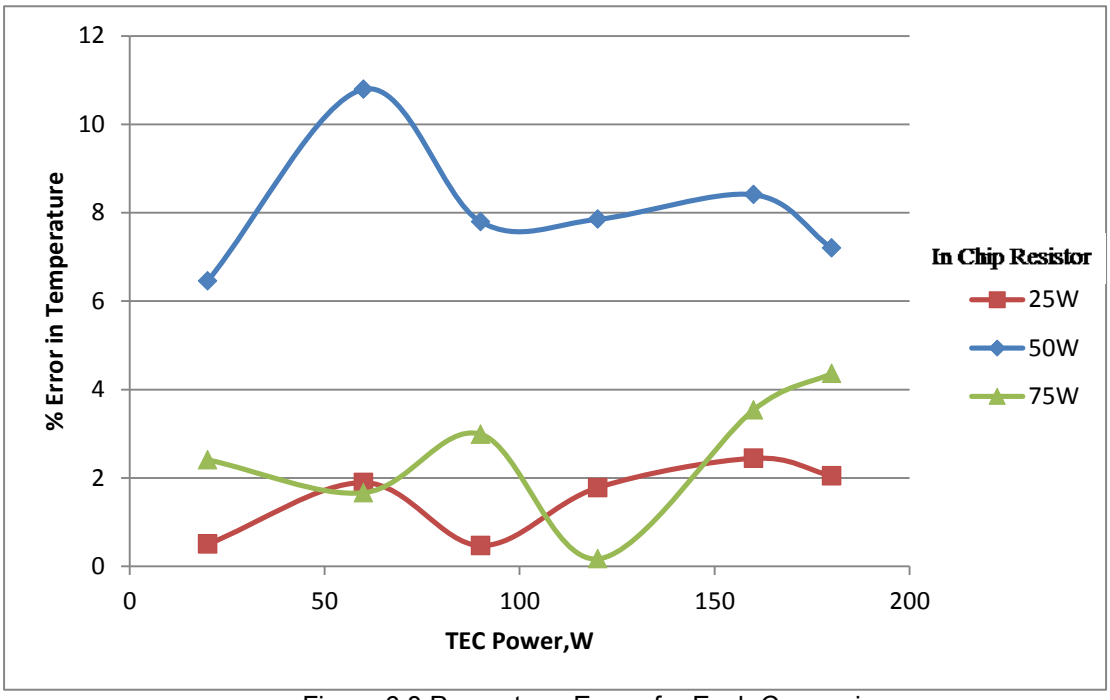

Figure 6.8 Percentage Errors for Each Comparison

Again, one more MHTS model is created in Ansys Icepak without TECs i.e. only heat sinks to compare the efficiency of MHTS apparatus to cool down the chip resistor. The figure 6.9 (next page) marks the temperature recorded at multiple chip resistor power values for MHTS without TECs and MHTS with TECs running at total power of 160W and also values are recorded without any current supplied to the TECs. The lowest temperature is found for MHTS

running at 160W total TECs power, while the highest temperature was found for MHTS with no power supply to the TECs. The reason behind these recorded temperature values is that, in TEC, without the current supplied, the electrons in p and n-type of semiconductors are not able to relocate the heat from cold side to hot side, making it work like thermal insulator. The temperature for MHTS with only heat sinks is found in between other two ran cases because of direct surface contact between copper core and heat sink. As a result, the heat is able to transfer easily from copper core to the heat sink.

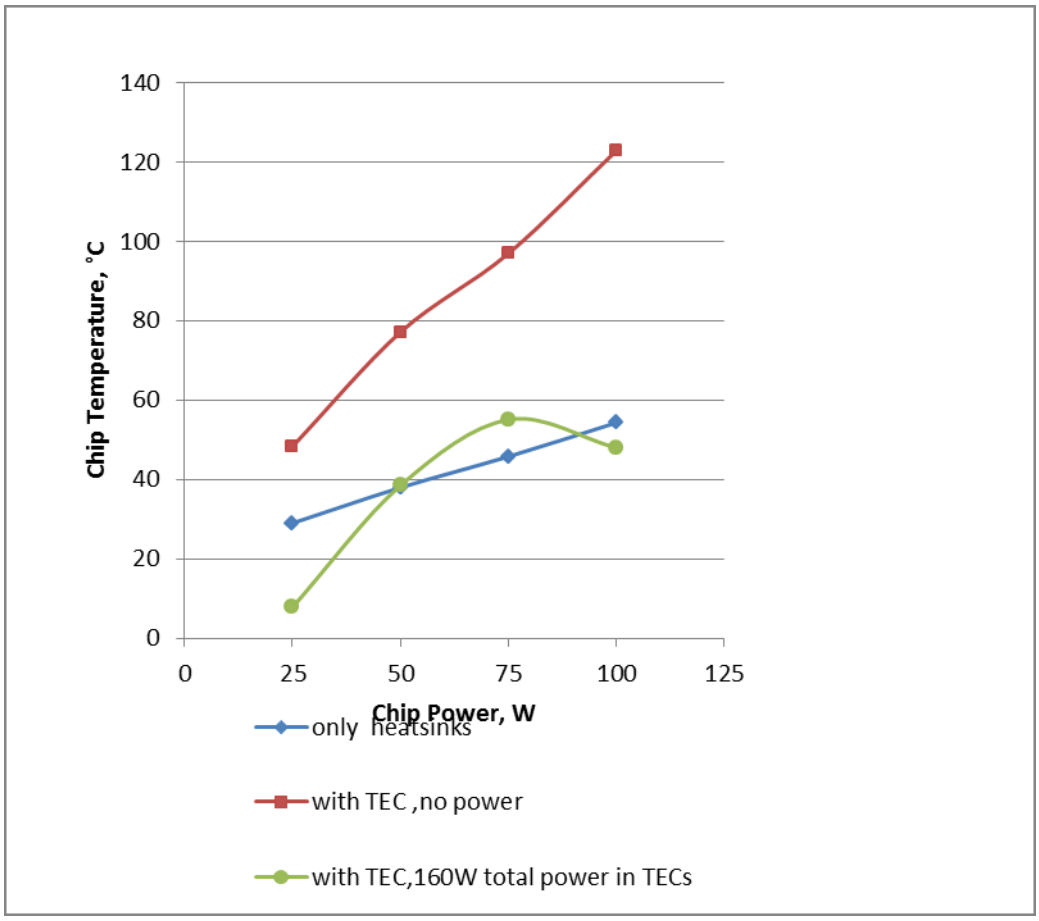

Figure 6.9 Comparisons of MHTS Model for Different Cases

6.4 Coefficient of Performance

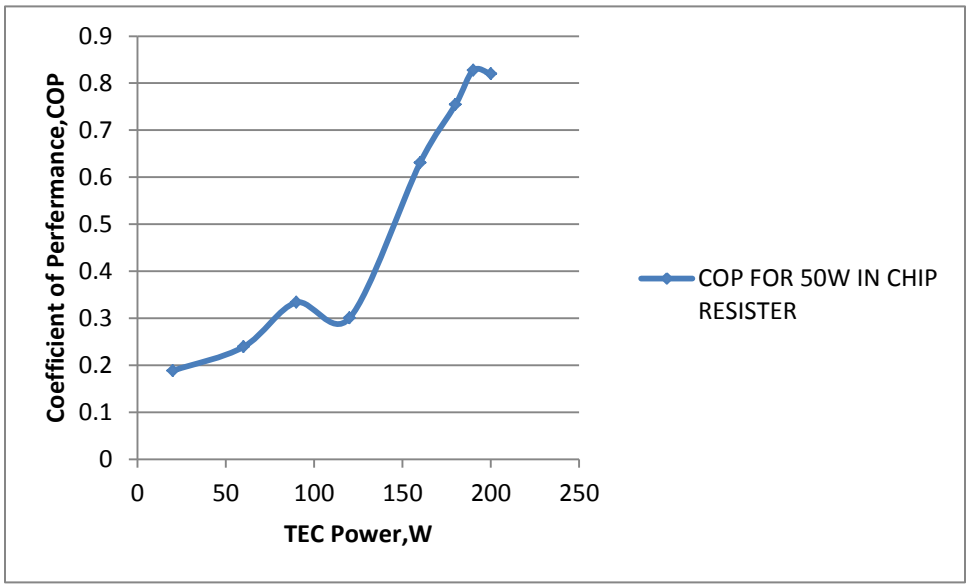

Figure 6.10 Coefficient of Performance for Chip Resistor at 50 W

The coefficient of performance is calculated from the cooling power, q_{net} values recorded at different TECs power in CFD model for chip resistor running at 50W. Figure 6.10 shows the graph of coefficient of performance versus the total power in TECs for 50W chip resistor power. The COP is observed to be increasing until the total power in TEC is reached to 190W after which decrement can be seen. The COP value at this point is calculated as 0.83. This graph proves the typical phenomenon of thermoelectric module that the coefficient of performance will increased in TEC until the current reaches its optimum value. After reaching the optimum value, the COP will start dropping. For this TEC model, CP 1.4-127-10L, the value for optimum current is found out to be 2.59A with maximum q_{net} as 156.54W.

CHAPTER 7

CONCLUSION AND FUTURE WORK

Both the computational model and the experimental model show a similar characteristic of initially lowering of core temperature and as the wattage is increased the Fourier and Joule heating effect overcomes the cooling characteristic resulting in increase in temperature after certain TEC power. This causes the temperature of the core to rise and gives a maximum efficiency range.

7.1 Conclusion

The chip resistor temperature can be effectively reduced to below ambient value, proving that MHTS is a significant improvement over conventional cooling apparatus. For, experimental Model, the lowest temperature was found out at 160W total power in TECs of 14.9ºC for 25 W power in chip resistor while for CFD Model, lowest temperature was found to be 7.85ºC at 160W total TECs power with 25 W in chip resistor. From 50W power in 3D-IC, temperature was noted above ambient temperature. Also, from the graphs in previous chapter, it can be said that the MHTS was not able to cool chip resistor below ambient conditions from 25W chip resistor power onwards.

The percentage error between the experimental and computational models are found to be below 11%, this is an acceptable value for this type of study as errors in the computational model and experimental setup will compound.

Again, MHTS with TECs is able to cool chip resistor more efficiently that without the TECs. The COP in TEC is recorded between 0.18 to 0.83, for 50W chip power. The highest COP was 0.82 for 190W total TECs power with each TEC at 47.5W power. This COP gives optimum current as 2.59A.

7.2 Future Work

From above conducted experiments, it is noted that cooling efficiency of MHTS needs to be increased to bring the temperature of high power devices below ambient condition. Heat sink efficiency can be improved to increase the cooling efficiency of the whole system as it has been shown to be a bottleneck for heat dissipation. Heat pipes or vapor chambers can also be used to increase the cooling efficiency and possibly connect multiple MHTS to increase the total heat dissipation area as illustrated in figure 6.1.

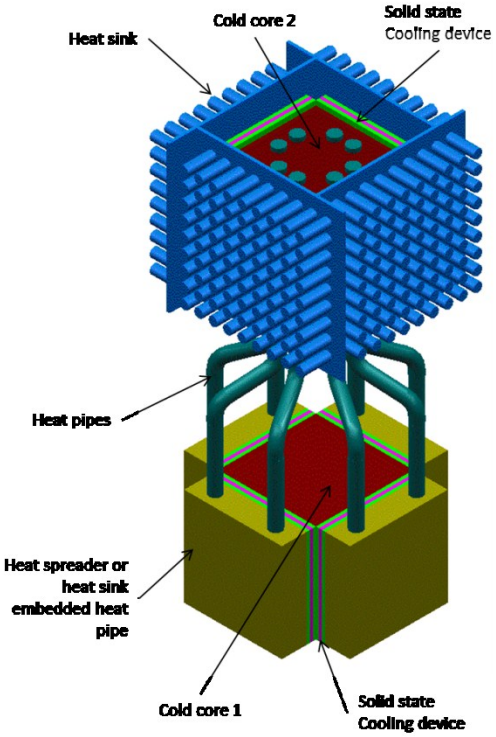

Figure 7.1 Multiple MHTS Connected By Heat Pipes [9]

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BIOGRAPHICAL INFORMATION

Vaidehi Patel was born in 1987 in Mumbai, India. She came to the United States in 2009 as an immigrant. Ms. Patel attended Gujarat University, India in 2004 and graduated with a B.E in Aeronautical Engineering in 2008. Her main research interest is multidimensional sub-ambient cooling of 3D-IC.