PASSIVATION OF Si (100) SURFACE AND FABRICATION OF DOPING-FREE MOSFET

by

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ABSTRACT

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Chalcogen atoms have been successfully used for the passivation of GaAs(100) as well as Ge(100) and Si(100) substrates. Unlike GaAs(100) and Ge(100), the native oxide(SiO_2) of Si(100) substrate is not soluble in ammonium sulfide solution ($(NH_4)_2S_x$) or water, which is a major problem to passivate Si(100) surface in a solution.

In this work, a wet chemical process has been developed in which a compatible etchant ammonium hydroxide (NH_4OH) is added with a passivating solution ($(NH_4)_2S$). Because of the compatibility of the etchant with the passivating solution, native oxide on Si(100) surface is removed in-situ to expose a fresh and clean surface, right before the surface is passivated by the passivating solution. To characterize the passivated surface, Schottky contacts have been fabricated using different work function metals

(Al, Ni, Ti, Cr) on Si(100) substrate. The Schottky diodes were characterized by current-voltage, capacitance-voltage and activation-energy measurements. Due to the passivation of Si dangling bonds by S, surface states are reduced to a great extent and Schottky barriers formed by those metals on Si(100) substrates show greater sensitivity to their respective work functions. S-passivation provided very low barrier height(<0.11 eV) with Al on n-type Si(100) and the highest barrier height(~1.1 eV) with Al on p-type Si(100).

A new doping-free MOSFET structure is also proposed in this work. In this doping-free MOSFET, the high temperature doping step(~1000^{o} C) that is required to form the source/drain contact in a conventional MOSFET is replaced by a more energy efficient passivation technique(maximum ~500^{o} C). The energy dissipated in a high-temperature process is directly proportional to the fourth power of its absolute temperature($\propto T^4$). By reducing the process temperature from 1,000°C to 500°C, the energy consumption can be cut by a significant amount. 2-D device simulations show that the doping-free MOSFET has similar performance characteristics provided by the conventional MOSFET but with the additional advantages of process simplicity and energy savings. Though fabricated devices show a maximum current drive of ~2×10^{-7} A/μm and low on/off ratio, suggestions have been provided to improve the performance characteristics and to achieve ideal characteristics as predicted by the simulation results.

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INTRODUCTION

1.1 Motivation

The stability and reliability of all semiconductor devices are intimately related to their surface conditions. So a good understanding of the semiconductor surface is very significant. This is quite evident in the case of the metal-oxide-semiconductor field-effect transistor (MOSFET), the transport mechanism of which is a surface phenomenon. The first Bipolar Junction Transistor (BJT), the transport mechanism of which is a bulk phenomenon, was built in 1951 [1] prior to the fabrication of a MOSFET. But, the basic concepts underlying the MOS transistor were described by Lilienfeld in the 1920s [1]. Due to the lack of proper understanding of the surface-states, the successful fabrication of the MOSFET was delayed until 1960, when Kahng and Atala demonstrated the first silicon MOSFET [1].

Another device that is badly affected by the semiconductor surface condition is the Schottky diode. In fact, Schottky diode, basically a metal-semiconductor contact, is the first semiconductor device ever studied. Ferdinand Braun (1874) [2] was the first who discovered the asymmetric nature of electrical conduction between metal contacts and semiconductors. But the theory of operation was not understood until 1938 when Walter Schottky suggested that the rectification between a metal and a semiconductor

could arise as a result of a stable space charge in the semiconductor and this structure has become known as the Schottky-barrier diode.

The surface/interface-state is a common problem for semiconductors like GaAs, Ge or InP. Different groups have tried different techniques to passivate these surfaces and to get improved electrical characteristics. Sandroff et al. [3] first applied a chemical treatment using a solution of Na_2S to their GaAs/AlGaAs HBT device and found a 60-fold increase in current gain. Several different groups have used different chemistry for the passivation of a GaAs surface. Carpenter et al. [4] and Besser et al. [5] showed that a treatment with ammonium sulfide ($(NH_4)_2S$) provided more durable passivation than with sodium sulfide treatment. Others have used sodium sulfide and ammonium sulfide solution to passivate a GaAs surface and analyze the modified surface properties [6-10]. Sandroff et al. [11] also showed that a treatment of Na_2Se in NH_4OH solution provided better quality passivation than with Na_2S solution. Then different kinds of selenium solutions like selenium sulfide (SeS_2) [12,13], Se/ NH_4OH solution [14], $(NH_4)_2S$ + Se solution [15] were used to passivate a GaAs substrate. Phosphorus penta sulfide (P_2S_2) solutions [16-18] and sulfur chloride (S_2Cl_2) [19] have also been used. A comprehensive study was done by Bessolov and Lebedev on the chalcogenide passivation of III-V semiconductor surfaces[20]

Passivation of InP(100) [21,22] and Ge(100) [23] surfaces have been done using $(NH_4)_2S$ solution.

One important thing that needs to be mentioned here is that the native oxide of GaAs or Ge is soluble in aqueous solution, which facilitated the successful passivation of those semiconductors while in a solution.

Based on the valence-mending technique, Tao et al. [24, 25] for the first time provided a comprehensive way to passivate the Si(100) surface using precisely one monolayer of Se. They have demonstrated that the Schottky barriers formed on Se-passivated Si(100) surface are very close to the ideal barrier heights [25, 26]. From their experiments it is also found that contact resistance can be reduced to a great extant [27], the high resistance phase of Ni silicide can be suppressed [28, 29] by Se passivation. The stability of Se passivation was analyzed by annealing Schottky contacts on the passivated surface [30] and also by positron annihilation induced Auger electron spectroscopy (PAES) [31]. But in this technique, the passivation has to be carried out in the ultra high vacuum (UHV) Molecular-beam epitaxy (MBE) system. This technique is very expensive, complicated, and provides very low throughput. This is not feasible for mass production.

So far no passivation technique has been reported to passivate a Si(100) surface from a solution (wet-chemical). However this is part of the goal in this work. This technique can be very simple, cost effective, energy efficient, and it can provide very high throughput for mass production. The other part of this work involves the fabrication of a MOSFET with a very energy efficient process. In order to understand the significance of this new device, a brief description of the fabrication process of a conventional MOSFET is provided here.

Among the field-effect devices, the metal-oxide-semiconductor field-effect transistor (MOSFET) is the most popular and widely used. Since the fabrication of the first MOSFET in 1960 by Atalla and Kahng, numerous types of MOSFET structures have been developed to meet different kinds of requirements and performance criteria [32]. Figure 1.1 shows a conventional n-channel enhancement type MOSFET. This is

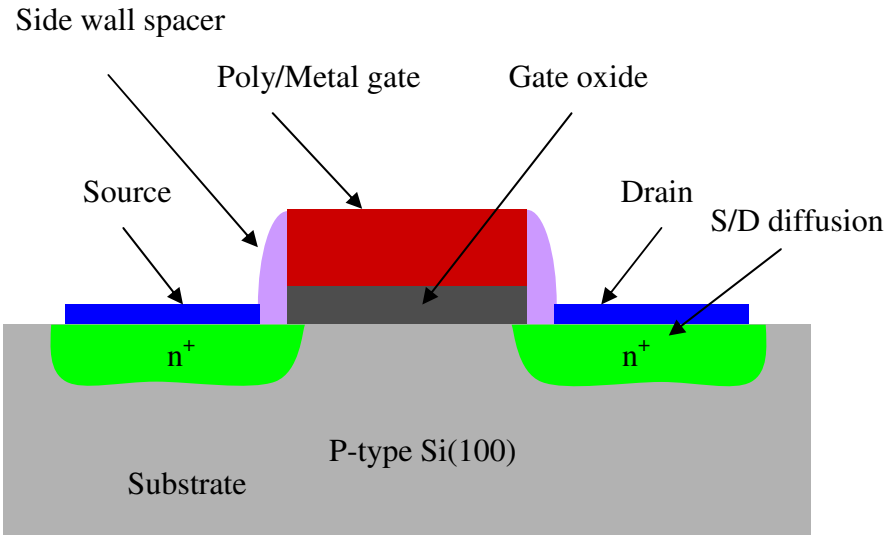


Figure 1.1 Schematic of an n-channel enhancement type conventional MOSFET

basically a four- terminal device and the terminals are source, drain, gate and substrate.

To fabricate this kind of MOSFET, first the gate oxide is formed at ~1000^{o} C by thermal oxidation on a clean Si(100) surface. Then a metal or polysilicon is deposited on top of the oxide to work as the gate electrode. Using a photolithography step, the gate is patterned. Then a thin conformal layer of oxide or nitride is deposited using chemical vapor deposition (CVD). The temperature in this step is around 300^{o} to 350^{o} C. Using an anisotropic etching, the side-wall spacer is formed. This side-wall spacer

separates the gate from the source and drain in the later steps. Now, a high temperature step is needed to dope the source/drain region in which a p-n junction is formed in the source and the drain region. This p-n junction paves the way to make very low resistance path to the inversion layer channel and very high resistance path to the body with the S/D contacts. This doping step is done either by diffusion or by ion implantation followed by annealing. This doping process takes place at a very high temperature (~1000^{o} C -1200^{o} C) for a significant amount of time depending on the process requirements. After the doping process is completed, metal is deposited on the whole area to form source and drain contact. At this point, a high temperature anneal is done to form metal silicide in the S/D region. Using a suitable etchant, the unreacted metal is etched away from all over the surface, while the metal silicide is left on the S/D contacts. Thus the source/drain contacts are formed.

The energy dissipated in a high-temperature process is directly proportional to the fourth power of its absolute temperature ($\propto T^4$) [33]. By reducing the process temperature from 1,000°C to 500°C, the energy consumption can be cut by a significant amount. The high-temperature processes in the manufacture of discrete Si devices like that in Fig. 1.1 or a p-n junction diode include doping, oxidation, annealing, and epitaxy. The temperature involved in these processes is typically ~1,000°C for a period of seconds to minutes. Major efforts have been invested in reducing the high temperature involved in these processes. The temperature for dry oxidation of silicon can be reduced from ~1000^{o} C to 500^{o} C by using ozone (O_3), instead of oxygen (O_2)

[34]. Silicon epitaxy has been achieved by ultrahigh vacuum CVD with SiH_4 as the precursor below 500^o C [35].

Currently there is no low-temperature alternative available for diffusion or annealing for the purpose of doping. Doping is required to control the electrical properties of Si for device operation and performance. One way to reduce the temperature involved in diffusion and annealing for doping is to control the electrical properties of Si without doping.

In this work, first a passivation technique has been developed and demonstrated to passivate the dangling bonds of Si(100) surface from a solution. This passivation technique is then integrated to replace the high-temperature doping step in the S/D region to fabricate a new energy efficient, low-temperature and doping-free MOSFET.

1.2 Organization of this Document

Chapter 2 provides an overview of the metal-semiconductor contact, surface-state, determination of barrier height and design procedure of a Schottky diode. The design procedure also provides different techniques to reduce the edge effects. The applications of Schottky diode are also presented here.

Chapter 3 briefly explains the "Valence-Mending Concept" and using this technique, it provides the procedure to passivate Si(100) surface from a solution. It also provides the experiments to optimize the parameters to get good quality passivation.

Chapter 4 shows the electrical characterization of S-passivated Si(100) surface by depositing different work function metals. It also provides a comparison with the non-passivated samples. Finally it briefly explains the "Surface-Dipole" phenomenon

and how much it affects the Schottky barrier height in comparison to the “Surface-States”.

Chapter 5 first explains the operating principle of a conventional MOSFET. It then explains the concept for the fabrication of doping-free p-n junction utilizing the passivation technique. It then provides the process flow and detailed description of the fabrication steps for the fabrication of doping-free MOSFET.

Chapter 6 provides a 2-D numerical process and device simulations of the MOSFET using TSUPREM4 and MEDICI. It also provides a comparison between the simulated results and the experimental results.

Chapter 7 summarizes the whole work and provides direction for future work.

CHAPTER 2

METAL-SEMICONDUCTOR CONTACT

2.1 Introduction

The Metal-semiconductor contact is the earliest and simplest device to be fabricated. But to get the ideal characteristics, things get quite complicated. In this section, a brief description of metal-semiconductor contact, carrier transport mechanism, design procedure and applications are provided.

2.2 Ideal Metal-Semiconductor Contact

When a metal makes intimate contact with a semiconductor, a barrier is formed at the metal-semiconductor interface. The formation of a metal-semiconductor contact can be best explained by drawing its energy band diagram. Figure 2.1(a) shows the energy band diagram of a metal and an n-type semiconductor at the instant the contact is made. At this point, the electrons in the semiconductor have higher potential energy than the electrons in the metal. So electrons in the semiconductor will transfer to the metal to establish thermal equilibrium. At thermal equilibrium, the Fermi levels in the metal and semiconductor must be equal, and the vacuum level must be continuous. These two requirements determine a unique energy-band diagram as shown in figure 2.1(b). The Barrier height of such contact is defined as the difference between the metal work function and the electron affinity of the semiconductor, which is given by [32]

$$q\phi_{Bn} = q(\phi_m - \chi_S) \tag{2.1}$$

where Φ_m denotes the metal work function, χ_s is the electron affinity of the semiconductor and q is the electron charge. The parameter Φ_{Bn} describes the barrier for

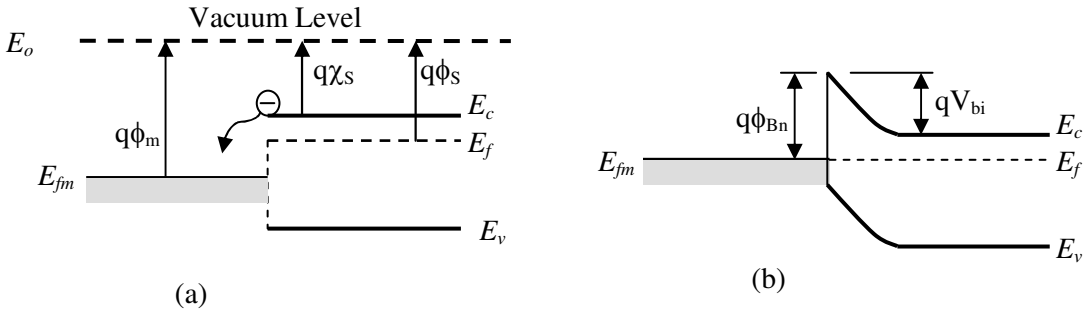


Figure 2.1 Band diagram of metal and n-type semiconductor (a) just after contact, (b) at thermal equilibrium.

the flow of electrons from the metal to the semiconductor. For the flow of electrons from the semiconductor to the metal, the barrier height is given by

$$qV_{bi} = q\phi_{Bn} - (E_C - E_f) \tag{2.2}$$

where E_C denotes the energy level of the lower conduction band edge and E_F is the Fermi level. The quantity V_{bi} is known as the built-in or diffusion potential. Although it is usually attributed to Schottky, equation (2.1) was first stated implicitly by Mott (1938) and is referred to as Schottky-Mott limit [2]. Figure 2.2 shows the energy band diagram of a metal and p-type semiconductor contact. For an ideal contact between a metal and a p-type semiconductor, the barrier height is given by [32]

$$q\phi_{Bp} = E_g - q(\phi_m - \chi_S) \tag{2.3}$$

where E_g is the energy band gap of the semiconductor and Φ_{Bp} is the barrier for the flow of holes from the metal to the semiconductor.

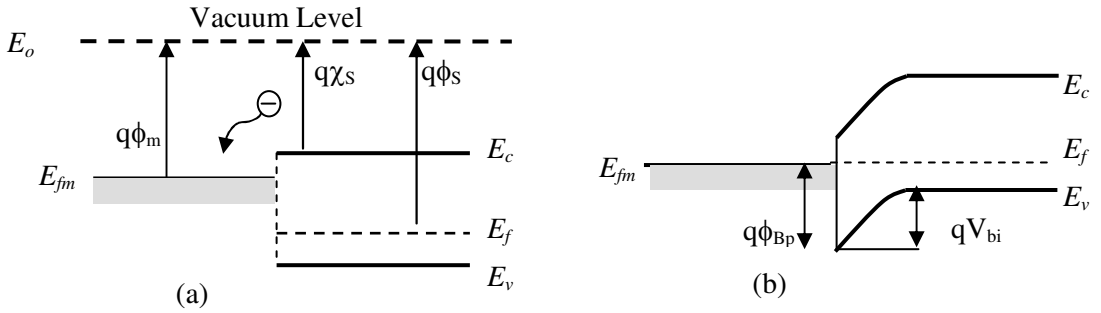


Figure 2.2 Band diagram of metal and p-type semiconductor (a) just after contact, (b) at thermal equilibrium

In practical metal-semiconductor contacts, the ideal barrier heights as given by the equations (2.1) and (2.3) are never achieved [2, 32]. Experimentally it is found that the barrier height is a less sensitive function of Φ_m and under certain circumstances Φ_B is almost independent of the choice of metal.

2.3 Schottky Barrier in Presence of Surface-States

An explanation of this weak dependence of barrier height on Φ_m was put forward by Bardeen (1947) [36]. He suggested that the discrepancy might be due to the effect of surface states. The surface states can occur either from the termination of the periodic structure of the semiconductor crystal at the surface or from the presence of the adsorbed foreign atoms on the surface. Due to these high surface and interface states,

the surface Fermi level of the semiconductor gets pinned at a certain position. So when metal is deposited on this surface, the barrier height no longer depends on that metal work function. Mead and Spitzer(1964) [37] summarized all the data available that time, which included 14 different semiconductors and found that almost all of them exhibited a Fermi-level at the interface fixed very close to $E_g/3$ from the valence band-edge.

Consider the Si(100) surface, where each surface atom has two broken bonds [Figure 2.3(a)]. In ultra high vacuum this surface undergoes reconstruction to minimize its surface energy and thus forms a dimmer bond with the neighboring atom [25]. Figure 2.3(b) shows the atomic structure of Si(100) in ultra high vacuum after they undergo reconstruction. So each surface atom is left with a dangling bond and shares a dimmer bond with the neighboring atom. These dangling bonds give rise to high surface states which pin the surface Fermi level. When metal is deposited on this surface, the interface Fermi level is pinned rendering the Schottky barrier independent of the metal

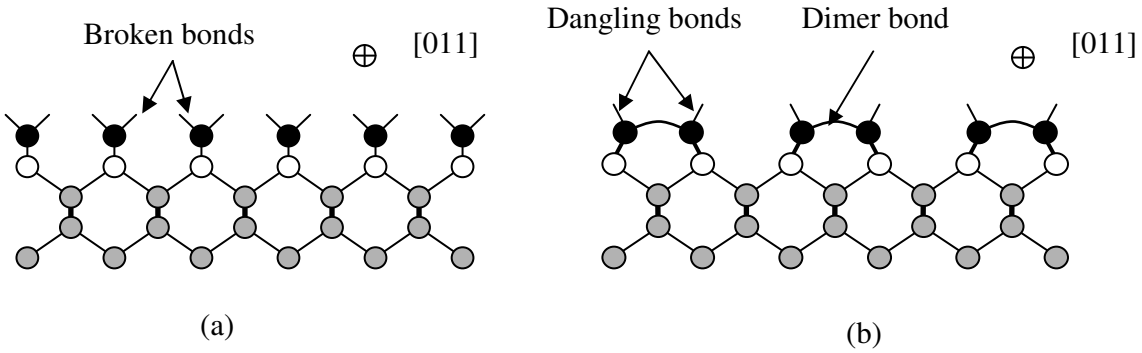


Figure 2.3 Side view into the [011] direction of Si(100) surface (a) before reconstruction, (b) after reconstruction in UHV.

work function. Table 2.1 lists some of the reported barrier heights along with the corresponding ideal barrier height according to Schottky-Mott theory for a comparison purpose [32]. From Table 2.1, it can be see that other than gold (Au), the barrier heights of different metals on n- and p-type Si(100) are way off their ideal values. In fact, though the metals have different work function values, their barrier heights are very close to each other.

Table 2.1 Ideal and measured Schottky barrier heights on n-and p-type Si (eV at 300 K)

Metal	Work Function (Φ_m)	n-type Si(100)		p-type Si(100)	
		Ideal Φ_{Bn}	Measured Φ_{Bn}	Ideal Φ_{Bp}	Measured Φ_{Bp}
Al	4.28	-0.01	0.72	1.13	0.58
Ti	4.33	0.04	0.50	1.08	0.61
Cr	4.50	0.21	0.61	0.91	0.50
W	4.55	0.26	0.67	0.86	0.45
Mo	4.60	0.31	0.68	0.81	0.42
Cu	4.65	0.36	0.58	0.76	0.46
Au	5.10	0.81	0.80	0.31	0.34
Ni	5.15	0.86	0.61	0.26	0.51

The barrier height as provided by Schottky and Mott was never found in practical metal-semiconductor contacts. Based on the Bardeen's theory, the dependence of the barrier height on metal work function, surface states and the thickness of the interfacial layer is provided here which was first derived by Cowley and Sze [38]. The energy band diagram of a metal-n-type semiconductor as shown in Fig. 2.4 is used in deriving the relation.

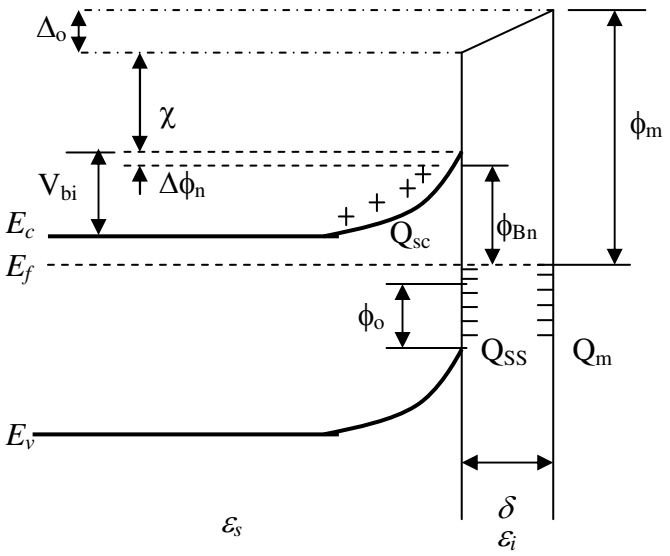


Figure 2.4 Energy-band diagram of a metal-n-type semiconductor contact with an interfacial layer.

In Fig. 2.4, $\Delta\phi_n$ is the image force barrier lowering, Δ_0 the potential across the interfacial layer, δ the thickness of the interfacial layer, ϕ_0 specifies the level below which all surface states must be filled for charge neutrality at the semiconductor surface, Q_{SC} the space-charge density in the semiconductor, Q_{SS} the surface state charge density in semiconductor and Q_m the surface charge density on the metal.

The relationship is given as [38]

$$\varphi_{Bn} = \gamma(\varphi_m - \chi) + (1-\gamma)(E_g - \varphi_0) - \Delta\varphi_n \tag{2.4}$$

where γ is a constant defined as

$$\gamma = \varepsilon_i / (\varepsilon_i + eD_S\delta) \tag{2.5}$$

and where D_S is the density of surface states, ε_i is the permittivity of the interfacial layer. Now it is seen that when $D_S \to 0$, $\gamma \to 1$, and equation (2.4) reduces to

$$\varphi_{Bn} = (\varphi_m - \chi) - \Delta\varphi_n \tag{2.6}$$

This is known as the Schottky-Mott limit. When $D_S \to \infty$, $\gamma \to 0$, and equation (2.4) reduces to

$$\varphi_{Bn} = (E_g - \varphi_0) - \Delta\varphi_n \tag{2.7}$$

This is known as the Bardeen limit.

So if the density of surface-states is too high, it effectively makes the barrier height independent of the metal work function. But if the surface-states can be removed, it is possible to get metal-dependent barrier height.

2.4 Carrier Transport Mechanism

The current transport mechanism in metal-semiconductor is mainly due to majority carriers. Figure 2.5 shows the four basic transport processes under forward bias condition. In Fig. 2.5, (1) shows the transport of electrons from the semiconductor over the potential barrier into the metal, which is the dominant transport process for Schottky contact with moderately doped semiconductors (for Si with $N_d \leq 10^{17}$ cm^{-3}), (2) shows quantum-mechanical tunneling of electrons through the barrier, which is dominant in heavily doped semiconductors, (3) shows recombination in the space-charge region and (4) shows hole injection from the metal to the semiconductor. In addition, there may be some edge leakage current due to high electric field at the contact periphery or interface current due to traps at the metal semiconductor interface.

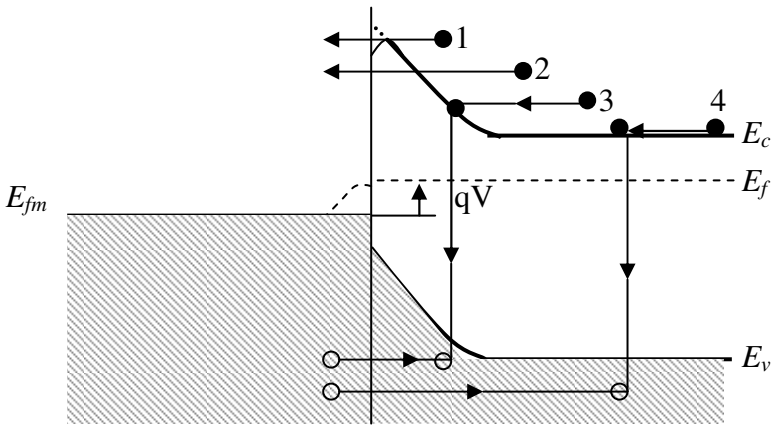


Figure 2.5 Four basic transport processes under forward bias

Below three important transport mechanisms are discussed.

(i) Thermionic Emission Theory

Thermionic emission theory, proposed by Bethe [32], is the dominant transport mechanism for Schottky contact with moderately doped semiconductor. The theory was derived with the following assumptions:

(i) The barrier height $q\Phi_{Bn}$ is much larger than kT

(ii) Thermal equilibrium is established at plane that determines emission

(iii) The existence of a net current flow does not affect this equilibrium, so that the two current fluxes-one from metal to semiconductor, the other from semiconductor to metal, can be superimposed.

Therefore, the total current density can be written as [32]

$$J = J_S[\exp(\frac{qV_a}{nkT}) - 1] \tag{2.8}$$

where I_S is the saturation current, V_a is the applied voltage across the junction, q is the electron charge, k is the Boltzmann constant, T is the temperature and n is the ideality factor. The ideality factor (n) is defined as

$$n \equiv \frac{q}{kT}\frac{\partial V_a}{\partial(\ln J)} \tag{2.9}$$

The saturation current density (J_S) can be represented as

$$J_S = A^* T^2 \exp(-\frac{q\phi_{Bn}}{kT}) \tag{2.10}$$

where A^* is the Richardson constant, ϕ_{Bn} is the barrier height. The Richardson constant is expressed as

$$A^* = \frac{4\pi q m^* k^2}{h^3} \tag{2.11}$$

where m^* is the effective mass, k is the Boltzmann constant and h is the Planck constant.

An advanced form of the thermionic emission theory was proposed by Crowell and Sze, which takes care of the quantum mechanical tunneling and reflection at the barrier and J_S is modified in the following way

$$J_S = A^{**} T^2 \exp(-\frac{q\phi_{Bn}}{kT}) \tag{2.12}$$

where A^{**} is the effective Richardson constant and is given by [32]

$$A^{**} = \frac{f_p f_q A^*}{1 + f_p f_q v_R v_D} \tag{2.13}$$

where f_p is the probability of electron emission over the potential maximum and f_q is the ratio of the total current flow, considering the quantum mechanical tunneling and reflection, to the current flow neglecting these effects.

(ii) Field and Thermionic-Field Emission

For a heavily doped semiconductor and/or for operation at low temperatures, the tunneling current may become the dominant transport process. In that case, thermionic-field and field emission come into play. Thermionic (thermal assisted) field emission

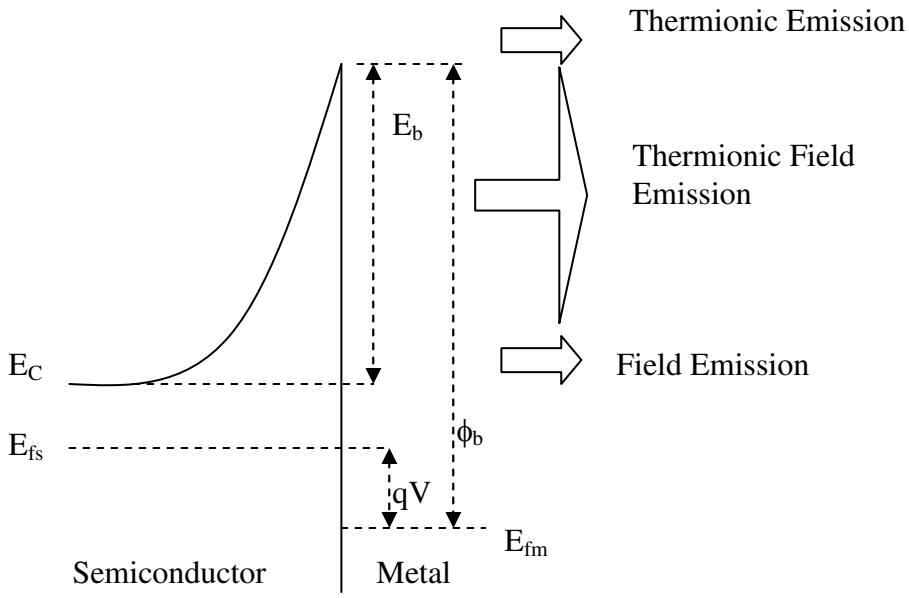


Figure 2.6 The energy ranges for three types of transport mechanism in an n-type semiconductor.

dominates the transport when carriers have enough thermal energy to tunnel through a portion of a barrier near the top but not enough to reach the top and be emitted over it. At cryogenic temperature, the thermal energy of carriers is negligible and the transport is dominated by pure tunneling, which is the pure field emission. Figure 2.6

schematically shows the three transport mechanism in an n-type semiconductor. Padovani [39,40], Crowell [41] and Rideout [42] have provided a detailed analysis on these transport mechanism. Crowell and Rideout [41] have provided a smooth transition from thermionic to thermionic-field and to pure field emission. In high temperature and low doping range, where $kT/E_{00} >> 1$, thermionic emission dominates and for high doping and low temperature, where $kT/E_{00} << 1$, field emission dominates. Here k is the Boltzmann constant, T is the absolute temperature and E_{00} is a constant of the material, which is defined as [41]

$$E_{00} = 18.5 \times 10^{-12} \left[\frac{N}{m_r \varepsilon_r} \right]^{1/2} eV \qquad (2.14)$$

where m_r is the tunneling effective mass, N the impurity concentration and ε_r the static dielectric constant.

2.5 Determination of Barrier Height

The barrier height of a Schottky contact is a very important parameter. So, different groups [39-51] have used different methods to determine the barrier height with their relative advantages and disadvantages. Below, three widely used methods are discussed.

2.5.1 I-V Measurement

For moderately doped semiconductor, the current transport mechanism in metal semiconductor contact is governed by the thermionic emission theory. So in terms of total current, equation 2.8 can be written as

$$I = I_S[\exp(\frac{qV_a}{nkT}) - 1] \tag{2.15}$$

where I_S is the saturation current and the other notations are already defined. The saturation current (I_S) can be represented as

$$I_S = AA^{**}T^2 \exp(-\frac{q\phi_{B0}}{kT}) \tag{2.16}$$

where A is the area of the contact. If the substrate resistance is negligible, the saturation current can be determined by extrapolating the forward current (I_F) at zero voltage and the Schottky barrier can be obtained as

$$\phi_{BO} = \frac{kT}{q}\ln\left(\frac{AA^{**}T^2}{I_S}\right) \tag{2.17}$$

But if the substrate resistance is not negligible, the barrier height cannot be determined as mentioned above. In this case equations 2.15 & 2.16 can be combined and the effect of substrate resistance can be included as

$$I = AA^{**}T^2 e^{-\phi_{BO}\frac{q}{kT}}(e^{\frac{q}{nkT}(V-IR)} - 1) \tag{2.18}$$

where R is the substrate resistance. One way to extract the barrier height in this case is to fit this equation with the experimental data and get the barrier height.

2.5.2 Activation Energy Measurement

In activation-energy measurements, the barrier height is determined from the temperature-dependent reverse saturation current (I_S). With some rearrangements and taking log on both sides of equation 2.16, we get

$$\ln(\frac{I_S}{T^2}) = -\frac{1}{T}\frac{q}{k}\phi_B + \ln(AA^{**}) \tag{2.19}$$

A plot of $\ln(I_S/T^2)$ vs. 1/T gives a straight line and the barrier height is calculated from the slope [45]

$$Slope = -\frac{q}{k}\phi_B \tag{2.20}$$

The advantage of this method is that, with a sufficiently large reverse voltage, the effect of the high series resistance can be minimized and also in activation energy measurement, no assumption of electrically active area is required. Also from the intercept on the y-axis, the effective Richardson constant (A^{**}) can be determined.

In activation-energy measurements, the barrier height can also be determined from the forward characteristics as follows [32]

$$\ln(\frac{I_F}{T^2}) = \ln(AA^{**}) - q(\phi_B - V_F)/kT \tag{2.21}$$

where V_F and I_F are the forward voltage and current. The rest of the procedure is the same. But if the series resistance is high, it will introduce error in the barrier height measurement.

2.5.3 C-V Measurement

In C-V measurements, a small ac voltage is superimposed on a dc bias. So charges of one sign are induced on the metal surface and charges of the opposite sign are induced in the semiconductor. The differential depletion capacitance can be written as [32]

$$C = \left| \frac{\partial Q_{SC}}{\partial V} \right| = \sqrt{\frac{q\varepsilon_s N_D}{2(V_i - V - kT/q}} \tag{2.22}$$

From this equation a couple of important relations can be obtained. By squaring Eq. 2.22 we can obtain

$$\frac{1}{C^2} = \frac{2(V_i - V - kT/q)}{q\varepsilon_s N_D} \tag{2.23}$$

From Eq. 2.23, doping concentration can be derived as [32]

$$N_D = \frac{2}{q\varepsilon_s}\left[-\frac{1}{d(1/C^2)/dV} \right] \tag{2.24}$$

If N_d is constant through the depletion region, a plot of $1/C^2$ versus V will provide a straight line and the doping concentration can be determined from the slope and the barrier height can be calculated as [32]

$$\phi_B = V_i + V_n + \frac{kT}{q} - \Delta\phi \tag{2.25}$$

where V_i is the intercept on the voltage axis from the $1/C^2$-vs.-V plot, V_n is the difference between conduction band and Fermi level for n-type Si(100) and $\Delta\phi$ is the amount of Schottky barrier lowering due to image force.

The Schottky barrier lowering ($\Delta\phi$) is defined as [32]

$$\Delta\phi = \sqrt{\frac{q\xi}{4\pi\varepsilon_S}} \tag{2.26}$$

where ξ is the electric field and ε_s is the appropriate permittivity characterizing the semiconductor medium.

2.6 Design Procedure of Schottky Rectifier

In this section a simple design procedure is provided for a medium voltage Schottky rectifier. The main device design variables, which affect Schottky rectifier characteristics are the contact metal work function, the epilayer doping, the epilayer thickness and the junction edge termination.

The break down voltage of a Schottky rectifier depends on the semiconductor critical field, epilayer doping, epilayer thickness and the junction edge termination technique. The critical field of a certain semiconductor is pretty much fixed. So the breakdown voltage can be used to determine the optimal epilayer doping and thickness under parallel plane avalanche breakdown conditions. The desired epilayer doping is the maximum doping which will sustain the specified breakdown voltage. The relationship for the epilayer doping is [52]

$$N_D = \frac{\varepsilon_s E_{CR}^2}{2qV_B} \tag{2.27}$$

where E_{CR} is the semiconductor critical field and V_B is the breakdown voltage.

The corresponding epilayer thickness is the reverse bias depletion width at the breakdown voltage, which is defined as [52]

$$t_{epi} = \frac{2V_B}{E_{CR}} \tag{2.28}$$

where t_{epi} is epilayer thickness.

2.7 Methods of Avoiding Edge Effects

The break down voltage discussed so far is for parallel plane junction, which is not observed in the fabricated diode unless some junction termination techniques are applied to avoid the edge effect. Significant efforts [53-63] have been taken to understand the edge effect and to develop methods to get rid of it as much as possible. The field crowding caused by the sharp edge around the periphery of the metal plate reduces the breakdown voltage than the rated parallel plane breakdown voltage. To eliminate this effect, different kinds of edge termination techniques have been developed. To get a clear view of the electric field distribution at different regions of the metal semiconductor contact, a 2-D MEDICI simulation is performed. Figure 2.7 (a) shows a Schottky diode structure without any edge termination technique and Fig. 2.7 (b) shows the electric field magnitude along the interface. From figure 2.7, it is observed that the electric field is maximum ($>1x10^6$ V/cm) at the edge of metal contact with silicon, which is well above the break down field for silicon ($\sim 3x10^5$ V/cm). So at that reverse voltage, break down will initiate at the metal edge even before it reaches 50 volts. Below some of the edge termination techniques are discussed.

(i) Metal overlay structure: This is the simplest edge termination technique. In this method, a certain thickness of oxide layer is left all around the Schottky contact and the Schottky metal is extended over the oxide region for a certain distance. Figure 2.8 (a) shows the Schottky diode with the metal overlay structure and Fig. 2.8 (b) shows the electric field magnitude along the interface of silicon and oxide/metal. It is seen from the simulation that the maximum field is now reduced to some extant ($<6x10^5$ V/cm),

but it is still higher than that of the middle portion of the contact. The electric field can be further reduced by adjusting the oxide thickness, which is shown in Fig. 2.9. The maximum electric field is still higher than the middle region.

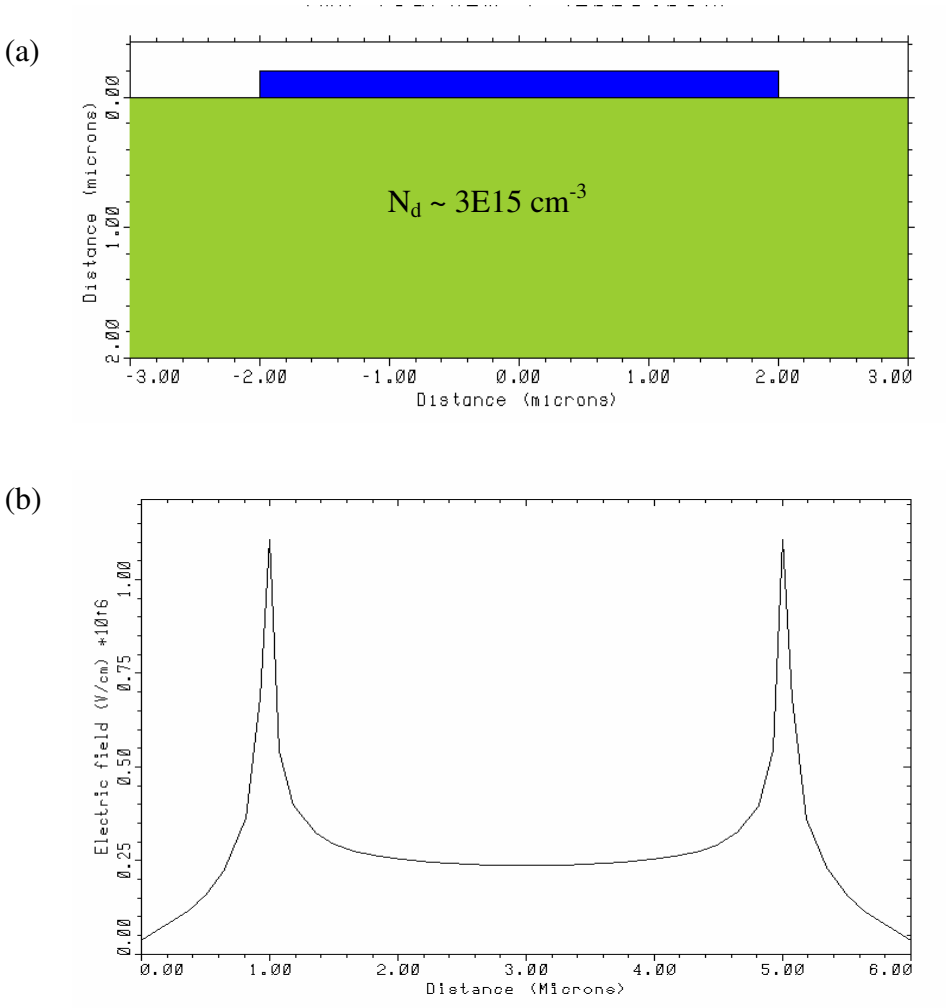


Figure 2.7 (a) Cross section of the Schottky diode, (b) electric field magnitude along the interface of metal/Si contact for V_R = 50 volts.

(a)

(b)

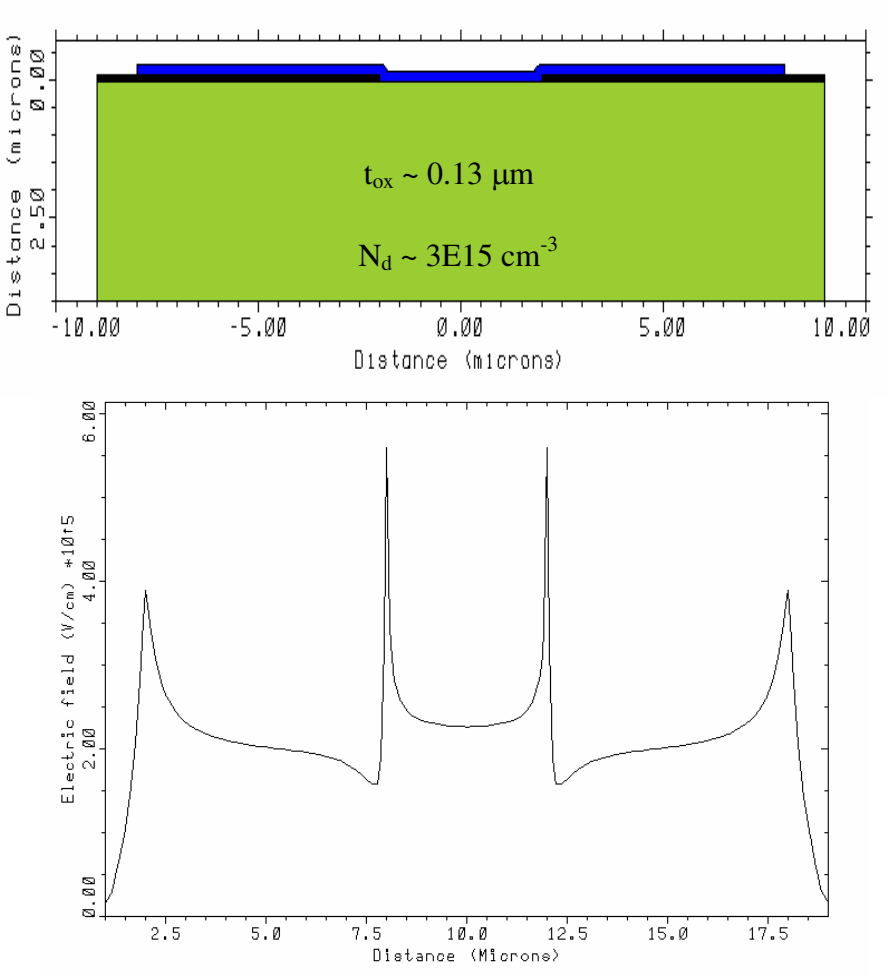
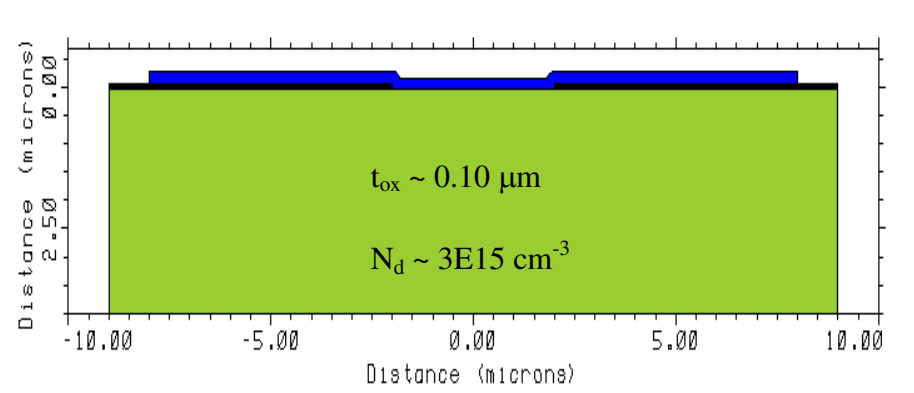


Figure 2.8 (a) Schottky diode with metal overlay structure, (b) electric field magnitude along the interface of silicon/oxide/metal for V_R = 50 volts

(a)



(b)

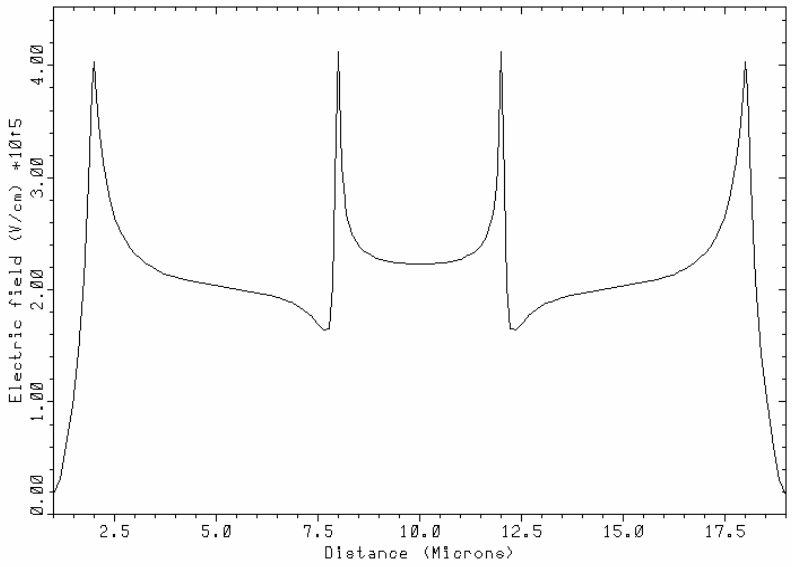


Figure 2.9 (a) Schottky diode with metal overlay structure, (b) electric field magnitude along the interface of silicon/oxide/metal for V_R = 50 volts

(ii) Diffused guard ring: This method is often used and is very effective to reduce the edge effect [59]. The doping profile of this diffused guard ring is tailored to give the p-n junction a higher breakdown voltage than that of the metal-semiconductor contact. Figure 2.10 shows the Schottky contact with diffused guard ring

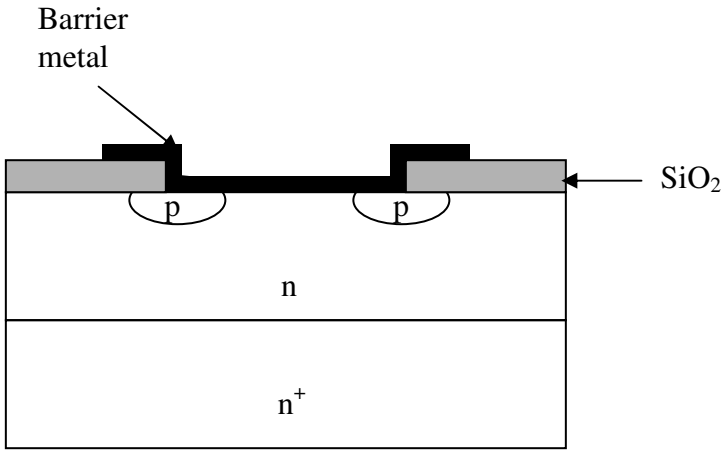


Figure 2.10 Schottky contact with diffused guard ring structure

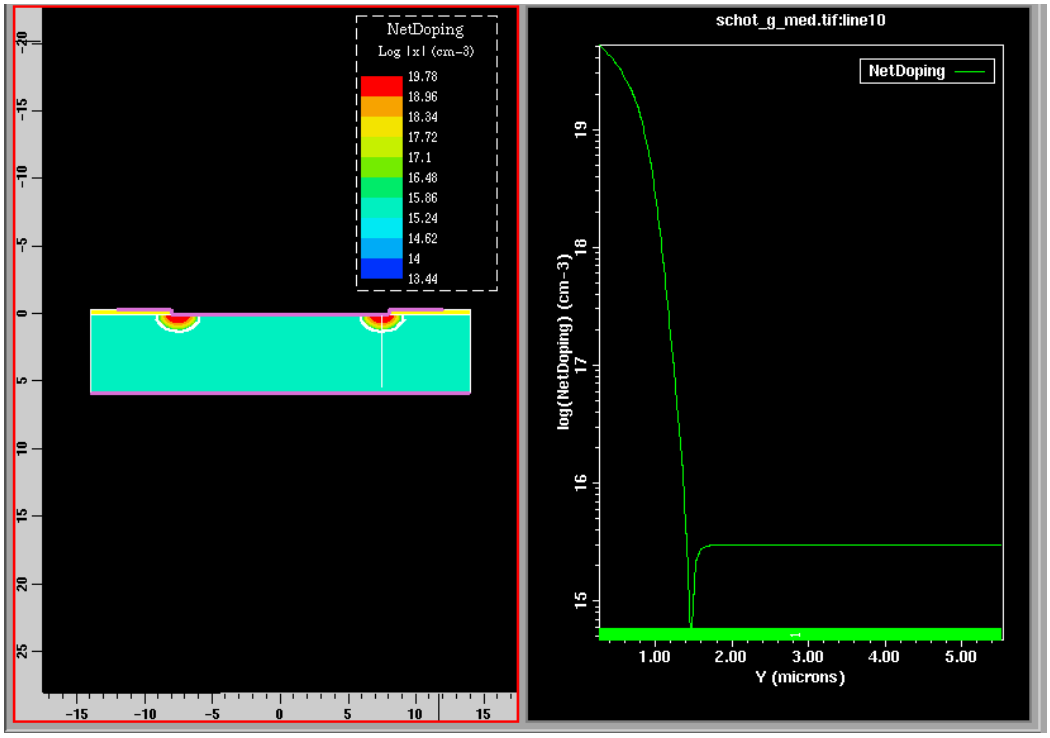


Figure 2.11 TSUPREM simulation of the diffused guard ring structure with the doping profile on the right.

structure and Fig. 2.11 shows the TSUPREM simulation of the diffused guard ring structure with the doping profile. From the doping profile, the junction depth is found to be ~1.5 μm. Figure 2.12 shows the electric field distribution of this Schottky contact with diffused guard ring. It is seen from Fig. 2.12 that the maximum field is at the metal/oxide interface, the effect of which can easily be eliminated by increasing the oxide thickness. In this structure, there is no field crowding at the junction of metal, silicon and oxide that we saw in the metal overlay structure. In this case, the field

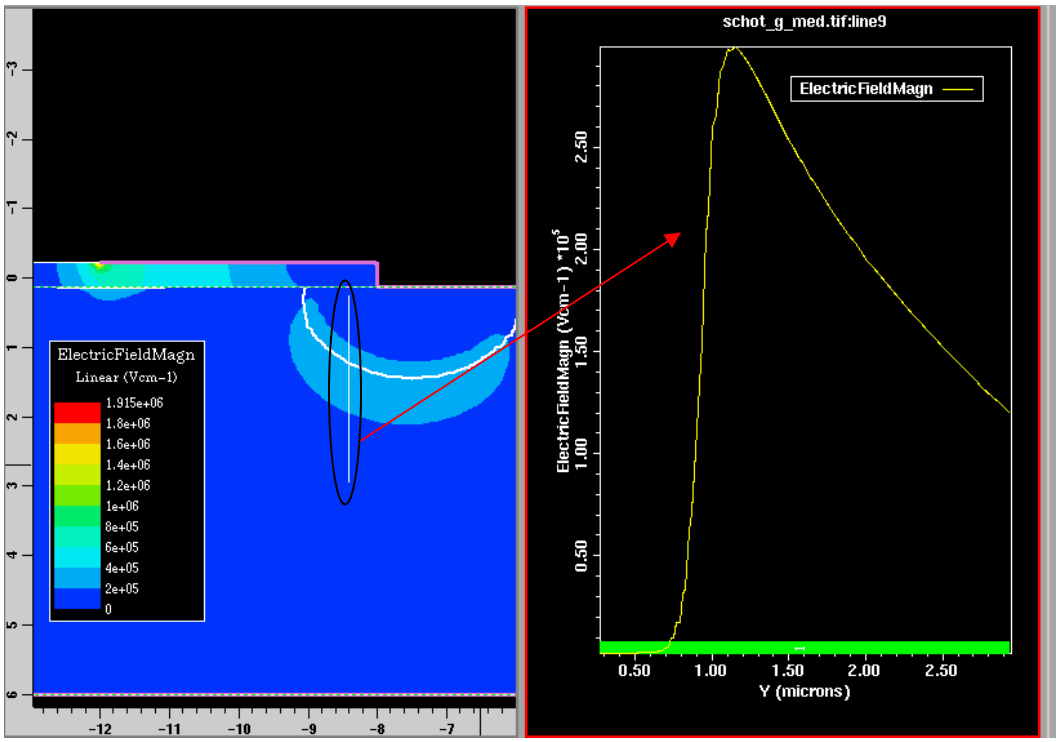


Figure 2.12 Electric field distribution and magnitude for diffused guard ring structure for V_R = 50 volts

crowding is located at the p-n junction of the diffused guard ring. The field is maximum where the radius of curvature is minimum. In this structure, the maximum electric field

in the semiconductor region has come down to ~$3x10^5$ V/cm from the initial >$1x10^6$ V/cm for the Schottky contact without any junction termination technique. However this structure is complicated to implement and expensive. It also suffers to some extent from the minority carrier storage problem.

(iii) Double diffused guard ring: Figure 2.13 shows the Schottky diode structure with double diffused guard ring [60]. This structure is even more complicated than the single guard ring structure but it has the advantage of having faster switching speed than the single guard ring structure.

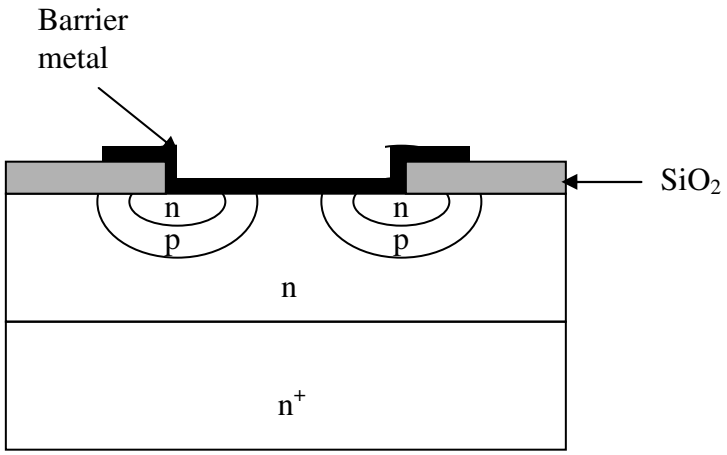


Figure 2.13 Schottky diode structure with double diffused guard ring

(iv) Beveled structure: Figure 2.14 shows another version of overlay structure, which involves beveling of the insulator thickness at the edge. This beveling helps in reducing the electric field but practically it is hard to implement.

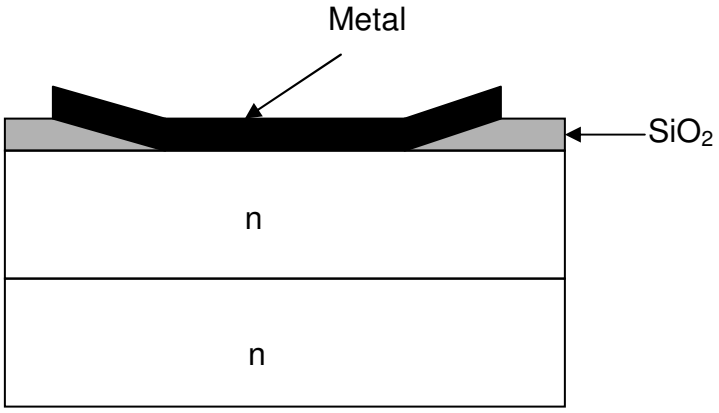


Figure 2.14 Schottky diode structure with beveled insulator and metal overlay

(v) Truncated cone structure: This structure is sometimes used for certain microwave power generators. Figure 2.15 shows this truncated cone structure [32]. In this structure, the angle between the metal overhang and the semiconductor cone must be larger than 90^{o}, so that the electric field at the contact periphery is always smaller than that in the center.

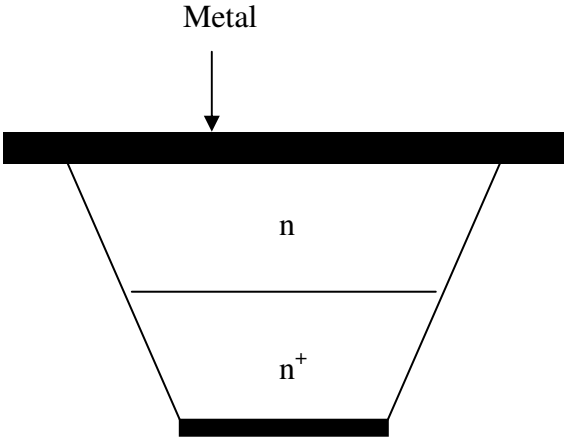


Figure 2.15 Schottky diode with truncated cone structure.

(vi) Metal guard ring structure: This is another version of the guard ring structure, which is implemented by two different work function metals [32]. But practically large variations in barrier height are not found as mentioned in the beginning of this chapter due to surface-state. But by implementing the passivation technique, this structure can be realized and it will be simpler and cost effective.

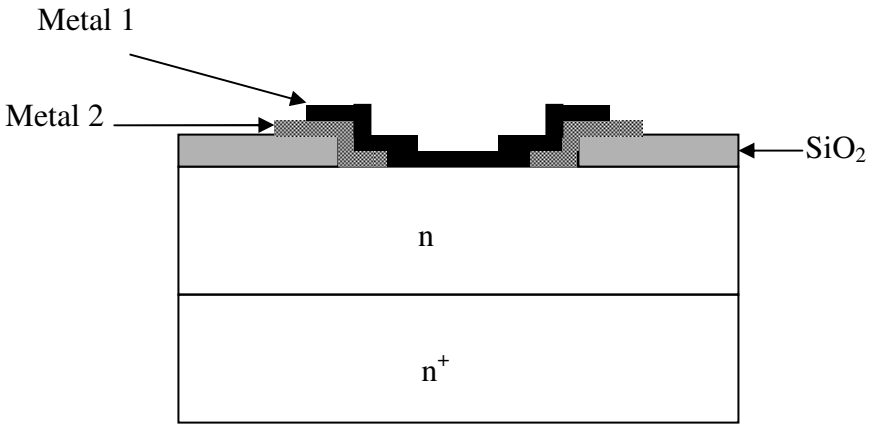


Figure 2.16 Schottky diode with metal guard ring structure.

2.8 Applications

Schottky contacts are widely used in semiconductor industries. As Schottky diodes are majority carrier devices, which means that they do not have minority carrier storage problem. The absence of minority carrier storage results in a faster response than the p-n junction diodes. This difference makes the Schottky diodes useful in high-speed switching applications and as a detector in microwave frequencies. It can be used as an ESD (electro static discharge) protection element at different pins of an IC. In power rectifier applications, less power will be dissipated by a Schottky diode than a p-n junction diode. In bipolar transistor logic circuits, the minority-carrier storage in the

base can be avoided by connecting a Schottky-barrier diode between the base and collector of an npn transistor.

2.9 Summary

In this chapter, an overview of metal-semiconductor contact is provided along with the transport mechanism, the effect of surface-states, diode design procedure and its application. It has been shown that in the absence of surface-states, the barrier height of a Schottky contact is a function of the metal work function. If the surface-state is too high then the barrier height becomes independent of the deposited metal work function. It is also explained that due to the finite radius of curvature effect, the break down voltage of the Schottky diode is way below its ideal break down voltage. In order to reduce the sharp edge effect and thus increase the break down voltage, different junction termination techniques have been discussed.

CHAPTER 3

WET-CHEMICAL PASSIVATION OF Si (100) SURFACE

3.1 Introduction

The problem of surface states has been explained in the previous chapter. Different techniques have been developed to remove the surface states from different semiconductors like Si, GaAs, Ge as well as InP. In this chapter a brief description of the "Valence-mending concept", is explained and based on this concept, a new passivation technique is demonstrated to passivate the dangling bonds of Si(100) surface from a solution.

3.2 Valence-Mending Concept

The key to the passivation of any semiconductor surface is to turn the broken surface atoms into bulk-terminated ones. In the case of Si(100) surface, the dangling bonds have to be terminated, the dimmer bonds have to be removed, and the strained back bonds have to be relaxed. But no guide lines were available until 1991, when Kaxiras proposed his "Valence-mending" technique to passivate semiconductor surface and its application to Si(100) surface [64]. He provided a set of criteria to choose the "Valence-mending Adsorbate" for the passivation of semiconductor surface. His selection criteria can be summarized as:

i) The valence difference between the substrate and the adsorbate should be such that, when adsorbate atoms replace the bulk-terminated plane, all the broken covalent bonds are eliminated.

ii) The adsorbate must exist in a bulk phase with the same local bonding geometry as in the restored surface.

iii) The difference between the covalent radii of the adsorbate and the substrate should be as small as possible.

iv) The difference between the bond angles of the adsorbate in its bulk phase and in the restored surface geometry should be as small as possible.

v) Finally the formation of the restored surface should be an exothermic process but the energy released should not be large on the scale of surface bond energies, since undesired reactions such as etching may follow.

Using his first two criteria group VI elements (O, S, Se, Te) are the best choices for Si(100) surface. Based on his other criteria only S and Se stand out to be the best candidates for the passivation of Si(100) surface. Table 3.1 provides some parameters of Si, S, Se and Te. From Table 3.1, it is found that Se and S match closely with Si in terms of covalent radius, atomic radius, bond angle and bond length with Se being the best choice.

Table 3.1 Different parameters of Si, S, Se and Te [64, 65]

	Si	Se	S	Te	Restored Si(100):Se	Restored Si(100):S
Covalent Radius (A^o)	1.17	1.17	1.04	1.37	-	-
Atomic Radius (A^o)	1.18	1.16	1.06	1.42	-	-
Bond length (A^o)	2.35	2.34	2.05	-	2.34	2.24
Bond angle (deg.)	109.4	105.5	107.9	-	110.2	118.4

Theoretical studies performed by Kaxiras [64] and Kruger et al. [66] showed that both S and Se are adsorbed in the bridge position on a clean Si(100)-2×1 surface and change the Si(100)-2×1 structure to bulk terminated Si(100)-1×1 structure. Lacharme et al. [67] have shown by photoemission spectroscopy that surface states are removed when the Si(100) surface is exposed to a S flux at room temperature. Papageorgopoulos and Kamaratos [68, 69] have studied the adsorption and desorption of S and Se on Si(100)- 2×1 surface. They have also found that the reconstructed Si(100)- 2×1 surface turned into its original bulk terminated Si(100)- 1×1 configuration due to S or Se adsorption.

3.3 Selection of the Passivating Solution

As discussed above, the key to successful passivation of the Si(100) surface is to terminate the silicon dangling bonds at the surface with the properly chosen atom. For wet-chemical passivation, the wafer is dipped in a solution containing valence-mending atoms for a certain time to terminate the dangling bonds. Unlike Ge or GaAs, the native oxide of silicon is not soluble in aqueous solution. Whenever a silicon surface is

exposed to atmosphere, a thin layer of oxide is formed on the surface. So, the key to successful passivation of Si(100) substrates from a solution is to in-situ etch SiO_2 right before passivation. Even though a Si wafer can be cleaned in a solution like HF, native oxide still forms when the wafer is transferred from the HF solution to the passivant solution.

Our approach to wet-chemically passivate Si(100) involves adding an etchant for SiO_2 into an aqueous passivant solution for Si(100) to in-situ remove the oxide layer right before the surface is passivated by the passivating agent. There are several requirements for the choices of passivant and etchant.

Passivant:

i) It has to contain "Valence-mending" agent (S/Se)

ii) It should stay in an ionized form in the solution, so that it readily reacts with the dangling bonds on the Si surface

iii) It should not contain any element that can cause a doping effect or contamination to the wafer

Etchant:

i) It has to be compatible with the Passivant

Table 3.2 lists some available solutions containing valence-mending adsorbates. From Table 3.2, it is seen that $(NH4)_2S$ or $(NH4)_2Se$ solution can be used for the passivation. Though Se has better matching parameters with Si, $(NH4)_2Se$ is not commercially available. The commercially available $(NH4)_2S$ solution is chosen as the passivating agent.

Table 3.2 List of some available solutions containing valence-mending atom

Solution	Comment
$Na_2S.9\ H_2O$	Na ion contamination
Na_2Se/NH_4OH	Na ion contamination
S_2Cl_2 in CCl_4	C contamination
P_2S_5/NH_4OH	P doping effect
$(NH4)_2S$/ $(NH4)_2Se$	Best Choice

Compatibility of the etchant with the passivant means it should not react with the passivant. For a instance, HF is well known to be a good etchant for SiO_2. When it is added to a solution containing $(NH_4)_2S$, it was found that they reacted with each other, releasing H_2S and forming milk-white precipitates. This excludes HF on compatibility ground. From the literature, it is found that ammonium hydroxide [NH_4OH] etch SiO_2 at elevated temperatures [70]. Our experiments suggest that NH_4OH is compatible with $(NH_4)_2S$ for in-situ etching of SiO_2.

3.4 Characterization of the Passivation Quality

Although various techniques, such as Auger electron spectroscopy (AES) and x-ray photoelectron spectroscopy (XPS) are available for surface analysis, only positron annihilation induced Auger electron spectroscopy (PAES) is applicable for the analysis of our monolayer-passivated surface because of its topmost-surface sensitivity in nature [71]. PAES is a time-consuming technique. Here, an indirect method is used to monitor the passivation process by measuring the I-V relation of two back-to-back Schottky diodes formed by Al on S-passivated n-type Si(100), which provides the reverse

saturation current of the Schottky diodes as shown in Fig. 3.1(a). Since S passivation is expected to reduce the Schottky barrier height between Al and n-type Si, it should lead to a significantly higher reverse saturation current. Therefore, good-quality passivation requires maximization of the reverse saturation current.

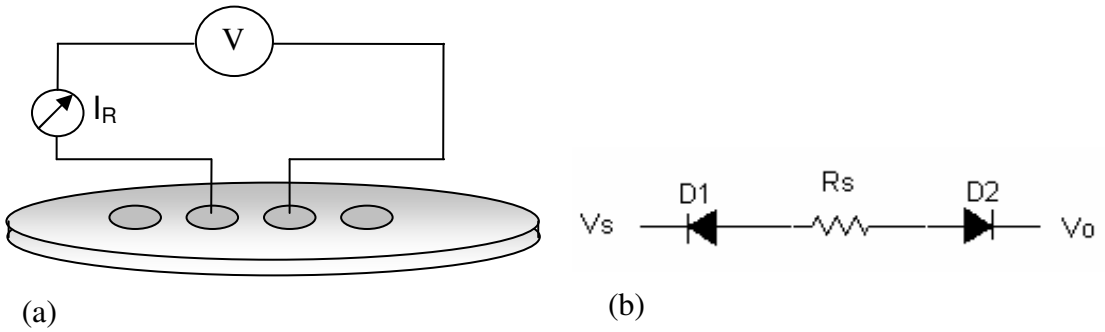


Figure 3.1 (a) Test structure for the measurement of reverse saturation current from two back-to-back Schottky diodes and (b) equivalent circuit corresponding to (a), where D1 and D2 are the Schottky diodes and R_s is the series resistance.

Figure 3.1(b) is the equivalent circuit corresponding to the test structure. Figure 3.2(a) shows the band diagram of the Al/n-type Si(100) contact before passivation. Due to interface states, the Schottky barrier height between Al and n-type Si is way off its ideal barrier height of -0.01 eV [25]. With S terminating dangling bonds on Si(100), the barrier height should decrease significantly and thus a higher reverse saturation current is expected. In this experiment, reverse saturation current is used as an indication of passivation quality. Figure 3.2(b) shows the band diagram of the same contact after all the interface states are passivated [25].

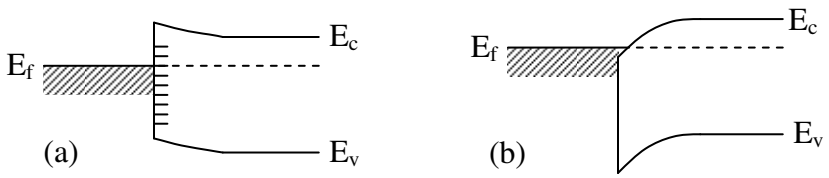


Figure 3.2 Band diagram of Al/n-type Si(100) contacts (a) before passivation with interface states and (b) after passivation without interface states.

3.5 Experimental

Si(100) wafers of n-type were used for the experiments. The n-type wafers were doped with arsenic in the low 10^{15} cm^{-3} range. The nominal wafer miscut was less than 0.5°. The wafers were first cleaned with 2% hydrofluoric acid (HF) for 30 seconds. A 20-Å SiO_2 layer was grown by ozone oxidation at 500°C. The samples were then dipped in a mixture of $(NH_4)_2S$ and NH_4OH at 60°C for a certain time for passivation. By growing the thin oxide layer and then etching it in-situ in the solution, this process has the inherent advantage of removing carbon along with other contaminants.

A 700-Å Al layer was deposited by evaporation on the n-type passivated wafers. All the wafers were then patterned using a lift-off process. The contact size was 100, 200, and 300 μm in diameter. The front Schottky diodes were characterized by current-voltage (I-V) measurement.

The experimental parameters, which impact the passivation quality include:

i) Solution temperature;

ii) Concentration of NH_4OH;

iii) Passivation time;

iv) Concentration of $(NH_4)_2S$.

i) Solution Temperature:

Temperature mainly affects the etch rate of SiO_2 by NH_4OH [70]. Increasing the temperature increases the etch rate. However, increasing the temperature too much causes rapid evaporation of the solution. The optimum solution temperature is, therefore, chosen to be 60°C for a balance between a fast etch rate and a slow evaporation rate.

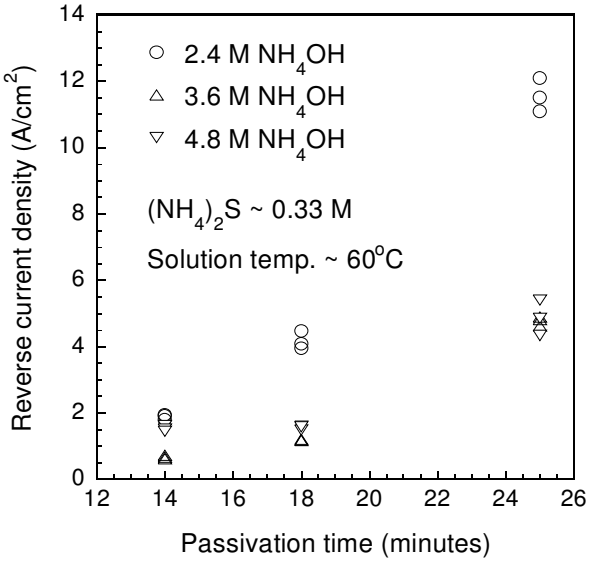


Figure 3.3 Effect of NH_4OH concentration on reverse saturation current at 1 V measured from two back-to-back Al/S-passivated n-type Si(100) diodes.

ii) Concentration of NH_4OH:

The concentration of NH_4OH mainly affects the etch rate of SiO_2. For a reasonable throughput, the SiO_2 layer needs to be removed from the Si(100) surface in a suitable time frame. Figure 3.3 shows the effect of NH_4OH concentration on reverse

saturation current. The reverse saturation current reaches a maximum for 2.4 M concentration of NH_4OH and 25 minutes, indicating that the SiO_2 layer is completely removed with that concentration and time and the dangling bonds on Si(100) are effectively passivated by the passivant.

iii) Passivation Time

Good passivation needs to be realized in a reasonable time frame. Figure 3.4 shows the effect of passivation time on reverse saturation current. The concentrations of NH_4OH and $(NH_4)_2S$ are kept constant at 2.4 M and 0.33 M, respectively, and the passivation is carried out for different times. After 20 minutes, there is no significant increase in reverse saturation current. This suggests that by ~20 minutes, SiO_2 is completely removed and the dangling bonds are effectively passivated. A process window of 20-30 minutes is thus determined for passivation time. In the following experiments, the passivation time is fixed at 25 minutes.

iv) Concentration of $(NH_4)_2S$

Figure 3.5 shows the effect of $(NH_4)_2S$ concentration on reverse saturation current, with other parameters fixed at 25 minutes for passivation time, 60°C for solution temperature, and 2.4 M for $(NH_4)OH$ concentration. With an increase in $(NH_4)_2S$ concentration, the reverse saturation current first increases and then saturates for $(NH_4)_2S$ concentrations of 0.33 M and higher. Therefore, a process window of 0.33-1.0 M is determined for $(NH_4)_2S$ concentration. In the following experiments, the concentration of $(NH_4)_2S$ is fixed at 0.33 M.

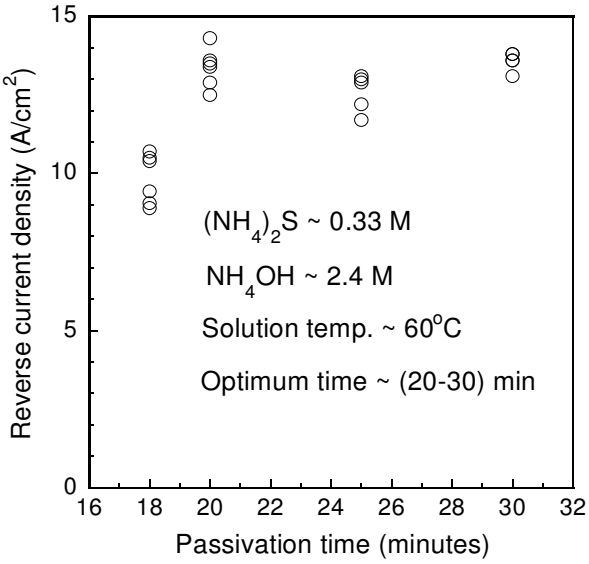


Figure 3.4 Effect of passivation time on reverse saturation current at 1 V measured from two back-to-back Al/S-passivated n-type Si(100) diodes.

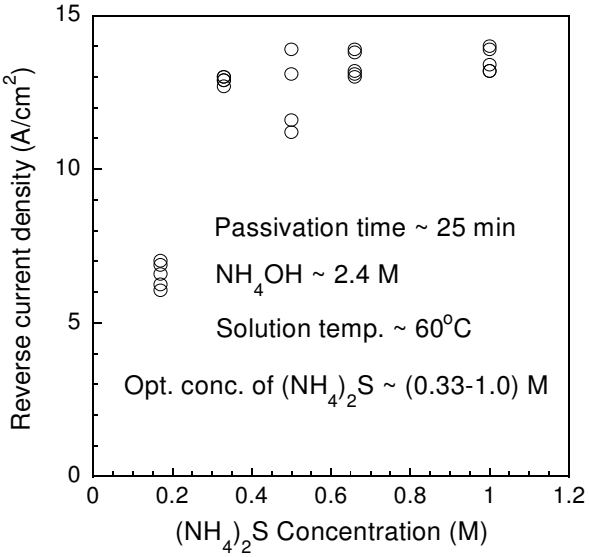


Figure 3.5 Effect of $(NH_4)_2S$ concentration on reverse saturation current at 1 V measured from two back-to-back Al/S-passivated n-type Si(100) diodes.

The optimized parameters for good quality passivation are as follows:

- Temperature ~ 60^{o} C
- Concentration of NH_4OH ~ 2.4 M
- Passivation Time ~ 25 minutes
- Concentration of $(NH_4)_2S$ ~ 0.33 M

3.6 Summary

In this chapter, the "Valence-mending technique" is explained and using this technique a wet-chemical process is developed for the passivation of Si(100) surface. It is shown that the four parameters namely temperature, time, concentration of $(NH_4)OH$ and concentration of $(NH_4)_2S$ are optimized to get good quality passivation. From the experiments, it is found that there is process window for the concentration of NH_4OH, $(NH_4)_2S$ and passivation time. So in the case of a little variation in the process, passivation quality will not be affected.

CHAPTER 4

EFFECT OF DIFFERENT METALS ON S-PASSIVATED Si (100)

4.1 Introduction

With the optimized parameters both n-and p-type Si(100) wafers were passivated in the S-solution. Metals with different work functions were deposited on the passivated surface to do the electrical characterization. As a comparison purpose, control samples were also made with the same metals. The samples were characterized using current-voltage, activation energy and capacitance-voltage measurement. Finally a brief description of surface dipole is provided.

4.2 Experimental

Si(100) wafers of both n- and p-type were used for the experiments. The n-type wafers were doped with arsenic and the p-type with boron, both in the low 10^{15} cm^{-3} range. The nominal wafer miscut was less than 0.5°. One set of the wafers was S passivated while the other set had no S passivation for a comparison purpose. For the S-passivated samples, the wafers were first cleaned with 2% hydrofluoric acid (HF) for 30 seconds. The wafers were then passivated with S in a solution containing $(NH_4)_2S$. A 700-Å Al layer was deposited by thermal evaporation on one set of the passivated wafers (both n- and p-type). On another set of the passivated wafers (both n- and p-type), a 700-Å Ni layer was deposited in the same manner. Ti and Cr were deposited on

the n-type wafers. All the wafers were then patterned using a lift-off technique. The contact size was 100 μm, 200 μm and 300 μm in diameter. For the set of wafers without S passivation, they were cleaned with 2% HF for 30 seconds only and then those four different metals were deposited and patterned in the same manner as the passivated samples. Aluminum was deposited on the backside of all the wafers for the back ohmic contact. The larger area of the back contact compared to the front contacts (>10^5 times larger) made possible characterization of the front diodes with negligible effect of the Schottky behavior from the back contact. The front Schottky diodes were characterized by current-voltage (I-V), capacitance-voltage (C-V) and activation-energy measurements.

4.3 Electrical Characterization

4.3.1 Al on n-and p-type Si(100)

Figure 4.1 shows the I-V characteristics of two back-to-back Schottky diodes with Al on S-passivated n-type Si(100) at different temperatures. The I-V characteristics are linear at temperatures as low as 138 K, the lowest achievable temperature in our laboratory. With this linear I-V characteristics, C-V and activation-energy methods fail to yield a barrier height. It should be noted that the Schottky characteristics of a very low Schottky barrier can be overshadowed by a high series resistance. In such cases, the barrier height can be determined with low-temperature I-V measurements [72]. A simple-minded fitting of the thermionic-emission model (Eq. 2.18) to the low-temperature data at 138 K, shown as a solid line in Fig. 4.1, suggests that the barrier

height is no more than 0.11 eV. This value agrees well with the barrier height measured for Al on Se-passivated n-type Si(100) [26].

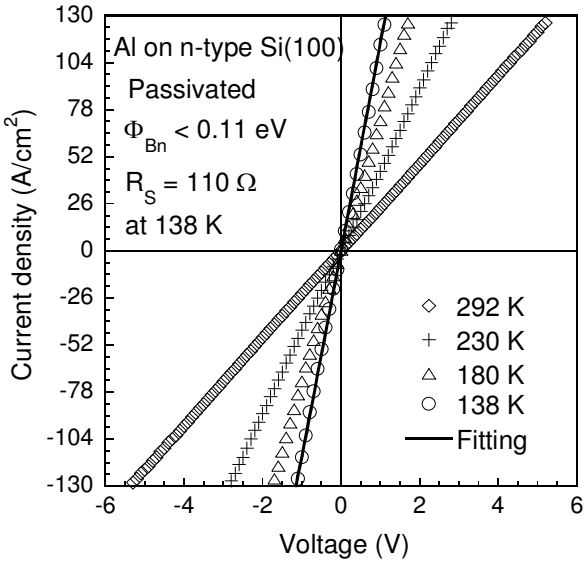


Figure 4.1 I-V characteristics of two back-to-back Schottky diodes with Al on S-passivated n-type Si(100) at different temperatures. The solid line shows the fitting result with the thermionic-emission model for data at 138 K.

Figure 4.2 shows the I-V characteristics of Schottky diodes with Al on n- and p-type Si(100) at room temperature. Sulfur passivation reduces the reverse saturation current by more than an order of magnitude for Al/p-type Si(100) diodes, implying that S passivation increases the barrier height for Al/p-type Si(100) contacts. This observation is quantitatively verified by activation-energy and C-V measurements. The I-V characteristics in Fig. 4.2 were fitted with the thermionic-emission model as shown by the solid lines in the figure. The fittings allowed the extraction of the barrier height and ideality factor, which are listed in Table 4.1 under Column I-V.

Figure 4.3 shows an activation-energy plot of Al on both S-passivated and non-passivated p-type Si(100). Two back-to-back Schottky diodes were used for the measurement of reverse saturation current. Activation-energy measurements reveal that S passivation increases the barrier height by ~0.13 eV for Al/p-type Si(100) contacts.

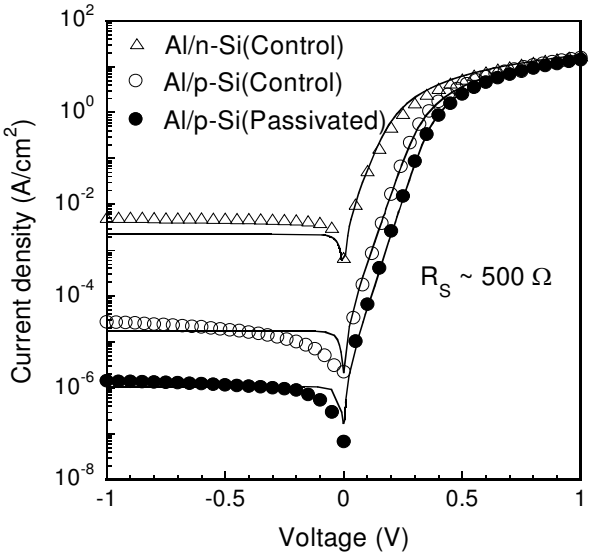


Figure 4.2 I-V characteristics of Al on n- and p-type Si(100) at room temperature. The solid lines are the fitting results with the thermionic-emission model for corresponding experimental data.

Figure 4.4 shows a $1/C^2$-vs.-V plot of Al on both S-passivated and non-passivated p-type Si(100). The C-V measurement was performed at 1 MHz and the extracted doping concentration is ~2×10^{15} cm^{-3}, in agreement with the wafer specification. The maximum Schottky barrier lowering ($\Delta\phi$) is estimated at ~0.01 eV and is not included in the analysis. This C-V measurement reveals that S passivation increases the barrier height by ~0.13 eV for Al/p-type Si(100) contacts.

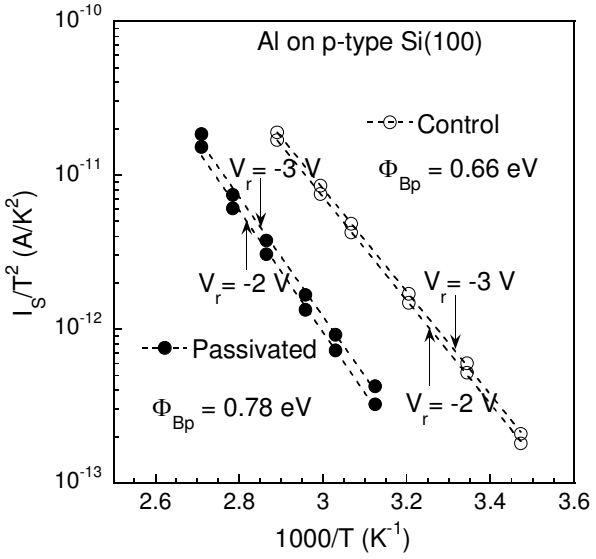


Figure 4.3 Determination of Schottky barrier height between Al and p-type Si(100) from activation-energy measurement

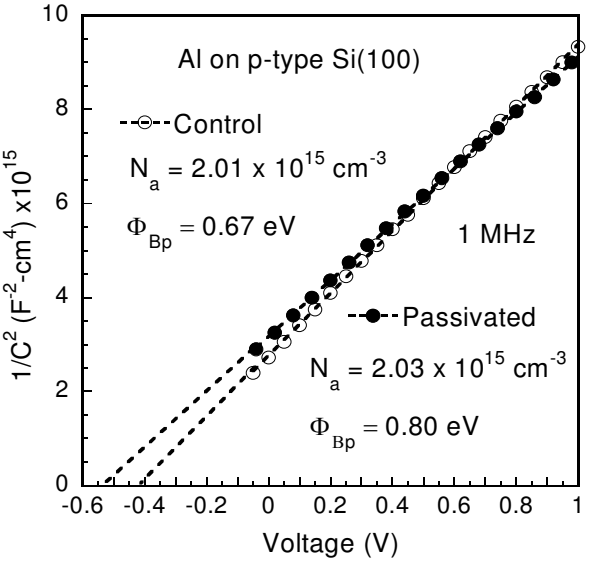


Figure 4.4 Determination of Schottky barrier height between Al and p-type Si(100) from C-V measurement for both S-passivated and non-passivated samples

4.3.2 Ni on n-and p-type Si(100)

Figure 4.5 shows the I-V characteristics of Schottky diodes with Ni on n- and p-type Si(100) at room temperature. Sulfur passivation reduces the reverse saturation current by more than an order of magnitude for Ni/n-type Si(100) diodes, while it doubles the reverse current for Ni/p-type Si(100) diodes. In both Figs. 4.2 and 4.5, it is noticed that the forward current does not appear linear in the logarithmic plots, indicating that the forward current is limited by a high series resistance (~500 Ω) in all the samples.

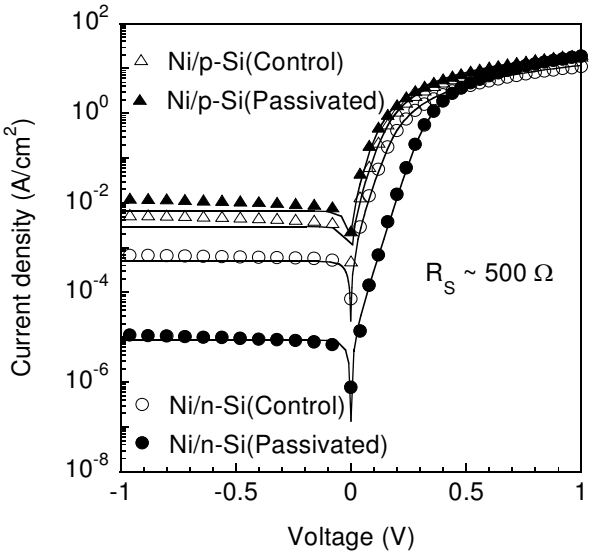
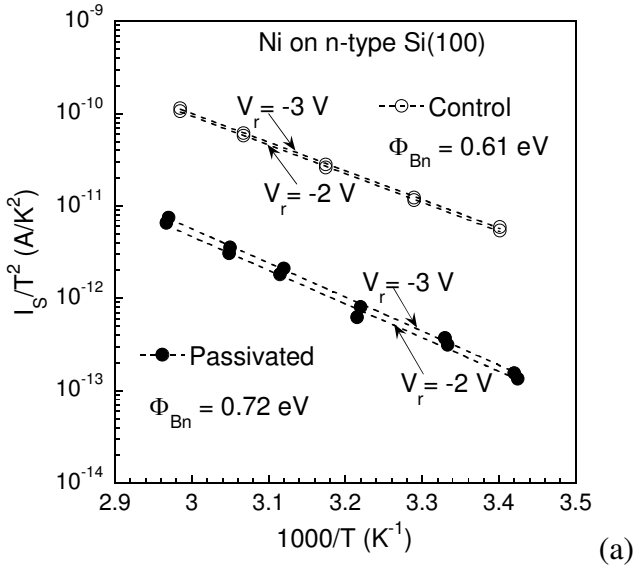
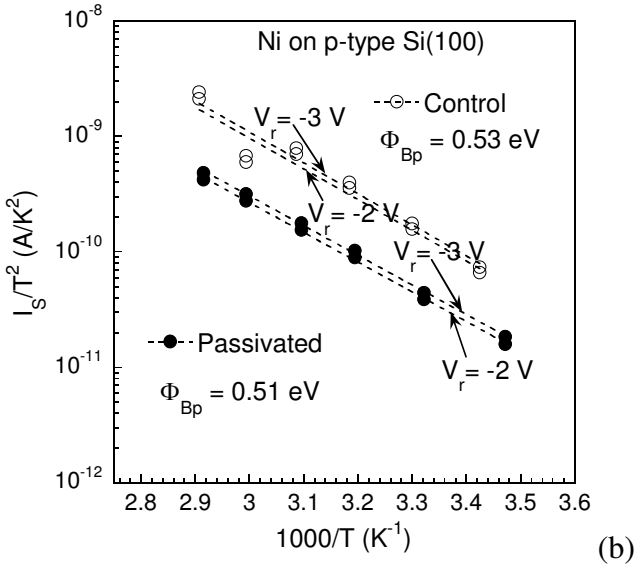


Figure 4.5 I-V characteristics of Ni on n- and p-type Si(100) at room temperature. The solid lines are the fitting results with the thermionic-emission model for corresponding experimental data.

The I-V characteristics in Fig. 4.5 were fitted with the thermionic-emission model as shown by the solid lines in the figure. The fittings allowed the extraction of the barrier height and ideality factor, which are listed in Table 4.1 under Column I-V.



(a)



(b)

Figure 4.6 Determination of Schottky barrier height from activation-energy measurement between (a) Ni and n-type Si(100) (b) Ni and p-type Si(100) for both S-passivated and non-passivated samples

As can be seen from Table 4.1, S passivation increases the barrier height by ~0.12 eV for Ni/n-type Si(100) contacts and decreases the barrier height by ~0.03 eV

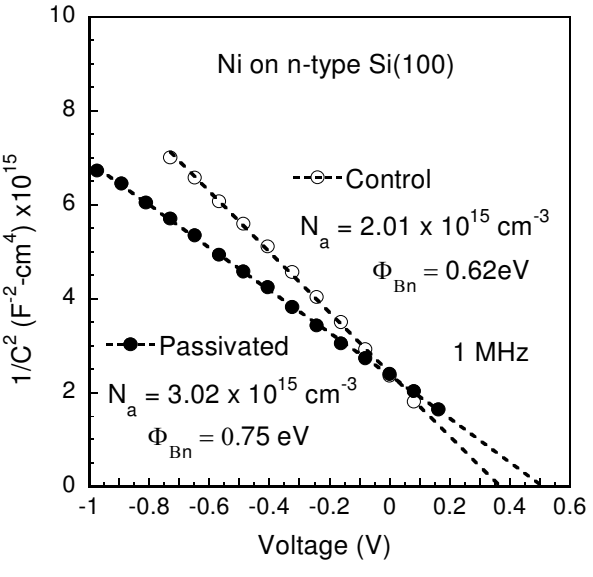
for Ni/p-type Si(100) contacts. The changes in barrier height are reflected in the reverse saturation currents measured.

Figure 4.6(a) and 4.6(b) show activation-energy plots of Ni on n-type Si(100) and Ni on p-type Si(100), respectively on both S-passivated and non-passivated samples. Sulfur passivation increases the barrier height by ~0.12 eV for Ni/n-type Si(100) contacts, but decreases the barrier height by ~0.02 eV for Ni/p-type Si(100), which supports the I-V measurement discussed above.

The effective Richardson constant A^{**} can be extracted from the activation-energy plots in Figs. 4.3 and 4.6. Its values for electrons are ~669 and ~580 A/cm^2-K^2 for control and S-passivated samples, respectively. The values of A^{**} for holes are ~130 and ~195 A/cm^2-K^2 for control and S-passivated samples, respectively. The difference in effective Richardson constant between control and S-passivated samples is marginal, considering the fact that Richardson constant depends on several surface factors such as surface preparation and cleaning procedure [73].

Figure 4.7(a) shows a 1/C^2-vs.-V plot of Ni on n-type Si(100) and Fig. 4.7(b) of Ni on p-type Si(100) for both S-passivated and non-passivated samples. We can notice that for Ni on n-type Si(100), S-passivation increases the barrier height by about ~0.13 eV, while for Ni on p-type Si(100), S passivation reduces the barrier height by ~0.03 eV and thus doubles the reverse current as found in the I-V measurement. The doping concentration found from C-V for the control sample of Ni/p-Si(100) is ~6×10^{14} cm^{-3}, which is lower as compared to other samples. In Figs. 4.7(a) and 4.7(b), there is a slope

change between control and S-passivated samples. It is speculated that different doping concentrations in the wafers may be the cause for the slope change.



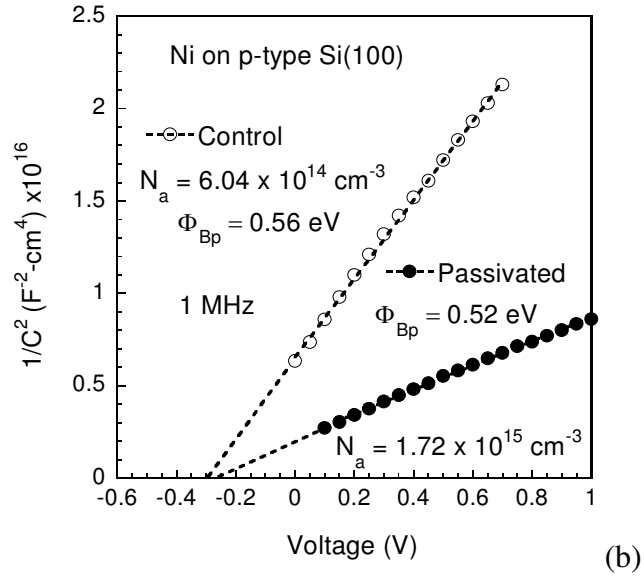


Figure 4.7 Determination of Schottky barrier height from C-V measurement between (a) Ni and n-type Si(100) (b) Ni and p-type Si(100) for both S-passivated and non-passivated samples.

4.3.3 Ti on n-type Si(100)

Figure 4.8 shows the I-V characteristics of two back-to-back Schottky diodes with Ti on S-passivated n-type Si(100) at different temperatures. The I-V characteristics are linear at temperatures as low as 173 K. A simple-minded fitting of the thermionic-emission model (Eq. 2.18) to the low-temperature data at 173 K, shown as a solid line in Fig. 4.8, suggests that the barrier is less than 0.17 eV.

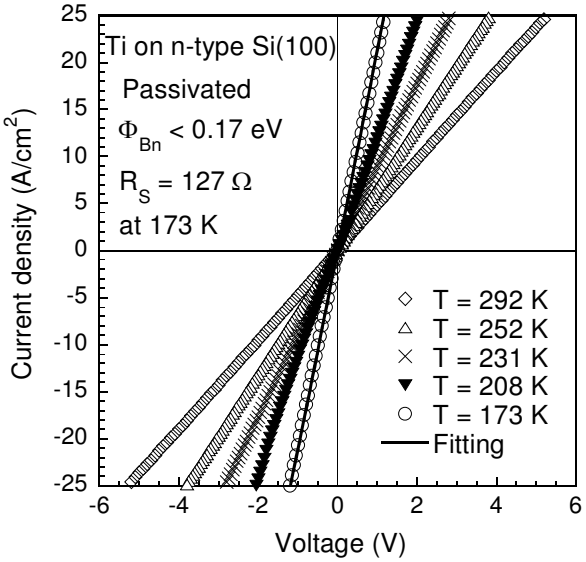


Figure 4.8 I-V characteristics of two back-to-back Schottky diodes with Ti on S-passivated n-type Si(100) at different temperatures. The solid line shows the fitting result with the thermionic-emission model for data at 173 K.

Figure 4.9 shows the I-V characteristics of two back-to-back Schottky diodes with Ti on n-type Si(100) at room temperature. It shows that S-passivation increases the reverse saturation current by about three orders of magnitude. The fitting result with the thermionic emission model is shown for the control sample only, while for the

passivated sample the fitting is shown in Fig. 4.8. The extracted barrier height is listed in Table 4.1.

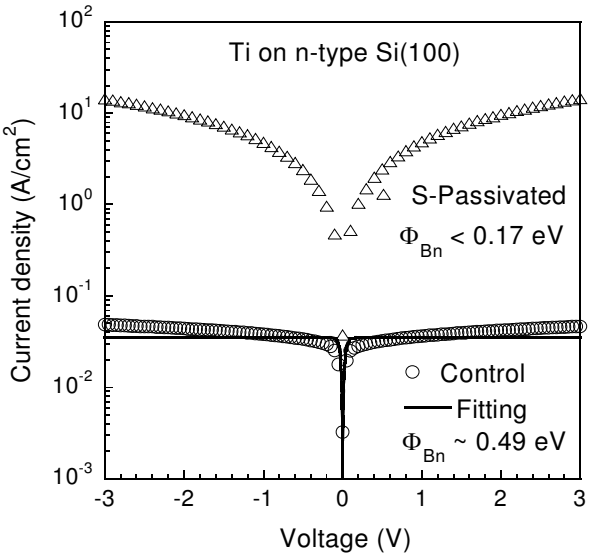


Figure 4.9 I-V characteristics of Ti on n-type Si(100) at room temperature. The solid lines are the fitting result with the thermionic-emission model for corresponding experimental data.

4.3.4 Cr on n-type Si(100)

Figure 4.10 shows the I-V characteristics of Schottky diodes with Cr on n-type Si(100) at room temperature. Sulfur passivation increases the reverse saturation current by more than three orders of magnitude. The I-V characteristics in Fig. 4.10 were fitted with the thermionic-emission model as shown by the solid lines in the figure. The fittings allowed the extraction of the barrier height and ideality factor, which are listed in Table 4.1 under Column I-V.

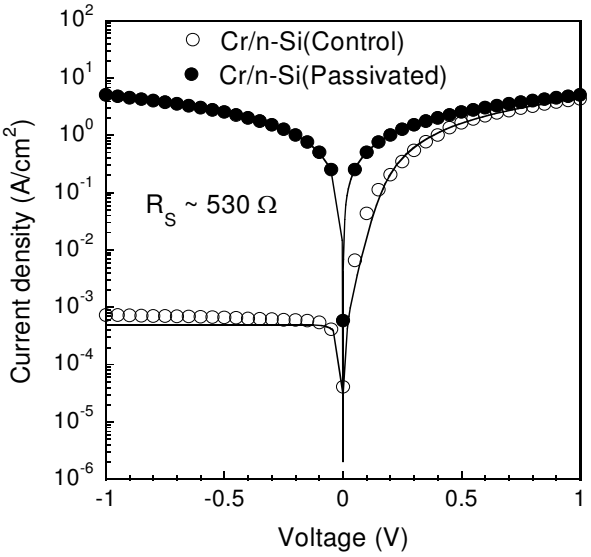


Figure 4.10 I-V characteristics of Cr on n-type Si(100) at room temperature. Solid lines are the fitting results with the thermionic-emission model for corresponding experimental data.

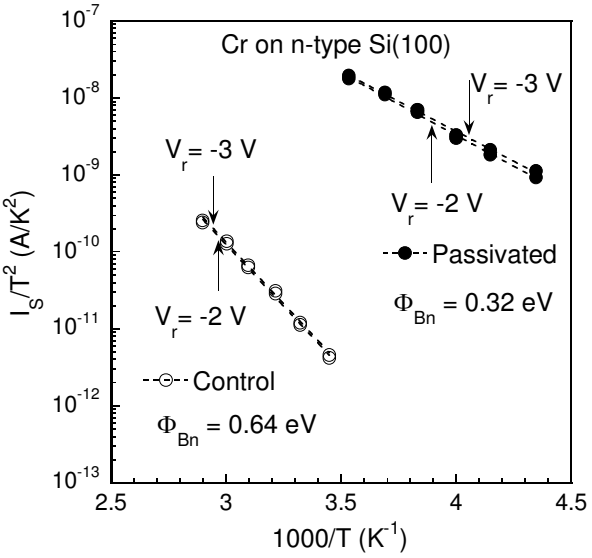


Figure 4.11 Determination of Schottky barrier height from activation-energy measurement between Cr and n-type Si(100) for both S-passivated and non-passivated samples

Figure 4.11 shows activation-energy plots of Cr on n-type Si(100) on both S-passivated and non-passivated samples. Sulfur passivation decreases the barrier height by ~0.32 eV which supports the I-V measurement discussed above.

Figure 4.12 shows a $1/C^2$-vs.-V plot of Cr on n-type Si(100) for both S-passivated and non-passivated samples. It can be noticed that for Cr on n-type Si(100), S-passivation reduces the barrier height by ~0.3 eV, which supports the I-V and activation energy measurements. The C-V measurement was performed at 1 MHz and the extracted doping concentration is ~1.1×10^{15} cm^{-3}, in agreement with the wafer specification.

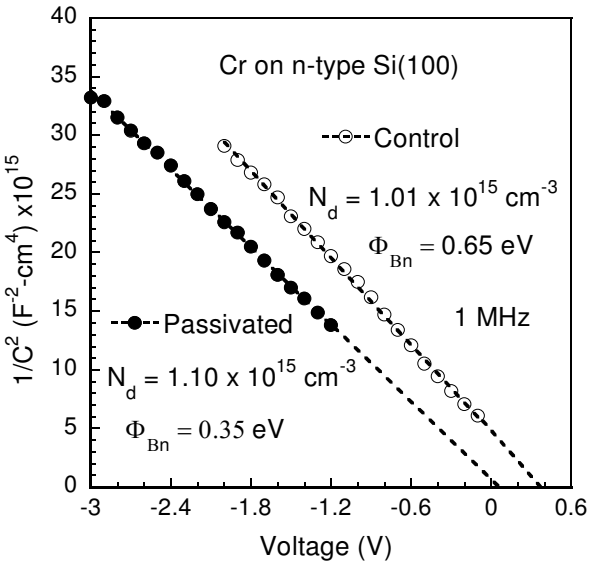


Figure 4.12 Determination of Schottky barrier height from C-V measurement between Cr and n-type Si(100) for both S-passivated and non-passivated samples.

4.3.5 Summary of Measurements

Table 4.1 provides a summary of the measured barrier height and ideality factor (n) for these Schottky diodes using different methods; current-voltage (I-V), activation energy and capacitance-voltage (C-V) measurements. It also lists the ideal barrier heights of those metals for a comparison purpose. In calculating the ideal barrier heights, the electron affinity of Si is taken as 4.29 eV [26] and the work functions of Al and Ni are taken as 4.28 eV and 5.15 eV, respectively [74]. The ideal barrier height for Al on n-type Si(100) is -0.01 eV, and the ideal barrier height for Al on p-type Si(100) is 1.13 eV. This means that the conduction band bends down and crosses the Fermi

Table 4.1 Summary of measured Schottky barrier height and ideality factor (n) on both S-passivated Si(100) and non-passivated Si(100) (unit: eV).

Metal	Type	Ideal barrier	Sample type	n	I-V	Activation Energy	C-V
Al	n	-0.01	Control	1.2	0.56	-	-
Al	n	-0.01	Passivated	-	<0.11	-	-
Al	p	1.13	Control	1.15	0.65	0.66	0.67
Al	p	1.13	Passivated	1.08	0.71	0.78	0.80
Ni	n	0.86	Control	1.08	0.59	0.61	0.62
Ni	n	0.86	Passivated	1.02	0.70	0.72	0.75
Ni	p	0.26	Control	1.10	0.52	0.53	0.56
Ni	p	0.26	Passivated	1.03	0.50	0.51	0.52
Ti	n	0.04	Control	-	0.49	-	-
Ti	n	0.04	Passivated	-	<0.17	-	-
Cr	n	0.21	Control	1.08	0.59	0.64	0.64
Cr	n	0.21	Passivated	1.05	0.34	0.32	0.35

Table 4.2 Band gap values of Si by adding the measured barrier heights for Ni on n- and p-type Si(100) (unit: eV).

Sample type	I-V	Activation Energy	C-V
Ni/Si	1.11	1.14	1.18
Ni/S/Si	1.2	1.23	1.27

level causing degeneracy at the Al/Si(100) interface. Table 4.2 shows the band gap values of Si by adding the measured barrier heights of Ni on n- and p-type Si(100) [32]. Control samples provide a better agreement for the band gap of Si (1.12 eV) than passivated samples. The worst case is for Al on S-passivated Si(100). The measured barrier heights on n- and p-type add up to a maximum of 0.91 eV, which is 0.2 eV below the band gap of Si. It is speculated that wet-chemical passivation cannot guarantee perfect monolayer passivation. Incomplete passivation of the Si(100) surface leaves non-passivated regions where the Schottky barrier height is determined by the pinned interface Fermi level. The effect of incomplete passivation is particularly prominent with a high barrier, such as Al/p-type Si(100) contacts, where the difference in barrier height between passivated regions and non-passivated regions is high. The measured barrier height on such a sample should be much lower than the ideal barrier height.

4.4 Surface States vs. Surface Dipole

The changes in barrier height due to S passivation may be attributed to two factors. One is the reduction of surface states due to the passivation of dangling bonds,

and the other is the S-induced surface dipole. An interesting question is which factor is the dominant one? With the choices of metal with different work functions, Al with a low work function (4.28 eV) and Ni with a high work function (5.15 eV), our results provide an answer to the question.

Following the surface-state theory, in the absence of surface states, the Schottky barrier height depends solely on the metal work function and semiconductor electron affinity. The density of surface states can be estimated by the procedure developed by Cowley and Sze [38]. With their procedure, the density of surface-states can be calculated for the S-passivated Si(100) surface and it turned out to be ~3.86×10^{12} cm^{-2}, while for the non-passivated Si(100) surface, it was ~9.9×10^{13} cm^{-2}. Therefore, S passivation reduces the density of surface states on Si(100) by more than an order of magnitude. Carpenter et al. [4] have found similar improvement with S passivation of the GaAs(100) surface.

When Si atom is terminated by S-atom, a dipole forms depending on the electro-negativities of the two atoms. The change in barrier height due to adsorbate-induced dipole can be expressed as [75]

$$\Delta\phi_B = (\frac{q}{\varepsilon_o\varepsilon_i})\mu_o N_{ad} \tag{4.1}$$

Where ε_o and ε_i are the permittivity of vacuum and interface layer, respectively, μ_o the dipole moment and N_{ad} the number of adsorbed atoms per unit surface area. N_{ad} is 6.78×10^{14} cm^{-2} for a perfectly-passivated Si(100) surface. ε_i is often taken as 4.0 [75-77]. For the Si-S system, the dipole moment was experimentally found to be 0.2 Debye

for monolayer coverage by Papageorgopoulos et al. [78]. Using these values, the barrier height change ($\Delta\phi_B$) is ~0.13 eV for perfect one monolayer S coverage. Even though the exact value of barrier height change may be arguable, the key point is that the change in barrier height due to surface dipole is always unidirectional. For the Si-S system, the surface dipole will always decrease the barrier height on n-type Si(100) and increase the barrier height on p-type Si(100) [75]. This is in contrast with experiments in which S passivation decreases the barrier height for Ni on p-type Si(100) and increases the barrier height for Ni on n-type Si(100). However, these results are expected from the surface-state theory, i.e., depending on the work function of metal, the change in barrier height can go in both directions when surface states are passivated. These experimental findings suggest that surface dipole plays a less significant role than surface states in determining the Schottky barrier height in these metal-Si systems.

4.5 Summary

The effect of S passivation of the Si(100) surface, both n- and p-type, on Schottky barrier height has been investigated with different work-function metals (Al, Ni, Ti, Cr). It is found that S passivation of Si(100) reduces the density of surface states by more than an order of magnitude. This reduction in surface-state density results in changes in Schottky barrier height, which are more sensitive to the work function of the chosen metal. These experimental results suggest that surface states play the dominant role over surface dipoles in controlling the Schottky barrier height in these metal-Si systems.

CHAPTER 5

FABRICATION OF DOPING-FREE MOSFET

5.1 Introduction

In this chapter the operating principle of a conventional MOSFET is explained. The concept of a doping-free p-n junction is presented. It then provides the process flow and detailed description of the process steps for the fabrication of doping-free MOSFET. During the process of fabrication, the optimization of different steps are also provided. Finally the source/drain characteristics of the fabricated device is presented.

5.2 Principle of Operation

MOS (metal oxide semiconductor) capacitor [79] is at the heart of MOSFET operation. Figure 5.1 shows the cross section of an Al/SiO_2/Si MOS capacitor.

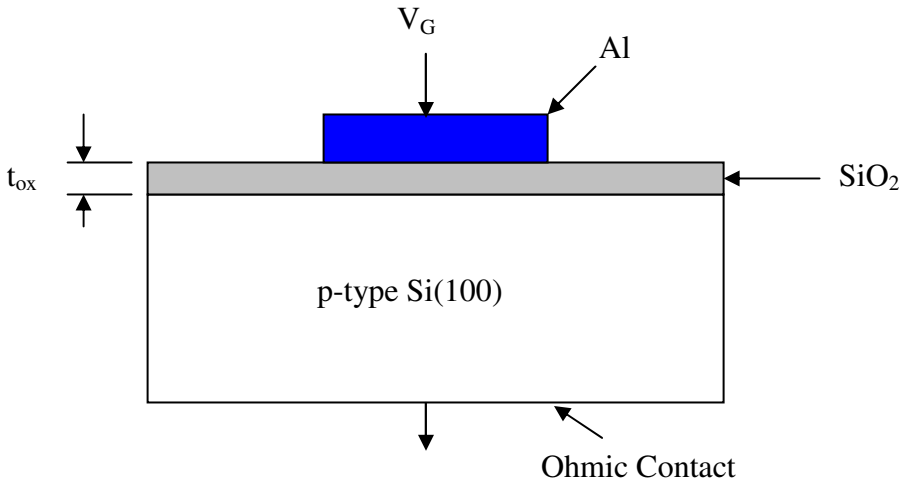


Figure 5.1 Cross section of an Al/SiO_2/Si MOS capacitor

Here t_{ox} is the thickness of the SiO_2 layer, Vg is the voltage on the Al electrode and the bottom is considered as an ohmic contact which is grounded. Several key terms like flat-band voltage, accumulation, inversion and threshold voltage will be explained with regard to this structure. Figure 5.2 shows the energy-band diagram of an isolated metal(Al) adjacent to an isolated insulator (SiO_2) which is adjacent to an isolated semiconductor(p-type Si), where Φ_{Al} is the work function of aluminum, χ_{ox} and χ_{Si} are

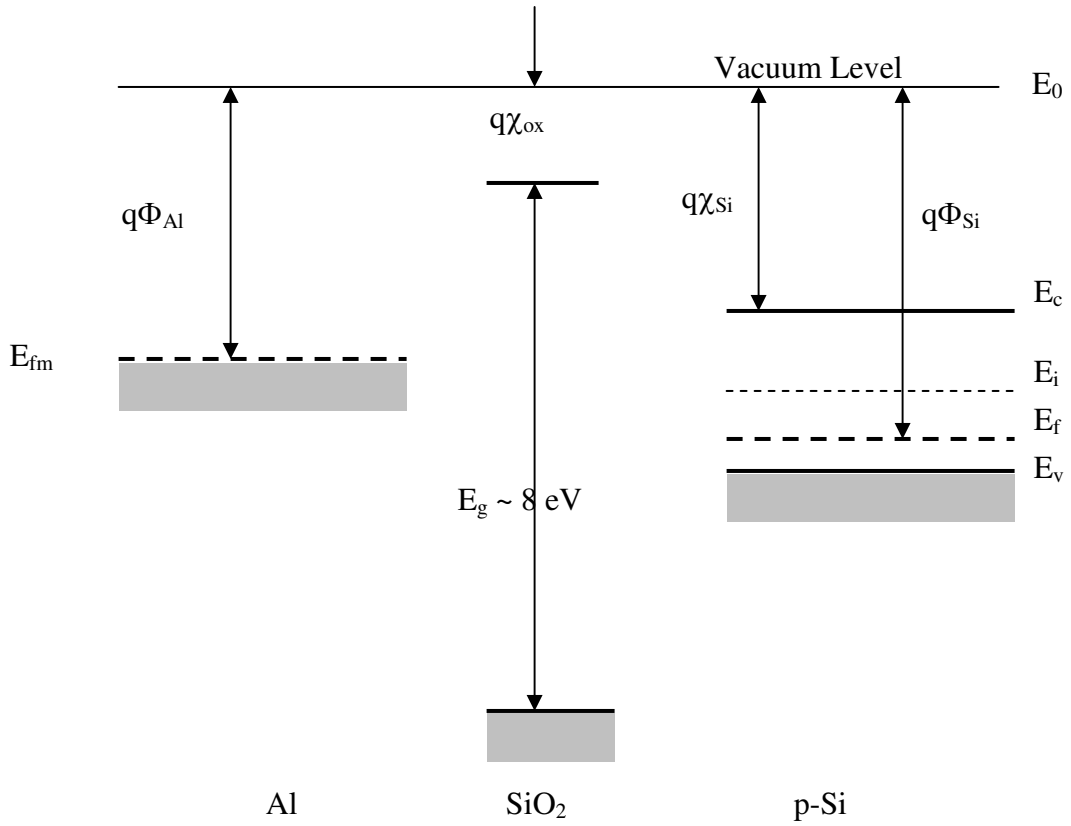


Figure 5.2 Band diagram in the isolated metal(Al), insulator(SiO_2) and semiconductor (p-type Si)

the electron affinities of SiO_2 and Si respectively, Φ_{Si} is the work function of Si, E_c is the conduction band minimum, E_i is the intrinsic level, E_f is the Fermi level, E_v is the

valence band maximum and E_o is the vacuum level. After the contact is made and at thermal equilibrium, the Fermi levels in the Al and semiconductor must be equal and the vacuum level must be continuous. These two requirements determine a unique energy-band diagram for the ideal MOS capacitor as shown in Figure 5.3. With the loss of electrons, Al will have a thin layer of positive charge at the metal-oxide interface, while the p-type Si will have a negative space charge due to ionized acceptors which are not neutralized by free holes. To accommodate the work function differences, the bands bend down.

To compensate the work function difference between the metal and the semiconductor, an external voltage with a certain polarity can be applied to the metal

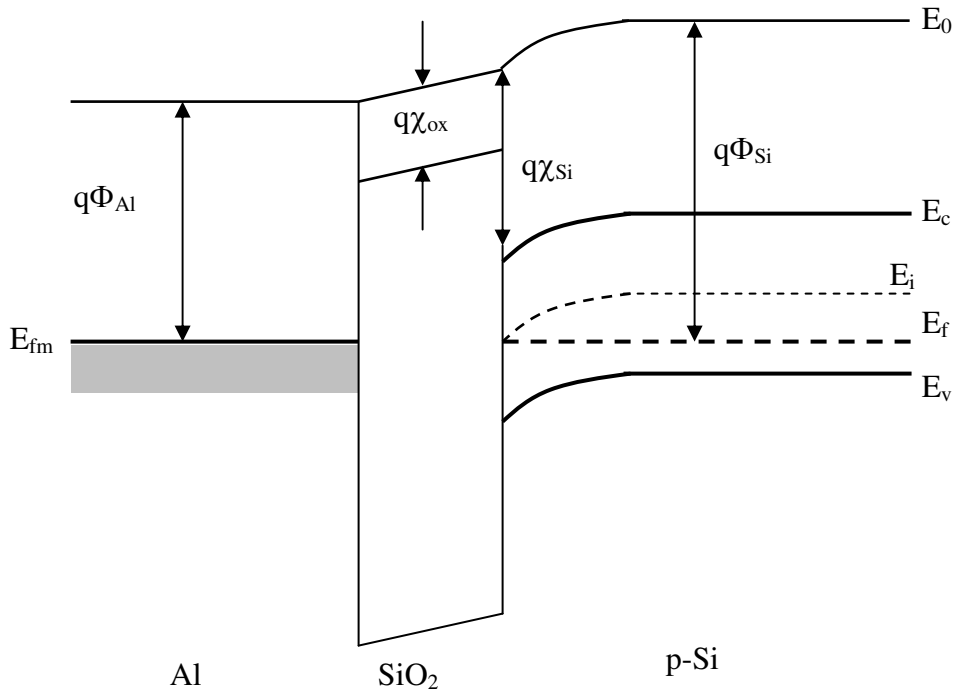


Figure 5.3 Energy-band diagram for an Al/ SiO_2/p-Si MOS capacitor at thermal equilibrium.

electrode and thus make the bands in the semiconductor flat, which is known as the flat band condition. This applied voltage to achieve the flat bands is called the flat-band voltage. The ideal flat-band voltage V_{FB} is the work function difference as given by the following equation:

$$V_{FB} = \Phi_M - \Phi_S \tag{5.1}$$

The sign of the difference of the metal and semiconductor work functions gives the polarity connected to the metal to obtain the flat-band condition.

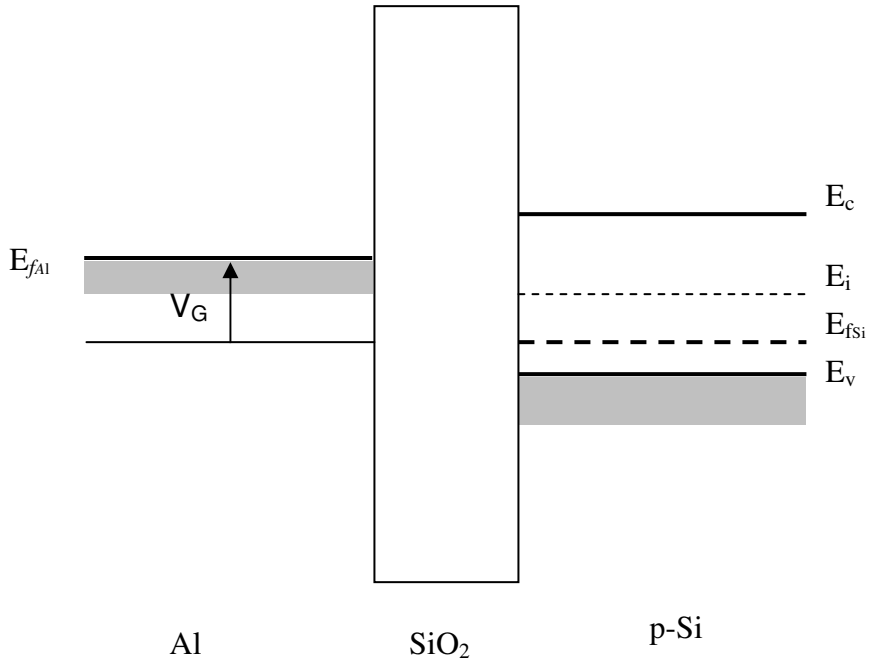


Figure 5.4 Energy-band diagram of MOS capacitor for flat-band condition

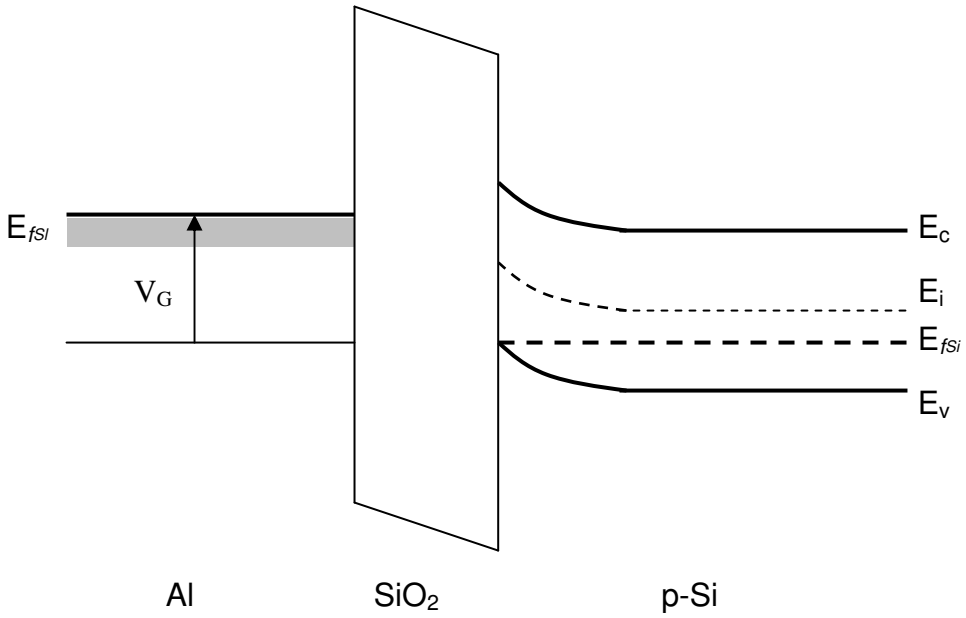


Figure 5.5 Energy-band diagram for an ideal MOS capacitor in accumulation condition.

For the case of $|Vg| \neq V_{FB}$, two important phenomena can be observed. When the negative Vg is increased so that $|Vg| > V_{FB}$, a larger hole concentration takes place at the surface than in the p-type bulk, which is known as accumulation. Figure 5.5 shows the energy-band diagram of a MOS capacitor in the accumulation condition. When the positive Vg is increased gradually, the majority carriers are depleted from the semiconductor surface and this is called the depletion condition. When a larger positive voltage is applied, the bands bend downward so much that the intrinsic level at the surface crosses over the Fermi level. At this point the number of electrons at the surface is larger than that of the holes, and the surface is thus inverted.

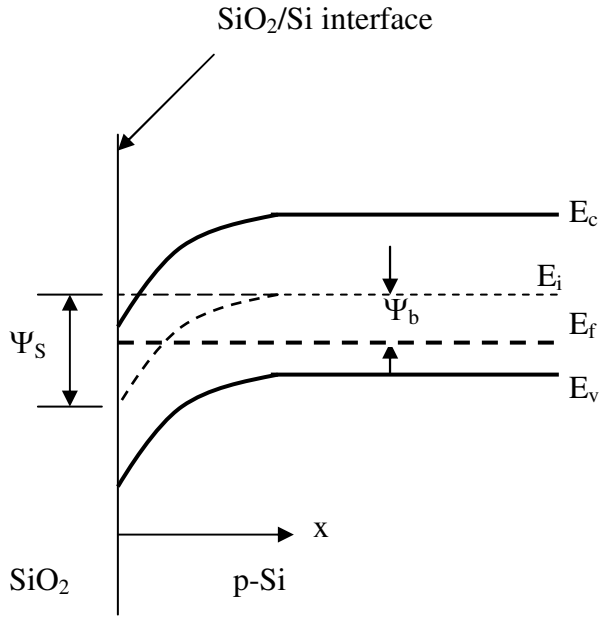


Figure 5.6 Energy-band diagram of the semiconductor side at the condition of strong inversion.

The threshold voltage of strong inversion or the turn on voltage of an n-MOSFET is defined as [79]

$$V_{Tn} = V_{FB} + 2|\psi_b| + \frac{\sqrt{4q\varepsilon_{Si}N_a^-|\psi_b|}}{(\varepsilon_{ox}/t_{ox})} \tag{5.2}$$

Where V_{Tn} is the threshold voltage, V_{FB} is the ideal flat-band voltage, Ψ_b is the potential difference between the Fermi level and the intrinsic level as shown in Fig. 5.6, N_a is the doping concentration, t_{ox} is the oxide thickness, ε_{Si} and ε_{ox} are the permittivities of silicon and oxide respectively.

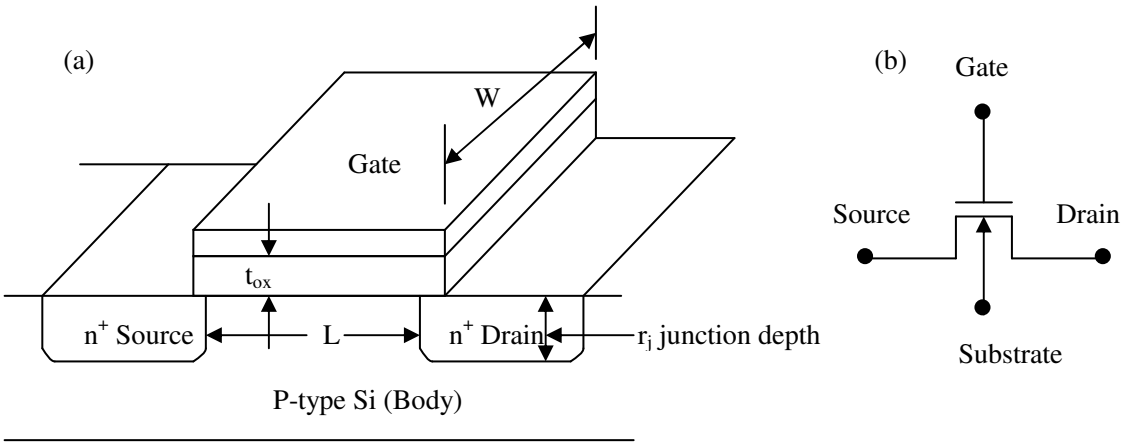


Figure 5.7 (a) Basic MOSFET structure, (b) MOSFET circuit symbol

Figure 5.7 shows the basic MOSFET (metal-oxide-semiconductor field effect transistor) structure. It is a four terminal device and consists of a p-type (for n channel) semiconductor substrate into which two n regions, the source and drain are formed. The metal contact on the insulator is called the gate. Heavily doped polysilicon or a combination of silicide and polysilicon can also be used as the gate electrode. The basic device parameters are the channel length L, which is the difference between the two metallurgical n-p junctions; the channel width Z, the insulator thickness d, the junction depth r_j, and the substrate doping N_a.

When a voltage is applied across a MOS structure, it modifies the distribution of charges in the semiconductor. For a P-type semiconductor, a positive voltage, V_{GS}, from gate to source creates a depletion layer by forcing the positively charged holes away from the gate-insulator/semiconductor interface, leaving exposed a carrier-free region of

immobile, negatively charged acceptor ions. When V_{GS} is greater than threshold voltage (V_{th}), a high concentration of negative charge carriers forms in an inversion layer located in a thin layer next to the interface between the semiconductor and the insulator. When a voltage is applied across source and drain, electrons from source can flow to the drain through the inversion layer, which constitute the drain current I_D.

The operation of a MOSFET can be divided into three different modes, cutt off region, linear region and saturation region, depending on the voltages at the terminals. For an enhancement-mode, n-channel MOSFET the three operational modes are:

(i) Cut-off or Sub-threshold or Weak Inversion Mode:

When $V_{GS} < V_{th}$, the MOSFET is said to be in the cut-off region. According to the basic threshold model, the transistor is turned off, and there is no conduction between drain and source. In reality, the Boltzmann distribution of electron energies allows some of the more energetic electrons at the source to enter the channel and flow to the drain, resulting in a subthreshold current that is an exponential function of gate–source voltage. While the current between drain and source should ideally be zero when the transistor is being used as a turned-off switch, there is a weak-inversion current, which is called subthreshold leakage. In weak inversion the current varies exponentially with gate-to-source bias V_{GS}. The subthreshold current is given by [32]

$$I_D = \mu_n \frac{W}{L} \frac{aC_{ox}}{2\beta^2} \left(\frac{n_i}{N_A} \right)^2 \left(1 - e^{-\beta V_D}\right) e^{\beta \Psi_S} \left(\beta \Psi_S\right)^{1/2} \tag{5.3}$$

where μ_n is the carrier effective mobility, W is the gate width, L is the gate length and C_{ox} is the gate oxide capacitance per unit area, a is a constant, n_i is the intrinsic carrier

concentration, N_a is the substrate doping, V_D is the voltage across source and drain ψ_S is the surface potential and β is the thermal voltage.

(ii) Triode Mode or Linear Region (also referred to as the Ohmic Mode):

When $V_{GS} > V_{th}$ and $V_{DS} < (V_{GS} - V_{th})$, the MOSFET is said to be in the linear region. The transistor is turned on, and a channel has been created which allows current to flow between the drain and source. The MOSFET operates like a resistor, controlled by the gate voltage relative to both the source and drain voltages. The current from drain to source is modeled as:

$$I_D = \mu_n C_{ox} \frac{W}{L}\left((V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right) \tag{5.4}$$

Where the notations have their usual meaning.

(iii) Saturation Mode (also referred to as the Active Mode):

When $V_{GS} > V_{th}$ and $V_{DS} > (V_{GS} - V_{th})$, the MOSFET is said to be in the saturation region. Now, the MOSFET as a switch is turned on, and a channel has been created, which allows current to flow between the drain and source. Since the drain voltage is higher than the gate voltage, the electrons spread out, and conduction is not through a narrow channel but through a broader, two- or three-dimensional current distribution extending away from the interface and deeper in the substrate. The onset of this region is also known as pinch-off to indicate the lack of channel region near the drain. The drain current is now weakly dependent upon drain voltage and controlled primarily by the gate–source voltage, and modeled very approximately as:

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}\left(V_{GS} - V_{th}\right)^2\left(1 + \lambda V_{DS}\right) \tag{5.5}$$

The additional factor involving λ, the channel-length modulation parameter, models current dependence on drain voltage due to the Early effect, or channel length modulation.

5.3 Doping-Free Approach

A p-n junction is usually formed by doping a p-type semiconductor with an n-type impurity or an n-type semiconductor with a p-type impurity as shown in Fig. 5.8. Doping can be done either by diffusion or by ion implantation followed by annealing. In both cases, it involves the application of high temperature in the range of 1000^o C for a significant amount of time depending on the process requirements [80]. As discussed in chapter 1 that in a conventional MOSFET fabrication, this high temperature doping step is required to form the source/drain region, which is basically a p-n junction.

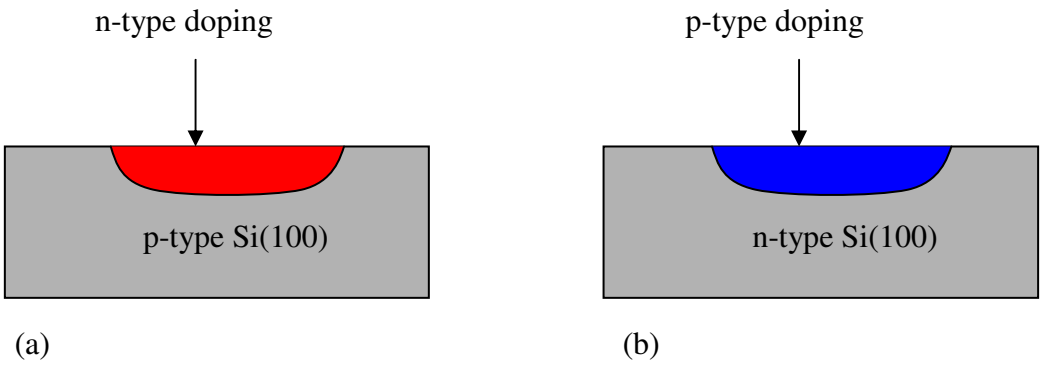


Figure 5.8 Formation of p-n junction by doping (a) n-type on p-type Si and (b) p-type on n-type Si.

In this work, the high-temperature doping step that is used to form the p-n junction for the source/drain contact in the conventional MOSFET fabrication will be

replaced and the p-n junction will be formed by engineering the S/D region by valence-mending technique. According to Schottky-Mott theory, if a low work function metal is deposited on a p-type Si(100), the Schottky barrier will be very high and if ϕ_m is low enough, the surface band-bending will be so high that the surface of p-type Si(100) will be inverted and a p-n junction will be formed. Figure 5.9(a) shows this kind of band diagram with a low work function metal on p-type Si(100) to form the p-n junction. In this case the surface is n-type and the bulk is the p-type. The junction depth can be defined as the point where the intrinsic level intersects the Fermi level as shown in that figure. Figure 5.9(b) shows the formation of p-n junction with a high work-function metal on n-type Si(100). In this case the surface is p-type and the bulk is the n-type. Our experimental results show that such a doping-free formation of p-n junction is possible with Al (ϕ_m = 4.28 eV) on S-passivated p-type Si(100). Figure 10 shows the barrier height measurement for Al on S-passivated Si(100) from capacitance-voltage measurement [81]. From this C-V measurement, we get a very high surface band-bending of ~ 0.98 eV, which gives a barrier height of ~1.1 eV [81].

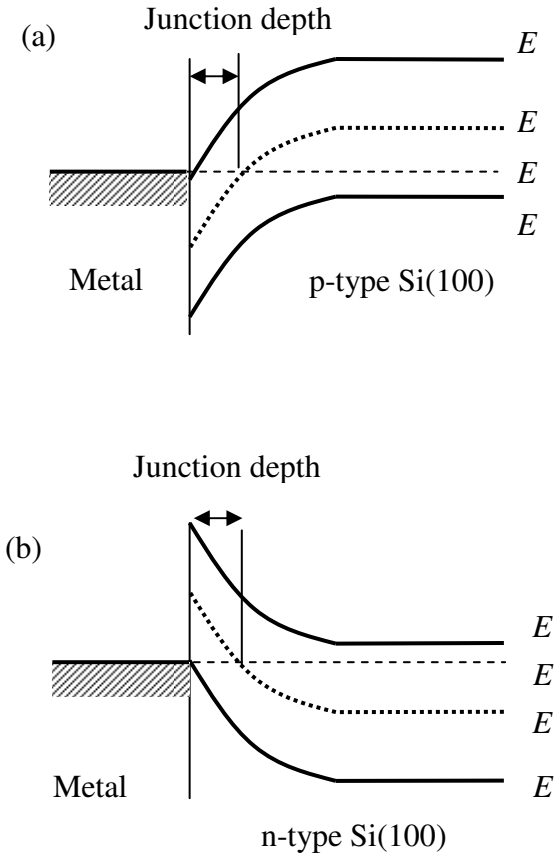


Figure 5.9 Band diagrams for doping-free formation of p-n junction. (a) A low work-function metal on S-passivated p-type Si(100), (b) a high work-function metal on S-passivated n-type Si(100).

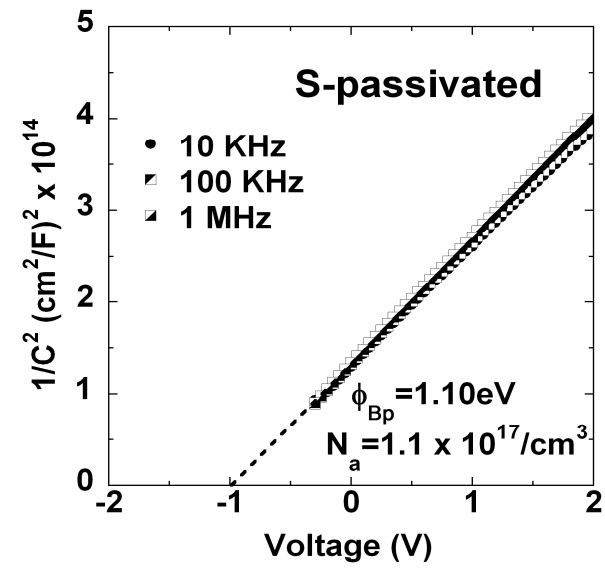


Figure 5.10 Extraction of Schottky-barrier height from $1/C^2$ – V plot for Al/S-passivated p-type Si(100)

The achievement of this high barrier proves the theoretical band diagram of Fig. 5.9(a) and lays the foundation for the fabrication of low-temperature doping-free MOSFET.

5.4 Process Flow for Doping-Free MOSFET

Figure 5.11, 5.12, 5.13 and 5.14 show the different steps in the process flow for the fabrication of doping-free MOSFET. The steps are explained in the next section.

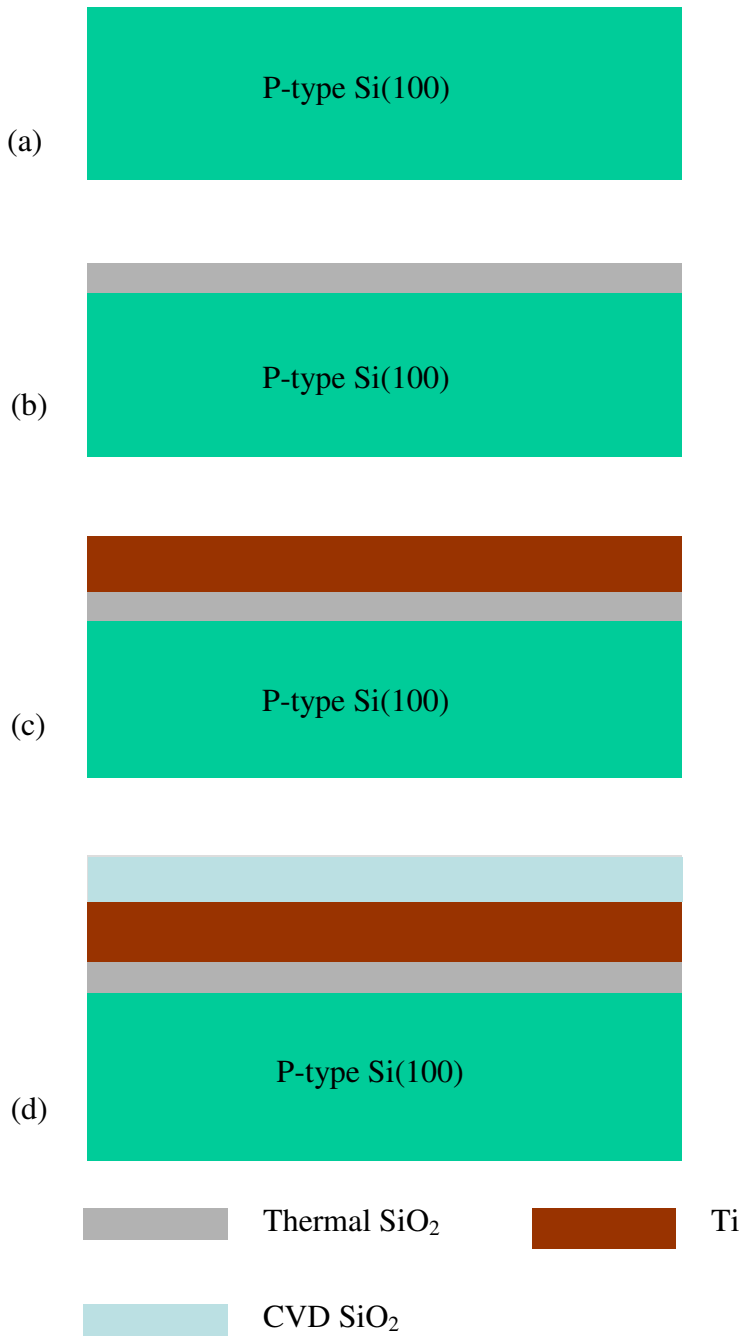


Figure 5.11 Process flow for doping-free MOSFET. (a) p-type starting wafer, (b) thermal oxide growth, (c) Ti deposition and (d) CVD oxide deposition.

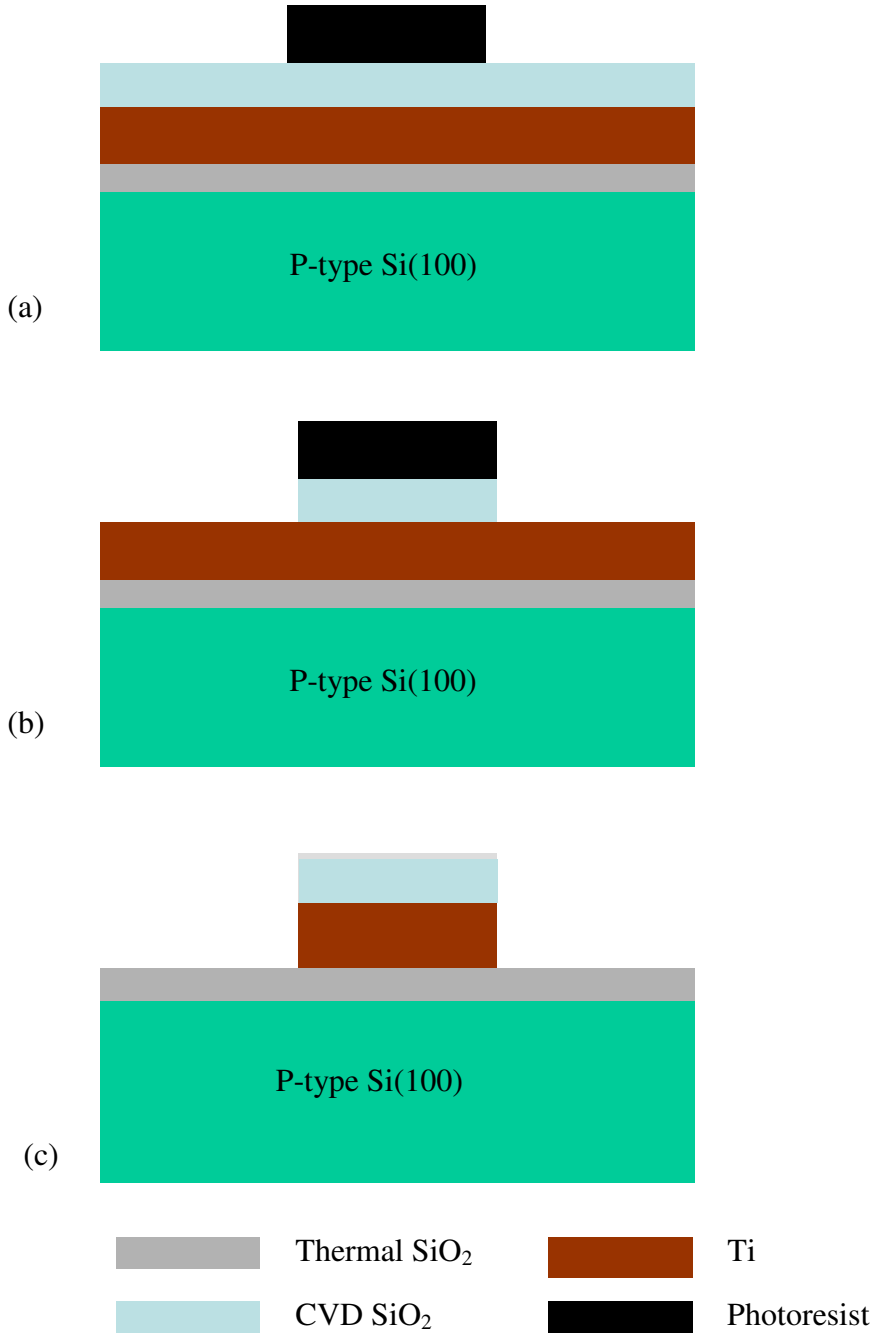


Figure 5.12 (a) photoresist deposition and patterned, (b) CVD oxide etched in RIE and (c) Ti etched in wet etchant.

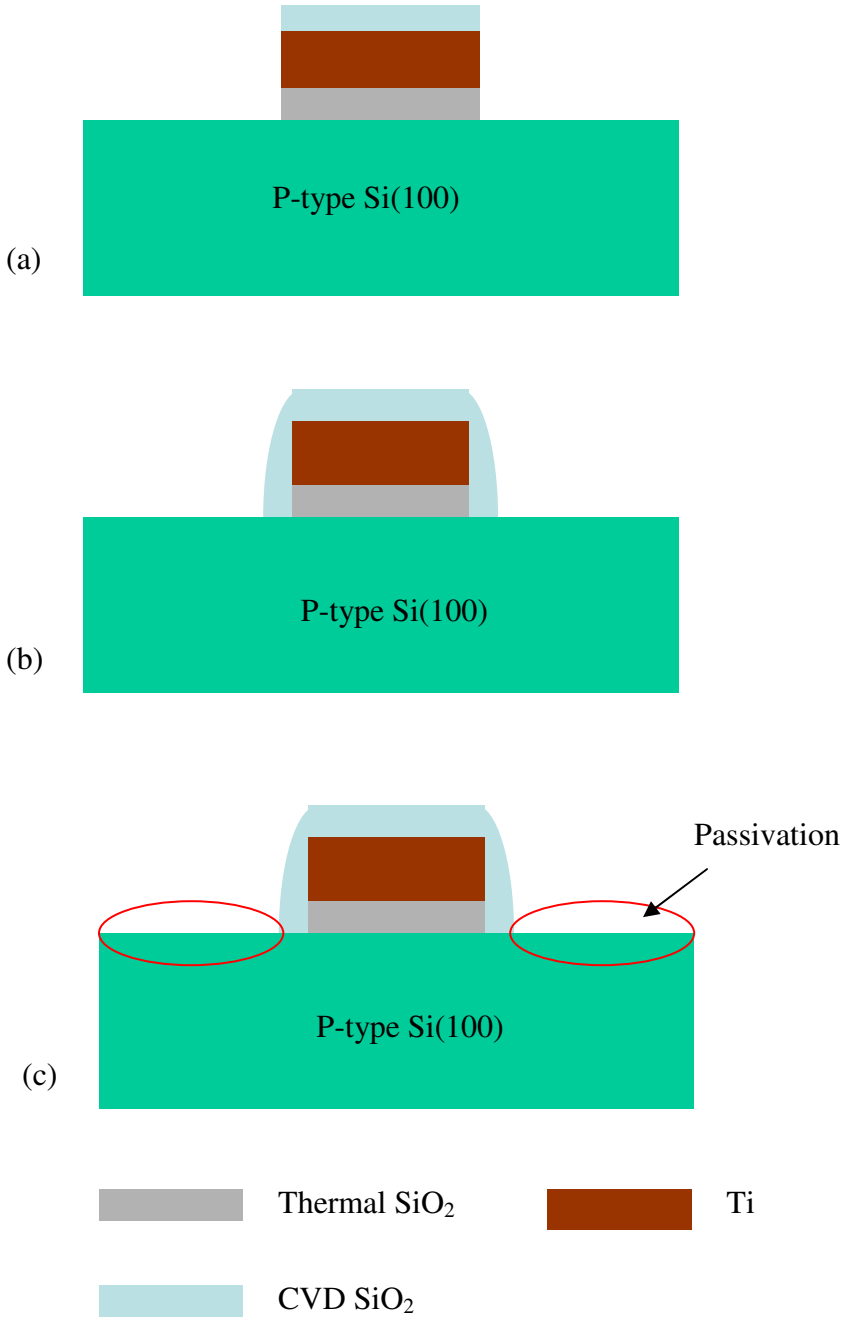


Figure 5.13 (a) thermal oxide etched in RIE, (b) spacer formation and (c) passivation is carrier out in the S/D region.

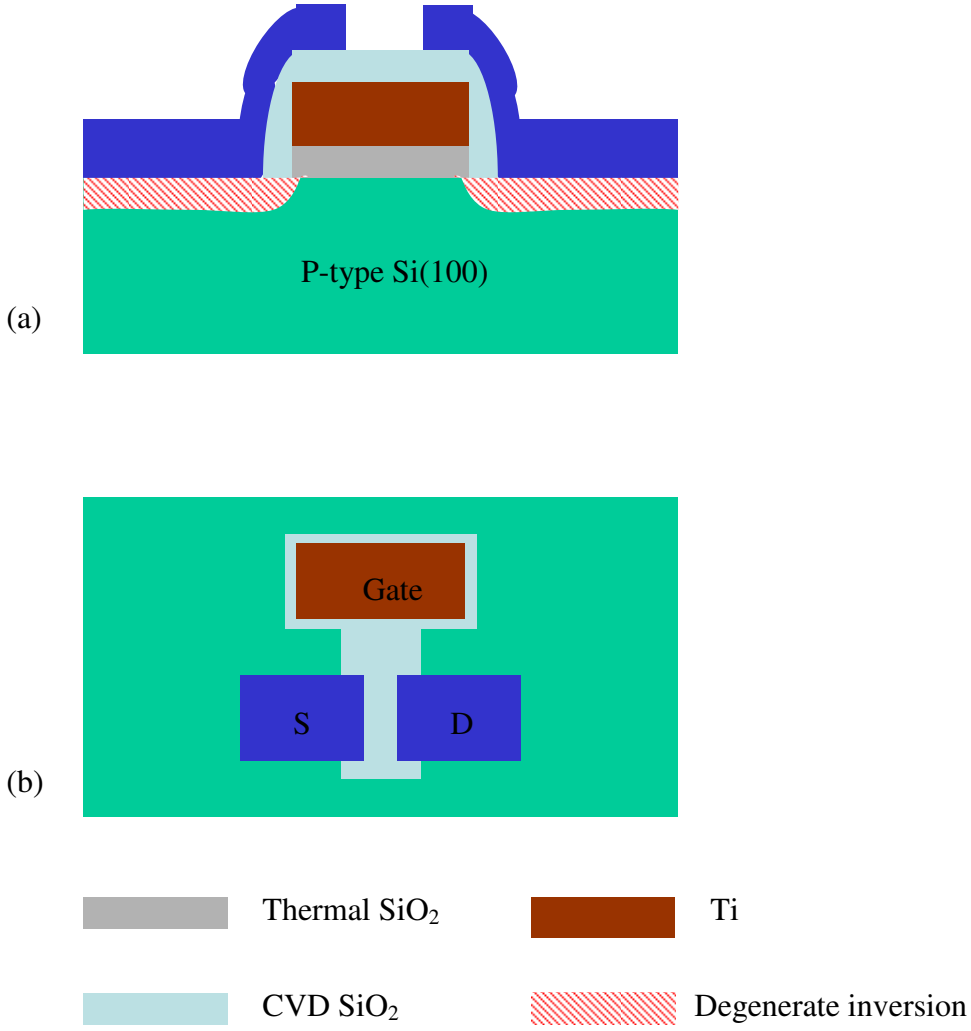


Figure 5.14 (a) S/D metal deposition and (b) opening of gate contact.

5.5 Fabrication and Characterization

The fabrication steps of the doping-free MOSFET are provided below.

Step 1: Si(100) wafer of p-type was used for the experiments. The p-type wafer was doped with boron in the low 10^{17} cm^{-3}. The nominal wafer miscut was less than 0.5°. The wafer was cleaned in 2% HF (Figure 5.11 (a)).

Step 2: A thin layer (~20 nm) of silicon dioxide is grown in thermal oxidation at about 850^{o} C as the gate oxide (Figure 5.11 (b)).

Step 3: The wafer was then transferred to the EBEAM evaporator to deposit Ti as the gate electrode. About 80 nm of Ti is deposited for this purpose (Figure 5.11 (c)).

Step 4: The wafer is then transferred to the CVD chamber for the deposition of CVD oxide. About 70 nm of CVD oxide is grown to isolate the gate electrode from subsequent processing (Figure 5.11 (d)). The optimization of the CVD oxide deposition condition is provided in the next section.

Step 4: Then photoresist is deposited and patterned using Mask 1 (Figure 5.12 (a)).

Step 5: The wafer is then transferred to the RIE chamber to etch the CVD oxide, where the photoresist acts as the mask (Figure 5.12 (b)).

Step 6: The Ti layer is then etched in the Piranha solution, where the CVD oxide acts as the mask. In this step the Piranha solution removes all the photoresist (Figure 5.12 (c)). Piranha solution was made by a mixture of 50% sulfuric acid (H_2SO_4) and 50% hydrogen peroxide (H_2O_2).

Step 7: The wafer is then transferred to the RIE chamber again to etch the thermal oxide (Figure 5.13 (a)). In this step, the CVD oxide on top of Ti is also etched to some extant.

Step 8: In this step, the side wall spacer is formed by depositing a thin (~30 nm) conformal CVD oxide and then doing an anisotropic etch (Figure 4.13 (b)). By forming this side wall spacer, the gate metal is totally encapsulated from the source/ drain metal.

Step 9: In this step, the wet chemical passivation is carried out as explained in chapter 3 (Figure 4.13 (c)).

Step 10: Now the source/drain metal (in this case Al) is deposited and patterned using Mask 2. Thus the source and the drain regions are separated from each other (Figure 4.14 (a)).

Step 11: Then the opening of gate contact is done using Mask 3. In this step first lithography is done to open a contact in the gate region and then by doing RIE the oxide on top of gate metal is removed and finally the photoresist is removed by dipping the wafer in acetone (Figure 4.14 (b)).

Step 12: In this final step, Al is deposited on the backside for back ohmic contact.

In the process of fabricating the whole device, several process steps had to be optimized. Those are discussed below:

PhotoLithography: Photolithography is a very crucial step in any fabrication process. In this case, the step of isolating the source/drain regions is very crucial. The minimum isolation space is 1 μm, which is hard to achieve in our clean room. The optimized parameters for the photolithography using negative resist NR7 is provided below:

- Spin coating at 3.5 K for 40 seconds
- Soft bake at 110^{o} C for 2 minutes
- Exposure for 20 seconds. It depends on the UV power supply.
- Hard bake at 110^{o} C for 1 minute
- Develop in RD6 for 35 seconds

Figure 5.16 shows the different isolation spacing with the optimized parameters for the photolithography.

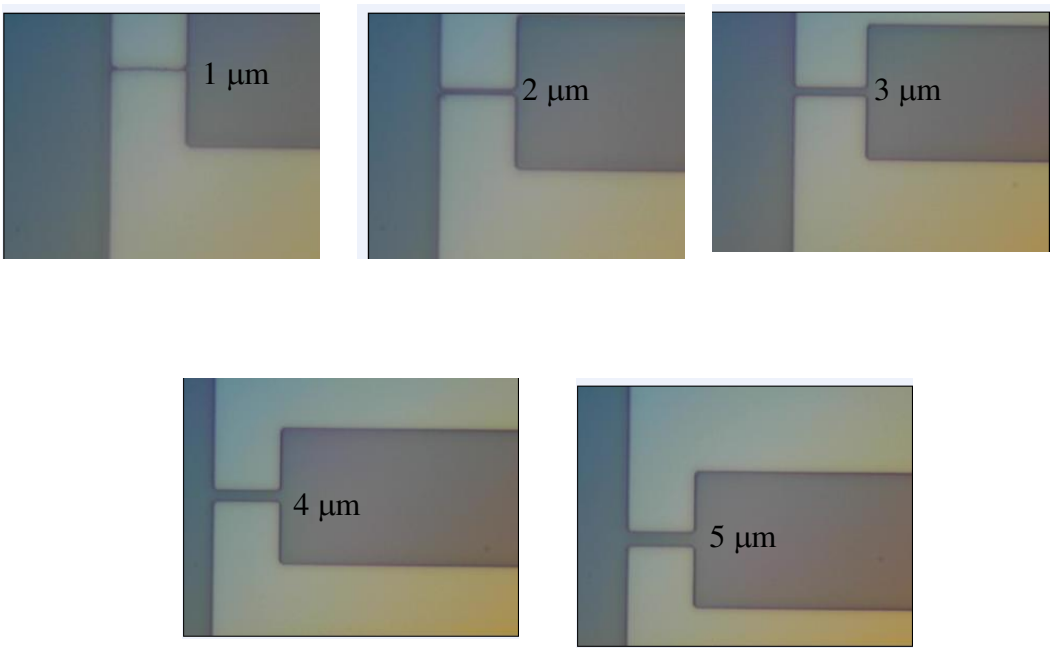


Figure 5.15 Different isolation spacing for source/drain isolation

Determination of etch rate of thermal oxide:

The etch rate of thermal oxide was determined in both RIE and 2% HF. The recipe for the RIE is provided below:

- RF power = 50 w
- CF_4 flow rate = 5 SCCM
- Base pressure = 10 mT
- Process pressure = 130 mT

Figure 5.16 shows the etch rate of thermal oxide in RIE. The etch rate was found to be 2.4 Å/Sec with the mentioned recipe.

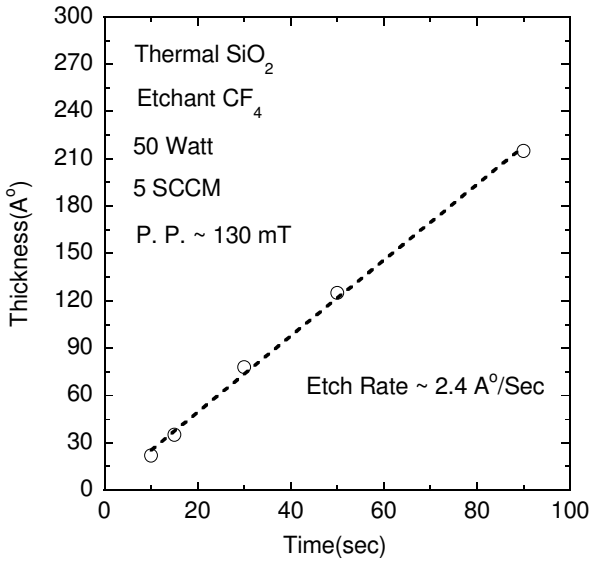


Figure 5.16 Determination of etch rate of thermal oxide in RIE

The etch rate was also determined in 2% HF. Figure 5.17 shows the etch rate of thermal oxide in 2% HF. The etch rate was found to be ~ 0.81 Å/Sec.

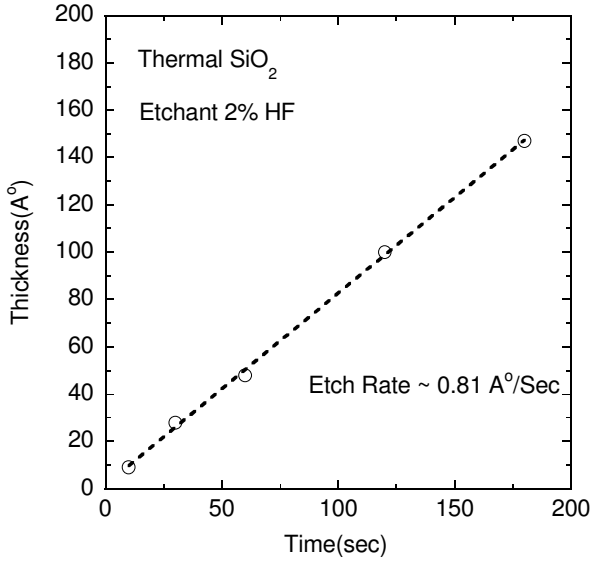


Figure 5.17 Determination of etch rate of thermal oxide in 2% HF

The etch rate of the initial CVD oxide (before optimization) was determined in both RIE and in 2% HF. Figure 5.18 shows the etch rate of this CVD oxide in RIE and the etch rate was found to be ~ 4 Å/Sec. Figure 5.19 shows the etch rate of this CVD oxide

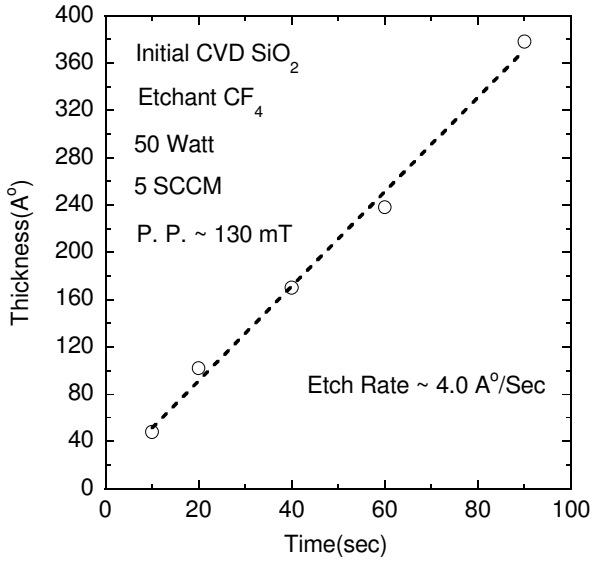


Figure 5.18 Determination of etch rate of CVD oxide in RIE

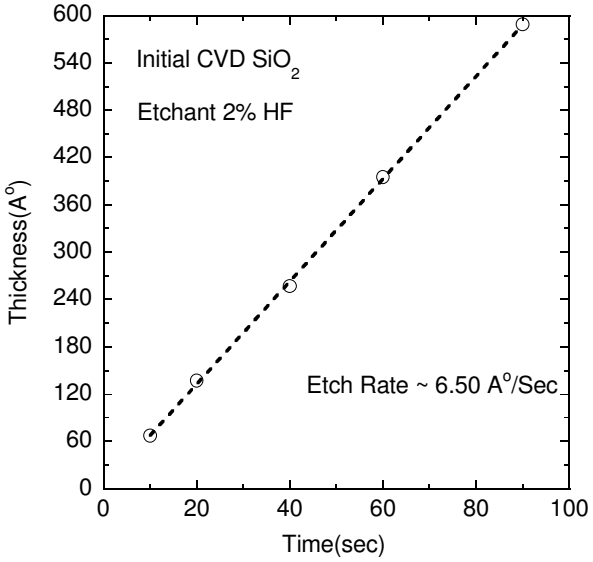


Figure 5.19 Determination of etch rate of CVD oxide in 2% HF

in 2% HF and the etch rate was found to be ~ 6.5 Å/Sec. Then the parameters for the deposition of CVD oxide were optimized. With that optimized parameters, the etch rate of the CVD oxide was determined both in RIE and in 2% HF. Figure 5.20 shows the

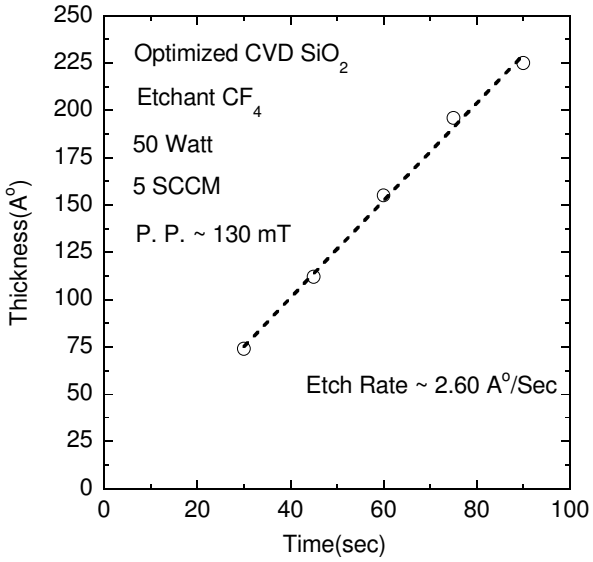


Figure 5.20 Determination of etch rate of optimized CVD oxide in RIE

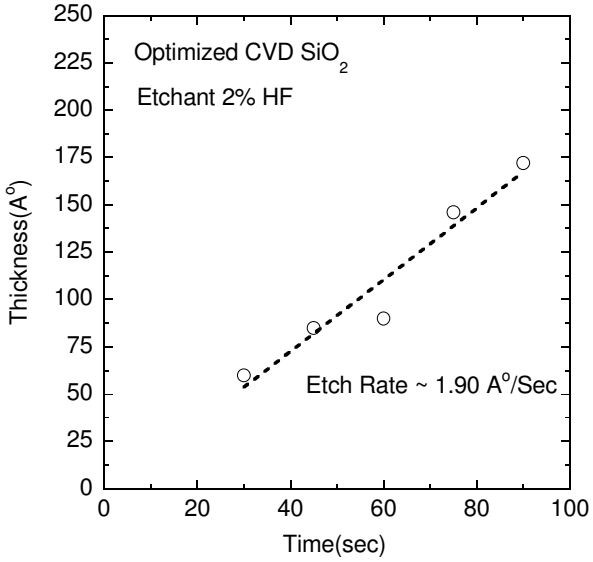


Figure 5.21 Determination of etch rate of optimized CVD oxide in 2% HF

etch rate of the optimized CVD oxide in RIE and the etch rate was found to be ~ 2.6 Å/Sec, which was ~ 4 Å/Sec in the unoptimized case. Figure 5.21 shows the etch rate of optimized CVD oxide in 2% HF. The etch rate was found to be 1.9 Å/Sec, which was ~ 6.5 Å/Sec in the unoptimized case. So a significant improvement in the etch rate was found by optimizing the parameters, which are as follows:

- Power ~ 500 Watt
- Temperature ~ 350^{o} C
- Flow of SiH_4 ~ 5 SCCM
- Flow of N_2O ~ 179 SCCM
- Flow of N_2 ~ 250 SCCM

In an effort to further reduce the etch rate of CVD oxide in 2% HF, the deposited oxide was annealed at 800^{o} C for 2 minutes in the RTA chamber. Figure 5.22 shows the etch

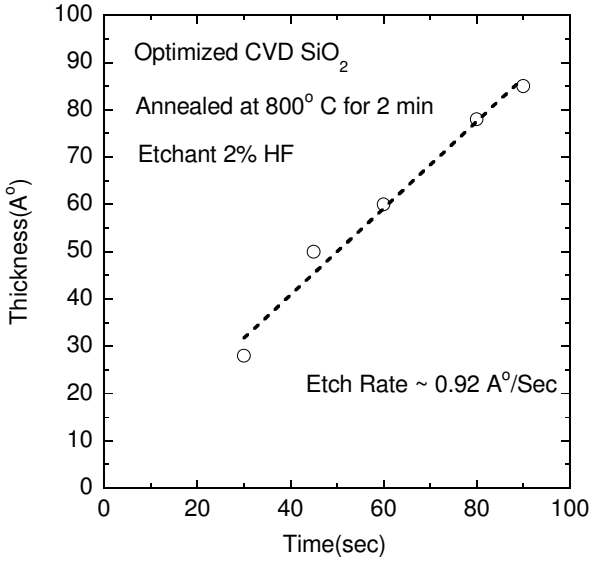


Figure 5.22 Determination of etch rate of CVD oxide after annealed at 800^{o} C for 2 min in 2% HF

rate of this annealed CVD oxide in 2% HF. It was found that the etch rate went down to ~ 0.92 Å/Sec, which is close to the etch rate of thermal oxide. But during the fabrication process, the CVD oxide is deposited on Ti. So after the 800^{o} C anneal step, it was found the Ti layer was oxidized, and it was hard to make contact with the Ti layer. So this annealing step was not used in the fabrication process.

The CVD oxide was also characterized by current-voltage measurement, from which the breakdown voltage was measured. Figure 5.23 shows the I-V characteristics of CVD oxide for SiH_4 flow rate of ~ 2 SCCM. The breakdown field was found to be ~6.66 MV/cm. It also shows low leakage current.

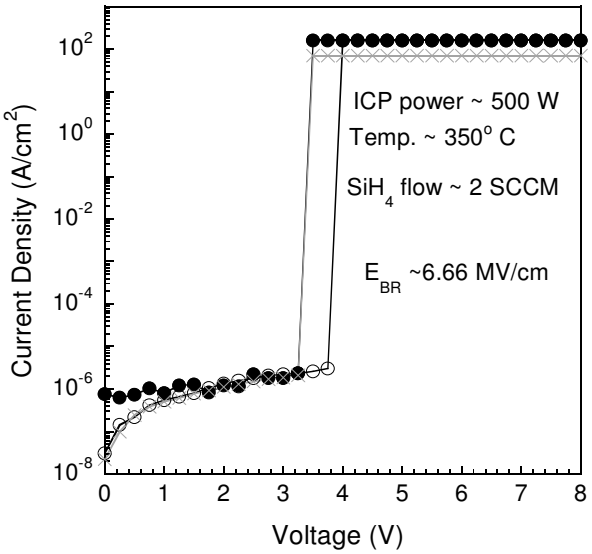


Figure 5.23 I-V characteristics of CVD oxide for SiH_4 flow rate of ~ 2 SCCM

Figure 5.24 shows the I-V characteristics of CVD oxide for SiH_4 flow rate of ~ 5 SCCM. The breakdown field was found to be ~6.77 MV/cm but leakage current is found to be much higher than that in Fig. 5.23.

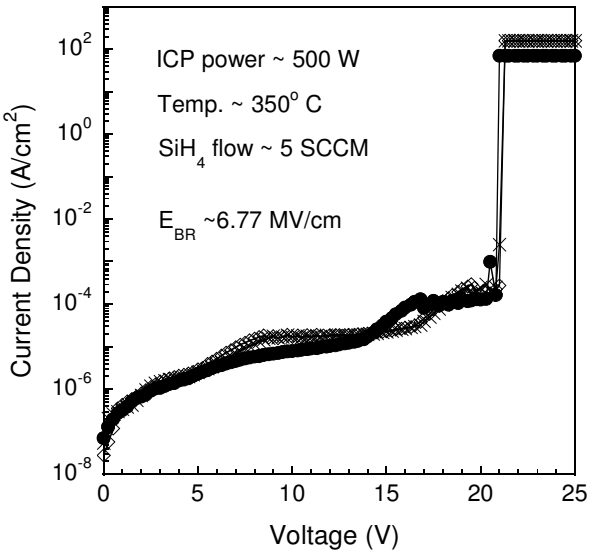


Figure 5.24 I-V characteristics of CVD oxide for SiH_4 flow rate of ~ 5 SCCM

Figure 5.25 shows the I-V characteristics of CVD oxide for SiH_4 flow rate of ~ 10 SCCM. The breakdown field was found to be ~6.60 MV/cm but leakage current is found to be higher than those in Fig. 5.23 and Fig. 5.24. It is observed from this I-V analysis that the higher the SiH_4 flow rate, the higher the leakage. This is due to the fact that for higher SiH_4 flow rate, the Si content in the deposited film is higher, which causes the increased leakage.

Figure 5.26 shows the C-V characteristics of the gate oxide for different annealing condition. We can observe the positive oxide charge reduction [82] from this

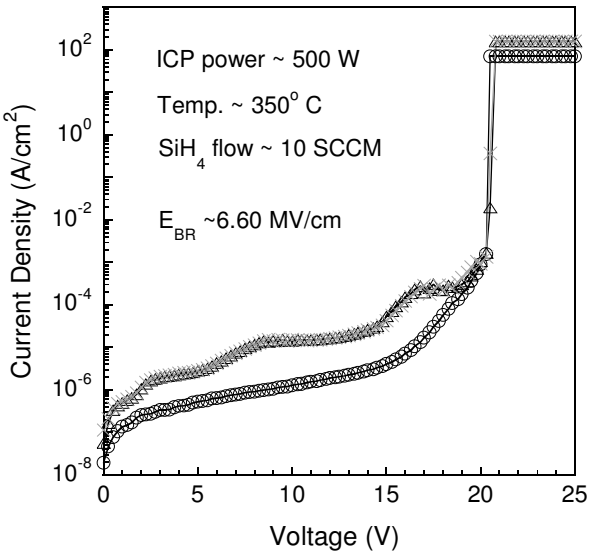


Figure 5.25 I-V characteristics of CVD oxide for SiH_4 flow rate of ~ 10 SCCM

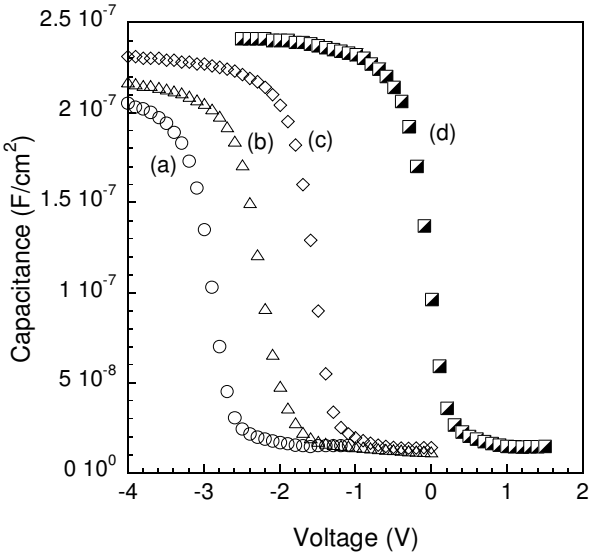


Figure 5.26 C-V characteristics of gate oxide for different annealing condition; (a) not annealed, (b) annealed for 10 min in N_2, (c) annealed for 20 min in N_2 and (d) annealed for 40 min in N_2.

figure. After the growth of the thermal oxide, if the wafer is taken out immediately without annealing in N_2 ambient, a very high amount of positive oxide charge is left, which is shown in Fig 5.26 (a). After annealing in N_2 ambient for 10 minutes (Fig. 5.26(b)) and 20 minutes (Fig5.26(c)), the reduction in positive oxide charge is well observed and the maximum reduction is found by annealing for about 40 minutes as shown in Fig. 5.26(d).

Figure 5.27 shows the masks that are used for the fabrication of a doping-free MOSFET. Fig. 5.27(a) is used to pattern the gate, Fig 5.27(b) is used to pattern the source/drain region and Fig. 5.27(c) is used to make the opening for the gate contact.

Figure 5.28 shows the SEM image of a Si/SiO_2(thermal)/Al/SiO_2(CVD) structure which was annealed at 500^o C for 20 minutes. There is couple of things to notice here. First the top CVD oxide is porous and second as the melting point of Al is low, possibility is that Al can melt and come out through these holes. So Al can not be used at this step, which has to go through a temperature of 500^o C for passivation. Ti has a very high melting temperature, so Ti can be easily used for this purpose.

Figure 5.29 shows the SEM image of the gate structure (Si/SiO_2(thermal) /Ti/ SiO_2(CVD)) after the gate is patterned. The top layer is the CVD oxide used for isolation.

Figure 5.30 shows the SEM image of doping-free MOSFET after the whole structure is completed. The isolation of the source/drain region over the gate is clearly seen and the opening of the gate contact is also visible.

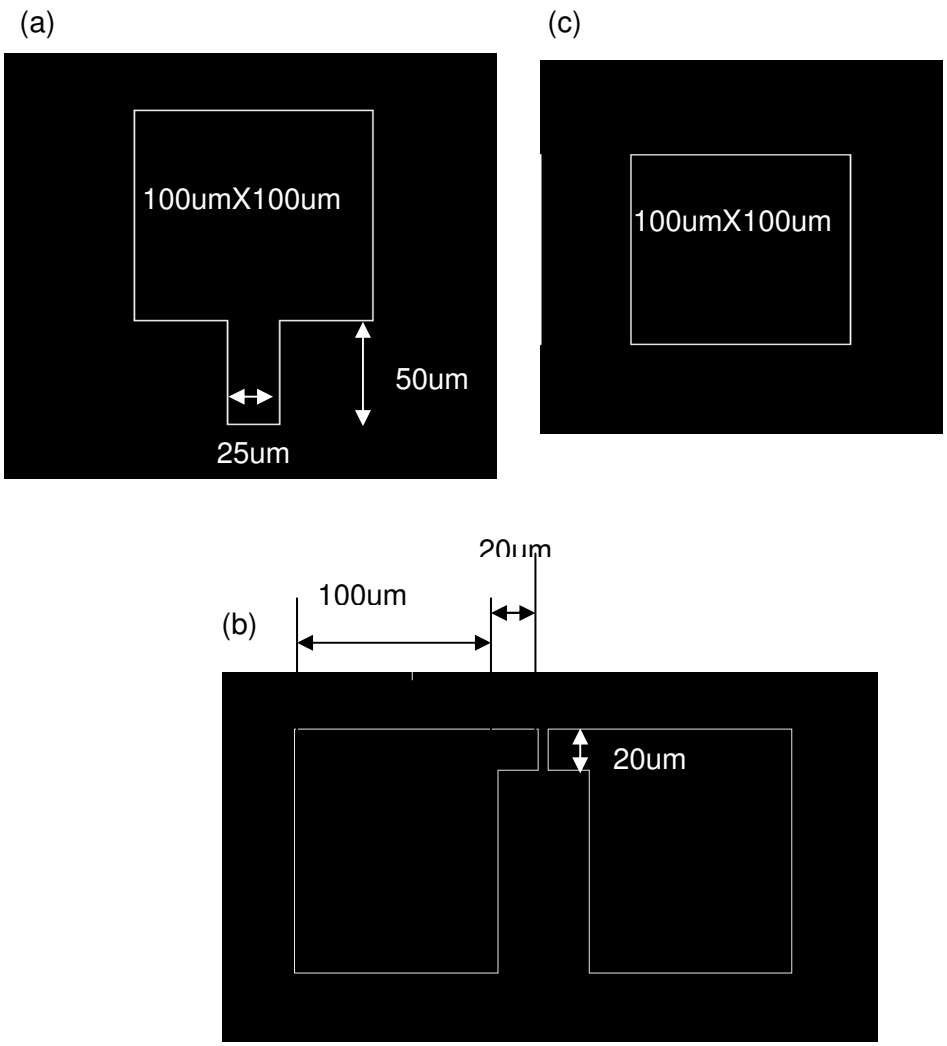


Figure 5.27 Schematic of mask for the fabrication of doping-free MOSFET; (a) gate formation, (b) source/drain contact formation and (c) gate contact opening.

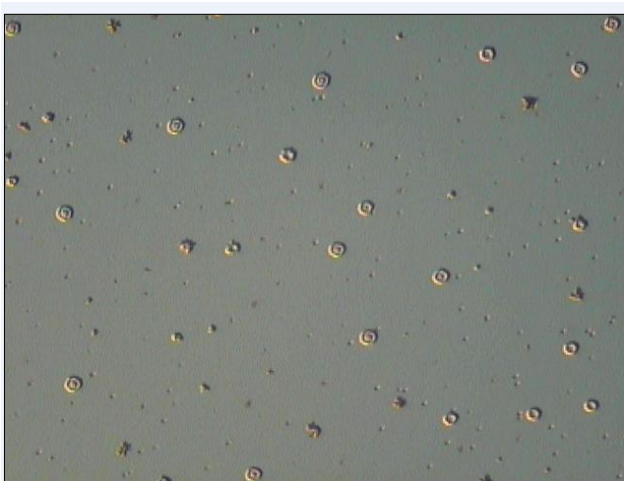


Figure 5.28 SEM image of Si/SiO_2(thermal)/Al/SiO_2(CVD) structure after annealing at 500^o C for 20 min.

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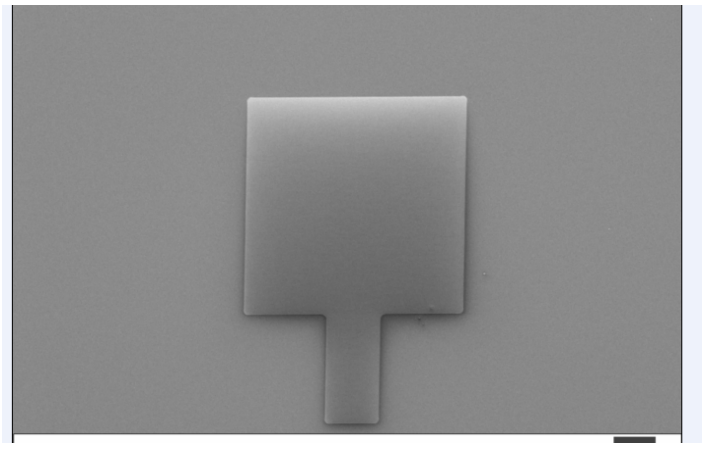


Figure 5.29 SEM image of gate structure (Si/SiO_2(thermal)/Ti/SiO_2(CVD))

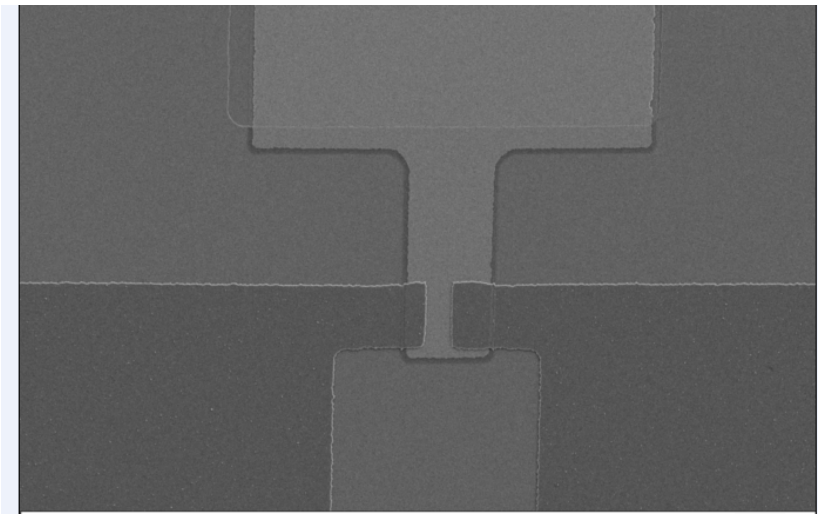


Figure 5.30 SEM image of the fabricated doping-free MOSFET.

Figure 5.31 shows the source/drain characteristics of the doping-free MOSFET. This is from an earlier stage fabrication and it is observed that the drive current is quite low. This drive current is intimately related to the quality of passivation in the source/drain region. So, efforts have been made to improve the quality of passivation, which is also limited by the facilities in our clean room too. The best result so far found is shown in Fig. 5.32. From Fig. 5.32 it is observed that the drive current improved to some extant but still kind of low.

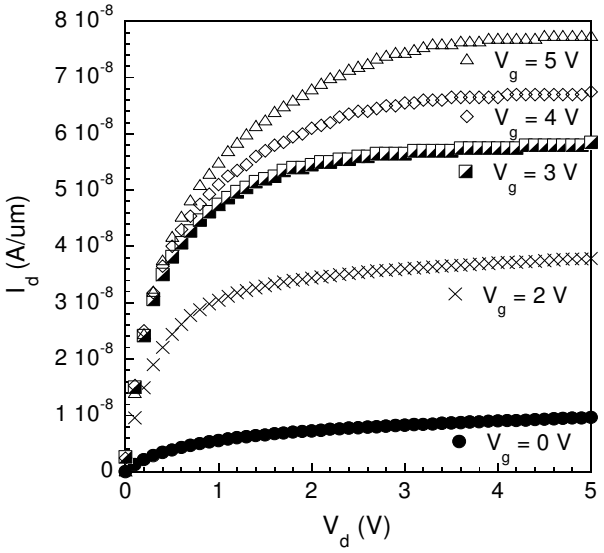


Figure 5.31 Source/drain characteristics of doping-free MOSFET (early stage)

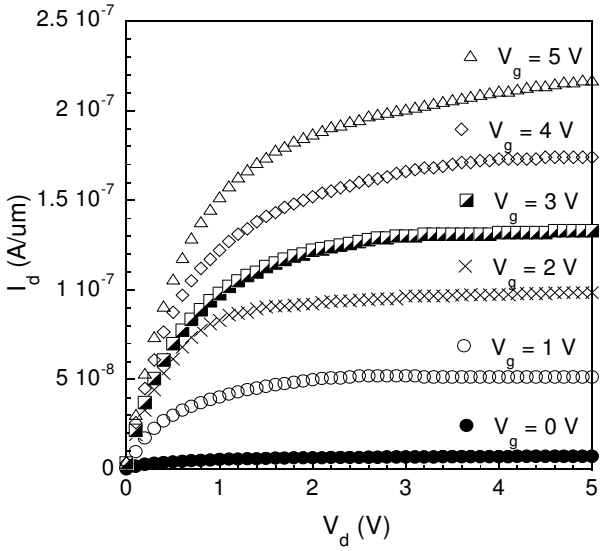


Figure 5.32 Improved source/drain characteristics of doping-free MOSFET

5.6 Summary

In this chapter, the basic operating principle of a MOSFET is explained. Then the doping-free approach is presented for the fabrication of doping-free MOSFET. Experimental verification of the doping-free formation of p-n junction is also presented. A detailed description of the fabrication process of doping-free MOSFET is provided. From the fabricated device, it is found that the drive current is not very high. A 2-D device simulation is provided in the next chapter to have an idea of the ideal characteristics of our doping-free MOSFET and a comparison is also made with our experimental results. In chapter 7, suggestions have also been made to improve the characteristics of our doping-free MOSFET.

CHAPTER 6

2-D NUMERICAL SIMULATION OF MOSFET

6.1 Introduction

2-D process and device simulations are used to get an idea of the ideal characteristics of this new energy efficient doping-free MOSFET. TSUPREM-4 is used for the process simulation and MEDICI is used for the device simulation, both of which are from Synopsys. The structure generated by TSUPREM-4 is passed to MEDICI for device simulation.

6.2 Process Simulation of Doping-Free MOSFET

The initial structure is defined as a rectangular region. The grid is then set. The grid can be set either by automatic gridding or by manual gridding. Here, automatic gridding is done. Without a grid structure or meshing, no process simulation can be done. The maximum number of nodes that can be implemented in TSUPREM-4 is 100,000. To implement the MOSFET structure, the MASK is defined in TLayout, which is also from Synopsys. Then the different process simulation statements are carried out to implement the MOSFET structure. A conventional MOSFET structure was also created by doing source/drain diffusion with a junction depth of ~0.19 μm to compare the results with the doping-free MOSFET structure.

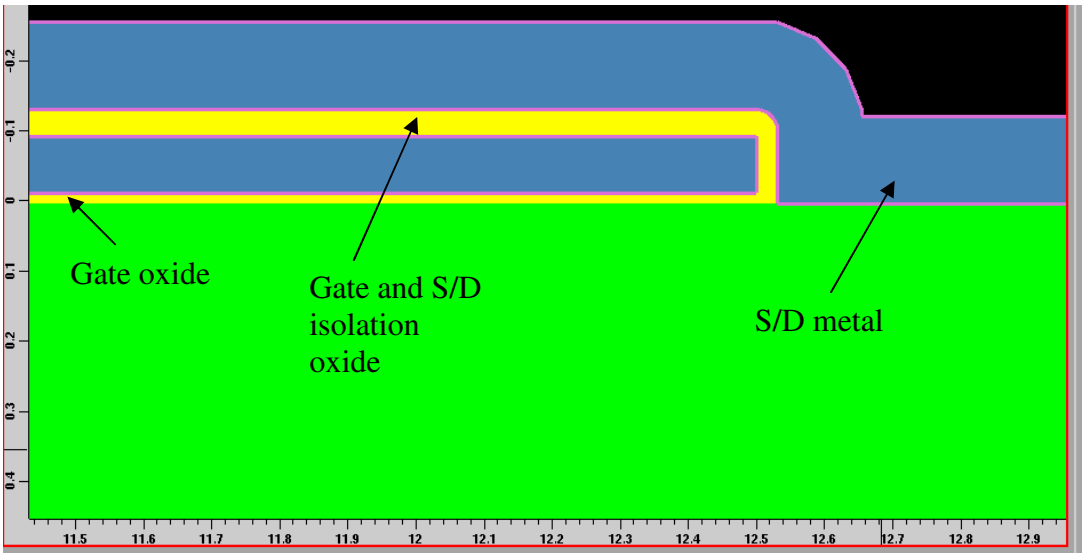
6.3 Device Simulation of Doping-Free MOSFET

The MOSFET structure developed in TSUPREM-4 is used in MEDICI for device simulation. The maximum number of nodes that can be implemented in MEDICI is 10,000. So, the structure is remeshed in MEDICI to provide enough nodes in the critical regions and fewer nodes deep in the bulk region. The barrier height is implemented by fixing the work function of the source/drain metal and the electron affinity of silicon. The doping concentration used is 10^{17} cm^{-3} and barrier height for the source/drain contact is 1.10 eV. Fermi-Dirac statistics is used to handle the degeneracy at the surface. Simulations were performed both for the doping-free MOSFET structure and the conventional MOSFET structure for a comparison purpose.

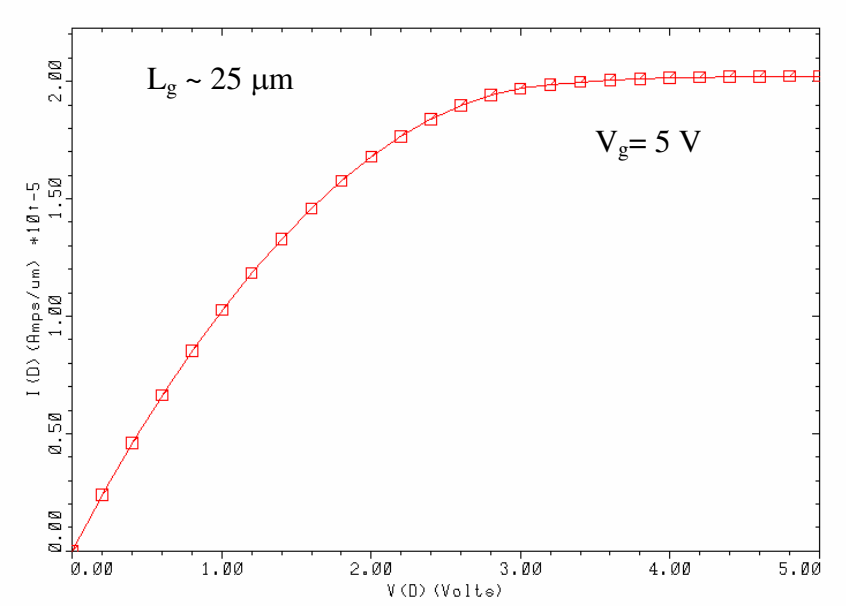
Figure 6.1(a) shows the TSUPREM-4 simulation of the doping-free MOSFET structure and Fig. 6.1(b) shows the MEDICI simulation of source/drain characteristics of this MOSFET. From Fig. 6.1(b) it is seen that the current drive is about 2×10^5 A/μm at 5 volts of gate and drain voltage. The gate length is taken as 25 μm to get a similar structure to the fabricated device.

Figure 6.2(a) shows the TSUPREM-4 simulation of the conventional equivalent MOSFET structure of the doping-free MOSFET and Fig. 6.2(b) shows the MEDICI simulation of source/drain characteristics of this MOSFET. From Fig. 6.2(b) it is found that the current drive of the doping-free MOSFET is equivalent to the conventional MOSFET.

So, in the case of the doping-free MOSFET, it has the advantages of simplicity in fabrication and large energy savings.

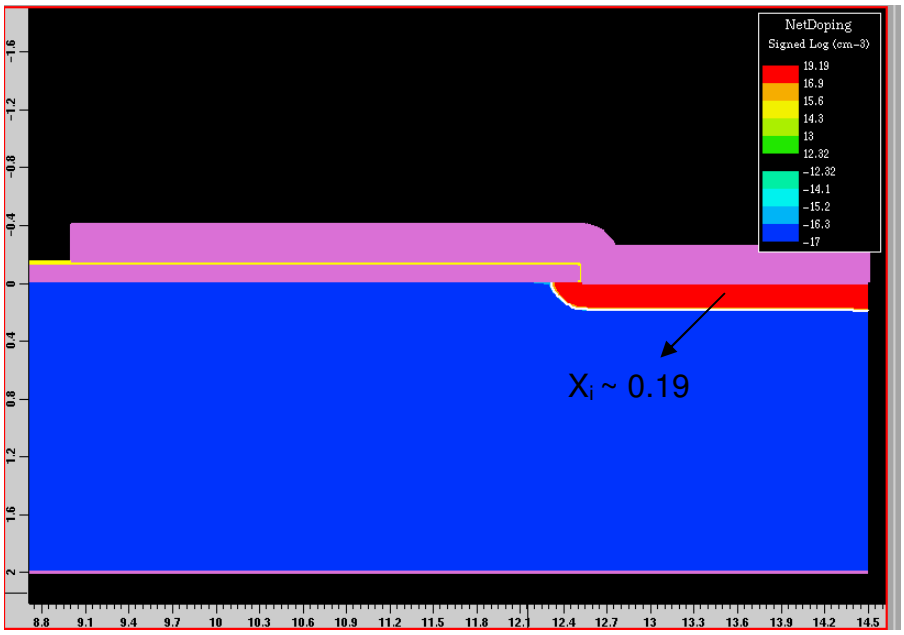


(a)

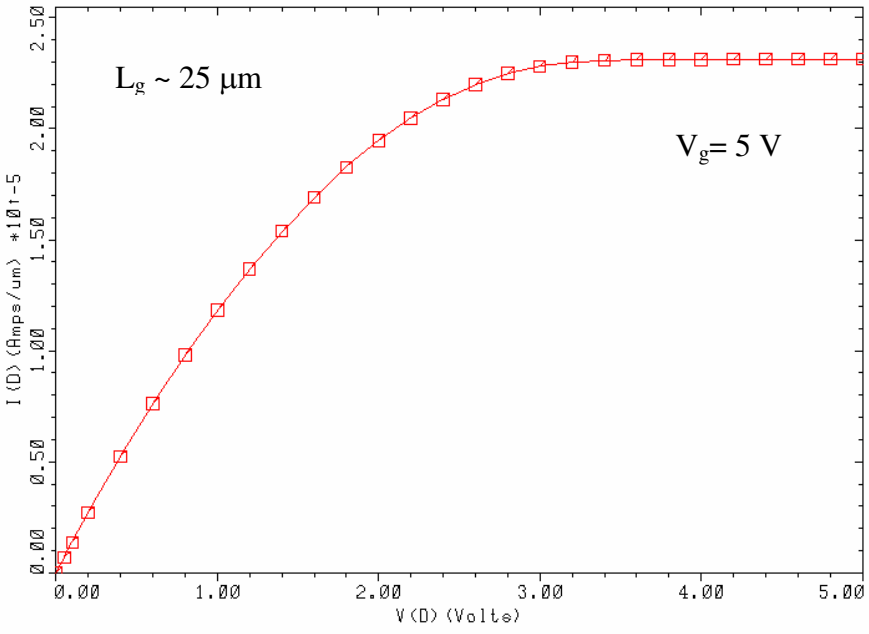


(b)

Figure 6.1 (a) TSUPREM-4 simulation for the doping-free MOSFET, (b) MEDICI simulation of the source/drain characteristics.



(a)



(b)

Figure 6.2 (a) TSUPREM-4 simulation for the conventional equivalent MOSFET, (b) MEDICI simulation of the source/drain characteristics.

6.4 Comparison with the Experimental Results

From the experimental results, it is found that current drive lower than the simulation results. So another simulation is performed to match the experimental results and it is found that a barrier height of the source/drain metal to p-type substrate is ~0.82 eV.

6.5 Summary

In this chapter, the proposed doping-free MOSFET structure is analyzed using 2-D process and device simulations. TSUPREM-4 is used for process simulation, and MEDICI is used for device simulation. It is found from the device simulation that the proposed doping-free MOSFET structure provides the same performance characteristics as the conventional MOSFET. However, the doping-free MOSFET has several advantages over its counterpart; simplicity in the process, low cost, and, best of all, reduction in maximum process temperature from 1000^{o} C to 500^{o} C. This gives a large energy saving in the processing of these MOSFETs.

CHAPTER 7

CONCLUSION

A new passivation technique has been developed for the passivation of Si(100) surface from a solution. The solution contains an etchant for SiO_2, NH_4OH, and a passivant, $(NH_4)_2S$. The compatibility of the etchant with the passivant allows SiO_2, native or thermal, to be removed in-situ. Thus a fresh, and clean Si(100) surface is exposed right before S passivation. Effects of passivation conditions on passivation quality, as monitored by the reverse saturation current of two back-to-back Al/Si Schottky diodes, are investigated, including passivation time, $(NH_4)_2S$ concentration, and $(NH_4)OH$ concentration. The effect of S passivation of the Si(100) surface, both n- and p-type, on Schottky barrier height has been investigated with low and high work-function metals, Al and Ni, respectively. It is found that S passivation of Si(100) reduces the density of surface states by more than an order of magnitude. This reduction in surface-state density results in changes in Schottky barrier height, which are more sensitive to the work function of the chosen metal. Aluminum, a low work function metal, shows a very low barrier height of <0.11 eV on S-passivated n-type Si(100) and a maximum barrier height of ~1.10 eV on S-passivated p-type Si(100), as compared to 0.56 eV and ~0.66 eV for non-passivated n- and p-type Si(100), respectively. Nickel, a high work function metal, shows ~0.75 eV and ~0.51 eV on S-passivated n- and p-type

Si(100), respectively, as compared to ~0.61 eV and ~0.54 eV on non-passivated n- and p-type Si(100), respectively. Ti and Cr show a barrier height of <0.17 eV and 0.32 eV on S-passivated n-type Si(100), as compared to 0.49 eV and 0.64 eV for non-passivated n-type Si(100) respectively. These experimental results suggest that surface states play the dominant role over surface dipole in controlling the Schottky barrier height in these metal-Si systems.

In this work a new energy efficient low-temperature doping-free MOSFET has also been proposed and fabricated. In a conventional MOSFET, the doping step(~1000^{o} C) is required to form the source/drain region, which is basically a p-n junction. But in the doping-free approach, the high-temperature doping step is replaced by more energy efficient low temperature process using S-passivation technique. From the experimental results, it is found that a very low work function metal (Al) on S-passivated p-type Si(100) yields a very high barrier height (~1.10 eV), which in turn causes degenerate inversion at surface. Due to this degenerate inversion, the surface acts like n-type and the bulk is p-type. Thus a p-n junction is formed without doping. In this process, the maximum process temperature is ~500^{o} C. Thus in this new doping-free approach, the maximum process temperature has been brought down from ~1000^{o} C to ~500^{o} C, which means a huge savings in terms of energy. 2-D device simulations show that doping-free MOSFET provide similar performance characteristics as in the case of a conventional MOSFET but with additional advantages like simplicity in process and huge savings in energy. A detailed description of the fabrication process is provided here along with the optimization of different process steps. The fabricated devices show

a maximum current drive of ~2×10^{-7} A/μm and low on/off ratio. This low current drive is related to the long gate length and the quality of passivation in the source/drain region. With the same gate length, 2-D device simulations show that in our fabricated device, the barrier height in the source/drain region is short of achieving the value(~1.10 eV) needed for good performance.

The quality of passivation is intimately related to the surface condition. In the fabrication of doping-free MOSFET, the source/drain region is exposed by doing the RIE (reactive ion etching) step for couple of times. This RIE badly damages the source/drain region of the silicon wafer. So, in order to get good quality passivation, either the silicon surface needs to be protected or the damaged surface needs to be removed, so that a clean and fresh surface is provided for S-passivation. In either case, thermal oxide can be used to do the work. However, to remove the thermal oxide, there should be very good selectivity between the thermal oxide, and the gate isolation oxide. Otherwise, during the process of removing the thermal oxide, the gate isolation oxide will be etched away and after the deposition of source/drain metal, the source/drain region will be shorted. In the case of CVD oxide, the etch rate in 2% HF is quite high compared to the thermal oxide, which was a major bottleneck in this fabrication process.

To avoid this bottleneck, silicon nitride (Si_3N_4) can be used instead of silicon dioxide (SiO_2). Silicon nitride (Si_3N_4) has a better selectivity [83] than silicon dioxide (thermal or CVD) in HF etchant. But due to the facility limitations, it could not be implemented here. Another thing that can be tried in future is the fabrication of p-

channel doping-free MOSFET. Though not very high barrier height is observed between metal and n-type Si(100), more research can be done to make further improvement. Further the process flow for the fabrication of doping-free MOSFET, as explained in chapter 5, is not self-aligned. One way to make it self-aligned is to use a process called chemical mechanical polishing (CMP) [84]. This process is complicated and has not been tried yet, but certainly it is worthy of investigation.

APPENDIX A

TSUPREM-4 CODES FOR THE PROCESS SIMULATION OF DOPING-FREE MOSFET

```
$ TSUPREM4 NMOS transistor simulation

$ Define the initial grid

MESH  GRID.FAC=.45

$ Read the mask definition file

MASK IN.FILE=mos25.tl1 PRINT GRID="Gate,SD_Metal,G_Contact"

$ Initialize the structure

INITIALIZE <100> BORON=1E17

$ GATE OXIDE FORMATION

DIFFUSION TIME=120 TEMP=850 DRY

$ GATE METAL DEPOSITION

DEPOSIT ALUMINUM THICKNESS=0.08

$ Oxide DEPOSITION FOR INSULATION

DEPOSIT OXIDE THICKNESS=.04

DEPOSIT PHOTORESIST POSITIVE THICKNESS=1

EXPOSE MASK=Gate

DEVELOP

$ PATTERN GATE

ETCH OXIDE TRAP

ETCH ALUMINUM TRAP

ETCH OXIDE TRAP

ETCH PHOTORESIST ALL

$ SPACER FORMATION
```

```
DEPOSIT OXIDE THICKNESS=.03

ETCH OXIDE  THICKNESS=.031

$ DEPOSIT S/D METAL

DEPOSIT ALUMINUM THICKNESS=0.125

DEPOSIT PHOTORESIST POSITIVE THICKNESS=1.0

EXPOSE MASK=SD_Metal

DEVELOP

ETCH ALUMINUM TRAP

ETCH PHOTORESIST ALL

$ OPENING OF GATE CONTACT

DEPOSIT PHOTORESIST NEGATIVE THICKNESS=1

EXPOSE MASK=G_Contact

DEVELOP

ETCH OXIDE TRAP

ETCH PHOTORESIST ALL

$SAVEFILE OUT.FILE=sbmos_out1

STRUCTURE REFLECT LEFT

STRUCTURE TRUNCATE BOTTOM Y=2

STRUCTURE TRUNCATE LEFT X=-14.5

STRUCTURE TRUNCATE RIGHT X=14.5

ELECTROD X=-13 NAME=S

ELECTROD X=13 NAME=D
```

```
ELECTROD X=0 NAME=G

ELECTROD BOTTOM NAME=B

SAVEFILE OUT.FILE=sbmos25_t_out MEDICI

SAVEFILE OUT.FILE=sbmos25_t_out.tif TIF

PLOT.2D SCALE X.MIN=-13 X.MAX=13 Y.MAX=3

$ Color fill the region

COLOR SILICON COLOR=3

COLOR OXIDE COLOR=1

COLOR NITRIDE COLOR=2

COLOR ALUM COLOR=4
```

APPENDIX B

MEDICI CODES FOR THE DEVICE SIMULATION OF DOPING-FREE MOSFET

```
$ IMPORT STRUCTURE FROM TSUPREM4 IN MEDICI
$ DEFINE ELECTRODE
MESH IN.FILE=sbmos25_t_out TSUPREM4
CONTACT NAME=S WORKFUNC=4.07 SURF.REC=1E12 ^PIN
CONTACT NAME=D WORKFUNC=4.07 SURF.REC=1E12 ^PIN
CONTACT NAME=G WORKFUNC=4.33 SURF.REC=1E12
CONTACT NAME=B WORKFUNC=5.15
MATERIAL SILICON AFFINITY=4.05 EG300=1.12
MODELS FERMIDIR QM.PHILI CONMOB SRH AUGER SBT
INTERFACE QF=1E11
$ DO A POISSON SOLVE ONLY TO BIAS GATE
SYMB CARRIERS=0
METHOD ICCG DAMPED
SOLVE V(G)=0
$REGRID POTENTIAL   RATIO=.3  smooth=1
REGRID ELECTRON LOG RATIO=2   smooth=1
SYMB CARRIERS=0
METHOD ICCG DAMPED
SOLVE V(G)=0
$REGRID POTENTIAL   RATIO=.3  smooth=1
REGRID ELECTRON LOG RATIO=2   smooth=1
SYMB CARRIERS=0
```

```
METHOD ICCG DAMPED

SOLVE V(G)=5

$ USE NEWTONS METHOD AND SOLVE FOR ELECTRON

SYMB NEWTON CARRIERS=1  ELECTRON

$SYMB NEWTON CARRIERS=2  ELECTRON HOLES

$ RAMP THE DRAIN

 SOLVE V(D)=0 ELEC=D VSTEP=.20 NSTEP=25

SAVEFILE OUT.FILE=sbmos25_med.tif TIF

$ PLOT Ids VS Vds

PLOT.1D Y.AXIS=I(D) X.AXIS=V(D) POINTS COLOR=2

+ TITLE=" DRAIN CHARACTERISTICS"
```

APPENDIX C

TSUPREM-4 CODES FOR THE PROCESS SIMULATION OF CONVENTIONAL MOSFET

```
$ TSUPREM4 NMOS transistor simulation
$ INITIAL GRID
MESH  GRID.FAC=.45
$ Read the mask definition file
MASK IN.FILE=mos25.tl1 PRINT GRID="Gate,SD_Metal,G_Contact"
$ Initialize the structure
INITIALIZE <100> BORON=1E17
$ GATE OXIDE FORMATION
DIFFUSION TIME=120 TEMP=850 DRY
$DIFFUSION TIME=40 TEMP=850 NITROGEN
$ GATE METAL DEPOSITION
DEPOSIT ALUMINUM THICKNESS=0.1
$ Oxide DEPOSITION FOR INSULATION
$DEPOSIT OXIDE THICKNESS=.04 SPACES=4
DEPOSIT PHOTORESIST POSITIVE THICKNESS=1
EXPOSE MASK=Gate
DEVELOP
$ PATTERN GATE
$ETCH OXIDE TRAP
ETCH ALUMINUM TRAP
ETCH OXIDE TRAP
ETCH PHOTORESIST ALL
```

```
DEPOSIT OXIDE THICKNESS=1 SPACES=4

DEPOSIT PHOTORESIST NEGATIVE THICKNESS=1.0

EXPOSE MASK=SD_Metal

DEVELOP

ETCH OXIDE THICKNESS=1

ETCH OXIDE

ETCH PHOTORESIST ALL

$ PRE DEPOSITION

DIFFUSION TIME=30 TEMP=1000 P=1E19

$DIFFUSION TIME=90 TEMP=1000 INERT

ETCH OXIDE

DEPOSIT OXIDE THICKNESS=.04

DEPOSIT PHOTORESIST POSITIVE THICKNESS=1

EXPOSE MASK=Gate

DEVELOP

$ PATTERN OXIDE

ETCH OXIDE TRAP

ETCH PHOTORESIST ALL

$ SPACER FORMATION

DEPOSIT OXIDE THICKNESS=.03 SPACES=2

ETCH OXIDE  THICKNESS=.03

$ DEPOSIT S/D METAL
```

```
DEPOSIT ALUMINUM THICKNESS=0.25

DEPOSIT PHOTORESIST POSITIVE THICKNESS=1.0

EXPOSE MASK=SD_Metal

DEVELOP

ETCH ALUMINUM TRAP

ETCH PHOTORESIST ALL

$ OPENING OF GATE CONTACT

DEPOSIT PHOTORESIST NEGATIVE THICKNESS=1

EXPOSE MASK=G_Contact

DEVELOP

ETCH OXIDE TRAP

ETCH PHOTORESIST ALL

STRUCTURE REFLECT LEFT

STRUCTURE TRUNCATE BOTTOM Y=2

STRUCTURE TRUNCATE LEFT X=-14.5

STRUCTURE TRUNCATE RIGHT X=14.5

ELECTROD X=-13 NAME=S

ELECTROD X=13 NAME=D

ELECTROD X=0 NAME=G

ELECTROD BOTTOM NAME=B

SAVEFILE OUT.FILE=mos_t_out25 MEDICI

SAVEFILE OUT.FILE=mos_t_out25.tif TIF
```

```
PLOT.2D SCALE X.MIN=0 X.MAX=7 Y.MAX=.25

$ Color fill the region

COLOR SILICON COLOR=3

COLOR OXIDE COLOR=1

COLOR NITRIDE COLOR=2

COLOR ALUM COLOR=4
```

APPENDIX D

MEDICI CODES FOR THE DEVICE SIMULATION OF CONVENTIONAL MOSFET

```
$ IMPORT STRUCTURE FROM TSUPREM4 IN MEDICI
$ DEFINE ELECTRODE
$MESH IN.FILE=mos_t_out25 TSUPREM4
MESH IN.FILE=mos_t_out25.tif TIF ABC JUNC.ABC
+  ^GRIDTOP ^RFN.CRNR
ABC.MESH BOUNDARY REGION1=Silicon1 REGION2= Silicon1
+ X.MAX=-12.30 GRDLEFT H1=0.015 H2=0.1
ABC.MESH BOUNDARY REGION1=Silicon1 REGION2= Oxide1
+ X.MAX=-12.30 GRDLEFT H1=0.02 H2=0.02
ABC.MESH BOUNDARY REGION1=Silicon1 REGION2= Oxide1
+ X.MIN=-12.30 GRDRIGHT H1=0.2 H2=0.2
ABC.MESH BOUNDARY REGION1=Silicon1 REGION2= Silicon1
+ X.MIN=12.30 GRDRIGHT H1=0.015 H2=0.1
ABC.MESH BOUNDARY REGION1=Silicon1 REGION2= Oxide1
+ X.MIN=12.30 GRDRIGHT H1=0.02 H2=0.02
ABC.MESH OXIDE NORMAL=.1
ABC.MESH REGION=Silicon1 NORMAL=0.001
ABC.MESH REGION=Silicon1 Y.MIN=.15 NORMAL=0.01
CONTACT NAME=S WORKFUNC=4.07 SURF.REC=1E12 ^PIN
CONTACT NAME=D WORKFUNC=4.07 SURF.REC=1E12 ^PIN
CONTACT NAME=G WORKFUNC=4.33 SURF.REC=1E12
CONTACT NAME=B WORKFUNC=5.15
```

```
MATERIAL SILICON AFFINITY=4.05 EG300=1.12
MODELS FERMIDIR QM.PHILI HPMOB SRH AUGER SBT
INTERFACE QF=1E10
$ DO A POISSON SOLVE ONLY TO BIAS GATE
$SYMB CARRIERS=0
$METHOD ICCG DAMPED
$SOLVE V(G)=0
SYMB CARRIERS=0
METHOD ICCG DAMPED
SOLVE V(G)=5
$ USE NEWTONS METHOD AND SOLVE FOR ELECTRON
SYMB NEWTON CARRIERS=1  ELECTRON
$SYMB NEWTON CARRIERS=2  ELECTRON HOLES
$ RAMP THE DRAIN
 SOLVE V(D)=0 V(B)=0 ELEC=D VSTEP=.20 NSTEP=25
SAVEFILE OUT.FILE=mos25_med.tif TIF
$ PLOT Ids VS Vds
PLOT.1D Y.AXIS=I(D) X.AXIS=V(D) POINTS COLOR=2
+ TITLE=" DRAIN CHARACTERISTICS"
```

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